1A Low Noise, Buck-Boost DC/DC Converter

FEATURES

- **Regulated Output with Input Voltage Above, Below or Equal to the Output Voltage**
- **1.8V to 5.5V Input and Output Voltage Range**
- **1A Continuous Output Current for $V_{IN} \geq 3V$, $V_{OUT} = 3.3V$**
- **±1% Output Voltage Accuracy**
- Low Noise Buck-Boost Architecture
- Up to 95% Efficiency
- Programmable Frequency from 300kHz to 2MHz
- Synchronizable Oscillator
- Burst Mode® Operation: 32µA I_Q
- Internal 1ms Soft-Start
- Output Disconnect in Shutdown
- Shutdown Current: 1µA
- Short-Circuit Protection
- Small Thermally Enhanced 12-Pin MSOP and 10-Pin (3mm × 3mm) DFN Packages

APPLICATIONS

- Wireless Inventory Terminals
- Handheld Medical Instruments
- Wireless Locators, Microphones
- Supercapacitor Backup Power Supply

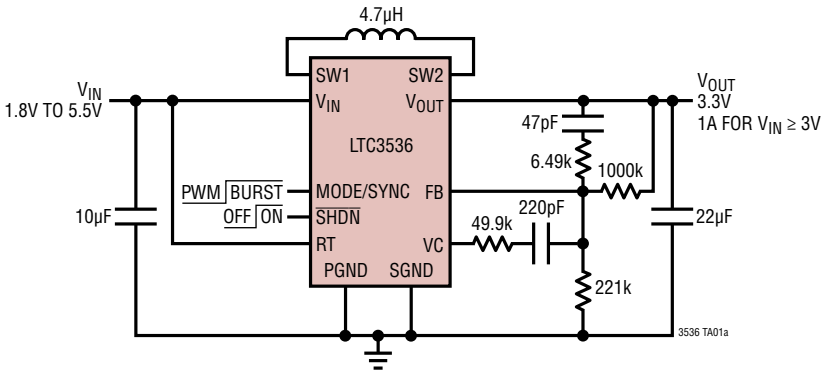
DESCRIPTION

The LTC®3536 is an extended V_{IN} range, fixed frequency, synchronous buck-boost DC/DC converter that operates from input voltages above, below or equal to the regulated output voltage. The topology incorporated in the LTC3536 provides low noise operation, making it ideal for RF and precision measurement applications.

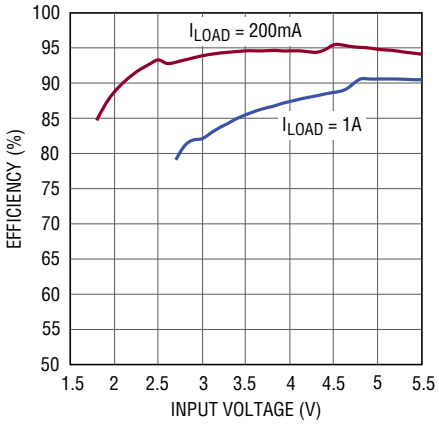
The device can produce up to 1A of continuous output current, and it includes two N-channel and two P-channel MOSFET switches. Switching frequencies up to 2MHz can be programmed with an external resistor and the oscillator can be synchronized to an external clock. Quiescent current is only 32µA in Burst Mode operation, maximizing battery life in portable applications. Burst Mode operation is user controlled and improves efficiency at light loads.

Other features include a 1µA shutdown current, internal soft-start, overtemperature protection and current limit. The LTC3536 is available in 12-pin thermally enhanced MSOP and 10-pin (3mm × 3mm) DFN packages.

TYPICAL APPLICATION



Efficiency vs Input Voltage



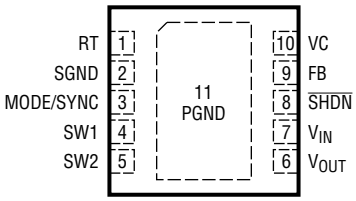
3536 TA01b

ABSOLUTE MAXIMUM RATINGS (Note 1)

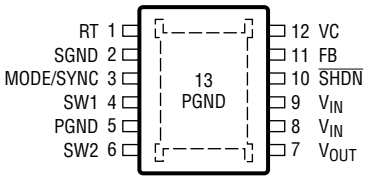
V_{IN}, V_{OUT}, (SV_{IN}, PV_{IN}) Voltage ..... –0.3V to 6V
SW1, SW2 Voltage
DC ..... –0.3V to 6V
Pulsed (<100ns) ..... –1.0V to 7V
VC, RT, FB, $\overline{SHDN}$ Voltage ..... –0.3V to 6V
MODE/SYNC Voltage ..... –0.3V to 6V

Operating Junction Temperature Range
(Notes 2, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSE ..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 39.7°C/W
EXPOSED PAD (PIN 11) IS PGND, MUST BE SOLDERED TO PCB



MSE PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 13) IS PGND MUST BE SOLDERED TO PCB
FOR RATED THERMAL PERFORMANCE AND LOAD REGULATION

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3536EDD#PBF	LTC3536EDD#TRPBF	LFZD	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3536IDD#PBF	LTC3536IDD#TRPBF	LFZD	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3536EMSE#PBF	LTC3536EMSE#TRPBF	3536	12-Lead Plastic MSOP	–40°C to 125°C
LTC3536IMSE#PBF	LTC3536IMSE#TRPBF	3536	12-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 3.3V, V_{OUT} = 3.3V, R_T = 100kΩ unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Operating Range		●	1.8		5.5	V
Output Voltage Adjust Range		●	1.8		5.5	V
Undervoltage Lockout Threshold	V_{IN} Ramping Down V_{IN} Ramping Up	● ●	1.6	1.67 1.75	 1.8	V V
Feedback Voltage	0°C < T_J < 85°C (Note 5) –40°C < T_J < 125°C	 ●	0.594 0.591	0.6 0.6	0.606 0.609	V V
Feedback Pin Input Current (FB)	V_{FB} = 0.6V in Servo Loop, $V_{MODE/SYNC}$ = 0V				50	nA
Quiescent Current, Burst Mode Operation	V_{FB} = 0.7V, $V_{MODE/SYNC}$ = V_{IN}			32	42	µA
Quiescent Current, Shutdown (I_{VIN})	$V_{\overline{SHDN}}$ = 0V			0.1	1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 3.3V, V_{OUT} = 3.3V, R_T = 100kΩ unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Current, Active (I_{VIN})	V_{FB} = 0.7V, $V_{MODE/SYNC}$ = 0V				800	µA
Input Current Limit	$V_{MODE/SYNC}$ = 0V (Note 4)	●	2	2.5		A
Peak Current Limit	$V_{MODE/SYNC}$ = 0V (Note 4)			3.4	4	A
Burst Mode Peak Current Limit	$V_{MODE/SYNC}$ = V_{IN} (Note 4)		0.4	0.6		A
Reverse Current Limit	(Note 4)	●	0.3	0.55		A
NMOS Switch Leakage	Switch B, C: SW1 = SW2 = 5.5V, V_{IN} = 5.5V, V_{OUT} = 5.5V			0.1	1	µA
PMOS Switch Leakage	Switch A, D: SW1 = SW2 = 0V, V_{IN} = 5.5V, V_{OUT} = 5.5V			0.1	1	µA
NMOS Switch On-Resistance	Switch B (From SW1 to GND) (Note 6) Switch C (From SW2 to GND) (Note 6)			0.11 0.1		Ω Ω
PMOS Switch On-Resistance	Switch A (From V_{IN} to SW1) (Note 6) Switch D (From V_{OUT} to SW2) (Note 6)			0.12 0.145		Ω Ω
Frequency Accuracy	R_T = 100k	●	0.8	1	1.2	MHz
Frequency Accuracy Default	R_T = V_{IN}	●	0.96	1.2	1.44	MHz
Internal Soft-Start Time	V_{FB} from 0.06V to 0.54V		0.6	0.9	1.2	ms
Maximum Duty Cycle	Percentage of Period SW2 is Low in Boost Mode	●	88	91		%
Minimum Duty Cycle	Percentage of Period SW1 is High in Buck Mode	●			0	%
Error Amplifier AVOL				90		dB
Error Amplifier Sink Current	FB = 1.3V, VC = 1V		250	300		µA
Error Amplifier Source Current	FB = 0.3V, VC = 0V		400	480		µA
MODE/SYNC Input Logic Threshold	Disable Burst Mode Operation		0.3		1	V
MODE/SYNC External Synchronization	SYNC Level High SYNC Level Low	● ●	1.2		 0.4	V V
MODE/SYNC Synchronization Frequency		●	0.3		2	MHz
MODE/SYNC Input Current	$V_{MODE/SYNC}$ = 5.5V = V_{IN}				1	µA
$\overline{SHDN}$ Input Logic Threshold		●	0.3		1	V
$\overline{SHDN}$ Input Current	$V_{\overline{SHDN}}$ = 5.5V = V_{IN}				1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3536 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3536E is guaranteed to meet specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3536I is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}),$$

where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: Current measurements are performed when the LTC3536 is not switching. The current limit values measured in operation will be somewhat higher due to the propagation delay of the comparators.

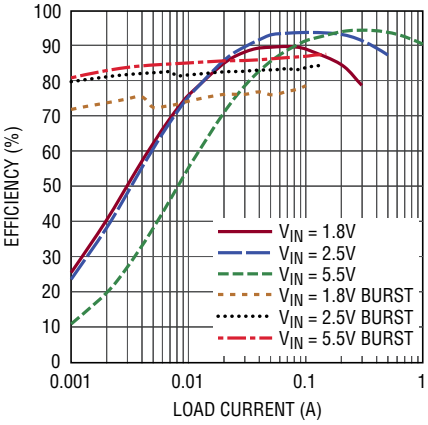
Note 5: Guaranteed by design characterization and correlation with statistical process controls.

Note 6: Guaranteed by correlation and design.

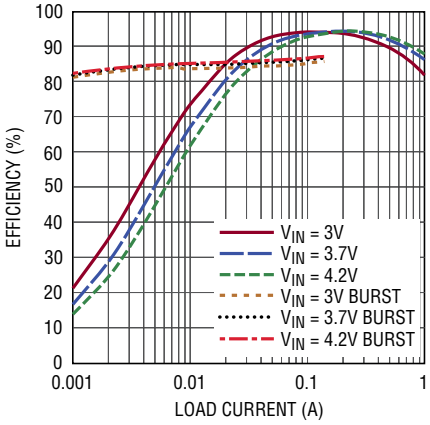
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = V_{OUT} = 3.3 V unless otherwise noted.

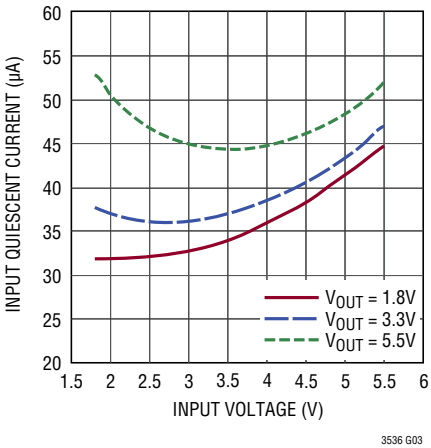
Efficiency 3.3V vs Load Current



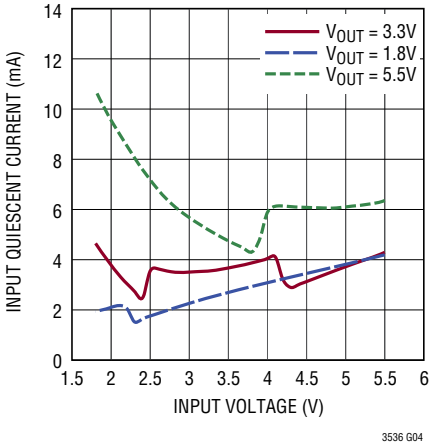
Efficiency Li-Ion (3V, 3.7V, 4.2V) to 3.3V Output



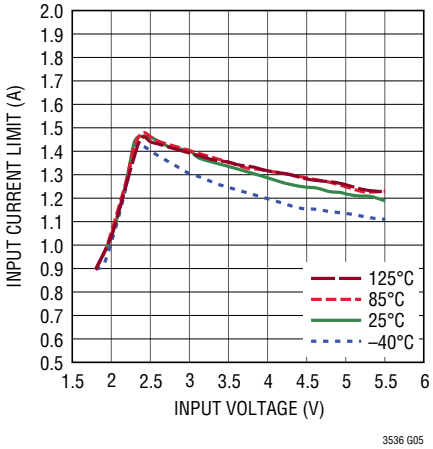
No-Load Quiescent Current in Burst Mode Operation (MODE = V_{IN})



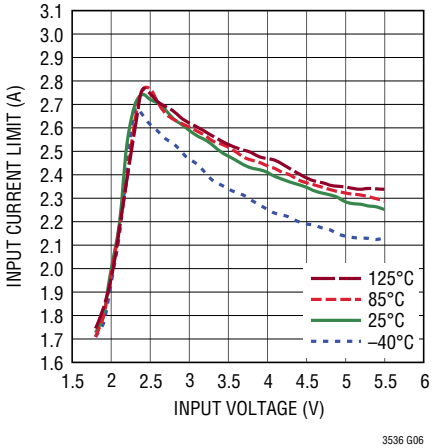
No-Load Quiescent Current in PWM Mode Operation



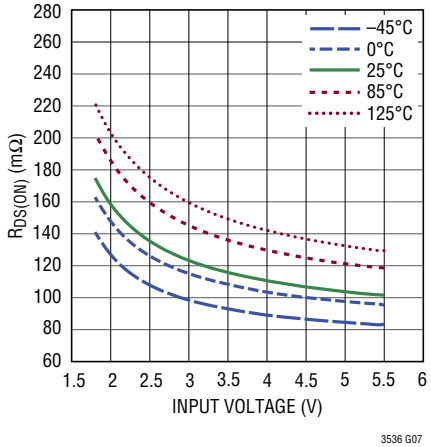
Input Current Limit vs Supply Voltage, V_{OUT} = GND



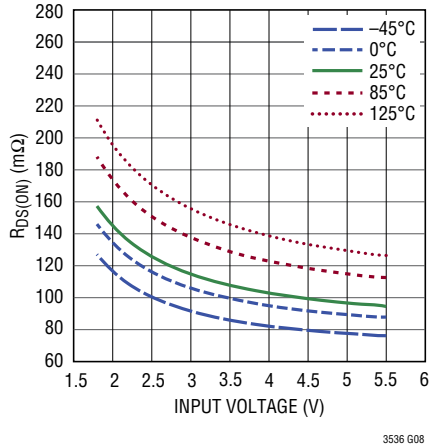
Input Current Limit vs Supply Voltage, V_{OUT} = 3.3V



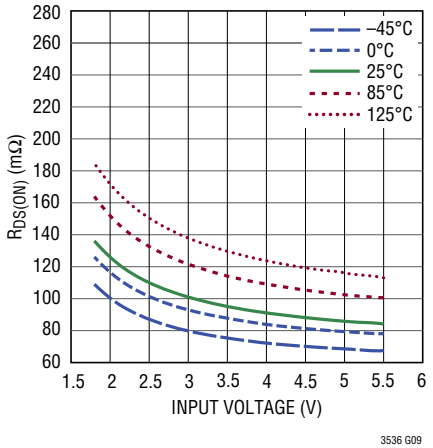
$R_{DS(ON)}$ for P-Channel Switch A



$R_{DS(ON)}$ for N-Channel Switch B



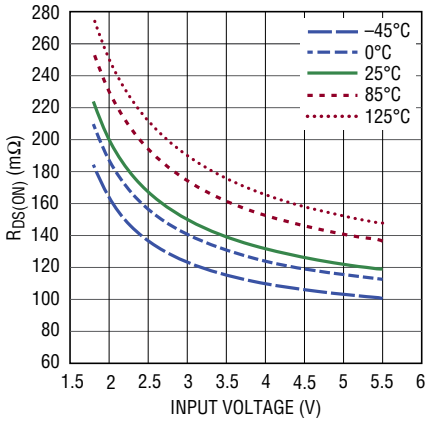
$R_{DS(ON)}$ for N-Channel Switch C



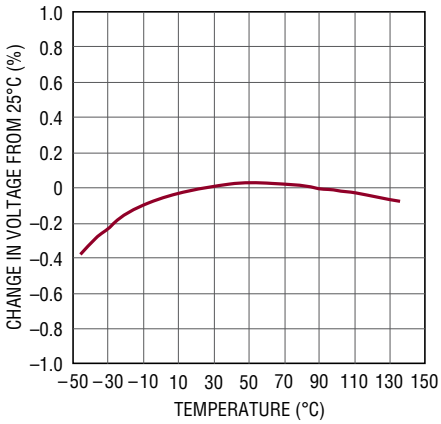
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = V_{OUT} = 3.3 V unless otherwise noted.

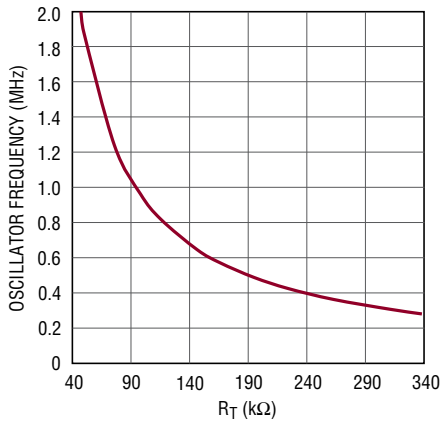
$R_{DS(ON)}$ for P-Channel Switch D



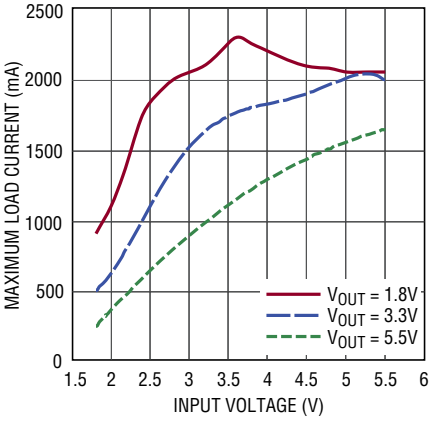
Feedback Voltage



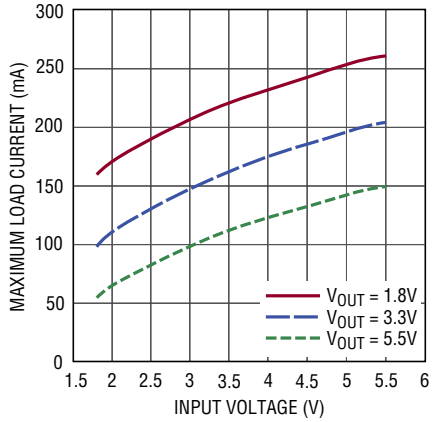
Oscillator Frequency vs R_T



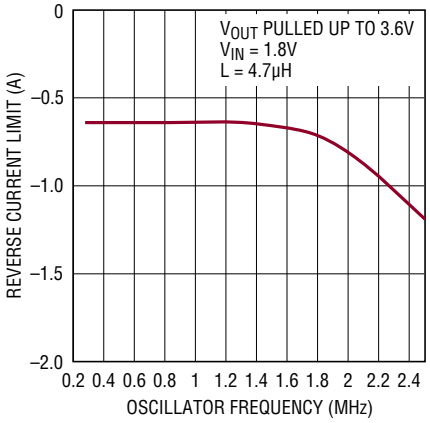
Maximum Load Current in PWM Mode vs Input Voltage 1MHz Switching Frequency, 4.7µH Inductor Value



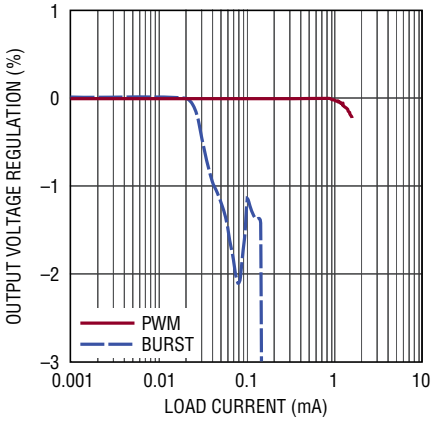
Maximum Load Current in Burst Mode Operation vs Input Voltage



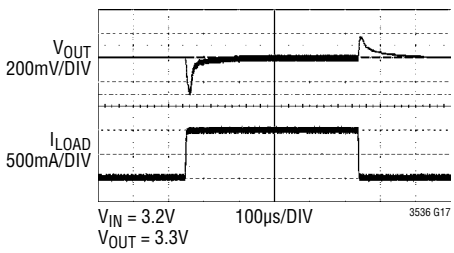
Negative Inductor Current vs Oscillator Frequency



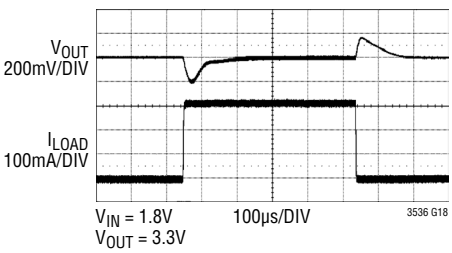
Change in Output Voltage vs Load Current for 3.3V Output and 3.3V Input



Load Step 0A to 1A



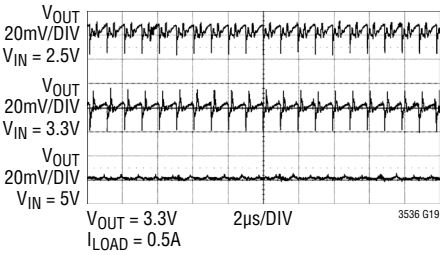
Load Step 0mA to 300mA



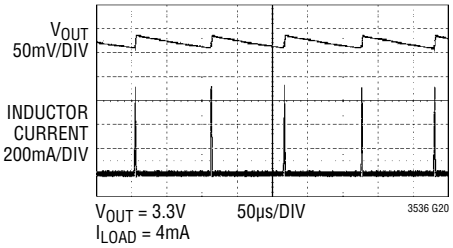
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = V_{OUT} = 3.3 V unless otherwise noted.

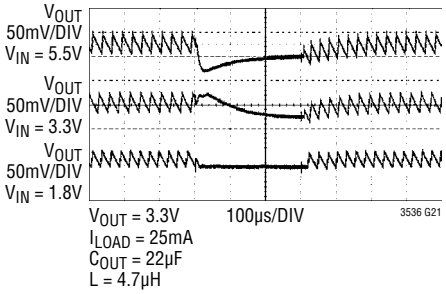
Output Voltage Ripple in PWM Mode



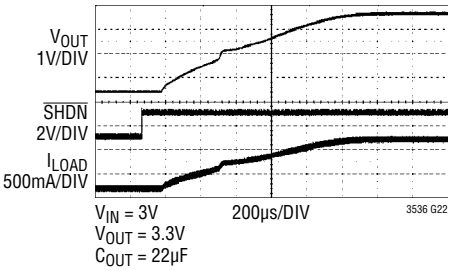
Output Voltage Ripple in Burst Mode Operation



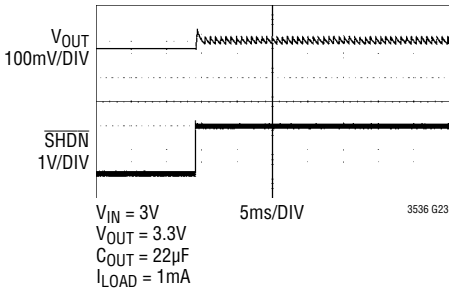
Burst Mode Operation to PWM Mode Transient



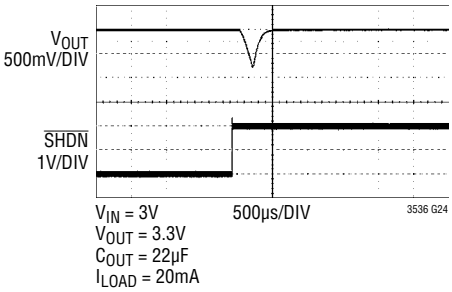
Soft-Start



Start-Up in Burst Mode Operation with Output Precharged



Start-Up in PWM Mode Operation with Output Precharged



PIN FUNCTIONS (DFN/MSOP)

RT (Pin 1/Pin 1): Oscillator Frequency Programming Input. Connect a resistor from RT to GND to program the internal oscillator frequency. The frequency is given by:

$$f_{OSC}\ (MHz) = 100/R_T\ (k\Omega)$$

where R_T is in kΩ and f_{OSC} is between 0.3MHz and 2MHz. Tying the RT pin to V_{IN} enables the internal 1.2MHz default oscillator frequency.

SGND (Pin 2/Pin 2): Ground Connection for the LTC3536. A ground plane is highly recommended. Sensitive analog components terminated at ground should connect to the GND pin with a Kelvin connection, separated from the high current path.

MODE/SYNC (Pin 3/Pin 3): Pulse Width Modulation/Burst Mode Selection and Synchronization Input. Driving MODE to a logic 0 state programs fixed frequency, low noise PWM operation. Driving MODE to logic 1 state programs Burst Mode operation for highest efficiency at light loads. In Burst Mode operation, the output current capability is significantly less than what is available in PWM operation. Refer to the Applications Information section of this data sheet for details. Frequency synchronization is achieved if a clock pulse is applied to MODE/SYNC. The external clock pulse amplitude must have an amplitude equal or higher than 1.2V and duty cycle from 10% and 90%. The free-running frequency of the LTC3536 oscillator can be programmed slower or faster than the synchronization clock frequency.

SW1 (Pin 4/Pin 4): Switch Pin. Connect to internal power switches A and B. Connect one side of the buck-boost inductor to SW1. Provide a short wide PCB trace from the inductor to SW1 to minimize voltage transients and noise.

SW2 (Pin 5/Pin 6): Switch Pin. Connect to internal power switches C and D. Connect one side of the buck-boost inductor to SW2. Provide a short wide PCB trace from the inductor to SW2 to minimize voltage transients and noise.

V_{OUT} (Pin 6/Pin 7): Output Voltage. This pin is the power output for the regulator. A low ESR capacitor should be placed between this pin and the ground plane. The capacitor should be placed as close to this pin as possible and have a short return path to ground.

V_{IN} (Pin 7/Pins 8, 9): Power Input for the Converter. A low ESR 10µF or larger bypass capacitor should be connected between this pin and ground. The capacitor should be placed as close to this pin as possible and have a short return path to ground.

$\overline{SHDN}$ (Pin 8/Pin 10): Enable Input. A logic 1 on $\overline{SHDN}$ activates the buck-boost regulator. A logic 0 on $\overline{SHDN}$ deactivates the buck-boost regulator.

FB (Pin 9/Pin 11): Output Voltage Programming Feedback Divider Input. The regulator output voltage is programmed by the voltage divider connected to FB. The buck-boost output is given by the following equation:

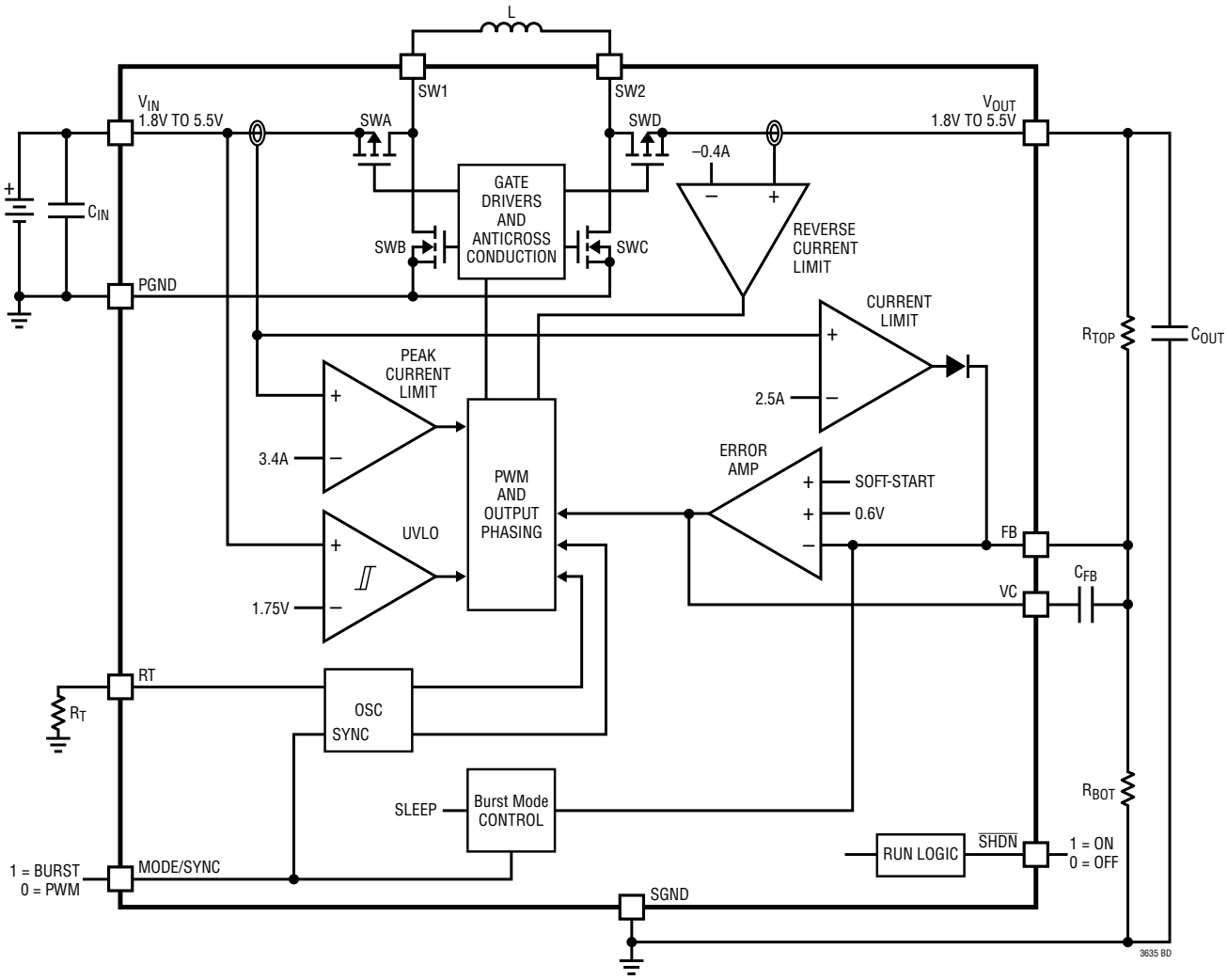
$$V_{OUT} = 0.6V \bullet (1 + R_{TOP}/R_{BOT})\ (V)$$

where R_{BOT} is a resistor connected between FB and ground and R_{TOP} is a resistor connected between FB and V_{OUT}. The buck-boost output voltage can be adjusted from 1.8V to 5.5V.

VC (Pin 10/Pin 12): Error Amplifier Output. Frequency compensation components are connected between VC and FB to provide stable operation of the converter. Refer to the Applications Information section of this data sheet for design details.

PGND (Exposed Pad Pin 11/Pin 5, Exposed Pad Pin 13): Power Ground. The exposed pad must be soldered to the PCB and electrically connected to ground through the shortest and lowest impedance connection possible.

BLOCK DIAGRAM



OPERATION

INTRODUCTION

The LTC3536 is a monolithic buck-boost converter that can operate with input and output voltages from as low as 1.8V to as high as 5.5V. A proprietary switch control algorithm allows the buck-boost converter to maintain output voltage regulation with input voltages that are above, below or equal to the output voltage. Transitions between these operating modes are seamless and free of transients and subharmonic switching.

The LTC3536 can be configured to operate over a wide range of switching frequencies, from 300kHz to 2MHz, allowing applications to be optimized for board area and efficiency. The LTC3536 has an internal fixed-frequency oscillator with a switching frequency that is easily set by a single external resistor. In noise sensitive applications, the converter can also be synchronized to an external clock via the MODE/SYNC pin. The operating frequency defaults to 1.2MHz when RT is connected to V_{IN} eliminating the external resistor.

The LTC3536 has been optimized to reduce input current in shutdown and standby for applications that are sensitive to quiescent current draw, such as battery-powered devices. In Burst Mode operation, the no-load standby current is only 32µA and in shutdown the total supply current is reduced to less than 1µA.

PWM MODE OPERATION

With the MODE/SYNC pin forced low or driven by an external clock, the LTC3536 operates in a fixed-frequency pulse-width modulation (PWM) mode using a voltage mode control loop. This mode of operation maximizes the output current that can be delivered by the converter, reduces output voltage ripple, and yields a low noise fixed-frequency switching spectrum. A proprietary switching algorithm provides seamless transitions between operating modes and eliminates discontinuities in the average inductor current, inductor current ripple, and loop transfer function throughout all regions of operation. These advantages result in increased efficiency, improved loop stability, and lower output voltage ripple in comparison to the traditional 4-switch buck-boost converter.

Figure 1 shows the topology of the LTC3536 power stage which is comprised of two P-channel MOSFET switches and two N-channel MOSFET switches and their associated gate drivers. In response to the error amplifier output, an internal pulse-width modulator generates the appropriate switch duty cycles to maintain regulation of the output voltage.

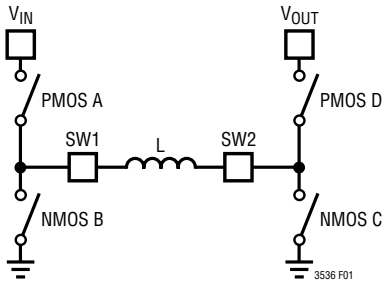


Figure 1. Power Stage Schematic

When the input voltage is significantly greater than the output voltage, the buck-boost converter operates in buck mode. Switch D turns on continuously and switch C remains off. Switch A and B are pulse-width modulated to produce the required duty cycle to support the output regulation voltage. As the input voltage decreases, switch A remains on for a larger portion of the switching cycle. When the duty cycle reaches approximately 90% the switch pair AC begins turning on for a small fraction of the switching period. As the input voltage decreases further, the AC switch pair remains on for longer durations and the duration of the BD phase decreases proportionally. At this point, switch A remains on continuously while switch pair CD is pulse-width modulated to obtain the desired output voltage. At this point, the converter is operating solely in boost mode.

Oscillator and Phase-Locked Loop

The LTC3536 operates from an internal oscillator with a switching frequency that can be configured by a single external resistor between RT and ground. Tying RT to V_{IN} sets the default internal operating frequency to typically 1.2MHz. If the RT pin is driven externally to a level higher than V_{IN}, a current limiting resistor should be used. 1M for 6V on the RT pin limits the current to 6µA. Also, a Schottky

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diode from the RT pin to V_{IN} can be used in addition to current limiting resistor. For noise sensitive applications, an internal phase-locked loop allows the LTC3536 to be synchronized to an external clock signal applied to the MODE/SYNC pin. The free-running frequency of the oscillator can be programmed slower or faster than the synchronization clock frequency.

Whether operating from its internal oscillator or when synchronized to an external clock signal, the LTC3536 is able to operate with a switching frequency from 300kHz to 2MHz, providing the ability to minimize the size of the external components and optimize the power conversion efficiency.

Error Amplifier

The LTC3536 has an internal high gain operational amplifier which provides frequency compensation of the control loop that maintains output voltage regulation. To ensure stability of this control loop, an external compensation network must be installed in the application circuit. A Type III compensation network as shown in Figure 2 is recommended for most applications since it provides the flexibility to optimize the converter's transient response while simultaneously minimizing any DC error in the output voltage. Details on designing the compensation network in LTC3536 applications can be found in the Applications Information section of this data sheet.

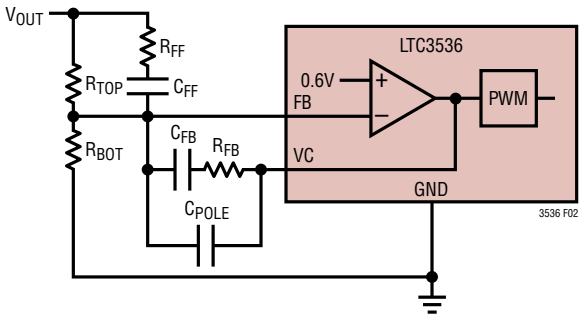

Figure 2. Error Amplifier and Compensation Network

Input and Peak Current Limits

The LTC3536 has two current limit circuits that are designed to limit the peak inductor current to ensure that the switch currents remain within the capabilities of the IC during output short-circuit or overload conditions. The input current limit operates by injecting a current into the feedback pin, which is proportional to the extent that the inductor current exceeds the input current limit threshold (typically 2.5A). Due to the high gain of the feedback loop, this injected current forces the error amplifier output to decrease until the average current through the inductor is approximately reduced to the current limit threshold. For this current limit feature to be most effective, the Thevenin resistance (R_{BOT}//R_{TOP}) from FB to ground should exceed 100kΩ.

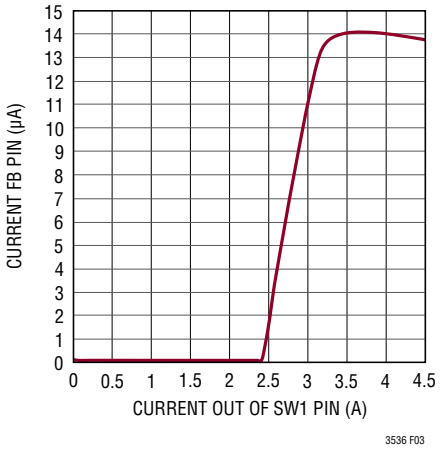

Figure 3. FB Current for Input Current Limitation

Since this input current limit circuit maintains the error amplifier in an active state it ensures a smooth recovery and minimal overshoot once the current limit fault condition is removed. On a hard output short, it is possible for the inductor current to increase substantially beyond the current limit threshold before the input current limit has time to react and reduce the inductor current. For this reason, there is a second current limit circuit (peak current limit), which turns off power switch A if the current through switch A exceeds the approximately 3.4A limit threshold. This provides additional protection in the case of an instantaneous hard output short and provides time for the primary current limit to react. When the input voltage is lower than 2.4V, the input and peak current limit thresholds are gradually decreased. For minimum input voltage (1.8V) they are typically 1.7A and 2.3A respectively. See the Typical Performance Characteristics and the Inductor Selection section for information about the inductor value for maximum output current capability.

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Reverse Current Limit

In PWM mode operation the LTC3536 has the ability to actively conduct current away from the output if that is necessary to maintain regulation. If the output is held above regulation, this could result in large reverse currents. This situation can occur if the output of the LTC3536 is held up momentarily by another supply as may occur during a power-up or power-down sequence. To prevent damage to the part under such conditions, the LTC3536 has a reverse current comparator that monitors the current entering power switch D from the load. If this current exceeds 0.55A (typical) switch D is turned off for the remainder of the switching cycle in order to prevent the reverse inductor current from reaching unsafe levels.

For no-load current application, the inductor current ripple must be lower than double the minimum reverse current limit (0.3A • 2 = 0.6A maximum inductor current ripple). See the Inductor Selection section for information about how to calculate the inductor current ripple.

Output Current Capability

The maximum output current that can be delivered by the LTC3536 is dependent upon many factors, the most significant being the input and output voltages. For V_{OUT} = 3.3V and $V_{IN} \geq$ 3V, the LTC3536 is able to support a 1A load continuously. For V_{OUT} = 3.3V and V_{IN} =1.8V, the LTC3536 is able to support a 300mA load continuously.

Typically, the output current capability is greatest when the input voltage is approximately equal to the output voltage. At larger step-up voltage ratios, the output current capability is reduced because the lower duty cycle of switch D results in a larger inductor current being needed to support a given load. Additionally, the output current capability generally decreases at large step-down voltage ratios due to higher inductor current ripple which reduces the maximum attainable inductor current.

The output current capability can also be affected by inductor characteristics. An inductor with large DC resistance will degrade output current capability, particularly in boost mode operation. In addition, larger value inductors generally maximize output current capability by reducing inductor current ripple. See the Typical Performance Characteristics and the Inductor Selection section for information.

Burst Mode OPERATION

When MODE/SYNC is held high, the buck-boost converter operates in Burst Mode operation using a variable frequency switching algorithm that minimizes the no-load input quiescent current and improves efficiency at light load by reducing the amount of switching to the minimum level required to support the load. The output current capability in Burst Mode operation is substantially lower than in PWM mode and is intended to support light stand-by loads. Curves showing the maximum Burst Mode load current as a function of the input and output voltage can be found in the Typical Performance Characteristics section of this data sheet. If the converter load in Burst Mode operation exceeds the maximum Burst Mode current capability, the output will lose regulation.

Each Burst Mode cycle is initiated when switches A and C turn on producing a linearly increasing current through the inductor. When the inductor current reaches the Burst Mode peak current limit (0.6A typically), switches B and D are turned on, discharging the energy stored in the inductor into the output capacitor and load. Once the inductor current reaches zero, all switches are turned off and the cycle is complete. Current pulses generated in this manner are repeated as often as necessary to maintain regulation of the output voltage. In Burst Mode operation, the error amplifier is used as burst comparator. If the MODE pin is driven externally to a level higher than V_{IN}, a current limiting resistor should be used. 1M for 6V on the MODE pin limits the current to 6µA. Also, a Schottky diode from the MODE pin to V_{IN} can be used in addition to current limiting resistor.

SOFT-START

To minimize input current transients on power-up, the LTC3536 incorporates an internal soft-start circuit with a nominal duration of 0.9ms. The soft-start is implemented by a linearly increasing ramp of the error amplifier reference voltage during the soft-start duration. As a result, the duration of the soft-start period is largely unaffected by the size of the output capacitor or the output regulation voltage. Given the closed-loop nature of the soft-start implementation, the converter is able to respond to load transients that occur during the soft-start interval. The

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soft-start period is reset by thermal shutdown and UVLO events on V_{IN} and the mode of operation is always PWM.

In case the output voltage at start -up is already precharged above 90% (typically) of the target value, the internal soft-start is skipped and the LTC3536 immediately enters the mode of operation that has been set on the MODE pin.

If the MODE pin is tied high and Burst Mode operation is selected, the output voltage is regulated smoothly to the target voltage value. Instead if the MODE pin is tied low and PWM mode is selected, the error amplifier needs to charge up the VC pin and the output voltage might be pulled to lower voltage values for a short period of time, proportional to the value of the main compensation capacitor.

UNDERVOLTAGE LOCKOUT

To ensure proper operation, the LTC3536 incorporates internal undervoltage lockout (UVLO) circuitry. The converter is disabled if V_{IN} falls below its respective UVLO threshold (typical 1.67V). If the input voltage falls below this level all switching is disabled until the input voltage rises above 1.75V (nominal).

OUTPUT DISCONNECT

The LTC3536 is designed to allow true output disconnect by opening both P-channel MOSFET rectifiers. This allows V_{OUT} to go to zero volts during shutdown, drawing no current from the input source.

THERMAL CONSIDERATIONS

The power switches in the LTC3536 are designed to operate continuously with currents up to the internal current limit thresholds. However, when operating at high current levels there may be significant heat generated within the IC. As a result, careful consideration must be given to the thermal environment of the IC in order to optimize efficiency and ensure that the LTC3536 is able to provide its full-rated output current. Specifically, the exposed pad of both the DD and MSOP packages shall be soldered to the PC board and the PC board should be designed to maximize the conduction of heat out of the IC package.

If the die temperature exceeds approximately 165°C, the IC will enter overtemperature shutdown and all switching will be inhibited. The part will remain disabled until the die cools by approximately 10°C. The soft-start circuit is reinitialized in overtemperature shutdown to provide a smooth recovery when the fault condition is removed.

If the $\overline{SHDN}$ pin is driven externally to a level higher than V_{IN}, a current limiting resistor should be used. 1M for 6V on the $\overline{SHDN}$ pin limits the current to 6µA. Also, a Schottky diode from the $\overline{SHDN}$ pin to V_{IN} can be used in addition to current limiting resistor.

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The standard LTC3536 application circuit is shown as the Typical Application on the front page of this data sheet. The appropriate selection of external components is dependent upon the required performance of the IC in each particular application given considerations and trade-offs such as PCB area, cost, output and input voltage, allowable ripple voltage, efficiency and thermal considerations. This section of the data sheet provides some basic guidelines and considerations to aid in the selection of external components and the design of the application circuit.

Inductor Selection

The choice of inductor used in LTC3536 application circuits influences the maximum deliverable output current, the magnitude of the inductor current ripple, and the power conversion efficiency. The inductor must have low DC series resistance or output current capability and efficiency will be compromised. Larger inductance values reduce inductor current ripple and will therefore generally yield greater output current capability. For a fixed DC resistance, a larger value of inductance will yield higher efficiency by

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reducing the peak current to be closer to the average output current and therefore minimize resistive losses due to high RMS currents. However, a larger inductor within any given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

An inductor used in LTC3536 applications should have a saturation current rating that is greater than the worst-case average inductor current plus half the ripple current. The peak-to-peak inductor current ripple for each operational mode can be calculated from the following formula, where f is the switching frequency in MHz, L is the inductance in µH.

$$\Delta I_{L(P-P)(BUCK)} = \frac{V_{OUT}}{f \bullet L}\left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

$$\Delta I_{L(P-P)(BOOST)} = \frac{V_{IN}}{f \bullet L}\left(\frac{V_{OUT} - V_{IN}}{V_{OUT}}\right)$$

In addition to its influence on power conversion efficiency, the inductor DC resistance can also impact the maximum output capability of the buck-boost converter particularly at low input voltages. In buck mode, the output current of the buck-boost converter is limited only by the inductor current reaching the current limit threshold. However, in boost mode, especially at large step-up ratios, the output current capability can also be limited by the total resistive losses in the power stage. These include switch resistances, inductor resistance and PCB trace resistance. Use of an inductor with high DC resistance can degrade the output current capability from that shown in the Typical Performance Characteristics section of this data sheet. As a guideline, in most applications the inductor DC resistance should be significantly smaller than the typical power switch resistance of 120mΩ.

The minimum inductor value must guarantee that the worst-case average input current plus half the ripple current don't reach the input current limit threshold. For a switching frequency of 1MHz the recommended typical inductor value is 4.7µH. For a higher and lower switching frequency the inductor value should be changed accordingly in order to have the same current ripple (2.2µH for 2MHz, 15µH for 300kHz).

Different inductor core materials and styles have an impact on the size and price of an inductor at any given current rating. Shielded construction is generally preferred as it minimizes the chances of interference with other circuitry. The choice of inductor style depends upon the price, sizing, and EMI requirements of a particular application. Table 1 provides a small sampling of inductors that are well suited to many LTC3536 applications.

Table 1. Recommended Inductors

VENDOR	PART/STYLE
Coilcraft 847-639-6400 www.coilcraft.com	LPO2506 LPS4012, LPS4018 MSS6122 MSS4020 MOS6020 DS1605, DO1608 XPL4020 XAL4040 XFL4020
Coiltronics www.cooperet.com	SD52, SD53 SD3114, SD311B
Murata 714-852-2001 www.sumida.com	LQH55D
Sumida 847-956-0666 www.sumida.com	CDH40D11
Taiyo Yuden www.t-yuden.com	NP04S8 NR3015 NR4018
TDK 847-803-6100 www.component.tdk.com	VLP, LTF VLF, VLCF
Würth Elektronik 201-785-8800 www.we-online.com	WE-TPC Type S, M, MH

Output Capacitor Selection

A low ESR output capacitor should be utilized at the buck-boost converter output in order to minimize output voltage ripple. Multilayer ceramic capacitors are an excellent option as they have low ESR and are available in small footprints. The capacitor value should be chosen large enough to reduce the output voltage ripple to acceptable levels.

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Neglecting the capacitor ESR and ESL, the peak-to-peak output voltage ripple can be calculated by the following formulas, where f is the frequency in MHz, C_{OUT} is the capacitance in µF and I_{LOAD} is the output current in amps.

$$\Delta V_{(P-P)(BUCK)} = \frac{V_{OUT}}{8 \bullet f^2 \bullet L \bullet C_{OUT}} \left(\frac{V_{IN} - V_{OUT}}{V_{IN}} \right)$$

$$\Delta V_{(P-P)(BOOST)} = \frac{I_{LOAD}}{f \bullet C_{OUT}} \left(\frac{V_{OUT} - V_{IN}}{V_{OUT}} \right)$$

Given that the output current is discontinuous in boost mode, the ripple in this mode will generally be much larger than the magnitude of the ripple in buck mode.

In addition to output voltage ripple generated across the output capacitance, there is also output voltage ripple produced across the internal resistance of the output capacitor. The ESR-generated output voltage ripple is proportional the series resistance of the output capacitor.

Input Capacitor Selection

The PV_{IN} pin carries the full inductor current and provides power to internal control circuits in the IC. To minimize input voltage ripple and ensure proper operation of the IC, a low ESR bypass capacitor with a value of at least 10µF should be located as close to this pin as possible. The traces connecting this capacitor to PV_{IN} and the ground plane should be made as short as possible. The SV_{IN} pin provides power to the internal circuitry. In every application, the SV_{IN} and PV_{IN} must be connected together on the PC Board.

Recommended Input and Output Capacitors

The capacitors used to filter the input and output of the LTC3536 must have low ESR and must be rated to handle the large AC currents generated by switching converters. This is important to maintain proper functioning of the IC and to reduce output voltage ripple.

The choice of capacitor technology is primarily dictated by a trade-off between cost, size and leakage current. Ceramic capacitors are often utilized in switching converter applications due to their small size, low ESR and low leakage currents. However, many ceramic capacitors designed for power applications experience significant loss in capacitance from their rated value with increased DC bias voltages. For example, it is not uncommon for a small surface mount ceramic capacitor to lose more than 50% of its rated capacitance when operated near its rated voltage. As a result, it is sometimes necessary to use a larger value capacitance or a capacitor with a higher voltage rating than required in order to actually realize the intended capacitance at the full operating voltage. To ensure that the intended capacitance is realized in the application circuit, be sure to consult the capacitor vendor's curve of capacitance versus DC bias voltage.

The capacitors listed in Table 2 provide a sampling of small surface mount ceramic capacitors that are well suited to LTC3536 application circuits. All listed capacitors are either X5R or X7R dielectric in order to ensure that capacitance loss over temperature is minimized.

Table 2. Representative Bypass and Output Capacitors

PART NUMBER	VALUE (µF)	VOLTAGE (V)	SIZE (mm) L × W × H (FOOTPRINT)
AVX			
12066D106K	10	6.3	3.2 × 1.6 × 0.5 (1206)
12066D226K	22	6.3	3.2 × 1.6 × 0.5 (1206)
12066D476K	47	6.3	3.2 × 1.6 × 0.5 (1206)
Kemet			
C0603C106K9P	10	6.3	1.6 × 0.8 × 0.8 (0603)
C0805C226K9P	22	6.3	2.0 × 1.25 × 1.25 (0805)
C0805C476K9P	47	6.3	2.0 × 1.25 × 1.25 (0805)
Murata			
GRM21	10	10	2.0 × 1.25 × 1.25 (0805)
GRM21	22	6.3	2.0 × 1.25 × 1.25 (0805)
TDK			
C2102X5R0J	22	6.3	2.0 × 1.25 × 0.85 (0805)
C2102X5R0J	47	6.3	2.0 × 1.25 × 1.25 (0805)
Taiyo Yuden			
JMK212BJ	22	6.3	2.0 × 1.25 × 0.85 (0805)
JMK212BJ	47	6.3	2.0 × 1.25 × 0.85 (0805)

Small-Signal Model

The LTC3536 uses a voltage mode control loop to maintain regulation of the output voltage. An externally compensated error amplifier drives the VC pin to generate the appropriate duty cycle of the power switches. Use of an external compensation network provides the flexibility for optimization of closed-loop performance over the wide

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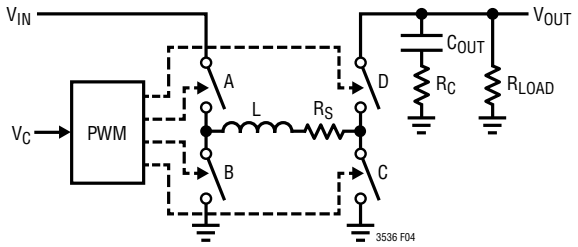

Figure 4. Small-Signal Model

variety of output voltages, switching frequencies, and external component values supported by the LTC3536.

V_{IN} is the input supply voltage, V_{OUT} the programmed output voltage, L is the external buck-boost inductor, C_{OUT} the output capacitor, R_S the series resistance in the power path (it can be approximated as twice the average power switch resistance plus the DC resistance of the inductor) and R_C is the output capacitor ESR.

Buck Mode

The small-signal transfer function of the buck-boost converter is different in the buck and boost modes of operation and care must be taken to ensure stability in both operating regions. When stepping down from a higher input voltage to a lower output voltage, the converter will operate in buck mode and the small-signal transfer function from the error amplifier output, V_C, to the converter output voltage is given by the following equation:

$$\left.\frac{V_{OUT}}{V_C}(s)\right|_{Buck\ Mode} = 2.64 \bullet V_{IN} \bullet \frac{1+sR_CC_{OUT}}{1+\frac{s}{\omega_0 Q}+\left(\frac{s}{\omega_0}\right)^2}$$

This transfer function has a single zero created by the output capacitor ESR and a resonant pair of poles. In most applications, an output capacitor with a very low ESR is utilized in order to reduce the output voltage ripple to acceptable levels. Such low values of capacitor ESR result in a very high frequency zero and as a result the zero is commonly too high in frequency to significantly impact compensation of the feedback loop.

The denominator of the buck mode transfer function exhibits a pair of resonant poles generated by the LC_{OUT} filtering of the power stage. The resonant frequency of the power stage, f_0, is given by the following expression where L is the value of the inductor in henries.

$$\omega_0 = \frac{1}{\sqrt{LC_{OUT}}},\ f_0 = \frac{1}{2\pi\sqrt{LC_{OUT}}}$$

The quality factor, Q, has a significant impact on compensation of the voltage loop since a higher Q factor produces a sharper loss of phase near the resonant frequency. The quality factor is inversely related to the amount of damping in the power stage and is substantially influenced by the average series resistance of the power stage, R_S. Lower values of R_S will increase the Q and result in a sharper loss of phase near the resonant frequency and will require more phase boost or lower bandwidth to maintain an adequate phase margin.

$$Q = \frac{\sqrt{LC_{OUT}}}{C_{OUT}\left(R_C+R_S\right)+\frac{L}{R_{LOAD}}}$$

Boost Mode

When stepping up from a lower input voltage to a higher output voltage, the buck-boost converter will operate in boost mode where the small-signal transfer function from control voltage, V_C, to the output voltage is given by the following expression:

$$\left.\frac{V_{OUT}}{V_C}(s)\right|_{Boost\ Mode} = 2.64 \bullet G \frac{\left(1+sR_CC_{OUT}\right)\left(1-\frac{s}{\omega_Z}\right)}{1+\frac{s}{\omega_0 Q}+\left(\frac{s}{\omega_0}\right)^2}$$

In boost mode operation, the transfer function is characterized by a pair of resonant poles and a zero generated by the ESR of the output capacitor as in buck mode. However, in addition there is a right-half plane zero which generates

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increasing gain and decreasing phase at higher frequencies. As a result, the crossover frequency in boost mode operation generally must be set lower than in buck mode in order to maintain sufficient phase margin.

$$G = V_{IN} \bullet \frac{R_{LOAD}}{R_S} \bullet \frac{1 - \frac{R_S}{R_{LOAD}} \bullet \left(\frac{V_{OUT}}{V_{IN}}\right)^2}{1 + \frac{R_{LOAD}}{R_S} \bullet \left(\frac{V_{IN}}{V_{OUT}}\right)^2}$$

$$\omega_O = \sqrt{\frac{R_S + R_{LOAD}\left(\frac{V_{IN}}{V_{OUT}}\right)^2}{LC_{OUT}\left(R_{LOAD} + R_C\right)}}$$

In boost mode operation, the frequency of the right-half plane zero, f_Z, is given by the following expression. The frequency of the right half plane zero decreases at higher loads and with larger inductors.

$$\omega_Z = \frac{\left(\frac{V_{IN}}{V_{OUT}}\right)^2 R_{LOAD} - R_S}{L}, \quad f_Z = \frac{\left(\frac{V_{IN}}{V_{OUT}}\right)^2 R_{LOAD} - R_S}{2\pi L}$$

Finally, the magnitude of the quality factor of the power stage in boost mode operation is given by the following expression:

$$Q = \frac{\sqrt{LC_{OUT}\left(R_{LOAD} + R_C\right)}\sqrt{R_S + R_{LOAD}\left(\frac{V_{IN}}{V_{OUT}}\right)^2}}{L + C_{OUT}R_{LOAD}R_C\left(\frac{V_{IN}}{V_{OUT}}\right)^2 + R_S C_{OUT}\left(R_{LOAD} + R_C\right)}$$

Buck-Boost Mode

When the converter operates in buck-boost mode and the small-signal transfer function from control voltage, V_C, to the output voltage is given by the following expression:

$$\frac{V_{OUT}}{V_C}(s)\Big|_{\text{Buck-Boost Mode}} = 17.62 \bullet G \frac{\left(1 + sR_C C_{OUT}\right)\left(1 - \frac{s}{\omega_Z}\right)}{1 + \frac{s}{\omega_O Q} + \left(\frac{s}{\omega_O}\right)^2}$$

Also in buck-boost mode operation, the transfer function is characterized by a pair of resonant poles and a zero generated by the ESR of the output capacitor as in buck mode and a right half plane zero.

$$G = \frac{0.15 \bullet V_{OUT}\left(R_{LOAD} \bullet \varepsilon^2 \bullet 1.85 - R_S \bullet (1.85 - \varepsilon)\right)}{\varepsilon \bullet (1.85 - \varepsilon) \bullet \left(R_S + R_{LOAD} \bullet \varepsilon^2\right)}$$

where the variable ε is defined:

$$\varepsilon = \frac{V_{IN} \bullet 1.85}{V_{OUT} + V_{IN}}$$

$$\omega_O = \sqrt{\frac{R_S + R_{LOAD} \bullet \varepsilon^2}{LC_{OUT}\left(R_{LOAD} + R_C\right)}}$$

In buck-boost mode operation, the frequency of the right-half plane zero, f_Z, is given by the following expression. The frequency of the right-half plane zero decreases at higher loads and with larger inductors.

$$\omega_Z = \frac{1.85 \bullet \varepsilon^2 R_{LOAD} - R_S \bullet (1.85 - \varepsilon)}{L \bullet (1.85 - \varepsilon)}$$

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Finally, the magnitude of the quality factor of the power stage in buck-boost mode operation is given by the following expression:

$$Q = \frac{\sqrt{LC_{OUT}\left(R_{LOAD}+R_C\right)}\sqrt{R_S+R_{LOAD}\bullet\varepsilon^2}}{L+C_{OUT}R_{LOAD}R_C\bullet\varepsilon^2+R_SC_{OUT}\left(R_{LOAD}+R_C\right)}$$

Compensation of the Voltage Loop

The small-signal models of the LTC3536 reveal that the transfer function from the error amplifier output, VC, to the output voltage is characterized by a set of resonant poles and a possible zero generated by the ESR of the output capacitor as shown in the Bode plot of Figure 5. In boost mode operation, there is an additional right-half plane zero that produces phase lag and increasing gain at higher frequencies. Typically, the compensation network is designed to ensure that the loop crossover frequency is low enough that the phase loss from the right-half plane zero is minimized. The low frequency gain in buck mode is a constant, but varies with both V_{IN} and V_{OUT} in boost mode.

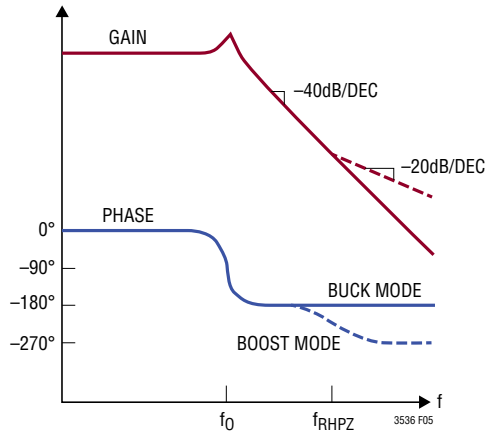

Figure 5. Buck-Boost Converter Bode Plot

For charging or other applications that do not require an optimized output voltage transient response, a simple Type I compensation network as shown in Figure 6 can be used to stabilize the voltage loop. To ensure sufficient phase margin, the gain of the error amplifier must be low enough that the resultant crossover frequency of the control loop is well below the resonant frequency.

In most applications, the low bandwidth of the Type I compensated loop will not provide sufficient transient response performance. To obtain a wider bandwidth feedback loop, optimize the transient response, and minimize the size of the output capacitor, a Type III compensation network as shown in Figure 7 is required.

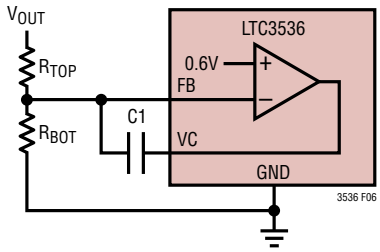

Figure 6. Error Amplifier with Type I Compensation

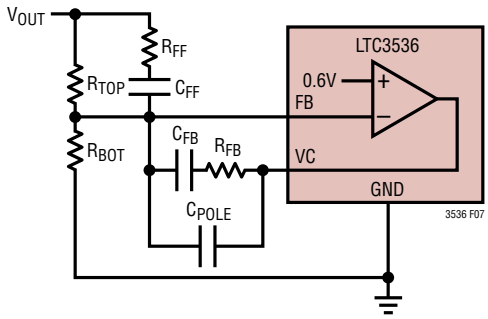

Figure 7. Error Amplifier with Type III Compensation

A Bode plot of the typical Type III compensation network is shown in Figure 8. The Type III compensation network provides a pole near the origin which produces a very high loop gain at DC to minimize any steady-state error in the regulation voltage. Two zeros located at f_{ZERO1} and f_{ZERO2} provide sufficient phase boost to allow the loop crossover frequency to be set above the resonant frequency, f_O, of the power stage. The Type III compensation network also introduces a second and third pole. The second pole, at frequency f_{POLE2}, reduces the error amplifier gain to a zero slope to prevent the loop crossover from extending too high in frequency. The third pole at frequency f_{POLE3} provides attenuation of high frequency switching noise.

APPLICATIONS INFORMATION

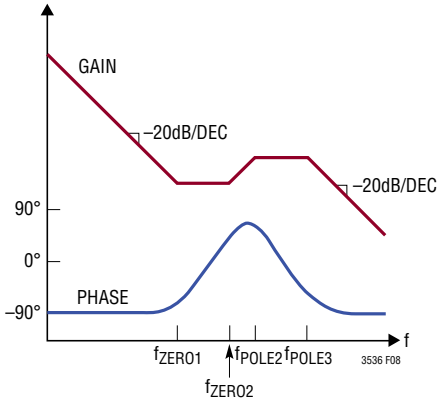

Figure 8. Type III Compensation Bode Plot

The transfer function of the compensated Type III error amplifier from the input of the resistor divider to the output of the error amplifier, VC, is:

$$\frac{V_{C(S)}}{V_{OUT(S)}} = G_{EA} \frac{\left(1+\frac{s}{2\pi f_{ZERO1}}\right)\left(1+\frac{s}{2\pi f_{ZERO2}}\right)}{s\left(1+\frac{s}{2\pi f_{POLE1}}\right)\left(1+\frac{s}{2\pi f_{POLE2}}\right)}$$

The error amplifier gain is given by the following equation. The simpler approximate value is sufficiently accurate in most cases since C_{FB} is typically much larger in value than C_{POLE}.

$$G_{EA} = \frac{1}{R_{TOP}\left(C_{FB}+C_{POLE}\right)} \approx \frac{1}{R_{TOP}C_{FB}}$$

The pole and zero frequencies of the Type III compensation network can be calculated from the following equations where all frequencies are in Hz, resistances are in ohms, and capacitances are in farads.

$$f_{ZERO1} = \frac{1}{2\pi R_{FB}C_{FB}}$$

$$f_{ZERO2} = \frac{1}{2\pi\left(R_{TOP}+R_{FF}\right)C_{FF}} \approx \frac{1}{2\pi R_{TOP}C_{FF}}$$

$$f_{POLE2} = \frac{C_{FB}+C_{POLE}}{2\pi C_{FB}C_{POLE}R_{FB}} \approx \frac{1}{2\pi C_{POLE}R_{FB}}$$

$$f_{POLE3} = \frac{1}{2\pi C_{FF}R_{FF}}$$

In most applications the compensation network is designed so that the loop crossover frequency is above the resonant frequency of the power stage, but sufficiently below the boost mode right-half plane zero to minimize the additional phase loss. Once the crossover frequency is decided upon, the phase boost provided by the compensation network is centered at that point in order to maximize the phase margin. A larger separation in frequency between the zeros and higher order poles will provide a higher peak phase boost but may also increase the gain of the error amplifier which can push out the loop crossover to a higher frequency.

The Q of the power stage can have a significant influence on the design of the compensation network because it determines how rapidly the 180° of phase loss in the power stage occurs. For very low values of series resistance, R_S, the Q will be higher and the phase loss will occur sharply. In such cases, the phase of the power stage will fall rapidly to –180° above the resonant frequency and the total phase margin must be provided by the compensation network.

However, with higher losses in the power stage (larger R_S) the Q factor will be lower and the phase loss will occur more gradually. As a result, the power stage phase will not be as close to –180° at the crossover frequency and less phase boost is required of the compensation network.

The LTC3536 error amplifier is designed to have a fixed maximum bandwidth in order to provide rejection of switching noise to prevent it from interfering with the control loop. From a frequency domain perspective, this can be viewed as an additional single pole as illustrated in Figure 9. The nominal frequency of this pole is 400kHz. For typical loop crossover frequencies below about 40kHz the phase contributed by this additional pole is usually

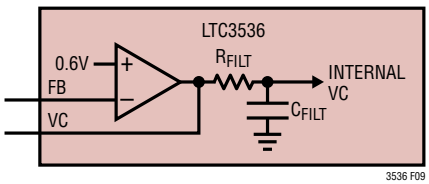

Figure 9. Internal Loop Filter

APPLICATIONS INFORMATION

negligible (for 40kHz is around –5.7°). However, for loops with higher crossover frequencies this additional phase lag should be taken into account when designing the compensation network.

Loop Compensation Example

This section provides an example illustrating the design of a compensation network for a typical LTC3536 application circuit. In this example a 3.3V regulated output voltage is generated with the ability to supply 300mA load from an input power source ranging from 1.8V to 5.5V. To optimize efficiency 1MHz switching frequency has been chosen. In this application the maximum inductor current ripple will occur at the highest input voltage. An inductor value of 4.7µH has been chosen to limit the worst-case inductor current ripple. A low ESR output capacitor with a value of 22µF is specified to yield a worst-case output voltage ripple of approximately 10mV (occurring at the worst-case step-up ratio and maximum load current). In summary, the key power stage specifications for this LTC3536 example application are given below:

f = 1MHz
V_{IN} = 1.8V to 5.5V
V_{OUT} = 3.3V at 300mA
C_{OUT} = 22µF,
R_C = 10mΩ
L = 4.7µH,
R_L = 60mΩ

With the power stage parameters specified, the compensation network can be designed. A reasonable approach is to design the compensation network at this worst-case corner and then verify that sufficient phase margin exists across all other operating conditions. In this example application, at V_{IN} = 1.8V and the full 300mA load current, the right-half plane zero will be located at 100kHz and this will be a dominant factor in determining the bandwidth of the control loop.

The first step in designing the compensation network is to determine the target crossover frequency for the compensated loop. This example will be designed for a 60° phase margin to ensure adequate performance over parametric variations and varying operating conditions. As a result, the target crossover frequency, f_C, will be the point at which the phase of the buck-boost converter reaches –180°. It is generally difficult to determine this frequency analytically, because it is significantly impacted by the Q factor of the resonance in the power stage. As a result, it is best determined from a Bode plot of the buck-boost converter as shown in Figure 10. This Bode plot is for the LTC3536 buck-boost converter using the previously specified power stage parameters and was generated from the small signal model equations using LTspice® software.

In this case, the phase reaches –180° at 37.8kHz making f_C = 37.8kHz the target crossover frequency for the compensated loop. From the Bode plot of Figure 9 the gain of the power stage at the target crossover frequency is –2dB.

At this point in the design process, there are three constraints that have been established for the compensation network. It must have +2dB gain at f_C = 37.8kHz, a peak phase boost of 60° and the phase boost must be centered at f_C = 37.8kHz.

An analytical approach can be used to design a compensation network with the desired phase boost, center frequency and gain. In general, this procedure can be cumbersome due to the large number of degrees of freedom in a Type III compensation network. However the design process can be simplified by assuming that both compensation zeros

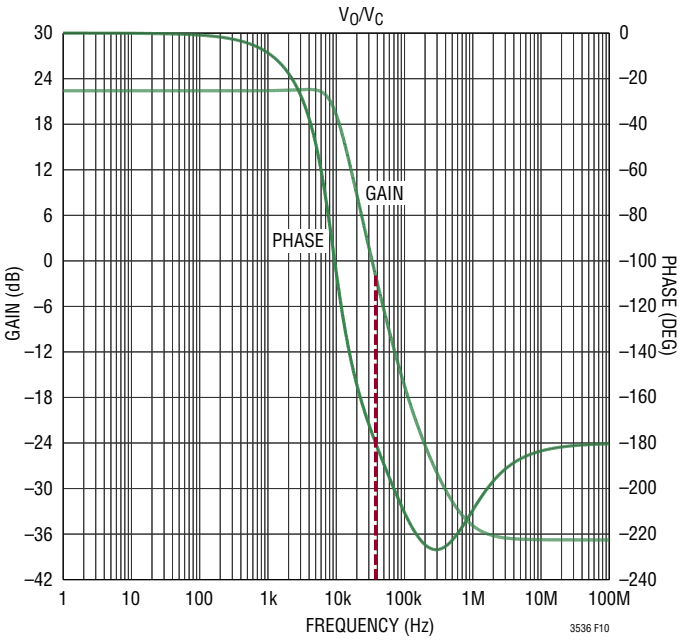

Figure 10. Converter Bode Plot, V_{IN} = 1.8V, I_{LOAD} = 300mA

APPLICATIONS INFORMATION

occur at the same frequency, f_Z, and both higher order poles (f_{POLE2} and f_{POLE3}) occur at the common frequency, f_P .

This is a good starting point for determining the compensation network. However the Bode plot for the complete loop should be checked overall operating conditions and for variations in components values to ensure that sufficient phase margin and gain margin exists in all cases.

A reasonable choice is to pick the frequency of the poles, f_P, to be about 50 times higher than the frequency of the zeros, f_Z, which provides a peak phase boost of approximately $\Phi_{MAX} = 60°$ as was assumed previously. Next, the phase boost must be centered so that the peak phase occurs at the target crossover frequency. The frequency of the maximum phase boost, f_C, is the geometric mean of the pole and zero:

$$f_C = \sqrt{f_P \bullet f_Z} = \sqrt{50 \bullet f_Z^2} = 7 \bullet f_Z$$

Therefore, in order to center the phase boost given a factor of 50 separation between the pole and zero frequencies, the zeros should be located at one-seventh of the crossover frequency and the poles should be located at seven times the crossover frequency as given by the following equations:

$$f_Z = \frac{1}{7} \bullet f_C = \frac{1}{7} \bullet (37.8kHz) = 5.4kHz$$

$$f_P = 7 \bullet f_C = 7 \bullet (37.8kHz) = 264.6kHz$$

This placement of the poles and zeros will yield a peak phase boost of 60° that is centered at the crossover frequency, f_C. Next, in order to produce the desired target crossover frequency, the gain of the compensation network at the point of maximum phase boost, G_{CENTER}, must be set to +2dB. The gain of the compensated error amplifier at the point of maximum phase gain is given by:

$$G_{CENTER} = 10\log\left[\frac{2\pi f_P}{(2\pi f_Z)^3 (R_{TOP} C_{FB})^2}\right]$$

Assuming a multiple of 50 separation between the pole frequencies and zero frequencies this can be simplified to the following expression:

$$G_{CENTER} = 20\log\left[\frac{50}{(2\pi f_C)(R_{TOP} C_{FB})}\right]$$

The first step in defining the compensation component values is to pick a value for R_{TOP} that provides an acceptably low quiescent current through the resistor divider. A value of R_{TOP} = 845k is a reasonable choice. Next, the value of C_{FB} can be found:

G_{CENTER} = 2dB

$$C_{FB} \frac{50}{2\pi \bullet (37.8kHz) \bullet 845k\Omega \bullet 10^{\frac{2dB}{20}}} = 198pF \approx 180pF$$

The compensation poles can be set at 264.6kHz and the zeros at 5.4kHz by using the expressions for the pole and zero frequencies given in the previous section. Setting the frequency of the first zero, f_{ZERO1}, to 5.4kHz results in the following value for R_{FB}:

$$R_{FB} = \frac{1}{2\pi \bullet (180pF) \bullet 5.4kHz} = 163k\Omega \approx 162k\Omega$$

This leaves the free parameter, C_{POLE}, to set the frequency f_{POLE1} to the common pole frequency of 264.6kHz as given:

$$C_{POLE} = \frac{1}{2\pi \bullet (162k\Omega) \bullet 264.6kHz} = 3.71pF \approx 3.9pF$$

Next, C_{FF} can be chosen to set the second zero, f_{ZERO2}, to the common zero frequency of 5.4kHz.

$$C_{FF} = \frac{1}{2\pi \bullet (845k\Omega) \bullet 5.4kHz} = 34.9pF \approx 33pF$$

Finally, the resistor value R_{FF} can be chosen to place the second pole at 264.6kHz:

$$R_{FF} = \frac{1}{2\pi \bullet (33pF) \bullet 264.6kHz} = 18.2k\Omega$$

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A Bode plot of the error amplifier with the designed compensation component values is shown in Figure 11. The Bode plot confirms that the peak phase occurs at 37.8kHz and the phase boost at that point is about 60°. In addition, the gain at the peak phase frequency is 2dB which is close to the design target.

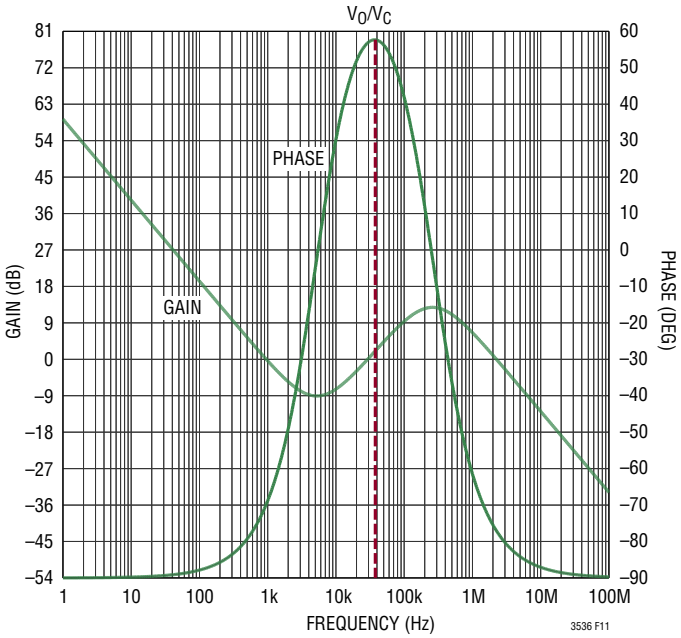

Figure 11. Compensated Error Amplifier Bode Plot

The final step in the design process is to compute the Bode plot for the entire loop using the designed compensation network and confirm its phase margin and crossover frequency. The complete loop Bode plot for this example is shown in Figure 12. The loop crossover frequency is 37.8kHz which matches the design target and the phase margin is approximately 60°.

The Bode plot for the complete loop should be checked overall operating conditions and for variations in component values to ensure that sufficient phase margin and gain margin exists in all cases. The stability of the loop should also be confirmed via time domain simulation and by evaluating the transient response of the converter in the actual circuit.

In this example the V_{IN} varies from 1.8V to 5.5V. In buck-boost operation (when $0.85 \bullet V_{OUT} < V_{IN} < V_{OUT}/0.85$) the Bode plot of the complete loop shows a phase margin of

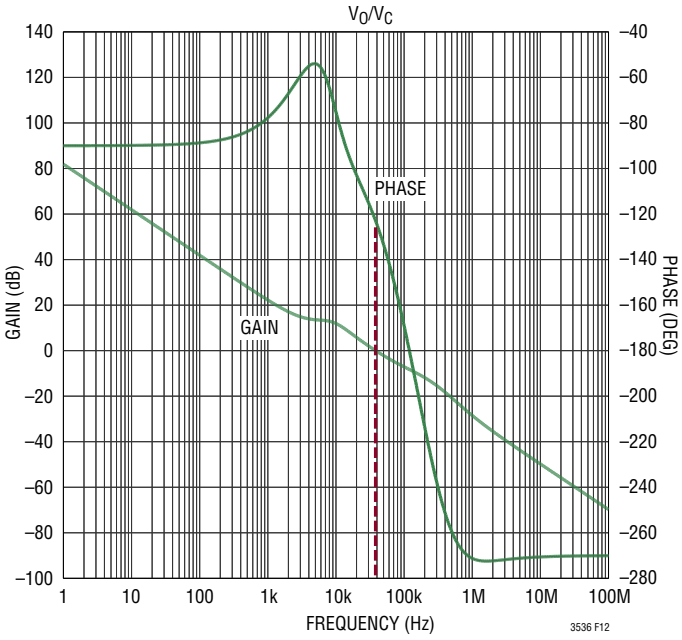

Figure 12. Complete Loop Bode Plot for Boost Operation Mode

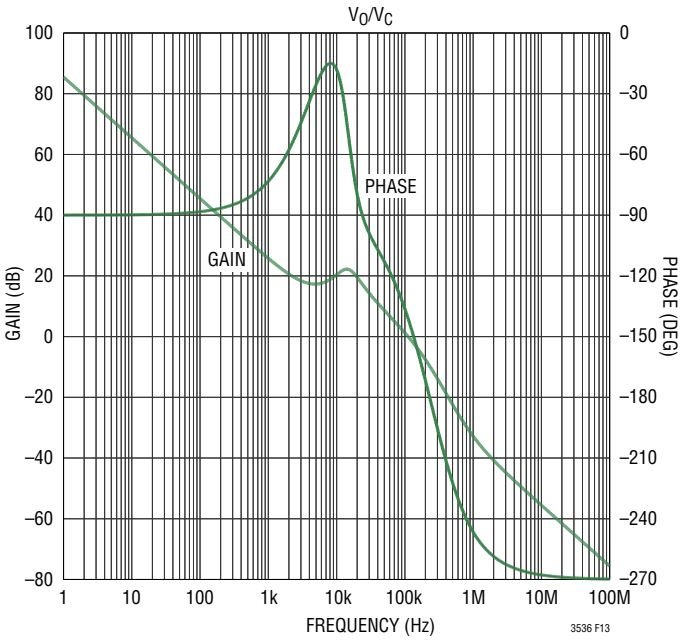

Figure 13. Complete Loop Bode Plot for Buck-Boost Operation Mode

40° for $V_{IN} = V_{OUT} = 3.3V$. In fact in this mode of operation the DC gain increase and often make this the most critical region to compensate.

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In order to improve the stability also in buck-boost mode of operation, the two compensation zeros could be move to different frequency:

$$f_{ZERO2} = \frac{1}{2\pi R_{TOP} C_{FF}} = 5.4kHz$$

$$f_{ZERO1} = \frac{1}{2\pi R_{FB} C_{FB}} = 2 \bullet f_{ZERO2} = 10.8kHz$$

The new R_{FB} value is:

$$R_{FB} = \frac{1}{2\pi \bullet (180pF) \bullet 10.8kHz} = 81.9k\Omega \approx 80.6k\Omega$$

As consequence the f_{POLE2} will move to higher frequency:

$$f_{POLE2} = \frac{1}{2\pi C_{POLE} R_{FB}} = 532kHz$$

As shown from Figures 14 and 15, the stability is now improved for the buck-boost region (V_{IN} = 3V) and remains good for the boost region (V_{IN} = 1.8V).

In buck mode there is no right-half plane zero and the stability is normally achieved.

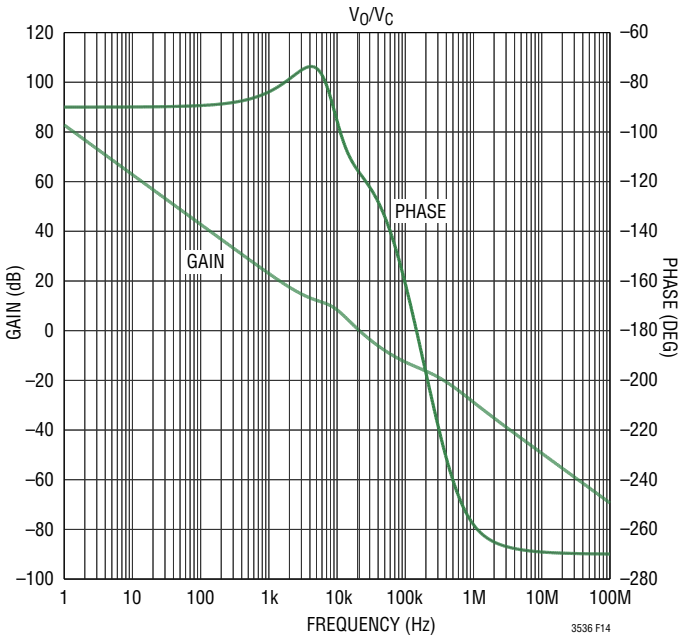


Figure 14. Complete Loop Bode Plot for Boost Operation Mode

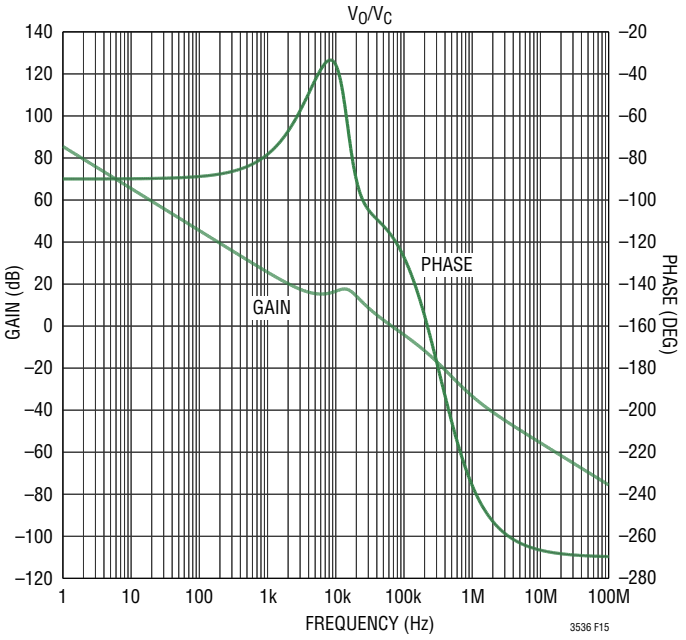


Figure 15. Complete Loop Bode Plot for Buck-Boost Operation Mode

Output Voltage Programming

The output voltage is set via the external resistor divider comprised of resistors R_{TOP} and R_{BOT}. The resistor divider values determine the output regulation voltage according to:

$$V_{OUT} = 0.6\left(1 + \frac{R_{TOP}}{R_{BOT}}\right)V$$

In addition to setting the output voltage, the value of R_{TOP} is instrumental in controlling the dynamics of the compensation network. When changing the value of this resistor, care must be taken to understand the impact this will have on the compensation network. As noted in the Input and Peak Current Limit section, "for current limit feature to be most effected, the Thevenin resistance (R_{TOP}//R_{BOT}) from FB to ground should exceed 100k."

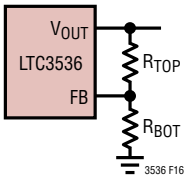


Figure 16. FB Resistor Network

APPLICATIONS INFORMATION

Switching Frequency Selection

Higher switching frequencies facilitate the use of smaller inductors as well as smaller input and output filter capacitors which results in a smaller solution size and reduced component height. However, higher switching frequencies also generally reduce conversion efficiency due to the increased switching losses. In addition, the maximum voltage step-up ratio is reduced slightly at higher switching frequencies as shown in the maximum duty cycle versus switching frequency curve in the Typical Performance Characteristics section of this data sheet.

PCB Layout Considerations

The LTC3536 buck-boost converter switches large currents at high frequencies. Special attention should be paid to the PC board layout to ensure a stable, noise-free and efficient application circuit. A few key guidelines are provided:

1. The parasitic inductance and resistance of all circulating high current paths should be minimized. This can be accomplished by keeping the routes as short and as wide as possible. Capacitor ground connections should via down to the ground plane by way of the shortest route possible. The bypass capacitors on PV_{IN} and V_{OUT} should be placed as close to the IC as possible and should have the shortest possible paths to ground.
2. The exposed pad is the electrical power ground connection for the LTC3536 in the DD package. Multiple vias should connect the backpad directly to the ground plane. In addition, maximization of the metallization connected to the backpad will improve the thermal environment and improve the power handling capabilities of the IC in either package.
3. The components their connections with high current should all be placed over a complete ground plane to minimize loop cross-sectional areas. This minimizes EMI and reduces inductive drops.
4. Connections to all of the components with high current should be made as wide as possible to reduce the series resistance. This will improve efficiency and maximize the output current capability of the buck-boost converter
5. To prevent large circulating currents in the ground plane from disrupting operation of the LTC3536, all small-signal grounds should return directly to GND by way of a dedicated Kelvin route. This includes the ground connection for the RT pin resistor and the ground connection for the feedback network.
6. Keep the routes connecting to the high impedance, noise sensitive inputs FB and RT as short as possible to reduce noise pick-up. Example from MODE route in case the chip is synchronized with external clock.

APPLICATIONS INFORMATION

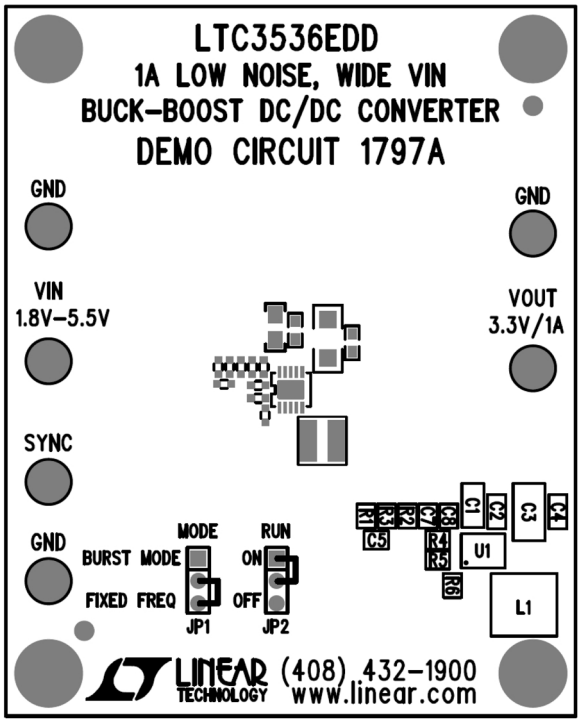


Figure 17a. Fabrication Layer of Example PCB with 4 Layers

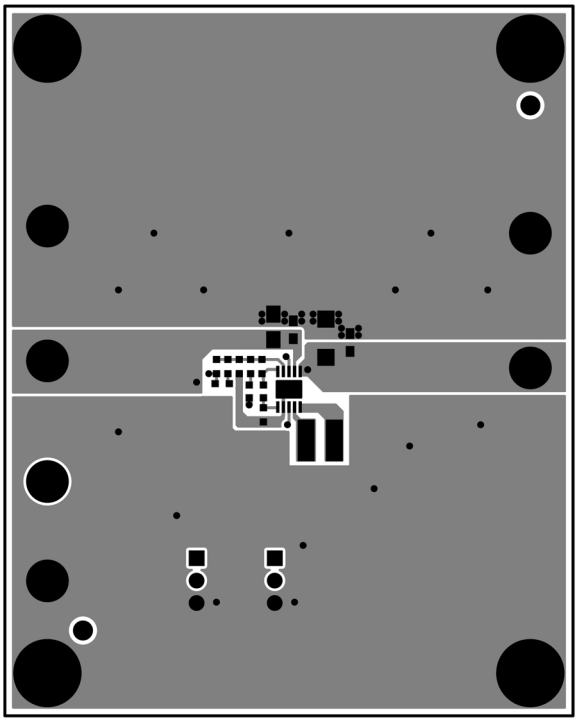


Figure 17b. Top Layer of Example PCB

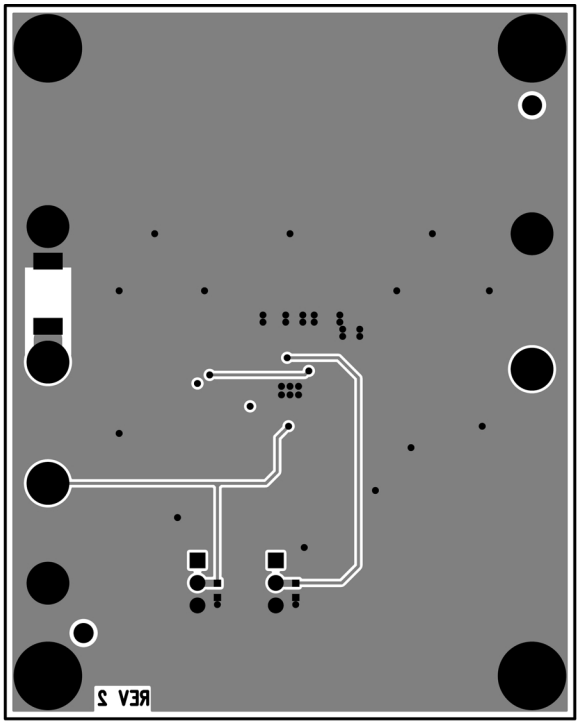
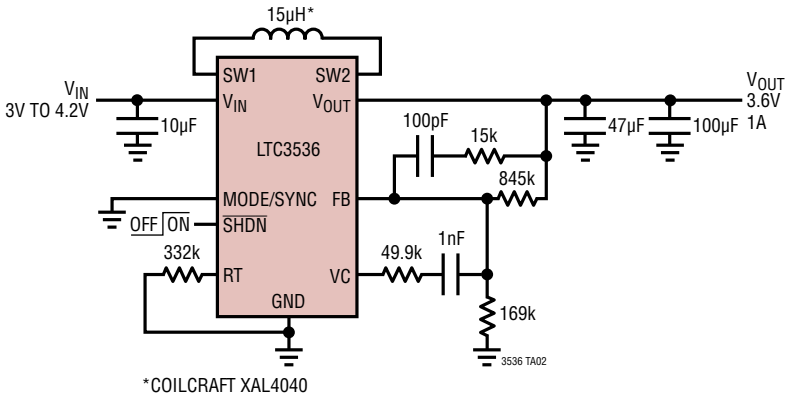


Figure 17c. Bottom Layer of Example PCB

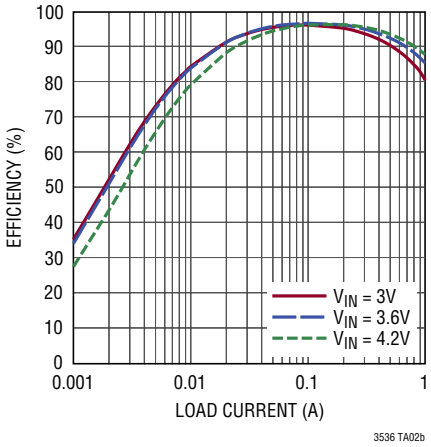
TYPICAL APPLICATIONS

300kHz High Efficiency Li-Ion to 3.6V at 1A, Pulsed with Manual Mode Control

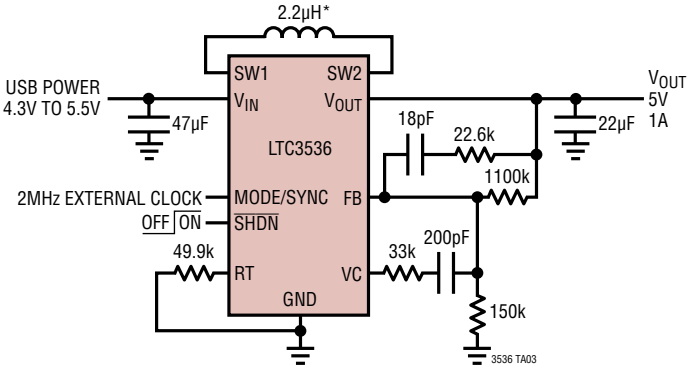


*COILCRAFT XAL4040

Efficiency 3.6V, 300kHz vs Load Current

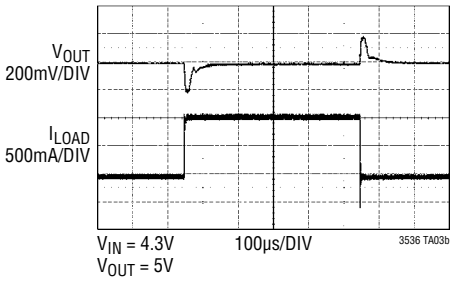


USB to 5V Converter



*COILCRAFT XFL4020

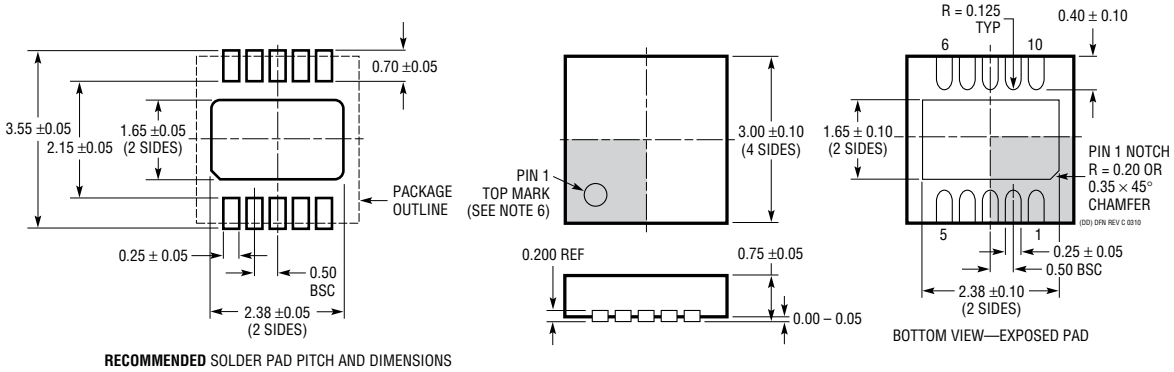
Load Step



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

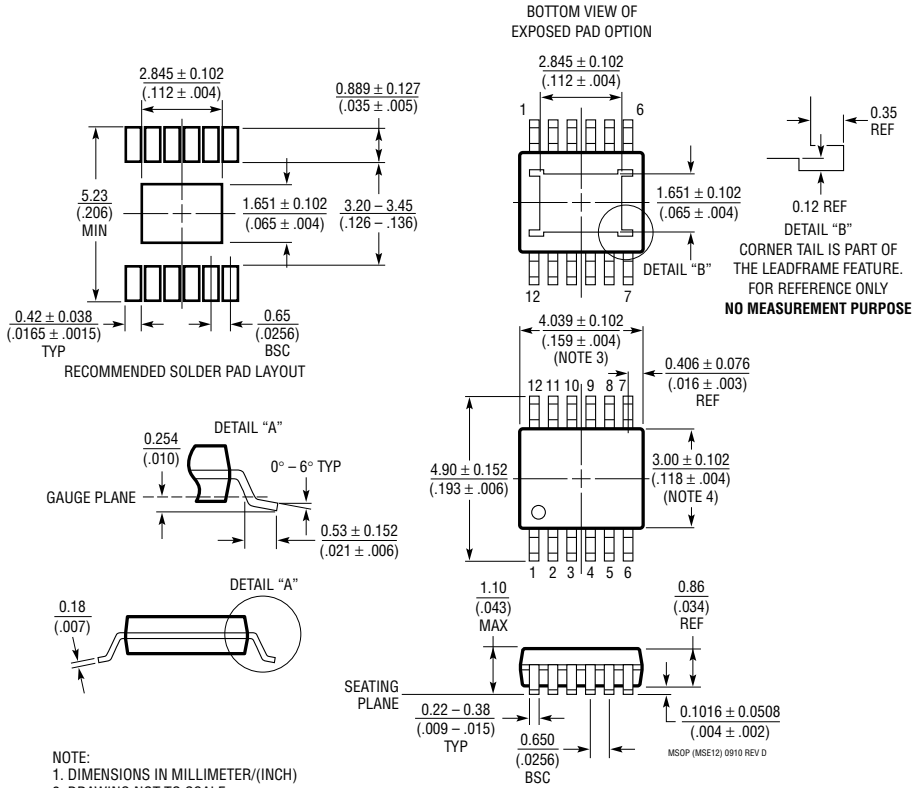
DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev D)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/11	Add new bullet Output Disconnect in Shutdown to Features bullet list.	1
		In the Absolute Maximum Ratings section change (Notes 1, 2) to (Note 1) and (Note 2) to (Notes 2, 3).	2
		In Electrical Characteristics table add conditions for Error Amplifier Sink Current and Error Amplifier Source Current.	3
		In Pin Functions add Exposed Pad Pin 13 and remove last sentence to PGND pin description.	7
		Change negative input of Peak Current Limit comparator to 3.4V and negative input of UVLO comparator to 1.75V.	8
		Add new section Output Disconnect to Operations section.	12