LTC4274A
Single LTPoE++ PSE Controller

DESCRIPTION

Demonstration circuit 1814A features the LTC®4274A, single port power sourcing equipment (PSE) controller, capable of delivering up to 90W of LTPoE++® power to a compatible LTPoE++ powered device (PD). A proprietary detection/classification scheme allows mutual identification between an LTPoE++ PSE and LTPoE++ PD while remaining compatible and interoperable with existing Type 1 (13W) and Type 2 (25.5W) PDs. The LTC4274A feature set is a superset of the popular LTC4274. These PSE controllers utilize low R_{ON} external MOSFETs and 0.25Ω sense resistors which are especially important at the LTPoE++ current levels to maintain the lowest possible heat dissipation.

The LTC4274A is available in multiple power grades, allowing delivered PD power of 13W, 25.5W, 38.7W, 52.7W, 70W and 90W. The DC1814A has four variations DC1814A-A, DC1814A-B, DC1814A-C, and DC1814A-D which accommodate the LTPoE++ power levels (Table 1).

The LTC4274A is configured in the DC1814A as an AUTO pin high, MID pin high, autonomous midspan power injector; input data from an existing network system is sent out, along with power, to a PD. The LTC4274A autonomously detects a PD, turns power on to the port, and disconnects port power without the need for a microcontroller. A single 55V supply is required to power the DC1814A. A simple LDO regulator circuit on the board powers the digital supply of the LTC4274A. A $\overline{SHDN}$ pushbutton shuts down the port and disables detection. A $\overline{RESET}$ pushbutton resets the LTC4274A to the AUTO pin high state.

Design files for this circuit board are available at http://www.linear.com/demo/DC1814A

Table 1. DC1814A Power Levels

DEMO BOARD	PSE CONTROLLER	MAXIMUM DELIVERED PD POWER	POWER SUPPLY*
DC1814A-A	LTC4274A-1	38.7W	72W
DC1814A-B	LTC4274A-2	52.7W	72W
DC1814A-C	LTC4274A-3	70W	120W
DC1814A-D	LTC4274A-4	90W	140W

*Recommended DC1814A power supply minimum to avoid drooping in a worst-case scenario with I_{LIM} current at the port. Set the voltage between 54.75V to 57V for LTPoE++ compliance.

QUICK START PROCEDURE

Demonstration circuit 1814A is easy to set up for evaluating the performance of the LTC4274A. Refer to Figure 1 for proper test equipment setup and follow the procedure below.

1. Connect a 55V to 57V power supply across AGND (+) and VEE (–). Size the power supply considering the maximum power delivered to the PD.
2. Connect an 802.3 Type 1 or Type 2, or LTPoE++ compatible PD to RJ45 connector J1 with an Ethernet cable.
3. Measure the port output voltage to the PD across VPORT+ and VPORT– test points.
4. (Optional) Connect a PHY to RJ45 connector J2 with an Ethernet cable for data tests.

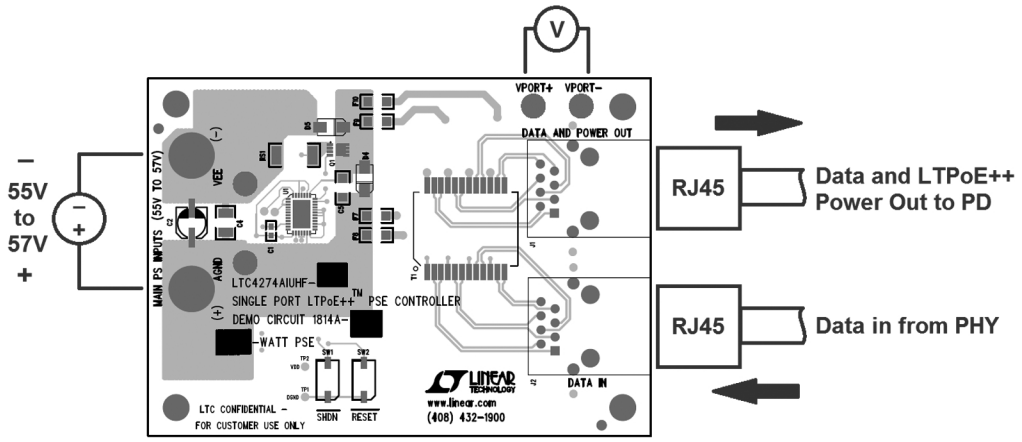


Figure 1. DC1814A Setup

BOARD LAYOUT

Proper components placement and board layout with respect to the LTC4274A is important to provide electrical robustness and correct operation. The following mentioned components, also shown in Figure 2, must be close to their respective LTC4274A pins with no other components in between on the connection path. Place a 0.1µF capacitor (C1) directly across the LTC4274A VDD and DGND pins. Place a 1µF, 100V capacitor (C4) and a SMAJ58A TVS (D3) directly across the LTC4274A AGND and VEE pins. Place a 0.22µF, 100V capacitor (C5) directly to the OUT pin and an AGND plane.

The power path is from VEE to the sense resistor, to the MOSFET, and out to the port. Select a trace width appropriate for the maximum current.

Kelvin sensing is necessary to provide accurate current readings. The sense resistor used with the LTC4274A must be 0.25Ω, 1% or better, and with a power rating that can handle the maximum DC current passed through it. A dedicated sense trace from the SENSE pin of the LTC4274A must go directly to the sense resistor solder pad. Avoid connecting to copper cutouts and other traces. The VEE side of the sense resistor must also connect to the VEE pins of the LTC4274A either through a direct trace (Figure 3A), or a VEE copper plane (Figure 3B), without any other components in between on this connection.

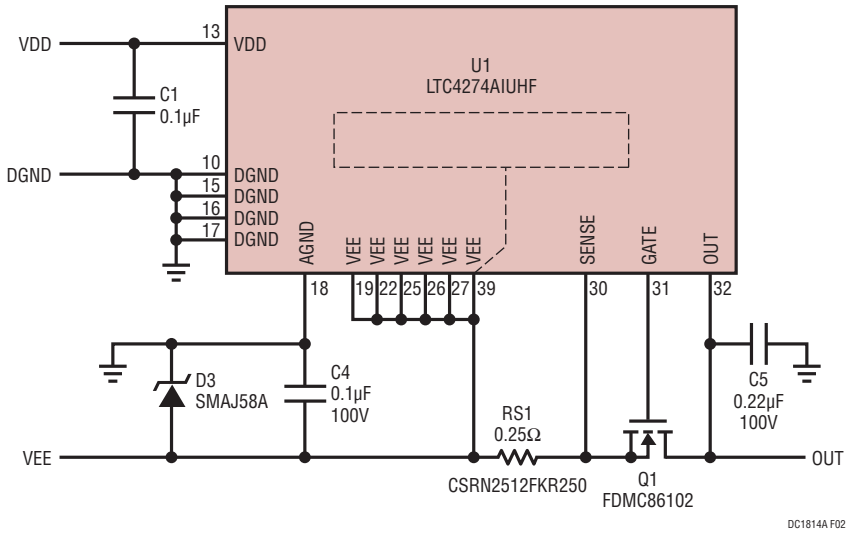


Figure 2. LTC4274A Key Application Components for Board Placement

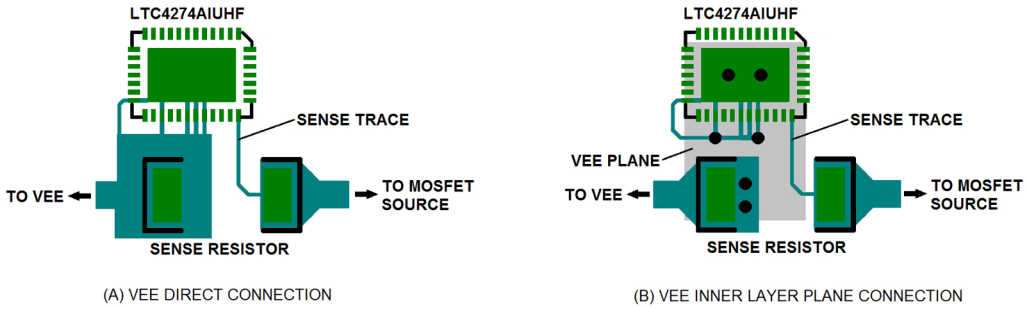


Figure 3. LTC4274IUHF VEE and SENSE Kelvin Connection to Sense Resistor

SUPPLY VOLTAGES

Select a VEE supply with enough power to sustain the port at maximum load. Table 1 shows the maximum delivered PD power as well as a recommended VEE power supply minimum to avoid drooping in a worst case scenario with I_{LIM} current.

The LTC4274A also requires a digital 3.3V supply. The DC1814A uses a simple LDO regulator circuit to power the 3.3V digital supply from the VEE supply. The LTC4274A VDD supply is allowed to be within 5V above or below AGND. On the DC1814A, VDD is tied to AGND and DGND is a negative voltage below AGND. D1, R5, Q2, and R11 generate the negative voltage referenced to AGND (Figure 4). These components are sized to handle the power required to supply the LTC4274A and LEDs on the DC1814A. Contact Linear Technology Applications for 3.3V options.

Surge Protection

Ethernet ports can be subject to significant cable surge events. To keep PoE voltages below a safe level and protect the application against damage, protection components are required at the main supply, at the LTC4274A supply pins and at the port. Refer to Figure 5.

Bulk transient voltage suppression devices and bulk capacitance are required across the main PoE supply and should be sized to accommodate system level surge requirements. Across the LTC4274A AGND pin and VEE pin are an SMAJ58A, 58V TVS and a 1µF, 100V bypass capacitor. These components must be placed close to the LTC4274A pins.

In a high surge environment, a 10Ω, 0805 resistor in series from supply AGND to the LTC4274A AGND and VDD pin is recommended. The bulk TVS and capacitance remain on the supply side of this 10Ω resistor. The LTC4274A supply pins local TVS and capacitance remain at the LTC4274A side of this 10Ω resistor.

The port requires a pair of S1B clamp diodes: one from OUT to supply AGND and one from supply VEE to OUT. The diodes at the ports steer harmful surges into the supply rails where they are absorbed by the surge suppressors and the VEE bypass capacitance. The layout of these paths must be low impedance.

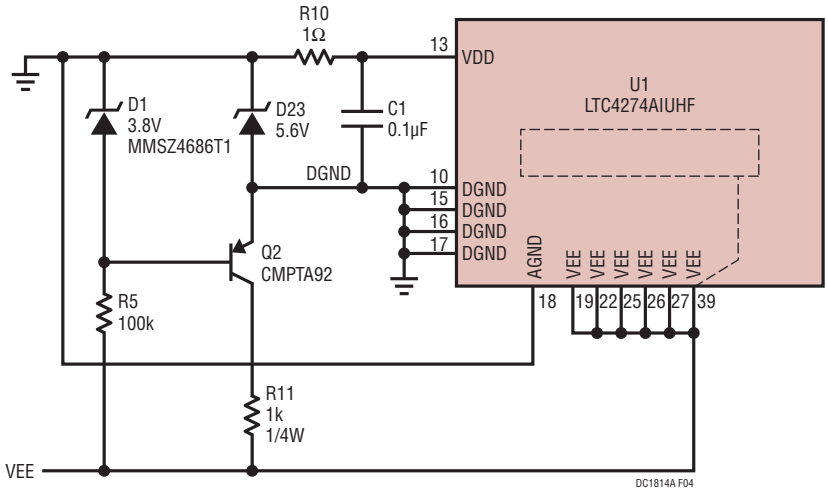


Figure 4. DC1814A LDO Circuit for the LTC4274A Digital Supply

SUPPLY VOLTAGES

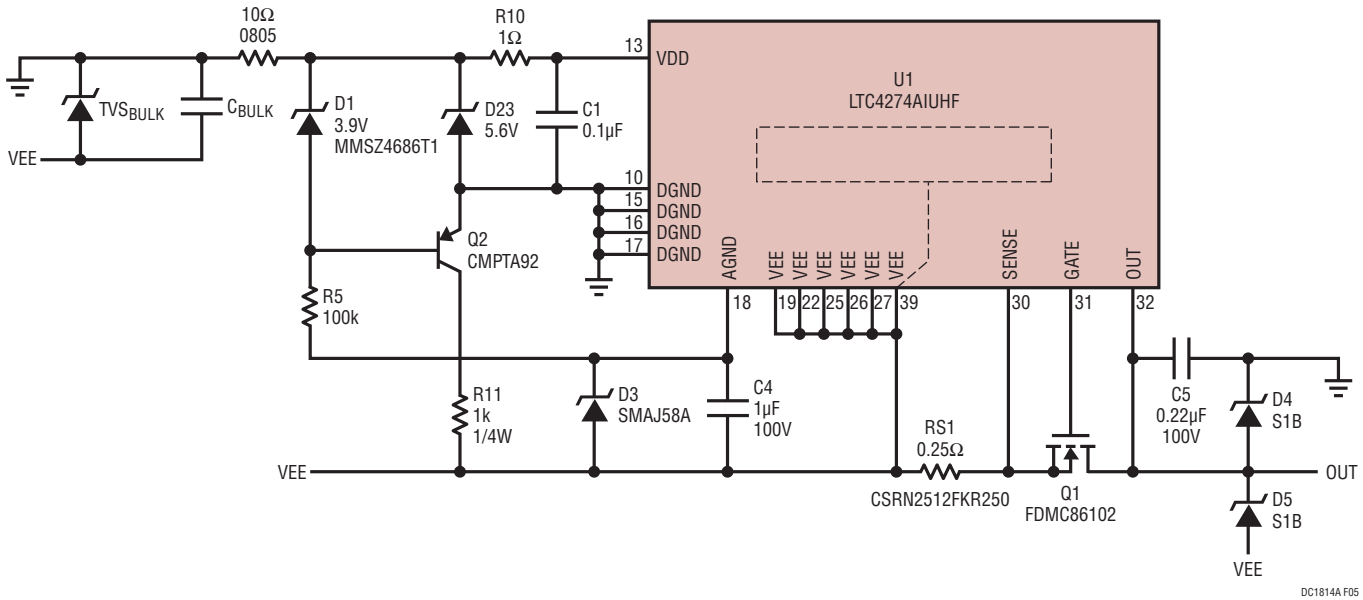
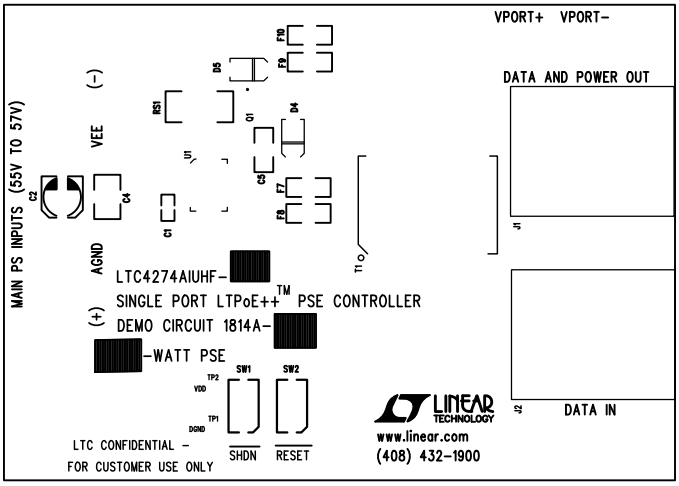


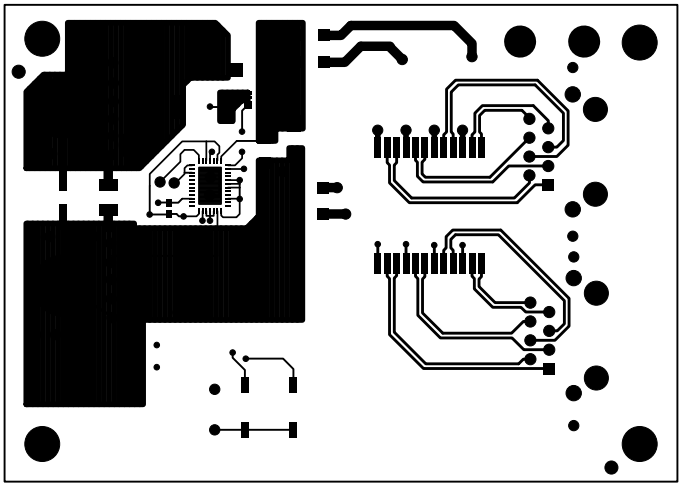
Figure 5. High Surge Environment Recommended LTC4274A Protection

PCB LAYOUT

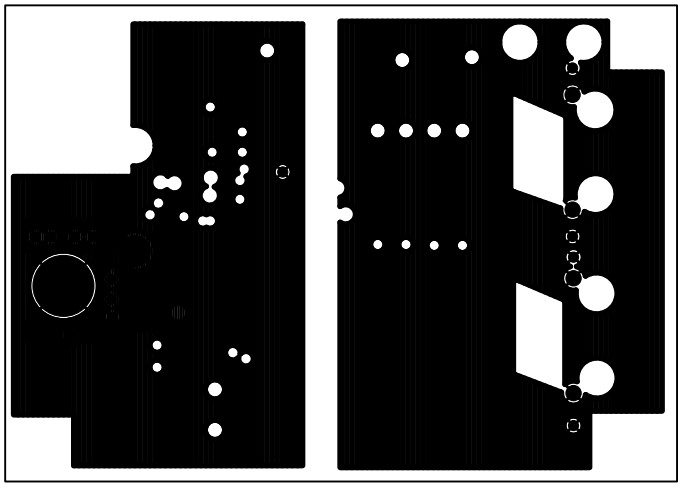
Top Silkscreen



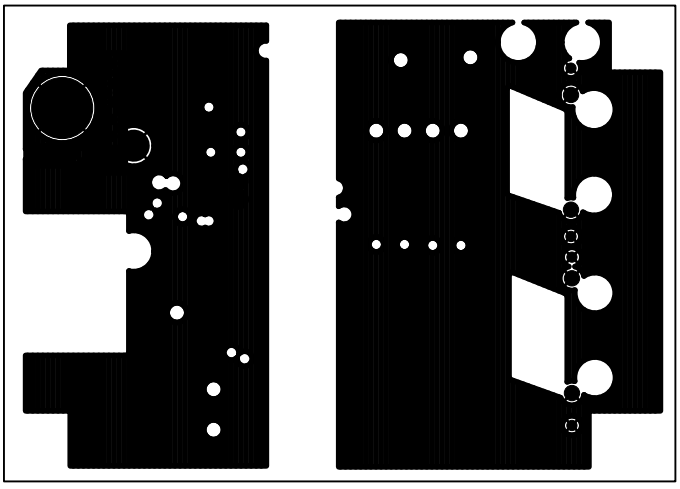
Layer 1. Top Layer



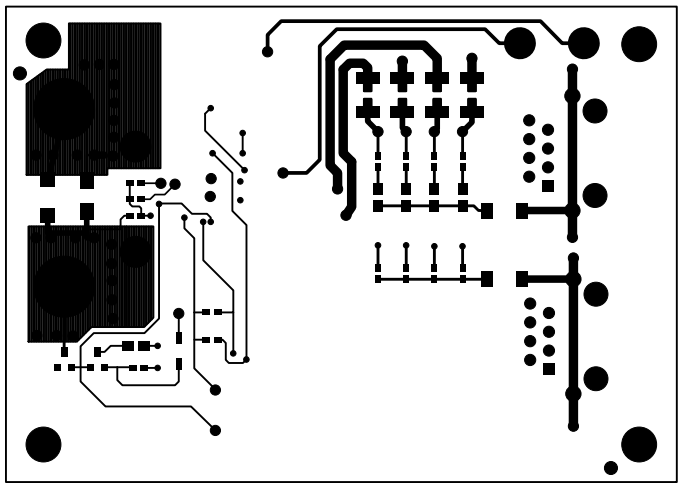
Layer 2. –VIN 1



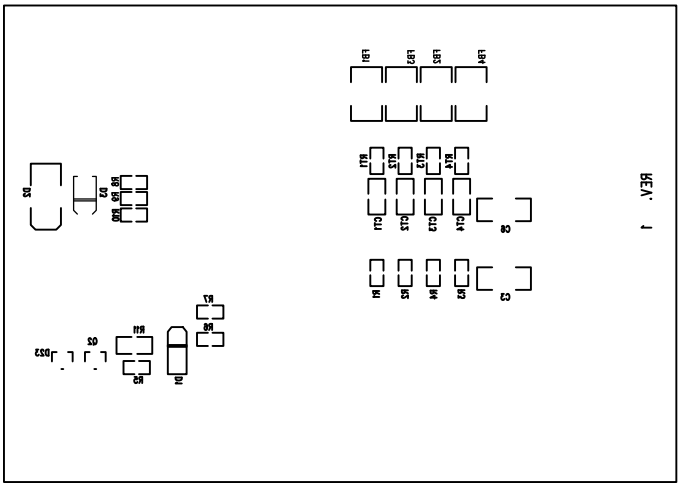
Layer 3. –VIN 2



Layer 4. Bottom Layer



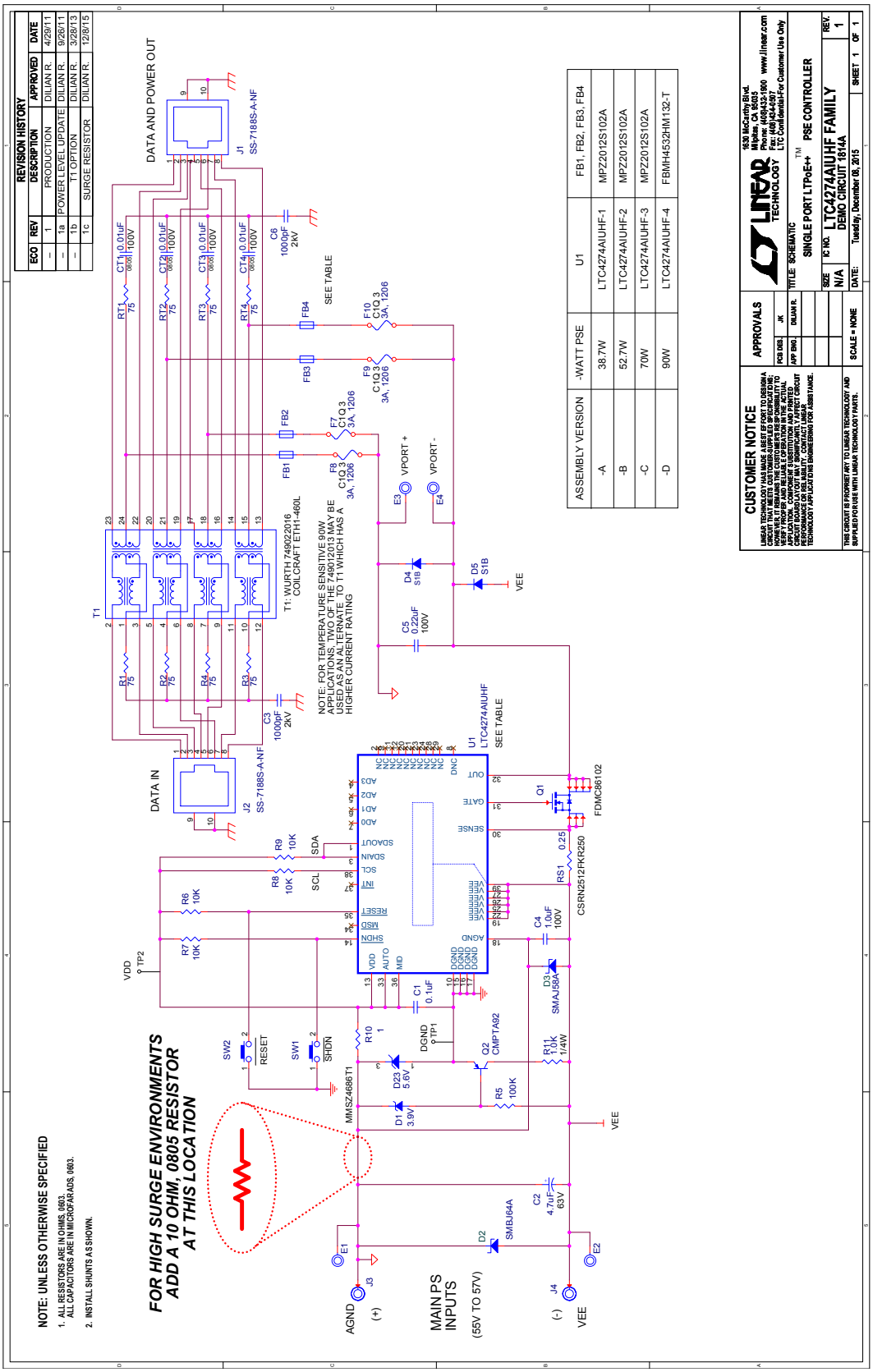
Bottom Silkscreen



PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	1	C1	CAP, 0603 0.1µF 10% 25V X7R	TDK C1608X7R1E104K (BAL. FR#1807)
2	1	C2	CAP, 4.7µF 20% 63V ALUM.	PANASONIC, EEEFK1J4R7R
3	1	C5	CAP, 1206 0.22µF 20% 100V X7R	AVX 12061C224MAT
4	1	C4	CAP, 1210 1.0µF 10% 100V X7R	AVX, 12101C105KAT
5	2	C3, C6	CAP, 1808 1000pF 10% 2KV X7R	TDK C4520X7R3D102K
6	4	CT1-CT4	CAP, 0805 0.01µF 5% 100V X7R	AVX 08051C103JAT
7	2	D4, D5	DIODE, RECTIFIER, 100V 1A, SMA	VISHAY S1B
8	1	D3	DIODE, TVS 58V 400W SMA	DIODES INC., SMAJ58A-13-F
9	1	D2	DIODE, TVS, 64V 600W SMB	DIODES INC., SMBJ64A-13-F
10	1	D1	DIODE, ZENER 3.9V SOD-123	ON SEMI MMSZ4686T1G
11	1	D23	DIODE, ZENER 5.6V 5% SOT23	FAIRCHILD, BZX84C5V6
12	4	E1-E4	TESTPOINT, TURRET, 0.094" PBF	MILL-MAX, 2501-2-00-80-00-00-07-0
13	4	F7-F10	FUSE, 3A, 63VDC 1206	BEL FUSE C1Q 3
14	2	J3, J4	CONN, JACK, BANANA	KEYSTONE 575-4
15	2	J1, J2	CONN, RJ45, SINGLE PORT	STEWART CONN., SS-7188S-A-NF
16	1	R10	RES, 0603 1.0Ω 5% 1/10W	VISHAY CRCW06031R00JNEA
17	4	R6-R9	RES, 0603 10k 5% 1/10W	YAGEO, RC0603JR-0710KL
18	1	R5	RES, 0603 100k 5% 1/10W	YAGEO, RC0603JR-07100KL
19	8	R1-R4, RT1-RT4	RES, 0603 75Ω 5% 1/10W	YAGEO, RC0603JR-0775RL
20	1	R11	RES, THICK FILM 0805 1.0k 5% 1/4W	PANASONIC, ERJ-P06J102V
21	1	RS1	RES, 2512 0.25Ω 1% 2W	STACKPOLE, CSRN2512FKR250
22	4	MH1-MH4	STAND-OFF, NYLON 0.75"	KEYSTONE, 8834(SNAP ON)
23	2	SW1, SW2	SWITCH, MOMENTARY PUSHBUTTON	WÜRTH, 434 123 050 816
24	1	Q1	XSTR, MOSFET, N-CHANNEL 100V 2.3A POWER-33	FAIRCHILD FDMC86102
25	1	Q2	XSTR, PNP, 300V 500MA SOT23 CMPTA92	CENTRAL SEMI CMPTA92
26	1	T1	XFMR, POE+ 1.5A (Option)	WÜRTH ELECTRONICS, 749022016 COILCRAFT ETH1-460L
DC1814A-A				
1	1	DC1814A	GENERAL BOM	
2	4	FB1-FB4	FERRITE BEAD, 1k, 0805	TDK MPZ2012S102A
3	1	U1	IC, LTC4274A-1, SINGLE PORT 38.7W PSE CONTROLLER	LINEAR LTC4274AIUHF-1
4	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1814A
DC1814A-B				
1	1	DC1814A	GENERAL BOM	
2	4	FB1-FB4	FERRITE BEAD, 1k, 0805	TDK MPZ2012S102A
3	1	U1	IC, LTC4274A-2, SINGLE PORT 52.7W PSE CONTROLLER	LINEAR LTC4274AIUHF-2
4	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1814A
DC1814A-C				
1	1	DC1814A	GENERAL BOM	
2	4	FB1-FB4	FERRITE BEAD, 1k, 0805	TDK MPZ2012S102A
3	1	U1	IC, LTC4274A-3, SINGLE PORT 70W PSE CONTROLLER	LINEAR LTC4274AIUHF-3
4	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1814A
DC1814A-D				
1	1	DC1814A	GENERAL BOM	
2	4	FB1-FB4	FERRITE BEAD, 1300Ω, 1812	TAIYO YUDEN FBMH4532HM132-T
3	1	U1	IC, LTC4274A-4, SINGLE PORT 90W PSE CONTROLLER	LINEAR LTC4274AIUHF-4
4	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1814A

SCHEMATIC DIAGRAM



ASSEMBLY DRAWING