18-Bit, 2.5Msps SAR ADC with Pin-Configurable Analog Input Range and 99.8dB SNR

FEATURES

- **2.5Msps Throughput Rate**
- **±3LSB INL (Max)**
- **Guaranteed 18-Bit, No Missing Codes**
- **Pin-Configurable Analog Input Range:**
  - **±4.096V Fully Differential**
  - **0V to 4.096V Pseudo-Differential Unipolar**
  - **±2.048V Pseudo-Differential Bipolar**
- **99.8dB (Fully Differential)/95.2dB (Pseudo Differential) SNR (Typ) at f_{IN} = 2kHz**
- –116dB (Fully Differential)/–112dB (Pseudo Differential) THD (Typ) at f_{IN} = 2kHz
- Guaranteed Operation to 125°C
- Single 5V Supply
- Internal 20ppm/°C (Max) Reference
- Internal Reference Buffer
- 162.5mW Power Dissipation at 2.5Msps
- No Pipeline Delay, No Cycle Latency
- 1.8V to 5V I/O Voltages
- Parallel and Serial I/O Interface
- 48-pin 7mm × 7mm LQFP and QFN Packages

APPLICATIONS

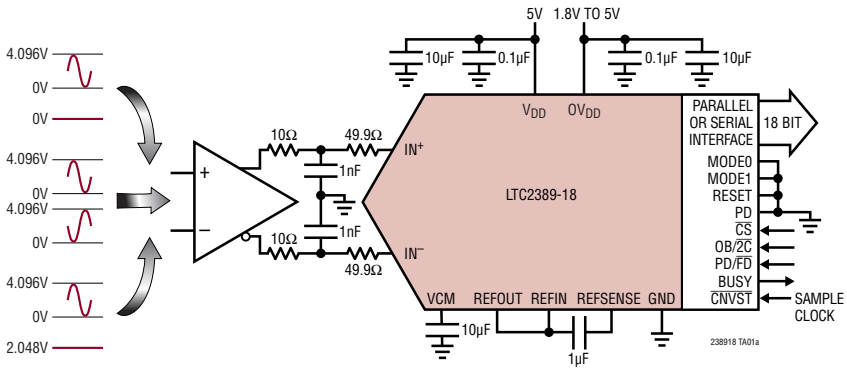
- Medical Imaging
- High Speed, Wide Dynamic Range Data Acquisition
- Industrial Process Control
- Instrumentation
- ATE

DESCRIPTION

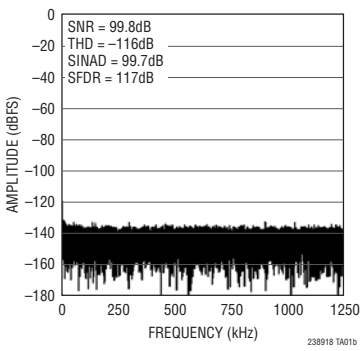
The LTC®2389-18 is a low noise, high speed 18-bit successive approximation register (SAR) ADC. Operating from a single 5V supply, the LTC2389-18 supports pin-configurable fully differential (±4.096V), pseudo-differential unipolar (0V to 4.096V), and pseudo-differential bipolar (±2.048V) analog input ranges, allowing it to interface with multiple signal chain formats without requiring additional level translation or signal conditioning. The LTC2389-18 achieves ±3LSB INL (maximum), no missing codes at 18-bits, and 99.8dB (fully differential)/95.2dB (pseudo differential) SNR (typical).

The LTC2389-18 includes a precision internal 4.096V reference, with a guaranteed 0.5% initial accuracy and a ±20ppm/°C (maximum) temperature coefficient, as well as an internal reference buffer. Fast 2.5Msps throughput with no cycle latency in the parallel interface modes makes the LTC2389-18 ideally suited for a wide variety of high speed applications. An internal oscillator sets the conversion time, easing external timing considerations. The LTC2389-18 dissipates only 162.5mW at 2.5Msps, while both nap and sleep power-down modes are provided to further reduce power consumption during inactive periods.

TYPICAL APPLICATION



32k Point FFT f_{SMPL} = 2.5Msps, f_{IN} = 2kHz

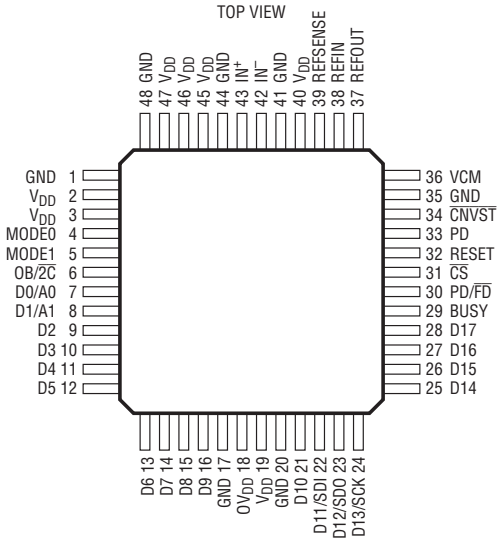


ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

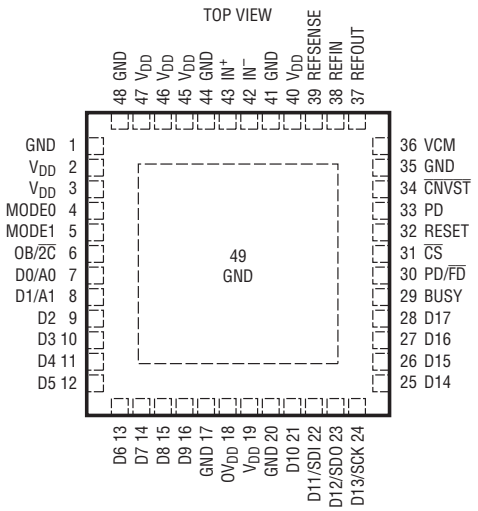
Supply Voltage (V_{DD}, OV_{DD}) 6V
Analog Input Voltage (Note 3)
IN^+, IN^-, REFIN, $\overline{CNVST}$.....(GND – 0.3V) to (V_{DD} + 0.3V)
Digital Input Voltage
(Note 3)..... (GND – 0.3V) to (OV_{DD} + 0.3V)
Digital Output Voltage
(Note 3)..... (GND – 0.3V) to (OV_{DD} + 0.3V)
Power Dissipation 500mW

Operating Temperature Range
LTC2389C ..... 0°C to 70°C
LTC2389I ..... –40°C to 85°C
LTC2389H..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
LX Package..... 300°C

PIN CONFIGURATION



LX PACKAGE
48-LEAD (7mm × 7mm) PLASTIC LQFP
T_{JMAX} = 150°C, θ_{JA} = 50°C/W



UK PACKAGE
48-LEAD (7mm × 7mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 29°C/W
EXPOSED PAD (PIN 49) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2389CUK-18#PBF	LTC2389CUK-18#TRPBF	LTC2389UK-18	48-Lead 7mm × 7mm Plastic QFN	0°C to 70°C
LTC2389IUK-18#PBF	LTC2389IUK-18#TRPBF	LTC2389UK-18	48-Lead 7mm × 7mm Plastic QFN	–40°C to 85°C
LEAD FREE FINISH	**TRAY**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC2389CLX-18#PBF	LTC2389CLX-18#PBF	LTC2389LX-18	48-Lead 7mm × 7mm Plastic LQFP	0°C to 70°C
LTC2389ILX-18#PBF	LTC2389ILX-18#PBF	LTC2389LX-18	48-Lead 7mm × 7mm Plastic LQFP	–40°C to 85°C
LTC2389HLX-18#PBF	LTC2389HLX-18#PBF	LTC2389LX-18	48-Lead 7mm × 7mm Plastic LQFP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN+}	Absolute Input Range (IN^+)	(Note 5)	●	–0.1		V_{REF} + 0.1	V
V_{IN-}	Absolute Input Range (IN^-)	Fully Differential (Note 5)	●	–0.1		V_{REF} + 0.1	V
		Pseudo-Differential Unipolar (Note 5)	●	–0.1	0	0.1	V
		Pseudo-Differential Bipolar (Note 5)	●	$V_{REF}/2$ – 0.1	$V_{REF}/2$	$V_{REF}/2$ + 0.1	V
$V_{IN+} – V_{IN-}$	Input Differential Voltage Range	Fully Differential	●	$–V_{REF}$		V_{REF}	V
		Pseudo-Differential Unipolar	●	0		V_{REF}	V
		Pseudo-Differential Bipolar	●	$–V_{REF}/2$		$V_{REF}/2$	V
V_{CM}	Input Common Mode Voltage Range	Fully Differential	●	$V_{REF}/2$ – 0.1	$V_{REF}/2$	$V_{REF}/2$ + 0.1	V
I_{IN}	Analog Input Leakage Current	C- and I-Grades	●	–1		1	µA
		H-Grade	●	–2		2	µA
C_{IN}	Analog Input Capacitance	Sample Mode			45		pF
		Hold Mode			5		pF
CMRR	Input Common Mode Rejection Ratio				70		dB
$V_{IH\overline{CNVST}}$	$\overline{CNVST}$ High Level Input Voltage		●	1.5			V
$V_{IL\overline{CNVST}}$	$\overline{CNVST}$ Low Level Input Voltage		●			0.5	V
$I_{IN\overline{CNVST}}$	$\overline{CNVST}$ Input Current	V_{IN} = 0V to V_{DD}	●		–25	–60	µA

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	18			Bits
	No Missing Codes		●	18			Bits
	Transition Noise	Fully Differential			0.76		LSB_{RMS}
		Pseudo-Differential Unipolar			1.5		LSB_{RMS}
		Pseudo-Differential Bipolar			1.5		LSB_{RMS}
INL	Integral Linearity Error	Fully Differential (Note 6)	●	–3	±1.25	3	LSB
		Pseudo-Differential Unipolar (Note 6)	●	–3	±1.25	3	LSB
		Pseudo-Differential Bipolar (Note 6)	●	–3	±1.25	3	LSB
DNL	Differential Linearity Error	Fully Differential	●	–0.9	±0.3	0.9	LSB
		Pseudo-Differential Unipolar	●	–0.9	±0.3	0.9	LSB
		Pseudo-Differential Bipolar	●	–0.9	±0.3	0.9	LSB
ZSE	Zero-Scale Error	Fully Differential (Note 7)	●	–10	0	10	LSB
		Pseudo-Differential Unipolar (Note 7)	●	–15	0	15	LSB
		Pseudo-Differential Bipolar (Note 7)	●	–15	0	15	LSB
	Zero-Scale Error Drift				±0.05		ppm/°C
FSE	Full-Scale Error	External Reference (Note 7)	●			0.15	%
		Internal Reference (Note 7)				0.15	%
	Full-Scale Error Drift				±5		ppm/°C

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS (Notes 4, 8)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	Fully Differential, f_{IN} = 2kHz	●	97.3	99.7		dB
		Pseudo-Differential Unipolar, f_{IN} = 2kHz	●	92.2	94.5		dB
		Pseudo-Differential Bipolar, f_{IN} = 2kHz	●	92.7	95.1		dB
		Fully Differential, f_{IN} = 2kHz (H-Grade)	●	96.6	99.7		dB
		Pseudo-Differential Unipolar, f_{IN} = 2kHz (H-Grade)	●	92.0	94.5		dB
		Pseudo-Differential Bipolar, f_{IN} = 2kHz (H-Grade)	●	92.5	95.1		dB
SNR	Signal-to-Noise Ratio	Fully Differential, f_{IN} = 2kHz	●	98.1	99.8		dB
		Pseudo-Differential Unipolar, f_{IN} = 2kHz	●	92.7	94.6		dB
		Pseudo-Differential Bipolar, f_{IN} = 2kHz	●	93.3	95.2		dB
		Fully Differential, f_{IN} = 2kHz (H-Grade)	●	97.7	99.8		dB
		Pseudo-Differential Unipolar, f_{IN} = 2kHz (H-Grade)	●	92.5	94.6		dB
		Pseudo-Differential Bipolar, f_{IN} = 2kHz (H-Grade)	●	93.1	95.2		dB
THD	Total Harmonic Distortion	Fully Differential, f_{IN} = 2kHz, First 5 Harmonics	●		–116	–105	dB
		Pseudo-Differential Unipolar, f_{IN} = 2kHz, First 5 Harmonics	●		–112	–102	dB
		Pseudo-Differential Bipolar, f_{IN} = 2kHz, First 5 Harmonics	●		–111	–102	dB
		Fully Differential, f_{IN} = 2kHz, First 5 Harmonics (H-Grade)	●		–116	–103	dB
		Pseudo-Differential Unipolar, f_{IN} = 2kHz, First 5 Harmonics (H-Grade)	●		–112	–102	dB
		Pseudo-Differential Bipolar, f_{IN} = 2kHz, First 5 Harmonics (H-Grade)	●		–111	–102	dB
SFDR	Spurious-Free Dynamic Range	Fully Differential, f_{IN} = 2kHz	●	106	117		dB
		Pseudo-Differential Unipolar, f_{IN} = 2kHz	●	102	113		dB
		Pseudo-Differential Bipolar, f_{IN} = 2kHz	●	102	112		dB
		Fully Differential, f_{IN} = 2kHz (H-Grade)	●	104	117		dB
		Pseudo-Differential Unipolar, f_{IN} = 2kHz (H-Grade)	●	102	113		dB
		Pseudo-Differential Bipolar, f_{IN} = 2kHz (H-Grade)	●	102	112		dB
	–3dB Input Bandwidth				50		MHz
	Aperture Delay				0.5		ns
	Aperture Jitter				1		ps_{RMS}
	Transient Response	Full-Scale Step			70		ns

REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REFOUT}	Internal Reference Voltage	REFOUT Tied to REFIN, I_{OUT} = 0µA		4.076	4.096	4.116	V
	V_{REFOUT} Tempco	I_{OUT} = 0µA (Note 9)	●		±10	±20	ppm/°C
	REFOUT Output Impedance	–0.1mA ≤ I_{OUT} ≤ 0.1mA			2.3		kΩ
	REFOUT Line Regulation	V_{DD} = 4.75V to 5.25V			0.3		mV/V
V_{REF}	Converter REFIN Voltage			4.076	4.096	4.116	V
	REFIN Input Impedance				74		kΩ
	VCM Output Voltage	I_{OUT} = 0µA			2.08		V

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	0.8 • OV_{DD}			V
V_{IL}	Low Level Input Voltage		●			0.2 • OV_{DD}	V
I_{IN}	Digital Input Current	V_{IN} = 0V to OV_{DD}	●	–10		10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	I_{OUT} = –500µA	●	OV_{DD} – 0.2			V
V_{OL}	Low Level Output Voltage	I_{OUT} = 500µA	●			0.2	V
I_{OZ}	Hi-Z Output Leakage Current	V_{OUT} = 0V to OV_{DD}	●	–10		10	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = OV_{DD}			10		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		●	4.75	5	5.25	V
OV_{DD}	Supply Voltage		●	1.71		5.25	V
I_{VDD}	Core Supply Current	2.5Msps Sample Rate 2.5Msps Sample Rate, Internal Reference Enabled	●		32.5 34.1	36	mA mA
I_{OVDD}	I/O Supply Current	2.5Msps Sample Rate (C_L = 15pF)			1.6		mA
I_{PD}	Power Down Current (I_{VDD} + I_{OVDD})	Conversion Done, P_D = OV_{DD}, Other Digital Inputs Tied to OV_{DD} or GND	●		15	250	µA
P_D	Power Dissipation	2.5Msps Sample Rate Conversion Done, P_D = OV_{DD}, Other Digital Inputs Tied to OV_{DD} or GND			162.5 75	180 1250	mW µW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SMPL}	Sampling Frequency	Parallel Output Modes Serial Output Mode	● ●			2.5 1.9	Msps Msps
t_{CONV}	Conversion Time		●	245	280	310	ns
t_{ACQ}	Acquisition Time	t_{ACQ} = t_{CYC} – t_{CONV} – t_{BUSYLH} (Note 10)	●	77	110		ns
t_{CYC}	Time Between $\overline{CNVST}$↓		●	400			ns
$t_{\overline{CNVST}L}$	$\overline{CNVST}$ Low Time		●	20			ns
$t_{\overline{CNVST}H}$	$\overline{CNVST}$ High Time		●	200			ns
t_{BUSYLH}	$\overline{CNVST}$↓ to BUSY Delay	C_L = 15pF	●			13	ns
t_{RESETH}	RESET Pulse Width		●	200			ns
t_{SCK}	SCK Period	(Notes 5, 11)	●	10			ns
t_{SCKH}	SCK High Time		●	4			ns
t_{SCKL}	SCK Low Time		●	4			ns
t_{DSCK}	SCK↓ Delay From $\overline{CS}$↓		●	10			ns
t_{SSDI}	SDI Setup Time From SCK↓		●	2			ns

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

t_{HSDI}	SDI Hold Time From SCK↓		●	1		ns
t_{DSDO}	SDO Data Valid Delay From SCK↑	C_L = 15pF	●		9	ns
t_{HSDO}	SDO Data Remains Valid Delay From SCK↑	C_L = 15pF	●	1		ns
$t_{DDBUSYL}$	Data Valid to BUSY↓	C_L = 15pF	●	1		ns
t_{EN}	Bus Enable Time After $\overline{CS}$↓		●		11	ns
t_{DDA1A0}	Data Valid Delay From A1 or A0 Transition	C_L = 15pF	●		8	ns
t_{DIS}	Bus Relinquish Time After $\overline{CS}$↑		●		11	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground.

Note 3: When these pin voltages are taken below ground or above V_{DD} or OV_{DD}, they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground, or above V_{DD} or OV_{DD}, without latchup.

Note 4: V_{DD} = 5V, OV_{DD} = 5V, V_{REF} = 4.096V external reference, f_{SMPL} = 2.5MHz, unless otherwise noted.

Note 5: Recommended operating conditions.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Fully differential zero-scale error is the offset voltage measured from –0.5LSB when the output code flickers between 00 0000 0000 0000 0000 and 11 1111 1111 1111 1111 in two's complement format. Unipolar zero-scale error is the offset voltage measured from 0.5LSB when the output code flickers between 00 0000 0000 0000 0000 and 00 0000 0000 0000 0001. Bipolar zero-scale error is the offset voltage measured from –0.5LSB when the output code flickers between 00 0000 0000 0000 0000 and 11 1111 1111 1111 1111. Fully differential full-scale error is the worst-case deviation of the first and last code transitions from ideal and includes the effect of offset error. Unipolar full-scale error is the deviation of the last code transition from ideal and includes the effect of offset error. Bipolar full-scale error is the worst-case deviation of the first and last code transitions from ideal and includes the effect of offset error.

Note 8: All specifications in dB are referred to a full-scale ±4.096V (fully differential), 0V to 4.096V (pseudo-differential unipolar), or ±2.048V (pseudo-differential bipolar) input with a 4.096V reference voltage.

Note 9: Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

Note 10: Guaranteed by design, not subject to test.

Note 11: A t_{SCK} period of 10ns minimum allows a shift clock frequency of up to 100MHz for rising capture.

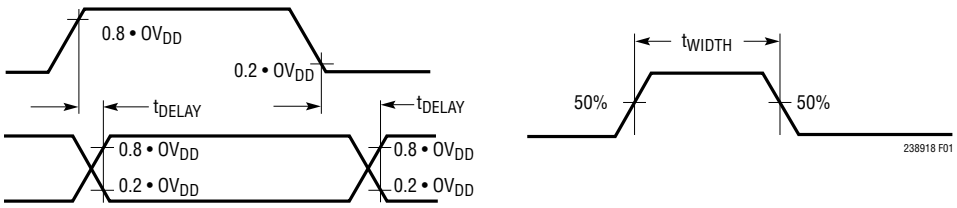
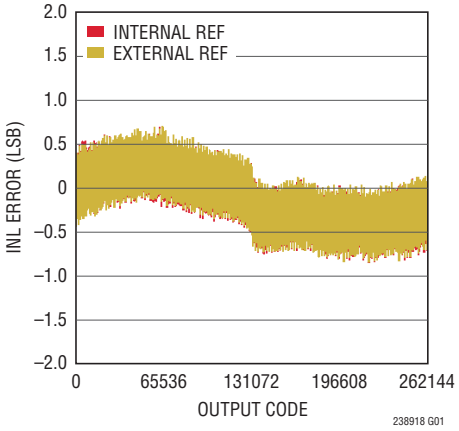


Figure 1. Voltage Levels for Timing Specifications

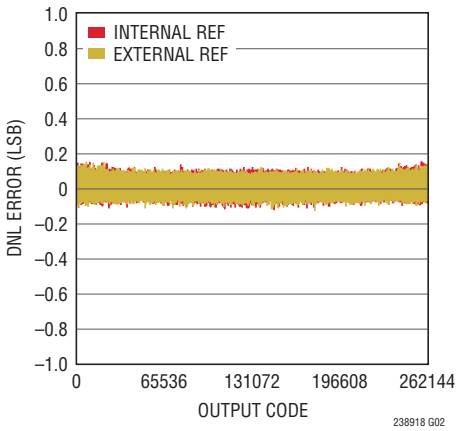
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, V_{REF} = 4.096V External Reference, Fully Differential Range (PD/$\overline{FD}$ = 0V), V_{CM} = 2.048V, f_{SMPL} = 2.5Msps, unless otherwise noted.

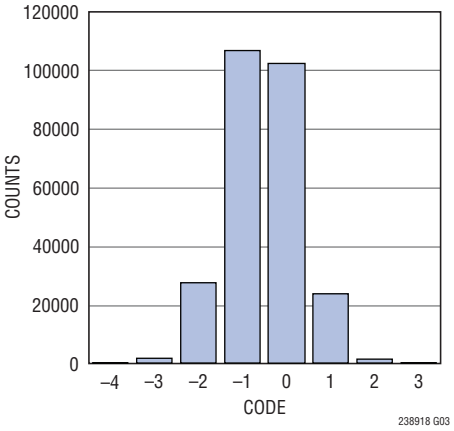
Integral Nonlinearity vs Output Code



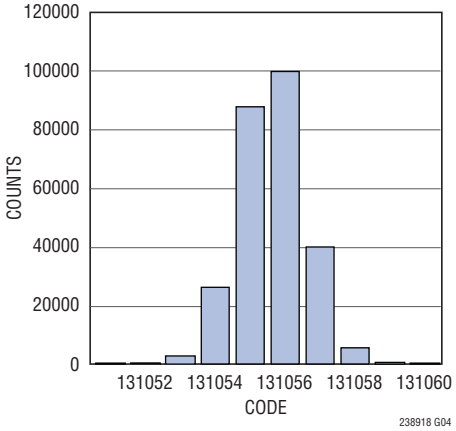
Differential Nonlinearity vs Output Code



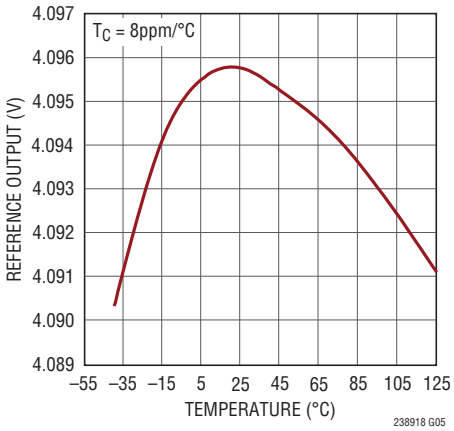
DC Histogram (Zero-Scale)



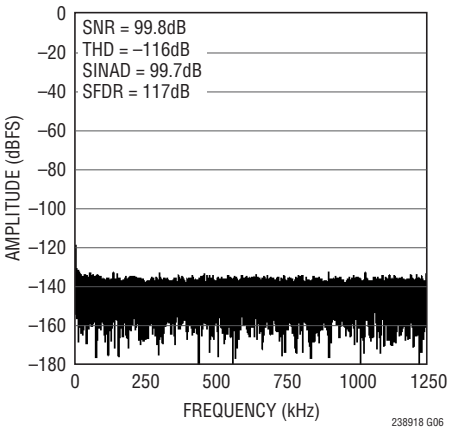
DC Histogram (Near Full-Scale)



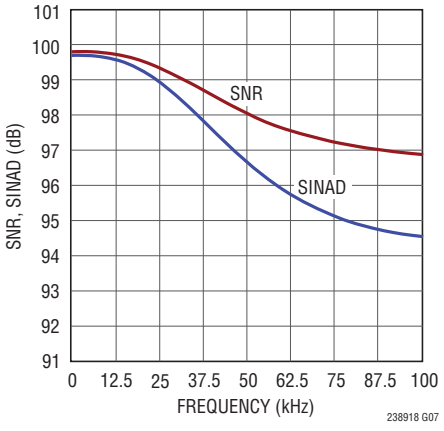
Internal Reference Output vs Temperature



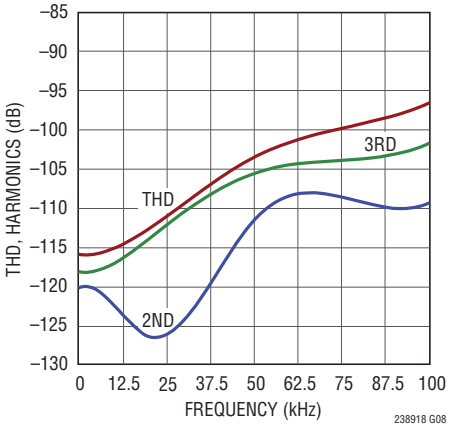
32k Point FFT f_{SMPL} = 2.5Msps, f_{IN} = 2kHz



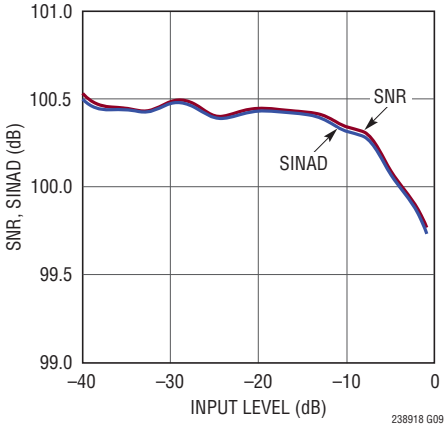
SNR, SINAD vs Input Frequency



THD, Harmonics vs Input Frequency



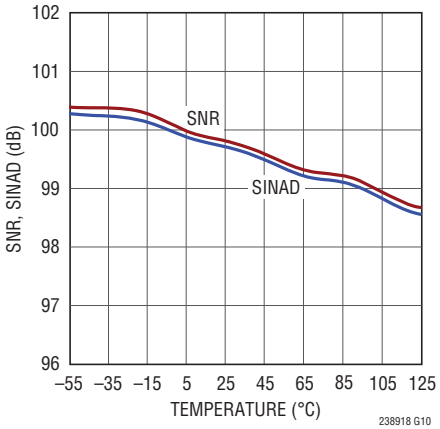
SNR, SINAD vs Input Level, f_{IN} = 2kHz



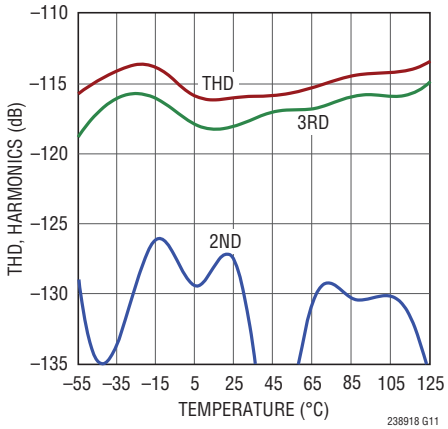
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, V_{REF} = 4.096V
External Reference, Fully Differential Range (PD/$\overline{FD}$ = 0V), V_{CM} = 2.048V, f_{SMPL} = 2.5Msps, unless otherwise noted.

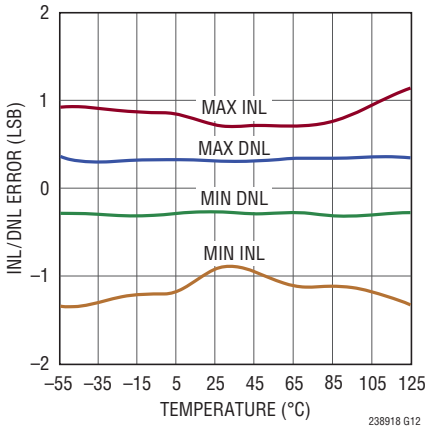
SNR, SINAD vs Temperature, f_{IN} = 2kHz



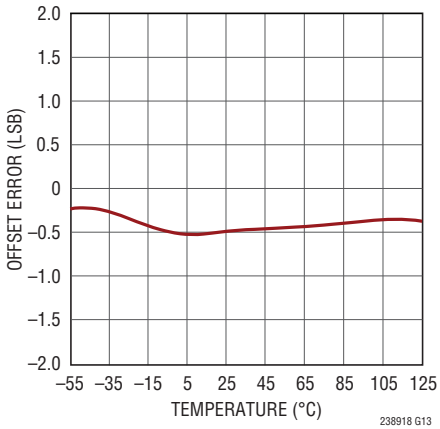
THD, Harmonics vs Temperature, f_{IN} = 2kHz



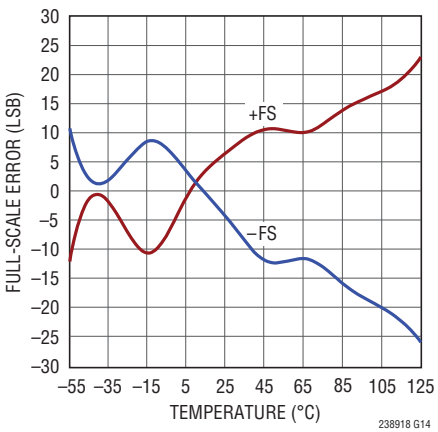
INL/DNL vs Temperature



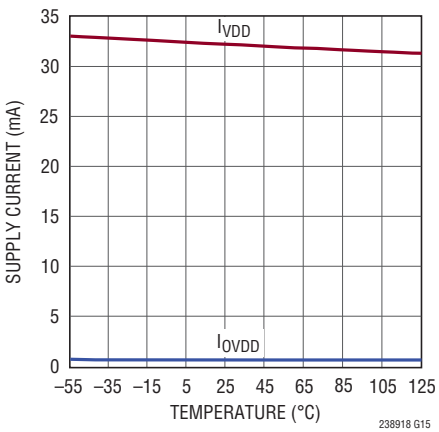
Offset Error vs Temperature



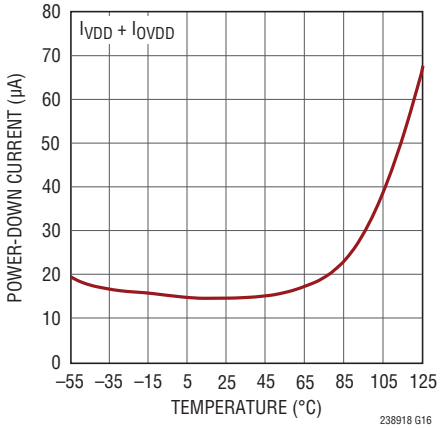
Full-Scale Error vs Temperature



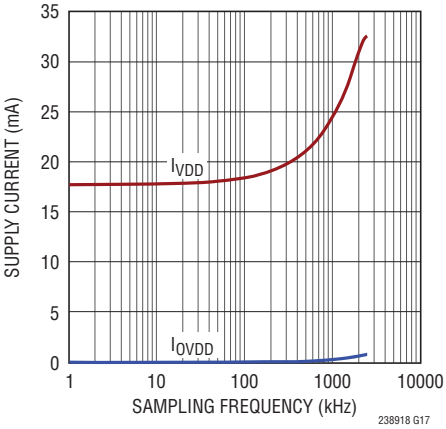
Supply Current vs Temperature



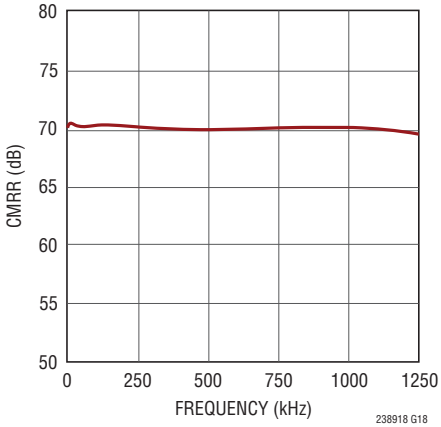
Power-Down Current vs Temperature



Supply Current vs Sampling Frequency



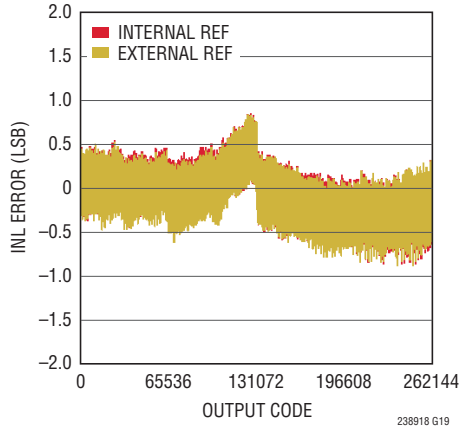
CMRR vs Input Frequency



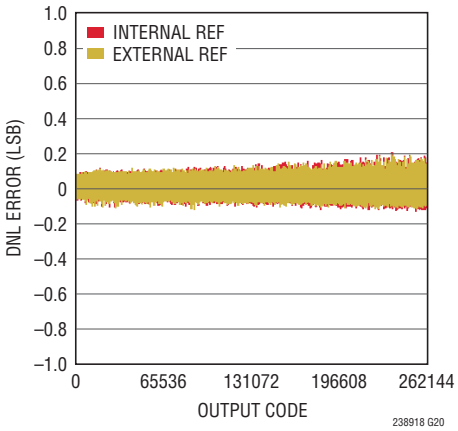
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, V_{REF} = 4.096V
External Reference, Pseudo-Differential Unipolar Range (PD/$\overline{FD}$ = OV_{DD}, OB/$\overline{2C}$ = OV_{DD}), f_{SMPL} = 2.5Msps, unless otherwise noted.

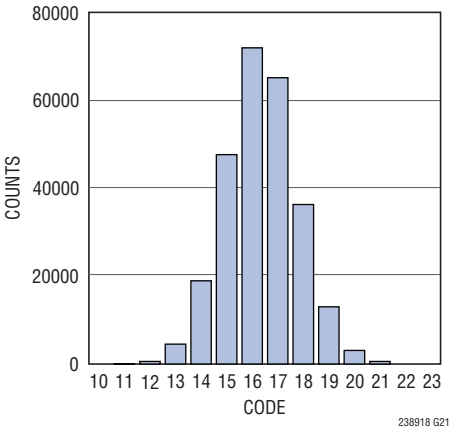
Integral Nonlinearity vs Output Code



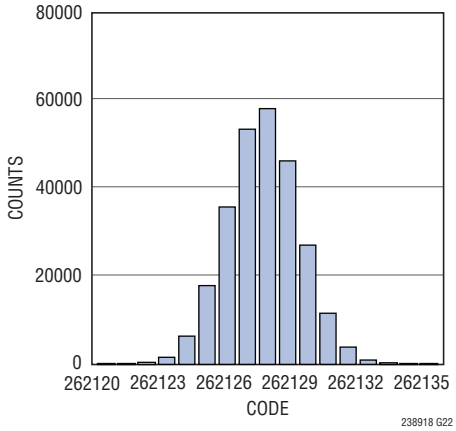
Differential Nonlinearity vs Output Code



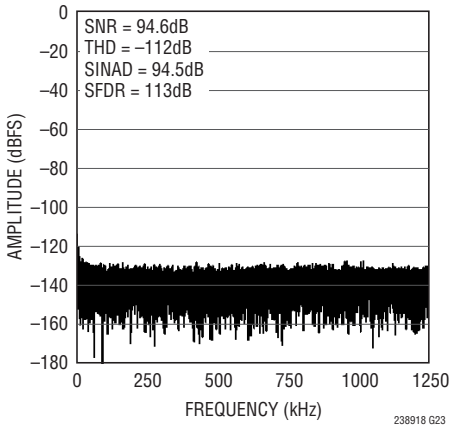
DC Histogram (Near Zero-Scale)



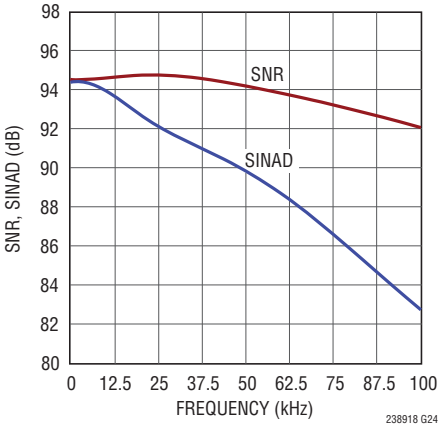
DC Histogram (Near Full-Scale)



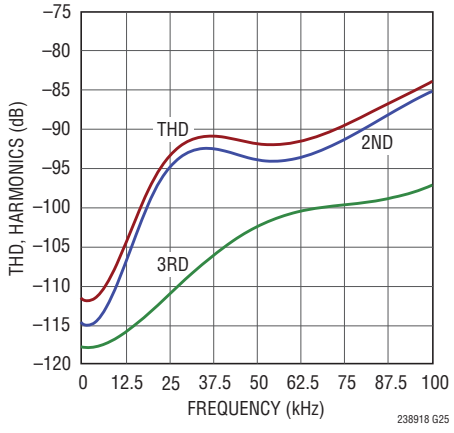
32k Point FFT f_{SMPL} = 2.5Msps, f_{IN} = 2kHz



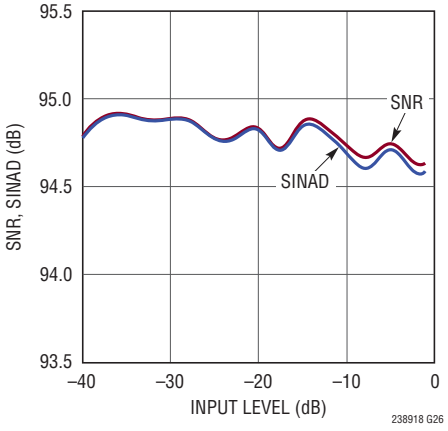
SNR, SINAD vs Input Frequency



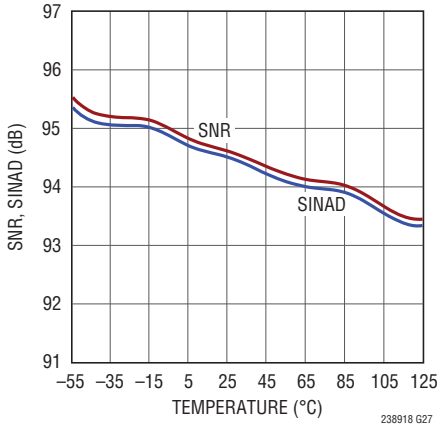
THD, Harmonics vs Input Frequency



SNR, SINAD vs Input Level, f_{IN} = 2kHz



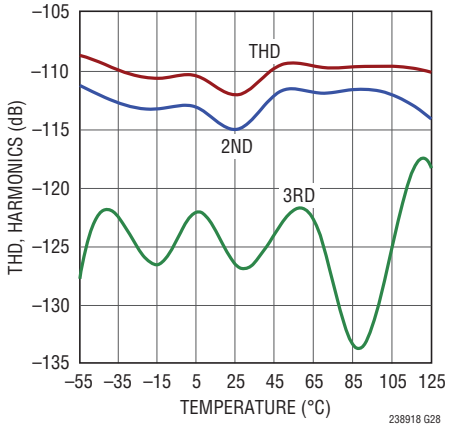
SNR, SINAD vs Temperature, f_{IN} = 2kHz



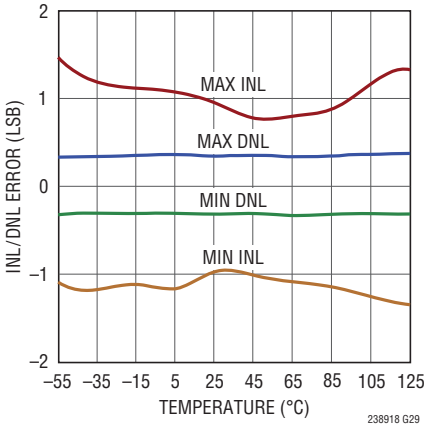
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, V_{REF} = 4.096V
External Reference, Pseudo-Differential Unipolar Range (PD/$\overline{FD}$ = OV_{DD}, OB/$\overline{2C}$ = OV_{DD}), f_{SMPL} = 2.5Msps, unless otherwise noted.

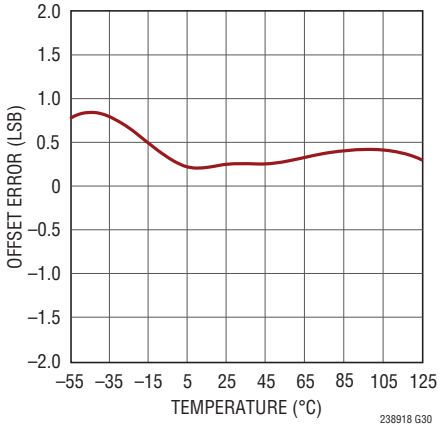
THD, Harmonics vs Temperature, f_{IN} = 2kHz



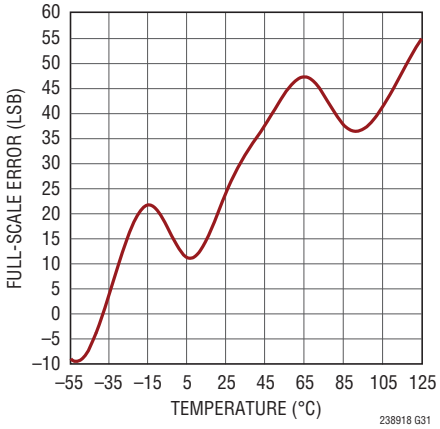
INL/DNL vs Temperature



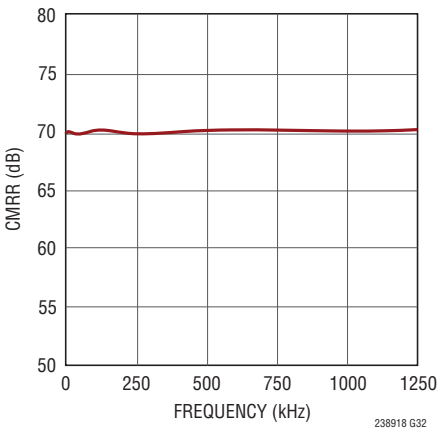
Offset Error vs Temperature



Full-Scale Error vs Temperature



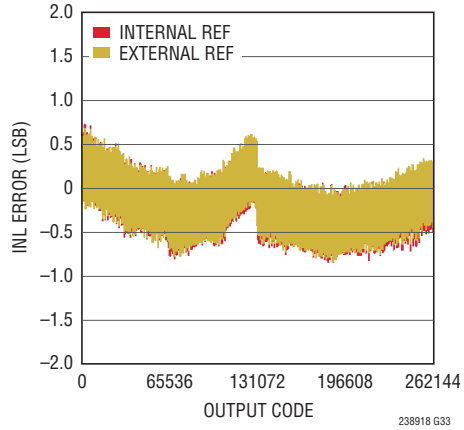
CMRR vs Input Frequency



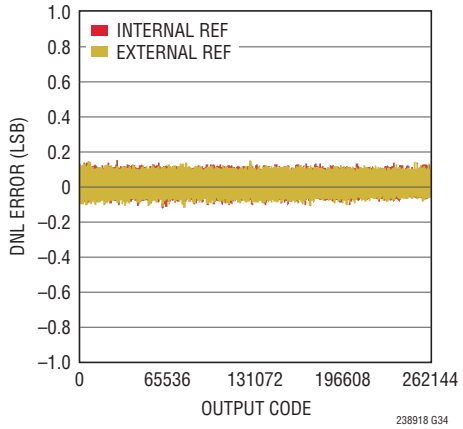
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, V_{REF} = 4.096V
External Reference, Pseudo-Differential Bipolar Range (PD/$\overline{FD}$ = OV_{DD}, OB/$\overline{2C}$ = OV), f_{SMPL} = 2.5Msps, unless otherwise noted.

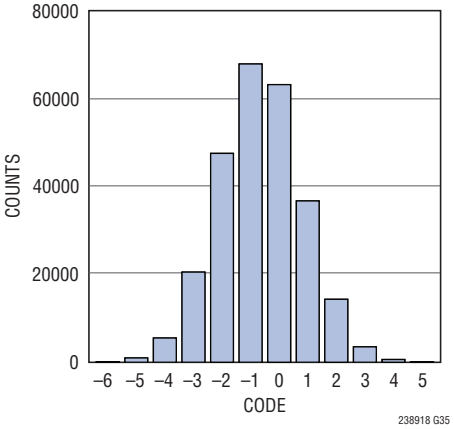
Integral Nonlinearity vs Output Code



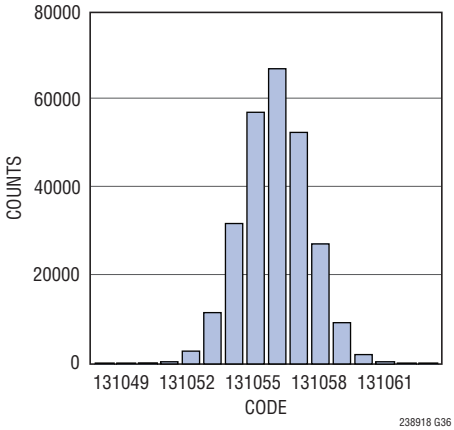
Differential Nonlinearity vs Output Code



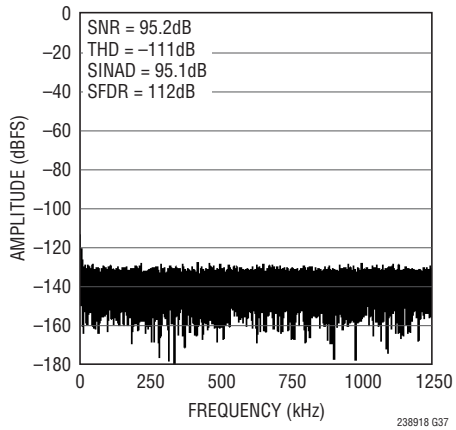
DC Histogram (Zero-Scale)



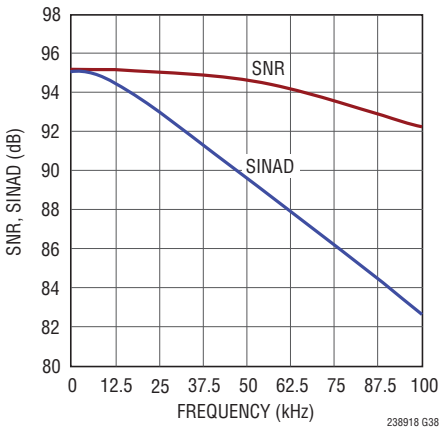
DC Histogram (Near Full-Scale)



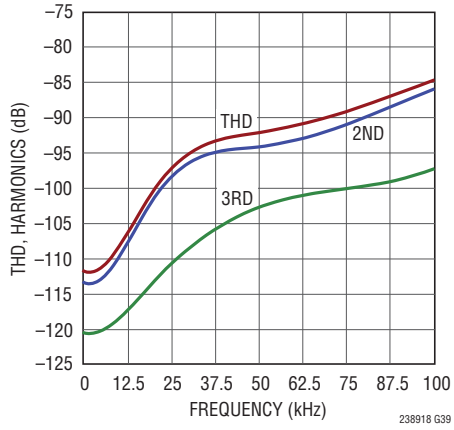
32k Point FFT f_{SMPL} = 2.5Msps, f_{IN} = 2kHz



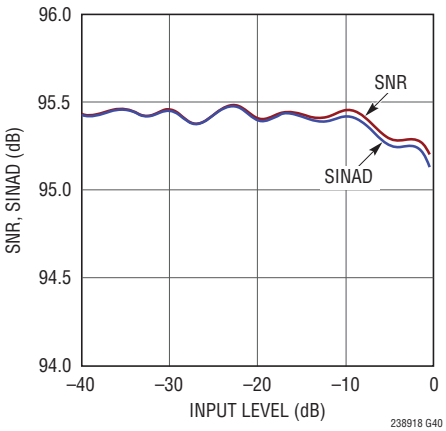
SNR, SINAD vs Input Frequency



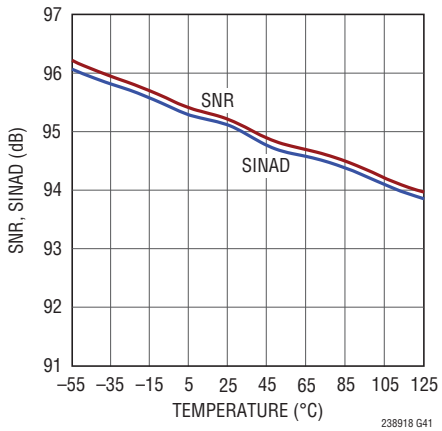
THD, Harmonics vs Input Frequency



SNR, SINAD vs Input Level, f_{IN} = 2kHz



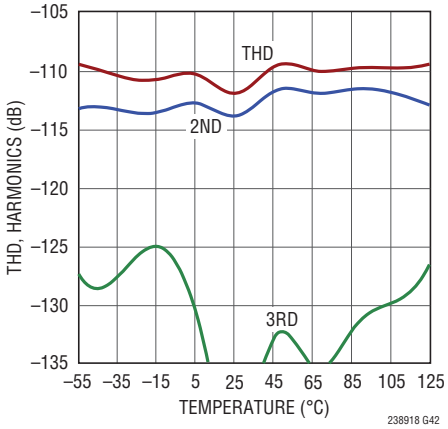
SNR, SINAD vs Temperature, f_{IN} = 2kHz



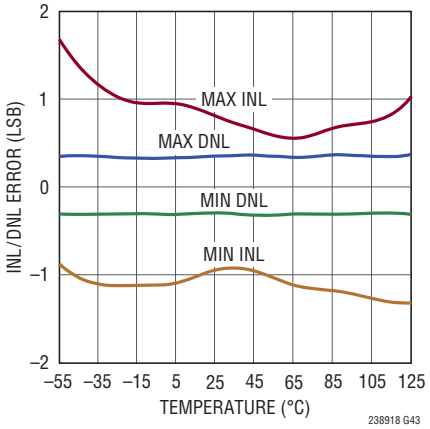
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, V_{REF} = 4.096V
External Reference, Pseudo-Differential Bipolar Range (PD/$\overline{FD}$ = OV_{DD}, OB/$\overline{2C}$ = OV), f_{SMPL} = 2.5Msps, unless otherwise noted.

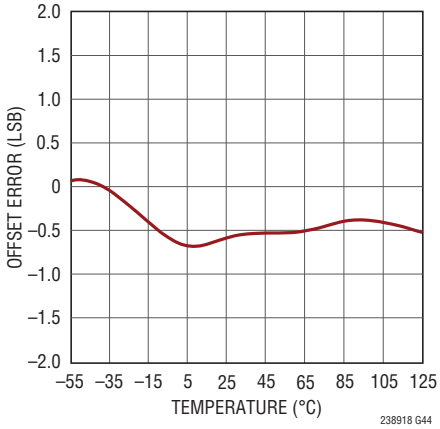
THD, Harmonics vs Temperature, f_{IN} = 2kHz



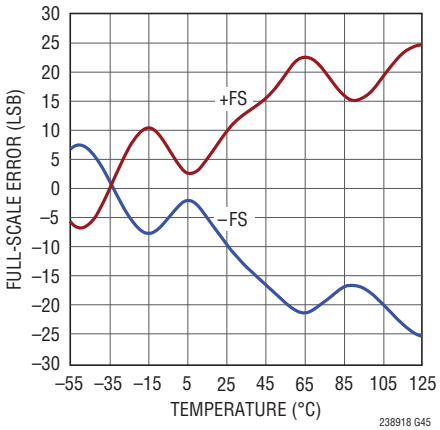
INL/DNL vs Temperature



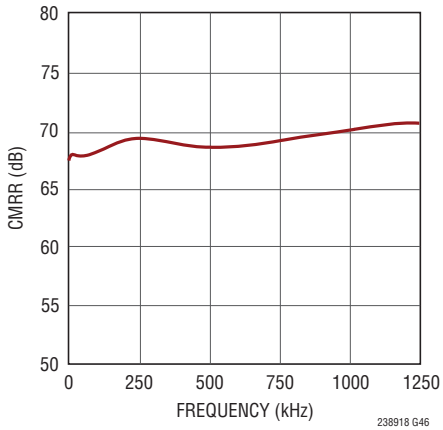
Offset Error vs Temperature



Full-Scale Error vs Temperature



CMRR vs Input Frequency



PIN FUNCTIONS

GND (Pins 1, 17, 20, 35, 41, 44, 48, Exposed Pad Pin 49 (QFN Only)): Ground. Solder all GND pins and exposed pad to the ground plane.

V_{DD} (Pins 2, 3, 19, 40, 45, 46, 47): 5V Power Supply. The range of V_{DD} is 4.75V to 5.25V. Bypass V_{DD} network to GND with a 0.1µF ceramic capacitor close to each pin and a 10µF ceramic capacitor in parallel.

MODE0, MODE1 (Pin 4, Pin 5): Data Bus Configuration Inputs. These pins control the parsing and presentation of conversion results on the output data bus. Based on the state of MODE = MODE[1:0], the bus is configured to provide either 18-bit parallel (MODE = 00), 16-bit parallel (MODE = 01), 8-bit parallel (MODE = 10) or serial (MODE = 11) data, as described in Table 1. Digital outputs that are not active in a particular mode become Hi-Z. Logic levels are determined by OV_{DD}. For information regarding pin compatibility with 16-bit versions of the LTC238x family, refer to the Pin Compatibility with LTC238x-16 section.

OB/$\overline{2C}$ (Pin 6): Offset Binary/Two's Complement Input. This pin, in conjunction with Pin 30 (PD/$\overline{FD}$), controls the analog input range of the converter and the binary format of the conversion result, as described in Table 2. Logic levels are determined by OV_{DD}.

D0/A0 (Pin 7): Data Bit 0/Address Bit 0. When MODE = 00, this pin is Bit 0 of the parallel data output bus. When MODE = 01 or 10, this pin is Bit 0 of the parallel address input bus, where the binary address A[1:0] determines which segment of the conversion result is driven on the upper bits of the output data bus, as described in Table 1. Logic levels are determined by OV_{DD}. For information regarding pin compatibility with 16-bit versions of the LTC238x family, refer to the Pin Compatibility with LTC238x-16 section.

D1/A1 (Pin 8): Data Bit 1/Address Bit 1. When MODE = 00, this pin is Bit 1 of the parallel data output bus. When MODE = 01 or 10, this pin is Bit 1 of the parallel address input bus, where the binary address A[1:0] determines which segment of the conversion result is driven on the upper bits of the output data bus, as described in Table 1. Logic levels are determined by OV_{DD}. For information regarding pin compatibility with 16-bit versions of the LTC238x family, refer to the Pin Compatibility with LTC238x-16 section.

D2 (Pin 9): Data Bit 2. When MODE = 00 or 01, this pin is Bit 2 of the parallel data output bus, as described in Table 1. Logic levels are determined by OV_{DD}.

D3 (Pin 10): Data Bit 3. When MODE = 00 or 01, this pin is Bit 3 of the parallel data output bus, as described in Table 1. Logic levels are determined by OV_{DD}.

D4 (Pin 11): Data Bit 4. When MODE = 00 or 01, this pin is Bit 4 of the parallel data output bus, as described in Table 1. Logic levels are determined by OV_{DD}.

D5 (Pin 12): Data Bit 5. When MODE = 00 or 01, this pin is Bit 5 of the parallel data output bus, as described in Table 1. Logic levels are determined by OV_{DD}.

D6 (Pin 13): Data Bit 6. When MODE = 00 or 01, this pin is Bit 6 of the parallel data output bus, as described in Table 1. Logic levels are determined by OV_{DD}.

D7 (Pin 14): Data Bit 7. When MODE = 00 or 01, this pin is Bit 7 of the parallel data output bus, as described in Table 1. Logic levels are determined by OV_{DD}.

D8 (Pin 15): Data Bit 8. When MODE = 00 or 01, this pin is Bit 8 of the parallel data output bus, as described in Table 1. Logic levels are determined by OV_{DD}.

D9 (Pin 16): Data Bit 9. When MODE = 00 or 01, this pin is Bit 9 of the parallel data output bus, as described in Table 1. Logic levels are determined by OV_{DD}.

OV_{DD} (Pin 18): I/O Interface Power Supply. The range of OV_{DD} is 1.71V to 5.25V. Bypass OV_{DD} to GND close to the pin with a 0.1µF and a 10µF ceramic capacitor in parallel.

D10 (Pin 21): Data Bit 10. When MODE = 00, 01 or 10, this pin is Bit 10 of the parallel data output bus, as described in Table 1. Logic levels are determined by OV_{DD}.

D11/SDI (Pin 22): Data Bit 11/Serial Data Input. When MODE = 00, 01 or 10, this pin is Bit 11 of the parallel data output bus, as described in Table 1. When MODE = 11, this pin is the serial data input, which can be used to daisy chain two or more converters on a single SDO line. The digital data level on SDI is output on SDO with a delay of 18 SCK periods after the start of the read sequence. Logic levels are determined by OV_{DD}.

D12/SDO (Pin 23): Data Bit 12/Serial Data Output. When MODE = 00, 01 or 10, this pin is Bit 12 of the parallel data

PIN FUNCTIONS

output bus, as described in Table 1. When MODE = 11, this pin is the serial data output line, which serially outputs the result of the most recent conversion clocked by SCK. The data is output MSB first on the rising edge of SCK. The data format is determined by the logic levels of pins PD/$\overline{FD}$ and OB/$\overline{2C}$, as described in Table 2. Logic levels are determined by OV_{DD}.

D13/SCK (Pin 24): Data Bit 13/Serial Clock Input. When MODE = 00, 01 or 10, this pin is Bit 13 of the parallel data output bus, as described in Table 1. When MODE = 11, this pin this is the serial clock input. Logic levels are determined by OV_{DD}.

D14 (Pin 25): Data Bit 14. When MODE = 00, 01 or 10, this pin is Bit 14 of the parallel data output bus, as described in Table 1. Logic levels are determined by OV_{DD}.

D15 (Pin 26): Data Bit 15. When MODE = 00, 01 or 10, this pin is Bit 15 of the parallel data output bus, as described in Table 1. Logic levels are determined by OV_{DD}.

D16 (Pin 27): Data Bit 16. When MODE = 00, 01 or 10, this pin is Bit 16 of the parallel data output bus, as described in Table 1. Logic levels are determined by OV_{DD}.

D17 (Pin 28): Data Bit 17. When MODE = 00, 01 or 10, this pin is Bit 17 of the parallel data output bus, as described in Table 1. Logic levels are determined by OV_{DD}.

BUSY (Pin 29): Busy Output. This pin transitions low to high at the start of each conversion and stays high until the conversion is complete. The falling edge of BUSY can be used as the data-ready clock signal. Logic levels are determined by OV_{DD}.

PD/$\overline{FD}$ (Pin 30): Pseudo-Differential/Fully-Differential Input. This pin, in conjunction with Pin 6 (OB/$\overline{2C}$), controls the analog input range of the converter and the binary format of the conversion result, as described in Table 2. Logic levels are determined by OV_{DD}.

$\overline{CS}$ (Pin 31): Chip Select Input. The data I/O bus is enabled when $\overline{CS}$ is low and goes Hi-Z when $\overline{CS}$ is high. $\overline{CS}$ also gates the external shift clock. Logic levels are determined by OV_{DD}.

RESET (Pin 32): Reset Input. When this pin is brought high, the LTC2389-18 is reset. If this occurs during a conversion, the conversion is halted and the data bus becomes Hi-Z. Logic levels are determined by OV_{DD}.

Table 1. Data Bus Configuration Table. Use Inputs MODE1 and MODE0 to Select Bus Configuration Based on Application Bus Width. In 16-Bit and 8-Bit Parallel Configurations, Inputs D1/A1 and D0/A0 Control Mapping of Conversion Result R[17:0] Onto Data Bus Pins D[17:2]. Shaded Cells Denote Bidirectional Pins Configured as Inputs.

BUS CONFIGURATION	MODE1	MODE0	D[17:16]	D[15:14]	D13	D12	D11	D10	D[9:4]	D[3:2]	D1/A1	D0/A0
18-Bit Parallel	0	0	R[17:0]									
16-Bit Parallel	0	1	R[17:2]								X	0
			All Zeros							R[1:0]	0	1
			R[1:0]	All Zeros							1	1
8-Bit Parallel	1	0	R[17:10]						All Hi-Z		0	0
			All Zeros				R[1:0]		All Hi-Z		0	1
			R[9:2]						All Hi-Z		1	0
			R[1:0]	All Zeros					All Hi-Z		1	1
Serial	1	1	All Hi-Z		SCK	SDO	SDI	All Hi-Z				

PIN FUNCTIONS

PD (Pin 33): Power-Down Input. When this pin is brought high, the LTC2389-18 is powered down and subsequent conversion requests are ignored. Before enabling power-down, the result of the last conversion result should be read. Logic levels are determined by OV_{DD}.

$\overline{CNVST}$ (Pin 34): Conversion Start Input. A falling edge on this pin puts the internal sample-and-hold into the hold mode and starts a conversion. $\overline{CNVST}$ is independent of $\overline{CS}$. Logic levels are determined by V_{DD}.

VCM (Pin 36): Common Mode Analog Output. Typically the output voltage on this pin is 2.08V. Bypass to GND with a 10µF capacitor.

REFOUT (Pin 37): Internal Reference Output. Connect this pin to REFIN if using the internal reference, giving a nominal reference voltage of 4.096V. If an external reference is used, connect REFOUT to ground to power down the internal reference.

REFIN (Pin 38): Reference Input. Connect this pin to REFOUT if using the internal reference, giving a nominal reference voltage of 4.096V. An external reference can be applied to REFIN if a more accurate reference is required. If an external reference is used tie REFOUT to ground to power down the internal reference. For increased filtering of reference noise, bypass this pin to REFSENSE using a 1µF, or larger, ceramic capacitor.

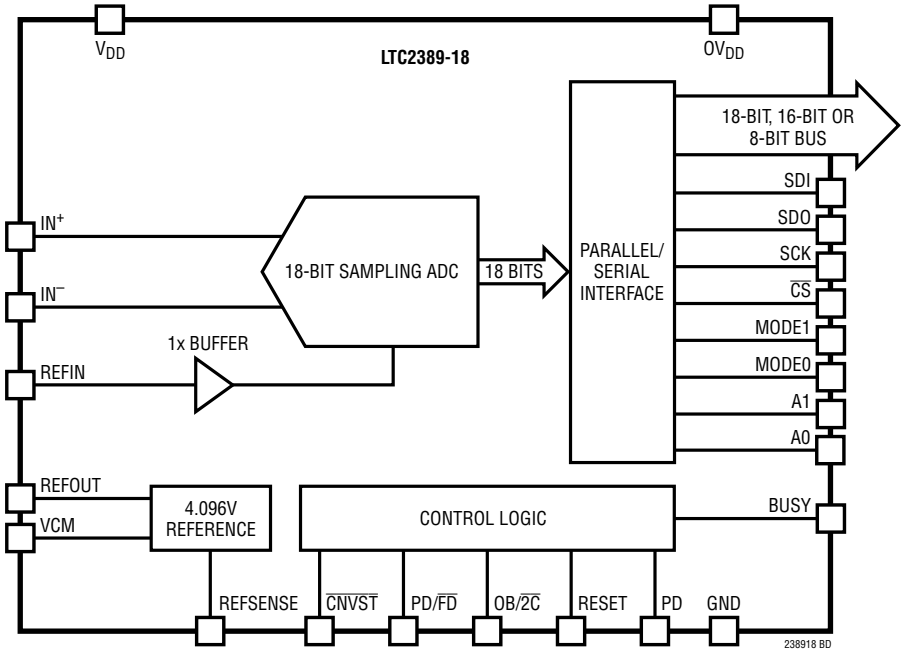
REFSENSE (Pin 39): Reference Input Sense. Do not connect REFSENSE to ground when using the internal reference. If an external reference is used, connect REFSENSE to the ground pin of the external reference.

IN^-, IN^+ (Pin 42, Pin 43): Negative and Positive Analog Inputs. The analog input range depends on the levels applied to Pin 30 (PD/$\overline{FD}$) and Pin 6 (OB/$\overline{2C}$), as described in Table 2.

Table 2. Analog Input Range and Output Binary Format Configuration Table. Use Inputs PD/$\overline{FD}$ and OB/$\overline{2C}$ to Select Converter Analog Input Range and Binary Format of Conversion Result.

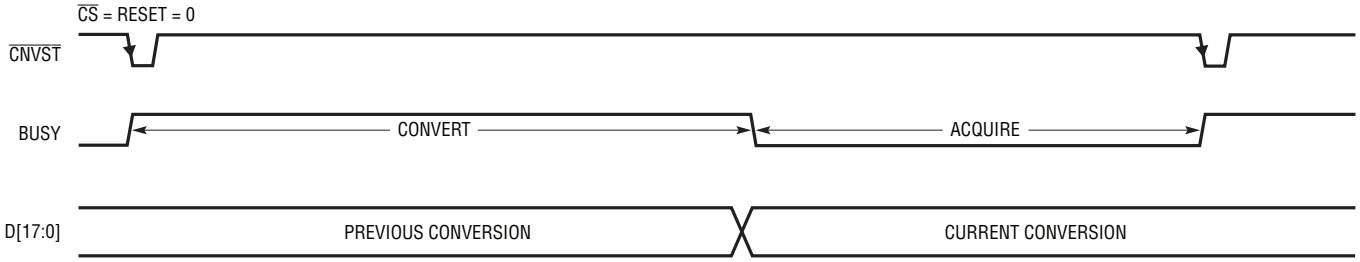
PD/$\overline{FD}$	OB/$\overline{2C}$	ANALOG INPUT RANGE	BINARY FORMAT OF CONVERSION RESULT
0	0	Fully-Differential	Two's Complement
0	1	Fully-Differential	Offset Binary
1	0	Pseudo-Differential Bipolar	Two's Complement
1	1	Pseudo-Differential Unipolar	Straight Binary

FUNCTIONAL BLOCK DIAGRAM

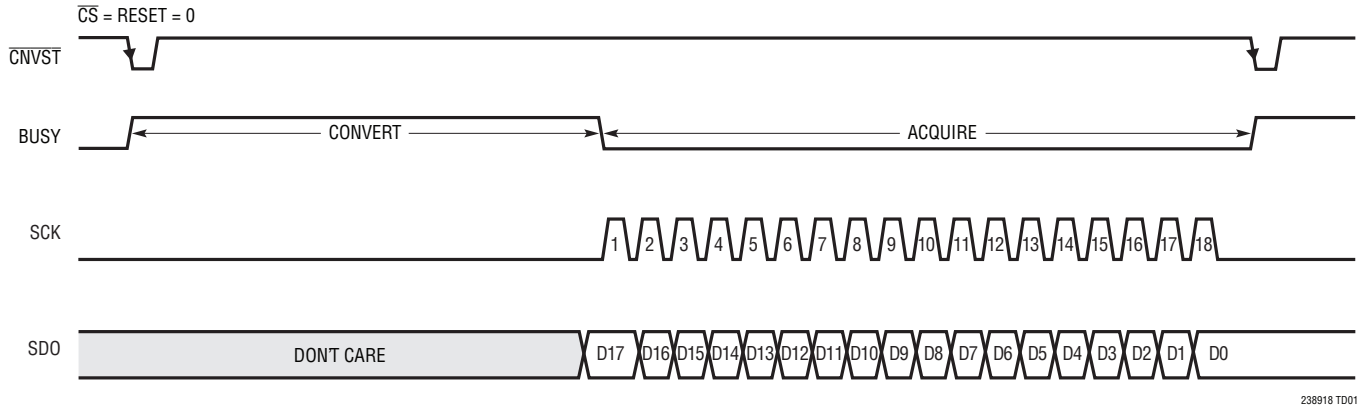


TIMING DIAGRAMS

Conversion Timing Using the Parallel Interface



Conversion Timing Using the Serial Interface



238918 TD01

APPLICATIONS INFORMATION

OVERVIEW

The LTC2389-18 is a low noise, high speed 18-bit successive approximation register (SAR) ADC. Operating from a single 5V supply, the LTC2389-18 supports pin-configurable fully differential (±4.096V), pseudo-differential unipolar (0V to 4.096V) and pseudo-differential bipolar (±2.048V) analog input ranges, allowing it to interface with multiple signal chain formats without requiring additional level translation or signal conditioning. The LTC2389-18 achieves ±3LSB INL (maximum), no missing codes at 18-bits, and 99.8dB (fully differential)/95.2dB (pseudo differential) SNR (typical).

The LTC2389-18 includes a precision internal 4.096V reference, with a guaranteed 0.5% initial accuracy and a ±20ppm/°C (maximum) temperature coefficient, as well as an internal reference buffer. Fast 2.5Msps throughput with no cycle latency in the parallel interface modes makes the LTC2389-18 ideally suited for a wide variety of high speed applications. An internal oscillator sets the conversion time, easing external timing considerations. The LTC2389-18 dissipates only 162.5mW at 2.5Msps, while both nap and sleep power-down modes are provided to further reduce power consumption during inactive periods.

CONVERTER OPERATION

The LTC2389-18 operates in two phases. During the acquisition phase, the charge redistribution capacitor D/A converter (CDAC) is connected to the IN^+ and IN^- pins to sample the differential analog input voltage. A falling edge on the $\overline{CNVST}$ pin initiates a conversion. During the conversion phase, the 18-bit CDAC is sequenced through a successive approximation algorithm, effectively comparing the sampled input with binary-weighted fractions of the reference voltage (e.g., $V_{REF}/2$, $V_{REF}/4$ … $V_{REF}/262144$) using a differential comparator. At the end of conversion, the CDAC output approximates the sampled analog input. The ADC control logic then prepares the 18-bit digital output code for parallel or serial transfer.

TRANSFER FUNCTION

The LTC2389-18 digitizes the full-scale voltage of $2 \bullet V_{REF}$ in fully-differential mode and V_{REF} in pseudo-differential mode, into 2^{18} levels. With $V_{REF} = 4.096V$, the resulting LSB sizes in fully-differential and pseudo-differential mode are 31.25µV and 15.625µV, respectively. The binary format of the conversion result depends on the logic levels on pins PD/$\overline{FD}$ and OB/$\overline{2C}$, as described in Table 2. The ideal two's complement transfer function is shown in Figure 2, while the ideal straight binary transfer function is shown in Figure 3. The ideal offset binary transfer function can be obtained from the two's complement transfer function by inverting the most significant bit (MSB) of each output code.

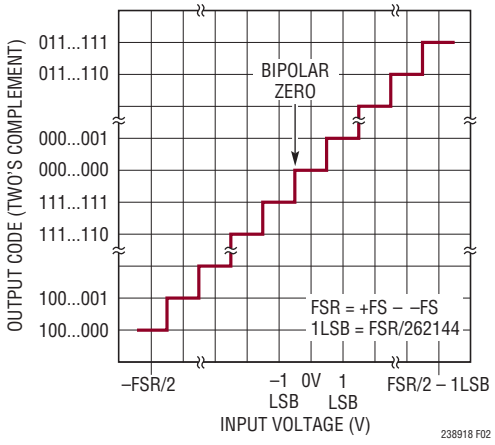


Figure 2. LTC2389-18 Two's Complement Transfer Function. Offset Binary Transfer Function Can Be Obtained by Inverting the Most Significant Bit (MSB) of Each Output Code

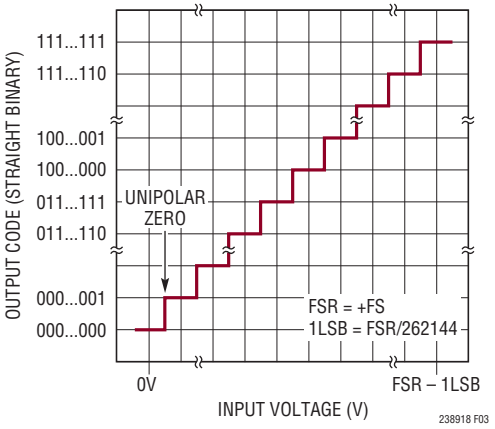


Figure 3. LTC2389-18 Straight Binary Transfer Function

APPLICATIONS INFORMATION

ANALOG INPUT

The analog inputs of the LTC2389-18 can be pin configured to accept one of three input voltage ranges: fully differential (±4.096V), pseudo-differential unipolar (0V to 4.096V), and pseudo-differential bipolar (±2.048V). In all three ranges, the ADC samples and digitizes the voltage difference between the two analog input pins ($IN^+ – IN^–$), and any unwanted signal that is common to both inputs is reduced by the common mode rejection ratio (CMRR) of the ADC. Independent of the selected range, the analog inputs can be modeled by the equivalent circuit shown in Figure 4. The diodes at the input provide ESD protection. In the acquisition phase, each input sees approximately 40pF (C_{IN}) from the sampling CDAC in series with 40Ω (R_{IN}) from the on-resistance of the sampling switch. The inputs draw a small current spike while charging the C_{IN} capacitors during acquisition. During conversion, the analog inputs draw only a small leakage current.

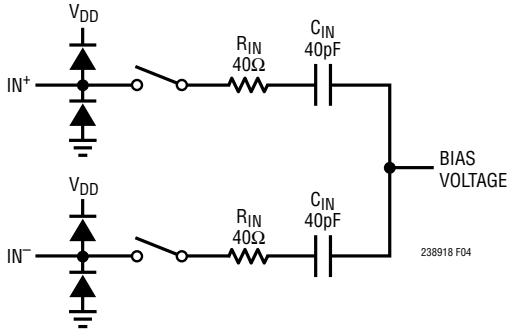


Figure 4. Equivalent Circuit for the Differential Analog Input of the LTC2389-18

Fully Differential Input Range

The fully differential input range provides the widest input signal swing, configuring the ADC to digitize the differential analog input voltage ($IN^+ – IN^–$) over a span of ($±V_{REF}$). In this range, the IN^+ and $IN^–$ pins should be driven 180 degrees out-of-phase with respect to each other, centered around a common mode voltage ($(IN^+ + IN^–)/2$ that is restricted to ($V_{REF}/2 ± 0.1V$). Both the IN^+ and $IN^–$ pins are allowed to swing from (GND – 0.1V) to ($V_{REF} + 0.1V$). Unwanted signals common to both inputs are reduced by the CMRR of the ADC.

Pseudo-Differential Unipolar Input Range

In the pseudo-differential unipolar input range, the ADC digitizes the differential analog input voltage ($IN^+ – IN^–$) over a span of (0V to V_{REF}). In this range, a single-ended unipolar input signal, driven on the IN^+ pin, is measured with respect to the signal ground reference level, driven on the $IN^–$ pin. The IN^+ pin is allowed to swing from (GND – 0.1V) to ($V_{REF} + 0.1V$), while the $IN^–$ pin is restricted to (GND ± 0.1V). Unwanted signals common to both inputs are reduced by the CMRR of the ADC.

Pseudo-Differential Bipolar Input Range

In the pseudo-differential bipolar input range, the ADC digitizes the differential analog input voltage ($IN^+ – IN^–$) over a span of ($±V_{REF}/2$). In this range, a single-ended bipolar input signal, driven on the IN^+ pin, is measured with respect to the signal mid-scale reference level, driven on the $IN^–$ pin. The IN^+ pin is allowed to swing from (GND – 0.1V) to ($V_{REF} + 0.1V$), while the $IN^–$ pin is restricted to ($V_{REF}/2 ± 0.1V$). Unwanted signals common to both inputs are reduced by the CMRR of the ADC.

INPUT DRIVE CIRCUITS

A low impedance source can directly drive the high impedance inputs of the LTC2389-18 without gain error. A high impedance source should be buffered to minimize settling time during acquisition and to optimize the distortion performance of the ADC. Minimizing settling time is important even for DC signals because the ADC inputs draw a current spike when entering acquisition.

For best performance, a buffer amplifier should be used to drive the analog inputs of the LTC2389-18. The amplifier provides low output impedance enabling fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the current spike drawn by the ADC inputs when entering acquisition.

APPLICATIONS INFORMATION

Input Filtering

The noise and distortion of the buffer amplifier and other supporting circuitry must be considered since they add to the ADC noise and distortion. A buffer amplifier with low noise density must be selected to minimize SNR degradation. A filter network should be placed between the buffer output and ADC input to both minimize the noise contribution of the buffer and reduce disturbances reflected into the buffer from ADC sampling transients. A simple one-pole lowpass RC filter is sufficient for many applications. It is important that the RC time constants of this filter be small enough to allow the analog inputs to completely settle to 18-bit resolution within the ADC acquisition time (t_{ACQ}), as insufficient settling can limit INL and THD performance. In many applications an RC time constant of 10ns is fast enough to allow for sufficient transient settling during acquisition while simultaneously filtering driver wideband noise.

Often it is also beneficial to add small series resistors between the primary lowpass RC filter and the ADC inputs. These resistors, in conjunction with the ADC sampling capacitance C_{IN} and sampling switch resistance R_{IN}, form a second lowpass RC filter which further limits high-frequency driver noise as well as reduces the magnitude of the current spike drawn by the analog inputs when entering acquisition. The time constant of this secondary lowpass filter also directly affects settling of the analog inputs during acquisition and must be kept fast. In many applications 49.9Ω series resistors allow for sufficient transient settling during acquisition while providing useful additional filtering of wideband driver noise.

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Fully Differential Inputs

The LTC2389-18 accepts fully differential input signals directly. For most fully differential applications, it is recommended that the LTC2389-18 be driven using the LT6201 ADC driver configured as two unity-gain buffers, as shown in Figure 5a. The LT6201 combines fast settling and good DC linearity with a 0.95nV/$\sqrt{Hz}$ input-referred noise density, enabling it to achieve the full ADC data sheet SNR and THD specifications, as shown in the FFT plot in Figure 5b. This topology may also be used to buffer single-ended signals and achieves full ADC data sheet SNR and THD specifications in both pseudo-differential input modes, as shown in the FFT plots in Figures 5c and 5d.

APPLICATIONS INFORMATION

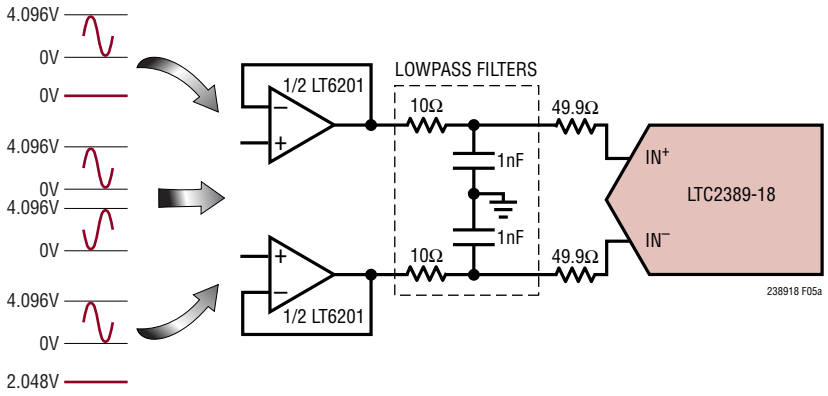


Figure 5a. LT6201 Buffering a Fully-Differential or Single-Ended Signal Source

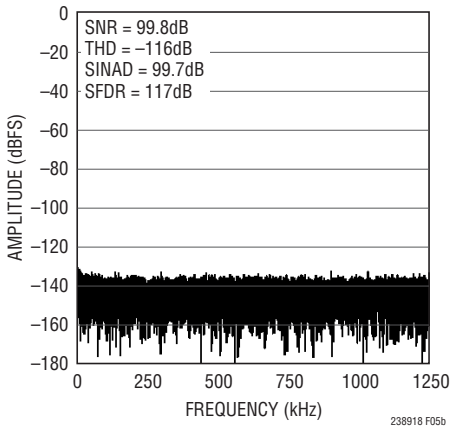


Figure 5b. 32k Point FFT f_{SMPL} = 2.5Msps, f_{IN} = 2kHz, for Circuit Shown in Figure 5a; Driven with Fully Differential Inputs

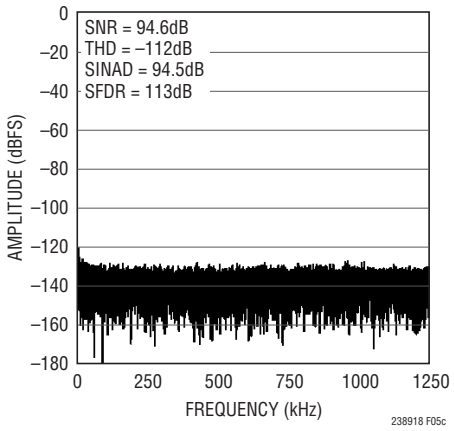


Figure 5c. 32k Point FFT f_{SMPL} = 2.5Msps, f_{IN} = 2kHz, for Circuit Shown in Figure 5a; Driven with Unipolar Inputs

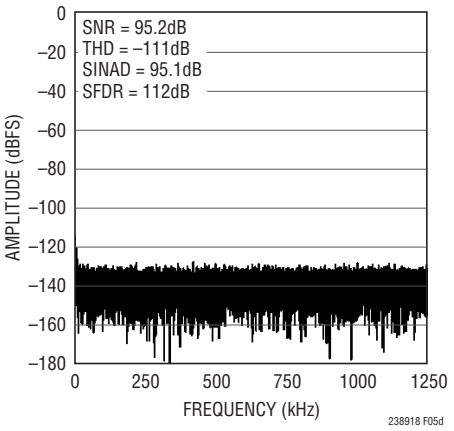


Figure 5d. 32k Point FFT f_{SMPL} = 2.5Msps, f_{IN} = 2kHz, for Circuit Shown in Figure 5a; Driven with Bipolar Inputs

APPLICATIONS INFORMATION

In applications where slightly degraded SNR and THD performance is acceptable, it is possible to drive the LTC2389-18 using the lower power LT6231 ADC driver configured as two unity-gain buffers, as shown in Figure 6a. The RC time constant of the output lowpass filter is larger in this topology to limit the high frequency noise contribution of the LT6231. As shown in the FFT plots in Figures 6b-6d, this circuit achieves 99.2dB SNR and –116dB THD in fully differential input mode, 93.8dB SNR and –111dB THD in unipolar input mode, and 94.2dB SNR and –109dB THD in bipolar input mode.

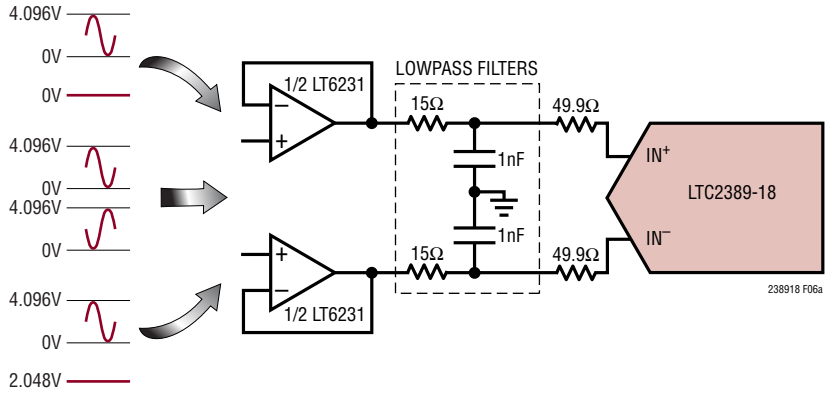


Figure 6a. LT6231 Buffering a Fully-Differential or Single-Ended Signal Source

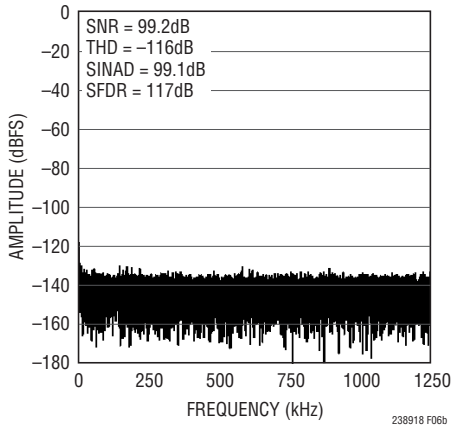


Figure 6b. 32k Point FFT f_{SMPL} = 2.5Msps, f_{IN} = 2kHz, for Circuit Shown in Figure 6a; Driven with Fully Differential Inputs

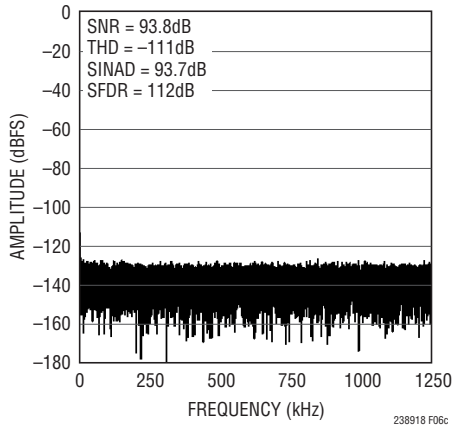


Figure 6c. 32k Point FFT f_{SMPL} = 2.5Msps, f_{IN} = 2kHz, for Circuit Shown in Figure 6a; Driven with Unipolar Inputs

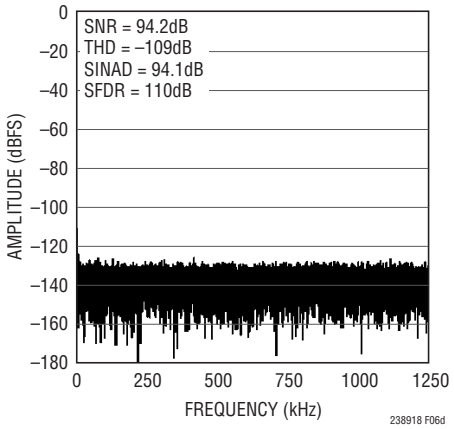


Figure 6d. 32k Point FFT f_{SMPL} = 2.5Msps, f_{IN} = 2kHz, for Circuit Shown in Figure 6a; Driven with Bipolar Inputs

APPLICATIONS INFORMATION

Single-Ended to Differential Conversion

In some applications it may be desirable to convert a single-ended unipolar or bipolar signal to a fully-differential signal prior to driving the LTC2389-18 to take advantage of the higher SNR of the LTC2389-18 in fully differential input mode. The LT6201 ADC driver configured in the topology shown in Figure 7a can be used to convert a 0V to 4.096V single-ended input signal to a fully-differential ±4.096V output signal. The RC time constant of the output lowpass filters is chosen to allow for sufficient transient settling of the LTC2389-18 analog inputs during acquisition. This wide filter bandwidth, coupled with the relatively high wideband noise of the single-ended to differential conversion circuit, limits the achievable SNR of this topology to 98.8dB, as shown in the FFT plot in Figure 7b.

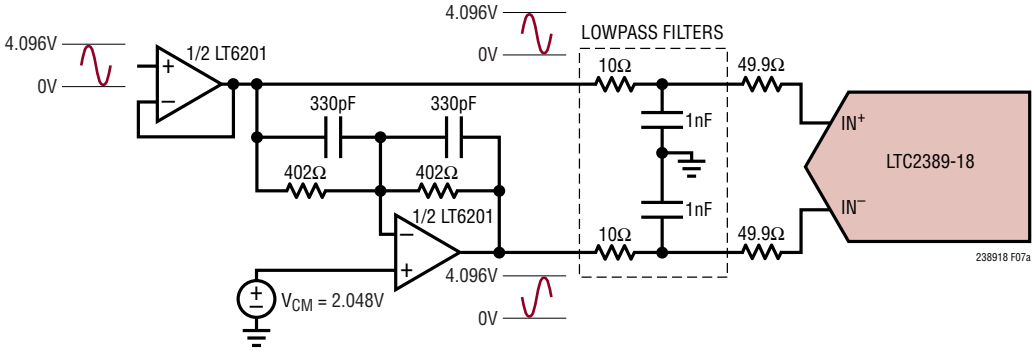


Figure 7a. LT6201 Converting a 0V to 4.096V Single-Ended Signal to a ±4.096V Fully-Differential Signal

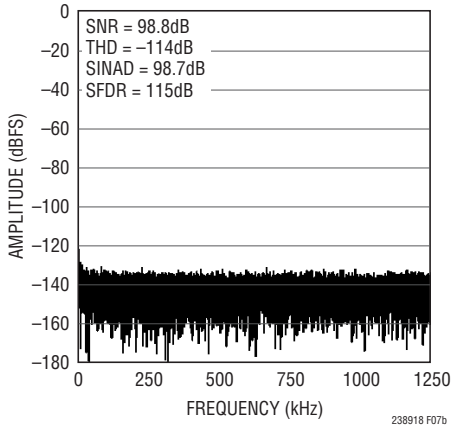


Figure 7b. 32k Point FFT f_{SMPL} = 2.5Msps, f_{IN} = 2kHz, for Circuit Shown in Figure 7a

APPLICATIONS INFORMATION

An alternate single-ended to differential topology employing the LT6231 followed by the LT6201 is shown in Figure 8a. This topology enables additional band-limiting of the wideband noise of the single-ended to differential conversion circuit using lowpass filters A without affecting the settling at the inputs of the LTC2389-18 during acquisition. This circuit achieves the full ADC data sheet SNR specifications, as shown in the FFT plot in Figure 8b.

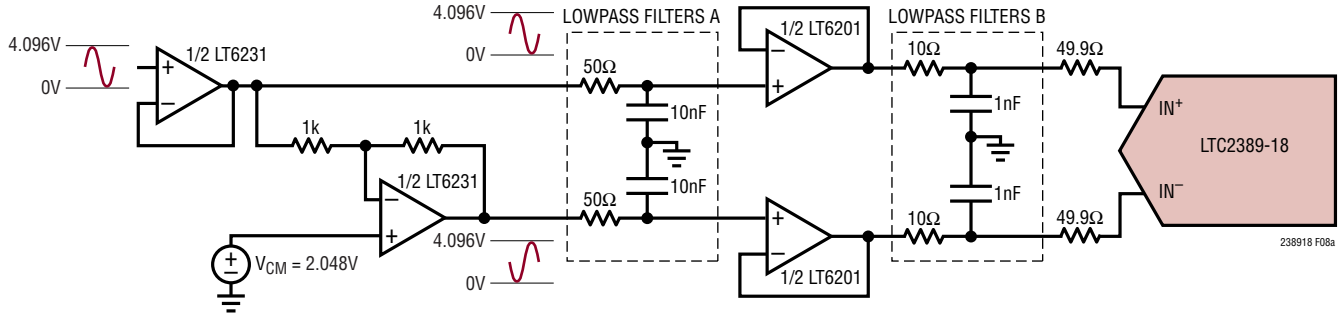


Figure 8a. LT6231 Converting a 0V to 4.096V Single-Ended Signal to a ±4.096V Fully-Differential Signal Followed by LT6201 Buffering Fully-Differential Signal

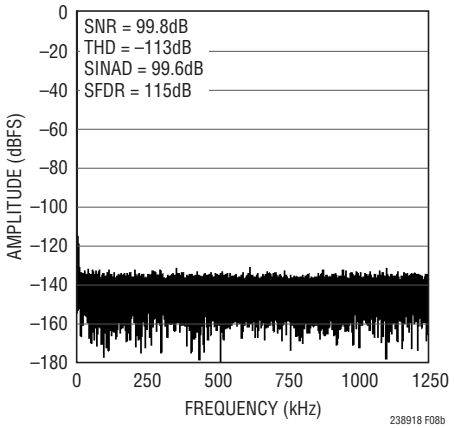


Figure 8b. 32k Point FFT f_{SMPL} = 2.5Msps, f_{IN} = 2kHz, for Circuit Shown in Figure 8a

APPLICATIONS INFORMATION

Single-Ended Unipolar and Bipolar Inputs

The LTC2389-18 accepts both single-ended unipolar and single-ended bipolar input signals directly. For most single-ended applications, it is recommended that the LTC2389-18 be driven using the LT6200 ADC driver configured as a unity-gain buffer, as shown in Figure 9a. The LT6200 combines fast settling and good DC linearity with a 0.95nV/$\sqrt{Hz}$ input-referred noise density, enabling it to achieve the full ADC data sheet SNR and THD specifications in both pseudo-differential input modes, as shown in the FFT plots in Figures 9b and 9c.

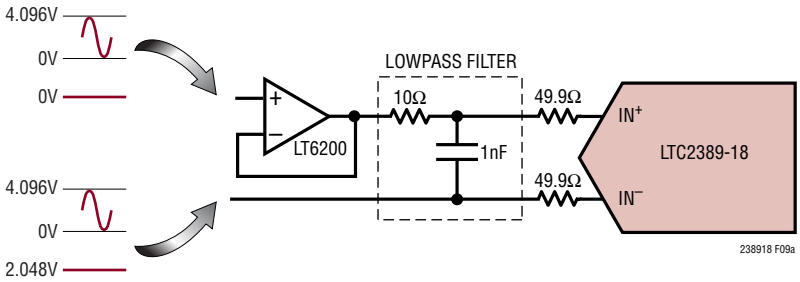


Figure 9a. LT6200 Buffering a Single-Ended Signal Source

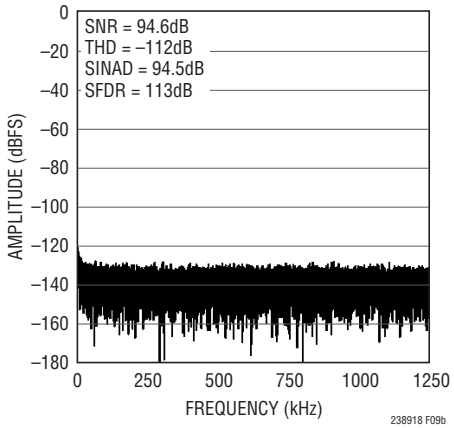


Figure 9b. 32k Point FFT f_{SMPL} = 2.5Msps, f_{IN} = 2kHz, for Circuit Shown in Figure 9a; Driven with Unipolar Inputs

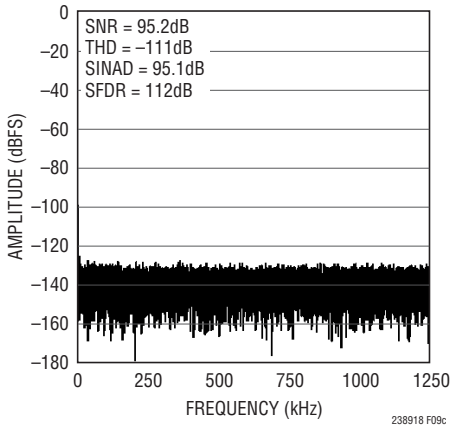


Figure 9c. 32k Point FFT f_{SMPL} = 2.5Msps, f_{IN} = 2kHz, for Circuit Shown in Figure 9a; Driven with Bipolar Inputs

APPLICATIONS INFORMATION

In applications where slightly degraded SNR and THD performance is acceptable, it is possible to drive the LTC2389-18 using the lower power LT6230 ADC driver configured as a unity-gain buffer, as shown in Figure 10a. The RC time constant of the output lowpass filter is larger in this topology to limit the high frequency noise contribution of the LT6230. As shown in the FFT plots in Figures 10b and 10c, this circuit achieves 94dB SNR and –111dB THD in unipolar input mode and 94.5dB SNR and –110dB THD in bipolar input mode.

Note that in the circuits of Figures 9a and 10a, the source impedance of the signal applied to IN^- directly affects input settling time during signal acquisition. In single-ended applications where the impedance of this reference signal is intrinsically high, the dual-buffer approach shown in Figures 5a and 6a will provide for faster acquisition time and better distortion performance from the ADC.

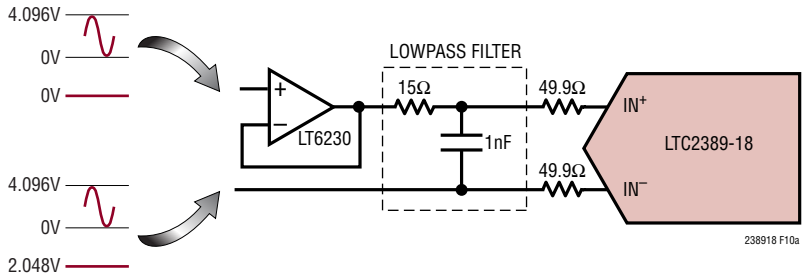


Figure 10a. The LT6230 Buffering a Single-Ended Signal Source

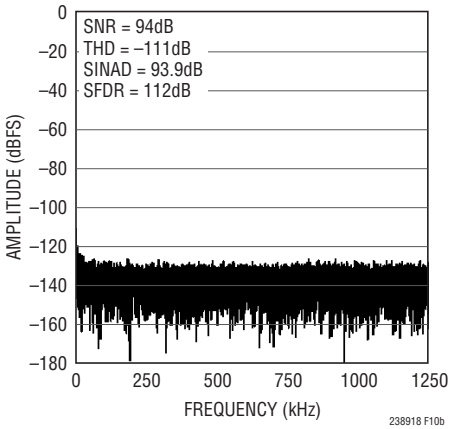


Figure 10b. 32k Point FFT f_{SMPL} = 2.5Msps, f_{IN} = 2kHz, for Circuit Shown in Figure 10a; Driven with Unipolar Inputs

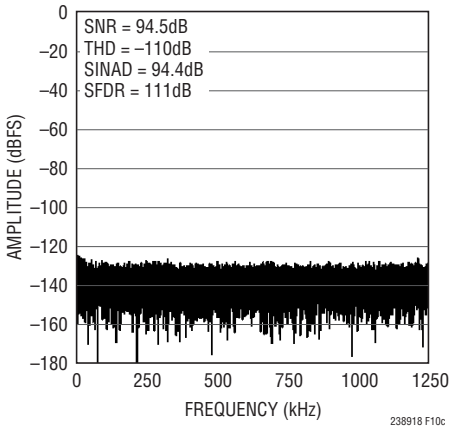


Figure 10c. 32k Point FFT f_{SMPL} = 2.5Msps, f_{IN} = 2kHz, for Circuit Shown in Figure 10a; Driven with Bipolar Inputs

APPLICATIONS INFORMATION

ADC REFERENCE

A low noise, low temperature drift reference is critical to achieving the full data sheet performance of the ADC. The LTC2389-18 provides an excellent internal reference with a ±20ppm/°C (maximum) temperature coefficient. If even better accuracy is required, an external reference can be used. In both cases, the high speed, low noise internal reference buffer is employed and cannot be bypassed. The buffer contributes a signal-dependent noise term to the converter with a typical standard deviation of:

$$\frac{(V_{IN+} - V_{IN-})}{V_{REF}} \bullet 16\mu V_{RMS},$$

which accounts for the increase in transition noise between zero-scale and full-scale inputs. The reference voltage applied to REFIN adds a similar signal-dependent noise term, but its magnitude is limited by a 4kHz (typical) lowpass filter in the internal buffer, making this term negligible in most cases.

Internal Reference

To use the internal reference, simply tie the REFOUT and REFIN pins together. This connects the 4.096V output of the internal reference to the input of the internal reference buffer. The output impedance of the internal reference is approximately 2.3kΩ and the input impedance of the internal reference buffer is about 74kΩ. It is recommended REFIN be bypassed to REFSENSE with a 1µF, or larger, capacitor to filter the output noise of the internal reference. Do not ground the REFSENSE pin when using the internal reference.

External Reference

An external reference can be used with the LTC2389-18 when even higher performance is required. The LTC6655 offers 0.025% (maximum) initial accuracy and 2ppm/°C (maximum) temperature coefficient for high precision applications. The LTC6655 is fully specified over the H-grade temperature range and complements the extended temperature operation of the LTC2389-18 up to 125°C. When using an external reference, connect the reference output to the REFIN pin and connect the REFOUT pin to ground. The REFSENSE pin should be connected to the ground of the external reference.

DYNAMIC PERFORMANCE

Fast fourier transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2389-18 provides guaranteed tested limits for both AC distortion and noise measurements.

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the A/D output. The output is band-limited to frequencies from above DC and below half the sampling frequency. Figure 11 shows that the LTC2389-18 achieves a typical SINAD of 99.7dB (fully differential) at a 2.5MHz sampling rate with a 2kHz input.

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 11 shows that the LTC2389-18 achieves a typical SNR of 99.8dB (fully differential) at a 2.5MHz sampling rate with a 2kHz input.

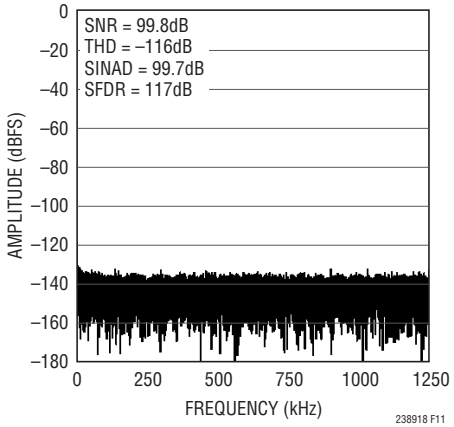


Figure 11. 32k Point FFT of LTC2389-18, f_{SMPL} = 2.5Msps, f_{IN} = 2kHz

APPLICATIONS INFORMATION

Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\frac{\sqrt{V2^2 + V3^2 + V4^2 + \ldots + V_N^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through V_N are the amplitudes of the second through Nth harmonics, respectively. Figure 11 shows that the LTC2389-18 achieves a typical THD of –116dB (fully differential) at a 2.5MHz sampling rate with a 2kHz input.

POWER CONSIDERATIONS

The LTC2389-18 provides two sets of power supply pins: the 5V core power supply (V_{DD}) and the digital input/output interface power supply (OV_{DD}). The flexible OV_{DD} supply allows the LTC2389-18 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems. Both the V_{DD} and OV_{DD} supply networks should be bypassed to GND with a 0.1µF ceramic capacitor close to each pin and a 10µF ceramic capacitor in parallel.

Power Supply Sequencing

The LTC2389-18 does not have any specific power supply sequencing requirements. Care should be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2389-18 has an internal power-on reset (POR) circuit which resets the converter on initial power-up or whenever the power supply voltage drops below 2.5V. Once the supply voltage re-enters the nominal supply voltage range, the POR reinitializes the ADC. With the POR, the result of the first conversion is valid after power-up as long as the reference has been given sufficient time to settle.

Nap Mode

The LTC2389-18 can be put into nap mode after a conversion has been completed to reduce the power consumption between conversions. In this mode some of the circuitry on the device is turned off. Nap mode is enabled by keeping $\overline{CNVST}$ low between conversions, as shown in Figure 12. To initiate a new conversion after entering nap mode, bring $\overline{CNVST}$ high and hold for at least 200ns before bringing it low again.

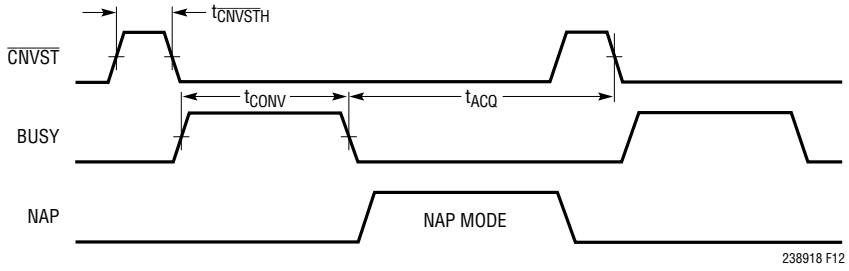


Figure 12. Nap Mode Timing for the LTC2389-18

APPLICATIONS INFORMATION

Power Shutdown Mode

When PD is tied high, the LTC2389-18 enters power shutdown. In this state, all internal functions, including the reference, are turned off and subsequent conversion requests are ignored. Before entering power shutdown, the digital output data should be read. If a request for power shutdown occurs during a conversion, the conversion will finish and then the device will power down, but the data from that conversion should be read only after power shutdown mode has ended. In this mode, power consumption drops to a typical value of 75µW from 162.5mW. This mode can be used if the LTC2389-18 is inactive for a long period of time and the user wants to minimize power dissipation.

Recovery From Power Shutdown Mode

To end the power shutdown and begin powering up the internal circuitry, return the PD pin to a low level. If the internal reference is used, the 2.3kΩ output impedance with the 1µF bypass capacitor on the REFIN/REFOUT pins will be the main time constant for the power-on recovery time. If an external reference is used, typically allow 5ms for recovery before initiating a new conversion.

Power Dissipation vs Sampling Frequency

When nap mode is employed, the power dissipation of the LTC2389-18 will decrease as the sampling frequency is reduced, as shown in Figure 13. This decrease in average power dissipation occurs because a portion of the circuitry on the LTC2389-18 is turned off during nap mode and the fraction of the conversion cycle (t_{CYC}) spent napping increases as the sampling frequency (f_{SMPL}) is decreased.

TIMING AND CONTROL

$\overline{CNVST}$ Timing

The LTC2389-18 conversion is controlled by $\overline{CNVST}$. A falling edge on $\overline{CNVST}$ initiates the conversion process, which once begun, cannot be restarted until the conversion is complete. For optimum performance, $\overline{CNVST}$ should be driven by a clean, low jitter signal and transitions on data I/O lines should be avoided leading up to the falling edge of $\overline{CNVST}$. Converter status is indicated by the BUSY output, which remains high while the conversion is in progress. Once $\overline{CNVST}$ is brought low to begin a conversion, it should be returned high either within 40ns from the start of the conversion or after the conversion is complete to ensure no errors occur in the digitized results. The $\overline{CNVST}$ timing required to take advantage of the reduced power nap mode of operation is described in the Nap Mode section.

Internal Conversion Clock

The LTC2389-18 has an internal clock that is trimmed to achieve a maximum conversion time of 310ns. No external adjustments are required and with a minimum acquisition time of 77ns, a throughput performance of 2.5Msps is guaranteed in the parallel output modes.

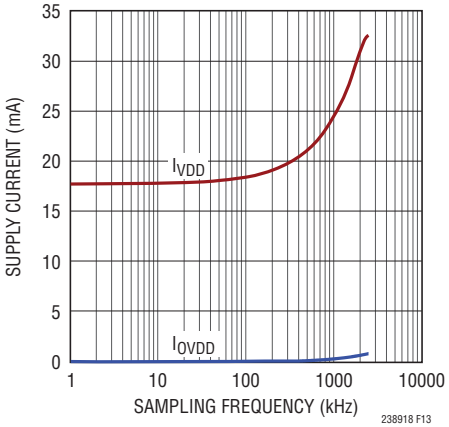


Figure 13. Supply Current vs Sampling Frequency. Power Dissipation of the LTC2389-18 Decreases with Decreasing Sampling Frequency

APPLICATIONS INFORMATION

DIGITAL INTERFACE

To accommodate a variety of application-specific processor and FPGA data bus widths, the LTC2389-18 output bus may be configured to operate in either 18-bit parallel, 16-bit parallel, 8-bit parallel or serial modes, as described in Table 1. The flexible OV_{DD} supply allows the LTC2389-18 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

18-Bit Parallel Bus Configuration

In applications such as FPGA and CPLD based solutions, where a full 18-bit wide parallel data bus is available, the LTC2389-18 is capable of providing each conversion result R[17:0] as one 18-bit word on pins D[17:0]. To select this bus configuration, pins MODE = MODE[1:0] should be driven to MODE = 00, as described in Table 1. If the application does not require the bus to be shared, drive the chip select pin $\overline{CS}$ = 0 to enable the LTC2389-18 to drive the bus continuously, as shown in Figure 14. In applications where the bus must be shared, drive $\overline{CS}$ = 1 when other devices are using the bus to Hi-Z the LTC2389-18 bus pins and drive $\overline{CS}$ = 0 to allow the LTC2389-18 to drive the bus, as shown in Figures 15 and 16.

16-Bit Parallel Bus Configuration

In applications such as 16-bit microcontroller based solutions, where a 16-bit wide parallel data bus is available, the LTC2389-18 is capable of providing each conversion result R[17:0] in two 16-bit words on pins D[17:2]. To select this bus configuration, pins MODE = MODE[1:0] should be driven to MODE = 01, as described in Table 1. In this configuration, pins D0/A0 and D1/A1 become a 2-bit wide address input A[1:0] which controls whether the upper 16 bits R[17:2] or the lower two bits R[1:0] of the conversion result are driven on D[17:2], as shown in Figure 17. Two formats are available for outputting the lowest two bits R[1:0] of the conversion result to accommodate various application-specific hardware and software constraints, as shown in Table 1. The chip select pin $\overline{CS}$ enables the 16-bit parallel bus to be shared between multiple devices. See the 18-Bit Parallel Bus Configuration section for further details.

8-Bit Parallel Bus Configuration

In applications such as 8-bit microcontroller based solutions, where an 8-bit wide parallel data bus is available, the LTC2389-18 is capable of providing each conversion result R[17:0] in three 8-bit words on pins D[17:10]. To select this bus configuration, pins MODE = MODE[1:0] should be driven to MODE = 10, as described in Table 1. In this configuration, pins D0/A0 and D1/A1 become a 2-bit wide address input A[1:0] which controls whether the upper eight bits R[17:10], the middle eight bits R[9:2], or the lower two bits R[1:0] of the conversion result are driven on D[17:10], as shown in Figure 18. Two formats are available for outputting the lowest two bits R[1:0] of the conversion result to accommodate various application-specific hardware and software constraints, as shown in Table 1. The chip select pin $\overline{CS}$ enables the 8-bit parallel bus to be shared between multiple devices. See the 18-Bit Parallel Bus Configuration section for further details.

APPLICATIONS INFORMATION

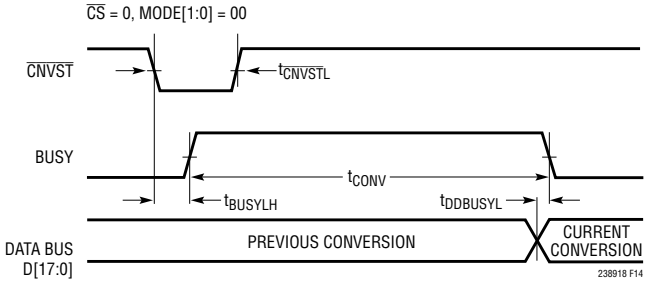


Figure 14. Read the Parallel Data Continuously. The Data Bus Is Always Driven and Cannot Be Shared

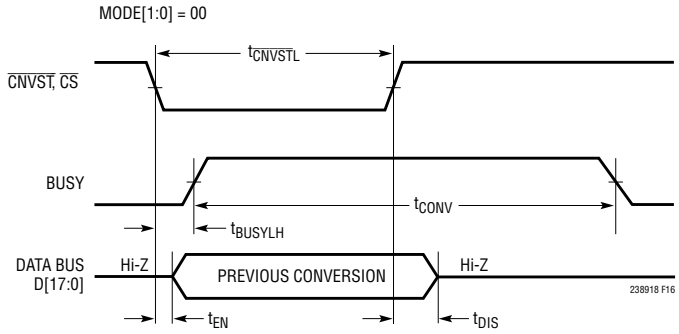


Figure 16. Read the Parallel Data During the Following Conversion

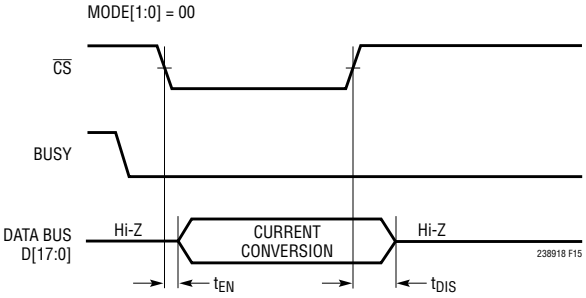


Figure 15. Read the Parallel Data After the Conversion

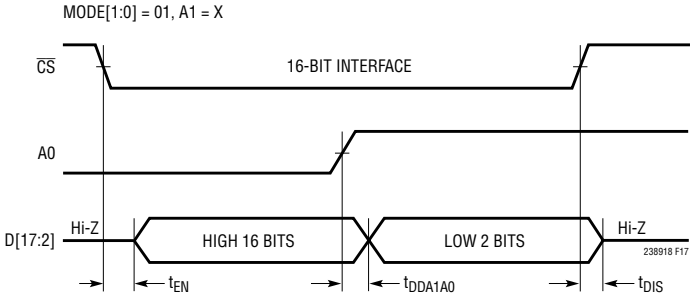


Figure 17. 16-Bit Parallel Interface Using A[1:0] Pins

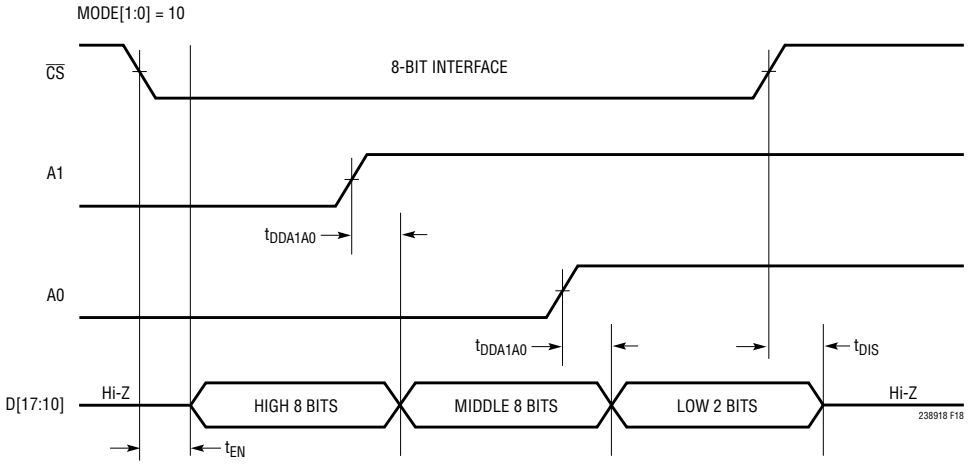


Figure 18. 8-Bit Parallel Interface Using A[1:0] Pins

APPLICATIONS INFORMATION

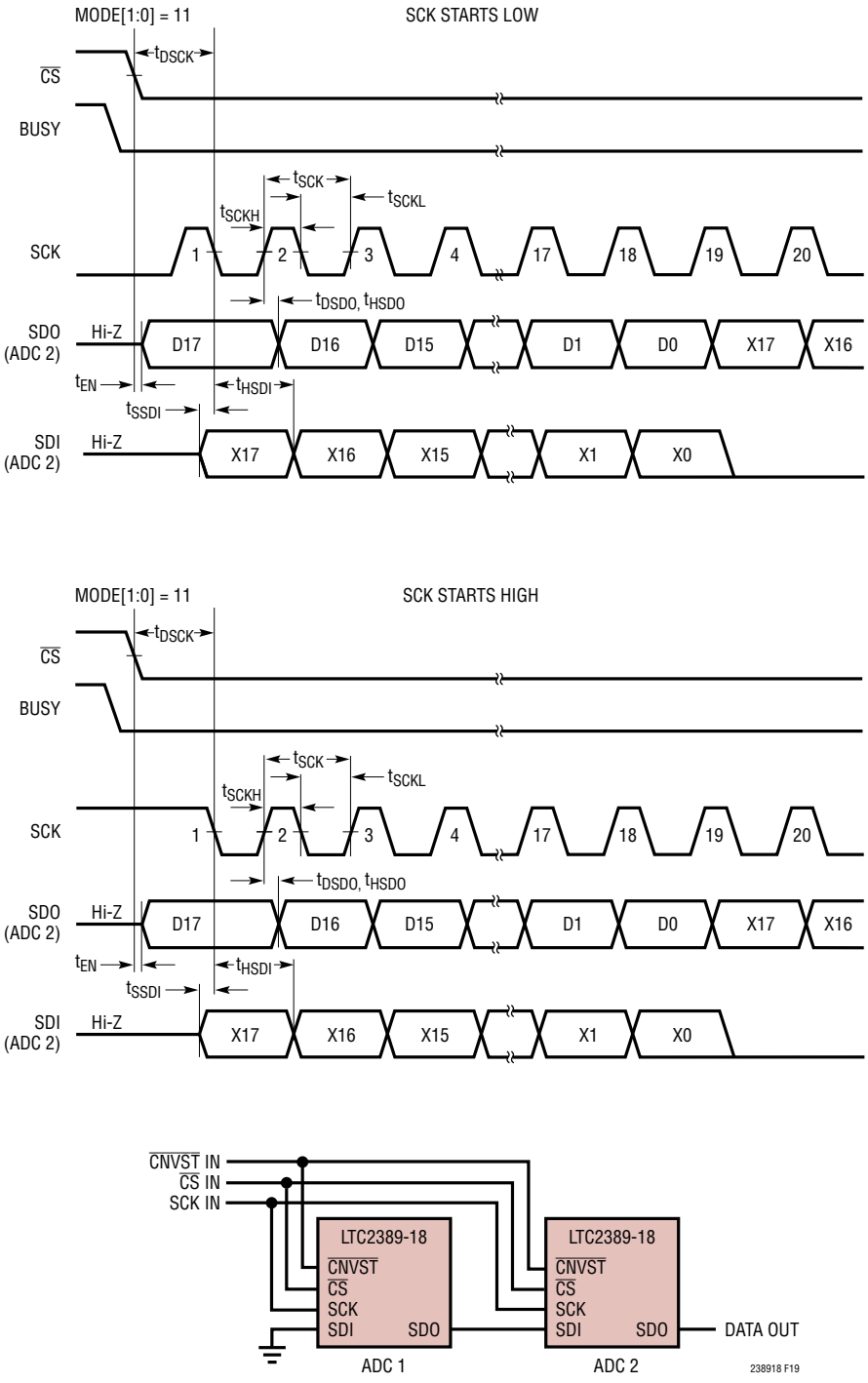


Figure 19. Serial Interface with External Clock. Read After the Conversion. Daisy Chain Multiple Converters

APPLICATIONS INFORMATION

Serial Bus Configuration

In applications where a serial bus is required to minimize the data bus width, the LTC2389-18 is capable of providing each conversion result R[17:0] serially on pin D12/SDO. To select this bus configuration, pins MODE = MODE[1:0] should be driven to MODE = 11, as described in Table 1. As shown in Figure 19, the serial output data is presented on the SDO pin in response to an external shift clock input applied to the SCK pin. The data on SDO changes state following rising edges of SCK. The one exception to this behavior is that D17 remains valid until the first SCK rising edge following the first SCK falling edge. If $\overline{CS}$ is used to gate the serial output data, the full conversion result should be read before $\overline{CS}$ is returned to a high level. For best performance do not clock serial data out when BUSY is high.

The SDI input pin can be used to daisy chain multiple converters, as shown in Figure 19. In this figure, two devices are cascaded with the MSB of ADC1 appearing at the serial output of ADC2 after an 18 SCK cycle delay. The serial output of ADC1 is clocked into ADC2 on the falling edges of SCK. This is useful in applications where hardware constraints limit the number of data lines available to interface with multiple converters.

Data Format

The binary format of the conversion result depends on the state of pins PD/$\overline{FD}$ and OB/$\overline{2C}$, as described in Table 2. These pins are active in both the parallel and serial modes of operation.

Reset

As shown in Figure 20, when the RESET pin is high, the LTC2389-18 is reset and the data bus is put into a high impedance mode. If this occurs during a conversion, the conversion is immediately halted. In reset, requests for new conversions are ignored. Once RESET returns low, the LTC2389-18 is ready to start a new conversion after the acquisition time has been met.

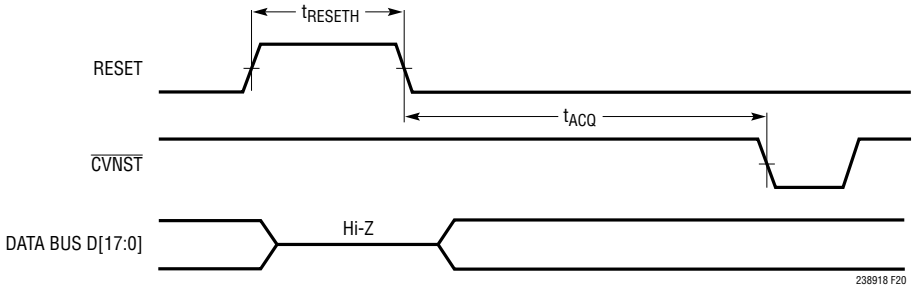


Figure 20. RESET Pin Timing

APPLICATIONS INFORMATION

BOARD LAYOUT

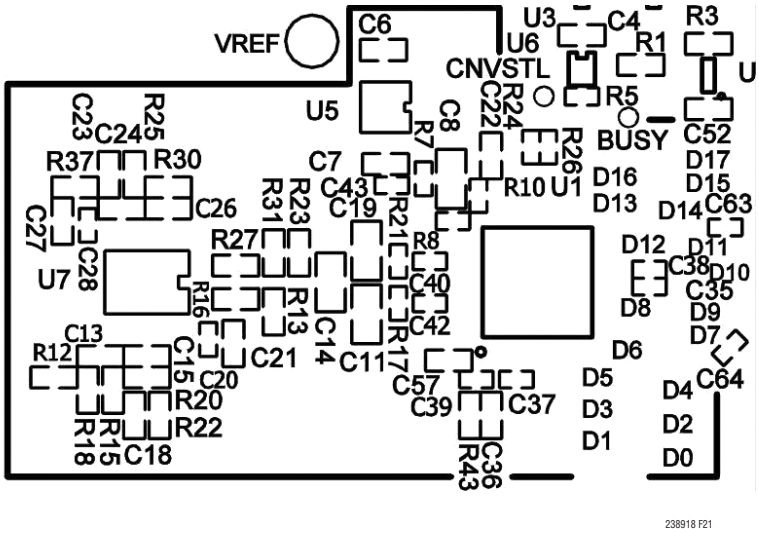
To obtain the best performance from the LTC2389-18, a printed circuit board (PCB) is recommended. Layout for the printed circuit board should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals alongside analog signals or underneath the ADC.

Pin Compatibility with LTC238x-16

To ensure a board layout intended for use with the LTC2389-18 is also compatible with 16-bit versions of the LTC238x family, the design should maintain the ability to drive Pins 5 (MODE1) and 7 (DO/AO) to logic low levels, to drive Pin 4 (MODE0) to both logic high and logic low levels, and to dynamically drive Pin 8 (D1/A1) to both logic high and logic low levels. Simplifications to these constraints are possible based on the specific application. For further details on the operation of LTC238x-16 devices, please refer the associated data sheets.

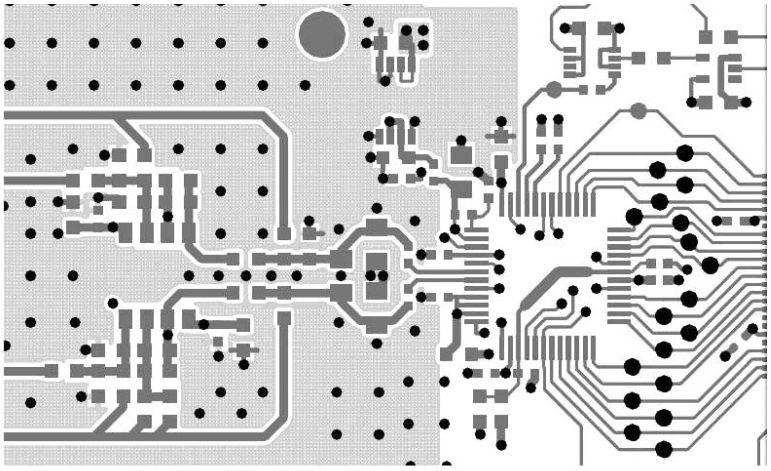
Recommended Layout

The following is an example of a recommended PCB layout. A single solid ground plane is used. Bypass capacitors to the supplies are placed as close as possible to the supply pins. Low impedance common returns for these bypass capacitors are essential to the low noise operation of the ADC. The analog input traces are shielded by ground. For more details and information refer to DC1826A-A, the evaluation kit for the LTC2389-18.



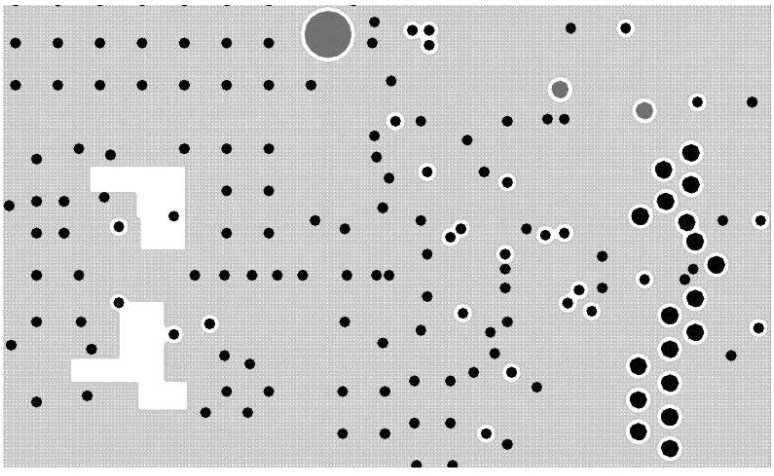
Partial Top Silkscreen

APPLICATIONS INFORMATION



238918 F22

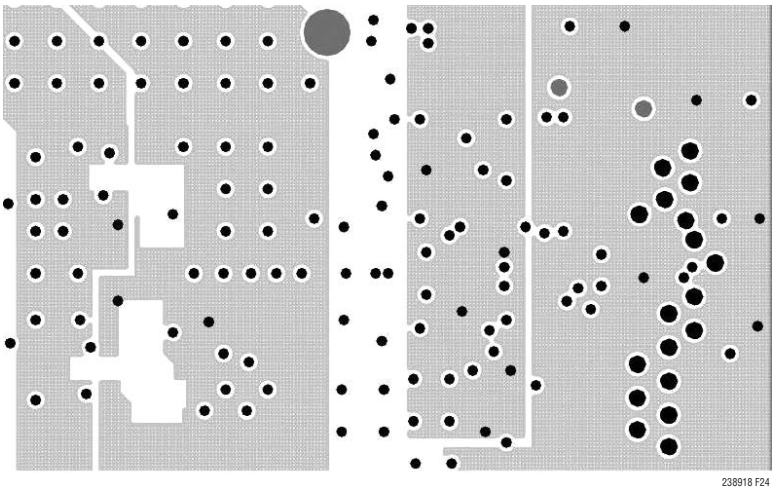
Partial Layer 1 Component Side



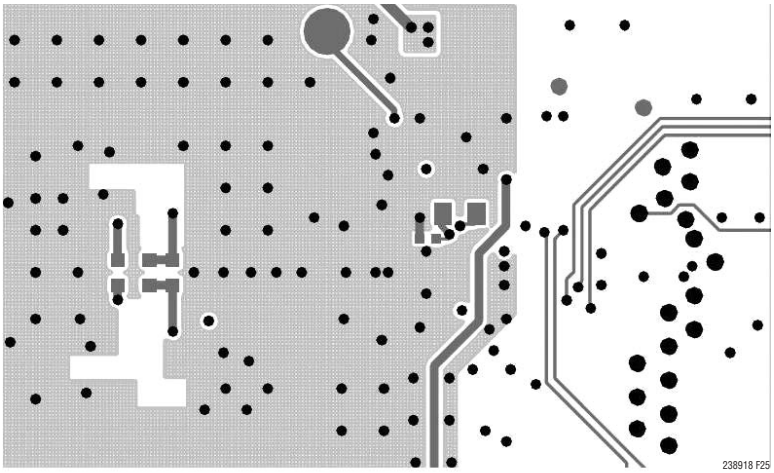
238918 F23

Partial Layer 2 Ground Plane

APPLICATIONS INFORMATION



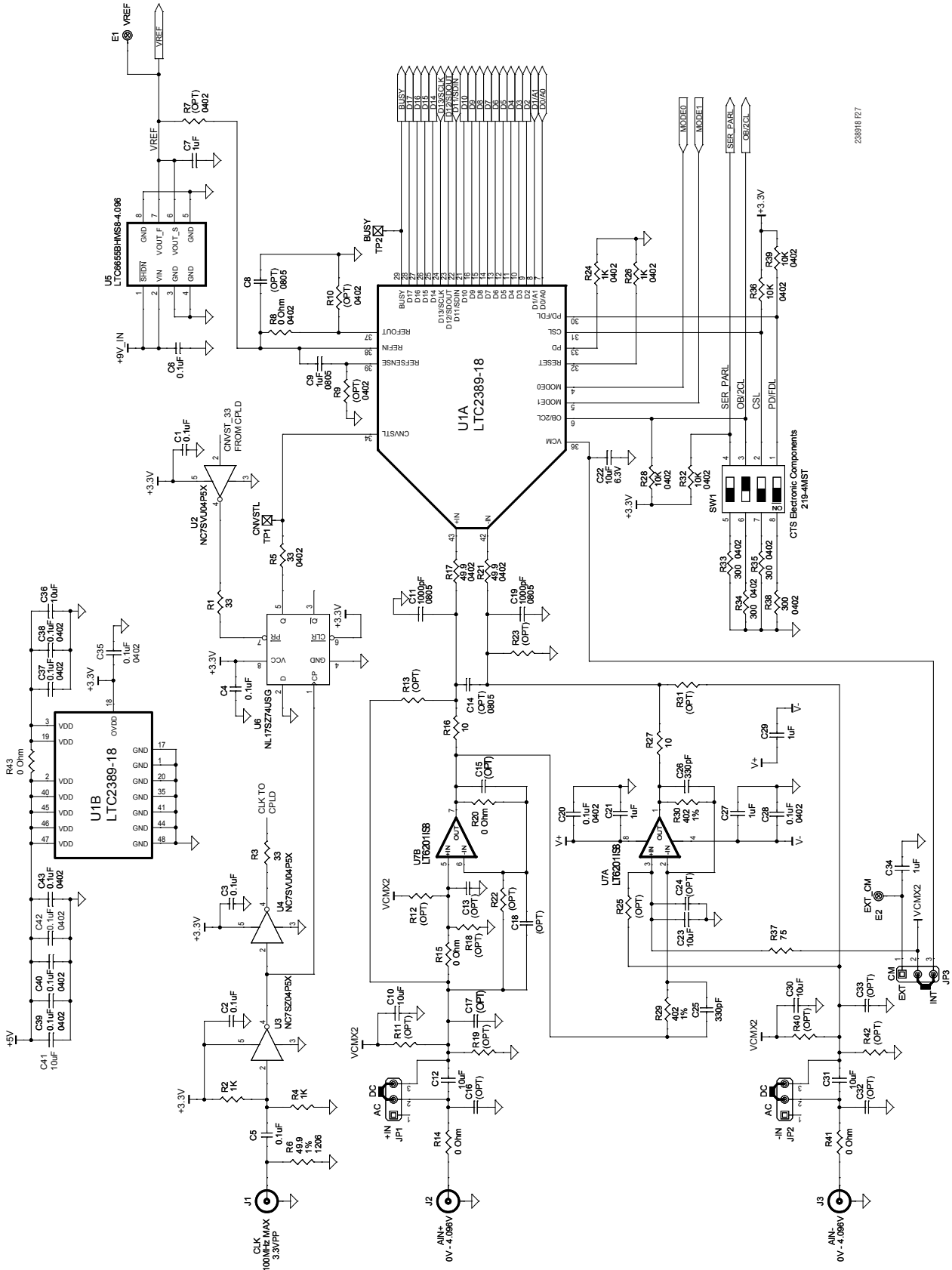
Partial Layer 3 Power Plane



Partial Layer 4 Bottom Layer

Bottom Silk Partial

APPLICATIONS INFORMATION

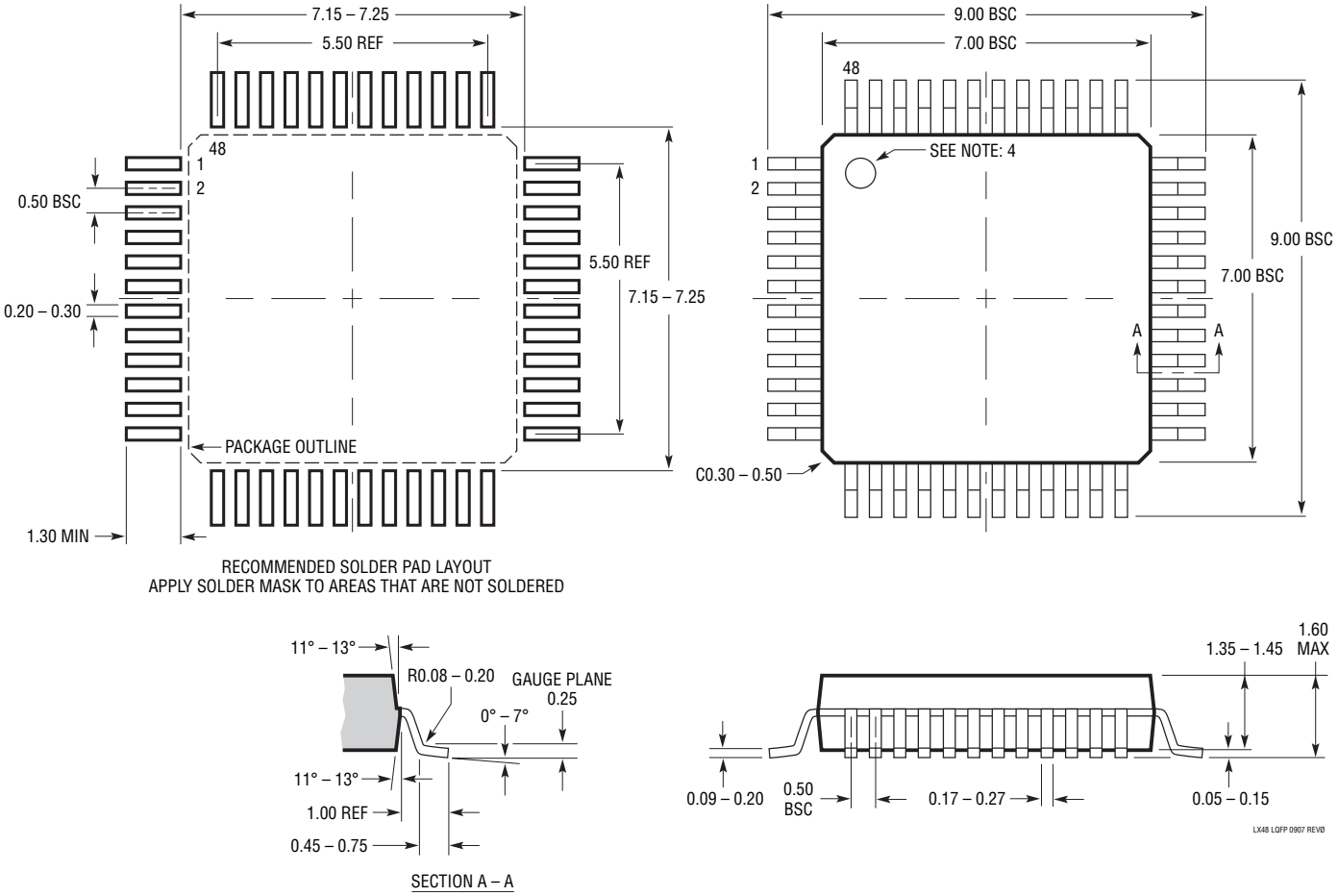


Partial Schematic of Demo Board

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

LX Package
48-Lead Plastic LQFP (7mm × 7mm)
(Reference LTC DWG # 05-08-1760 Rev Ø)

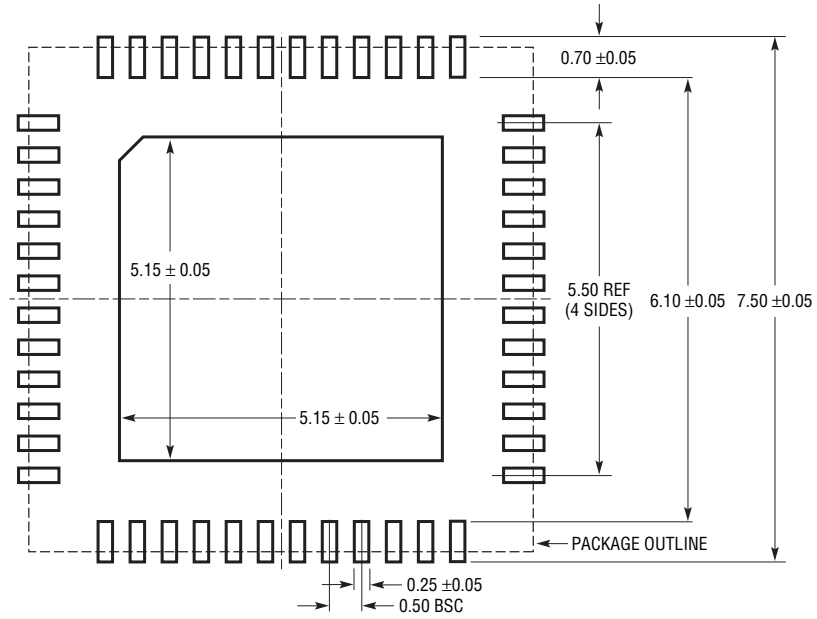


NOTE:
1. PACKAGE DIMENSIONS CONFORM TO JEDEC #MS-026 PACKAGE OUTLINE
2. DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.25mm ON ANY SIDE, IF PRESENT
4. PIN-1 INDENTIFIER IS A MOLDED INDENTATION, 0.50mm DIAMETER
5. DRAWING IS NOT TO SCALE

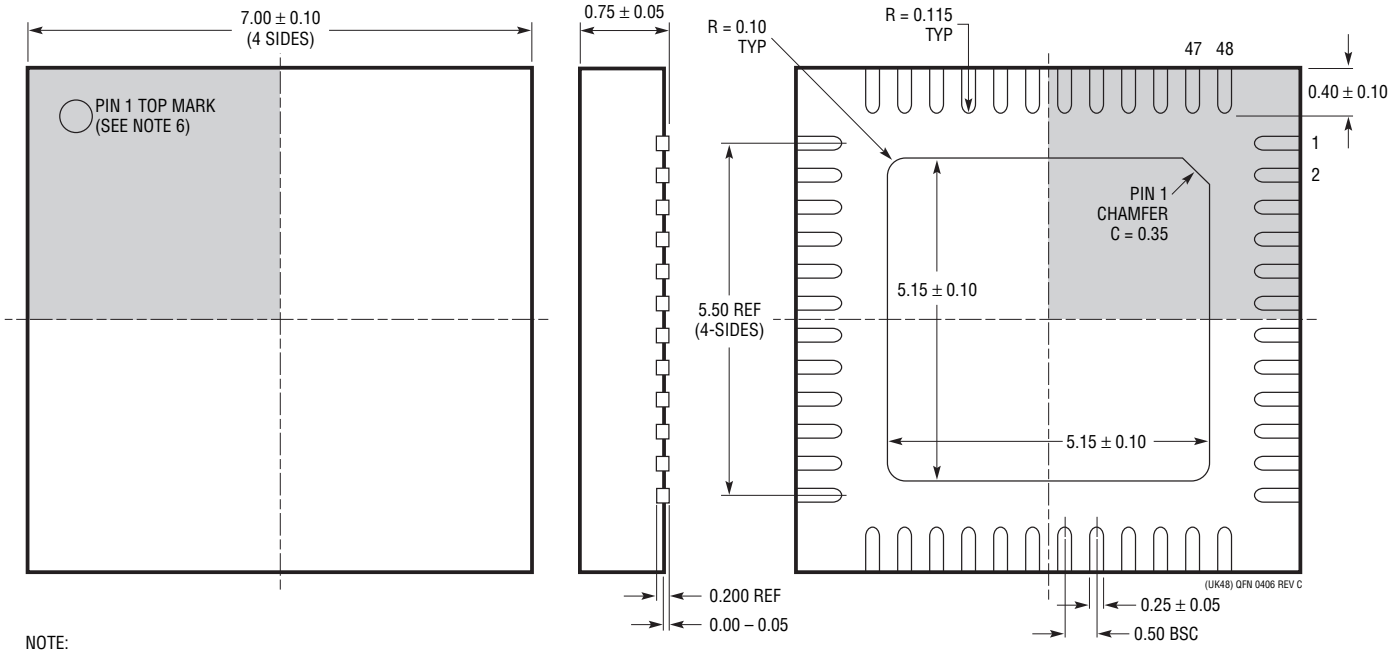
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UK Package
48-Lead Plastic QFN (7mm × 7mm)
(Reference LTC DWG # 05-08-1704)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WKKD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE