Wide Input Voltage Range Boost/SEPIC/Inverting Converter with 6A, 40V Switch

FEATURES

- **Wide V_{IN} Range: 1.6V (2.5V Start-Up) to 40V**
- **Positive or Negative Output Voltage Programming with a Single Feedback Pin**
- **$\overline{PGOOD}$ Output Voltage Status Report**
- Internal 6A/40V Power Switch
- Programmable Soft-Start
- Programmable Operating Frequency (100kHz to 1MHz) with One External Resistor
- Synchronizable to an External Clock
- Low Shutdown Current < 1µA
- $INTV_{CC}$ Regulator Supplied from V_{IN} or DRIVE
- Programmable Input Undervoltage Lockout with Hysteresis
- Thermally Enhanced QFN (5mm × 6mm) and TSSOP Packages

APPLICATIONS

- Automotive
- Telecom
- Industrial

DESCRIPTION

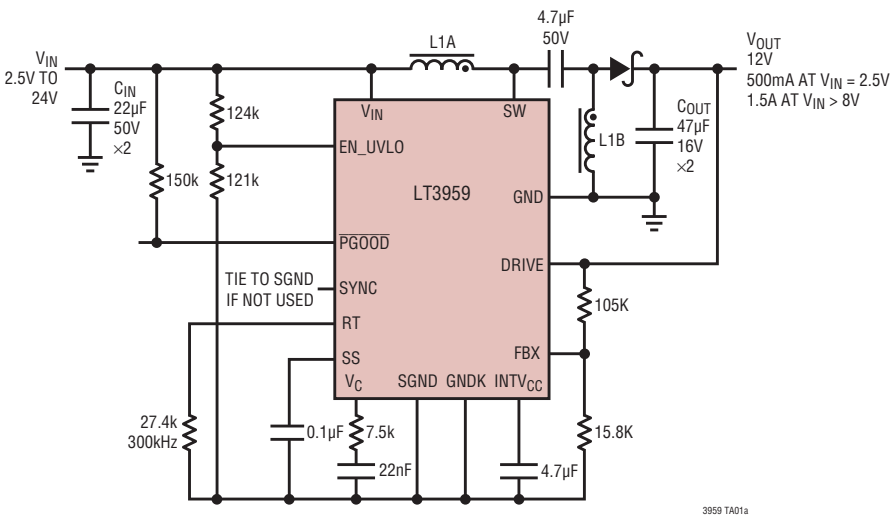
The LT®3959 is a wide input range, current mode, DC/DC controller which is capable of regulating either positive or negative output voltages from a single feedback pin. It can be configured as a boost, SEPIC or inverting converter.

It features an internal low side N-channel MOSFET rated for 6A at 40V and driven from an internal regulated supply provided from V_{IN} or DRIVE. The fixed frequency, current-mode architecture results in stable operation over a wide range of supply and output voltages. The operating frequency of LT3959 can be set over a 100kHz to 1MHz range with an external resistor, or can be synchronized to an external clock using the SYNC pin.

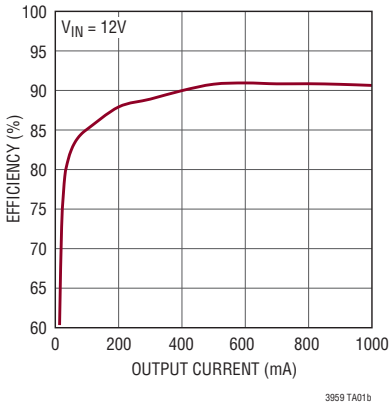
The LT3959 features soft-start and frequency foldback functions to limit inductor current during start-up and output short-circuit. A window comparator on the FBX pin reports via the $\overline{PGOOD}$ pin, providing output voltage status indication.

TYPICAL APPLICATION

2.5V to 24V Input, 12V Output SEPIC Converter
Excellent for Automotive 12V Post Regulator



Efficiency vs Output Current

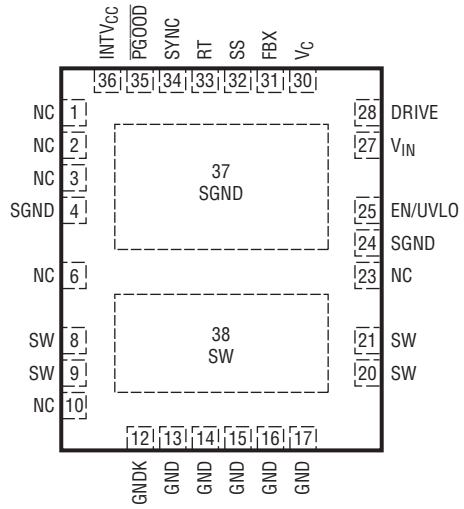


ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN} 40V
EN/UVLO (Note 2).....40V
DRIVE 40V
$\overline{PGOOD}$.....40V
SW 40V
$INTV_{CC}$ 8V
SYNC 8V
V_C, SS 3V
RT 1.5V
GND, GNDK to SGND .....±0.3V
FBX ..... –3V to 3V
Operating Junction Temperature Range (Note 3)
LT3959E/LT3959I ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION

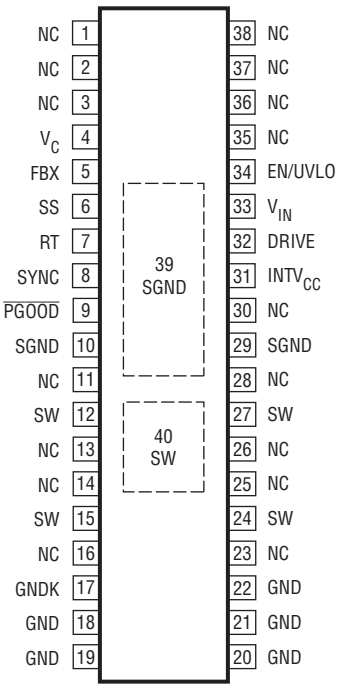
TOP VIEW



UHEMA PACKAGE
36-LEAD (5mm × 6mm) PLASTIC QFN

T_{JMAX} =125°C, θ_{JA} = 42°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 37) IS SGND, MUST BE SOLDERED TO SGND PLANE
EXPOSED PAD (PIN 38) IS SW, MUST BE SOLDERED TO SW PLANE

TOP VIEW



FE PACKAGE
38-LEAD PLASTIC TSSOP

T_{JMAX} =125°C, θ_{JA} = 42°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 39) IS SGND, MUST BE SOLDERED TO SGND PLANE
EXPOSED PAD (PIN 40) IS SW, MUST BE SOLDERED TO SW PLANE

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3959EUHE#PBF	LT3959EUHE#TRPBF	3959	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C
LT3959IUHE#PBF	LT3959IUHE#TRPBF	3959	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C
LT3959EFE#PBF	LT3959EFE#TRPBF	LT3959FE	38-Lead Plastic TSSOP	–40°C to 125°C
LT3959IFE#PBF	LT3959IFE#TRPBF	LT3959FE	38-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V, EN/UVLO = 12V, $INTV_{CC}$ = 4.75V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage		●	1.6		40	V
V_{IN} Start-Up Voltage	R_T = 27.4kΩ, FBX = 0	●		2.5	2.65	V
V_{IN} Shutdown I_Q	EN/UVLO < 0.4V EN/UVLO = 1.15V			0.1	1 6	µA µA
V_{IN} Operating I_Q				350	450	µA
DRIVE Shutdown Quiescent Current	EN/UVLO < 0.4V EN/UVLO = 1.15V			0.1 0.1	1 2	µA µA
DRIVE Quiescent Current (Not Switching)	R_T = 27.4kΩ, DRIVE = 6V			2.0	2.5	mA
SW Pin Current Limit		●	6.0	7.0	8.0	A
SW Pin On Voltage	I_{SW} = 3A			100		mV
SW Pin Leakage Current	SW = 40V				5	µA
Error Amplifier						
FBX Regulation Voltage ($V_{FBX(REG)}$)	FBX > 0V FBX < 0V	● ●	1.580 –0.815	1.6 –0.80	1.620 –0.785	V V
FBX Pin Input Current	FBX = 1.6V FBX = –0.8V		 –10	80	130 10	nA nA
Transconductance g_m ($\Delta I_{VC}/\Delta V_{FBX}$)	FBX = $V_{FBX(REG)}$			240		µs
V_C Output Impedance				5		MΩ
FBX Line Regulation [$\Delta V_{FBX(REG)}/(\Delta V_{IN} \bullet V_{FBX(REG)})$]	1.6V < V_{IN} < 40V, FBX >0 1.6V < V_{IN} < 40V, FBX <0			0.02 0.02	0.05 0.05	%/V %/V
V_C Source Current	FBX = 0V, V_C = 1.3V			–13		µA
V_C Sink Current	FBX = 1.7V, V_C = 1.3V FBX = –0.85V, V_C = 1.3V			13 10		µA µA
Oscillator						
Switching Frequency	R_T = 27.4k to SGND, V_{FBX} = 1.6V R_T = 86.6k to SGND, V_{FBX} = 1.6V R_T = 6.81k to SGND, V_{FBX} = 1.6V	●	250	300 100 1000	340	kHz kHz kHz
R_T Voltage	FBX = 1.6V, –0.8V			1.13		V
SW Minimum Off-Time				150	200	ns
SW Minimum On-Time				150	200	ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V, EN/UVLO = 12V, $INTV_{CC}$ = 4.75V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SYNC Input Low		●			0.4	V
SYNC Input High		●	1.5			V
SS Pull-Up Current	SS = 0V, Current Out of Pin	●	–14	–10.5	–7	µA
Low Dropout Regulators (DRIVE LDO and V_{IN} LDO)						
DRIVE LDO Regulation Voltage	DRIVE = 6V, Not Switching	●	4.6	4.75	4.9	V
V_{IN} LDO Regulation Voltage	DRIVE = 0V, Not Switching	●	3.6	3.75	3.9	V
DRIVE LDO Current Limit	$INTV_{CC}$ = 4V			60		mA
V_{IN} LDO Current Limit	DRIVE = 0V, $INTV_{CC}$ = 3V			60		mA
DRIVE LDO Load Regulation ($\Delta V_{INTVCC}/V_{INTVCC}$)	0 < I_{INTVCC} < 20mA, DRIVE = 6V		–1	–0.6		%
V_{IN} LDO Load Regulation ($\Delta V_{INTVCC}/V_{INTVCC}$)	DRIVE = 0V, 0 < I_{INTVCC} < 20mA		–1	–0.6		%
DRIVE LDO Line Regulation [$\Delta V_{INTVCC}/(V_{INTVCC} \bullet \Delta V_{IN})$]	1.6V < V_{IN} < 40V, DRIVE = 6V			0.03	0.07	%/V
V_{IN} LDO Line Regulation [$\Delta V_{INTVCC}/(V_{INTVCC} \bullet \Delta V_{IN})$]	DRIVE = 0V, 5V < V_{IN} < 40V			0.03	0.07	%/V
DRIVE LDO Dropout Voltage ($V_{DRIVE} - V_{INTVCC}$)	DRIVE = 4V, I_{INTVCC} = 20mA	●		190	400	mV
V_{IN} LDO Dropout Voltage ($V_{IN} - V_{INTVCC}$)	V_{IN} = 3V, DRIVE = 0V, I_{INTVCC} = 20mA	●		190	400	mV
$INTV_{CC}$ Undervoltage Lockout Threshold Falling		●	1.85	2.0	2.15	V
$INTV_{CC}$ Undervoltage Lockout Threshold Rising		●	2.15	2.3	2.45	V
$INTV_{CC}$ Current in Shutdown	EN/UVLO = 0V			25		µA
Logic						
EN/UVLO Threshold Voltage Falling		●	1.17	1.22	1.27	V
EN/UVLO Threshold Voltage Rising Hysteresis				20		mV
EN/UVLO Input Low Voltage	I_{VIN} < 1µA				0.4	V
EN/UVLO Pin Bias Current Low	EN/UVLO = 1.15V		1.8	2.2	2.6	µA
EN/UVLO Pin Bias Current High	EN/UVLO = 1.30V			10	100	nA
FBX Power Good Threshold Voltage	FBX > 0V, $\overline{PGOOD}$ Falling FBX < 0V, $\overline{PGOOD}$ Falling			$V_{FBX(REG)}$ – 0.08 $V_{FBX(REG)}$ + 0.04		V V
FBX Overvoltage Threshold	FBX > 0V, $\overline{PGOOD}$ Rising FBX < 0V, $\overline{PGOOD}$ Rising			$V_{FBX(REG)}$ + 0.12 $V_{FBX(REG)}$ – 0.06		V V
$\overline{PGOOD}$ Output Low (V_{OL})	$I_{\overline{PGOOD}}$ = 250µA			210	300	mV
$\overline{PGOOD}$ Leakage Current	$\overline{PGOOD}$ = 40V				1	µA
$INTV_{CC}$ Minimum Voltage to Enable $\overline{PGOOD}$ Function		●	2.5	2.7	2.9	V
$INTV_{CC}$ Minimum Voltage to Enable SYNC Function		●	2.5	2.7	2.9	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

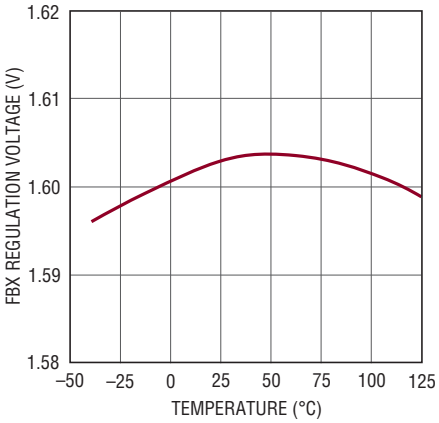
Note 2: For V_{IN} below 4V, the EN/UVLO pin must not exceed V_{IN} for proper operation.

Note 3: The LT3959E is guaranteed to meet performance specifications from the 0°C to 125°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3959I is guaranteed over the full –40°C to 125°C operating junction temperature range.

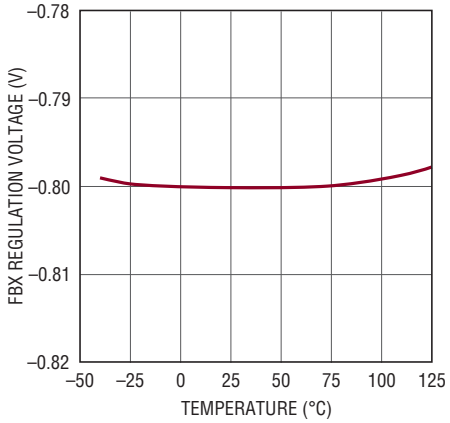
Note 4: The LT3959 is tested in a feedback loop which servos V_{FBX} to the reference voltages (1.6V and –0.8V) with the V_C pin forced to 1.3V.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

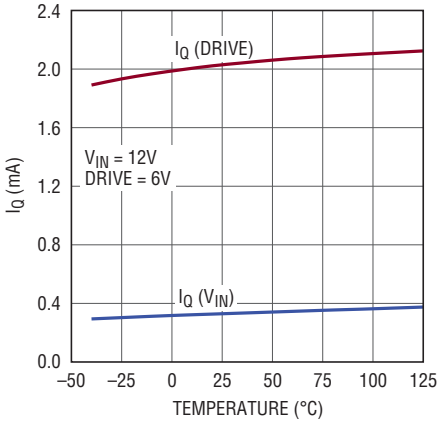
FBX Positive Regulation Voltage vs Temperature



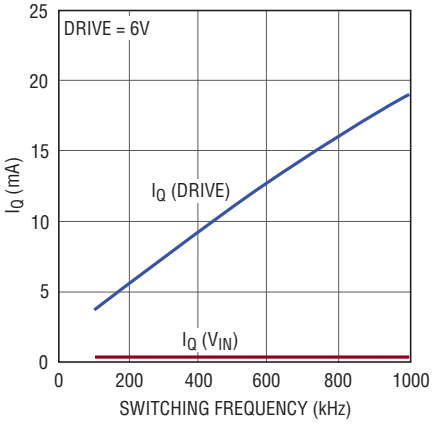
FBX Negative Regulation Voltage vs Temperature



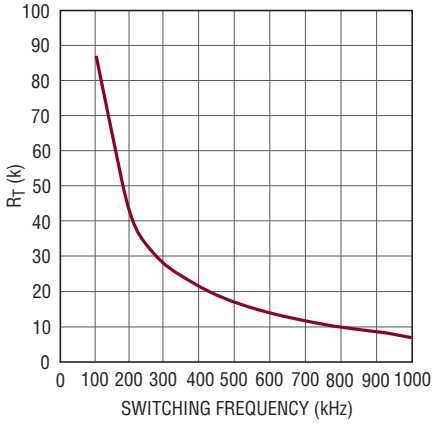
Quiescent Current vs Temperature



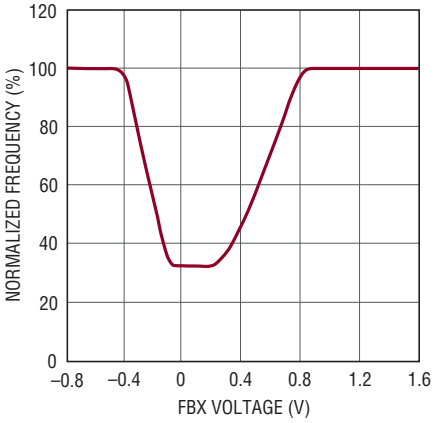
Dynamic Quiescent Current vs Switching Frequency



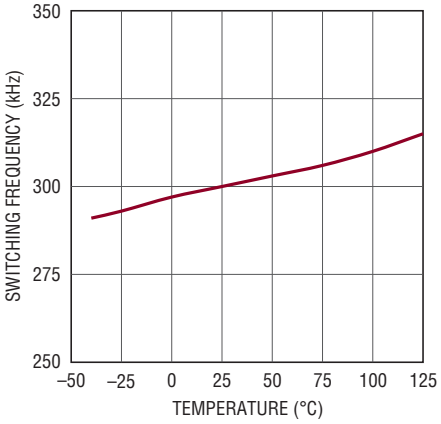
R_T vs Switching Frequency



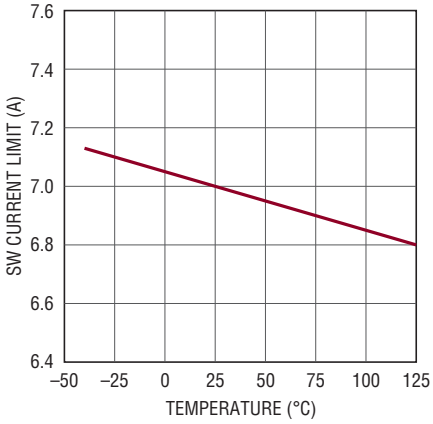
Normalized Switching Frequency vs FBX Voltage



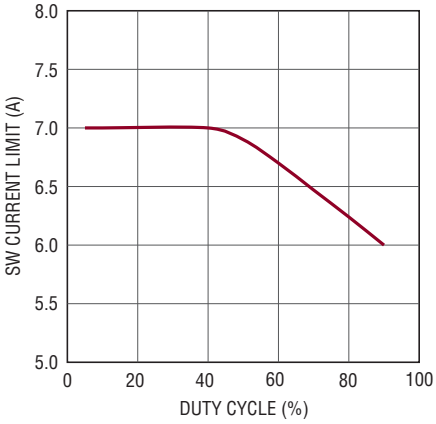
Switching Frequency vs Temperature



SW Current Limit vs Temperature

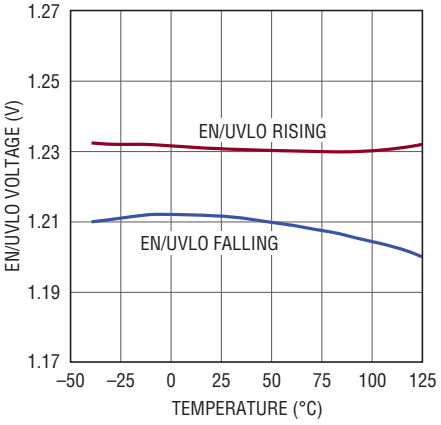


SW Current Limit vs Duty Cycle

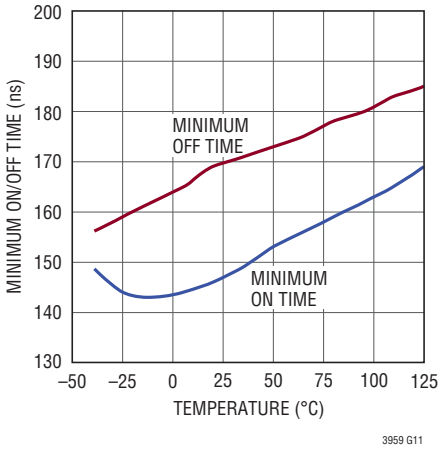


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

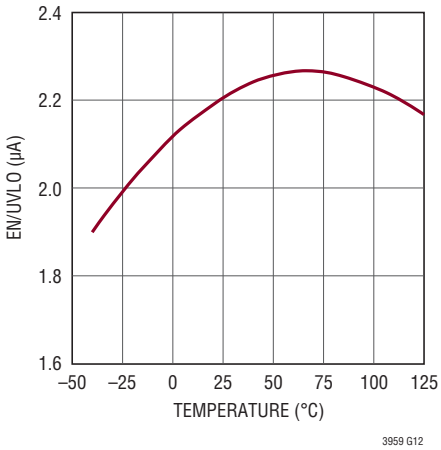
EN/UVLO Threshold vs Temperature



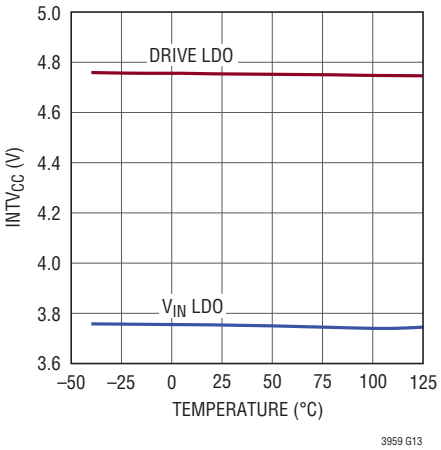
SW Minimum On- and Off-Times vs Temperature



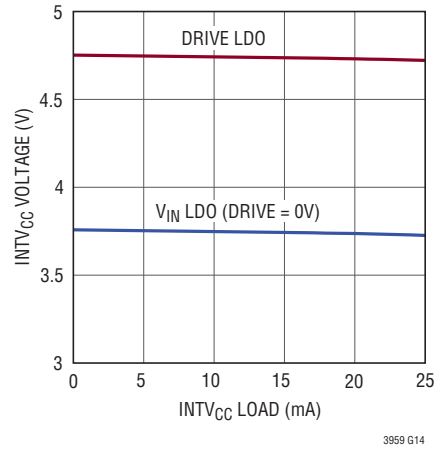
EN/UVLO Hysteresis Current vs Temperature



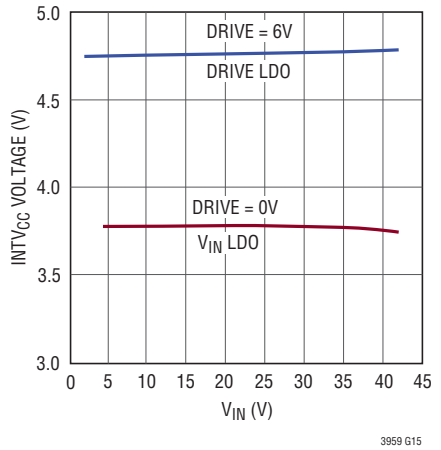
$INTV_{CC}$ vs Temperature



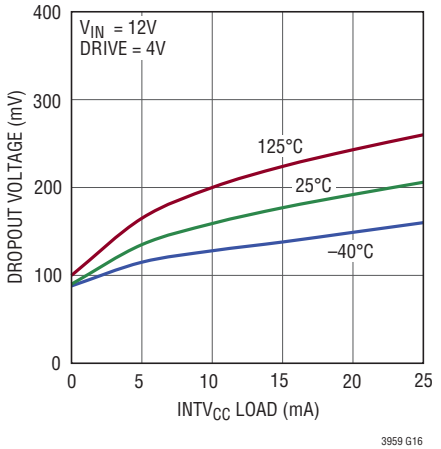
$INTV_{CC}$ Load Regulation



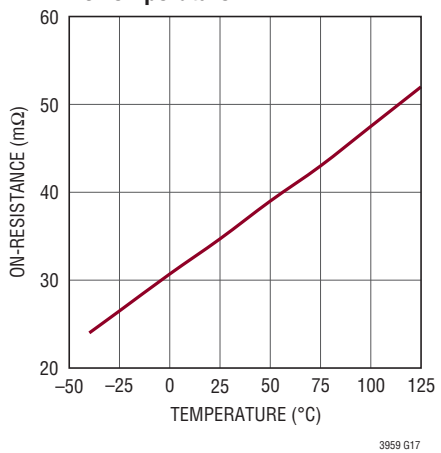
$INTV_{CC}$ Line Regulation



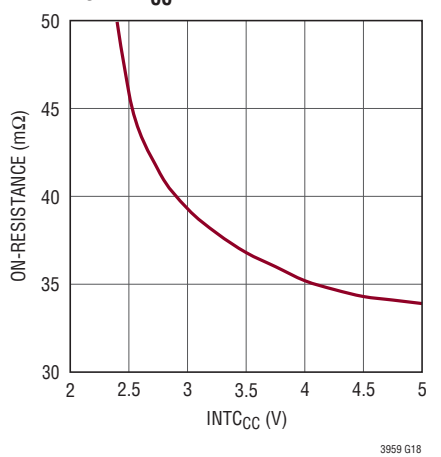
$INTV_{CC}$ Dropout Voltage vs Current, Temperature



Internal Switch On-Resistance vs Temperature



Internal Switch On-Resistance vs $INTV_{CC}$



PIN FUNCTIONS

DRIVE: DRIVE LDO Supply Pin. This pin can be connected to either V_{IN} or a quasi-regulated voltage supply such as a DC converter output. This pin must be bypassed to GND with a minimum of 1µF capacitor placed close to the pin. Tie this pin to V_{IN} if not used.

EN/UVLO: Shutdown and Undervoltage Detect Pin. An accurate 1.22V (nominal) falling threshold with externally programmable hysteresis detects when power is okay to enable switching. Rising hysteresis is generated by the external resistor divider and an accurate internal 2.2µA pull-down current. An undervoltage condition resets soft-start. Tie to 0.4V, or less, to disable the device and reduce V_{IN} quiescent current below 1µA.

FBX: Voltage Regulation Feedback Pin for Positive or Negative Outputs. Connect this pin to a resistor divider between the output and SGND. FBX is the input of two error amplifiers—one configured to regulate a positive output; the other, a negative output. Depending upon topology selected, switching causes the output to ramp positive or negative. The appropriate amplifier takes control while the other becomes inactive. Additionally FBX is input for two window comparators that indicate through the $\overline{PGOOD}$ pin when the output is within 5% of the regulation voltages. FBX also modulates the switching frequency during start-up and fault conditions when FBX is close to SGND.

GND: Source Terminal of Switch and the GND Input to the Switch Current Comparator.

GNDK: Kelvin Connection Pin between GND and SGND. Kelvin connect this pin to the SGND plane close to the IC. See the Board Layout section.

$INTV_{CC}$: Regulated Supply for Internal Loads and Gate Driver. Regulated to 4.75V if powered from DRIVE or regulated to 3.75V if powered from V_{IN}. The $INTV_{CC}$ pin must be bypassed to SGND with a minimum of 4.7µF capacitor placed close to the pin.

NC: No Internal Connection. Leave these pins open or connect them to the adjacent pins.

$\overline{PGOOD}$: Output Ready Status Pin. An open-collector pull down on $\overline{PGOOD}$ asserts when $INTV_{CC}$ is greater than 2.7V and the FBX voltage is within 5% (80mV if V_{FBX} = 1.6V or 40mV if V_{FBX} = –0.8V) of the regulation voltage.

RT: Switching Frequency Adjustment Pin. Set the frequency using a resistor to SGND. Do not leave the RT pin open.

SGND: Signal Ground. Must be soldered directly to the signal ground plane. Connect to ground terminal of: external resistor dividers for FBX and EN/UVLO; capacitors for $INTV_{CC}$, SS, and V_C; and resistor R_T.

SS: Soft-Start Pin. This pin modulates compensation pin voltage (V_C) clamp. The soft-start interval is set with an external capacitor. The pin has a 10µA (typical) pull-up current source to an internal 2.5V rail. The soft-start pin is reset to SGND by an EN/UVLO undervoltage condition, an $INTV_{CC}$ undervoltage condition or an internal thermal lockout.

SW: Drain of Internal Power N-Channel MOSFET.

SYNC: Frequency Synchronization Pin. Used to synchronize the internal oscillator to an outside clock. If this feature is used, an R_T resistor should be chosen to program a switching frequency 20% slower than SYNC pulse frequency. Tie the SYNC pin to SGND if this feature is not used. This signal is ignored during FB frequency foldback or when $INTV_{CC}$ is less than 2.7V.

V_{IN}: Supply Pin for Internal Leads and the V_{IN} LDO Regulator of $INTV_{CC}$. Must be locally bypassed to GND with a minimum of 1µF capacitor placed close to this pin.

V_C: Error Amplifier Compensation Pin. Used to stabilize the voltage loop with an external RC network. Place compensation components between the V_C pin and SGND.

BLOCK DIAGRAM (QFN Package)

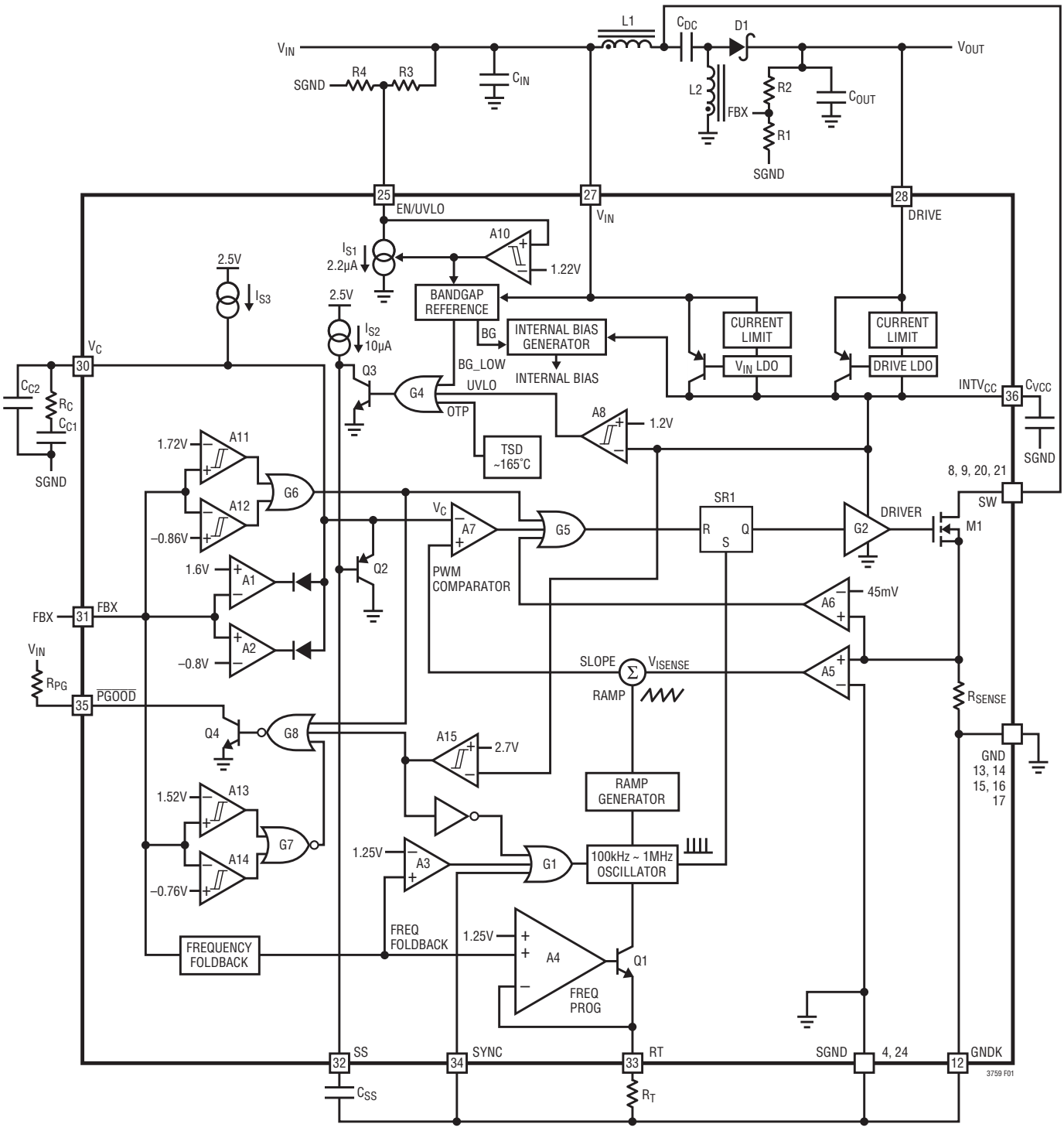


Figure 1. LT3959 Block Diagram Working as a SEPIC Converter (Shown for QFN Package)

APPLICATIONS INFORMATION

Main Control Loop

The LT3959 uses a fixed frequency, current mode control scheme to provide excellent line and load regulation. Operation can be best understood by referring to the Block Diagram in Figure 1.

The start of each oscillator cycle sets the SR latch (SR1) and turns on the internal power MOSFET switch M1 through driver G2. The switch current flows through the internal current sensing resistor R_{SENSE} and generates a voltage proportional to the switch current. This current sense voltage V_{ISENSE} (amplified by A5) is added to a stabilizing slope compensation ramp and the resulting sum (SLOPE) is fed into the positive terminal of the PWM comparator A7. When SLOPE exceeds the level at the negative input of A7 (V_C pin), SR1 is reset, turning off the power switch. The level at the negative input of A7 is set by the error amplifier A1 (or A2) and is an amplified version of the difference between the feedback voltage (FBX pin) and the reference voltage (1.6V or –0.8V, depending on the configuration). In this manner, the error amplifier sets the correct peak switch current level to keep the output in regulation.

The LT3959 has a switch current limit function. The current sense voltage is input to the current limit comparator A6. If the SENSE voltage is higher than the sense current limit threshold $V_{SENSE(MAX)}$ (45mV, typical), A6 will reset SR1 and turn off M1 immediately.

The LT3959 is capable of generating either positive or negative output voltage with a single FBX pin. It can be configured as a boost or SEPIC converter to generate positive output voltage, or as an inverting converter to generate negative output voltage. When configured as a SEPIC converter, as shown in Figure 1, the FBX pin is pulled up to the internal bias voltage of 1.6V by a voltage divider (R1 and R2) connected from V_{OUT} to SGND. Comparator A2 becomes inactive and comparator A1 performs the inverting amplification from FBX to V_C. When the LT3959 is in an inverting configuration, the FBX pin is pulled down to –0.8V by a voltage divider connected from V_{OUT} to SGND. Comparator A1 becomes inactive and comparator A2 performs the noninverting amplification from FBX to V_C.

The LT3959 has overvoltage protection functions to protect the converter from excessive output voltage overshoot during start-up or recovery from a short-circuit condition. An overvoltage comparator A11 (with 40mV hysteresis) senses when the FBX pin voltage exceeds the positive regulated voltage (1.6V) by 7.5% and turns off M1. Similarly, an overvoltage comparator A12 (with 20mV hysteresis) senses when the FBX pin voltage exceeds the negative regulated voltage (–0.8V) by 7.5% and turns off M1. Both reset pulses are sent to the main RS latch (SR1) through G6 and G5. The internal power MOSFET switch M1 is actively held off for the duration of an output overvoltage condition.

Programming Turn-On and Turn-Off Thresholds with EN/UVLO Pin

The EN/UVLO pin controls whether the LT3959 is enabled or is in shutdown state. A micropower 1.22V reference, a comparator A10 and controllable current source I_{S1} allow the user to accurately program the supply voltage at which the IC turns on and off. The falling value can be accurately set by the resistor dividers R3 and R4. When EN/UVLO is above 0.7V, and below the 1.22V threshold, the small pull-down current source I_{S1} (typical 2.2µA) is active.

The purpose of this current is to allow the user to program the rising hysteresis. The Block Diagram of the comparator and the external resistors is shown in Figure 1. The typical falling threshold voltage and rising threshold voltage can be calculated by the following equations:

$$V_{VIN(FALLING)} = 1.22 \bullet \frac{(R3+R4)}{R4}$$

$$V_{VIN(RISING)} = 2.2\,\mu A \bullet R3 + V_{IN(FALLING)}$$

For applications where the EN/UVLO pin is only used as a logic input, the EN/UVLO pin can be connected directly to the input voltage V_{IN} for always-on operation.

APPLICATIONS INFORMATION

$INTV_{CC}$ Low Dropout Voltage Regulators

The LT3959 features two internal low dropout (LDO) voltage regulators (V_{IN} LDO and DRIVE LDO) powered from different supplies (V_{IN} and DRIVE respectively). Both LDO's regulate the internal $INTV_{CC}$ supply which powers the gate driver and the internal loads, as shown in Figure 1. Both regulators are designed so that current does not flow from $INTV_{CC}$ to the LDO input under a reverse bias condition. DRIVE LDO regulates the $INTV_{CC}$ to 4.75V, while V_{IN} LDO regulates the $INTV_{CC}$ to 3.75V. V_{IN} LDO is turned off when the $INTV_{CC}$ voltage is greater than 3.75V (typical). Both LDO's can be turned off if the $INTV_{CC}$ pin is driven by a supply of 4.75V or higher but less than 8V (the $INTV_{CC}$ maximum voltage rating is 8V). A table of the LDO supply and output voltage combination is shown in Table 1.

Table 1. LDO's Supply and Output Voltage Combination (Assuming That the LDO Dropout Voltage is 0.15V)

SUPPLY VOLTAGES		LDO OUTPUT	LDO STATUS (Note 7)
V_{IN}	DRIVE	$INTV_{CC}$	
$V_{IN} \le 3.9V$	$V_{DRIVE} < V_{IN}$	$V_{IN} - 0.15V$	#1 Is ON
	$V_{DRIVE} = V_{IN}$	$V_{IN} - 0.15V$	#1 #2 are ON
	$V_{IN} < V_{DRIVE} < 4.9V$	$V_{DRIVE} - 0.15V$	#2 Is ON
	$4.9V \le V_{DRIVE} \le 40V$	4.75V	#2 Is ON
$3.9V < V_{IN} \le 40V$	$V_{DRIVE} < 3.9V$	3.75V	#1 Is ON
	$V_{DRIVE} = 3.9V$	3.75V	#1 #2 are ON
	$3.9V < V_{DRIVE} < 4.9V$	$V_{DRIVE} - 0.15V$	#2 Is ON
	$4.9V \le V_{DRIVE} \le 40V$	4.75V	#2 Is ON

Note 7: #1 is V_{IN} LDO and #2 is DRIVE LDO

The DRIVE pin provides flexibility to power the gate driver and the internal loads from a supply that is available only when the switcher is enabled and running. If not used, the DRIVE pin should be tied to V_{IN}.

The $INTV_{CC}$ pin must be bypassed to SGND immediately adjacent to the $INTV_{CC}$ pin with a minimum of 4.7µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate driver.

Operating Frequency and Synchronization

The choice of operating frequency may be determined by on-chip power dissipation, otherwise it is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing gate drive current and internal MOSFET and diode switching losses. However, lower frequency operation requires a physically larger inductor. Switching frequency also has implications for loop compensation. The LT3959 uses a constant-frequency architecture that can be programmed over a 100kHz to 1MHz range with a single external resistor from the RT pin to SGND, as shown in Figure 1. The RT pin must have an external resistor to SGND for proper operation of the LT3959. A table for selecting the value of R_T for a given operating frequency is shown in Table 2.

Table 2. Timing Resistor (R_T) Value

OSCILLATOR FREQUENCY (kHz)	R_T (kΩ)
100	86.6
200	41.2
300	27.4
400	21.0
500	16.5
600	13.7
700	11.5
800	9.76
900	8.45
1000	6.81

The switching frequency of the LT3959 can be synchronized to the positive edge of an external clock source. By providing a digital clock signal into the SYNC pin, the LT3959 will operate at the SYNC clock frequency. If this feature is used, an R_T resistor should be chosen to program a switching frequency 20% slower than SYNC pulse frequency. The SYNC pulse should have a minimum pulse width of 200ns. Tie the SYNC pin to SGND if this feature is not used.

APPLICATIONS INFORMATION

Duty Cycle Consideration

Switching duty cycle is a key variable defining converter operation. As such, its limits must be considered. Minimum on-time is the smallest time duration that the LT3959 is capable of turning on the internal power MOSFET. This time is generally about 150ns (typical) (see Minimum On-Time in the Electrical Characteristics table). In each switching cycle, the LT3959 keeps the power switch off for at least 150ns (typical) (see Minimum Off-Time in the Electrical Characteristics table).

The minimum on-time and minimum off-time and the switching frequency define the minimum and maximum switching duty cycles a converter is able to generate:

Minimum duty cycle = minimum on-time • frequency

Maximum duty cycle = 1 – (minimum off-time • frequency)

Programming the Output Voltage

The output voltage (V_{OUT}) is set by a resistor divider, as shown in Figure 1. The positive V_{OUT} and negative V_{OUT} are set by the following equations:

$$V_{OUT(POSITIVE)} = 1.6V \bullet \left(1 + \frac{R2}{R1}\right)$$

$$V_{OUT(NEGATIVE)} = -0.8V \bullet \left(1 + \frac{R2}{R1}\right)$$

The resistors R1 and R2 are typically chosen so that the error caused by the current flowing into the FBX pin during normal operation is less than 1% (this translates to a maximum value of R1 at about 121k).

Soft-Start

The LT3959 contains several features to limit peak switch currents and output voltage (V_{OUT}) overshoot during start-up or recovery from a fault condition. The primary purpose of these features is to prevent damage to external components or the load.

High peak switch currents during start-up may occur in switching regulators. Since V_{OUT} is far from its final value, the feedback loop is saturated and the regulator tries to charge the output capacitor as quickly as possible, resulting in large peak currents. A large surge current may cause inductor saturation or power switch failure.

LT3959 addresses this mechanism with the SS pin. As shown in Figure 1, the SS pin reduces the internal power MOSFET current by pulling down the V_C pin through Q2. In this way the SS allows the output capacitor to charge gradually toward its final value while limiting the start-up peak currents.

Besides start-up, soft-start can also be triggered by $INTV_{CC}$ undervoltage lockout and/or thermal lockout, which causes the LT3959 to stop switching immediately. The SS pin will be discharged by Q3. When all faults are cleared and the SS pin has been discharged below 0.2V, a 10µA current source I_{S2} starts charging the SS pin, initiating a soft-start operation.

The soft-start interval is set by the soft-start capacitor selection according to the equation:

$$T_{SS} = C_{SS} \bullet \frac{1.25V}{10\mu A}$$

FBX Frequency Foldback

When V_{OUT} is very low during start-up or a short-circuit fault on the output, the switching regulator must operate at low duty cycles to maintain the power switch current within the current limit range, since the inductor current decay rate is very low during switch off time. The minimum on-time limitation may prevent the switcher from attaining a sufficiently low duty cycle at the programmed switching frequency. So, the switch current will keep increasing through each switch cycle, exceeding the programmed current limit. To prevent the switch peak currents from exceeding the programmed value, the LT3959 contains a frequency foldback function to reduce the switching frequency when the FBX voltage is low (see the Normalized Switching Frequency vs FBX graph in the Typical Performance Characteristics section).

APPLICATIONS INFORMATION

Some frequency foldback waveforms are shown in the Typical Applications section. The frequency foldback function prevents I_L from exceeding the programmed limits because of the minimum on-time.

During frequency foldback, external clock synchronization is disabled to allow the frequency reducing operation to function properly.

Loop Compensation

Loop compensation determines the stability and transient performance. The LT3959 uses current mode control to regulate the output which simplifies loop compensation. The optimum values depend on the converter topology, the component values and the operating conditions (including the input voltage, load current, etc.). To compensate the feedback loop of the LT3959, a series resistor-capacitor network is usually connected from the V_C pin to SGND. Figure 1 shows the typical V_C compensation network. For most applications, the capacitor should be in the range of 470pF to 22nF, and the resistor should be in the range of 5k to 50k. A small capacitor is often connected in parallel with the RC compensation network to attenuate the V_C voltage ripple induced from the output voltage ripple through the internal error amplifier. The parallel capacitor usually ranges in value from 10pF to 100pF. A practical approach to design the compensation network is to start with one of the circuits in this data sheet that is similar to your application, and tune the compensation network to optimize the performance. Stability should then be checked across all operating conditions, including load current, input voltage and temperature.

The Internal Power Switch Current

For control and protection, the LT3959 measures the internal power MOSFET current by using a sense resistor (R_{SENSE}) between GND and the MOSFET source. Figure 2 shows a typical wave-form of the internal switch current (I_{SW}).

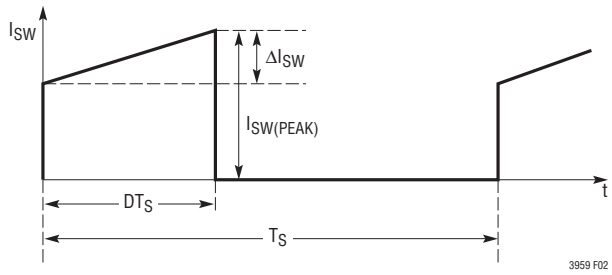


Figure 2. The SW Current During a Switching Cycle

Due to the current limit (minimum 6A) of the internal power switch, the LT3959 should be used in the applications that the switch peak current $I_{SW(PEAK)}$ during steady state normal operation is lower than 6A by a sufficient margin (10% or higher is recommended).

It is recommended to measure the IC temperature in steady state to verify that the junction temperature limit (125°C) is not exceeded. A low switching frequency may be required to ensure $T_{J(MAX)}$ does not exceed 125°C.

If LT3959 die temperature reaches thermal lockout threshold at 165°C (typical), the IC will initiate several protective actions. The power switch will be turned off. A soft-start operation will be triggered. The IC will be enabled again when the junction temperature has dropped by 5°C (nominal).

APPLICATION CIRCUITS

The LT3959 can be configured as different topologies. The design procedure for component selection differs somewhat between these topologies. The first topology to be analyzed will be the boost converter, followed by SEPIC and inverting converters.

APPLICATIONS INFORMATION

Boost Converter: Switch Duty Cycle and Frequency

The LT3959 can be configured as a boost converter for the applications where the converter output voltage is higher than the input voltage. Remember that boost converters are not short-circuit protected. Under a shorted output condition, the inductor current is limited only by the input supply capability. For applications requiring a step-up converter that is short-circuit protected, please refer to the Applications Information section covering SEPIC converters.

The conversion ratio as a function of duty cycle is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D}$$

in continuous conduction mode (CCM).

For a boost converter operating in CCM, the duty cycle of the main switch can be calculated based on the output voltage (V_{OUT}) and the input voltage (V_{IN}). The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}}$$

The alternative to CCM, discontinuous conduction mode (DCM) is not limited by duty cycle to provide high conversion ratios at a given frequency. The price one pays is reduced efficiency and substantially higher switching current.

Boost Converter: Maximum Output Current Capability and Inductor Selection

For the boost topology, the maximum average inductor current is:

$$I_{L(MAX)} = I_{O(MAX)} \bullet \frac{1}{1-D_{MAX}}$$

Due to the current limit of its internal power switch, the LT3959 should be used in a boost converter whose maximum output current ($I_{O(MAX)}$) is less than the maximum output current capability by a sufficient margin (10% or higher is recommended):

$$I_{O(MAX)} < \frac{V_{IN(MIN)}}{V_{OUT}} \bullet (6A - 0.5 \bullet \Delta I_{SW})$$

The inductor ripple current ΔI_{SW} has a direct effect on the choice of the inductor value and the converter's maximum output current capability. Choosing smaller values of ΔI_{SW} increases output current capability, but requires large inductances and reduces the current loop gain (the converter will approach voltage mode). Accepting larger values of ΔI_{SW} provides fast transient response and allows the use of low inductances, but results in higher input current ripple and greater core losses, and reduces output current capability.

Given an operating input voltage range, and having chosen the operating frequency and ripple current in the inductor, the inductor value of the boost converter can be determined using the following equation:

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \bullet f_{OSC}} \bullet D_{MAX}$$

The peak inductor current is the switch current limit (7A typical), and the RMS inductor current is approximately equal to $I_{L(MAX)}$. The user should choose the inductors having sufficient saturation and RMS current ratings.

Boost Converter: Output Diode Selection

To maximize efficiency, a fast switching diode with low forward drop and low reverse leakage is desirable. The peak reverse voltage that the diode must withstand is equal to the regulator output voltage plus any additional ringing across its anode-to-cathode during the on-time. The average forward current in normal operation is equal to the output current.

APPLICATIONS INFORMATION

It is recommended that the peak repetitive reverse voltage rating V_{RRM} is higher than V_{OUT} by a safety margin (a 10V safety margin is usually sufficient).

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

Where V_D is diode's forward voltage drop, and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{\theta JA}$$

The $R_{\theta JA}$ to be used in this equation normally includes the $R_{\theta JC}$ for the device plus the thermal resistance from the board to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

Boost Converter: Output Capacitor Selection

Contributions of ESR (equivalent series resistance), ESL (equivalent series inductance) and the bulk capacitance must be considered when choosing the correct output capacitors for a given output ripple voltage. The effect of these three parameters (ESR, ESL and bulk C) on the output voltage ripple waveform for a typical boost converter is illustrated in Figure 3.

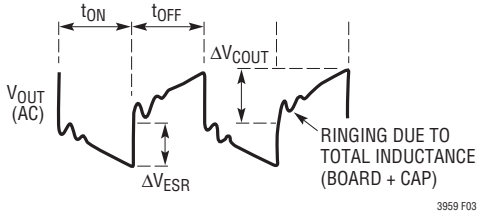


Figure 3. The Output Ripple Waveform of a Boost Converter

The choice of component(s) begins with the maximum acceptable ripple voltage (expressed as a percentage of the output voltage), and how this ripple should be divided between the ESR step ΔV_{ESR} and charging/discharging ΔV_{COUT}. For the purpose of simplicity, we will choose 2% for the maximum output ripple, to be divided equally between ΔV_{ESR} and ΔV_{COUT}. This percentage ripple will change, depending on the requirements of the application, and the following equations can easily be modified. For a 1% contribution to the total ripple voltage, the ESR of the output capacitor can be determined using the following equation:

$$ESR_{COUT} \le \frac{0.01 \bullet V_{OUT}}{I_{D(PEAK)}}$$

For the bulk C component, which also contributes 1% to the total ripple:

$$C_{OUT} \ge \frac{I_{O(MAX)}}{0.01 \bullet V_{OUT} \bullet f_{OSC}}$$

The output capacitor in a boost regulator experiences high RMS ripple currents, as shown in Figure 3. The RMS ripple current rating of the output capacitor can be determined using the following equation:

$$I_{RMS(COUT)} \ge I_{O(MAX)} \bullet \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

Multiple capacitors are often paralleled to meet ESR requirements. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the required RMS current rating. Additional ceramic capacitors in parallel are commonly used to reduce the effect of parasitic inductance in the output capacitor, which reduces high frequency switching noise on the converter output.

Boost Converter: Input Capacitor Selection

The input capacitor of a boost converter is less critical than the output capacitor, due to the fact that the inductor is in series with the input, and the input current waveform is continuous. The input voltage source impedance determines the size of the input capacitor, which is typically in the range of 10µF to 100µF. A low ESR capacitor is recommended, although it is not as critical as for the output capacitor.

The RMS input capacitor ripple current for a boost converter is:

$$I_{RMS(CIN)} = 0.3 \bullet \Delta I_L$$

APPLICATIONS INFORMATION

SEPIC CONVERTER APPLICATIONS

The LT3959 can be configured as a SEPIC (single-ended primary inductance converter), as shown in Figure 1. This topology allows for the input to be higher, equal, or lower than the desired output voltage. The conversion ratio as a function of duty cycle is:

$$\frac{V_{OUT}+V_D}{V_{IN}}=\frac{D}{1-D}$$

In continuous conduction mode (CCM).

In a SEPIC converter, no DC path exists between the input and output. This is an advantage over the boost converter for applications requiring the output to be disconnected from the input source when the circuit is in shutdown.

SEPIC Converter: Switch Duty Cycle and Frequency

For a SEPIC converter operating in CCM, the duty cycle of the main switch can be calculated based on the output voltage (V_{OUT}), the input voltage (V_{IN}) and diode forward voltage (V_D).

The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage:

$$D_{MAX}=\frac{V_{OUT}+V_D}{V_{IN(MIN)}+V_{OUT}+V_D}$$

SEPIC Converter: The Maximum Output Current Capability and Inductor Selection

As shown in Figure 1, the SEPIC converter contains two inductors: L1 and L2. L1 and L2 can be independent, but can also be wound on the same core, since identical voltages are applied to L1 and L2 throughout the switching cycle.

For the SEPIC topology, the current through L1 is the converter input current. Based on the fact that, ideally, the output power is equal to the input power, the maximum average inductor currents of L1 and L2 are:

$$I_{L1(MAX)}=I_{IN(MAX)}=I_{O(MAX)}\bullet\frac{D_{MAX}}{1-D_{MAX}}$$

$$I_{L2(MAX)}=I_{O(MAX)}$$

Due to the current limit of it's internal power switch, the LT3959 should be used in a SEPIC converter whose maximum output current (IO(MAX)) is less than the output current capability by a sufficient margin (10% or higher is recommended):

$$I_{O(MAX)} < (1-D_{MAX})\bullet(6A-0.5\bullet\Delta I_{SW})$$

The inductor ripple currents ΔI_{L1} and ΔI_{L2} are identical:

$$\Delta I_{L1}=\Delta I_{L2}=0.5\bullet\Delta I_{SW}$$

The inductor ripple current ΔI_{SW} has a direct effect on the choice of the inductor value and the converter's maximum output current capability. Choosing smaller values of ΔI_{SW} requires large inductances and reduces the current loop gain (the converter will approach voltage mode). Accepting larger values of ΔI_{SW} allows the use of low inductances, but results in higher input current ripple and greater core losses and reduces output current capability.

Given an operating input voltage range, and having chosen the operating frequency and ripple current in the inductor, the inductor value (L1 and L2 are independent) of the SEPIC converter can be determined using the following equation:

$$L1=L2=\frac{V_{IN(MIN)}}{0.5\bullet\Delta I_{SW}\bullet f_{OSC}}\bullet D_{MAX}$$

For most SEPIC applications, the equal inductor values will fall in the range of 1µH to 100µH.

By making L1 = L2, and winding them on the same core, the value of inductance in the preceding equation is replaced by 2L, due to mutual inductance:

$$L=\frac{V_{IN(MIN)}}{\Delta I_{SW}\bullet f_{OSC}}\bullet D_{MAX}$$

This maintains the same ripple current and energy storage in the inductors. The peak inductor currents are:

$$I_{L1(PEAK)}=I_{L1(MAX)}+0.5\bullet\Delta I_{L1}$$

$$I_{L2(PEAK)}=I_{L2(MAX)}+0.5\bullet\Delta I_{L2}$$

The maximum RMS inductor currents are approximately equal to the maximum average inductor currents.

APPLICATIONS INFORMATION

Based on the preceding equations, the user should choose the inductors having sufficient saturation and RMS current ratings.

SEPIC Converter: Output Diode Selection

To maximize efficiency, a fast switching diode with a low forward drop and low reverse leakage is desirable. The average forward current in normal operation is equal to the output current.

It is recommended that the peak repetitive reverse voltage rating V_{RRM} is higher than $V_{OUT} + V_{IN(MAX)}$ by a safety margin (a 10V safety margin is usually sufficient).

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

where V_D is diode's forward voltage drop, and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{\theta JA}$$

The $R_{\theta JA}$ used in this equation normally includes the $R_{\theta JC}$ for the device, plus the thermal resistance from the board, to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

SEPIC Converter: Output and Input Capacitor Selection

The selections of the output and input capacitors of the SEPIC converter are similar to those of the boost converter. Please refer to the Boost Converter, Output Capacitor Selection and Boost Converter, Input Capacitor Selection sections.

SEPIC Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC coupling capacitor (C_{DC}, as shown in Figure 1) should be larger than the maximum input voltage:

$$V_{CDC} > V_{IN(MAX)}$$

C_{DC} has nearly a rectangular current waveform. During the switch off-time, the current through C_{DC} is I_{IN}, while approximately $-I_O$ flows during the on-time. The RMS rating of the coupling capacitor is determined by the following equation:

$$I_{RMS(CDC)} > I_{O(MAX)} \bullet \sqrt{\frac{V_{OUT} + V_D}{V_{IN(MIN)}}}$$

A low ESR and ESL, X5R or X7R ceramic capacitor works well for C_{DC}.

INVERTING CONVERTER APPLICATIONS

The LT3959 can be configured as a dual-inductor inverting topology, as shown in Figure 4. The V_{OUT} to V_{IN} ratio is:

$$\frac{V_{OUT} - V_D}{V_{IN}} = -\frac{D}{1-D}$$

In continuous conduction mode (CCM).

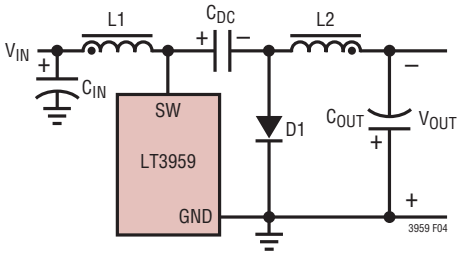


Figure 4. A Simplified Inverting Converter

Inverting Converter: Switch Duty Cycle and Frequency

For an inverting converter operating in CCM, the duty cycle of the main switch can be calculated based on the negative output voltage (V_{OUT}) and the input voltage (V_{IN}).

The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT} - V_D}{V_{OUT} - V_D - V_{IN(MIN)}}$$

APPLICATIONS INFORMATION

Inverting Converter: Output Diode and Input Capacitor Selections

The selections of the inductor, output diode and input capacitor of an inverting converter are similar to those of the SEPIC converter. Please refer to the corresponding SEPIC converter sections.

Inverting Converter: Output Capacitor Selection

The inverting converter requires much smaller output capacitors than those of the boost and SEPIC converters for similar output ripple. This is due to the fact that, in the inverting converter, the inductor L2 is in series with the output, and the ripple current flowing through the output capacitors are continuous. The output ripple voltage is produced by the ripple current of L2 flowing through the ESR and bulk capacitance of the output capacitor:

$$\Delta V_{OUT(P-P)} = \Delta I_{L2} \bullet \left(ESR_{COUT} + \frac{1}{8 \bullet f_{OSC} \bullet C_{OUT}} \right)$$

After specifying the maximum output ripple, the user can select the output capacitors according to the preceding equation.

The ESR can be minimized by using high quality X5R or X7R dielectric ceramic capacitors. In many applications, ceramic capacitors are sufficient to limit the output voltage ripple.

The RMS ripple current rating of the output capacitor needs to be greater than:

$$I_{RMS(COUT)} > 0.3 \bullet \Delta I_{L2}$$

Inverting Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC coupling capacitor (C_{DC}, as shown in Figure 4) should be larger than the maximum input voltage minus the output voltage (negative voltage):

$$V_{CDC} > V_{IN(MAX)} - V_{OUT}$$

C_{DC} has nearly a rectangular current waveform. During the switch off-time, the current through C_{DC} is I_{IN}, while approximately $-I_O$ flows during the on-time. The RMS rating of the coupling capacitor is determined by the following equation:

$$I_{RMS(CDC)} > I_{O(MAX)} \bullet \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

A low ESR and ESL, X5R or X7R ceramic capacitor works well for C_{DC}.

Board Layout

The high power and high speed operation of the LT3959 demands careful attention to board layout and component placement. Careful attention must be paid to the internal power dissipation of the LT3959 at high input voltages, high switching frequencies, and high internal power switch currents to ensure that a junction temperature of 125°C is not exceeded. This is especially important when operating at high ambient temperatures. Exposed pads on the bottom of the package are SGND and SW terminals of the IC, and must be soldered to a SGND ground plane and a SW plane respectively. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the IC and into the copper planes with as much as area as possible.

To prevent radiation and high frequency resonance problems, proper layout of the components connected to the IC is essential, especially the power paths with higher di/dt. The following high di/dt loops of different topologies should be kept as tight as possible to reduce inductive ringing:

- In boost configuration, the high di/dt loop contains the output capacitor, the internal power MOSFET and the Schottky diode.
- In SEPIC configuration, the high di/dt loop contains the internal power MOSFET, output capacitor, Schottky diode and the coupling capacitor.
- In inverting configuration, the high di/dt loop contains internal power MOSFET, Schottky diode and the coupling capacitor.

APPLICATIONS INFORMATION

Check the stress on the internal power MOSFET by measuring the SW-to-GND voltage directly across the IC terminals. Make sure the inductive ringing does not exceed the maximum rating of the internal power MOSFET (40V).

The small-signal components should be placed away from high frequency switching nodes. For optimum load regulation and true remote sensing, the top of the output voltage sensing resistor divider should connect independently to the top of the output capacitor (Kelvin connection), staying away from any high dV/dt traces. Place the divider resistors near the LT3959 in order to keep the high impedance FBX node short.

Figure 5 shows the suggested layout of the 2.5V to 8V input, 12V output boost converter in the Typical Application section.

APPLICATIONS INFORMATION

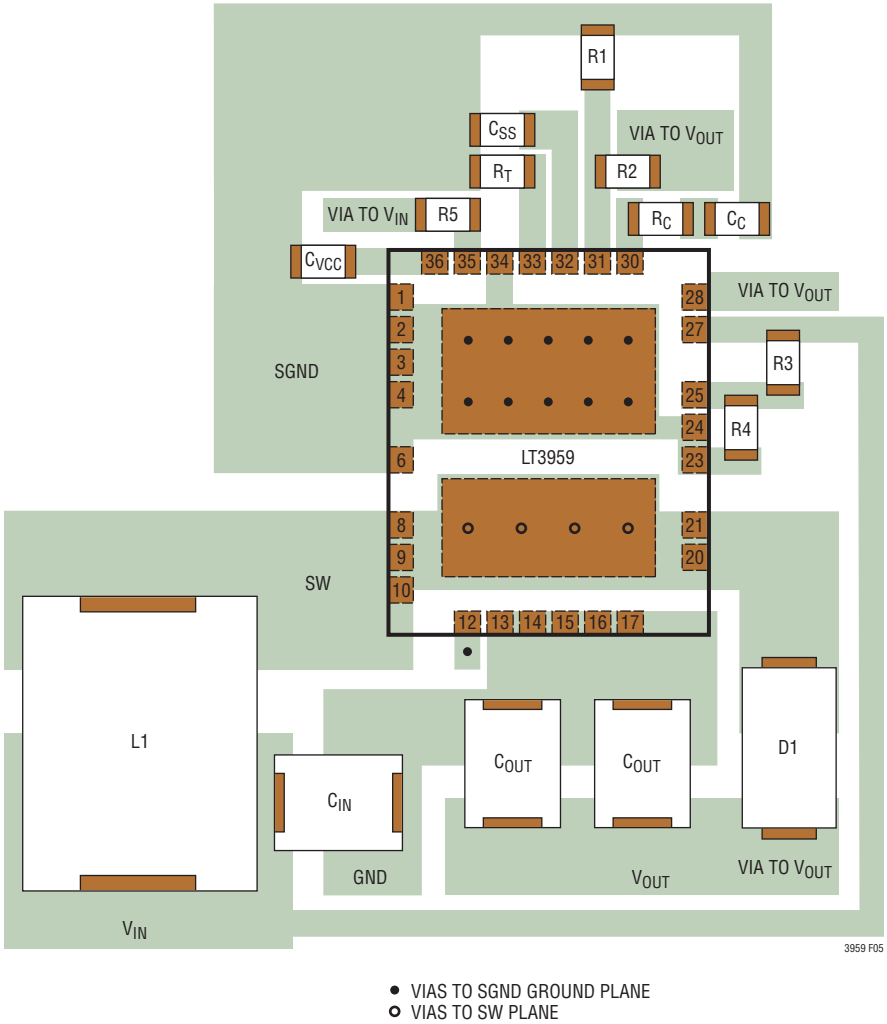
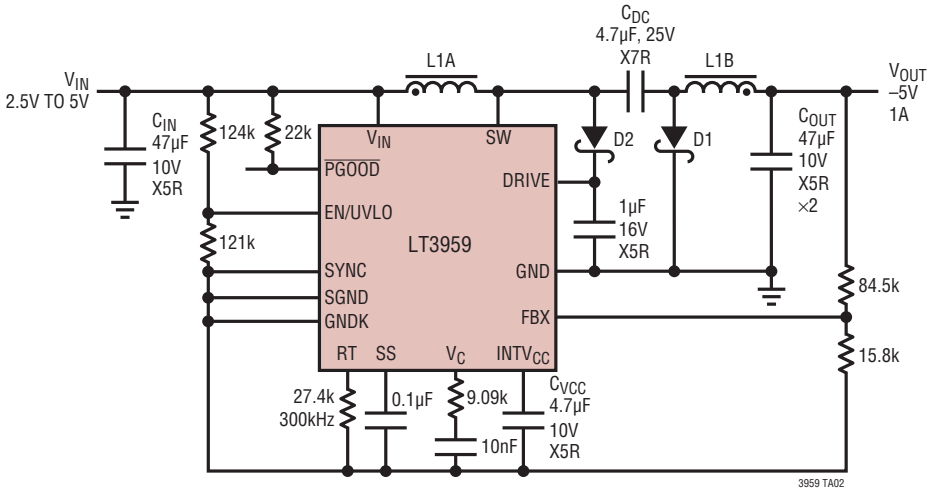


Figure 5. Suggested Layout of the 2.5V to 8V Input. 12V Output Boost Converter in the Typical Application Section (Shown for QFN Package)

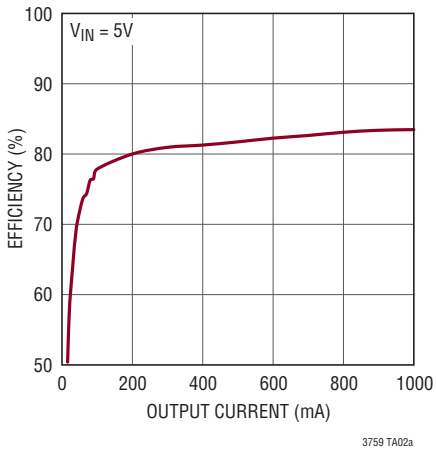
TYPICAL APPLICATIONS

2.5V to 5V Input, –5V Output Inverting Converter



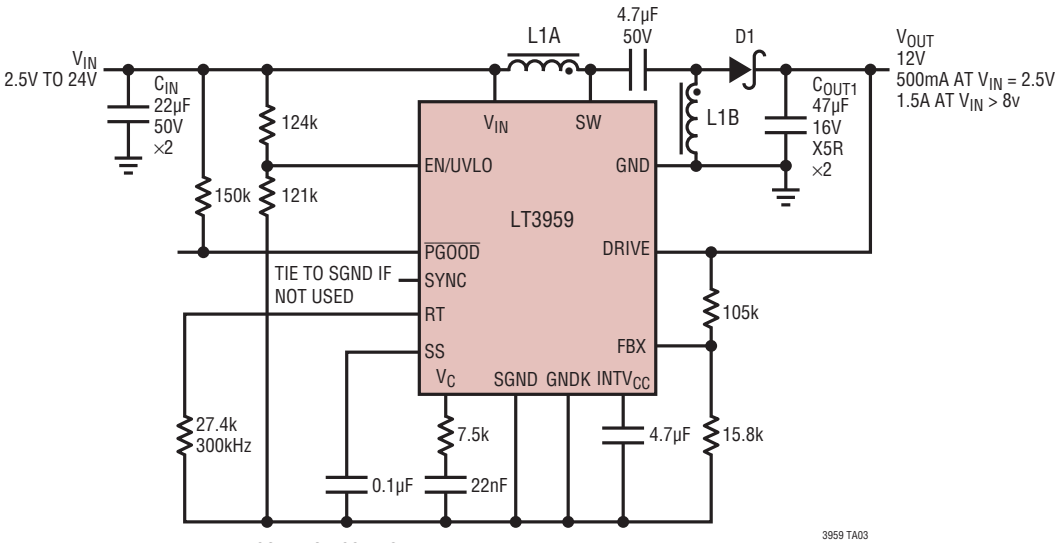
L1A, L1B: COILTRONICS DRQ127-3R3
D1: VISHAY 6CWQ03FN
D2: PHILIPS PMEG2005EJ

Efficiency vs Output Current



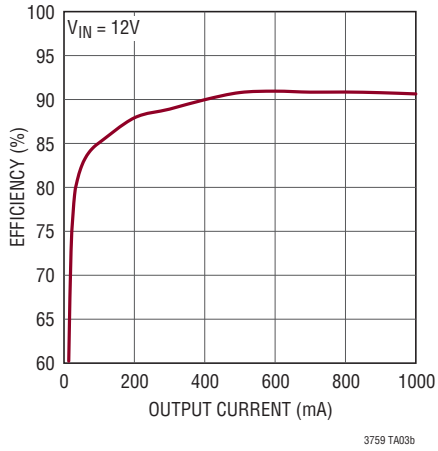
TYPICAL APPLICATIONS

2.5V to 24V Input, 12V Output SEPIC Converter

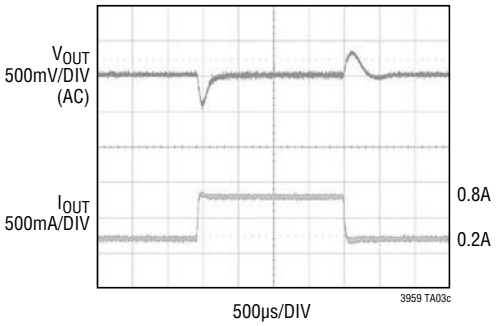


L1A, L1B: COILTRONICS DRQ127-150
D1: VISHAY 6CWQ06FN

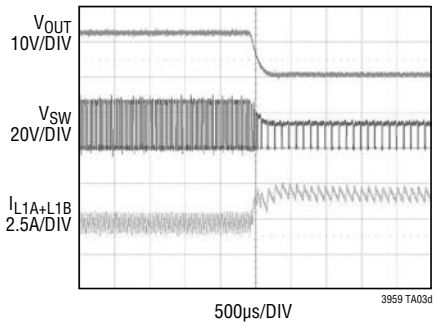
Efficiency vs Output Current



Load Step Response at V_{IN} = 12V

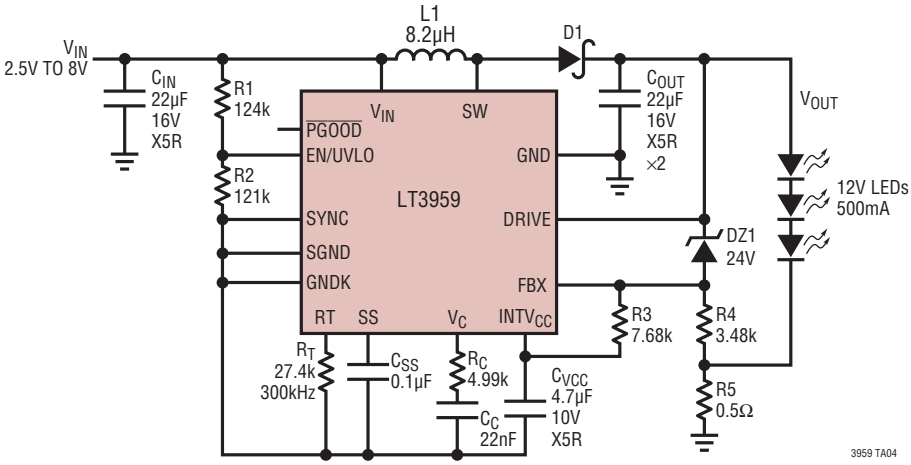


Frequency Foldback Waveforms When Output Short-Circuits



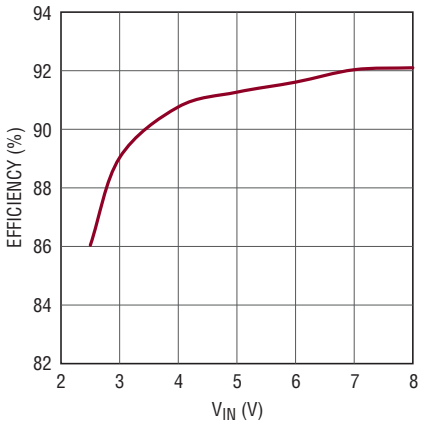
TYPICAL APPLICATIONS

2.5V to 8V Input, 12V LED Driver



L1: TOKO 962BS-BR2M
D1: VISHAY SILICONIX 20BQ030
DZ1: CENTRAL SEMICONDUCTOR CMHZ5252B

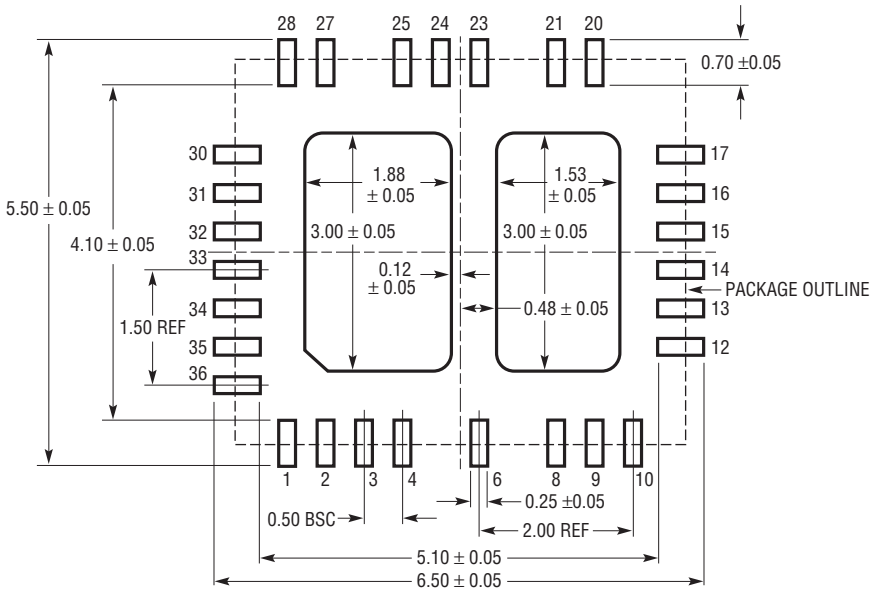
Efficiency vs V_{IN}



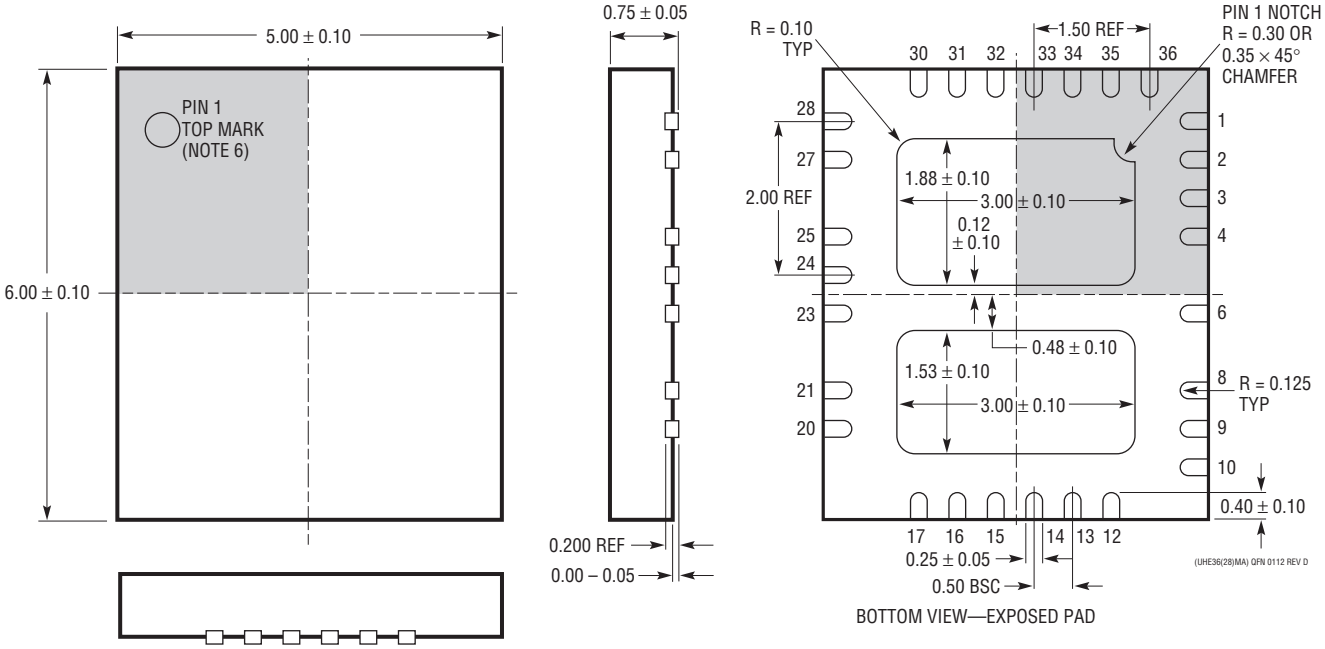
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UHE Package
Variation: UHE36(28)MA
36(28)-Lead Plastic QFN (5mm × 6mm)
(Reference LTC DWG # 05-08-1836 Rev D)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



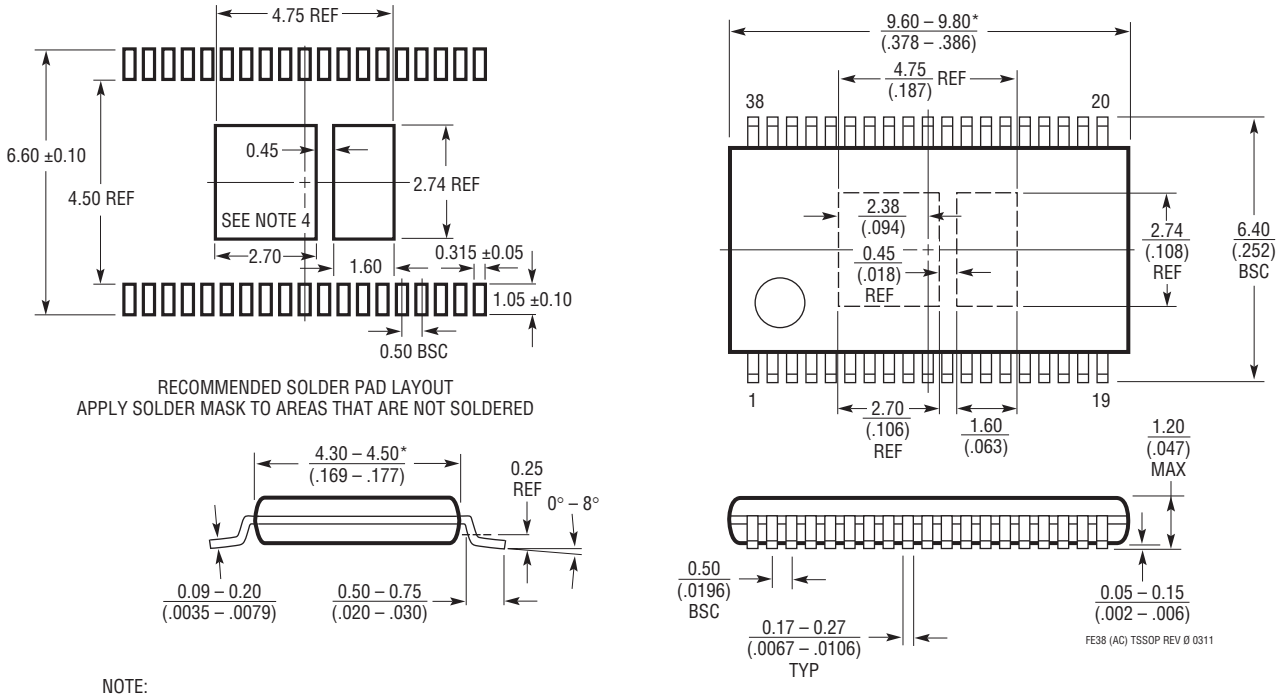
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
38-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1779 Rev Ø)
Split Exposed Pad Variation AC



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/13	Added TSSOP-28 package	1, 2, 7, 24