3A Monolithic Buck-Boost Supercapacitor Charger and Balancer with Accurate Input Current Limit

FEATURES

- **±2% Accurate Average Input Current Limit Programmable Up to 3A**
- **Programmable Maximum Capacitor Voltage Limit**
- **Active Charge Balancing for Fast Charging of Unmatched Capacitors**
- **Charges Single or Stacked Capacitors**
- **V_{IN} Range: 1.73V to 5.5V**
- **V_{OUT} Range: 1.8V to 5.5V**
- **<2µA Quiescent Current from V_{OUT} When Charged**
- Output Disconnect in Shutdown: <1µA I_Q Shutdown
- Power-Good Comparator
- Power Failure Indicator
- Thermally Enhanced 20-Lead (4mm × 5mm × 0.75mm) QFN and 24-Lead TSSOP Packages

APPLICATIONS

- Supercapacitor Based Backup Power
- Memory Backup
- Servers, RAID, RF Systems
- Industrial, Communications, Computing

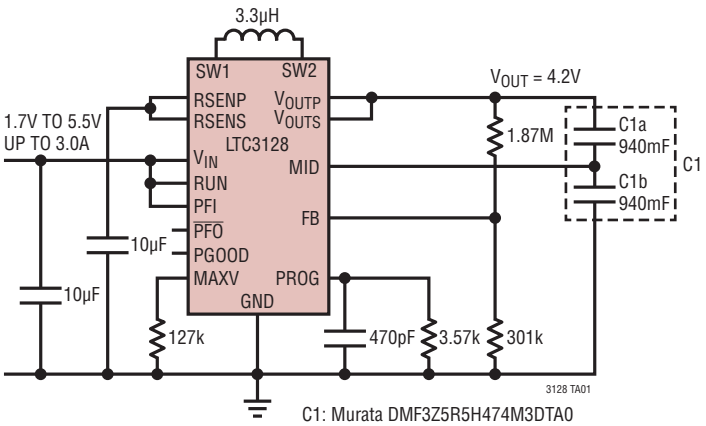
DESCRIPTION

The LTC®3128 is a highly efficient, buck-boost DC/DC supercapacitor charger. It operates efficiently from input voltages above, below or equal to the output voltage. The LTC3128 incorporates accurate programmable average input current limit, active charge balancing and programmable maximum capacitor voltage. This combination of features makes the LTC3128 ideal for safely charging and protecting large capacitors in backup power systems. The input current limit and maximum capacitor voltage are each programmed using a single resistor. Average input current is accurately controlled over a 0.5A to 3A programmable range while the individual maximum capacitor voltage can be set from 1.8V to 3.0V.

Other features of the LTC3128 include <2µA quiescent current from V_{OUT} in Burst Mode®operation, accurate power-good and power failure indicators, and thermal overload protection. The LTC3128 is offered in low profile, thermally enhanced 20-Lead 4mm × 5mm × 0.75mm QFN and 24-Lead TSSOP packages.

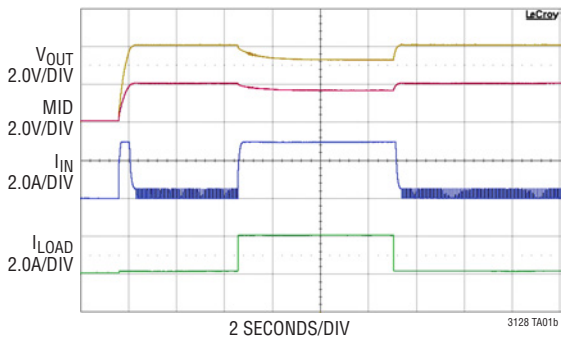
TYPICAL APPLICATION

Wide V_{IN} (3A Programmed Input Current) to 4.2V



C1: Murata DMF3Z5R5H474M3DTA0

Stacked Output Capacitors Charging Waveform

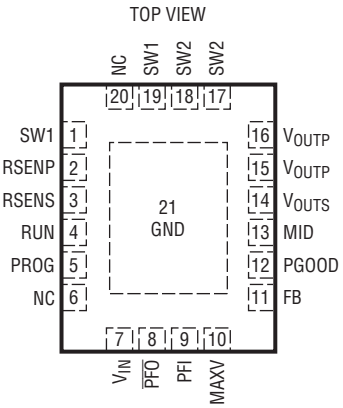


ABSOLUTE MAXIMUM RATINGS

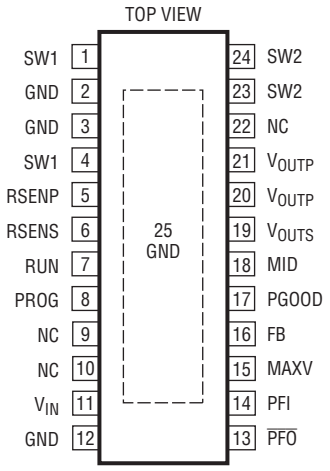
(Note 1)

V_{IN}, RSENP, V_{OUTP}, MID Voltage ..... –0.3V to 6V
RSENS, V_{OUTS} Voltage ..... –0.3V to 6V
RSENS DC Current ..... –4A
SW1, SW2 DC Voltage ..... –0.3V to 6V
SW1, SW2 Pulsed (<100ns) Voltage ..... –1.0V to 7V
PGOOD, $\overline{PFO}$, RUN Voltage ..... –0.3V to 6V
PROG, MAXV, FB, PFI Voltage ..... –0.3V to 6V
PGOOD, $\overline{PFO}$ DC Current 15mA
Operating Junction Temperature Range
(Notes 2, 4) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
FE Only ..... 300°C

PIN CONFIGURATION



UFD PACKAGE
20-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB (NOTE 5)



FE PACKAGE
24-LEAD PLASTIC TSSOP
T_{JMAX} = 125°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 25) SHOULD BE SOLDERED TO PCB (NOTE 5)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3128EUFD#PBF	LTC3128EUFD#TRPBF	3128	20-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3128IUFD#PBF	LTC3128IUFD#TRPBF	3128	20-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3128EFE#PBF	LTC3128EFE#TRPBF	LTC3128FE	24-Lead Plastic TSSOP	–40°C to 125°C
LTC3128IFE#PBF	LTC3128IFE#TRPBF	LTC3128FE	24-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 3.3V, V_{OUT} = 4.8V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Operating Range		●	1.73		5.5	V
Programmed Output Voltage Range		●	1.8		5. 5	V
FB Voltage		●	0.565	0.580	0.590	V
FB Voltage Hysteresis				8.5		mV
FB Input Current	FB > 0.590V			0.5	2	nA
Switching Frequency	While Charging	●	1.00	1.20	1.40	MHz
Power Good Rising Threshold Voltage	Measured as a % of FB Voltage	●	94.50	96.75	99.00	%FB
Power Good Hysteresis	Measured as a % of FB Voltage			3.6		%
Power Good Voltage Low	I_{PGOOD} = 5mA			200		mV
Power Good Leakage Current	PGOOD = 5.5V			0.1	1	µA
PFI Falling Threshold		●	0.565	0.580	0.590	V
PFI Hysteresis Current	V_{PFI} < 0.565V			0.2		µA
PFI Input Current	V_{PFI} > 0.590V			0.5	2	nA
$\overline{PFO}$ Voltage Low	$I_{\overline{PFO}}$ = 5mA			200		mV
$\overline{PFO}$ Leakage Current	$\overline{PFO}$ = 5.5V			0.1	1	µA
Maximum Capacitor Voltage – Rising	R_{MAXV} = 125k, –40°C to 125°C (Note 7) R_{MAXV} = 125k, 0°C to 85°C (Notes 6, 7) R_{MAXV} = 113k, –40°C to 125°C (Note 7) R_{MAXV} = 113k, 0°C to 85°C (Notes 6, 7)	● ● ● ●	2.350 2.400 2.150 2.170	2.500 2.500 2.260 2.260	2.650 2.600 2.380 2.350	V V V V
Maximum Capacitor Voltage Hysteresis				120	200	mV
MAXV Pin Current				20		µA
V_{IN} Quiescent Current – Sleep	V_{RUN} = 3.3V, V_{FB} > 0.590V			14		µA
V_{OUT} Quiescent Current – Sleep	V_{RUN} = 3.3V, Not Balancing, V_{FB} > 0.590V V_{RUN} = 3.3V, Balancing, V_{FB} > 0.590V			1.9 100		µA µA
V_{IN} Quiescent Current – Shutdown	V_{RUN} = 0V, Not Including SW Leakage			0.6	1	µA
V_{OUT} Quiescent Current – Shutdown	V_{RUN} = 0V, Not Including SW Leakage			0.4	1	µA
V_{OUT} Quiescent Current – Shutdown	V_{RUN} = 0V, V_{IN} = 0V, Not Including SW Leakage			0.4	1	µA
V_{IN} Quiescent Current – Active	V_{RUN} = 3.3V (Note 3)			600		µA
V_{IN} Quiescent Current – UVLO	V_{RUN} = 1.5V, V_{IN} = 1.5V, Not Including SW Leakage			25		µA
V_{OUT} Quiescent Current – UVLO	V_{RUN} = 1.5V, V_{IN} = 1.5V, Not Including SW Leakage			1	2	µA
Input Current Limit	R_{PROG} = 22.1k (Notes 3, 7) R_{PROG} = 22.1k (Notes 3, 7) R_{PROG} = 11k (Notes 3, 7) R_{PROG} = 11k (Notes 3, 7) R_{PROG} = 5.49k (Notes 3, 7) R_{PROG} = 5.49k (Notes 3, 7) R_{PROG} = 3.57k (Notes 3, 7) R_{PROG} = 3.57k (Notes 3, 7)	 ● ● ● ●	489 475 985 958 1973 1923 3034 2951	497 497 1000 1000 2003 2003 3081 3081	504 515 1015 1035 2033 2075 3127 3185	mA mA mA mA mA mA mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 3.3V, V_{OUT} = 4.8V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PROG Pin Gain	Measured at I_{IN} = 1A (Note 3)			52.7		µA/A
Internal Sense Resistor Value	(Note 6)			50		mΩ
Peak Inductor Current Limit	(Note 3)	●	5.50	6.5	9.00	A
Linear Inductor Current Limit	(Note 3)	●	4.00	5.0	6.85	A
N-Channel MOSFET Leakage	Switches B and C and E			0.1	5	µA
P-Channel MOSFET Leakage	Switches A and D Switch F			0.1 0.1	5 10	µA µA
N-Channel MOSFET On-Resistance	Switch B Switch C Switch E (V_{OUT} = 0V)			70 80 95		mΩ mΩ mΩ
P-Channel MOSFET On-Resistance	Switch A Switch D Switch F			45 40 300		mΩ mΩ mΩ
MID Leakage Current	V_{MID} = 0V, V_{IN} = 3.3V, V_{SW1} = 3.3V			0.1	10	µA
MID Pin Regulation	V_{OUT} = 4.8V	●	2.304	2.400	2.496	V
Active Charge Balancer Enable Threshold	$\lvert V_{OUT}/2\text{-}V_{MID}\rvert$			60	118	mV
Active Charge Balancer Hysteresis				60		mV
Active Charge Balancer Peak Current	(Note 3)			400		mA
Active Charge Balancer Valley Current	(Note 3)			50		mA
RUN Input High Threshold Voltage		●	1.2			V
RUN Input Low Threshold Voltage		●			0.3	V
RUN Input Current	RUN = 5.5V			0.01	1	µA

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. The LTC3128 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3128E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3128I is guaranteed over the full –40°C to 125°C operating junction temperature range.

The junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA}°C/W)$, where θ_{JA} is the package thermal impedance. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3. Current measurements are made when the output is not switching.

Note 4. This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

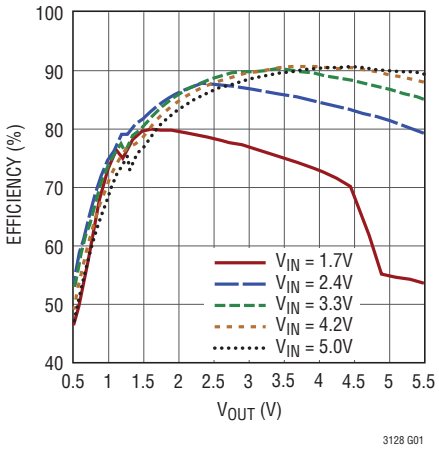
Note 5. Failure to solder the exposed backside of the package to the PC board ground plane will result in a thermal resistance much higher than 43°C/W in the QFN and 38°C/W in the TSSOP.

Note 6. Guaranteed by design. Not tested.

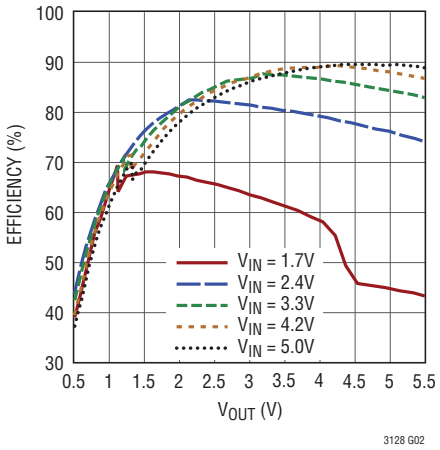
Note 7. Accuracy of this specification is directly related to the accuracy of the resistor used to program the parameter.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

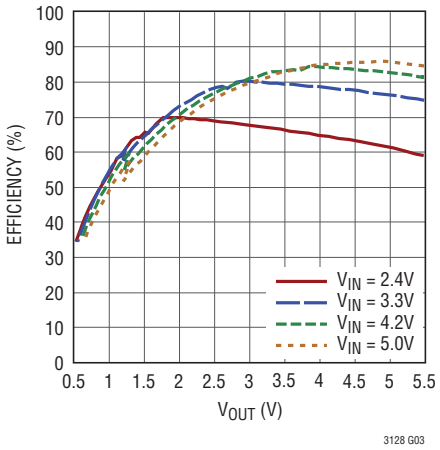
Efficiency vs V_{OUT} (0.5A I_{IN})



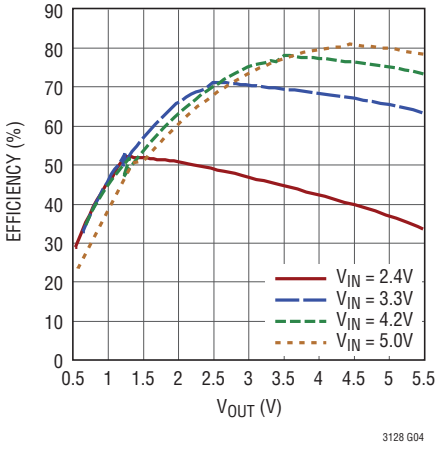
Efficiency vs V_{OUT} (1.0A I_{IN})



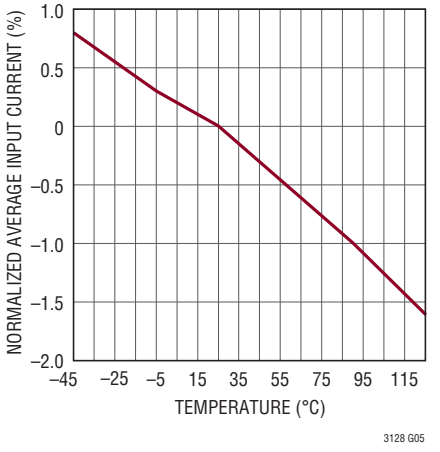
Efficiency vs V_{OUT} (2.0A I_{IN})



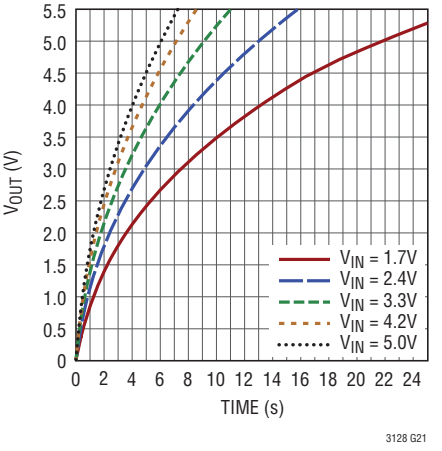
Efficiency vs V_{OUT} (3.0A I_{IN})



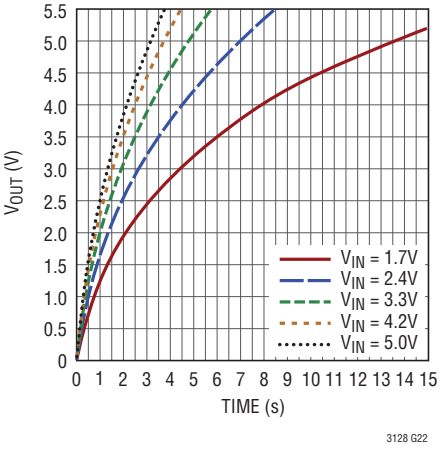
Average Input Current Limit vs Temperature (Normalized)



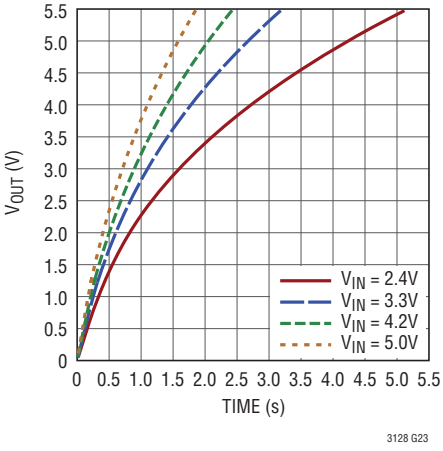
V_{OUT} vs Charge Time, C_{OUT} = 1F, R_{ESR} = 20mΩ, I_{IN} = 0.5A



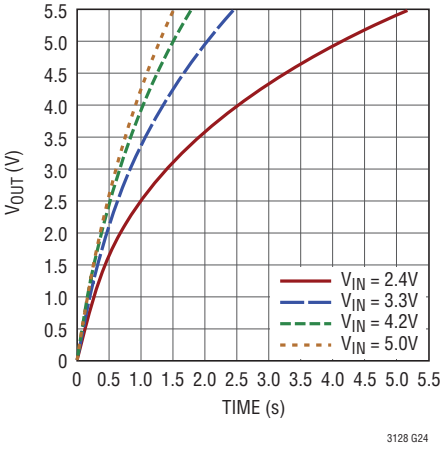
V_{OUT} vs Charge Time, C_{OUT} = 1F, R_{ESR} = 20mΩ, I_{IN} = 1.0A



V_{OUT} vs Charge Time, C_{OUT} = 1F, R_{ESR} = 20mΩ, I_{IN} = 2.0A

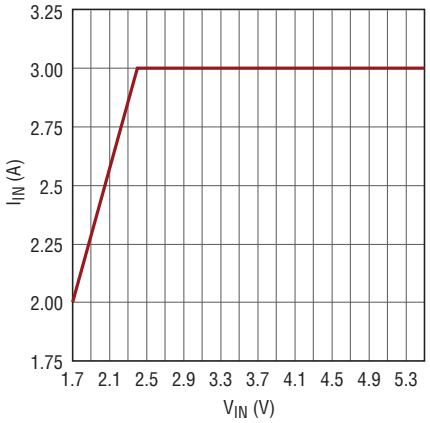


V_{OUT} vs Charge Time, C_{OUT} = 1F, R_{ESR} = 20mΩ, I_{IN} = 3.0A



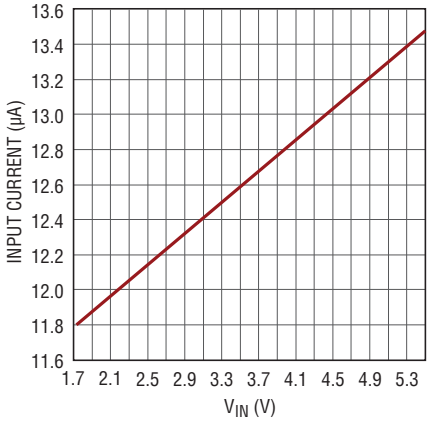
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Maximum Programmable I_{IN} vs V_{IN}



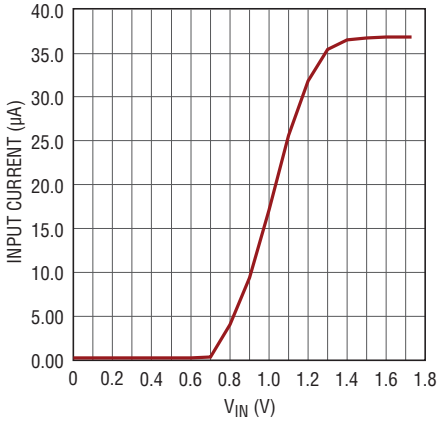
3128 G06

V_{IN} Quiescent Current vs V_{IN} (Burst Mode Operation Sleep)



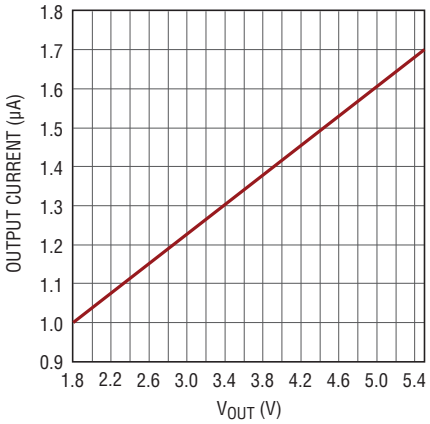
3128 G07

V_{IN} Quiescent Current vs V_{IN} (Input UVLO)



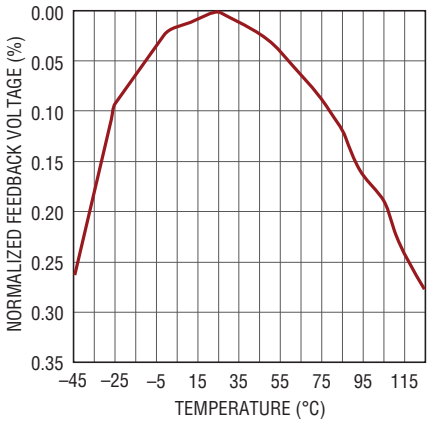
3128 G08

V_{OUT} Quiescent Current vs V_{OUT} (Burst Mode Operation Sleep)



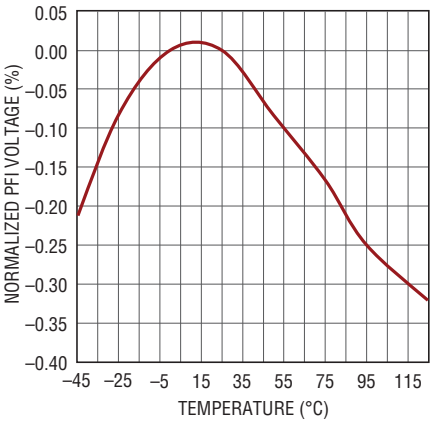
3128 G09

Feedback Voltage vs Temperature (Normalized)



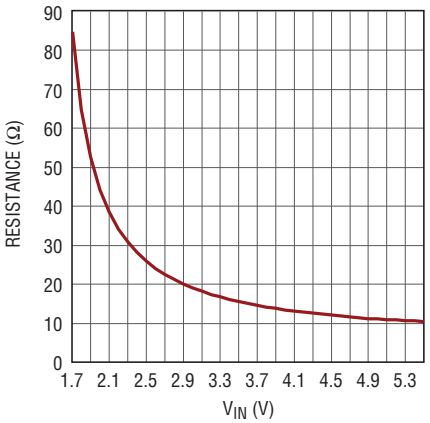
3128 G10

PFI Voltage vs Temperature (Normalized)



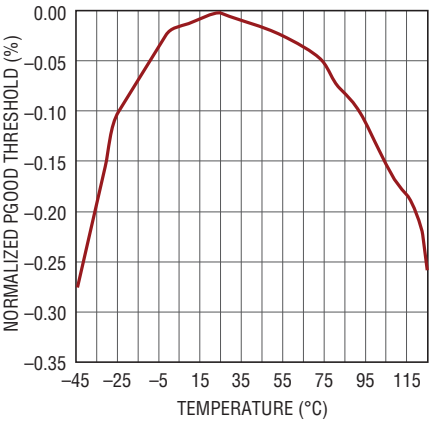
3128 G11

PFO Pull Down Resistance vs V_{IN}



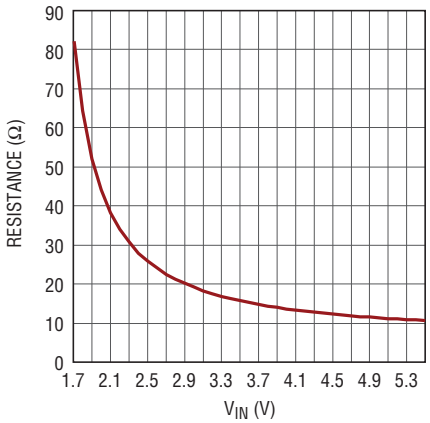
3128 G12

PGOOD Threshold vs Temperature (Normalized)



3128 G13

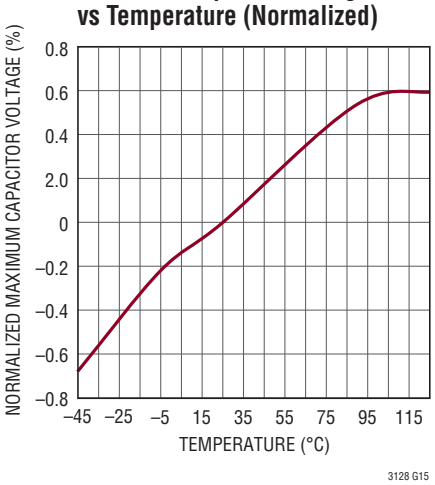
PGOOD Pull Down Resistance vs V_{IN}



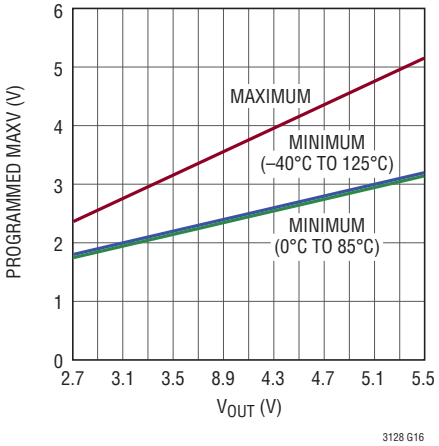
3128 G14

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

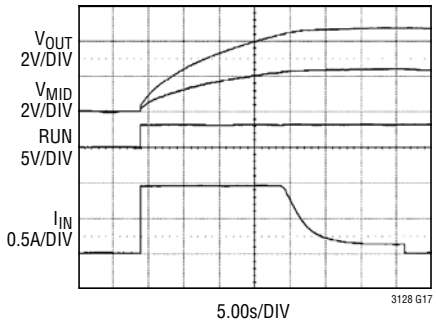
Maximum Capacitor Voltage vs Temperature (Normalized)



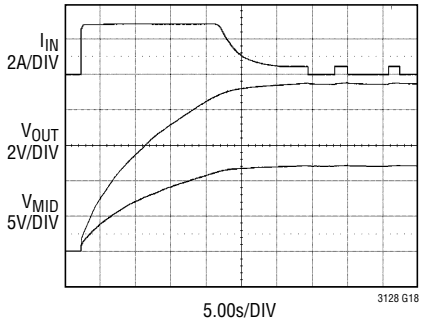
Minimum and Maximum Programmed Capacitor Voltage vs Programmed V_{OUT}



Startup Waveform 1.0A Input Current Limit



Startup Waveform 3.0A Input Current Limit



PIN FUNCTIONS (QFN/TSSOP)

SW1 (Pins 1, 19/Pins 1, 4): Switch pin where internal switches A and B are connected. Connect an inductor from SW1 to SW2.

RSENP (Pin 2/Pin 5): Sense Resistor Power Output. Connect other loads in the system to this pin. A 10µF or greater ceramic capacitor should be placed as close to RSENP and GND as possible.

RSENS (Pin 3/Pin 6): Sense Resistor Signal Input. This pin should be connected to RSENP through as short and wide a trace as possible.

RUN (Pin 4/Pin 7): Logic-Controlled Shutdown Input.

RUN ≥ 1.2V: Normal Operation
RUN ≤ 0.3V: Shutdown

PROG (Pin 5/Pin 8): Sets the average input current limit threshold. Connect a resistor and capacitor from PROG to GND. See below for component value selection.

R_{PROG} (kΩ) = 11/I_{LIMIT} (A)
C_{PROG} (pF) = 1600/(R_{PROG} (kΩ))

NC (Pins 6, 20/Pins 9, 10, 22): Not Connected. These pins should be tied to ground.

V_{IN} (Pin 7/Pin 11): Input Supply Pin. Internal V_{CC} for the IC and high current input to the internal sense resistor. A 10µF or greater ceramic capacitor should be placed as close to V_{IN} and GND as possible.

$\overline{PFO}$ (Pin 8/Pin 13): Power Fail Output. This is an open-drain output that sinks current when the supply being monitored is less than the programmed threshold voltage.

PFI (Pin 9/Pin 14): Power Fail Input. Connect resistor divider tap from supply to be monitored here. See below for component selection.

$V_{PFI(FALLING)}$ (V) = 0.58 • (1+R4/R3)
$V_{PFIHYST}$ (V) = R4 • 0.2µA

MAXV (Pin 10/Pin 15): Sets the maximum capacitor voltage across each capacitor. Connect a resistor from MAXV to GND. See below for component value selection. If charging only a single capacitor, tie this pin to ground.

R_{MAXV} (kΩ) = 50 • V_{MAXV}(V)

FB (Pin 11/Pin 16): Output Voltage Feedback Pin. Connect resistor divider tap here. The output voltage can be adjusted from 1.8V to 5.5V. The feedback reference voltage is 0.58V.

V_{OUT} (V) = 0.58 • (1+R2/R1)

PGOOD (Pin 12/Pin 17): Power Good Indicator. This is an open-drain output that pulls low when V_{OUT} is less than 96.75% of the programmed voltage.

MID (Pin 13/Pin 18): Output for the active charger balancer. This pin should be tied to the junction of the two output capacitors. If charging only a single output capacitor, tie this pin to ground as shown in the applications section.

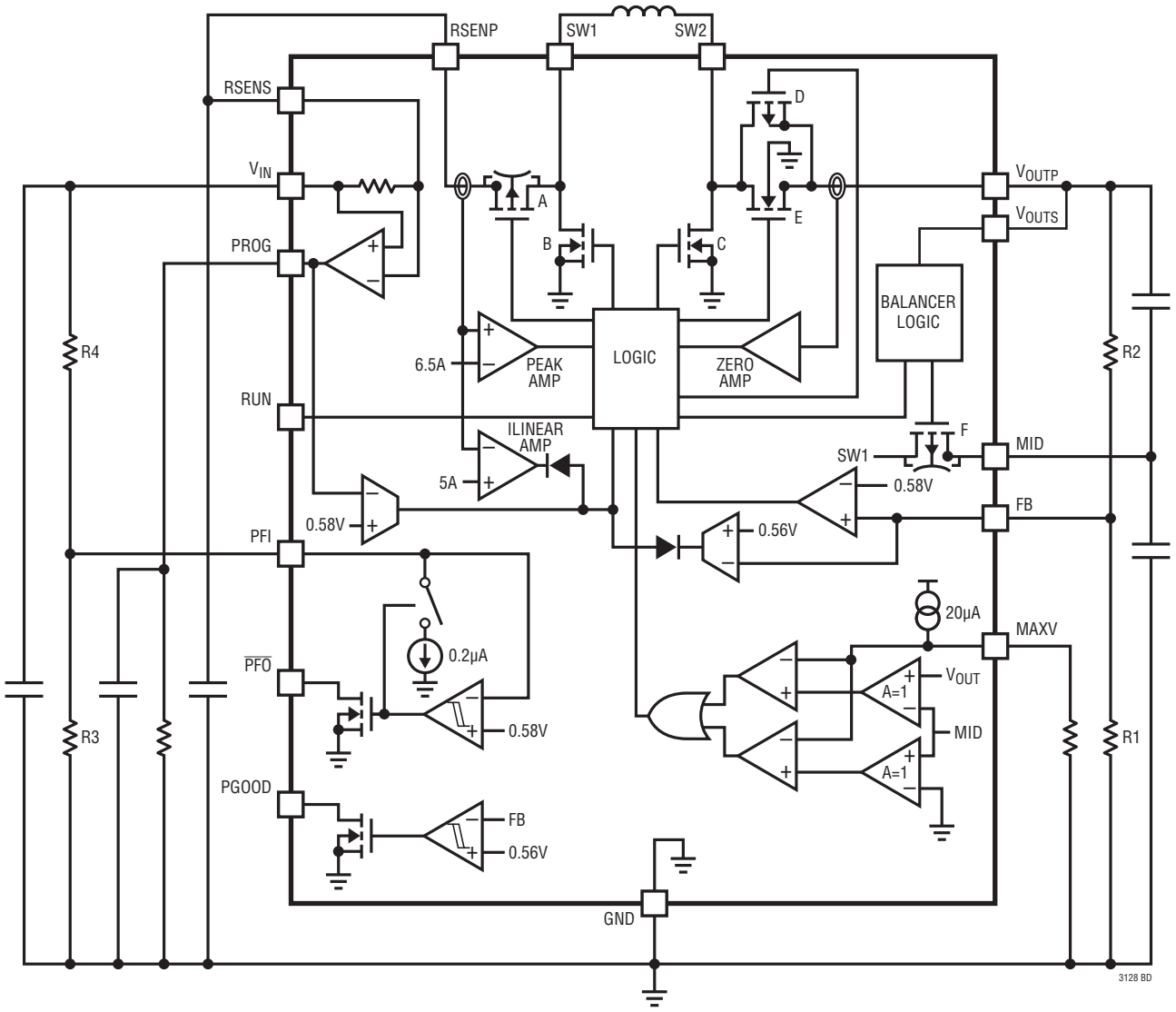
V_{OUTS} (Pin 14/Pin 19): Output Sense Input. This pin should be connected to the V_{OUT} capacitor through as short a trace as possible.

V_{OUTP} (Pins 15,16/Pins 20, 21): Output of the Synchronous Rectifier. Connect the output filter capacitor from this pin to GND. See the applications information section for capacitor recommendations.

SW2 (Pins 17,18/Pins 23, 24): Switch pin where internal switches C and D are connected. Connect inductor from SW1 to SW2.

GND (Exposed Pad Pin 21/Pins 2, 3, 12 Exposed Pad Pin 25): IC and Power Ground. **The exposed pad must be soldered to the PCB ground plane through a good electrical and thermal connection.**

BLOCK DIAGRAM



OPERATION

The LTC3128 is an average input current controlled buck-boost DC/DC charger offered in both a thermally enhanced 4mm × 5mm 20-lead QFN package and a thermally enhanced 24-lead TSSOP package. The buck-boost charger utilizes a proprietary switching algorithm which allows its output to be regulated above, below, or equal to the input voltage. The low $R_{DS(ON)}$, low gate charge synchronous switches provide high efficiency conversion to minimize the charging time of storage elements.

Charger Operation

The LTC3128 uses fixed frequency, average input current PWM control when charging the output capacitor(s). A proprietary switching algorithm allows the charger to switch between buck and boost modes without discontinuity in inductor current or loop characteristics. The switch topology for the buck-boost charger is shown in Figure 1. Two switches (D and E) connect SW2 to V_{OUT} to provide high efficiency over the entire output voltage range.

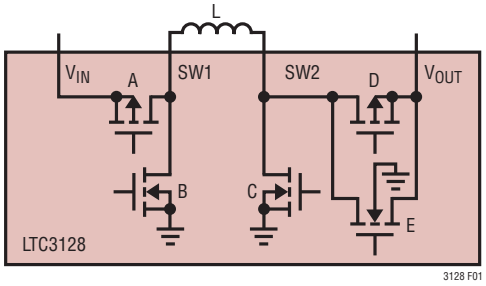


Figure 1. Buck-Boost Switch Topology

The LTC3128 uses a continuous switching algorithm where both SW1 and SW2 will switch regardless of the input or output. When the input voltage is significantly greater than the output voltage, the buck-boost converter operates in buck mode. Each cycle, switches B and C turn on for a minimum of 5% of the entire switching cycle. For the remainder of the switching cycle, switch D (switch D and E when V_{OUT} <1.5V typically) turns on continuously, switch C remains off, and switches A and B are pulse width modulated to produce the required duty cycle to support the output regulation voltage. As the input voltage decreases or as the output voltage increases, switch A remains on for a larger portion of the switching cycle. As the input voltage decreases further, switch pair CD is pulse width modulated to obtain the desired output voltage. At this point, the converter is operating solely in boost mode. When V_{OUT} is below 1.5V typical, switch D and E are modulated. This helps to improve efficiency at low V_{OUT} voltages.

This switching algorithm provides a seamless transition between operating modes and eliminates discontinuities in average inductor current, inductor current ripple, and loop transfer function throughout all operational modes. These advantages result in increased efficiency and stability in comparison to the traditional 4-switch buck-boost converter.

Error Amplifier And Compensation

The LTC3128 utilizes two control loops. The hysteretic voltage loop determines whether the output is in regulation or not, and commands the LTC3128 into a low quiescent current sleep state when V_{OUT} reaches its programmed level. The voltage loop is also equipped with a proportional gain control that reduces the charging current as V_{OUT} approaches regulation. This helps prevent chattering into and out of sleep because of the large charging currents and possibly high equivalent series resistance (ESR) capacitors. The current loop is internally compensated and forces the input current to the programmed input current limit. When the LTC3128 is not sleeping or balancing, it operates at a fixed 1.2MHz frequency.

Current Limit Operation

The LTC3128 has three current limit circuits. The primary current limit is an accurate average input current limit circuit that measures the input current drawn from the source by the LTC3128 and the other loads tied to the RSENS pin via an internal 50mΩ sense resistor. The LTC3128, when not sleeping, will always try to limit the input current passing through the sense resistor. Any current drawn externally from RSENS will result in a corresponding decrease in the charging current supplied by the LTC3128. If the load tied to RSENS draws more than the programmed amount, the LTC3128 will reduce the charging current to zero, although it cannot limit the current draw from external sources. The

OPERATION

input current limit is set by placing a resistor, R_{PROG}, from PROG to GND. This resistor and the C_{PROG} capacitor value can be calculated using the following formula:

$$R_{PROG}\ (k\Omega) = 11/I_{LIMIT}\ (A)$$

$$C_{PROG}\ (pF) \approx 1600/(R_{PROG}\ (k\Omega))$$

Where I_{LIMIT} is the average input current limit in amps.

A secondary linear current limit, limits the maximum average inductor current to 5.0A typically. If the peak inductor current reaches 6.5A (typical) switches A and C are immediately turned off, and switches B and D are turned on. The linear and peak current limits are fixed and therefore are not affected by the value of R_{PROG}.

Zero Current Comparator

The zero current comparator monitors the inductor current to the output and shuts off all power switches when this current reduces to approximately 30mA. This prevents the inductor current from reversing in polarity, improving efficiency at light loads.

Shutdown

Shutdown of the LTC3128 is accomplished by pulling the RUN pin below 0.3V and IC operation is enabled by pulling the RUN pin above 1.2V. Note that RUN can be driven above V_{IN} or V_{OUT}, as long as it is limited to less than the absolute maximum rating.

Thermal Shutdown

If the die temperature exceeds 165°C (typical) the LTC3128 will be disabled. All power devices will be turned off and both switch nodes will be pulled low. The LTC3128 will restart (if enabled) when the die temperature drops to approximately 155°C.

Thermal Regulator

To help prevent the part from going into thermal shut-down when charging very large capacitors at high current, the LTC3128 is equipped with a thermal regulator. If the die temperature exceeds 135°C (typical) the average current limit is lowered to help reduce the amount of power being dissipated in the package. The current limit will continue to be reduced to approximately 30% of the programmed limit just before thermal shutdown. The current limit will return to its full value when the die temperature drops below 135°C. See the PCB Layout Considerations section in the Applications Information portion of the data sheet for additional thermal considerations.

Undervoltage Lockout

If the input supply voltage drops below 1.60V (typical), the LTC3128 will be disabled and all power devices will be turned off. The LTC3128 will resume operation when V_{IN} rises above 1.73V.

Power Failure Indicator

The LTC3128 includes a power failure indicator comparator. Referring to the Block Diagram, the non-inverting input of the comparator is internally connected to a 0.58V reference and the inverting input is connected to the PFI pin. An external resistive divider can be placed from the supply being monitored to ground to program the threshold voltage. When the voltage at PFI drops below 0.58V, the open-drain N-channel MOSFET on $\overline{PFO}$ will turn on, pulling the pin low. The N-channel MOSFET is forced off when the LTC3128 is in shutdown. When PFI drops below 0.58V, a hysteresis current of 0.2µA will turn on, sinking current into the PFI pin providing hysteresis. Once the PFI pin rises above 0.58V plus the programmed hysteresis, the open-drain N-channel MOSFET on $\overline{PFO}$ will turn off. The power failure indicator voltage and hysteresis can be calculated as follows:

$$V_{PFI(FALLING)}\ (V) = 0.58 \bullet (1 + R4/R3)$$

$$V_{PFIHYST}\ (V) = R4 \bullet 0.2\mu A$$

Power-Good Indicator

The LTC3128 includes a power-good indicator comparator. The non-inverting input of the comparator is connected to the FB pin and the inverting input is internally connected to a 0.56V reference. When the voltage at FB drops below approximately 0.54V, the open-drain N-channel MOSFET on PGOOD will turn on, pulling the pin low. The N-channel MOSFET is forced off when the LTC3128 is in shutdown.

OPERATION

Maximum Capacitor Voltage Comparator

The LTC3128 monitors the voltage across each capacitor of the stacked output capacitors. If a capacitor exceeds the programmed maximum capacitor voltage, the LTC3128 will stop charging the output stack and begin balancing the voltage on the two capacitors. If the capacitors cannot be balanced and the fault condition still persists, charging will be halted until the output capacitors self discharge so that a fault condition no longer exists. This condition can exist if there is a shorted or damaged output capacitor. The maximum capacitor voltage is programmed by placing a single resistor from MAXV to GND. The R_{MAXV} resistor should be placed close to the MAXV pin to minimize the pin capacitance. The typical resistor value can be calculated using the following formula:

$$R_{MAXV}\ (k\Omega) = 50 \bullet V_{MAXV}\ (V)$$

Where V_{MAXV} is the maximum allowable voltage across a capacitor. With the calculated R_{MAXV} value, the observed V_{MAXV} can vary as much as ±6%. The maximum capacitor voltage comparator is not enabled until V_{OUT} is greater than approximately 1.5V. If the MAXV pin is tied to ground, both the maximum capacitor voltage comparator and the active charge balancer are disabled. The MAXV pin should be tied to ground if only a single output capacitor is being charged and no balancing is required. When using a single capacitor, the maximum capacitor voltage is programmed using the FB pin. The voltage loop will prevent overvoltaging of the output capacitor, and the MID pin should be grounded. Please refer to the Typical Applications section for an example.

Active Charge Balancer

The LTC3128 includes an active charge balancer for the stacked output capacitors. The balancer efficiently moves charge from the overcharged capacitor to the undercharged capacitor until the two capacitors are determined to be balanced. This helps to ensure the long term reliability of the capacitors by insuring one-half of the programmed output voltage is across each capacitor and eliminates the need for lossy balancing resistors or shunt regulators.

The active charge balancer is enabled once the voltage on the MID pin exceeds approximately 1.2V. The LTC3128 will try to balance the stack only if V_{OUT} has reached regulation, or if one of the capacitor voltages has exceeded the maximum programmed value. This ensures that the output stack is charged as quickly as possible while protecting each capacitor from being overcharged. The balancer is hysteretic and is enabled once the two capacitors are 60mV out of balance. Once the balancer has equalized the voltage across each capacitor, it is disabled.

The active charge balancer operates by using the inductor connected between SW1 and SW2 to efficiently move charge between the two output capacitors. The charge is moved through a switch that connects the MID pin to SW1 internally. Connecting the MID pin to SW1 allows the LTC3128 to either boost charge from the bottom capacitor to the top, or buck charge from the top capacitor by modulating switches C and D.

If V_{MID} is 60mV greater than $V_{OUT} – V_{MID}$ switches C and F are turned on until the inductor current reaches 400mA. Switch C is then turned off and switch D is turned on until the inductor current reaches 50mA. This switching cycle continues until $V_{MID} = V_{OUT} – V_{MID}$.

If $V_{OUT} – V_{MID}$ is 60mV greater than V_{MID}, switches D and F are turned on until the inductor current reaches –400mA. Switch D is then turned off and switch C is turned on until the inductor current reaches –50mA. The switching cycle continues until $V_{MID} = V_{OUT} – V_{MID}$.

The frequency that the balancer will operate at is dependent on the inductor value (L) and can be calculated by:

$$f_{balancer}\,(MHz) \approx \frac{V_{OUT}}{1.6 \bullet L\,(\mu H)}$$

APPLICATIONS INFORMATION

A typical LTC3128 application circuit is shown on the front page of this data sheet. The external component selection is determined by the desired output voltage, input current limit, maximum capacitor voltage, and V_{OUT} ripple requirements for each particular application. However, basic guidelines and considerations for the design process are provided in this section.

Output Voltage Programming

The output voltage is set by a resistive divider according to the formula:

$$V_{OUT}\,(V) = 0.58V \bullet (1 + R2/R1)$$

The external divider is connected to the output as shown in Figure 2. The LTC3128 buck-boost charger utilizes input current mode control, and the output divider resistance does not play a role in system stability. Large resistor values can be used to minimize output leakage. The programmed maximum capacitor voltage affects the maximum output voltage that can be programmed. This maximum programmed output voltage can be calculated by:

$$V_{OUT(MAX)} = 2 \bullet (V_{MAXV} - 440mV)\ (-40°C \text{ to } 125°C)$$

$$V_{OUT(MAX)} = 2 \bullet (V_{MAXV} - 385mV)\ (0°C \text{ to } 85°C)$$

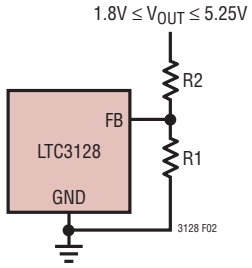


Figure 2. Setting the Buck-Boost Output Voltage

Inductor Selection

To achieve high efficiency, a low DCR inductor should be utilized for the buck-boost charger. The inductor must have a saturation rating greater than the worst case average inductor current plus half the ripple current. This is due to the fact that during start-up or high step down ratios, the inductor current will be at the linear current limit (4.0A minimum) even if the programmed input current is less. The peak-to-peak inductor current ripple for buck and boost mode can be calculated from the following formulas, where L is the inductance in micro Henries:

$$\Delta I_{L,P-P,BUCK}\,(A) = \frac{V_{OUT}\,(V_{IN} - V_{OUT})}{V_{IN} \bullet L \bullet 1.2}$$

$$\Delta I_{L,P-P,BOOST}\,(A) = \frac{V_{IN}\,(V_{OUT} - V_{IN})}{V_{OUT} \bullet L \bullet 1.2}$$

The 1.2MHz switching frequency allows the LTC3128 to utilize small surface mount inductors. Inductor values between 2.2µH and 4.7µH are recommended. These values provide low ripple in the inductor current, but will not adversely affect the stability of the LTC3128. An inductor value that is too small or large will limit the stable input voltage range for a given V_{OUT}.

High frequency ferrite core inductor materials reduce frequency dependent power losses compared to cheaper powdered iron types, improving efficiency. The inductor should have low DC resistance (approximately 20mΩ or less) to reduce the I^2R power losses, and must be able to support the peak inductor current without saturating. Molded chokes and chip inductors usually do not have enough core area to support the maximum peak inductor currents of up to 9.0A seen on the LTC3128. The inductor current can still reach currents greater than 5A even at low programmed input currents due to high voltage step-down ratios at start-up. See Table 1 and the reference schematics for suggested components and suppliers.

Input Capacitor Selection

The style and value of capacitors used with the LTC3128 determine input voltage ripple. It is required that a low equivalent series resistance (ESR) multilayer ceramic capacitor of at least 10µF be used to bypass the V_{IN}, RSENS and RSENP pins.

The value of the capacitor on V_{IN} directly controls the amount of input ripple for a given input current pulse, such as during a bucking switching cycle. Increasing the value of this capacitor will reduce the input ripple.

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Table 1: Recommended Inductors

VENDOR	VALUE (µH)	DCR (mΩ)	MAX DC CURRENT (A)	SIZE (mm) W × L × H
Coilcraft				
XAL5030-222ME	2.2	13.2	9.2	5.0 × 5.0 × 3.0
XAL5030-332ME	3.3	21.2	8.7	5.0 × 5.0 × 3.0
XAL6030-332ME	3.3	19.9	12.2	6.0 × 6.0 × 3.0
XAL6060-472ME	4.7	13.1	10.5	6.0 × 6.0 × 6.0
Coiltronics				
HC8-2R6-R	2.6	11.4	10.2	10.9 × 10.9 × 4.0
HC8-3R5-R	3.5	16.5	8.5	10.9 × 10.9 × 4.0
HC7-3R9-R	3.9	7.9	10.4	13.0 × 13.8 × 5.5
HC7-4R7-R	4.7	9	9.2	13.0 × 13.8 × 5.5
Sumida				
CDRH10D68RT125NP-2R2NC	2.2	7.1	10.5	10.2 × 10.2 × 6.8
CDRH10D38DHPNP-3R3PC	3.3	13.5	9.25	10.0 × 10.0 × 3.8
CDRH127/HPNP-4R7RC	4.7	18.8	10.8	12.5 × 12.5 × 8.0
TDK				
VLF12060T-2R7N100	2.7	5.3	10	11.7 × 12.0 × 6.0
VLF12060T-3R9N9R0	3.9	7	9	11.7 × 12.0 × 6.0
Würth Elektronik				
744311220	2.2	11.4	9	6.9 × 7.0 × 3.8
744325420	4.2	7.1	11	10.2 × 10.5 × 4.7

Multilayer ceramic chip capacitors (MLCC) typically have exceptional ESR performance. MLCCs combined with a tight board layout and an unbroken ground plane will yield very good performance and low EMI emissions. There are several types of ceramic capacitors available, each having considerably different characteristics. For example, X7R and X7S ceramic capacitors have the best voltage and temperature stability. X5R ceramic capacitors have higher packing density but poorer performance over their rated voltage and temperature ranges. Y5V ceramic capacitors are not recommended because of their extreme non-linear characteristic of capacitance versus voltage and poor temperature stability.

OUTPUT CAPACITOR SELECTION

The LTC3128 is designed to charge supercapacitors with a minimum total output capacitance value greater that 2mF. In general, lower capacitance capacitors have higher ESRs. To prevent modulation in and out of sleep due to the voltage step caused by capacitor ESR, the LTC3128 reduces charge current in the last 5% of the V_{OUT} charge cycle. At the end of the charging cycle immediately before sleep, the input current is reduced to 20% of the programmed value. Also of importance is to try and minimize the droop due to the ESR, and keep the droop less than 1% of the programmed output voltage. When the charging current is reduced to zero, the output voltage ESR component is eliminated. The maximum recommended ESR for the recommended 1% droop on V_{OUT} is calculated by:

$$(R_{ESR1}+R_{ESR2})(\Omega)\cong\frac{V_{OUT}{}^2}{(20\bullet V_{IN}\bullet I_{LIM}\bullet\eta)}$$

Where R_{ESR1}, R_{ESR2} are the ESR of each capacitor, V_{IN} is the input voltage to the charger, I_{LIM} is the programmed input current in amps, η is the fractional efficiency of the charger at 20% of the programmed input current, and V_{OUT} is the programmed output of the charger. If the ESR of the capacitors is larger than this calculated value, some chattering in and out of sleep at the end of charge may be observed. Figure 3 shows the voltage droop on V_{OUT} caused when charging stops.

The LTC3128 is stable with a total output capacitance value greater than 2mF, or 4mF for each stacked capacitor. Supercapacitors are much larger physically than ceramic or tantalum capacitors, and therefore usually cannot be placed close to the charger. To minimize layout contribution to capacitor ESR, the trace width connecting the capacitors to each other and the IC should be as large as possible. The MID pin trace is not as critical, as it only carries 200mA

APPLICATIONS INFORMATION

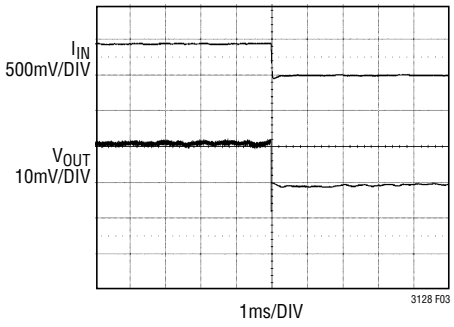

Figure 3. V_{OUT} Voltage Droop at End of Charging

of average current during balancing, but the V_{OUT} trace can carry more than 6A of current. It is recommended that local decoupling capacitors be placed from V_{OUT} to MID and from MID to ground, as close to the IC as possible. Multilayer ceramic capacitors are an excellent choice for output decoupling as they have extremely low ESR and are available in small footprints. While a 10µF decoupling capacitor is sufficient for most applications, larger values may be used without limitation.

If using a single output capacitor, where balancing is not required, the MAXV and the MID pin should be tied to ground, this prevents the LTC3128 from trying to balance. The hysteretic voltage loop of the LTC3128 will protect the output capacitor, by regulating it to the voltage programmed by the FB pin.

Pulsed Output Loads

A large output capacitance can be used to help with pulsed load applications by reducing the amount of current required by the LTC3128. The maximum load for a given pulsed load duty cycle and the minimum capacitance can be calculated by:

$$I_{LOAD(MAX)}(A) = \frac{V_{IN} \bullet I_{LIM} \bullet \eta}{D \bullet V_{OUT}}$$

$$C_{OUT(MIN)}(F) =$$

$$\left[I_{PULSE} - \left(\frac{V_{IN} \bullet I_{LIM} \bullet \eta}{V_{OUT}} - I_{STANDBY} \right) \right] \bullet \frac{D \bullet t}{V_{DROOP}}$$

Where $I_{STANDBY}$ is the continuous load current on the output in amps, I_{PULSE} is the pulsed load current in addition to $I_{STANDBY}$ in amps, I_{LIM} is the programmed average current in amps, η is the LTC3128 converter efficiency, D is the load pulse's duty cycle, and T is the period of the load pulse in seconds. When selecting output supercapacitors for large pulsed loads, the magnitude and duration of the pulsed current, together with the droop voltage specification, determine the choice of the output capacitor. Both the ESR and the charge stored in the capacitors each cycle contribute to the output voltage droop. The droop due to the pulsed load and ESR is calculated by:

$$V_{DROOP,LOAD}(V) =$$

$$\frac{\left[I_{PULSE} - \left(\frac{V_{IN} \bullet I_{LIM} \bullet \eta}{V_{OUT}} - I_{STANDBY} \right) \right] \bullet D \bullet T}{C_{OUT,TOTAL}(F)}$$

$$V_{DROOP,ESR}(V) =$$

$$\left[I_{PULSE} - \left(\frac{V_{IN} \bullet I_{LIM} \bullet \eta}{V_{OUT}} - I_{STANDBY} \right) \right]$$

$$\bullet \left(R_{ESR1} + R_{ESR2} \right)$$

Where $I_{STANDBY}$ is the continuous load current on the output in amps, I_{PULSE} is the pulsed load current in addition to $I_{STANDBY}$ in amps, I_{LIM} is the programmed average current in amps, D is the load pulse's duty cycle, and T is the period of the load pulse in seconds.

The total output voltage droop is given by:

$$V_{DROOP}(V) = V_{DROOP,LOAD} + V_{DROOP,ESR}$$

Low ESR and high capacitance are critical to maintaining low output droop. Table 2 and the Typical Applications schematics show supercapacitors that work well with the LTC3128.

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Table 2: Recommended Supercapacitors and Ultracapacitors

VENDOR	VALUE (F)	ESR (mΩ)	VOLTAGE (A)	TEMPERATURE RANGE (C)	SIZE (mm) W × L × H
Murata Electronics					
DMF3R5R5L334M3DTA0	0.33	60	4.2 (5.5 Peak)	–30 to 70	14.0 × 21.0 × 2.5
DMF3Z5R5H474M3DTA0	0.47	40	4.2 (5.5 Peak)	–30 to 70	14.0 × 21.0 × 3.2
Tecate					
TPL-10/10X30F	10	85	2.7	–40 to 65	10.0 × 10.0 × 30.0
TPL-25/16X26F	25	42	2.7	–40 to 65	16.0 × 16.0 × 26.0
TPL-100/22X45F	100	15	2.7	–40 to 65	22.0 × 22.0 × 45.0
TPLE-25/16X26F	25	42	2.3	–40 to 85	16.0 × 16.0 × 26.0
TPLE-100/22X45F	100	15	2.3	–40 to 85	22.0 × 22.0 × 45.0
TPLS-400/35X60F	400	12	2.7	–40 to 65	35.0 × 35.0 × 60.0
AVX					
BZ015A503Z_B	0.05	160	5.5	–20 to 70	28.0 × 17.0 × 4.1
BZ015A104Z_B	0.1	80	5.5	–20 to 70	28.0 × 17.0 × 6.7
CAP-XX					
HS206F	0.6	70	5.5	–40 to 85	39.0 × 17.0 × 2.5
HS230	1.2	50	5.5	–40 to 85	39.0 × 17.0 × 3.8
Cooper Bussmann					
A1635-2R5475-R	4.7	25	2.5	–25 to 70	16.0 × 16.0 × 35.0
M1325-2R5905-R	9	20	2.5	–40 to 60	13.0 × 13.0 × 26.0
HV1860-2R7107-R	100	10	2.7	–40 to 65	18.0 × 18.0 × 60.0
Illinois Capacitor					
506DER2R5SLZ	50	30	2.5	–40 to 70	18.0 × 18.0 × 60.0
357DER2R5SEZ	100	12	2.5	–40 to 70	35.0 × 35.0 × 60.0
Maxwell					
BCAP0005	5	170	2.7	–40 to 65	10.0 × 10.0 × 20.0
BCAP0100T01	100	15	2.7	–40 to 65	22.0 × 22.0 × 45.0
Taiyo Yuden					
PAS2026FR2R5504	0.5	55	2.5	–25 to 60	26.0 × 20.0 × 0.9
PAS0815LS2R5105	1	70	2.5	–25 to 70	8.0 × 8.0 × 15.0
LIC2540R3R8207	200	50	2.2 to 3.8	–25 to 70	25.0 × 25.0 × 40.0

Maximum Capacitor Voltage & Balancing

The service lifetime of a supercapacitor is determined by its rated voltage, rated temperature, rated lifetime, actual operating voltage, and operating temperature. To extend the life of a supercapacitor the operating voltage and temperature should be reduced from the maximum ratings. The websites for Illinois Capacitor[1] and Maxwell[2] provide the means to determine their capacitor lifetime.

Using the suggested derated voltage for each capacitor will improve lifetime. The LTC3128 will keep each capacitor voltage at $V_{OUT}/2$ once the output has reached regulation. To prevent an overvoltage on one of the output capacitors during charging, the maximum capacitor voltage comparators continuously monitor the output stack. If a capacitor exceeds the programmed maximum capacitor voltage, the LTC3128 immediately stops charging the stack. If a capacitor exceeds its maximum voltage and the MID pin is greater than 1.2V, the LTC3128 will balance the voltage of the capacitors, otherwise the part will halt charging until the maximum capacitor voltage violation clears, typically by an external load or leakage. The LTC3128 will start balancing the stacked output capacitors if the output is in regulation and the two capacitors are more than 60mV out of balance, or any time a maximum voltage event occurs.

How well the output capacitors are matched will determine the likelihood of triggering a maximum capacitor voltage fault during charging. The maximum capacitor voltage can only force the LTC3128 to stop charging and, depending on other conditions, attempt to balance the capacitors.

Note 1: http://www.illinoiscapacitor.com/tech-center/life-calculators.aspx

Note 2: http://www.maxwell.com/products/ultracapacitors/docs/APPLICATIONNOTE1012839_1.PDF

APPLICATIONS INFORMATION

The LTC3128 has minimal current draw from V_{OUT}, especially when the cells are in balance (typically < 2µA). Care should be taken to limit sources of current that may pull V_{OUT} above it's programmed regulation value, as there is no way for the LTC3128 to maintain regulation in this situation. If there is potential for external leakage to overvoltage the supercapacitors, measures should be taken to protect them.

PCB Layout Considerations

The LTC3128 switches large currents at high frequencies. Special care should be given to the PCB layout to ensure stable, noise free operation. Due to the high input and output power of the LTC3128 a four layer PCB with significant copper and ground planes is strongly recommended. Otherwise the thermal regulator may start to reduce the programmed input current at a lower ambient temperature, and may not be able to prevent the device from entering thermal shutdown.

The LTC3128 evaluation board shows a recommended layout and part placement. Figures 4 through 9 show the part placements and routing, a LTC3128 evaluation board is available on the Linear Technology website. The layout of the PCB and the amount of copper used directly effects the θ_{JA} of the LTC3128. The θ_{JA} of the LTC3128 on the evaluation board layout shown is 20°C/W. If thinner copper, less copper area, or fewer vias are used then this number will increase. The following items provide guidelines for layout of the LTC3128:

1. Use solid ground plane under the whole circuit (no other traces underneath)
2. Place all decoupling capacitors close to LTC3128 (that ensures low parasitic inductances)
3. Use 2 to 3 local ground vias next to the GND pad of each decoupling capacitor.
4. Place the maximum number of GND vias under the exposed pad of LTC3128 (for low thermal resistance)
5. Place a local GND via next to each component that is connected to ground.
6. Keep FB and MAXV nodes short (place the voltage divider resistors close to the pins)

The LTC3128 is equipped with a thermal regulator that is designed to help protect the LTC3128 from damage due to overheating. The thermal regulator will try to prevent the die temperature from exceeding 135°C by reducing the input current limit, but if it cannot, the LTC3128 will eventually enter thermal shutdown at 165°C. When the junction temperature of the LTC3128 drops back below 135°C the input current limit will no longer be affected.

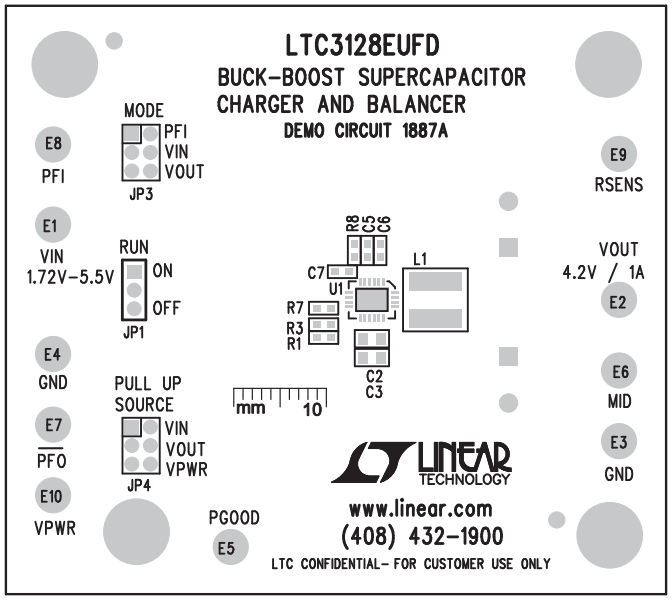


Figure 4. LTC3128 Evaluation Board Top Side Silkscreen

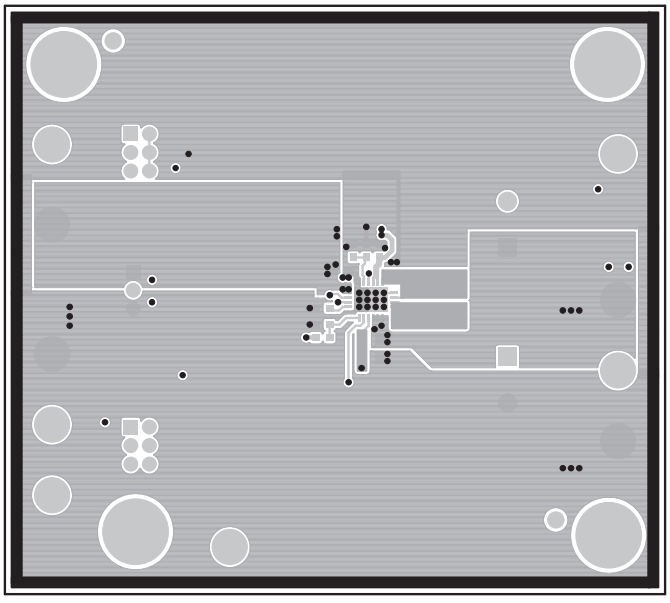


Figure 5. LTC3128 Evaluation Board Top Metal

APPLICATIONS INFORMATION

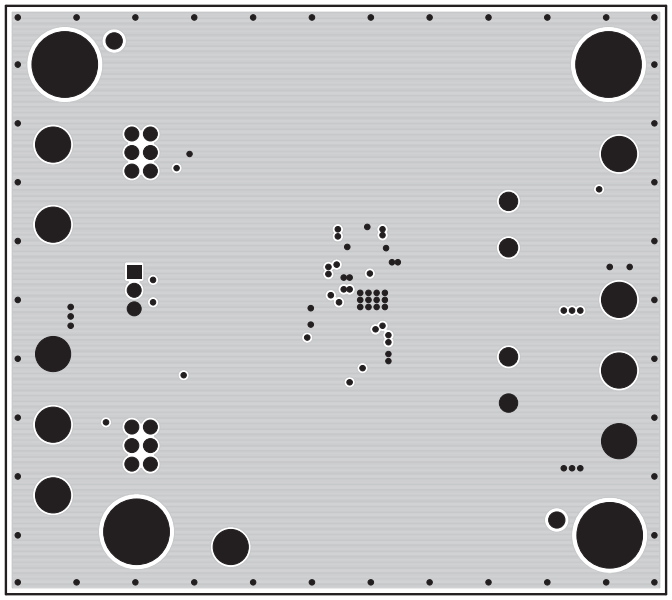


Figure 6. LTC3128 Evaluation Board Layer 2 Metal

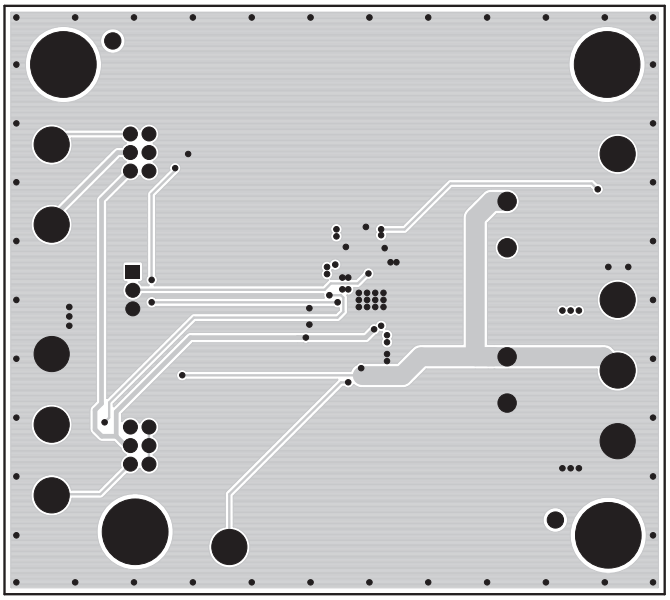


Figure 7. LTC3128 Evaluation Board Layer 3 Metal

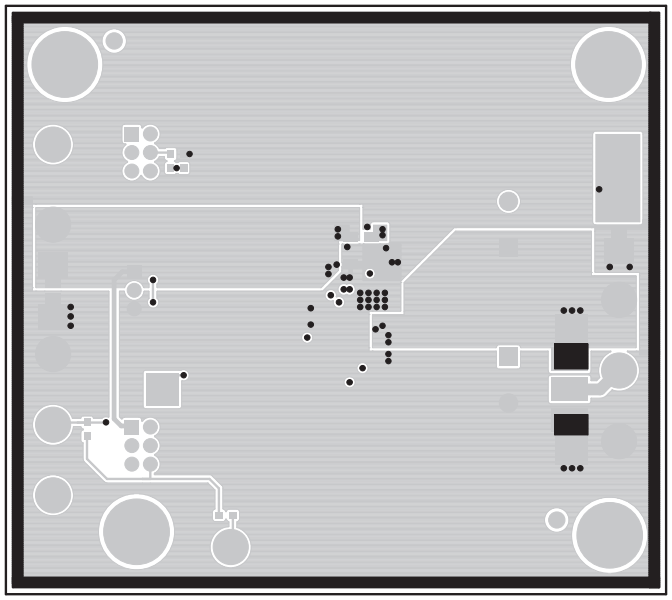


Figure 8. LTC3128 Evaluation Board Back Side Metal

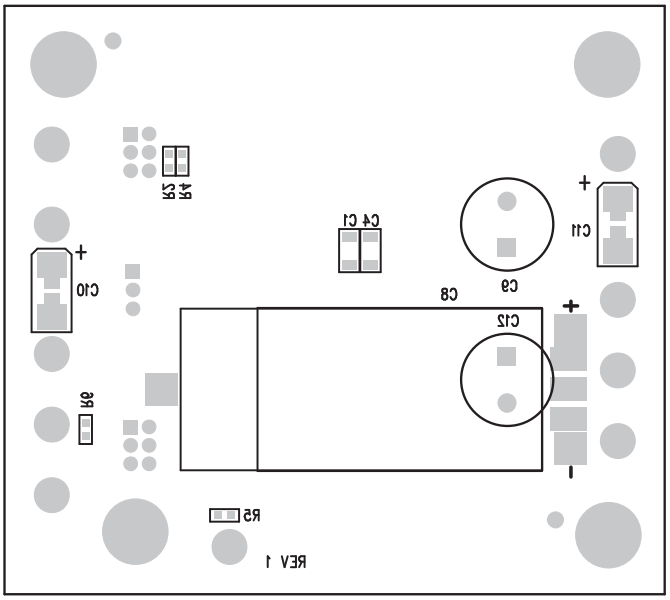
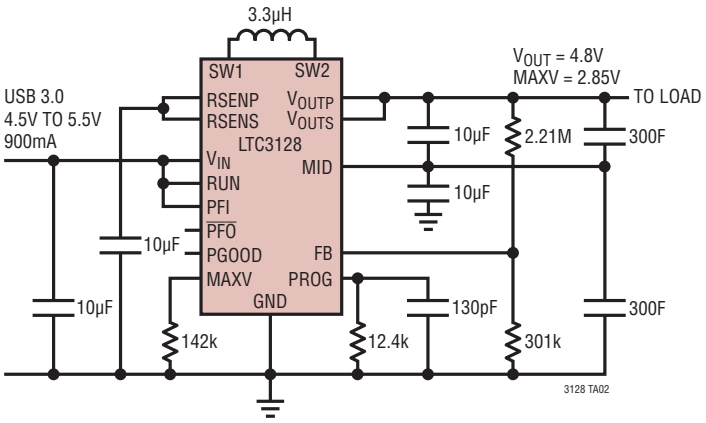
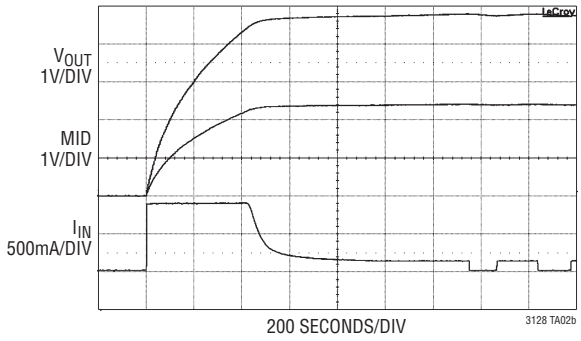


Figure 9. LTC3128 Evaluation Board Back Side Silkscreen

TYPICAL APPLICATIONS

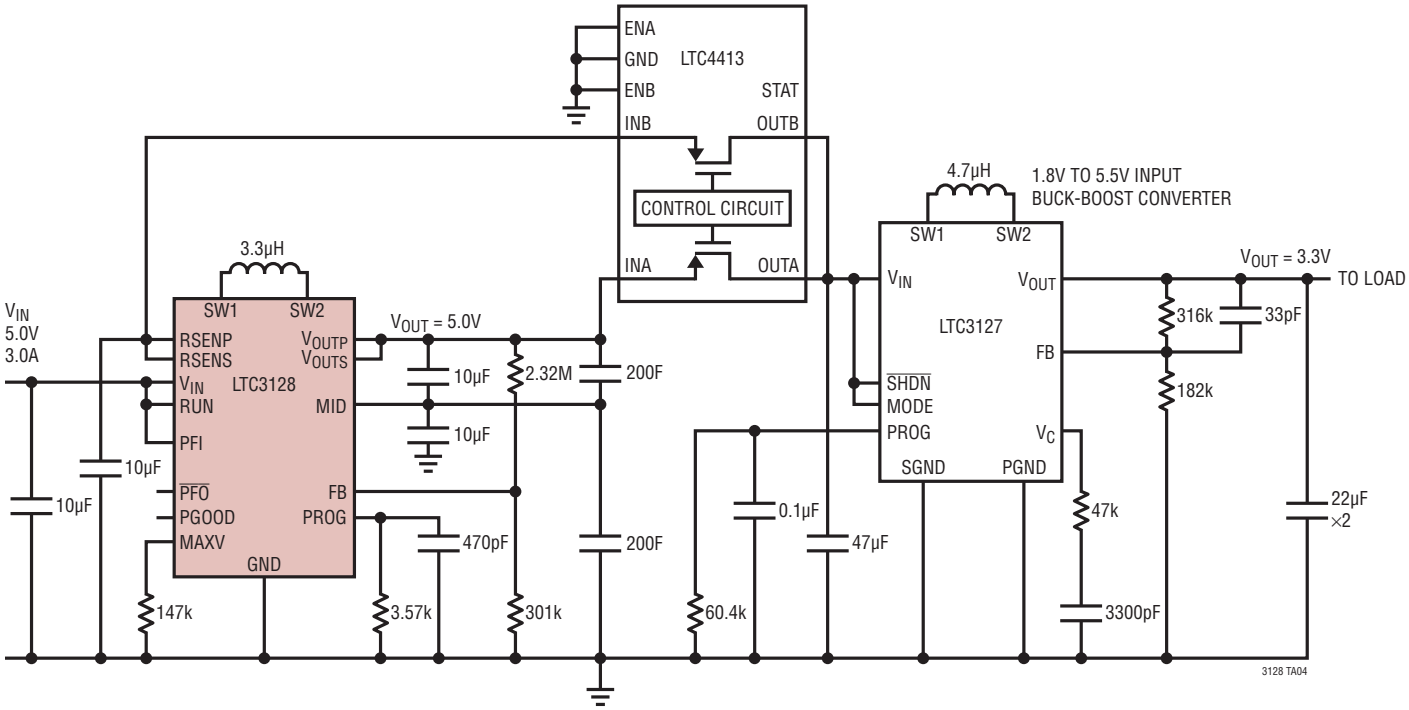
USB 3.0 (900mA Programmed Input Current) Powered, 4.8V Backup Supply



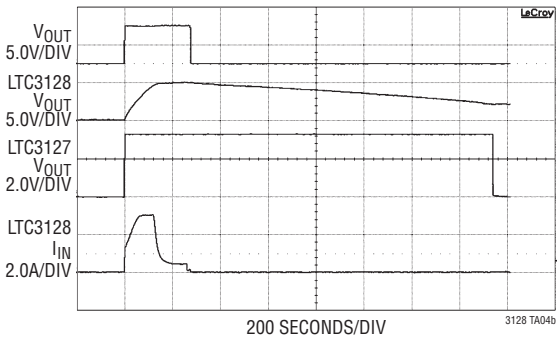


TYPICAL APPLICATIONS

5.0V to 3.3V Converter with Power Ride-Through



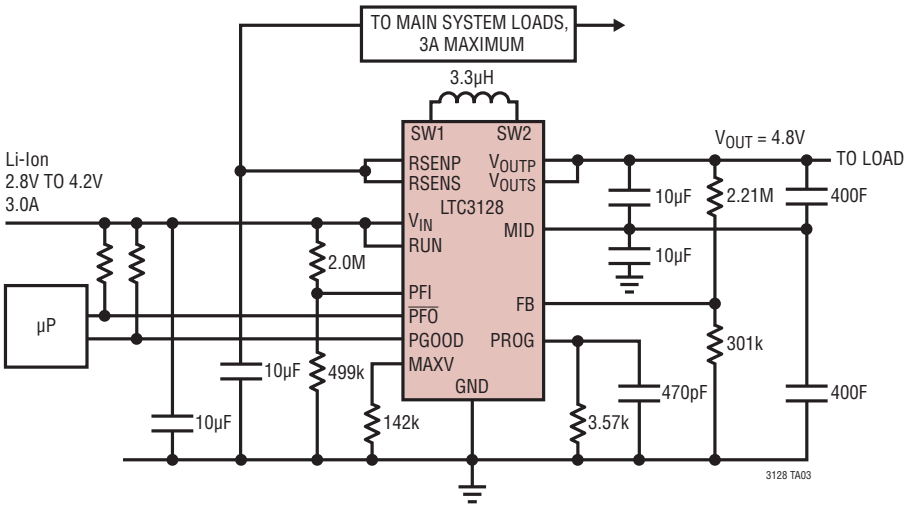
THIS CIRCUIT WILL PROVIDE THE 3.3V OUTPUT WHILE SUPERCAPACITORS ARE DISCHARGING FROM 5V DOWN TO 1.8V. THE LARGE DELTA FROM 5V DOWN TO 1.8V ALLOWS 87% OF STORED ENERGY IN THE SUPERCAPACITORS TO BE UTILIZED



200 SECONDS/DIV

TYPICAL APPLICATIONS

Supercapacitor Backup with Secondary Converters (3A Programmed Input Current)

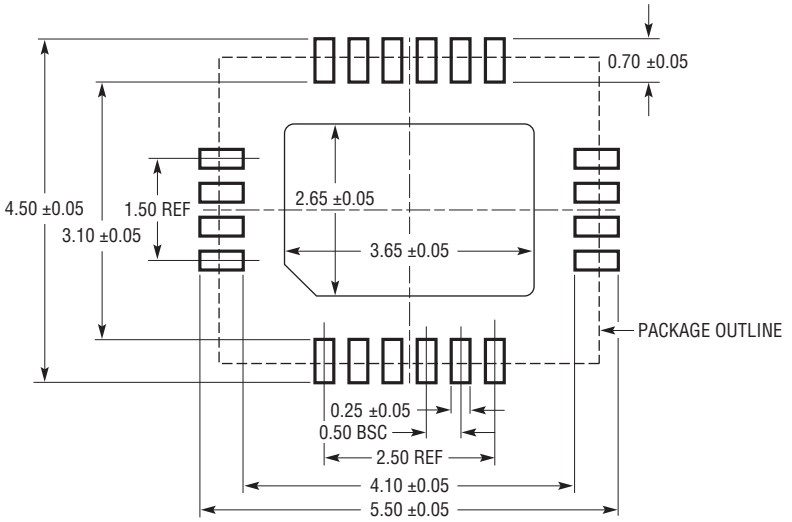


THIS SUPERCAPACITOR BACKUP CIRCUIT WILL DRAW ONLY THE CURRENT THAT IS LEFT OVER FROM THE 3A OF INPUT CURRENT CONSUMED BY MAIN LOADS IN THE SYSTEM

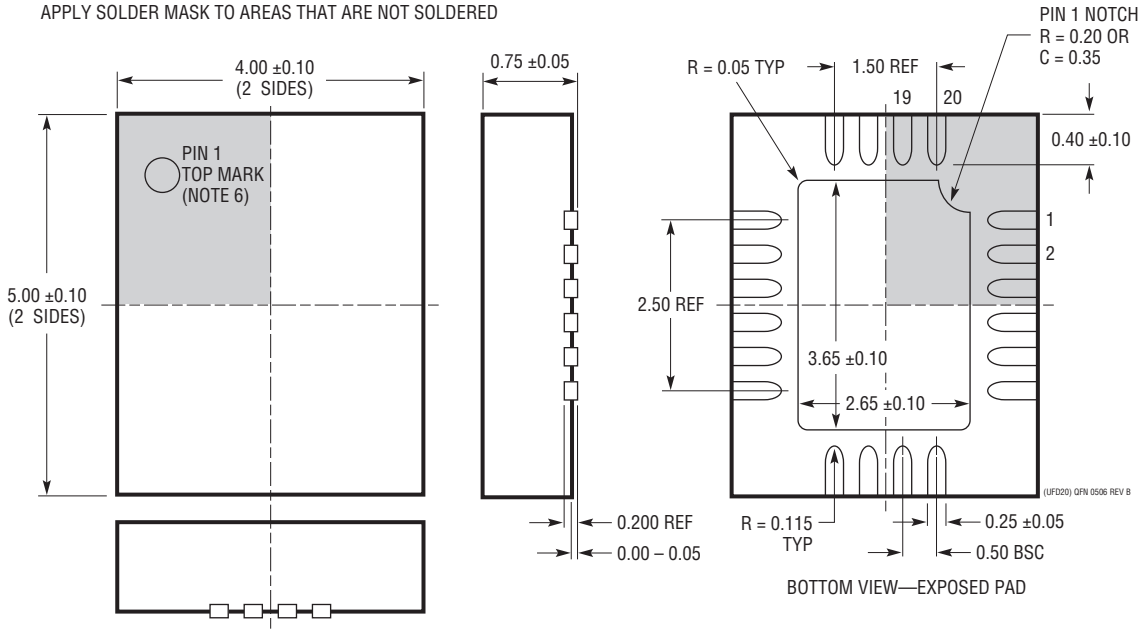
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UFD Package
20-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1711 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



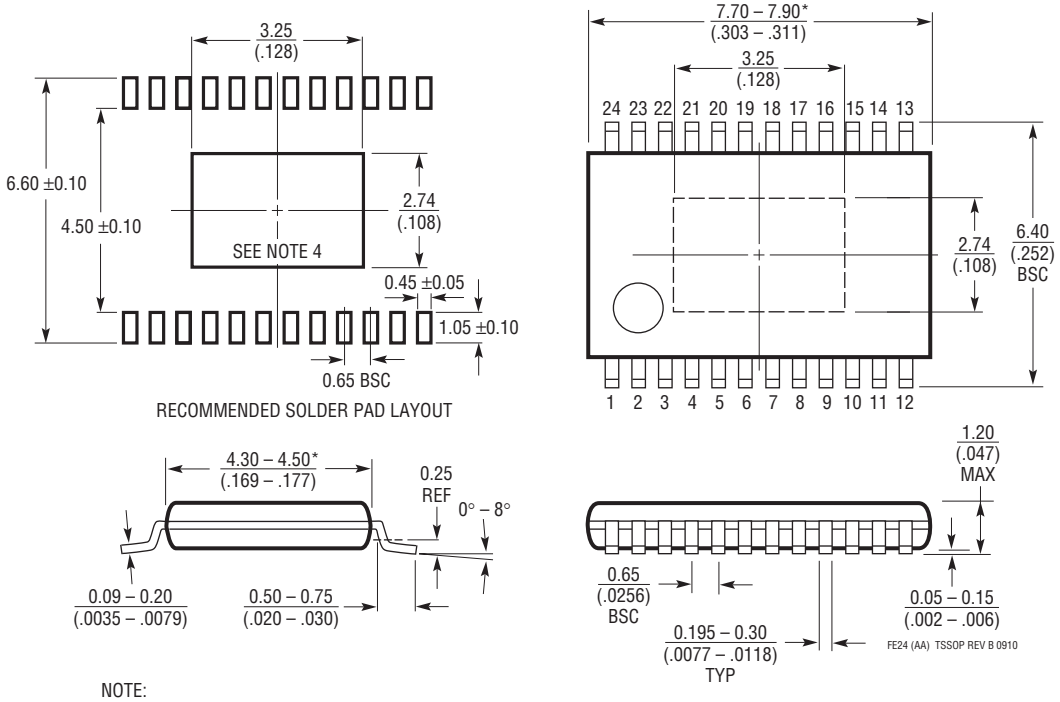
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
24-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1771 Rev B)
Exposed Pad Variation AA



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE