Micropower USB Power Manager with Li-Ion Charger, Always-On LDO and Buck Regulator

FEATURES

- **12µA Standby Mode Quiescent Current (All Outputs On)**
- **Seamless Transition Between Input Power Sources: Li-Ion/Polymer Battery and USB**
- **240mΩ Internal Ideal Diode Provides Low Loss PowerPath™**
- **High Efficiency 200mA Buck Regulator**
- **Always-On 150mA Low Dropout (LDO) Linear Regulator**
- **Pushbutton On/Off Control With System Reset**
- Full Featured Li-Ion/Polymer Battery Charger
- Programmable Charge Current With Thermal Limiting
- Instant-On Operation With Discharged Battery
- 3mm × 3mm × 0.75mm 20-Pin QFN Package

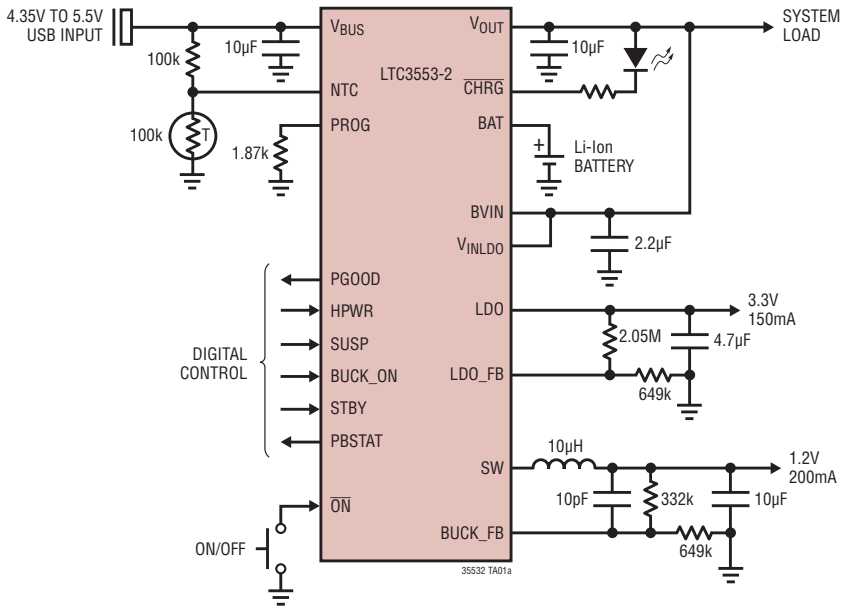
APPLICATIONS

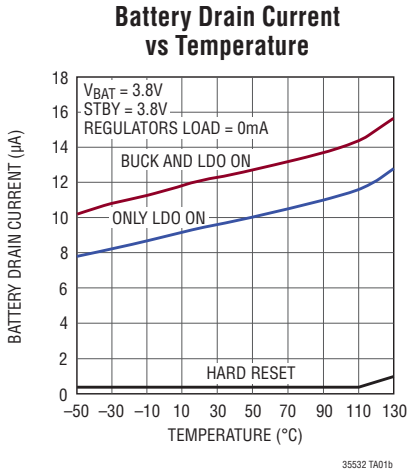
- USB-Based Handheld Products
- Portable Li-Ion/Polymer Based Electronic Devices
- Wearable Electronics
- Low Power Medical Devices

DESCRIPTION

The LTC®3553-2 is a micropower, highly integrated power management and battery charger IC for single-cell Li-Ion/Polymer battery applications. It includes a PowerPath manager with automatic load prioritization, a battery charger, an ideal diode and numerous internal protection features. Designed specifically for USB applications, the LTC3553-2 power manager automatically limits input current to a maximum of either 100mA or 500mA. Battery charge current is automatically reduced such that the sum of the load current and the charge current does not exceed the selected input current limit. The LTC3553-2 also includes a synchronous buck regulator, an always-on low dropout linear regulator (LDO), and a pushbutton controller. With all supplies enabled in standby mode, the quiescent current drawn from the battery is only 12µA. The LTC3553-2 is available in a 3mm × 3mm × 0.75mm 20-pin QFN package.

TYPICAL APPLICATION



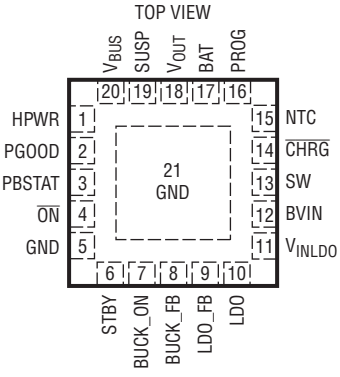


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

V_{BUS}, V_{OUT}
t < 1ms and Duty Cycle < 1% ..... –0.3V to 7V
Steady State..... –0.3V to 6V
BAT, NTC, $\overline{CHRG}$, SUSP, PBSTAT,
$\overline{ON}$, BUCK_FB, LDO_FB..... –0.3V to 6V
BUCK_ON, STBY, HPWR, PGOOD, BVIN, V_{INLDO},
LDO (Note 4).....–0.3V to V_{CC} + 0.3V
I_{BAT} 1A
I_{SW} (Continuous) 300mA
I_{LDO} (Continuous) 175mA
$I_{\overline{CHRG}}$, I_{PBSTAT}, I_{PGOOD} 75mA
Operating Temperature Range..... –40°C to 85°C
Junction Temperature ..... 110°C
Storage Temperature Range..... –65°C to 125°C

PIN CONFIGURATION



UD PACKAGE
20-LEAD (3mm × 3mm) PLASTIC QFN
T_{JMAX} = 110°C, θ_{JA} = 58.7°C/W
EXPOSED PAD (PIN 21) IS GND, AND MUST BE SOLDERED TO PCB GND

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3553EUD-2#PBF	LTC3553EUD-2#TRPBF	LGFJ	20-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

LTC3553 Options

PART NUMBER	LDO	PGOOD	HARD RESET TIME
LTC3553	ON/OFF Control	No	5 seconds
LTC3553-2	Always On	Yes	14 seconds

POWER MANAGER ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{BUS} = 5V, V_{BAT} = 3.8V, HPWR = SUSP = BUCK_ON = 0V, R_{PROG} = 1.87k, STBY = high, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
No-Load Quiescent Currents							
I_{BATQ}	Battery Drain Current (Note 5) Buck and LDO Shutdown, Hard Reset Buck and LDO Enabled LDO Enabled, Buck Shutdown	I_{OUT} = I_{SW} = I_{LDO} = 0 V_{BUS} = 0V, Hard Reset V_{BUS} = 0V, BUCK_ON = STBY = 3.8V V_{BUS} = 0V, BUCK_ON = 0V			0.2 8 8	2 16 16	 µA µA µA
I_{BATQC}	Battery Drain Current, V_{BUS} Available	V_{BAT} = V_{FLOAT}, Timer Timed Out			5	8	µA
I_{BUSQ}	V_{BUS} Input Current	100mA, 500mA Modes Charger On Timer Timed Out SUSP = 5V (Suspend Mode)			 300 150 15	 500 350 30	 µA µA µA

POWER MANAGER ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{BUS} = 5V, V_{BAT} = 3.8V, HPWR = SUSP = BUCK_ON = 0V, R_{PROG} = 1.87k, STBY = high, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{BVINQ}	BVIN Input Current Buck Shutdown Buck Enabled, Standby Mode Buck Enabled	V_{BUS} = 0V, V_{BVIN} = 3.8V, I_{SW} = 0 (Note 8) BUCK_ON = 0V BUCK_ON = STBY = 3.8V BUCK_ON = 3.8V, STBY = 0V			 0.01 1.5 22	 1 3 38	 µA µA µA
$I_{VINLDOQ}$	V_{INLDO} Input Current LDO Shutdown (Hard Reset) LDO Enabled	V_{BUS} = 0V, V_{INLDO} = 3.8V, I_{LDO} = 0 (Note 10)			 0.01 0.1	 1 1	 µA µA
Input Power Supply							
V_{BUS}	Input Supply Voltage			4.35		5.5	V
$I_{BUS(LIM)}$	Total Input Current	HPWR = 0V (100mA) HPWR = 5V (500mA)	● ●	80 400	90 450	100 500	mA mA
V_{UVLO}	V_{BUS} Undervoltage Lockout	Rising Threshold Falling Threshold		 3.5	3.8 3.6	3.9	V mV
V_{DUVLO}	V_{BUS} to BAT Differential Undervoltage Lockout	Rising Threshold Falling Threshold		 0	200 50	300	mV mV
R_{ON_ILIM}	Input Current Limit Power FET On-Resistance (Between V_{BUS} and V_{OUT})				350		mΩ
Battery Charger							
V_{FLOAT}	V_{BAT} Regulated Output Voltage	 0 ≤ T_A ≤ 85°C		4.179 4.165	4.2 4.2	4.221 4.235	V V
I_{CHG}	Constant-Current Mode Charge Current	R_{PROG} = 1.87k, 0 ≤ T_A ≤ 85°C		380	400	420	mA
V_{PROG} $V_{PROG,TRKL}$	PROG Pin Servo Voltage PROG Pin Servo Voltage in Trickle Charge	 V_{BAT} < V_{TRKL}			1 0.1		V V
h_{PROG}	Ratio of I_{BAT} to PROG Pin Current				750		mA/mA
I_{TRKL}	Trickle Charge Current	V_{BAT} < V_{TRKL}		30	40	50	mA
V_{TRKL}	Trickle Charge Threshold Voltage	V_{BAT} Rising V_{BAT} Falling		 2.6	2.9 2.75	3	V V
ΔV_{RECHRG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{FLOAT}		–75	–100	–125	mV
t_{TERM}	Safety Timer Termination Period	Timer Starts when V_{BAT} = V_{FLOAT} – 50mV		3.2	4	5	Hour
t_{BADBAT}	Bad Battery Termination Time	V_{BAT} < V_{TRKL}		0.4	0.5	0.63	Hour
$h_{C/10}$	End-of-Charge Indication Current Ratio	(Note 6)		0.085	0.1	0.115	mA/mA
R_{ON_CHG}	Battery Charger Power FET On-Resistance (Between V_{OUT} and BAT)	I_{BAT} = 200mA			220		mΩ
T_{LIM}	Junction Temperature in Constant Temperature Mode				110		°C
NTC							
V_{COLD}	Cold Temperature Fault Threshold Voltage	Rising NTC Voltage Hysteresis		75	76 1.3	77	$\%V_{BUS}$ $\%V_{BUS}$
V_{HOT}	Hot Temperature Fault Threshold Voltage	Falling NTC Voltage Hysteresis		34	35 1.3	36	$\%V_{BUS}$ $\%V_{BUS}$
V_{DIS}	NTC Disable Threshold Voltage	Falling NTC Voltage Hysteresis	●	1.2	1.7 50	2.2	$\%V_{BUS}$ mV
I_{NTC}	NTC Leakage Current	V_{NTC} = V_{BUS} = 5V		–50		50	nA

POWER MANAGER ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{BUS} = 5V, V_{BAT} = 3.8V, HPWR = SUSP = BUCK_ON = 0V, R_{PROG} = 1.87k, STBY = high, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Ideal Diode							
V_{FWD}	Forward Voltage Detection	(Note 12)			15		mV
$R_{DROPOUT}$	Diode On-Resistance, Dropout	I_{OUT} = 200mA, V_{BUS} = 0V			240		mΩ
I_{MAX}	Diode Current Limit	(Note 7)			1		A
Logic Inputs (HPWR, SUSP)							
V_{IL}	Input Low Voltage					0.4	V
V_{IH}	Input High Voltage			1.2			V
R_{PD}	Internal Pull-Down Resistance				4		MΩ
Logic Output ($\overline{CHRG}$)							
V_{OL}	Output Low Voltage	$I_{\overline{CHRG}}$ = 5mA			65	250	mV
$I_{\overline{CHRG}}$	Output Hi-Z Leakage Current	V_{BAT} = 4.5V, $V_{\overline{CHRG}}$ = 5V			0	1	µA

BUCK REGULATOR ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). BUCK_ON = V_{OUT} = BVIN = 3.8V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BVIN	Input Supply Voltage	(Note 9)	●	2.7		5.5	V
V_{OUT} UVLO	V_{OUT} Undervoltage Lockout	V_{OUT} Falling V_{OUT} Rising		2.5	2.6 2.8	 2.9	V V
f_{OSC}	Oscillator Frequency			0.955	1.125	1.295	MHz
I_{BUCK_FB}	BUCK_FB Input Current (Note 8)			–0.05		0.05	µA
R_{SW_PD}	SW Pull-Down in Shutdown	BUCK_ON = 0V			10		kΩ
Logic Input Pin (STBY)							
	Input High Voltage			1.2			V
	Input Low Voltage					0.4	V
	Input Current			–1		1	µA
Buck Regulator in Normal Operation (STBY Low)							
I_{LIM}	Peak PMOS Current Limit	BUCK_ON = 3.8V (Note 7)		300	500	650	mA
V_{BUCK_FB}	Regulated Feedback Voltage	BUCK_ON = 3.8V	●	780	800	820	mV
D_{MAX}	Max Duty Cycle			100			%
R_P	$R_{DS(ON)}$ of PMOS	I_{SW} = 100mA			1.1		Ω
R_N	$R_{DS(ON)}$ of NMOS	I_{SW} = –100mA			0.7		Ω
Buck Regulator in Standby Mode (STBY High)							
	Feedback Voltage Threshold	BUCK_ON = 3.8V, V_{BUCK_FB} Falling	●	770	800	820	mV
	Short-Circuit Current			30	50	100	mA
	Standby Mode Dropout Voltage	BUCK_ON = 2.9V, I_{SW} = 10mA, V_{BUCK_FB} = 0.76V, V_{OUT} = 2.9V, BVIN = 2.9V			50	100	mV

LDO REGULATOR ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{OUT} = V_{INLDO} = 3.8V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{INLDO}	Input Voltage Range	(Note 9)	●	1.65		5.5	V
V_{OUT} UVLO	V_{OUT} Undervoltage Lockout	V_{OUT} Falling V_{OUT} Rising		2.5	2.6 2.8	 2.9	V V
V_{LDO_FB}	Regulated Feedback Voltage	I_{LDO} = 1mA (Note 10)	●	780	800	820	mV
	V_{LDO_FB} Line Regulation	I_{LDO} = 1mA, V_{INLDO} = 1.65V to 5.5V (Note 10)			0.7		mV/V
	V_{LDO_FB} Load Regulation	I_{LDO} = 1mA to 150mA (Note 10)			0.025		mV/mA
I_{LDO_FB}	Feedback Pin Input Current			–50		50	nA
I_{LDO_OC}	Available Output Current		●	150			mA
I_{LDO_SC}	Short-Circuit Output Current	(Note 7)			300		mA
V_{DROP}	Dropout Voltage (Note 13)	I_{LDO} = 150mA, V_{INLDO} = 3.8V I_{LDO} = 150mA, V_{INLDO} = 2.5V I_{LDO} = 75mA, V_{INLDO} = 1.8V			160 220 180	260 350 280	mV mV mV
t_{LDO_SS}	Soft-Start Time				0.2		ms
R_{LDO_PD}	Output Pull-Down Resistance in Hard Reset				10		kΩ

PUSHBUTTON INTERFACE ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{BAT} = 3.8V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Pushbutton Pin ($\overline{ON}$)							
V_{CC_PB}	Pushbutton Operating Supply Range	(Notes 4 , 9)	●	2.7		5.5	V
$V_{\overline{ON}\_TH}$	$\overline{ON}$ Threshold Rising $\overline{ON}$ Threshold Falling			 0.4		1.2	V V
$I_{\overline{ON}}$	$\overline{ON}$ Input Current	$V_{\overline{ON}}$ = V_{CC} (Note 4)		–1		1	µA
R_{PB_PU}	Pushbutton Pull-Up Resistance	Pull-Up to V_{CC} (Note 4)		200	400	650	kΩ
Logic Input Pins (BUCK_ON)							
	Input High Voltage Input Low Voltage			1.2		 0.4	V V
	Input Current			–1		1	µA
Status Output Pins (PBSTAT, PGOOD)							
I_{PBSTAT}	PBSTAT Output High Leakage Current	V_{PBSTAT} = 3V		–1		1	µA
V_{PBSTAT}	PBSTAT Output Low Voltage	I_{PBSTAT} = 3mA			0.1	0.4	V
I_{PGOOD}	PGOOD Output High Leakage Current	V_{PGOOD} = 3V		–1		1	µA
V_{PGOOD}	PGOOD Output Low Voltage	I_{PGOOD} = 3mA			0.1	0.4	V
$V_{THPGOOD}$	PGOOD Threshold Voltage	(Note 14)			–8		%

PUSHBUTTON INTERFACE ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{BAT} = 3.8V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Pushbutton Timing Parameters (Note 11)							
$t_{\overline{ON}\_PBSTATL}$	Minimum $\overline{ON}$ Low Time to Cause PBSTAT Low	$\overline{ON}$ Brought Low During Power-On (PON) or Power-Up (PUP1, PUP2) States			50		ms
$t_{\overline{ON}\_PBSTATH}$	Delay from $\overline{ON}$ High to PBSTAT High	Power-On (PON) State, After PBSTAT Has Been Low for at Least t_{PBSTAT_PW}			900		µs
$t_{\overline{ON}\_PUP}$	Minimum $\overline{ON}$ Low Time to Enter Power-Up (PUP1 or PUP2) State	Starting in the Hard Reset (HR) or Power-Off (POFF) States			400		ms
$t_{\overline{ON}\_HR}$	Minimum $\overline{ON}$ Low Time to Hard Reset	$\overline{ON}$ Brought Low During the Power-On (PON) or Power-Up (PUP1, PUP2) States		11	14	17	s
t_{PBSTAT_PW}	PBSTAT Minimum Pulse Width	Power-On (PON) or Power-Up (PUP1, PUP2) States		40	50		ms
t_{EXTPWR}	Power-Up from USB Present to Power-Up (PUP1 or PUP2) State	Starting in the Hard Reset (HR) or Power-Off (POFF) States			100		ms
t_{PON_UP}	BUCK_ON High to Power-On State	Starting with BUCK_ON Low in the Power-Off (POFF) State			900		µs
$t_{PON\_DIS\_BUCK}$	BUCK_ON Low to Buck Disabled				1		µs
t_{PUP}	Power-Up (PUP1 or PUP2) State Duration				5		s
t_{PDN}	Power-Down (PDN1 or PDN2) State Duration				1		s
t_{PGOODH}	Regulators in Regulation to PGOOD High	All Enabled Regulators within PGOOD Threshold Voltage		1	1.8		ms
t_{PGOODL}	Regulator Out of Regulation to PGOOD Low	Any Enabled Regulator Below PGOOD Threshold Voltage			3		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3553-2E is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3553-2E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 110°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Note 4: V_{CC} is the greater of V_{BUS} or BAT.

Note 5: Total battery drain current represents the load a battery will see in application due to quiescent currents drawn by the BAT pin (I_{BATQ}) plus any current drawn from the V_{OUT} pin. In applications where the buck input (BVIN pin) and LDO input (V_{INLDO} pin) are connected to the PowerPath output (V_{OUT} pin), the quiescent currents on BVIN and V_{INLDO} must be added to I_{BATQ} to get the actual battery drain current that will be seen in application.

Note 6: $h_{C/10}$ is expressed as a fraction of programmed full charge current with specified PROG resistor.

Note 7: The current limit features of this part are intended to protect the IC from short term or intermittent fault conditions. Continuous operation above the absolute maximum specified pin current rating may result in device degradation or failure.

Note 8: BUCK_FB High, Not Switching

Note 9: V_{OUT} not in UVLO.

Note 10: Measured with the LDO operating in unity-gain, with its output and feedback pins tied together.

Note 11: See the Operation section of this data sheet for detailed explanation of the pushbutton state machine and the effects of each state on regulator and power manager operation.

Note 12: If $V_{BUS} < V_{UVLO}$ then V_{FWD} = 0 and the forward voltage across the ideal diode is equal to its current times $R_{DROPOUT}$.

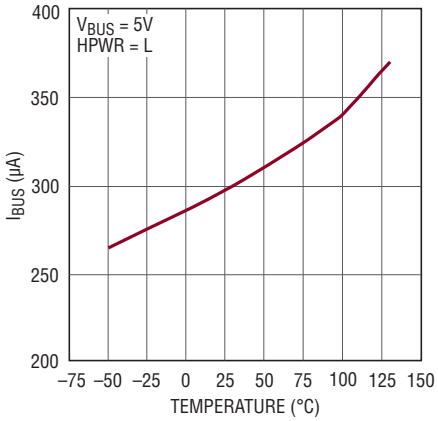
Note 13: Dropout voltage is the minimum input to output voltage differential needed for the LDO to maintain regulation at a specified output current. When the LDO is in dropout, its output voltage will be equal to: $V_{INLDO} – V_{DROP}$.

Note 14: PGOOD threshold is expressed as a percentage difference from the buck or LDO regulation voltage. The threshold is measured with the feedback pin voltage rising.

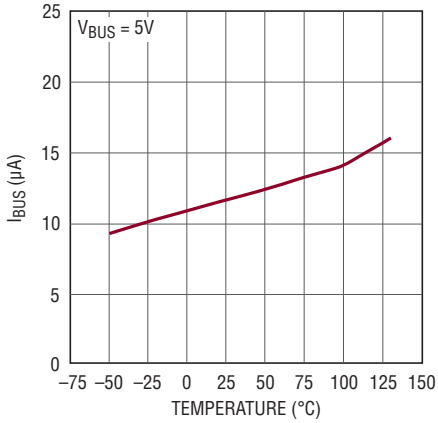
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise specified.

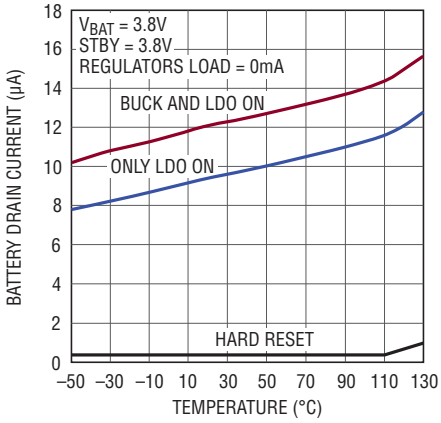
V_{BUS} Supply Current vs Temperature



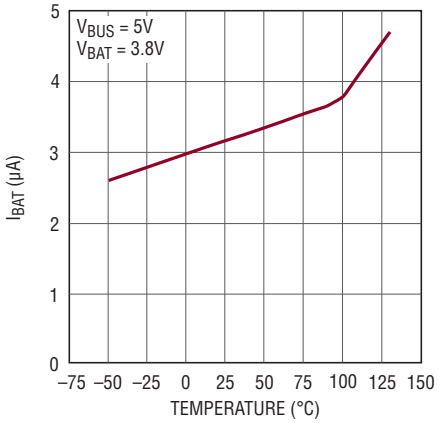
V_{BUS} Supply Current vs Temperature (Suspend Mode)



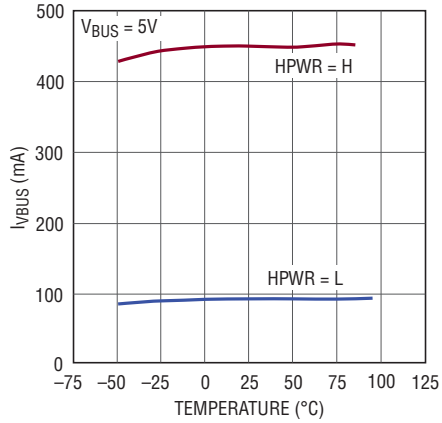
Battery Drain Current vs Temperature



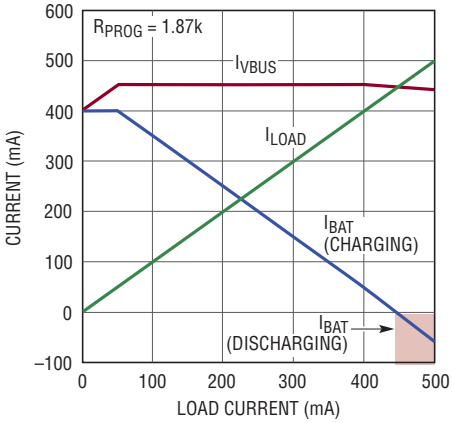
Battery Drain Current vs Temperature (Suspend Mode)



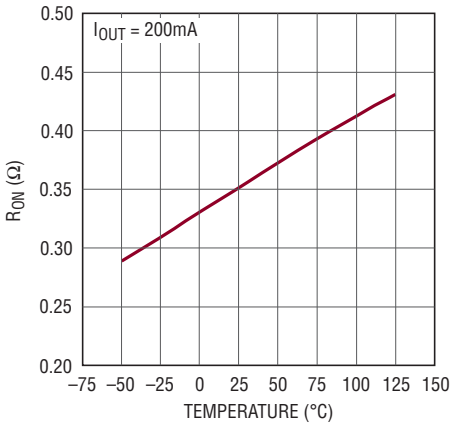
V_{BUS} Current Limit vs Temperature



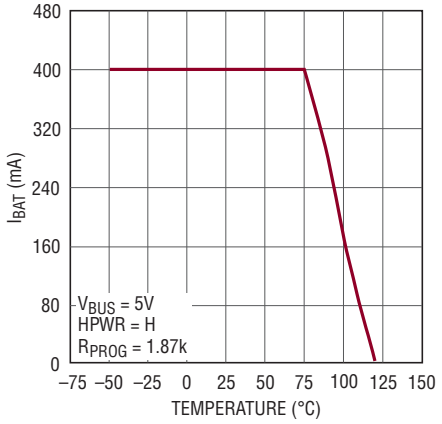
V_{BUS} and Battery Current vs Load Current



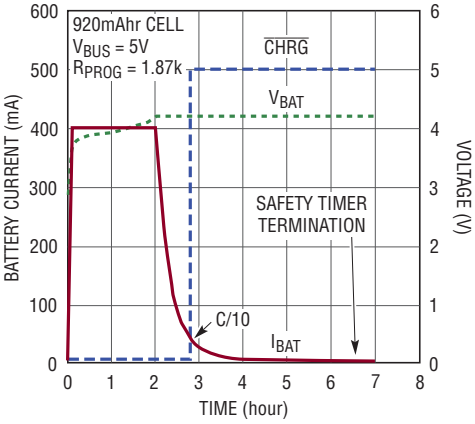
R_{ON} from V_{BUS} to V_{OUT} vs Temperature



Charge Current vs Temperature (Thermal Regulation)



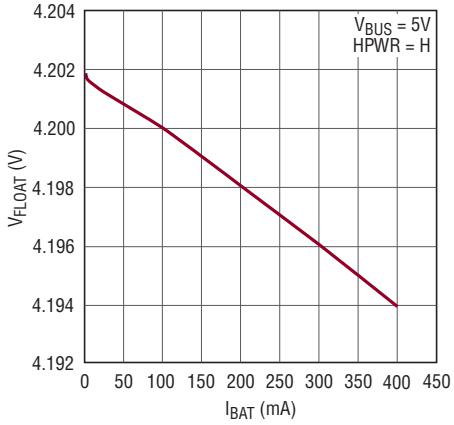
Battery Charge Current and Voltage vs Time



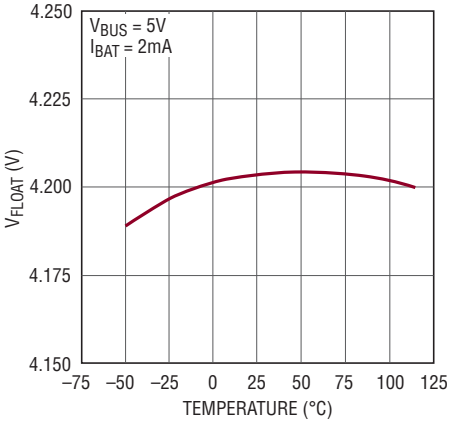
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise specified.

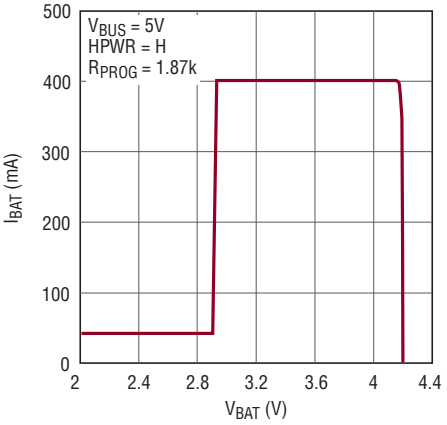
V_{FLOAT} Load Regulation



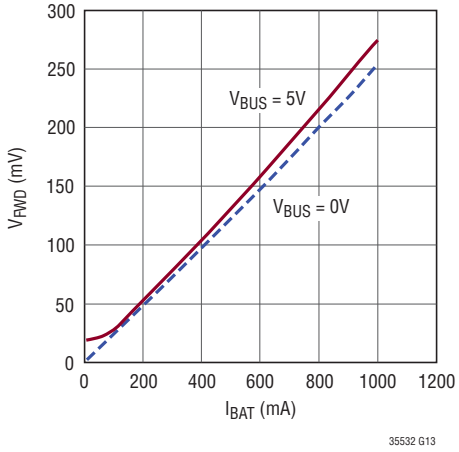
Battery Regulation (Float) Voltage vs Temperature



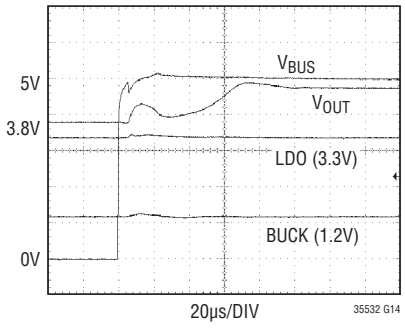
Battery Charge Current vs Battery Voltage



Forward Voltage vs Ideal Diode Current

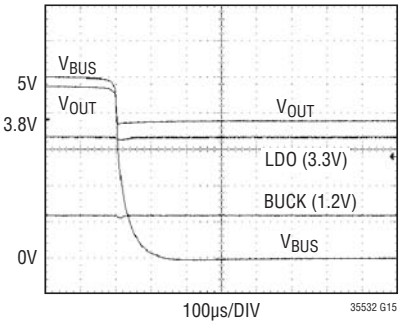


V_{BUS} Connect Waveform



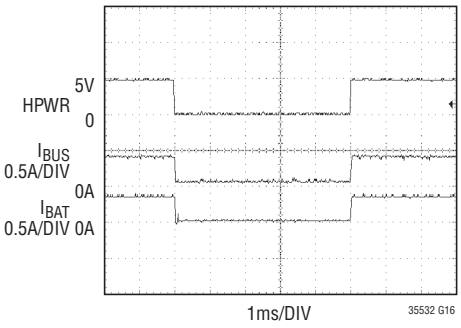
V_{BAT} = 3.8V
I_{LDO} = 100mA
I_{BUCK} = 100mA
HPWR = HIGH
SUSP = LOW
STBY = LOW

V_{BUS} Disconnect Waveform



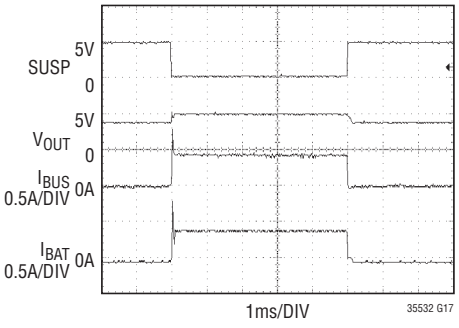
V_{BAT} = 3.8V
I_{LDO} = 100mA
I_{BUCK} = 100mA
HPWR = HIGH
SUSP = LOW
STBY = LOW

Switching from 100mA Mode to 500mA Mode



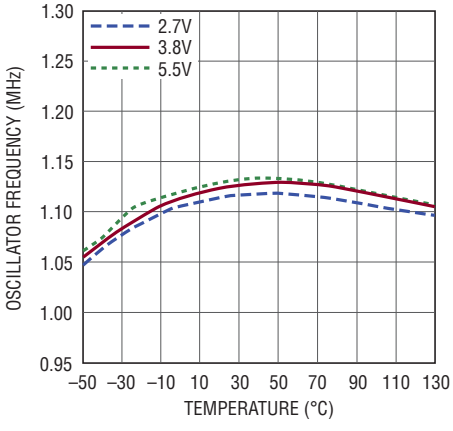
V_{BAT} = 3.75V
I_{OUT} = 50mA
R_{PROG} = 2k
SUSP = LOW

Switching from Suspend Mode to 500mA Mode



V_{BAT} = 3.75V
I_{OUT} = 50mA
R_{PROG} = 2k
HPWR = HIGH

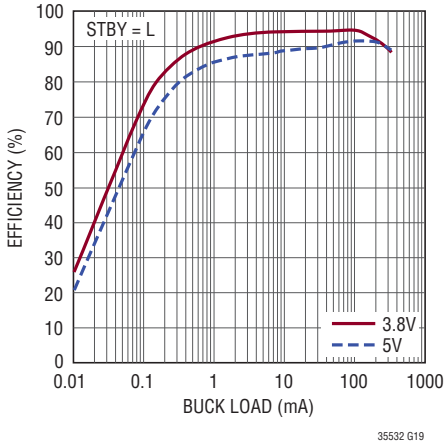
Oscillator Frequency vs Temperature



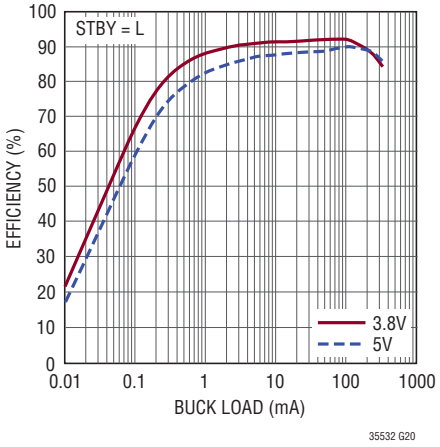
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise specified.

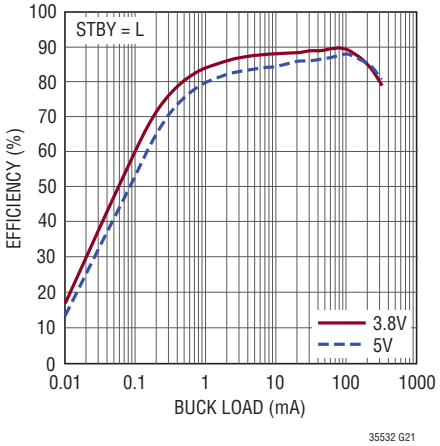
Buck Regulator 3.3V Output Efficiency vs Load



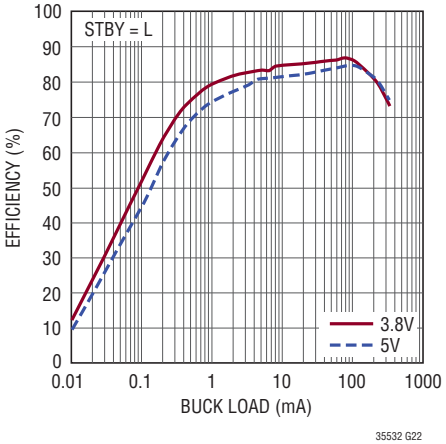
Buck Switching Regulator 2.5V Output Efficiency vs Load



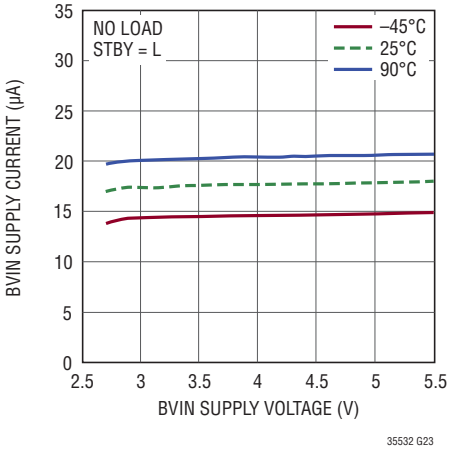
Buck Switching Regulator 1.8V Output Efficiency vs Load



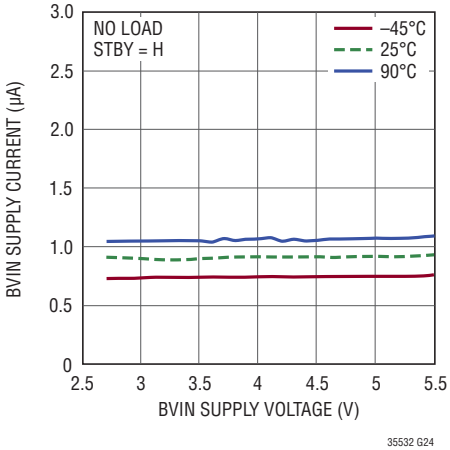
Buck Regulator 1.2V Output Efficiency vs I_{LOAD}



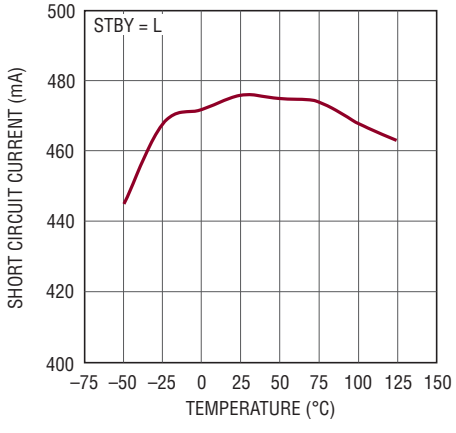
Buck Regulator Burst Mode® Operation BVIN Supply Current



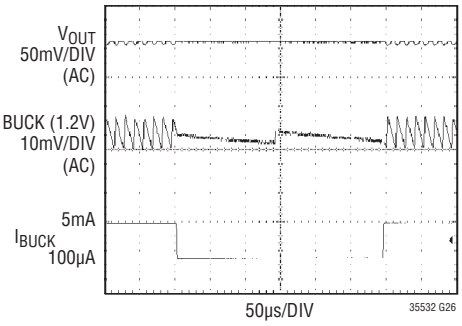
Buck Regulator Standby Mode BVIN Supply Current



Buck Regulator Short-Circuit Current vs Temperature

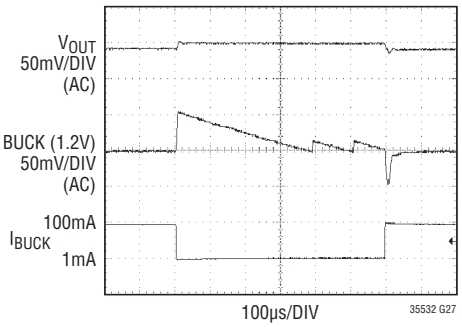


Buck Regulator Output Transient (STBY = High)



V_{BUS} = 0V
V_{BAT} = 3.8V
STBY = HIGH

Buck Regulator Output Transient (STBY = Low)

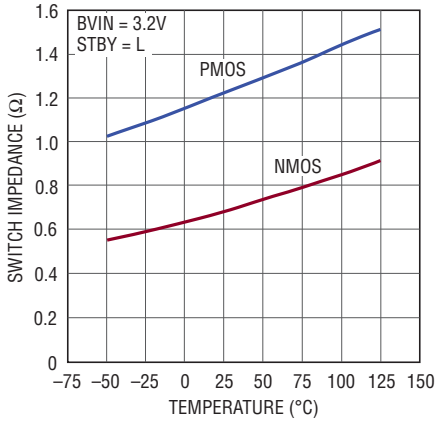


V_{BUS} = 0V
V_{BAT} = 3.8V
STBY = LOW

TYPICAL PERFORMANCE CHARACTERISTICS

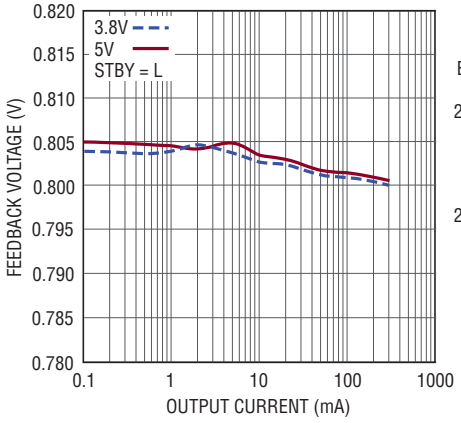
T_A = 25°C, unless otherwise specified.

Buck Regulator Switch Impedance vs Temperature



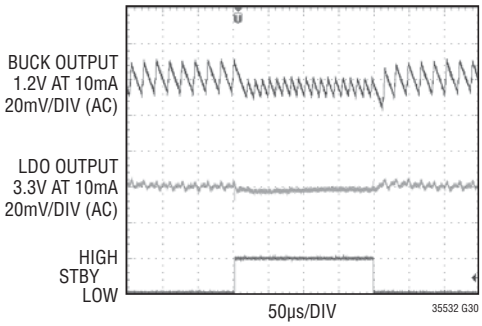
35532 G28

Buck Regulator Feedback Voltage vs Output Current



35532 G29

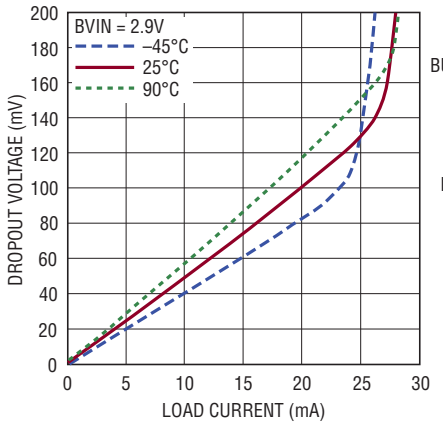
Regulator Output Transient During STBY Transition



35532 G30

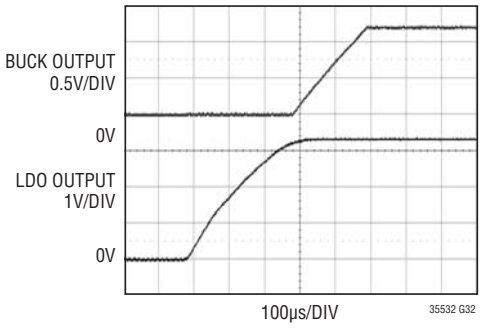
V_{BUS} = 0V
V_{BAT} = 3.8V

Buck Regulator Dropout Voltage in Standby Mode vs Load Current



35532 G31

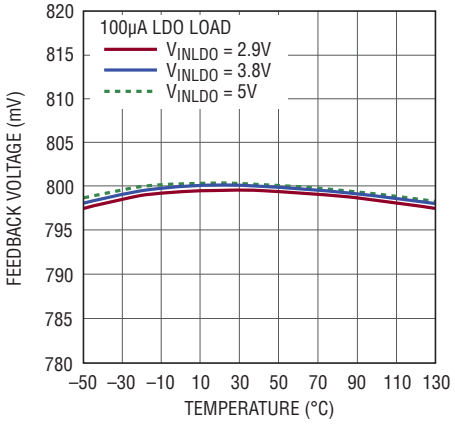
Power-Up Sequencing from Hard Reset



35532 G32

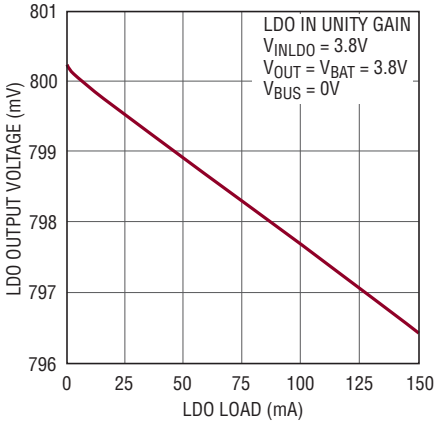
FRONT PAGE APPLICATION CIRCUIT

Regulated LDO Feedback Voltage vs Temperature



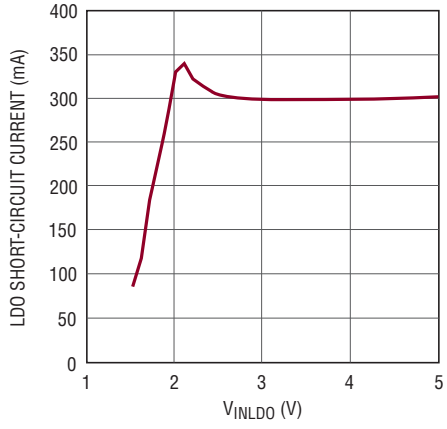
35532 G33

LDO Load Regulation



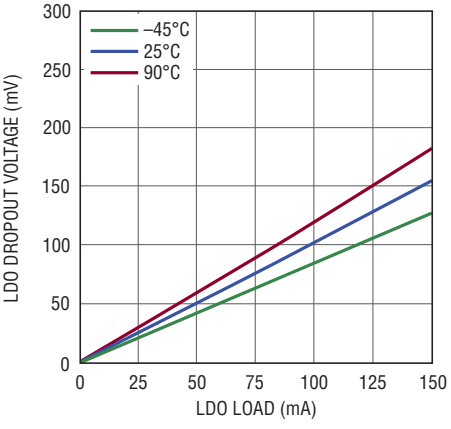
35532 G34

LDO Short-Circuit Current



35532 G35

LDO Dropout Voltage at V_{INLDO} = 3.8V

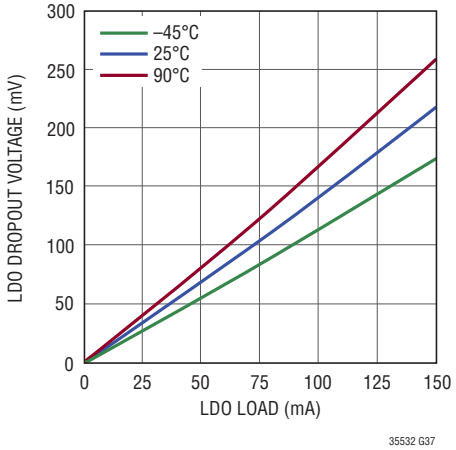


35532 G36

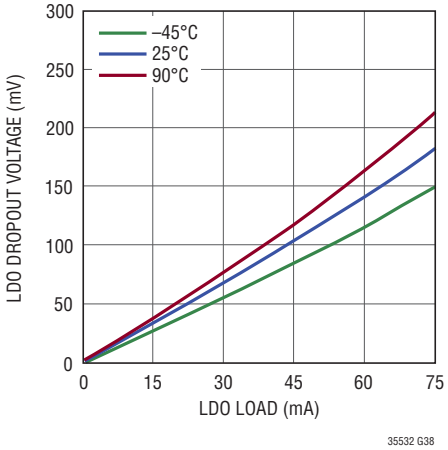
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise specified.

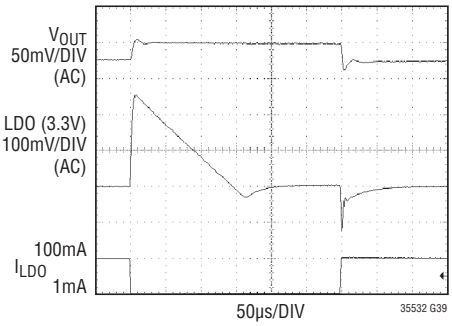
LDO Dropout Voltage at V_{INLDO} = 2.5V



LDO Dropout Voltage at V_{INLDO} = 1.8V



LDO Output Transient



V_{BUS} = 0V
V_{BAT} = 3.8V

PIN FUNCTIONS

HPWR (Pin 1): High Power Logic Input. When this pin is low the input current limit is set to 100mA and when this pin is driven high it is set to 500mA. The SUSP pin needs to be low for the input current limit circuit to be enabled. This pin has a conditional internal pull-down resistor when power is applied to the V_{BUS} pin.

PGOOD (Pin 2): Power Good. This open-drain output indicates that all enabled regulators have been in regulation for at least 1.8ms.

PBSTAT (Pin 3): Pushbutton Status. This open-drain output is a debounced and buffered version of the $\overline{ON}$ pushbutton input. It may be used to interrupt a microprocessor.

$\overline{ON}$ (Pin 4): Pushbutton Input. Weak internal pull-up forces a high state if $\overline{ON}$ is left floating. A normally open pushbutton is connected from $\overline{ON}$ to ground to force a low state on this pin.

GND (Pin 5, Exposed Pad Pin 21): Ground. The exposed package pad is ground and must be soldered to the PC board for proper functionality and for maximum heat transfer.

STBY (Pin 6): Standby Mode. When this pin is driven high, the buck regulator quiescent current is reduced to very low levels, while still maintaining output voltage regulation. In this mode, the buck regulator is limited to 10mA maximum load current. This pin must be driven to a valid logic level. Do not float this pin.

BUCK_ON (Pin 7): Logic Input Enables the Buck Regulator. This pin must be driven to a valid logic level. Do not float this pin.

BUCK_FB (Pin 8): Feedback Input for the Buck Regulator. This pin servos to a fixed voltage of 0.8V when the control loop is complete.

LDO_FB (Pin 9): Feedback Input for the Low Dropout Regulator. This pin servos to a fixed voltage of 0.8V when the control loop is complete.

LDO (Pin 10): Low Dropout (LDO) Linear Regulator Output. This pin should be bypassed with a low impedance multilayer ceramic capacitor.

V_{INLDO} (Pin 11): Power Input Pin for the LDO Regulator. This pin is to be connected to V_{OUT} or any supply voltage below V_{OUT}, such as the buck regulator output. This pin should be bypassed with a low impedance multilayer ceramic capacitor.

BVIN (Pin 12): Power Input for the Buck Regulator. It is recommended that this pin be connected to the V_{OUT} pin. It should be bypassed with a low impedance multilayer ceramic capacitor.

SW (Pin 13): Power Transmission (Switch) Pin for the Buck Regulator.

$\overline{CHRG}$ (Pin 14): Open-Drain Charge Status Output. This pin indicates the status of the battery charger. It is internally pulled low while charging. Once the battery charge current reduces to less than one-tenth of the programmed charge current, this pin goes into a high impedance state. An external pull-up resistor and/or LED is required to provide indication.

NTC (Pin 15): The NTC pin connects to a battery's thermistor to determine if the battery is too hot or too cold to charge. If the battery's temperature is out of range, charging is paused until it drops back into range. A low drift bias resistor is required from V_{BUS} to NTC and a thermistor is required from NTC to ground. If the NTC function is not desired, the NTC pin should be grounded.

PROG (Pin 16): Charge Current Program and Charge Current Monitor Pin. Connecting a resistor from PROG to ground programs the charge current as given by:

$$I_{CHG}\,(A) = \frac{750V}{R_{PROG}}$$

If sufficient input power is available in constant-current mode, this pin servos to 1V. The voltage on this pin always represents the actual charge current.

BAT (Pin 17): Single-Cell Li-Ion Battery Pin. Depending on available power and load, a Li-Ion battery on BAT will either deliver system power to V_{OUT} through the ideal diode or be charged from the battery charger.

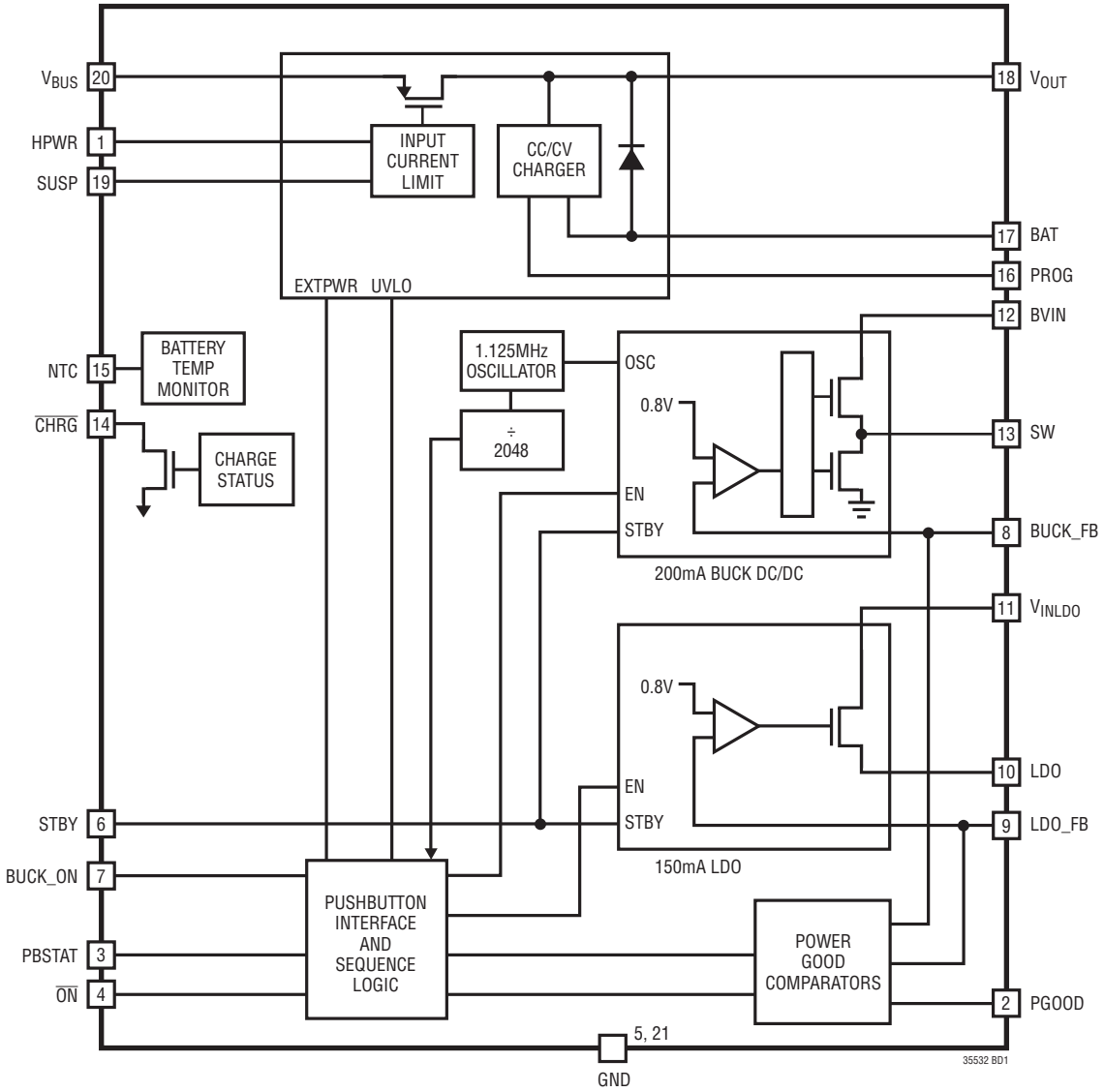
PIN FUNCTIONS

V_{OUT} (Pin 18): Output Voltage of the PowerPath Controller and Input Voltage of the Battery Charger. The majority of the portable products should be powered from V_{OUT}. The LTC3553-2 will partition the available power between the external load on V_{OUT} and the internal battery charger. Priority is given to the external load and any extra power is used to charge the battery. An ideal diode from BAT to V_{OUT} ensures that V_{OUT} is powered even if the load exceeds the allotted input current from V_{BUS} or if the V_{BUS} power source is removed. V_{OUT} should be bypassed with a low impedance multilayer ceramic capacitor.

SUSP (Pin 19): Suspend Mode Logic Input. If this pin is driven high the input current limit path is disabled. In this state the circuit draws negligible power from the V_{BUS} pin. Any load at the V_{OUT} pin is provided by the battery through the internal ideal diode. When this input is grounded, the input current limit will be set to desired value as determined by the state of the HPWR pin. This pin has a conditional internal pull-down resistor when power is applied to the V_{BUS} pin.

V_{BUS} (Pin 20): USB Input Voltage. V_{BUS} will usually be connected to the USB port of a computer or a DC output wall adapter. V_{BUS} should be bypassed with a low impedance multilayer ceramic capacitor.

BLOCK DIAGRAM



OPERATION

Introduction

The LTC3553-2 is a highly integrated power management IC that includes the following features:

PowerPath controller

Battery charger

Ideal diode

Pushbutton controller

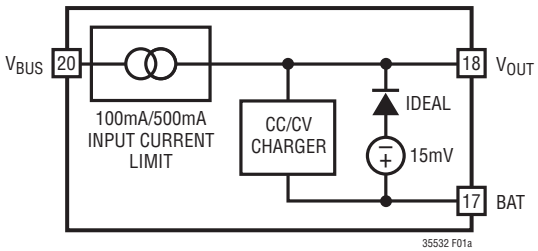
200mA buck regulator

Always-on 150mA low dropout (LDO) linear regulator

Designed specifically for USB applications, the PowerPath controller incorporates a precision input current limit which communicates with the battery charger to ensure that input current never violates the USB specifications. The ideal diode from BAT to V_{OUT} guarantees that ample power is always available to V_{OUT} even if there is insufficient or absent power at V_{BUS}. The LTC3553-2 also includes a pushbutton input to control the two regulators and system reset. The constant-frequency current mode step-down switching regulator provides 200mA and supports 100% duty cycle operation as well as Burst Mode operation for high efficiency at light load. No external compensation components are required for the switching regulator. The LDO can deliver up to 150mA, and is stable with a ceramic output capacitor of at least 1µF. For application flexibility, the LDO's power input pin, V_{INLDO}, is independent of the buck's BVIN pin.

Either regulator can be programmed for a minimum output voltage of 0.8V and can be used to power a microcontroller core, microcontroller I/O, memory or other logic circuitry. The buck regulator operates at 1.125MHz.

Simplified PowerPath Block Diagram



The buck regulator includes a low power standby mode which can be used to power essential keep-alive circuitry while draining ultralow current from the battery for extended battery life.

USB PowerPath Controller

The input current limit and charger control circuits of the LTC3553-2 are designed to limit input current as well as control battery charge current as a function of I_{VOUT}. V_{OUT} drives the combination of the external load, the buck and LDO regulators and the battery charger.

If the combined load does not exceed the programmed input current limit, V_{OUT} will be connected to V_{BUS} through an internal 350mΩ P-channel MOSFET. If the combined load at V_{OUT} exceeds the programmed input current limit, the battery charger will reduce its charge current by the amount necessary to enable the external load to be satisfied while maintaining the programmed input current. Even if the battery charge current is set to exceed the allowable USB current, the average input current USB specification will not be violated. Furthermore, load current at V_{OUT} will always be prioritized and only excess available current will be used to charge the battery.

The input current limit is programmed by the HPWR and SUSP pins. If SUSP pin set high, the input current limit is disabled. If SUSP pin is low, the input current limit is enabled. HPWR pin selects between 100mA input current limit when it is low and 500mA input current limit when it is high.

Ideal Diode From BAT to V_{OUT}

The LTC3553-2 has an internal ideal diode from BAT to V_{OUT} designed to respond quickly whenever V_{OUT} drops below BAT. If the load increases beyond the input current limit, additional current will be pulled from the battery via the ideal diode. Furthermore, if power to V_{BUS} (USB) is removed, then all of the application power will be provided by the battery via the ideal diode. The ideal diode is fast enough to keep V_{OUT} from dropping significantly with just the recommended output capacitor. The ideal diode consists of a precision amplifier that enables an on-chip

OPERATION

P-channel MOSFET whenever the voltage at V_{OUT} is approximately 15mV (V_{FWD}) below the voltage at BAT. The resistance of the internal ideal diode is approximately 240mΩ.

Suspend Mode

When the SUSP pin is pulled high the LTC3553-2 enters suspend mode to comply with the USB specification. In this mode, the power path between V_{BUS} and V_{OUT} is put in a high impedance state to reduce the V_{BUS} input current to 15µA. The system load connected to V_{OUT} is supplied through the ideal diode connected to BAT.

V_{BUS} Undervoltage Lockout (UVLO) and Undervoltage Current Limit (UVCL)

An internal undervoltage lockout circuit monitors V_{BUS} and keeps the input current limit circuitry off until V_{BUS} rises above the rising UVLO threshold (3.8V) and at least 200mV above V_{BAT}. Hysteresis on the UVLO turns off the input current limit circuitry if V_{BUS} drops below 3.6V or within 50mV of V_{BAT}. When this happens, system power at V_{OUT} will be drawn from the battery via the ideal diode. To minimize the possibility of oscillation in and out of UVLO when using resistive input supplies, the input current limit is reduced as V_{BUS} falls below 4.45V typical.

Battery Charger

The LTC3553-2 includes a constant-current/constant-voltage battery charger with automatic recharge, automatic termination by safety timer, low voltage trickle charging, bad cell detection and thermistor sensor input for out of temperature charge pausing. When a battery charge cycle begins, the battery charger first determines if the battery is deeply discharged. If the battery voltage is below V_{TRKL}, typically 2.9V, an automatic trickle charge feature sets the battery charge current to 10% of the programmed value. If the low voltage persists for more than 1/2 hour, the battery charger automatically terminates. Once the battery voltage is above 2.9V, the battery charger begins charging in full power constant current mode. The current delivered to the battery will try to reach 750V/R_{PROG}. Depending on available input power and external load conditions, the battery charger may or may not be able to charge at the full programmed current. The external load will always be prioritized over the battery charge current. The USB current limit programming will always be observed and only additional current will be available to charge the battery. When system loads are light, battery charge current will be maximized.

Charge Termination

The battery charger has a built-in safety timer. When the battery voltage approaches the float voltage, the charge current begins to decrease as the LTC3553-2 enters constant-voltage mode. Once the battery charger detects that it has entered constant-voltage mode, the four hour safety timer is started. After the safety timer expires, charging of the battery will terminate and no more current will be delivered to the battery.

Automatic Recharge

After the battery charger terminates, it will remain off drawing only microamperes of current from the battery. If the portable product remains in this state long enough, the battery will eventually self discharge. To ensure that the battery is always topped off, a charge cycle will automatically begin when the battery voltage falls below V_{RECHRG} (typically 4.1V). In the event that the safety timer is running when the battery voltage falls below V_{RECHRG}, the timer will reset back to zero. To prevent brief excursions below V_{RECHRG} from resetting the safety timer, the battery voltage must be below V_{RECHRG} for approximately 2ms. The charge cycle and safety timer will also restart if the V_{BUS} UVLO cycles low and then high (e.g., V_{BUS}, is removed and then replaced).

Charge Current

The charge current is programmed using a single resistor from PROG to ground. 1/750th of the battery charge current is delivered to PROG which will attempt to servo to 1.000V. Thus, the battery charge current will try to reach 750 times the current in the PROG pin. The program resistor and the charge current are calculated using the following equations:

$$R_{PROG} = \frac{750V}{I_{CHG}}, I_{CHG} = \frac{750V}{R_{PROG}}$$

OPERATION

In either the constant-current or constant-voltage charging modes, the PROG pin voltage will be proportional to the actual charge current delivered to the battery. Therefore, the actual charge current can be determined at any time by monitoring the PROG pin voltage and using the following equation:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 750$$

In many cases, the actual battery charge current, I_{BAT}, will be lower than I_{CHG} due to limited input current available and prioritization with the system load drawn from V_{OUT}.

Thermal Regulation

To prevent thermal damage to the IC or surrounding components, an internal thermal feedback loop will automatically decrease the programmed charge current if the die temperature rises to approximately 110°C. Thermal regulation protects the LTC3553-2 from excessive temperature due to high power operation or high ambient thermal conditions and allows the user to push the limits of the power handling capability with a given circuit board design without risk of damaging the LTC3553-2 or external components. The benefit of the LTC3553-2 thermal regulation loop is that charge current can be set according to the desired charge rate rather than worst-case conditions with the assurance that the battery charger will automatically reduce the current in worst-case conditions.

Charge Status Indication

The $\overline{CHRG}$ pin indicates the status of the battery charger. An open-drain output, the $\overline{CHRG}$ pin can drive an indicator LED through a current limiting resistor for human interfacing or simply a pull-up resistor for microprocessor interfacing. When charging begins, $\overline{CHRG}$ is pulled low and remains low for the duration of a normal charge cycle. When charging is complete, i.e., the charger enters constant-voltage mode and the charge current has dropped to one-tenth of the programmed value, the $\overline{CHRG}$ pin is released (high impedance). The $\overline{CHRG}$ pin does not respond to the C/10 threshold if the LTC3553-2 reduces the charge current due to excess load on the V_{OUT} pin. This prevents false end of charge indications due to insufficient power available to the battery charger. Even though charging is stopped during an NTC fault the $\overline{CHRG}$ pin will stay low indicating that charging is not complete.

Battery Charger Stability Considerations

The LTC3553-2's battery charger contains both a constant-voltage and a constant-current control loop. The constant-voltage loop is stable without any compensation when a battery is connected with low impedance leads. Excessive lead length, however, may add enough series inductance to require a bypass capacitor of at least 1µF from BAT to GND. Furthermore, a 100µF 1210 ceramic capacitor in series with a 0.3Ω resistor from BAT to GND is required to keep ripple voltage low if operation with the battery disconnected is allowed.

High value, low ESR multilayer ceramic chip capacitors reduce the constant-voltage loop phase margin, possibly resulting in instability. Ceramic capacitors up to 22µF may be used in parallel with a battery, but larger ceramics should be decoupled with 0.2Ω to 1Ω of series resistance.

In constant-current mode, the PROG pin is in the feedback loop rather than the battery voltage. Because of the additional pole created by any PROG pin capacitance, capacitance on this pin must be kept to a minimum. With no additional capacitance on the PROG pin, the battery charger is stable with program resistor values as high as 25k. However, additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 100kHz. Therefore, if the PROG pin has a parasitic capacitance, C_{PROG}, the following equation should be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \leq \frac{1}{2\pi \bullet 100kHz \bullet C_{PROG}}$$

OPERATION

NTC Thermistor

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. To use this feature connect the NTC thermistor, R_{NTC}, between the NTC pin and ground and a bias resistor, R_{NOM}, from V_{BUS} to NTC, as shown in Figure 1. R_{NOM} should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C (R25). The LTC3553-2 will pause charging when the resistance of the NTC thermistor drops to 0.54 times the value of R25 or approximately 54k (for a Vishay curve 1 thermistor, this corresponds to approximately 40°C). If the battery charger is in constant-voltage mode, the safety timer also pauses until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The LTC3553-2 is also designed to pause charging when the value of the NTC thermistor increases to 3.17 times the value of R25. For a Vishay curve 1 thermistor this resistance, 317k, corresponds to approximately 0°C. The hot and cold comparators each have approximately 3°C of hysteresis to prevent oscillation about the trip point.

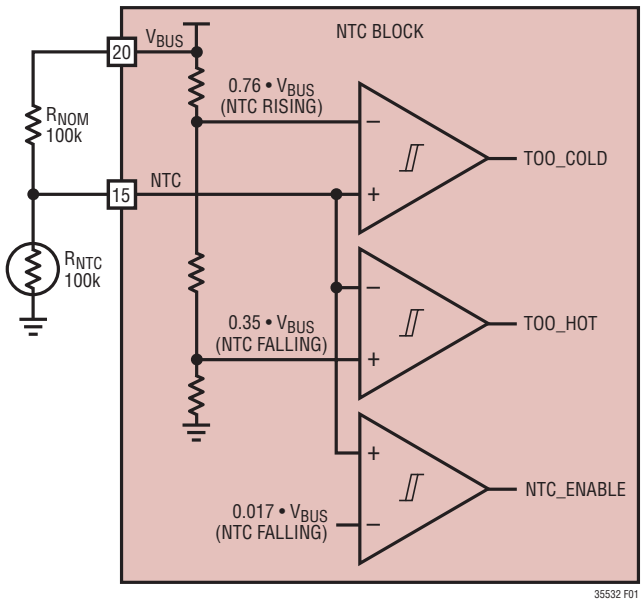


Figure 1. Typical NTC Thermistor Circuit

Alternate NTC Thermistors and Biasing

The LTC3553-2 provides temperature qualified charging if a grounded thermistor and a bias resistor are connected to NTC. By using a bias resistor whose value is equal to the room temperature resistance of the thermistor (R25) the upper and lower temperatures are preprogrammed to approximately 40°C and 0°C, respectively (assuming a Vishay curve 1 thermistor).

The upper and lower temperature thresholds can be adjusted by either a modification of the bias resistor value or by adding a second adjustment resistor to the circuit. If only the bias resistor is adjusted, then either the upper or the lower threshold can be modified but not both. The other trip point will be determined by the characteristics of the thermistor. Using the bias resistor in addition to an adjustment resistor, both the upper and the lower temperature trip points can be independently programmed with the constraint that the difference between the upper and lower temperature thresholds cannot decrease. Examples of each technique are given below.

NTC thermistors have temperature characteristics which are indicated on resistance-temperature conversion tables. The Vishay-Dale thermistor NTHS0603N011-N1003F, used in the following examples, has a nominal value of 100k and follows the Vishay curve 1 resistance-temperature characteristic.

In the explanation below, the following notation is used.

R25 = Value of the thermistor at 25°C

$R_{NTC|COLD}$ = Value of thermistor at the cold trip point

$R_{NTC|HOT}$ = Value of the thermistor at the hot trip point

r_{COLD} = Ratio of $R_{NTC|COLD}$ to R25

r_{HOT} = Ratio of $R_{NTC|HOT}$ to R25

R_{NOM} = Primary thermistor bias resistor (see Figure 2)

R1 = Optional temperature range adjustment resistor (see Figure 2)

OPERATION

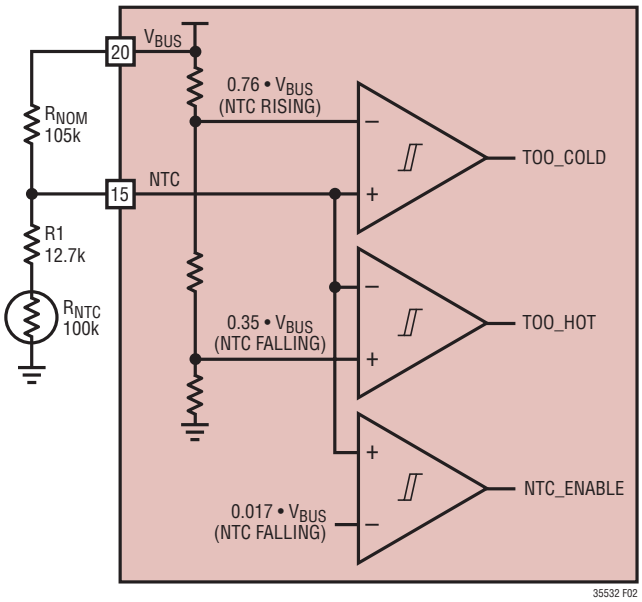


Figure 2. NTC Thermistor Circuit With Additional Bias Resistor

The trip points for the LTC3553-2's temperature qualification are internally programmed at 0.35 • V_{BUS} for the hot threshold and 0.76 • V_{BUS} for the cold threshold.

Therefore, the hot trip point is set when:

$$\frac{R_{NTC|HOT}}{R_{NOM}+R_{NTC|HOT}} \bullet V_{BUS} = 0.35 \bullet V_{BUS}$$

and the cold trip point is set when:

$$\frac{R_{NTC|COLD}}{R_{NOM}+R_{NTC|COLD}} \bullet V_{BUS} = 0.76 \bullet V_{BUS}$$

Solving these equations for $R_{NTC|COLD}$ and $R_{NTC|HOT}$ results in the following:

$$R_{NTC|HOT} = 0.538 \bullet R_{NOM}$$

and

$$R_{NTC|COLD} = 3.17 \bullet R_{NOM}$$

By setting R_{NOM} equal to R25, the above equations result in $r_{HOT} = 0.538$ and $r_{COLD} = 3.17$. Referencing these ratios to the Vishay Resistance-Temperature Curve 1 chart gives a hot trip point of about 40°C and a cold trip point of about 0°C. The difference between the hot and cold trip points is approximately 40°C.

By using a bias resistor, R_{NOM}, different in value from R25, the hot and cold trip points can be moved in either direction. The temperature span will change somewhat due to the nonlinear behavior of the thermistor. The following equations can be used to easily calculate a new value for the bias resistor:

$$R_{NOM} = \frac{r_{HOT}}{0.538} \bullet R25$$

$$R_{NOM} = \frac{r_{COLD}}{3.17} \bullet R25$$

where r_{HOT} and r_{COLD} are the resistance ratios at the desired hot and cold trip points. Note that these equations are linked. Therefore, only one of the two trip points can be independently set, the other is determined by the default ratios designed in the IC.

Consider an example where a 60°C hot trip point is desired. From the Vishay curve 1 R-T characteristics, r_{HOT} is 0.2488 at 60°C. Using the above equation, R_{NOM} should be set to 46.4k. With this value of R_{NOM}, the cold trip point is about 16°C. Notice that the span is now 44°C rather than the previous 40°C. This is due to the decrease in temperature gain of the thermistor as absolute temperature increases.

The upper and lower temperature trip points can be independently programmed by using an additional bias resistor as shown in Figure 2. The following formulas can be used to compute the values of R_{NOM} and R1:

$$R_{NOM} = \frac{r_{COLD} - r_{HOT}}{2.714} \bullet R25$$

$$R1 = 0.536 \bullet R_{NOM} - r_{HOT} \bullet R25$$

For example, to set the trip points to 0°C and 45°C with a Vishay curve 1 thermistor choose:

$$R_{NOM} = \frac{3.266 - 0.4368}{2.714} \bullet 100k = 104.2k$$

the nearest 1% value is 105k:

$$R1 = 0.536 \bullet 105k - 0.4368 \bullet 100k = 12.6k$$

The nearest 1% value is 12.7k. The final solution is shown in Figure 2 and results in an upper trip point of 45°C and a lower trip point of 0°C.

OPERATION

BUCK REGULATOR

Introduction

The LTC3553-2 includes a constant-frequency current-mode 200mA buck regulator. At light loads, the regulator automatically enters Burst Mode operation to maintain high efficiency.

Applications with a near-zero-current sleep or memory keep-alive mode can command the LTC3553-2 buck regulator into a standby mode that maintains output regulation while drawing only 1.5µA quiescent current. Load capability drops to 10mA in this mode.

The buck regulator is enabled, disabled and sequenced through the pushbutton interface (see the Pushbutton Interface section for more information). It is recommended that the buck regulator input supply (BVIN) be connected to the system supply pin (V_{OUT}). This is recommended because the undervoltage lockout circuit on the V_{OUT} pin (V_{OUT} UVLO) disables the buck regulator when the V_{OUT} voltage drops below the V_{OUT} UVLO threshold. If driving the buck regulator input supply from a voltage other than V_{OUT}, the regulator should not be operated outside its specified operating voltage range as operation is not guaranteed beyond this range.

Output Voltage Programming

Figure 3 shows the buck regulator application circuit. The output voltage for the buck regulator is programmed using a resistor divider from the buck regulator output connected to the feedback pin (BUCK_FB) such that:

$$V_{BUCK} = 0.8V \bullet \left(\frac{R1}{R2} + 1\right)$$

Typical values for R1 can be as high as 2.2MΩ. (R1 + R2) can be as high as 3MΩ. The capacitor C_{FB} cancels the pole created by feedback resistors and the input capacitance of the BUCK_FB pin and also helps to improve transient response for output voltages much greater than 0.8V. A variety of capacitor sizes can be used for C_{FB} but a value of 10pF is recommended for most applications. Experimentation with capacitor sizes between 2pF and 22pF may yield improved transient response.

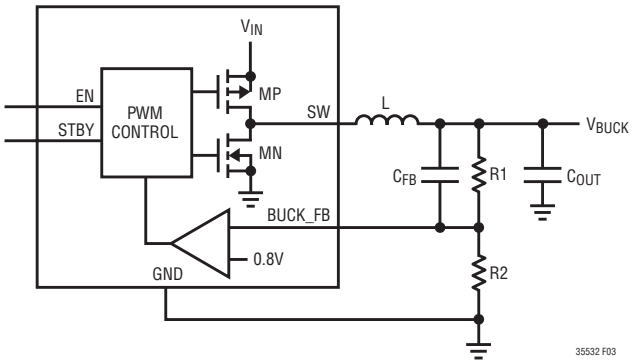


Figure 3. Buck Regulator Application Circuit

Normal Buck Operating Mode (STBY Pin Low)

In normal mode (STBY pin low), the buck regulator performs as a traditional constant-frequency current mode switching regulator. Switching frequency is determined by an internal oscillator which operates at 1.125MHz. An internal latch is set at the start of every oscillator cycle, turning on the main P-channel MOSFET switch. During each cycle, a current comparator compares the inductor current to the output of an error amplifier. The output of the current comparator resets the internal latch, which causes the main P-channel MOSFET switch to turn off and the N-channel MOSFET synchronous rectifier to turn on. The N-channel MOSFET synchronous rectifier turns off at the end of the clock cycle, or when the current through the N-channel MOSFET synchronous rectifier drops to zero, whichever happens first. Via this mechanism, the error amplifier adjusts the peak inductor current to deliver the required output power. All necessary compensation is internal to the buck regulator requiring only a single ceramic output capacitor for stability.

At light load and no-load conditions, the buck automatically switches to a power-saving hysteretic control algorithm that operates the switches intermittently to minimize switching losses. Known as Burst Mode operation, the buck cycles

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the power switches enough times to charge the output capacitor to a voltage slightly higher than the regulation point. The buck then goes into a reduced quiescent current sleep mode. In this state, power loss is minimized while the load current is supplied by the output capacitor. Whenever the output voltage drops below a predetermined value, the buck wakes from sleep and cycles the switches again until the output capacitor voltage is once again slightly above the regulation point. Sleep time thus depends on load current, since the load current determines the discharge rate of the output capacitor.

Standby Mode Buck Operation (STBY Pin High)

There are situations where even the low quiescent current of Burst Mode operation is not low enough. For instance, in a static memory keep alive situation, load current may fall well below 1µA. In this case, the 22µA typical BVIN quiescent current in Burst Mode operation becomes the main factor determining battery run time.

Standby mode cuts BVIN quiescent current down to just 1.5µA, greatly extending battery run time in this essentially no-load region of operation. The application circuit commands the LTC3553-2 into and out of standby mode via the STBY pin logic input. Bringing the STBY pin high places the regulator into standby mode, while bringing it low returns it to Burst Mode operation. In standby mode, buck load capability drops to 10mA.

In standby mode, the buck regulator operates hysteretically. When the BUCK_FB pin voltage falls below the internal 0.8V reference, a current source from BVIN to SW turns on, delivering current through the inductor to the switching regulator output capacitor and load. When the FB pin voltage rises above the reference plus a small hysteresis voltage, that current is shut off. In this way, output regulation is maintained.

Since the power transfer from BVIN to SW is through a high impedance current source rather than through a low impedance MOSFET switch, power loss scales with load current as in a linear low dropout (LDO) regulator, rather than as in a switching regulator. For near-zero load conditions where regulator quiescent current is the dominant power loss, standby mode is ideal. But at any appreciable load current, Burst Mode operation yields the best overall conversion efficiency.

Shutdown

The buck regulator is shut down and enabled via the pushbutton interface. In shutdown, it draws only a few nanoamps of leakage current from the BVIN pin. It also pulls down on its output with a 10k resistor from its switch pin to ground.

Dropout Operation

It is possible for the buck regulator's input voltage to fall near or below its programmed output voltage (e.g., a battery voltage of 3.4V with a programmed output voltage of 3.3V). When this happens, the PMOS switch duty cycle increases to 100%, keeping the switch on continuously. Known as dropout operation, the output voltage equals the regulator's input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor.

Soft-Start Operation

In normal operating mode, soft-start works by gradually increasing the maximum allowed peak inductor current for the buck regulator over a 500µs period. This allows the output to rise slowly, helping minimize the inrush current needed to charge up the output capacitor. A soft-start cycle occurs whenever the buck is enabled.

Soft-start occurs only in normal operation, but not in standby mode. Standby mode operation is already inherently current-limited, since the regulator works by intermittently turning on a current source from BVIN to SW. Changing the state of the STBY pin while the regulators are operating doesn't trigger a new soft-start cycle, to avoid glitching the outputs.

Inductor Selection

Many different sizes and shapes of inductors are available from numerous manufacturers. Choosing the right inductor from such a large selection of devices can be overwhelming, but following a few basic guidelines will make the selection process much simpler.

OPERATION

Inductor value should be chosen based on the desired output voltage. See Table 1. Table 3 shows several inductors that work well with the step-down switching buck regulator. These inductors offer a good compromise in current rating, DCR and physical size. Consult each manufacturer for detailed information on their entire selection of inductors.

Larger value inductors reduce ripple current, which improves output ripple voltage. Lower value inductors result in higher ripple current and improved transient response time, but will reduce the available output current. To maximize efficiency, choose an inductor with a low DC resistance.

Choose an inductor with a DC current rating at least 1.5 times larger than the maximum load current to ensure that the inductor does not saturate during normal operation. If output short circuit is a possible condition, the inductor should be rated to handle the maximum peak current specified for the buck converter.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. Inductors that are very thin or have a very small volume typically have much higher core and DCR losses, and will not give the best efficiency. The choice of which style inductor to use often depends more on the price versus size, performance and any radiated EMI requirements than on what the buck requires to operate.

The inductor value also has an effect on Burst Mode operation. Lower inductor values will cause Burst Mode switching frequency to increase.

Input/Output Capacitor Selection

Low ESR (equivalent series resistance) ceramic capacitors should be used at the buck output as well as at the buck input supply. Only X5R or X7R ceramic capacitors should be used because they retain their capacitance over wider voltage and temperature ranges than other ceramic types. For good transient response and stability the output capacitor should retain at least 4µF of capacitance over operating temperature and bias voltage. Generally, a good starting point is to use a 10µF output capacitor.

Table 1. Choosing the Inductor Value

DESIRED OUTPUT VOLTAGE	RECOMMENDED INDUCTOR VALUE
1.8V or Less	10µH
1.8V to 2.5V	6.8µH
2.5V to 3.3V	4.7µH

Table 2. Ceramic Capacitor Manufacturers

AVX	www.avxcorp.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay Siliconix	www.vishay.com
TDK	www.tdk.com

Table 3. Recommended Inductors for the Buck Regulator

INDUCTOR PART NO.	L (µH)	MAX I_{DC} (A)	MAX DCR (Ω)	SIZE (L × W × H) (mm)	MANUFACTURER
1117AS-4R7M 1117AS-6R8M 1117AS-100M	4.7 6.8 10	0.64 0.54 0.45	0.18* 0.250* 0.380*	3.0 × 2.8 × 1.0	Toko www.toko.com
CDRH2D11BNP-4R7N CDRH2D11BNP-6R8N CDRH2D11BNP-100N	4.7 6.8 10	0.7 0.6 0.48	0.248 0.284 0.428	3.0 × 3.0 × 1.2	Sumida www.sumida.com
SD3112-4R7-R SD3112-6R8-R SD3112-100-R	4.7 6.8 10	0.8 0.68 0.55	0.246* 0.291* 0.446*	3.1 × 3.1 × 1.2	Cooper www.cooperet.com
EPL2014-472ML_ EPL2014-682ML_ EPL2014-103ML_	4.7 6.8 10	0.88 0.8 0.6	0.254 0.316 0.459	2.0 × 1.8 × 1.4	Coilcraft www.coilcraft.com

* = Typical DCR

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The switching regulator input supply should be bypassed with a 2.2µF capacitor. Consult with capacitor manufacturers for detailed information on their selection and specifications of ceramic capacitors. Many manufacturers now offer very thin (<1mm tall) ceramic capacitors ideal for use in height-restricted designs. Table 2 shows a list of several ceramic capacitor manufacturers.

ALWAYS-ON LOW DROPOUT LINEAR REGULATOR (LDO)

The LDO regulator supports a load of up to 150mA. The LDO takes power from the V_{INLDO} pin and drives the LDO output pin with the goal of bringing the LDO_FB feedback pin voltage to 0.8V. Usually, a resistor divider is connected between the LDO's output pin, feedback pin and ground, in order to close the control loop and program the output voltage. For stability, the LDO output must be bypassed to ground with at least a 1µF ceramic capacitor.

The LDO is enabled whenever the LTC3553-2 is not in hard reset state. In hard reset state, an internal pull-down resistor is switched in to help bring the output to ground. When the LDO is enabled, a soft-start circuit ramps its regulation point from zero to final value over a period of roughly 0.2ms, reducing the required V_{INLDO} inrush current.

The LDO has two input voltage requirements. The LDO's quiescent bias current is supplied through an internal connection to the USB PowerPath V_{OUT} pin. The LDO's power input is taken from the V_{INLDO} pin. For proper LDO operation, the V_{INLDO} pin must be connected to a voltage no greater than V_{OUT}. Connecting V_{INLDO} to a voltage exceeding V_{OUT} may result in loss of regulation.

Output Voltage Programming

Figure 4 shows the LDO regulator application circuit. Program the LDO output voltage, V_{LDO}, by choosing R1 and R2 such that:

$$V_{LDO} = 0.8V \bullet \left(\frac{R1}{R2} + 1\right)$$

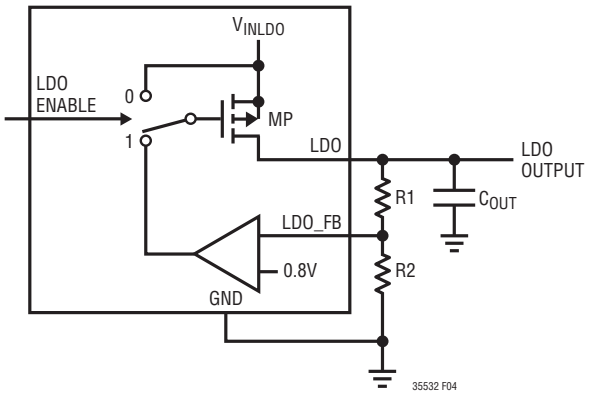

Figure 4. LDO Application Circuit

PGOOD Operation

The PGOOD pin is an open-drain output which indicates that all enabled regulators have reached their final regulation voltage. It goes high impedance 1.8ms after all enabled regulators reach 92% of their regulation value. The delay allows time for an external processor to reset itself. PGOOD may be used as a power-on reset to a microprocessor powered by the buck regulator. Since PGOOD is an open-drain output, a pull-up resistor to an appropriate power source is needed. A suggested approach is to connect the pull-up resistor to the LDO output or V_{OUT} pin so that power is not dissipated while in hard reset state.

V_{OUT} UNDERVOLTAGE LOCKOUT (V_{OUT} UVLO)

An undervoltage lockout circuit on the USB PowerPath V_{OUT} pin shuts down and prevents both the buck and the LDO from enabling when the V_{OUT} pin voltage drops below about 2.6V.

Buck Regulator UVLO Considerations

It is recommended that the buck regulator input supply (BVIN pin) be connected directly to the USB PowerPath output (V_{OUT} pin). With this connection, the V_{OUT} UVLO prevents the buck regulator from operating at low input

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supply voltages where loss of regulation or other undesirable operation may occur. In applications where the buck input is supplied from other than the V_{OUT} pin, other measures should be taken to ensure that the buck is not operated outside the specified BVIN input supply range, as operation beyond this range is not guaranteed.

LDO Regulator UVLO Considerations

The LDO regulator's bias current is supplied via an internal connection to the USB PowerPath V_{OUT} pin. The V_{OUT} UVLO shuts down the LDO when V_{OUT} drops below about 2.6V in order to prevent the LDO from operating incorrectly due to too low a bias supply voltage.

The LDO power input pin, V_{INLDO}, can be driven with as little as 1.65V. There is, however, no UVLO to enforce this requirement. It is thus recommended that V_{INLDO} be tied to the USB PowerPath V_{OUT} pin, to ensure proper operation.

PUSHBUTTON INTERFACE

State Diagram/Operation

Figure 5 shows the LTC3553-2 pushbutton state diagram. The pushbutton state machine has a clock with 1.82ms period.

Upon first application of power, V_{BUS} or BAT, an internal power on reset (POR) signal places the pushbutton

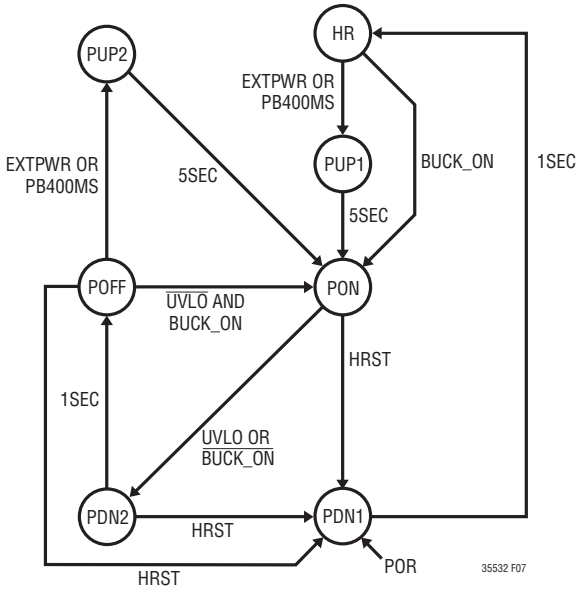

Figure 5. Pushbutton State Diagram

circuitry into the power-down (PDN1) state. One second after entering the PDN1 state the pushbutton circuitry will transition into the hard reset (HR) state.

In the HR state, all supplies are disabled. The PowerPath circuitry is placed in an ultralow quiescent state to minimize battery drain. If no external charging supply is present (V_{BUS}) then the ideal diode is shut down, disconnecting V_{OUT} from BAT to further minimize battery drain. The ultralow power consumption in the HR state makes it ideal for shipping or long term storage, minimizing battery drain.

The following events cause the state machine to transition out of HR into the power-up (PUP1) state:

$\overline{ON}$ input low for 400ms (PB400MS)

Application of external power (EXTPWR)

Upon entering the PUP1 state, the pushbutton circuitry will sequence up the LDO and buck regulators. The buck regulator is enabled once the feedback voltage of the LDO nears regulation.

The BUCK_ON input is ignored in the PUP1 state. The state machine remains in the PUP1 state for five seconds. During the five seconds, the application's microprocessor, powered by the regulators, has time to boot and assert BUCK_ON. Five seconds after entering the PUP1 state, the pushbutton circuitry automatically transitions into the power-on (PON) state.

In the PON state, the buck regulator can be enabled and shut down at any time by the BUCK_ON pin. A high on BUCK_ON is needed to keep the buck enabled. To remain in the PON state, the application circuit must keep the BUCK_ON input high, else the state machine enters the power-down (PDN2) state.

When BUCK_ON is low, or when V_{OUT} drops to its undervoltage lockout (V_{OUT} UVLO) threshold, the state machine will leave the PON state and enter the power-down (PDN2) state. In the power-down state (PDN2), the buck regulator is kept disabled regardless of the state of the BUCK_ON pin. The state machine remains in the power-down state for one second, before automatically entering the power-off (POFF) state. This one second delay allows the buck

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output time to power down completely before it can be re-enabled.

The same events used to exit the hard reset (HR) state are also used to exit the POFF state and enter the PUP2 state. The PUP2 state operates in a similar manner as the PUP1 state previously described.

Both regulators remain powered up during the five second power-up (PUP1 or PUP2) period, regardless of the state of the BUCK_ON input.

In either the HR or POFF states, if the BUCK_ON pin is driven high, the pushbutton circuitry directly enters the PON state, without passing through the power-up (PUP1 or PUP2) states.

Starting from the HR state, bringing the BUCK_ON pin high enables the PowerPath, if it wasn't already enabled due to V_{BUS} power being available. This powers up the V_{OUT} pin from V_{BUS} or BAT. When the V_{OUT} voltage rises above the V_{OUT} UVLO threshold, the state machine transitions from the HR state into the PON state. At this point both the LDO and buck regulator will simultaneously turn on.

The hard reset (HRST) event is generated by pressing and holding the pushbutton ($\overline{ON}$ input low) for 14 seconds. For a valid HRST event to occur the button press must start in the PUP1, PUP2 or PON state, but can end in any state. If a valid HRST event is present in PON, PDN2 or POFF, then the state machine will transition to the PDN1 state and subsequently transition to the HR state one second later.

Debounced Pushbutton Output (PBSTAT)

In the PON, PUP1, and PUP2 states, the PBSTAT open-drain output pin outputs a debounced version of the $\overline{ON}$ pushbutton signal. $\overline{ON}$ must be held low for at least 50ms for the pushbutton interface to recognize it and cause PBSTAT to go low. PBSTAT goes high impedance when $\overline{ON}$ goes high, except the logic enforces a minimum pulse width of 50ms on PBSTAT.

In the HR, POFF, PDN1, and PDN2 states, PBSTAT remains high impedance regardless of the state of $\overline{ON}$.

Power-Up Via Pushbutton Press from Hard Reset

Figure 6 shows the LTC3553-2 powering up through application of the external pushbutton. For this example the pushbutton circuitry starts in the HR state with a battery connected. Pushbutton application ($\overline{ON}$ low) for 400ms transitions the pushbutton circuitry into the PUP1 state and powers up the LDO followed by the buck. If BUCK_ON goes low after the five second period the buck regulator will be shut down.

PGOOD is asserted once all enabled regulators are within 8% of their regulation voltage for 1.8ms. The BUCK_ON input can be driven via a µP/µC or by one of the regulator outputs through a high impedance (100kΩ typical) to keep the buck enabled as described above. PBSTAT does not go low on initial pushbutton application for power-up, but will go low with subsequent $\overline{ON}$ pushbutton applications in the PUP1, PUP2 or PON states.

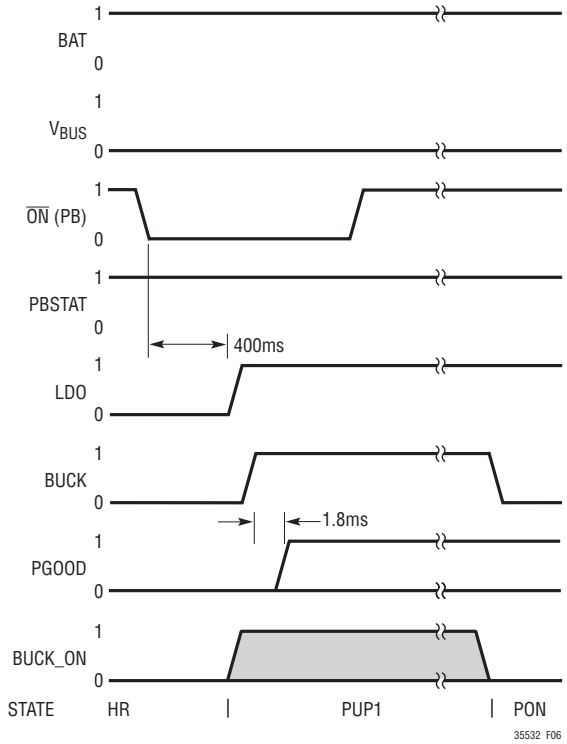


Figure 6. Power-Up via Pushbutton Press

OPERATION

Power-Up Via Applying External Power from Power Off

Figure 7 shows the LTC3553-2 powering up through application of external power (V_{BUS}). For this example the pushbutton circuitry starts in the POFF state with a battery connected. 100ms after V_{BUS} application the pushbutton circuitry transitions into the PUP2 state and powers up the buck. The 100ms delay time allows the applied supply to settle. The buck regulator will stay powered as long as the BUCK_ON input is driven high before the five second PUP2 period is over. If the BUCK_ON is low or goes low after the five second period the buck regulator will be shut down. In the above example the BUCK_ON pin is high at the end of the five second period and therefore the buck regulator continues to stay on at the end of the five second period. In this example, PGOOD is initially high as the always-on LDO is enabled. At the end of 100ms, the input power at V_{BUS} is validated and the buck regulator is enabled at this point PGOOD goes low and will stay low until the buck regulator is within 8% of its regulation voltage for 1.8ms.

The BUCK_ON input can be driven via a µP/µC or one of the regulator outputs through a high impedance (100kΩ typ) to keep the buck regulator enabled as described above.

Without a battery present, initial power application causes a power-on reset which puts the pushbutton circuitry in the PDN1 state and subsequently the HR state one second later. At this time, if a valid supply voltage is detected at the BUS pin (i.e., $V_{BUS} > V_{UVLO}$ and $V_{BUS} - V_{BAT} > V_{DUVLO}$), the pushbutton circuity immediately enters the PUP1 state. For this to work reliably, the BAT pin voltage must be kept well-behaved when no battery is connected. Ensure this by bypassing the BAT pin to GND with an RC network consisting of a 100µF ceramic capacitor in series with 0.3Ω.

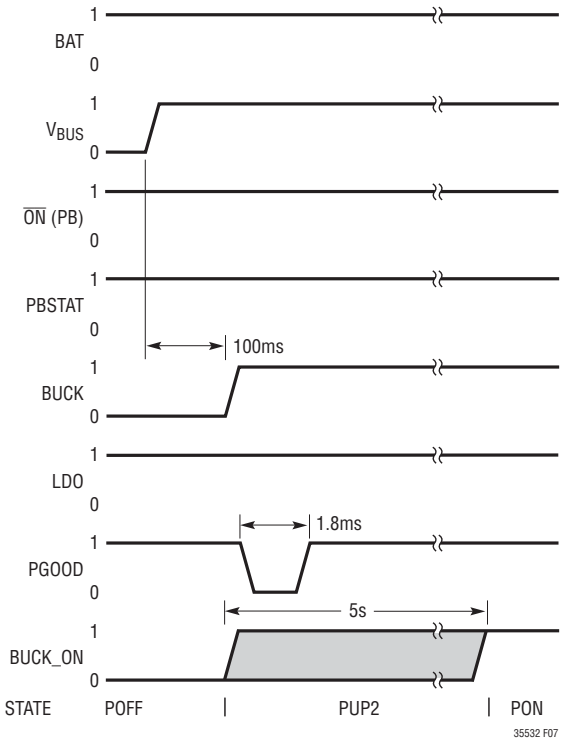


Figure 7. Power-Up via Applying External Power

OPERATION

Power-Up Via Asserting the BUCK_ON Pin

Figure 8 shows the LTC3553-2 powering up by driving BUCK_ON high. For this example the pushbutton circuitry starts in the HR state with a battery connected. Once BUCK_ON goes high, the pushbutton circuitry enters the PON state and the buck powers up. Also, as the part exits the hard reset state the LDO will power up simultaneously. The PGOOD is initially low and will go high once both regulators are within 8% of their regulation voltage for 1.8ms.

Powering up via asserting the BUCK_ON pin is useful for applications containing an always-on µC that's not powered by the LTC3553-2 regulators. That µC can power the application up and down for housekeeping and other activities not needing the user's control.

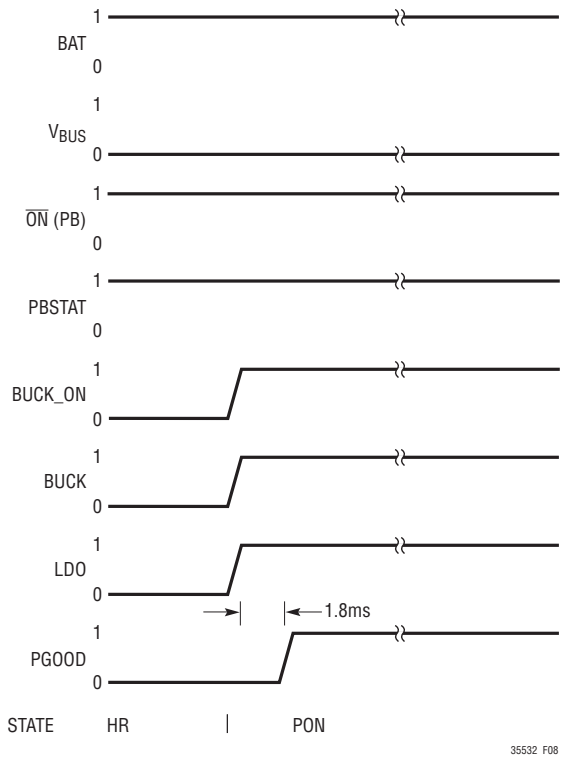


Figure 8. Power-Up via Asserting the BUCK_ON Pin

Power-Down by De-Asserting BUCK_ON

Figure 9 shows the LTC3553-2 powering down by µC/µP control. For this example the pushbutton circuitry starts in the PON state with a battery connected and both regulators enabled. The user presses the pushbutton ($\overline{ON}$ low) for at least 50ms, which generates a debounced, low impedance pulse on the PBSTAT output. After receiving the PBSTAT signal, the µC/µP software decides to drive the BUCK_ON input low in order to power down. After the BUCK_ON input goes low, the pushbutton circuitry will enter the PDN2 state. In the PDN2 state a one second wait time is initiated after which the pushbutton circuitry enters the POFF state. During this one second time, the $\overline{ON}$, and BUCK_ON inputs as well as external power application are ignored. Though the above assumes a battery

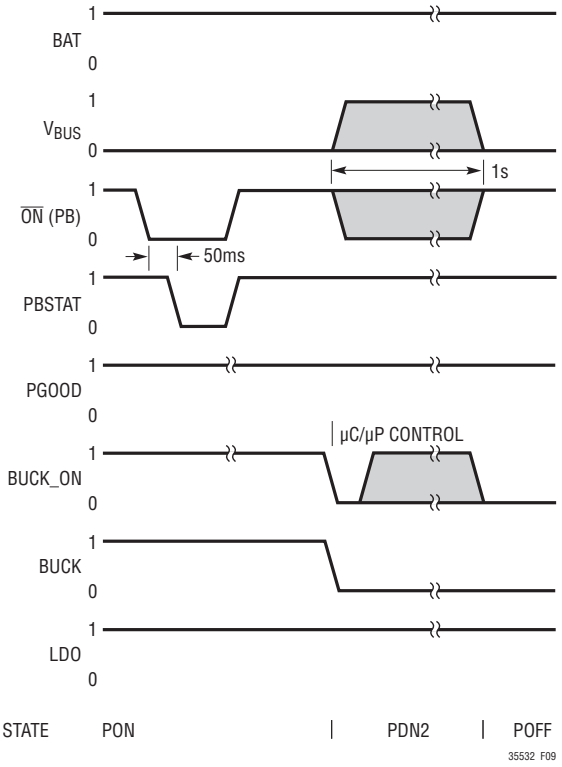


Figure 9. Power-Down via De-Assertion of BUCK_ON

OPERATION

present, the same operation would take place with a valid external supply (V_{BUS}) with or without a battery present.

The PGOOD remains asserted through this state transition as the LDO stays on.

Holding $\overline{ON}$ low through the one second power-down period will not cause a power-up event at end of the one second period. The $\overline{ON}$ pin must be brought high following the power-down event and then go low again to establish a valid power-up event.

UVLO Minimum Off-Time Timing (Low Battery)

Figure 10 assumes the battery is either missing or at a voltage below the V_{OUT} UVLO threshold, and the application is running via external power (V_{BUS}). A glitch on the external supply causes V_{OUT} to drop below the V_{OUT} UVLO threshold temporarily. This V_{OUT} UVLO condition causes the pushbutton circuitry to transition from the PON state to the PDN2 state. Upon entering the PDN2 state the buck regulator powers down. The V_{OUT} UVLO condition also disables the LDO causing the PGOOD to go low. Once the LDO powers back up and is in regulation for 1.8ms, the PGOOD will go high impedance.

In the typical case where the BUCK_ON pin is driven by logic powered by the buck regulator, the BUCK_ON pin would also go low, as depicted in Figure 10. If the external supply recovers after entering the PDN2 state such that V_{OUT} is no longer in UVLO, then the LTC3553-2 will transition back into the PUP2 state once the PDN2 one second delay is complete. Following the state diagram, the transition from PDN2 to PUP2 in this case actually occurs via a brief visit to the POFF state. During the brief

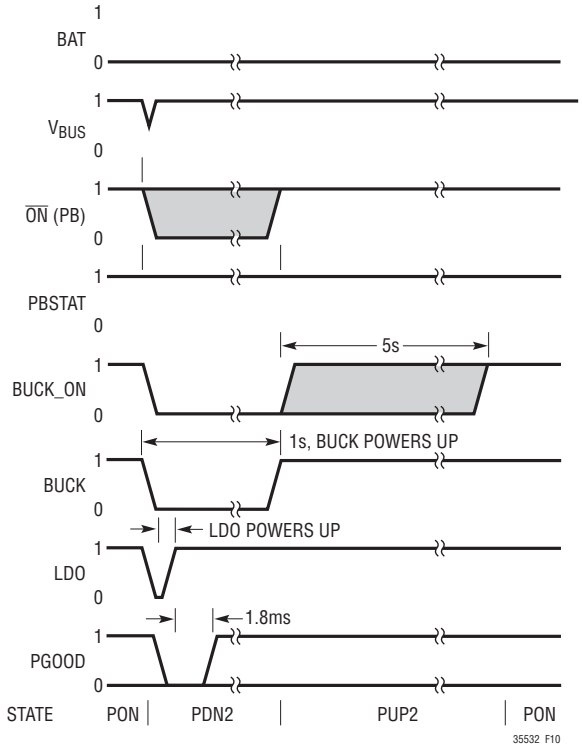


Figure 10. UVLO Minimum Off-Time Timing

OPERATION

POFF state, the state machine immediately recognizes that valid external power is available and transitions into the PUP2 state. Entering the PUP2 state will cause the buck to power up as described previously in the power-up sections.

Not depicted here, but in cases where the BUCK_ON pin is driven by a supply that remains high when entering the POFF state, then as per the state diagram in Figure 7, the pushbutton circuitry will enter the PON state once V_{OUT} is no longer in UVLO. Upon entering the PON state, the buck regulator will power up.

Note: If V_{OUT} drops too low (below about 1.9V) the LTC3553-2 will see this as a POR condition and will enter the PDN1 state rather than the PDN2 state. One second later the part will transition to the HR state. Under these conditions an explicit power-up event (such as a pushbutton press) may be required to bring the LTC3553-2 out of hard reset.

Hard Reset Timing

HARD RESET provides an ultralow power-down state for shipping or long term storage as well as a way to power down the application in case of a software lockup. In the case of software lockup, the user can hold the pushbutton ($\overline{ON}$ low) for 14 seconds and a hard reset event (HRST) will occur, placing the pushbutton circuitry in the power-down (PDN1) state. At this point the buck regulator will be shut down. Following a one second power-down period the pushbutton circuitry will enter the hard reset state (HR). At this point the LDO regulator will be shut down.

Holding $\overline{ON}$ low through the one second power-down period will not cause a power-up event at end of the one second period. $\overline{ON}$ must be brought high following the power-down event and then go low again for 400ms to establish a valid power-up event, as shown in Figure 11.

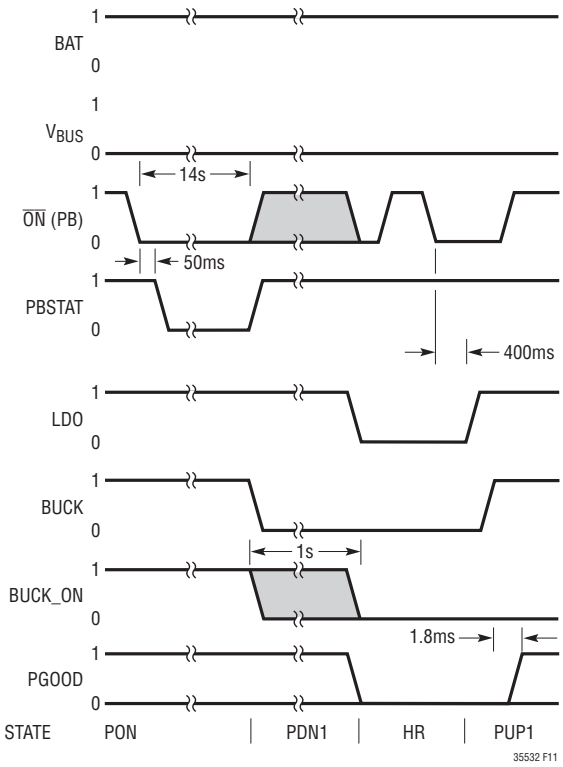


Figure 11. Hard Reset via Holding $\overline{ON}$ Low for 14 Seconds

OPERATION

Power-Up Sequencing

Figure 12 shows the actual power-up sequencing of the LTC3553-2. The regulators are both initially disabled (0V). Starting in hard reset state, if the pushbutton has been applied ($\overline{ON}$ low) for 400ms, the LDO is enabled. The LDO slews up and enters regulation. The actual slew rate is controlled by the soft start function of the LDO in conjunction with output capacitance and load (see the LDO Regulator Operation section for more information). When the LDO is within about 8% of final regulation, the buck is enabled and slews up into regulation. 1.8ms after the buck is within 8% of final regulation, the PGOOD output will go high impedance. The regulators in Figure 12 are slewing up with nominal output capacitors and no-load. Adding a load or increasing output capacitance on any of the outputs will reduce the slew rate and lengthen the time it takes the regulator to achieve regulation.

LAYOUT AND THERMAL CONSIDERATIONS

Printed Circuit Board Power Dissipation

In order to be able to deliver maximum charge current under all conditions, it is critical that the Exposed Pad on the backside of the LTC3553-2 package is soldered to a ground plane on the board. Correctly soldered to a 2500mm^2 ground plane on a double-sided 1oz copper board, the LTC3553-2 has a thermal resistance (θ_{JA}) of approximately 70°C/W. Failure to make good thermal contact between the Exposed Pad on the backside of the package and an adequately sized ground plane will result in thermal resistances far greater than 70°C/W.

The conditions that cause the LTC3553-2 to reduce charge current due to the thermal protection feedback can be approximated by considering the power dissipated in the

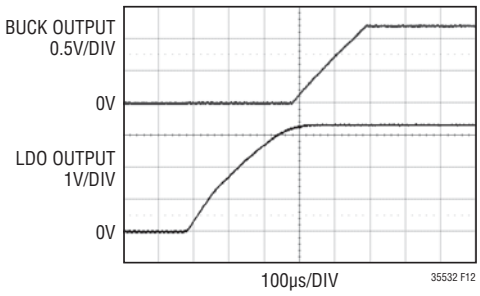


Figure 12. Power-Up Sequencing, Front Page Application Circuit

OPERATION

part. For high charge currents the LTC3553-2 power dissipation is approximately:

$$P_D = (V_{BUS}–BAT) \bullet I_{BAT} + P_{D(REGS)}$$

where P_D is the total power dissipated, V_{BUS} is the supply voltage, BAT is the battery voltage, and I_{BAT} is the battery charge current. $P_{D(REGS)}$ is the sum of power dissipated on chip by the step-down switching regulators.

The power dissipated by the buck regulator can be estimated as follows:

$$P_{D(BUCK)} = (B_{OUTx} \bullet I_{OUT}) \bullet (100 - Eff)/100$$

Where B_{OUTx} is the programmed output voltage, I_{OUT} is the load current and Eff is the % efficiency which can be measured or looked up on an efficiency table for the programmed output voltage.

The power dissipated by the LDO regulator can be estimated using:

$$P_{D(LDO)} = (V_{INLDO} – V_{LDO}) \bullet I_{LDO}$$

where V_{INLDO} is the LDO input supply voltage, V_{LDO} is the LDO regulated output voltage, and I_{LDO} is the LDO load current.

Thus the power dissipated by all regulators is:

$$P_{D(REGS)} = P_{D(BUCK)} + P_{D(LDO)}$$

It is not necessary to perform any worst-case power dissipation scenarios because the LTC3553-2 will automatically reduce the charge current to maintain the die temperature at approximately 110°C. However, the approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$$T_A = 110°C – P_D \bullet \theta_{JA}$$

Example: Consider the LTC3553-2 operating from a wall adapter with 5V (V_{BUS}) providing 400mA (I_{BAT}) to charge a Li-Ion battery at 3.3V (BAT). Also assume $P_{D(REGS)}$ = 0.3W, so the total power dissipation is:

$$P_D = (5V – 3.3V) \bullet 400mA + 0.3W = 0.98W$$

The ambient temperature above which the LTC3553-2 will begin to reduce the 400mA charge current, is approximately:

$$T_A = 110°C – 0.98W \bullet 70°C/W = 41.4°C$$

The LTC3553-2 can be used above 41.4°C, but the charge current will be reduced below 400mA. The charge current at a given ambient temperature can be approximated by:

$$P_D = (110°C – T_A) / \theta_{JA} = (V_{BUS} – BAT) \bullet I_{BAT} + P_{D(REGS)}$$

Thus:

$$I_{BAT} = \frac{[(110°C – T_A)/\theta_{JA} – P_{D(REGS)}]}{(V_{BUS} – BAT)}$$

Consider the above example with an ambient temperature of 60°C. The charge current will be reduced to approximately:

$$I_{BAT} = [(110°C – 60°C) / 70°C/W – 0.3W] / (5V – 3.3V)$$

$$I_{BAT} = (0.71W – 0.3W) / 1.7V = 241mA$$

OPERATION

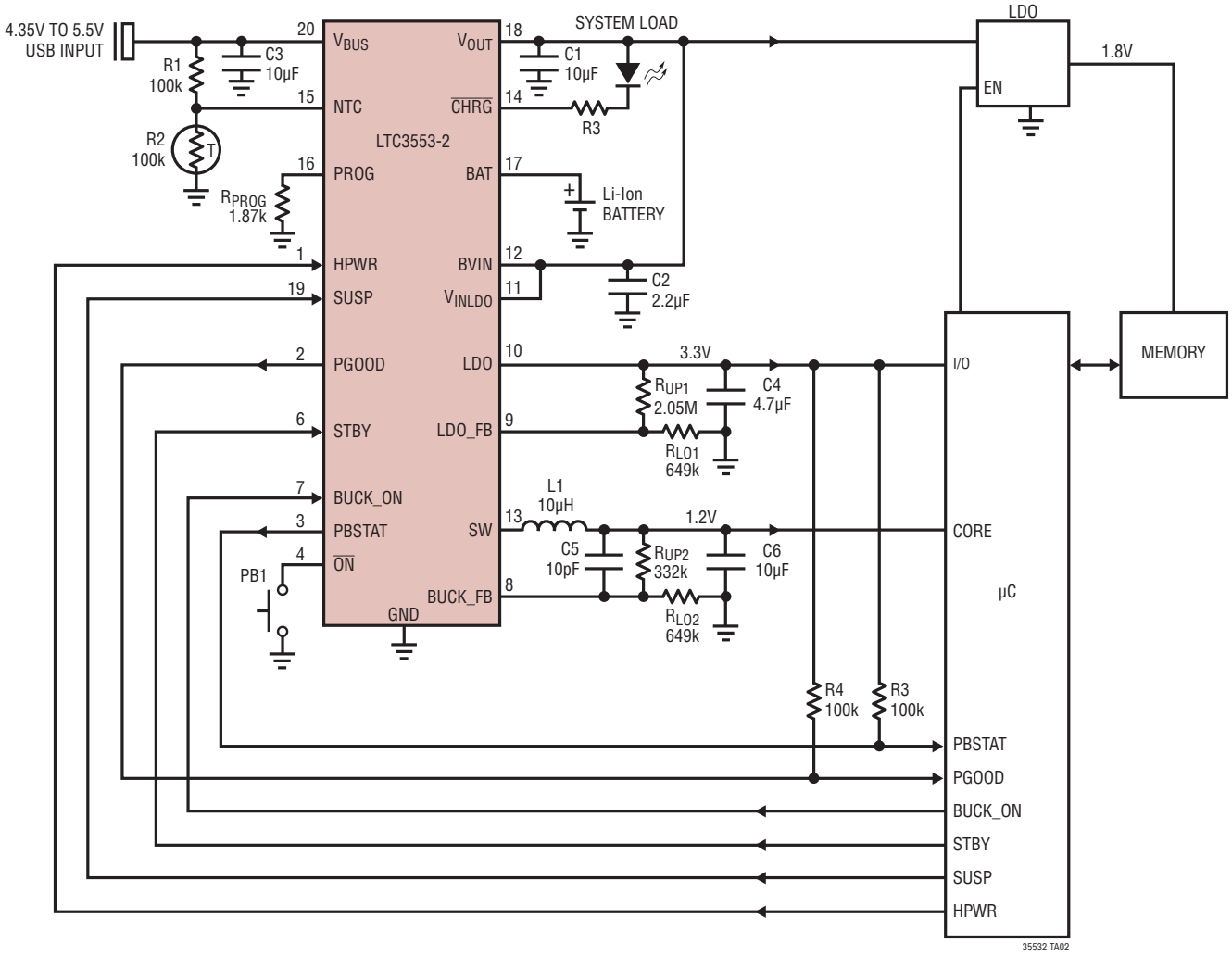
Printed Circuit Board Layout

When laying out the printed circuit board, the following list should be followed to ensure proper operation of the LTC3553-2:

1. The Exposed Pad of the package (Pin 21) should connect directly to a large ground plane to minimize thermal and electrical impedance.
2. The traces connecting the regulator input supply pins (BVIN and V_{INLDO}) and their respective decoupling capacitors should be kept as short as possible. The GND side of each capacitor should connect directly to the ground plane of the part. This capacitor provides the AC current to the internal power MOSFETs and their drivers. It is important to minimize inductance from this capacitor to the pin of the LTC3553-2. Connect BVIN to V_{OUT} and V_{INLDO} to its input supply through short low impedance traces.
3. The switching power trace connecting the SW pin to its inductor should be minimized to reduce radiated EMI and parasitic coupling. Due to the large voltage swing of the switching node, sensitive nodes such as the feedback nodes should be kept far away or shielded from the switching nodes or poor performance could result.
4. Connections between the buck regulator inductor and its output capacitor should be kept as short as possible. The GND side of the output capacitor should connect directly to the thermal ground plane of the part.
5. Keep the feedback pin traces (BUCK_FB and LDO_FB) as short as possible. Minimize any parasitic capacitance between the feedback traces and any switching node (i.e., SW and logic signals). If necessary, shield the feedback nodes with a GND trace.
6. Connections between the LTC3553-2 PowerPath pins (V_{BUS} and V_{OUT}) and their respective decoupling capacitors should be kept as short as possible. The GND side of these capacitors should connect directly to the ground plane of the part.

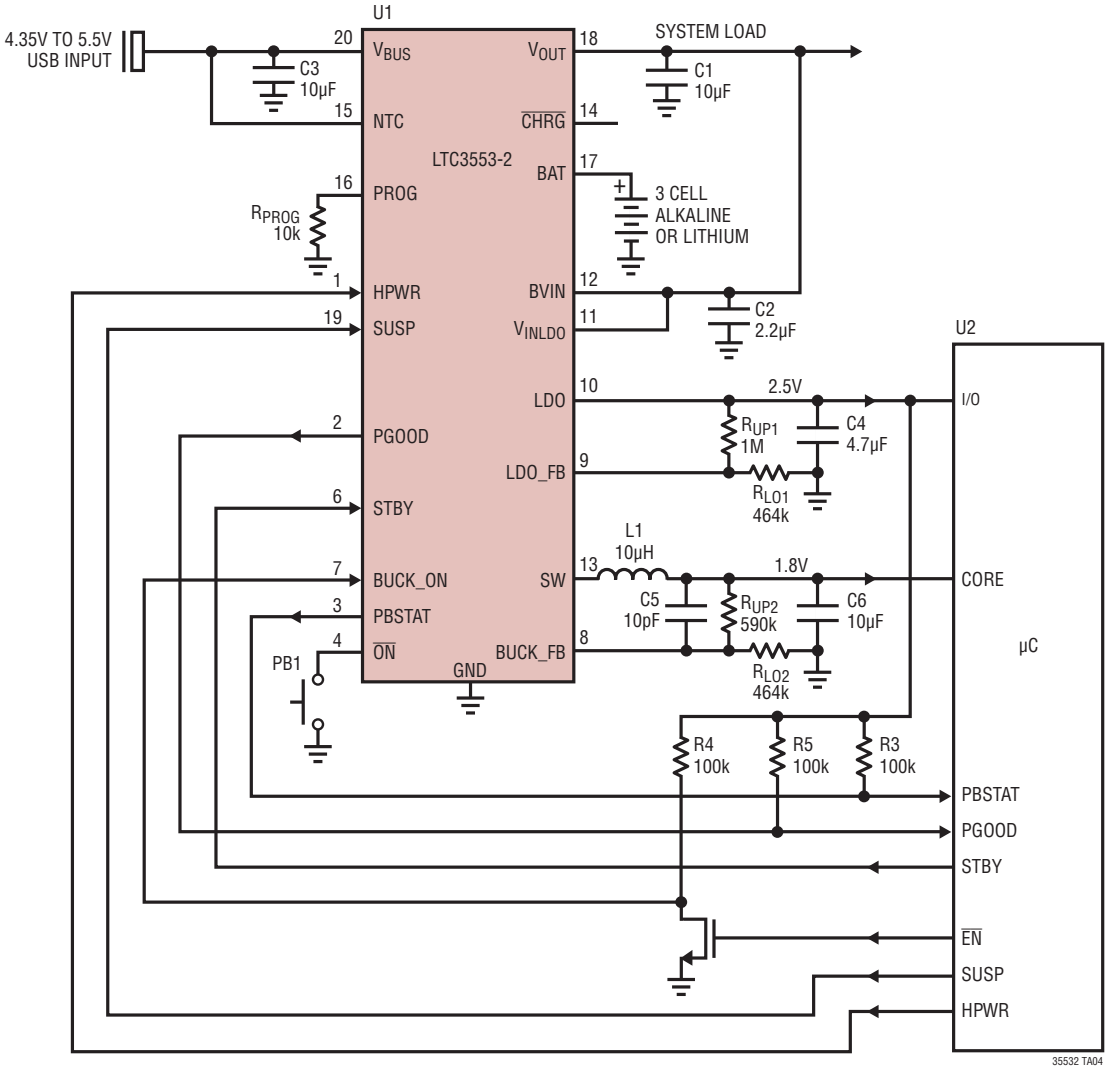
TYPICAL APPLICATIONS

USB PowerPath With Li-Ion Battery (NTC Qualified Charging)



TYPICAL APPLICATIONS

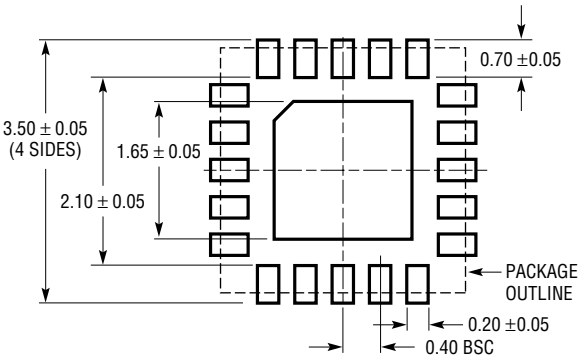
3-Cell Alkaline/Lithium With PowerPath (Charger Disabled)



PACKAGE DESCRIPTION

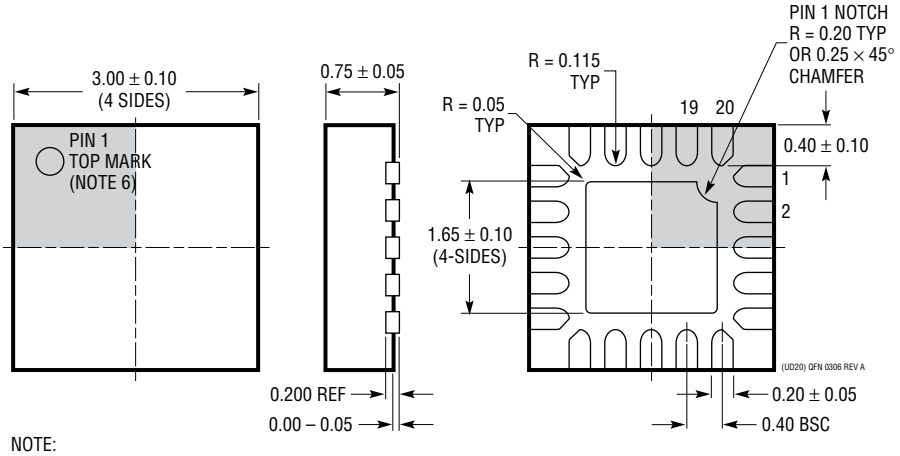
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UD Package
20-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1720 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE