Synchronous Step-Down DC/DC Controller with Differential Remote Sense and Nonlinear Control

FEATURES

- **V_{IN} Range: 4V to 38V**
- **V_{OUT} Range: 0.6V to 14V**
- **Nonlinear Control Architecture Minimizes Output Transient Excursions (Optional)**
- **Programmable DCR Temperature Compensation**
- **±0.75% 0.6V Voltage Reference**
- **Fixed Frequency Range of 200kHz to 1.2MHz**
- **PLL Frequency Synchronization**
- **R_{SENSE} or DCR Current Sensing**
- **Differential Remote Output Voltage Sense**
- Supports Smooth Start-Up into Pre-Biased Outputs
- Programmable Soft-Start or V_{OUT} Tracking
- Hiccup Mode/Soft Recovery from Output Overcurrent
- 24-Lead (4mm × 4mm) QFN Package

APPLICATIONS

- Automotive Systems
- Telecom Systems
- Industrial Equipment
- Distributed DC Power Systems

DESCRIPTION

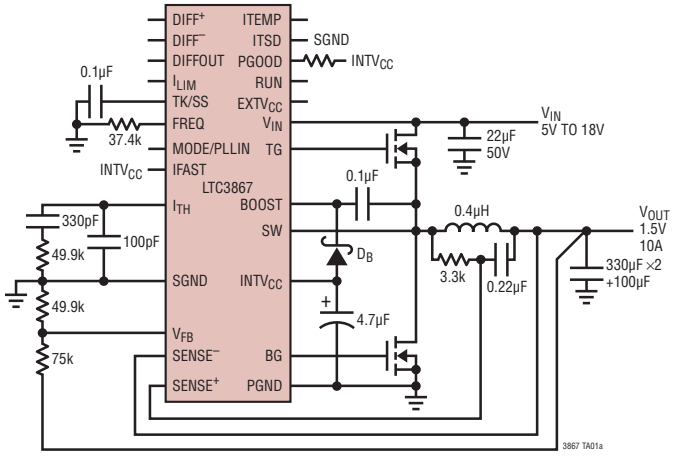
The LTC®3867 is a current mode synchronous step-down switching regulator controller that drives all N-channel power MOSFET stages. Output voltage transient excursions are minimized by use of a nonlinear control architecture to eliminate clock latency issues.

The maximum current sense voltage is programmable from 30mV to 75mV, allowing the use of either a discrete sense resistor or the inductor DCR as the sensing element. Programmable DCR temperature compensation allows constant current limit regardless of inductor temperature. Programmable inductor temperature-based thermal shutdown protects the power components from thermal stress. Soft recovery from output shorts or overcurrent minimizes output overshoot.

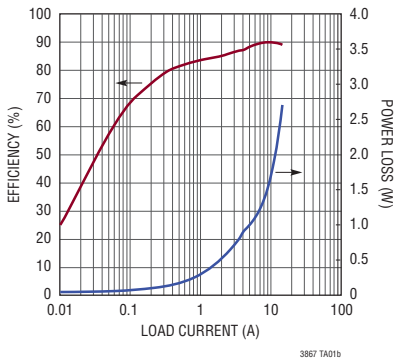
The LTC3867 features a precision 0.6V reference and can regulate output voltages up to 14V from a wide 4V to 38V input supply range. The LTC3867 includes a high speed differential remote sense amplifier. Burst Mode® operation, continuous and pulse-skipping modes are supported. The LTC3867 is available in a 24-lead (4mm × 4mm) QFN package.

TYPICAL APPLICATION

High Efficiency Synchronous Step-Down Controller



Efficiency and Power Loss

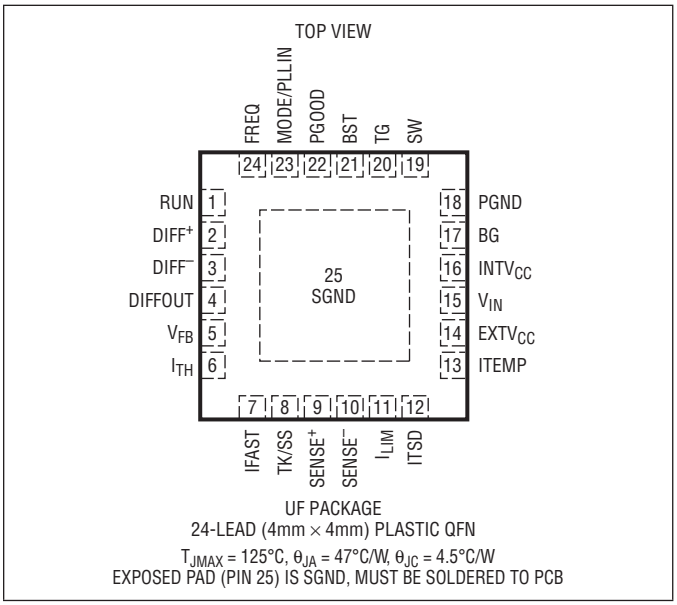


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage ..... –0.3V to 40V
BST Voltage..... –0.3V to 46V
SW Voltage..... –5V to 40V
(BST-SW) Voltage ..... –0.3V to 6V
RUN, PGOOD, $EXTV_{CC}$, $INTV_{CC}$ Voltage..... –0.3V to 6V
$SENSE^+$, $SENSE^-$ ..... –0.3V to 15V
$INTV_{CC}$ Peak Output Current..... 100mA
$DIFF^-$..... –0.3V to $INTV_{CC}$
All Other Pin Voltages Except TG, BG ..... –0.3V to $INTV_{CC}$
Operating Junction Temperature Range... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 47°C/W, θ_{JC} = 4.5°C/W
EXPOSED PAD (PIN 25) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3867EUF#PBF	LTC3867EUF#TRPBF	3867	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3867IUF#PBF	LTC3867IUF#TRPBF	3867	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 15V, V_{RUN} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop/Whole System							
V_{IN}	Input Voltage Range			4		38	V
V_{OUT}	Output Voltage Range			0.6		14	V
V_{FB}	Regulated Feedback Voltage	I_{TH} =1.2V, 0°C to 85°C I_{TH} =1.2V, –40°C to 125°C (Note 3)	 ●	595.5 594	600 600	604.5 606	mV mV
I_{FB}	Feedback Current				–15	–50	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{IN} = 4.5V to 38V			0.002	0.02	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	ΔI_{TH} =1.2V to 0.7V ΔI_{TH} =1.2V to 1.6V	● ●		0.01 –0.01	0.1 –0.1	% %
g_m	Transconductance Amplifier g_m	I_{TH} =1.2V, Sink/Source 5µA			2		mmho
V_{OVL}	Feedback Overvoltage Lockout	Measured at V_{FB}	●	5	7.5	10	%
I_Q	Input DC Supply Current Normal Mode Shutdown	 V_{RUN} = 0V (Note 4)			 3.5 30	 50	 mA µA
DF_{MAX}	Maximum Duty Factor	In Dropout, f_{SW} = 600kHz		96	98		%
UVLO	Undervoltage Lockout	V_{INTVCC} Falling		3.0	3.2	3.4	V
$UVLO_{HYS}$	UVLO Hysteresis				600		mV
I_{SENSE}	Sense Pin Bias Currents	V_{SENSE} = 3.3V	●		±1	±2	µA
I_{TEMP}	DCR Tempco Compensation Current	V_{ITEMP} = 500mV	●	27	30	33	µA
I_{FAST}	Fast Transient Programming Current	V_{IFAST} = 500mV	●	9	10	11	µA
$I_{TK/SS}$	Soft-Start Charge Current	$V_{TK/SS}$ = 0V		1	1.25	1.4	µA
V_{RUN}	RUN Pin On Threshold	V_{RUN} Rising	●	1.1	1.22	1.34	V
$V_{RUN(HYS)}$	RUN Pin On Hysteresis				80		mV
I_{RUN}	RUN Pin Pull-Up Current RUN < On Threshold RUN > On Threshold	 RUN < 1.1V RUN > 1.34V			 1 5		 µA µA
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	I_{TH} =1.85V, V_{SENSE} =3.3V I_{LIM} = 0V I_{LIM} = 1.5V I_{LIM} = Float I_{LIM} = 3.7V I_{LIM} = $INTV_{CC}$	 ● ● ● ● ●	 25 35 45 55 69	 30 40 50 60 75	 35 45 55 65 79	 mV mV mV mV mV
$t_{ON(MIN)}$	Minimum On-Time	(Note 6)			65		ns
Power Good							
$V_{PGOOD(ON)}$	PGOOD Pull-Down Resistance				90	200	Ω
$I_{PGOOD(OFF)}$	PGOOD Leakage Current	V_{PGOOD} = 5V		–2		2	µA
t_{PGOOD}	PGOOD Delay	V_{PGOOD} High to Low			45		µs
V_{PG1}	PGOOD Trip Level—with Delay	V_{FB} with Respect to Set Output Voltage V_{FB} Ramping Up V_{FB} Ramping Down	 	 5 –5	 7.5 –7.5	 10 –10	 % %

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 15V, V_{RUN} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{PG1(HYST)}$	PGOOD Trip Level Hysteresis				2		%
V_{PG2}	PGOOD 2nd Trip Level—No Delay	V_{FB} with Respect to Set Output Voltage V_{FB} Ramping Up V_{FB} Ramping Down			 17 –25		 % %
$V_{PG2(HYST)}$	PGOOD 2nd Trip Level Hysteresis				5		%
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Linear Regulator Voltage	6V < V_{IN} < 38V		5.1	5.3	5.5	V
V_{LDO} INT	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 20mA			0.5	2	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive		4.5	4.7		V
V_{LDO} EXT	$EXTV_{CC}$ Voltage Drop	I_{CC} = 20mA, V_{EXTVCC} = 5V			50	70	mV
$V_{LDO(HYS)}$	$EXTV_{CC}$ Hysteresis				200		mV
Differential Amplifier							
V_{DA}	DIFF+ Accuracy	Measured in a Servo Loop with EA in Loop I_{TH} =1.2V, 0°C to 85°C I_{TH} =1.2V, –40°C to 125°C	 ●	 595.5 594	 600 600	 604.5 606	 mV mV
I_{DIFF+}	Input Bias Current	DIFF+ to SGND		–200		200	nA
f_{0dB}	DA Unity-Gain Crossover Frequency	(Note 7)			4		MHz
$I_{OUT(SINK)}$	Maximum Sinking Current	DIFFOUT = 600mV			100		µA
$I_{OUT(SOURCE)}$	Maximum Sourcing Current	DIFFOUT = 600mV			500		µA
Oscillator and Phase-Locked Loop							
f_{OSC}	Oscillator Frequency	R_{FREQ} < 23.2kΩ R_{FREQ} = 30.1kΩ R_{FREQ} = 47.5kΩ R_{FREQ} = 54.9kΩ R_{FREQ} = 75.0kΩ Maximum Frequency Minimum Frequency		 1.2 	150 250 600 750 1.05 	 0.2	kHz kHz kHz kHz MHz MHz MHz
I_{FREQ}	FREQ Pin Output Current	V_{FREQ} = 0.8V		19	20	21	µA
$R_{MODE/PLLIN}$	MODE/PLLIN Input Resistance				250		kΩ
On-Chip Driver							
TG R_{UP}	TG Pull-Up $R_{DS(ON)}$	TG High			2.6		Ω
TG R_{DOWN}	TG Pull-Down $R_{DS(ON)}$	TG Low			1.5		Ω
BG R_{UP}	BG Pull-Up $R_{DS(ON)}$	BG High			2.4		Ω
BG R_{DOWN}	BG Pull-Down $R_{DS(ON)}$	BG Low			1.1		Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 15V, V_{RUN} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	TG Transition Time						
TG t_r	Rise Time	C_{LOAD} = 3300pF			25		ns
TG t_f	Fall Time	C_{LOAD} = 3300pF (Note 5)			25		ns
	BG Transition Time						
BG t_r	Rise Time	C_{LOAD} = 3300pF			25		ns
BG t_f	Fall Time	C_{LOAD} = 3300pF (Note 5)			25		ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay, Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			30		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay, Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			30		ns
Thermal Shutdown							
I_{ITSD}	Source Current	I_{ITSD} = 500mV			20		µA
V_{ITSD}	Comparator Trip Point				950		mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3867 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3867E is guaranteed to meet performance specifications from 0°C to 85°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3867I is guaranteed to meet performance specifications over the full –40°C to 125°C operating junction temperature range. The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the package thermal impedance and other environmental factors.

T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the following formula:

LTC3867UF: $T_J = T_A + (P_D \bullet 47°C/W)$

Note 3: The LTC3867 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}.

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

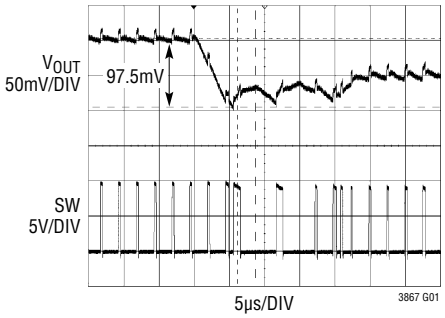
Note 5: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 6: The minimum on-time condition corresponds to the on inductor peak-to-peak ripple current ≥40% of I_{MAX} (see Minimum On-Time Considerations in the Applications Information section).

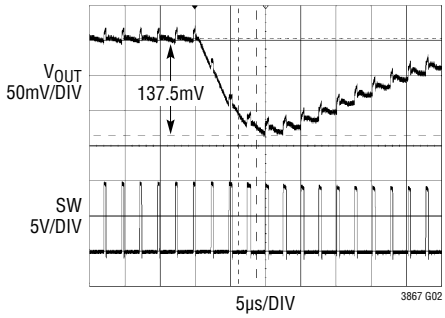
Note 7: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

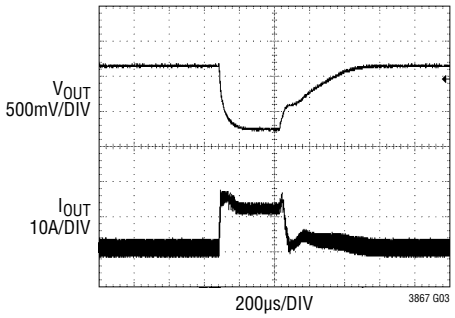
Load Step-Up (0A to 15A, 15A/µs) (Nonlinear Operation)



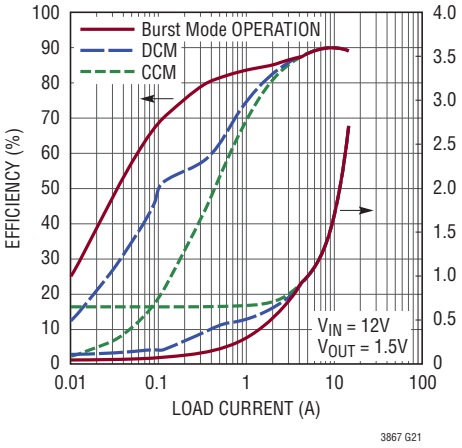
Load Step-Up (0A to 15A, 15A/µs) (Normal Operation)



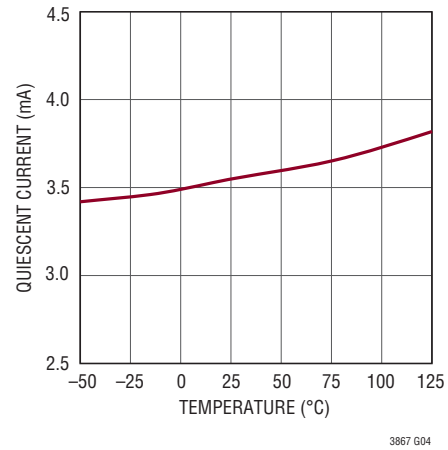
Overcurrent Recovery



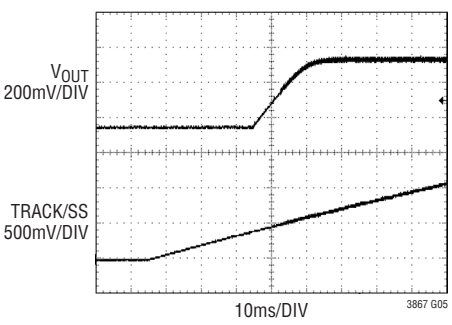
Efficiency and Output Current and Mode



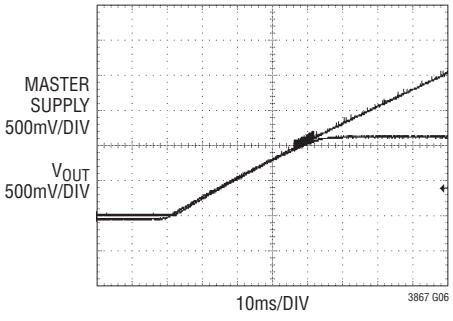
Quiescent Current vs Temperature



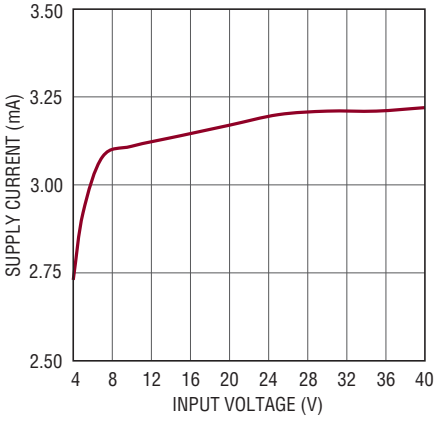
Pre-Bias Start-Up



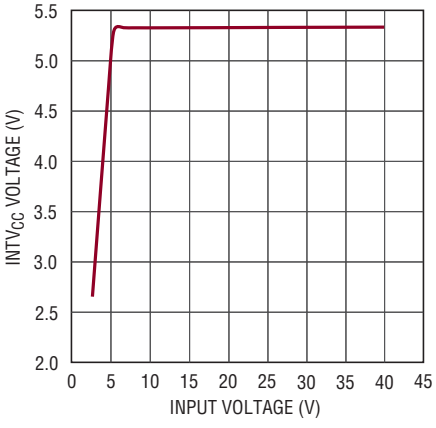
Coincident Tracking Master Supply



Quiescent Current vs Input Voltage without EXTVCC

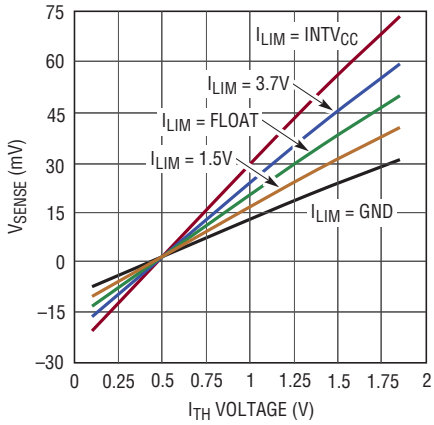


INTVCC Line Regulation



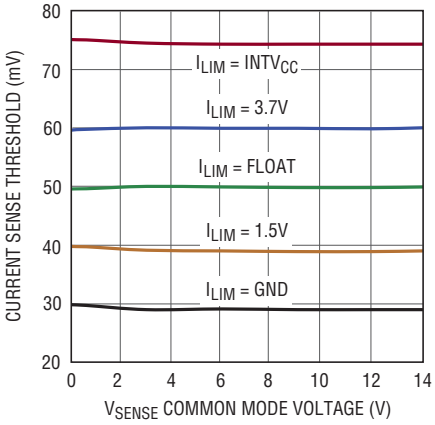
TYPICAL PERFORMANCE CHARACTERISTICS

Current Sense Threshold vs I_{TH} Voltage



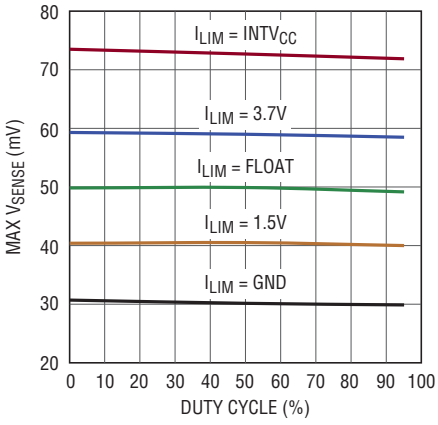
3867 G09

Maximum Current Sense Threshold vs Common Mode Voltage



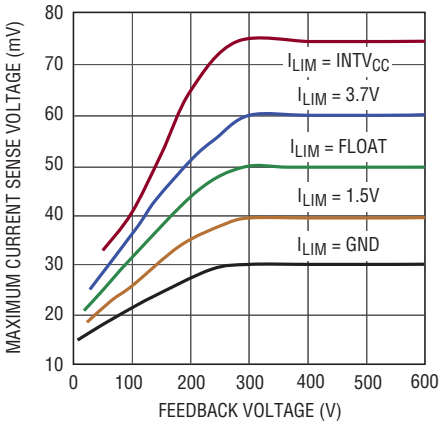
3867 G10

Maximum Current Sense Threshold vs Duty Cycle



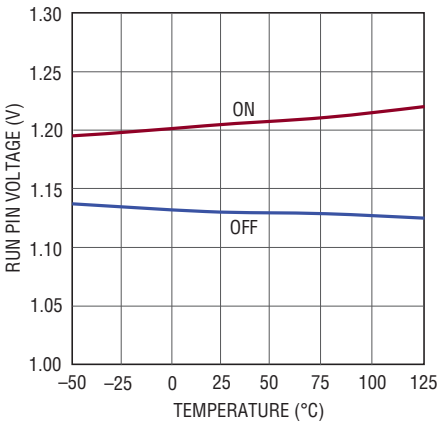
3867 G11

Maximum Current Sense Voltage vs Feedback Voltage (Current Foldback)



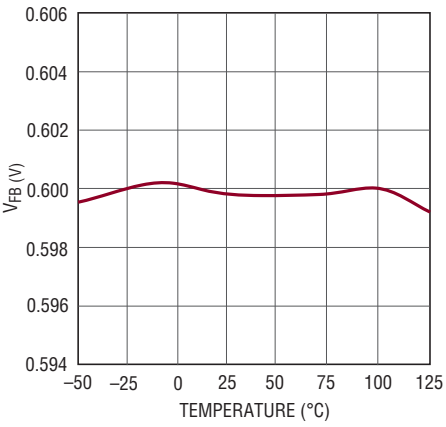
3867 G12

Shutdown (RUN) Threshold vs Temperature



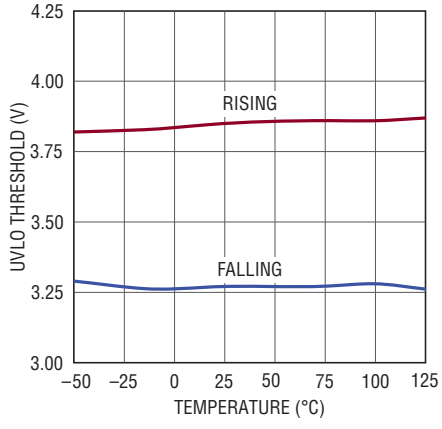
3867 G14

Regulated Feedback Voltage vs Temperature



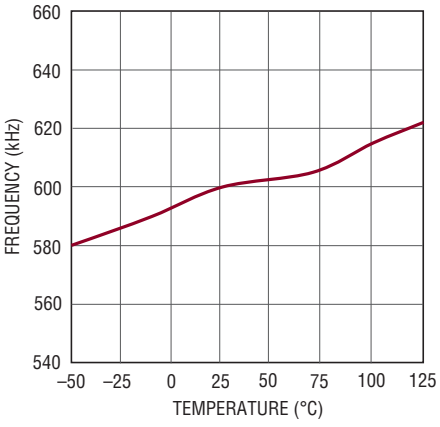
3867 G15

UVLO Threshold ($INTV_{CC}$) vs Temperature



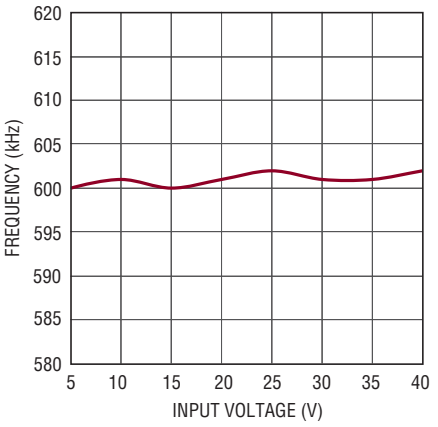
3867 G16

Oscillator Frequency vs Temperature



3867 G17

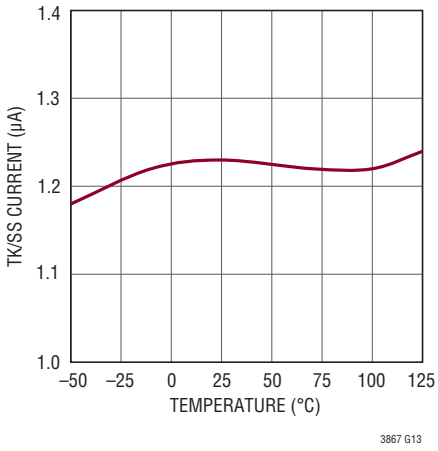
Oscillator Frequency vs Input Voltage



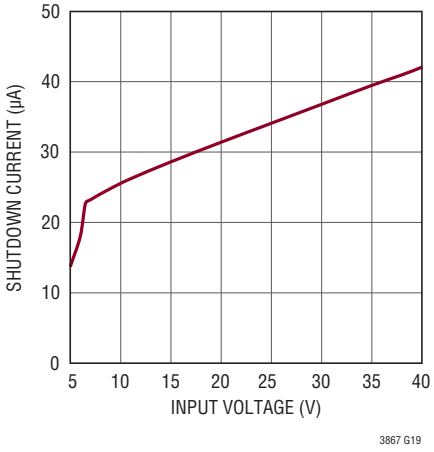
3867 G18

TYPICAL PERFORMANCE CHARACTERISTICS

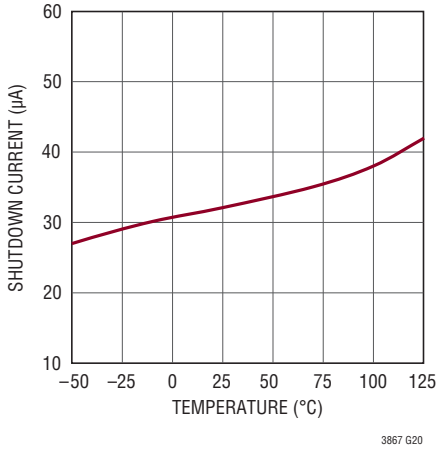
TK/SS Pull-Up Current vs Temperature



Shutdown Current vs Input Voltage



Shutdown Current vs Temperature



PIN FUNCTIONS

RUN (Pin 1): Run Control Input. A voltage above 1.22V turns on the IC. There is a 1µA pull-up current on this pin. Once the RUN pin rises above the 1.22V threshold the pull-up increases to 5µA.

DIFF$^+$ (Pin 2): Remote Sense Differential Amplifier Non-inverting Input. Connect to Feedback divider center tap with the divider across the output load.

DIFF$^-$ (Pin 3): Remote Sense Differential Amplifier Inverting Input. Connect to sense ground at the output load.

DIFFOUT (Pin 4): Differential Amplifier Output.

V_{FB} (Pin 5): Error Amplifier Inverting Input. Connect to DIFFOUT for remote V_{OUT} sensing.

I_{TH} (Pin 6): Current Control Thresholds and Error Amplifier Compensation Point. The current comparator's threshold increases with the I_{TH} control voltage.

IFAST (Pin 7): Programming Pin for Nonlinear Control Trip Threshold. A resistor to SGND programs the trip threshold for the nonlinear control circuit. Connect to $INTV_{CC}$ to disable this function.

TK/SS (Pin 8): Output Voltage Tracking and Soft-Start Input. The voltage ramp rate at this pin sets the voltage ramp rate of the output. A capacitor to ground accomplishes soft-start. This pin has a 1.25µA pull-up current.

SENSE$^+$ (Pin 9): Current Sense Comparator Input. The (+) input to the current comparator is normally connected to the midpoint of the inductor's parallel RC sense circuit or the inductor side of the current sensing resistor.

SENSE$^-$ (Pin 10): Current Sense Comparator Input. The (–) input to the current comparator is normally connected to V_{OUT}.

I_{LIM} (Pin 11): Current Comparator Sense Voltage Limit Selection Pin.

ITSD (Pin 12): Inductor Temperature-Based Thermal Shutdown. Sources a 20µA current. Use a Murata PRF18 series PTC to ground. Grounding this pin disables this function.

ITEMP (Pin 13): Input of the Temperature Sensing Comparators. Connect this pin to an external NTC resistor placed near the inductor. Floating this pin disables the DCR temperature compensation function.

$EXTV_{CC}$ (Pin 14): External Power Input to an Internal Switch Connected to $INTV_{CC}$. This switch closes and supplies the IC power, bypassing the internal 5.3V regulator, whenever $EXTV_{CC}$ is higher than 4.7V. Do not exceed 6V.

V_{IN} (Pin 15): Main Input Supply. Decouple this pin to PGND with a capacitor (0.1µF to 1µF)

PIN FUNCTIONS

$INTV_{CC}$ (Pin 16): Internal 5.3V Regulator Output and Bottom MOSFET Driver Supply. The control circuits are powered from this voltage. Decouple this pin to PGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor.

BG (Pin 17): Bottom Gate Driver Output. This pin drives the gate(s) of the bottom N-channel MOSFET(s) between PGND and $INTV_{CC}$.

PGND (Pin 18): Power Ground Pin. Connect this pin closely to the source(s) of the bottom N-channel MOSFET(s), the (–) terminal of C_{VCC} and (–) terminal of C_{IN}.

SW (Pin 19): Switch Node Connection to the Inductor. Voltage swing at this pin is from a Schottky diode (external) voltage drop below ground to V_{IN}.

TG (Pin 20): Top Gate Driver Output. This is the output of the floating driver with a voltage swing equal to $INTV_{CC}$ superimposed on the SW voltage.

BOOST (Pin 21): Boosted Floating Driver Supply. The (+) terminal of the bootstrap capacitor connects to this pin. This pin swings from a diode drop below $INTV_{CC}$ up to V_{IN} + $INTV_{CC}$.

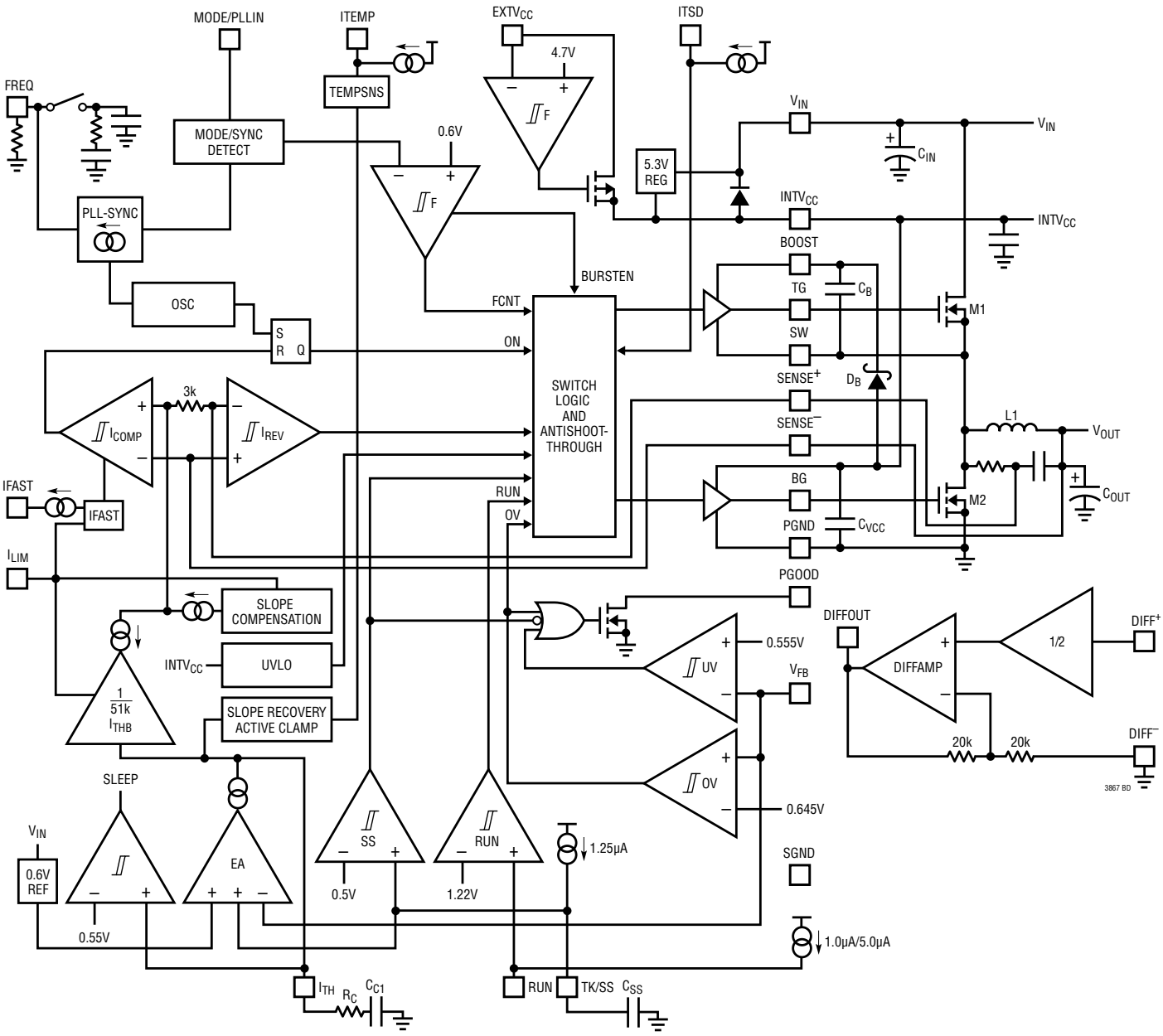
PGOOD (Pin 22): Power Good Indicator Output. Open-drain output that pulls to ground when output voltage is not in regulation.

MODE/PLLIN (Pin 23): This is a dual function pin. Tying this pin to SGND, $INTV_{CC}$ or floating it enables forced continuous mode, pulse-skipping mode or Burst Mode operation respectively. Applying a clock signal to this pin causes the internal PLL to synchronize the internal oscillator to the clock signal and forces forced continuous mode. The PLL compensation network is integrated on to the IC.

FREQ (Pin 24): Frequency Set/Select Pin. A resistor between this pin and SGND sets the switching frequency. This pin sources 20µA.

SGND (Exposed Pad Pin 25): Signal Ground. The exposed pad must be soldered to the PCB ground for electrical connection and rated thermal performance. All small-signal components and compensation components should be connected here. Connect to PGND at one point, close to the IC.

BLOCK DIAGRAM



OPERATION

Main Control Loop

The LTC3867 uses a constant frequency, current mode step-down architecture. During normal operation, the top MOSFET is turned on every cycle when the oscillator sets the RS latch, and turned off when the main current comparator, I_{CMP}, resets the RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier, EA. The remote sense amplifier (DIFFAMP) produces a signal equal to the differential voltage sensed across the output capacitor divided down by the feedback divider and re-references it to the local IC ground reference.

OPERATION

The V_{FB} pin receives this feedback signal and compares it to the internal 0.6V reference. When the load current increases, it causes a slight decrease in the V_{FB} pin voltage relative to the 0.6V reference, which in turn causes the I_{TH} voltage to increase until the inductor's average current equals the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the reverse current comparator, I_{REV}, or the beginning of the next cycle.

The main control loop is shut down by pulling the RUN pin low. Releasing RUN allows an internal 1.0µA current source to pull up the RUN pin. When the RUN pin reaches 1.22V, the main control loop is enabled and the IC is powered up. When the RUN pin is low, all functions are kept in a controlled state.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is left open or tied to a voltage less than 4.7V, an internal 5.3V linear regulator supplies $INTV_{CC}$ power from V_{IN}. If $EXTV_{CC}$ is taken above 4.7V, the 5.3V regulator is turned off and an internal switch is turned on connecting $EXTV_{CC}$ to $INTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as a switching regulator output. The top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during the off cycle through an external diode when the top MOSFET turns off. If the input voltage, V_{IN}, decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one-twelfth of the clock period plus 50ns every fifth cycle to allow C_B to recharge. However, it is recommended that a load be present or the IC operates at low frequency during the dropout transition to ensure C_B is recharged.

Internal Soft-Start

By default, the start-up of the output voltage is normally controlled by an internal soft-start ramp. The internal soft-start ramp represents a noninverting input to the error amplifier. The FB pin is regulated to the lower of the error amplifier's three noninverting inputs (the internal soft-start ramp, the TK/SS pin or the internal 600mV reference). As the ramp voltage rises from 0V to 0.6V over approximately 600µs, the output voltage rises smoothly from its prebiased value to its final set value.

Certain applications can result in the start-up of the converter into a non-zero load voltage, where residual charge is stored on the output capacitor at the onset of converter switching. In order to prevent the output from discharging under these conditions, the bottom MOSFET is disabled until soft-start is greater than V_{FB}.

Shutdown and Start-Up (RUN and TK/SS Pins)

The LTC3867 can be shut down using the RUN pin. Pulling the RUN pin below 1.22V shuts down the main control loop for the controller and most internal circuits, including the $INTV_{CC}$ regulator. Releasing the RUN pin allows an internal 1.0µA current to pull up the pin and enable the controller. Alternatively, the RUN pin may be externally pulled up or driven directly by logic. Be careful not to exceed the absolute maximum rating of 6V on this pin. The start-up of the controller's output voltage, V_{OUT}, is controlled by the voltage on the TK/SS pin. When the voltage on the TK/SS pin is less than the 0.6V internal reference, the LTC3867 regulates the V_{FB} voltage to the TK/SS pin voltage instead of the 0.6V reference. This allows the TK/SS pin to be used to program a soft-start by connecting an external capacitor from the TK/SS pin to SGND. An internal 1.25µA pull-up current charges this capacitor, creating a voltage ramp on the TK/SS pin. As the TK/SS voltage rises linearly from 0V to 0.6V (and beyond), the output voltage, V_{OUT}, rises smoothly from zero to its final value. Alternatively, the TK/SS pin can be used to cause the start-up of V_{OUT} to *track* that of another supply. Typically, this requires connecting to the TK/SS pin an external resistor divider from the other supply to ground (see the Applications Information section). When the RUN pin is pulled low to disable the controller, or when $INTV_{CC}$ drops below its undervoltage lockout threshold of 3.2V, the TK/SS pin is pulled low by an internal MOSFET. When in undervoltage lockout, the controller is disabled and the external MOSFETs are held off.

OPERATION

Light Load Current Operation (Burst Mode Operation, Pulse-Skipping or Continuous Conduction)

The LTC3867 can be enabled to enter high efficiency Burst Mode operation, constant-frequency pulse-skipping mode or forced continuous conduction mode. To select forced continuous operation, tie the MODE pin to SGND. To select pulse-skipping mode of operation, tie the MODE/PLLIN pin to $INTV_{CC}$. To select Burst Mode operation, float the MODE/PLLIN pin. When the controller is enabled for Burst Mode operation, the peak current in the inductor is set to approximately one-third of the maximum sense voltage even though the voltage on the I_{TH} pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier, EA, will decrease the voltage on the I_{TH} pin. When the I_{TH} voltage drops below 0.5V, the internal sleep signal goes high (enabling "sleep" mode) and both external MOSFETs are turned off.

In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator. When the controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (I_{REV}) turns off the bottom external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous mode has the advantages of lower output ripple and less interference with audio circuitry.

When the MODE/PLLIN pin is connected to $INTV_{CC}$, the LTC3867 operates in PWM pulse skipping mode at light loads. At very light loads, the current comparator, I_{CMP}, may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Frequency Selection and Phase-Locked Loop (FREQ and MODE/PLLIN Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

If the MODE/PLLIN pin is not being driven by an external clock source, the FREQ pin can be used to program the controller's operating frequency from 200kHz to 1.2MHz. There is a precision 20µA current flowing out of the FREQ pin so that the user can program the controller's switching frequency with a single resistor to SGND. A curve is provided later in the Applications Information section showing the relationship between the voltage on the FREQ pin and switching frequency.

A phase-locked loop (PLL) is available on the LTC3867 to synchronize the internal oscillator to an external clock source that is connected to the MODE/PLLIN pin. The PLL loop filter network is integrated inside the LTC3867. The phase-locked loop is capable of locking any frequency within the range of 250kHz to 1.1MHz. The frequency setting resistor should always be present to set the controller's initial switching frequency before locking to the external clock. The controller operates in forced continuous mode when it is synchronized.

Sensing the Output Voltage with a Differential Amplifier

The LTC3867 includes a low offset, high input impedance, unity-gain, high bandwidth differential amplifier for applications that require true remote sensing. Sensing the

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load across the load capacitors directly greatly benefits regulation in high current, low voltage applications, where board interconnection losses can be a significant portion of the total error budget. Connect DIFF$^+$ to the center tap of the feedback divider across the output load, and DIFF$^-$ to the load ground. See Figure 1

The LTC3867 differential amplifier has a typical output slew rate of 2V/µs. The amplifier is configured for unity gain, meaning that the difference between DIFF$^+$ and DIFF$^-$ is translated to DIFFOUT, relative to SGND.

Care should be taken to route the DIFF$^+$ and DIFF$^-$ PCB traces parallel to each other all the way to the remote sensing points on the board. In addition, avoid routing these sensitive traces near any high speed switching nodes in the circuit. Ideally, the DIFF$^+$ and DIFF$^-$ traces should be shielded by a low impedance ground plane to maintain signal integrity.

Power Good (PGOOD Pin)

The PGOOD pin is connected to the open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the V_{FB} pin voltage is not within ±7.5% of the 0.6V reference voltage. The PGOOD pin is also pulled low when the RUN pin is below 1.22V or when the LTC3867 is in the soft-start or tracking up phase. When the V_{FB} pin voltage is within the ±7.5% regulation window, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source of up to 6V. The PGOOD pin will flag power good immediately when the V_{FB} pin is within the regulation window. However, there is an internal 45µs power-bad mask when the V_{FB} goes out of the window. There is a second set of thresholds set at 17% and –25% that bypass this delay.

Output Overvoltage Protection

An overvoltage comparator, OV, guards against transient overshoots (>7.5%) as well as other more serious conditions that may overvoltage the output. In such cases, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Undervoltage Lockout

The LTC3867 has two functions that help protect the controller in case of undervoltage conditions. A precision UVLO comparator constantly monitors the $INTV_{CC}$ voltage to ensure that an adequate gate-drive voltage is present. It locks out the switching action when $INTV_{CC}$ is below 3.2V. To prevent oscillation when there is a disturbance on the $INTV_{CC}$, the UVLO comparator has 600mV of precision hysteresis.

Another way to detect an undervoltage condition is to monitor the V_{IN} supply. Because the RUN pin has a precision turn-on reference of 1.22V, one can use a resistor divider to V_{IN} to turn on the IC when V_{IN} is high enough. An extra 4µA of current flows out of the RUN pin once the RUN pin voltage passes 1.22V. The RUN comparator itself has about 80mV of hysteresis. One can program additional hysteresis for the RUN comparator by adjusting the values of the resistive divider. For accurate V_{IN} undervoltage detection, V_{IN} needs to be higher than 4.5V.

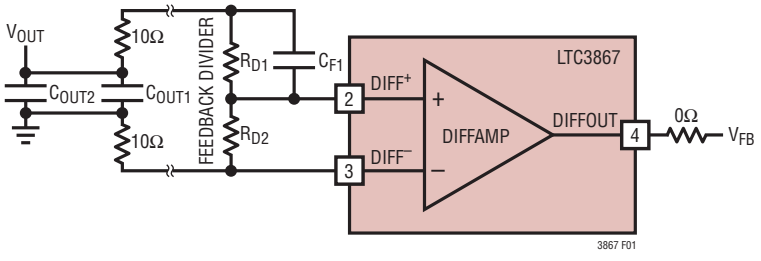

Figure 1. Differential Amplifier Connection

APPLICATIONS INFORMATION

The Typical Application on the first page of this data sheet is a basic LTC3867 application circuit. The LTC3867 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs are selected. Finally, input and output capacitors are selected.

Current Limit Programming

The I_{LIM} pin is a 5-level logic input which sets the maximum current limit of the controller. When I_{LIM} is either grounded, floated or tied to $INTV_{CC}$, the typical value for the maximum current sense threshold will be 30mV, 50mV or 75mV, respectively. Set I_{LIM} between 1.1V and 1.9V (typically 1.5V) for a 40mV maximum current sense threshold. For the 60mV setting, set I_{LIM} between 3.3V and 4.1V, typically 3.7V. These numbers are relative to a 5.3V $INTV_{CC}$. Setting I_{LIM} using a resistor divider off of $INTV_{CC}$ will allow the maximum current sense threshold setting to not change when the 5.3V LDO is in dropout at start-up. Please note that the I_{LIM} pin has an internal 500k pull-down to SGND and a 500k pull-up to $INTV_{CC}$.

Which setting should be used? For the best current limit accuracy, use the 75mV setting. The 30mV setting will allow for the use of very low DCR inductors or sense resistors, but at the expense of current limit accuracy.

SENSE+ and SENSE– Pins

The $SENSE^+$ and $SENSE^-$ pins are the inputs to the current comparators. The common mode input voltage range of the current comparators is 0V to 14V. All SENSE pins are high impedance inputs with small currents of less than 1µA. The high impedance inputs to the current comparators allow accurate DCR sensing. The $SENSE^-$ pin should be connected to V_{OUT} directly when DCR sensing is used. Care must be taken not to float these pins during normal operation. Filter components mutual to the sense lines should be placed close to the LTC3867, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 2). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 3b), resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes. The capacitor C1 should be placed close to the IC pins.

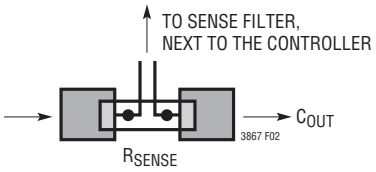

Figure 2. Sense Lines Placement with Sense Resistor

Low Value Resistors Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 3a. R_{SENSE} is chosen based on the required output current. The current comparator has a maximum threshold $V_{SENSE(MAX)}$ determined by the I_{LIM} setting. The input common mode range of the current comparator is 0V to 14V. The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

Because of possible PCB noise in the current sensing loop, the AC current sensing ripple of $\Delta V_{SENSE} = \Delta I_L \bullet R_{SENSE}$ also needs to be checked in the design to get a good signal-to-noise ratio. In general, for a reasonably good PCB layout, a 10mV ΔV_{SENSE} voltage is recommended as a conservative number to start with, either for R_{SENSE} or DCR sensing applications. For previous generation current mode controllers, the maximum sense voltage was high enough (e.g., 75mV for the LTC1628/LTC3728 family) that the voltage drop across the parasitic inductance of

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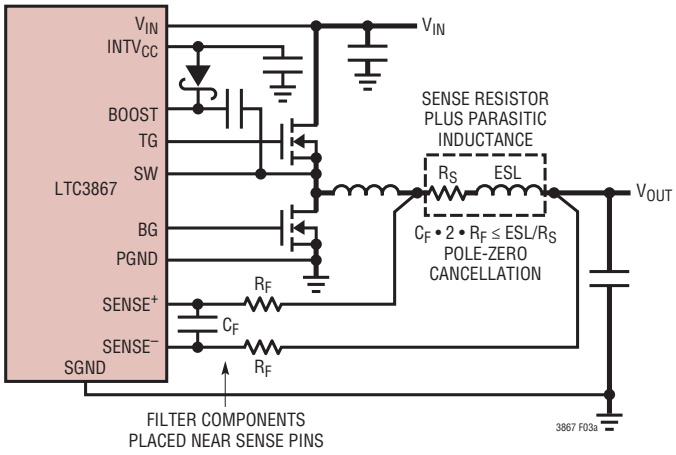
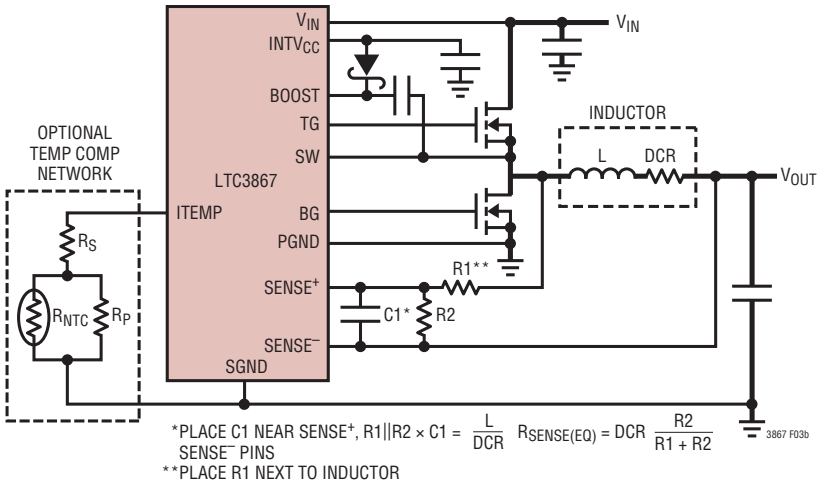


(3a) Using a Resistor to Sense Current



(3b) Using the Inductor DCR to Sense Current

Figure 3. Two Different Methods of Sensing Current

the sense resistor represented a relatively small error. For today's highest current density solutions, however, the value of the sense resistor can be less than 1mΩ and the peak sense voltage can be as low as 20mV. In addition, inductor ripple currents greater than 50% with operation up to 1MHz are becoming more common. Under these conditions the voltage drop across the sense resistor's parasitic inductance is no longer negligible.

In previous generations of controllers, a small RC filter placed near the IC was commonly used to reduce the effects of capacitive and inductive noise coupled in the sense traces on the PCB. A typical filter consists of two series 10Ω resistors connected to a parallel 1000pF capacitor, resulting in a time constant of 20ns. This same RC filter, with minor modifications, can be used to extract the resistive component of the current sense signal in the presence of parasitic inductance. For example, Figure 4 illustrates the voltage waveform across a 2mΩ sense resistor with a 2010 footprint for a 1.2V/15A converter operating at 100% load. The waveform is the superposition of a purely resistive component and a purely inductive component. It was measured using two scope probes and waveform math to obtain a differential measurement. Based on additional measurements of the inductor ripple current and the on-time and off-time of the top switch, the value

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of the parasitic inductance was determined to be 0.5nH using the equation:

$$ESL = \frac{V_{ESL(STEP)}}{\Delta I_L} \frac{t_{ON} \bullet t_{OFF}}{t_{ON} + t_{OFF}} \quad (1)$$

If the RC time constant is chosen to be close to the parasitic inductance divided by the sense resistor (L/R), the resulting waveform looks resistive again, as shown in Figure 5. For applications using low maximum sense voltages, check the sense resistor manufacturer's data sheet for information about parasitic inductance. In the absence of data, measure the voltage drop directly across the sense resistor to extract the magnitude of the ESL step and use Equation 1 to determine the ESL. However, do not overfilter. Keep the RC time constant, less than or equal to the inductor time constant to maintain a high enough ripple voltage of ΔV_{SENSE}. The above generally applies to high density/high current applications where I_{MAX} > 10A and low values of inductors are used. For applications where I_{MAX} < 10A, set R_F to 10Ω and C_F to 1000pF. This will provide a good starting point. The filter components need to be placed close to the IC. The positive and negative sense traces need to be routed as a differential pair and Kelvin connected to the sense resistor.

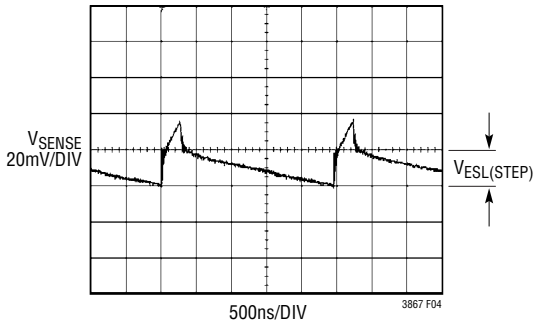

Figure 4. Voltage Waveform Measured Directly Across the Sense Resistor

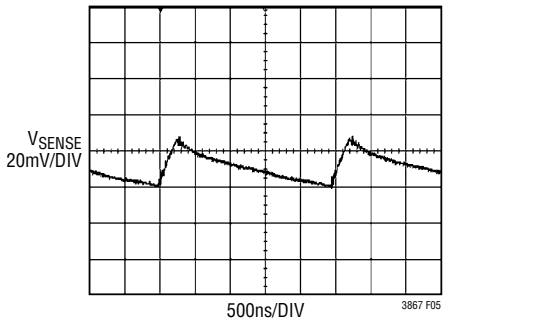

Figure 5. Voltage Waveform Measured After the Sense Resistor Filter. C_F = 1000pF, R_F = 100Ω

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC3867 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 3b. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, conduction loss through a sense resistor would cost several points of efficiency compared to DCR sensing. If the external R1|| R2 • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for the Maximum Current Sense Threshold ($V_{SENSE(MAX)}$) in the Electrical Characteristics table. Next, determine the DCR of the inductor. Where provided, use the manufacturer's maximum value, usually given at

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20°C. Increase this value to account for the temperature coefficient of resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C. To scale the maximum inductor DCR to the desired sense resistor value, use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{(MAX)} \text{ at } T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.047µF to 0.47µF. This forces R1|| R2 to around 2k, reducing error that might have been caused by the SENSE+ pin's ±1µA current. $T_{L(MAX)}$ is the maximum inductor temperature. The equivalent resistance R1|| R2 is scaled to the room temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR \text{ at } 20°C) \bullet C1}$$

The sense resistor values are:

$$R1 = \frac{R1||R2}{R_D},\ R2 = \frac{R1 \bullet R_D}{1 - R_D}$$

The LTC3867 also features a DCR temperature compensation circuit that uses an NTC temperature sensor. See the Inductor DCR Sensing Temperature Compensation section for details.

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}\ R1 = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \bullet V_{OUT}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method. To maintain a good signal-to-noise ratio for the current sense signal, use a minimum ΔV_{SENSE} of 10mV for duty cycles less than 40%. For a DCR sensing application, the actual ripple voltage will be determined by the equation:

$$\Delta V_{SENSE} = \frac{V_{IN} - V_{OUT}}{R1 \bullet C1} \frac{V_{OUT}}{V_{IN} \bullet f_{OSC}}$$

Inductor DCR Sensing Temperature Compensation and the ITEMP Pin

Inductor DCR current sensing provides a lossless method of sensing the instantaneous current. Therefore, it can provide higher efficiency for applications of high output currents. However, the DCR of the inductor, which is the small amount of DC winding resistance of the copper, typically has a positive temperature coefficient. As the temperature of the inductor rises, its DCR value increases. The current limit of the controller is therefore reduced.

The LTC3867 offers a method to counter this inaccuracy by allowing the user to place an NTC temperature sensing resistor near the inductor to actively correct this error. The ITEMP pin, when left floating, is at a voltage around 5V and DCR temperature compensation is disabled. The ITEMP pin has a constant 30µA precision current flowing out the pin. By connecting an NTC resistor from the ITEMP pin to SGND, the maximum current sense threshold can be varied over temperature according the following equation:

$$V_{SENSEMAX(ADJ)} = V_{SENSE(MAX)} \bullet \frac{1.8 - \frac{V_{ITEMP}}{2.8}}{1.3}$$

where:

$V_{SENSEMAX(ADJ)}$ is the maximum adjusted current sense threshold.

$V_{SENSE(MAX)}$ is the maximum current sense threshold specified in the Electrical Characteristics table. It is typically 75mV, 60mV, 50mV, 40mV or 30mV depending on the setting I_{LIM} pins.

V_{ITEMP} is the voltage of the ITEMP pin.

The valid voltage range for DCR temperature compensation on the ITEMP pin is 1.4V to 0.6V, with 1.4V or above being no DCR temperature correction and 0.6V the maximum correction. However, if the duty cycle of the controller is less than 25%, the ITEMP range is extended from 1.4V to 0V.

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The NTC resistor has a negative temperature coefficient, meaning its value decreases as temperature rises. The V_{ITEMP} voltage, therefore, decreases as temperature increases and in turn, the $V_{SENSEMAX(ADJ)}$ will increase to compensate the DCR temperature coefficient. The NTC resistor, however, is nonlinear and the user can linearize its value by building a resistor network with regular resistors. Consult the NTC manufacturer's data sheets for detailed information.

Another use for the ITEMP pins, in addition to NTC compensated DCR sensing, is adjusting $V_{SENSE(MAX)}$ to values between the nominal values of 30mV, 40mV, 50mV, 60mV and 75mV for a more precise current limit. This is done by applying a voltage less than 1.4V to the ITEMP pin. $V_{SENSE(MAX)}$ will be varied per the previous equation and the same duty cycle limitations will apply. The current limit can be adjusted using this method either with a sense resistor or DCR sensing.

NTC Compensated DCR Sensing

For DCR sensing applications where a more accurate current limit is required, a network consisting of an NTC thermistor placed from the ITEMP pin to ground will provide correction of the current limit over temperature. Figure 3b shows this network. Resistors R_S and R_P will linearize the impedance the ITEMP pin sees. To implement NTC compensated DCR sensing, design the DCR sense filter network per the same procedure mentioned in the previous selection, except calculate the divider components using the room temperature value of the DCR.

1. Set the ITEMP pin resistance to 46.7k at 25°C. With 30µA flowing out of the ITEMP pin, the voltage on the ITEMP pin will be 1.4V at room temperature. Current limit correction will occur for inductor temperatures greater than 25°C.
2. Calculate the ITEMP pin resistance and the maximum inductor temperature which is typically 100°C. Use the equations:

$$R_{ITEMP100C} = \frac{V_{ITEMP100C}}{30\mu A}$$

$$V_{ITEMP100C} = 1.4V - 3.64\frac{I_{MAX} \bullet DCR(MAX) \bullet R2/(R1+R2) \bullet (100°C - 25°C) \bullet 0.4/100}{V_{SENSE(MAX)}}$$

Calculate the values for R_P and R_S. A simple method is to graph the following R_S versus R_P equations with R_S on the y-axis and R_P on the x-axis.

$R_S = R_{ITEMP25C} - R_{NTC25C} \,||\, R_P$

$R_S = R_{ITEMP100C} - R_{NTC100C} \,||\, R_P$

Next, find the value of R_P that satisfies both equations which will be the point where the curves intersect. Once R_P is known, solve for R_S.

The resistance of the NTC thermistor can be obtained from the vendor's data sheet either in the form of graphs, tabulated data or formulas. The approximate value for the NTC thermistor for a given temperature can be calculated from the following equation:

$$R = R_0 \bullet \exp\left(B \bullet \left(\frac{1}{T+273} - \frac{1}{T_0+273}\right)\right)$$

where:

R = resistance at temperature T, which is in degrees C

R_0 = resistance at temperature T_0, typically 25°C

B = B-constant of the thermistor.

Figure 6 shows a typical resistance curve for a 100k thermistor and the ITEMP pin network over temperature.

Starting values for the NTC compensation network are listed below:

- NTC R_0 = 100k
- R_S = 20k
- R_P = 50k

But, the final values should be calculated using the above equations and checked at 25°C and 100°C.

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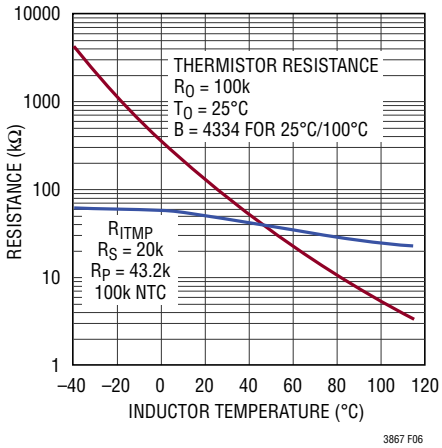

Figure 6. Resistance Versus Temperature for the ITEMP Pin Network and the 100k NTC

After determining the components for the temperature compensation network, check the results by plotting I_{MAX} versus inductor temperature using the following equations:

$$I_{MAX} = \frac{V_{SENSEMAX(ADJ)} - \Delta V_{SENSE}/2}{DCR(MAX) \text{ at } 25°C \bullet \left(1 + \left(T_{L(MAX)} - 25°C\right) \bullet 0.4/100\right)}$$

where:

$$V_{SENSEMAX(ADJ)} = V_{SENSE(MAX)} \bullet \frac{1.8V - \frac{V_{ITEMP}}{2.8}}{1.3} - A$$

$$V_{ITEMP} = 30\mu A \bullet \left(R_S + R_P \,||\, R_{NTC}\right)$$

Use typical values for $V_{SENSE(MAX)}$. Subtracting constant A will provide a minimum value for $V_{SENSE(MAX)}$. These values are summarized in Table 1.

Table 1

I_{LIM}	GND	FLOAT	$INTV_{CC}$
$V_{SENSE(MAX)}$ TYP	30mV	50mV	75mV
A	5mV	5mV	7mV

The resulting current limit should be greater than or equal to I_{MAX} for inductor temperatures between 25°C and 100°C.

These are typical values for the NTC compensation network:

- NTC R_0 = 100k, B-constant = 3000 to 4000
- $R_S \approx 20k$
- $R_P \approx 50k$

Generating the I_{MAX} versus inductor temperature curve plot first using the above values as a starting point and then adjusting the R_S and R_P values as necessary is another approach. Figure 7 shows a typical curve of I_{MAX} versus inductor temperature.

The same thermistor network can be used to correct for temperatures less than 25°C. But make sure V_{ITEMP} is greater than 0.6V for duty cycles of 25% or more, otherwise temperature correction may not occur at elevated ambients. For the most accurate temperature detection, place the thermistors next to the inductor as shown in Figure 8. Take care to keep the ITEMP pin away from the switch nodes.

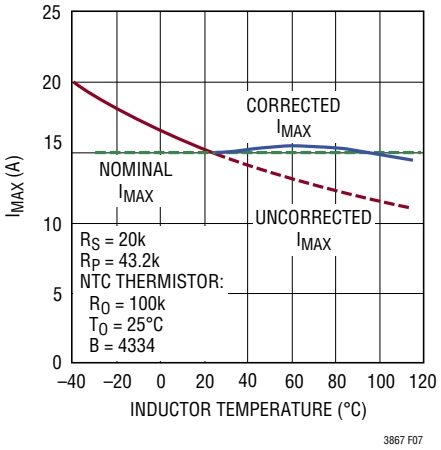

Figure 7. Worst-Case I_{MAX} Versus Inductor Temperature Curve with and without NTC Temperature Compensation

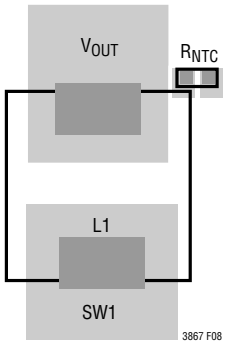

Figure 8. Thermistor Location. Place Thermistor Next to Inductor for Accurate Sensing of the Inductor Temperature, But Keep the ITEMP Pin Away from the Switch Nodes and Gate Drive Traces

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Pre-Biased Output Start-Up

There may be situations that require the power supply to start up with a pre-bias on the output capacitors. In this case, it is desirable to start up without discharging that output pre-bias. The LTC3867 can safely power up into a pre-biased output without discharging it.

The LTC3867 accomplishes this by disabling both TG and BG until the TK/SS pin voltage and the internal soft-start voltage are above the V_{FB} pin voltage. When V_{FB} is higher than TK/SS or the internal soft-start voltage, the error amp output is railed low. The control loop would like to turn BG on, which would discharge the output. Disabling BG and TG prevents the pre-biased output voltage from being discharged. When TK/SS and the internal soft-start both cross 500mV or V_{FB}, whichever is lower, TG and BG are enabled. If the pre-bias is higher than the OV threshold however, the bottom gate is turned on immediately to pull the output back into the regulation window.

Overcurrent Fault Recovery

When the output of the power supply is loaded beyond its preset current limit, the regulated output voltage will collapse depending on the load. The output may be shorted to ground through a very low impedance path or it may be a resistive short, in which case the output will collapse partially, until the load current equals the preset current limit. The controller will continue to source current into the short. The amount of current sourced depends on the I_{LIM} pin setting and the V_{FB} voltage as shown in the Current Foldback graph in the Typical Performance Characteristics section.

Upon removal of the short, the output soft starts using the internal soft-start, thus reducing output overshoot. In the absence of this feature, the output capacitors would have been charged at current limit, and in applications with minimal output capacitance this may have resulted in output overshoot. Current limit foldback is not disabled during an overcurrent recovery. The load must step below the folded back current limit threshold in order to restart from a hard short.

Thermal Protection

Excessive ambient temperatures, loads and inadequate airflow or heat sinking can subject the chip, inductor, FETs etc. to high temperatures. This thermal stress reduces component life and if severe enough, can result in immediate catastrophic failure. To protect the power supply from undue thermal stress, the LTC3867 has a fixed chip temperature-based thermal shutdown and an external inductor temperature-based thermal shutdown that is adjustable. The internal thermal shutdown is set for 160°C with 10°C of hysteresis. When the chip reaches 160°C, both TG and BG are disabled until the chip cools down below 150°C.

In addition, the ITSD pin sources 20µA of current. By placing a Murata PRF18 series PTC thermistor between this pin and ground, close to the inductor, the top and bottom FET can be turned off when the inductor reaches a pre-set temperature. The Murata PRF18 series PTC thermistors have a typical resistance of 470Ω at room temperature. Their temperature dependence is nonlinear. Over a fairly narrow temperature range, the resistance changes a few orders of magnitude. The LTC3867 trips when the PTC resistance is at about 47k. The PRF18 series includes thermistors with different trip points—select one based on the shutdown temperature desired. Please refer to the Murata data sheets for more details regarding the PRF18 series PTC thermistors.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency current mode architectures by preventing sub-harmonic oscillation at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, this results in a reduction of maximum inductor peak current for duty cycles greater than 40%. However, the LTC3867 uses a scheme that counteracts this compensating ramp, which allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

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Inductor Value Calculation

Given the desired input and output voltages, the inductor value and operating frequency, f_{OSC}, directly determine the inductor's peak-to-peak ripple current:

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN}} \left(\frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet L} \right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet I_{RIPPLE}} \bullet \frac{V_{OUT}}{V_{IN}}$$

Inductor Core Selection

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET and Schottky Diode (Optional) Selection

At least two external power MOSFETs need to be selected: One N-channel MOSFET for the top (main) switch and one or more N-channel MOSFET(s) for the bottom (synchronous) switch. The number, type and on-resistance of all MOSFETs selected take into account the voltage step-down ratio as well as the actual position (main or synchronous) in which the MOSFET will be used. A much smaller and much lower input capacitance MOSFET should be used for the top MOSFET in applications that have an output voltage that is less than 1/3 of the input voltage. In applications where $V_{IN} >> V_{OUT}$, the top MOSFETs' on-resistance is normally less important for overall efficiency than its input capacitance at operating frequencies above 300kHz. MOSFET manufacturers have designed special purpose devices that provide reasonably low on-resistance with significantly reduced input capacitance for the main switch application in switching regulators.

The peak-to-peak MOSFET gate drive levels are set by the voltage, V_{INTVCC}, requiring the use of logic-level threshold MOSFETs in most applications. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic-level MOSFETs are limited to 30V or less. Selection criteria for the power MOSFETs include the on-resistance, $R_{DS(ON)}$, input capacitance, input voltage and maximum output current. MOSFET input capacitance is a combination of several components but can be taken from the typical *gate charge* curve included on most data sheets (Figure 9). The curve is generated by forcing a constant input current into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time.

The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain drops the voltage

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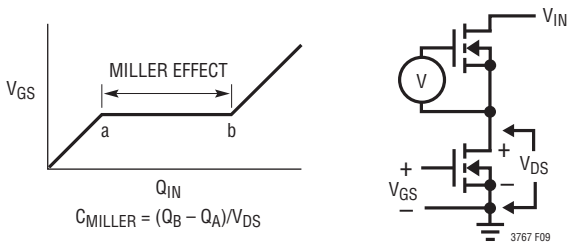

Figure 9. Gate Charge Characteristic

across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given V_{DS} drain voltage, but can be adjusted for different V_{DS} voltages by multiplying the ratio of the application V_{DS} to the curve specified V_{DS} values. A way to estimate the C_{MILLER} term is to take the change in gate charge from points a and b on a manufacturer's data sheet and divide by the stated V_{DS} voltage specified. C_{MILLER} is the most important selection criteria for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets. C_{RSS} and C_{OS} are specified sometimes but definitions of these parameters are not included. When the controller is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

The power dissipation for the main and synchronous MOSFETs at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet \left[\frac{1}{V_{INTVCC} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right]\bullet f$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$, R_{DR} is the effective top driver resistance (approximately 2Ω at $V_{GS} = V_{MILLER}$), V_{IN} is the drain potential and the change in drain potential in the particular application. $V_{TH(MIN)}$ is the data sheet specified typical gate threshold voltage specified in the power MOSFET data sheet at the specified drain current. C_{MILLER} is the calculated capacitance using the gate charge curve from the MOSFET data sheet and the technique described above.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which peak at the highest input voltage. For $V_{IN} < 20V$, the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

The optional Schottky diodes conduct during the dead time between the conduction of the two large power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead time and requiring a reverse-recovery period which could cost as much as several percent in efficiency. A 2A to 8A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition loss due to their larger junction capacitance.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[(V_{OUT})(V_{IN} - V_{OUT})\right]^{1/2}$$

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This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3867, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

Ceramic capacitors are becoming very popular for small designs but several cautions should be observed. X7R, X5R and Y5V are examples of a few of the ceramic materials used as the dielectric layer, and these different dielectrics have very different effect on the capacitance value due to the voltage and temperature conditions applied. Physically, if the capacitance value changes due to applied voltage change, there is a concommitant piezo effect which results in radiating sound! A load that draws varying current at an audible rate may cause an attendant varying input voltage on a ceramic capacitor, resulting in an audible signal. A secondary issue relates to the energy flowing back into a ceramic capacitor whose capacitance value is being reduced by the increasing charge. The voltage can increase at a considerably higher rate than the constant current being supplied because the capacitance value is decreasing as the voltage is increasing! Nevertheless, ceramic capacitors, when properly selected and used, can provide the lowest overall loss due to their extremely low ESR.

A small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC3867, is also suggested. A 2.2Ω to 10Ω resistor placed between C_{IN} (C1) and V_{IN} pin provides further isolation.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically once the ESR requirement is satisfied the capacitance is adequate for filtering. The steady-state output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_{RIPPLE}\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_{RIPPLE} = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_{RIPPLE} increases with input voltage. The output ripple will be less than 50mV at maximum V_{IN} with $\Delta I_{RIPPLE} = 0.4I_{OUT(MAX)}$ assuming:

C_{OUT} required ESR < N • R_{SENSE}

and

$$C_{OUT} > \frac{1}{(8f)(R_{SENSE})}$$

The emergence of very low ESR capacitors in small, surface mount packages makes very small physical implementations possible. The ability to externally compensate the switching regulator loop using the I_{TH} pin allows a much wider selection of output capacitor types. The impedance characteristic of each capacitor type is significantly different than an ideal capacitor and therefore requires accurate modeling or bench evaluation during design. Manufacturers such as Nichicon, Nippon Chemi-Con and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitors available from Sanyo and the Panasonic SP surface mount types have a good (ESR)(size) product.

Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. Ceramic capacitors from AVX, Taiyo Yuden, Murata and Tokin offer high capacitance value and very low ESR, especially applicable for low output voltage applications.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer surface mount capacitors offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent choices are the AVX TPS, AVX TPSV, the KEMET T510 series of surface mount tantalums or the Panasonic

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SP series of surface mount special polymer capacitors available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo POSCAP, Sanyo OS-CON, Nichicon PL series and Sprague 595D series. Consult the manufacturers for other specific recommendations.

Differential Amplifier

The LTC3867 has true remote voltage sense capability. The sensing connections should be returned from the load, back to the differential amplifier's inputs through a common, tightly coupled pair of PC traces. The differential amplifier rejects common mode signals capacitively or inductively radiated into the feedback PC traces as well as ground loop disturbances. The LTC3867 diffamp has high input impedance on $DIFF^+$. It is designed to be used with a feedback divider Kelvined to the load. The output of the diffamp connects to the V_{FB} pin.

Nonlinear Control Loop

The LTC3867 features a unique control loop that can speed up transient response dramatically. This feature is enabled and programmed through the IFAST pin. When IFAST is tied to $INTV_{CC}$, the nonlinear control loop is disabled. V_{IFAST} is the voltage that can be programmed on the IFAST pin. There is a precision 10µA flowing out of the IFAST pin. Connecting a resistor to SGND sets the V_{IFAST} voltage. When V_{IFAST} is set below 1.4V, the difference of 1.4V and V_{IFAST} sets the threshold voltage that triggers nonlinear control. Nonlinear control is only enabled when V_{FB} is within the UV and OV window. It should be enabled only for forced continuous mode of operation.

Once nonlinear control is enabled, the top gate of all channels will turn on if:

$$V_{FB} = V_{REF} - \frac{1.4 - V_{IFAST}}{12.5}$$

where V_{REF} is the reference voltage, normally at 0.6V, and V_{FB} is the feedback voltage.

External Soft-Start and Tracking

The LTC3867 has the ability to either soft-start by itself or track the output of another channel or external supply. When the controller is configured to soft-start by itself, a capacitor may be connected to its TK/SS pin or the internal soft-start may be used. The controller is in the shutdown state if its RUN pin voltage is below 1.22V and its TK/SS pin is actively pulled to ground in this shutdown state. If the RUN pin voltage is above 1.22V, the controller powers up. A soft-start current of 1.25µA then starts to charge the TK/SS soft-start capacitor. Note that soft-start or tracking is achieved not by limiting the maximum output current of the controller but by controlling the output ramp voltage according to the ramp rate on the TK/SS pin. Current foldback is disabled during this phase to ensure smooth soft-start or tracking. The soft-start or tracking range is defined to be the voltage range from 0V to 0.6V on the TK/SS pin. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = 0.6 \bullet \frac{C_{SS}}{1.25\mu A}$$

Regardless of the mode selected by the MODE pin, the controller always starts in discontinuous mode up to TK/SS = 0.5V. Between TK/SS = 0.5V and 0.565V, it will operate in forced continuous mode and revert to the selected mode once TK/SS > 0.565V. The output ripple is minimized during the 65mV forced continuous mode window ensuring a clean PGOOD signal. When the channel is configured to track another supply, the feedback voltage of the other supply is duplicated by a resistor divider and applied to the TK/SS pin. Therefore, the voltage ramp rate on this pin is determined by the ramp rate of the other supply's voltage. It is only possible to track another supply that is slower than the internal soft-start ramp. Note that the small soft-start capacitor charging current is always flowing, producing a small offset error. To minimize this error, select the tracking resistive divider value to be small enough to make this error negligible. In order to track down another channel or supply after

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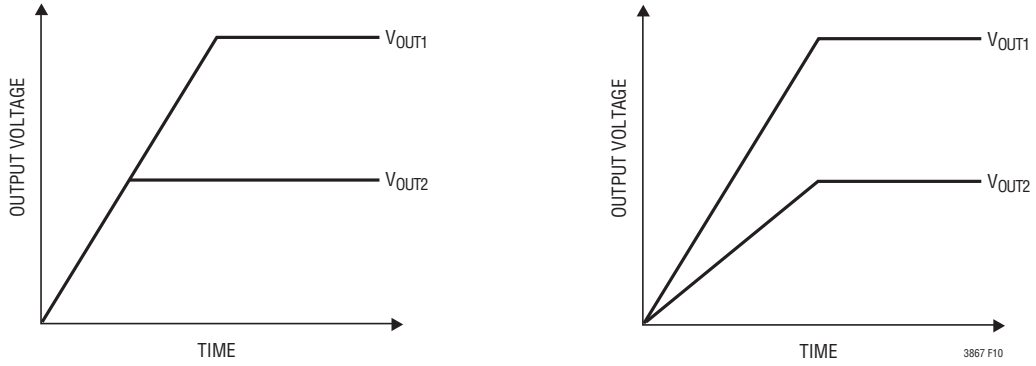
the soft-start phase expires, the LTC3867 is forced into continuous mode of operation as soon as V_{FB} is below the undervoltage threshold of 0.555V regardless of the setting on the MODE pin. However, the LTC3867 should always be set in forced continuous mode tracking down when there is no load. After TK/SS drops below 0.1V, the controller operates in discontinuous mode.

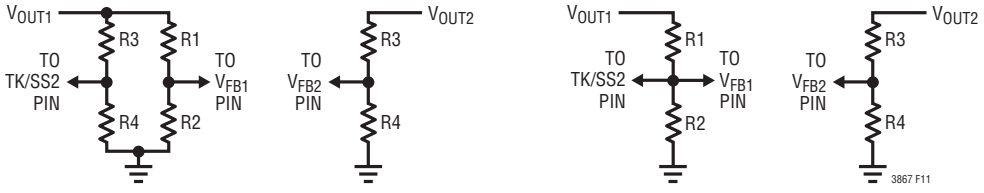
The LTC3867 allows the user to program how its output ramps up and down by means of the TK/SS pin. Through these pins, the output can be set up to either coincidentally or ratiometrically track another supply's output, as shown in Figure 10. In the following discussions, V_{OUT2} refers to the LTC3867's output as a slave and V_{OUT1} refers to another supply output as a master. To implement the coincident tracking in Figure 10a, connect an additional resistive divider to V_{OUT1} and connect its mid-point to the TK/SS pin of the slave controller. The ratio of this divider should be the same as that of the slave controller's feedback divider shown in Figure 11a. In this tracking mode, V_{OUT1} must be set higher than V_{OUT2}. To implement the ratiometric tracking in Figure 10b, the ratio of the V_{OUT2} divider should be exactly the same as the master controller's feedback divider shown in Figure 11b . By selecting different resistors, the LTC3867 can achieve different modes of tracking including the two in Figure 10.

So which mode should be programmed? While either mode in Figure 10 satisfies most practical applications, some trade-offs exist. The ratiometric mode saves a pair of resistors, but the coincident mode offers better output regulation. Under ratiometric tracking, when the master controller's output experiences dynamic excursion (under load transient, for example), the slave controller output will be affected as well. For better output regulation, use the coincident tracking mode instead of ratiometric.



(10a) Coincident Tracking **(10b) Ratiometric Tracking**

Figure 10. Two Different Modes of Output Voltage Tracking



(11a) Coincident Tracking Setup **(11b) Ratiometric Tracking Setup**

Figure 11. Setup and Coincident and Ratiometric Tracking

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$INTV_{CC}$ (LDO) and $EXTV_{CC}$

The LTC3867 features a true PMOS LDO that supplies power to $INTV_{CC}$ from the V_{IN} supply. $INTV_{CC}$ powers the gate drivers and much of the LTC3867's internal circuitry. The LDO regulates the voltage at the $INTV_{CC}$ pin to 5.3V when V_{IN} is greater than 5.8V. $EXTV_{CC}$ connects to $INTV_{CC}$ through a P-channel MOSFET and can supply the needed power when its voltage is higher than 4.7V. Either of these can supply a peak current of 100mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and PGND pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers. High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3867 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, may be supplied by either the 5.3V LDO or $EXTV_{CC}$. When the voltage on the $EXTV_{CC}$ pin is less than 4.5V, the LDO is enabled. Power dissipation for the IC in this case is highest and is equal to $V_{IN} \bullet I_{INTVCC}$. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics tables. For example, the LTC3867 $INTV_{CC}$ current is limited to less than 30mA from a 38V supply in the UF package and not using the $EXTV_{CC}$ supply with a 70°C ambient temperature:

$$T_J = 70°C + (30mA)(38V)(47°C/W) \cong 125°C$$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode (MODE = SGND) at maximum V_{IN}. When the voltage applied to $EXTV_{CC}$ rises above 4.7V, the $INTV_{CC}$ LDO is turned off and the $EXTV_{CC}$ is connected to the $INTV_{CC}$. The $EXTV_{CC}$ remains on as long as the voltage applied to $EXTV_{CC}$ remains above 4.5V. Using the $EXTV_{CC}$ allows the MOSFET driver and control power to be derived from an efficient switching regulator output during normal operation. If more current is required through the $EXTV_{CC}$ than is specified, an external Schottky diode can be added between the $EXTV_{CC}$ and $INTV_{CC}$ pins. Do not apply more than 6V to the $EXTV_{CC}$ pin and make sure that $EXTV_{CC} < V_{IN}$.

Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from $EXTV_{CC}$, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (duty cycle)/(switcher efficiency). Tying the $EXTV_{CC}$ pin to a 5V supply reduces the junction temperature in the previous example from 125°C to:

$$T_J = 70°C + (30mA)(5V)(47°C/W) = 77°C$$

However, for low voltage outputs, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from the internal LDO resulting in an efficiency penalty of up to 10% at high input voltages.
2. $EXTV_{CC}$ connected directly to V_{OUT}. This is the normal connection for a 5V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If a 5V external supply is available, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements.
4. $EXTV_{CC}$ connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 4.7V.

For applications where the main input power is 5V, tie the V_{IN} and $INTV_{CC}$ pins together and tie the combined pins to the 5V input with a 1Ω or 2.2Ω resistor as shown in Figure 12 to minimize the voltage drop caused by the gate charge current. This will override the $INTV_{CC}$ linear regulator and will prevent $INTV_{CC}$ from dropping too low due to the dropout voltage. Make sure the $INTV_{CC}$ voltage is at or exceeds the $R_{DS(ON)}$ test voltage for the MOSFET which is typically 4.5V for logic-level devices

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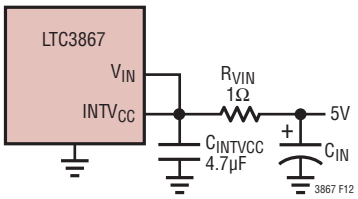


Figure 12. Setup for a 5V Input

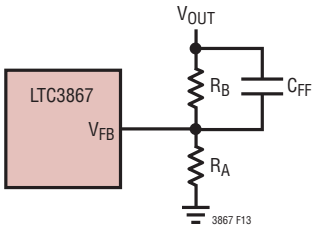


Figure 13. Setting Output Voltage

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitor, C_B, connected to the BOOST pin supplies the gate drive voltages for the topside MOSFET. Capacitor C_B in the Functional Diagram is charged though external diode D_B from $INTV_{CC}$ when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate source of the MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply:

$$V_{BOOST} = V_{IN} + V_{INTVCC} - V_{DB}$$

The value of the boost capacitor, C_B, needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Setting Output Voltage

The LTC3867 output voltage is set by an external feedback resistive divider carefully placed across the output, as shown in Figure 13. The regulated output voltage is determined by:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R_B}{R_A}\right)$$

To improve the frequency response, a feedforward capacitor, C_{FF}, may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

If the diffamp is used, then the resistor divider center tap should connect to the noninverting input of the diffamp, $DIFF^+$. DIFFOUT should then be shorted to V_{FB}.

Fault Conditions: Current Limit and Current Foldback

The LTC3867 includes current foldback to help limit load current when the output is shorted to ground. If the output falls below 50% of its nominal output level, then the maximum sense voltage is progressively lowered from its maximum programmed value to one-third of the maximum value. Foldback current limiting is disabled during the soft-start or tracking up using the TK/SS pin. It is not disabled for internal soft-start. Under short-circuit conditions with very low duty cycles, the LTC3867 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short circuit ripple current is determined by the minimum on-time $t_{ON(MIN)}$ of the LTC3867 (≈65ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \bullet \frac{V_{IN}}{L}$$

The resulting short-circuit current is:

$$I_{SC} = \left(\frac{1/3\, V_{SENSE(MAX)}}{R_{SENSE}} - \frac{1}{2}\Delta I_{L(SC)}\right)$$

After a short, or while starting with internal soft-start, make sure that the load current takes the folded-back current limit into account.

APPLICATIONS INFORMATION

Phase-Locked Loop and Frequency Synchronization

The LTC3867 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the turn-on of the top MOSFET to be locked to the rising edge of an external clock signal applied to the MODE/PLLIN pin. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. There is a precision 20µA current flowing out of the FREQ pin. This allows the user to use a single resistor to SGND to set the switching frequency when no external clock is applied to the MODE/PLLIN pin. The internal switch between the FREQ pin and the integrated PLL filter network is on, allowing the filter network to be pre-charged at the same voltage as of the FREQ pin. The relationship between the voltage on the FREQ pin and operating frequency is shown in Figure 14 and specified in the Electrical Characteristics table. If an external clock is detected on the MODE/PLLIN pin, the internal switch mentioned above turns off and isolates the influence of the FREQ pin. Note that the LTC3867 can only be synchronized to an external clock whose frequency is within range of the LTC3867's internal VCO. A simplified block diagram is shown in Figure 15.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the filter network. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the filter network. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the filter network is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor C_{LP} holds the voltage.

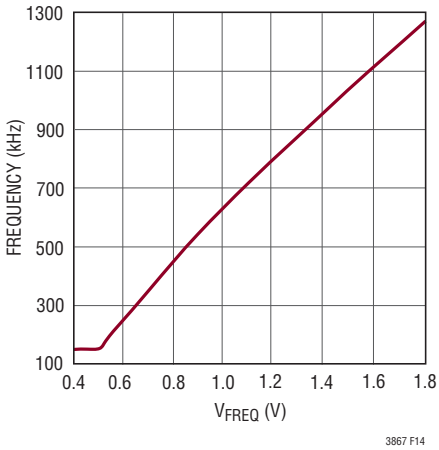


Figure 14. Relationship Between Oscillator Frequency and Voltage at the FREQ Pin

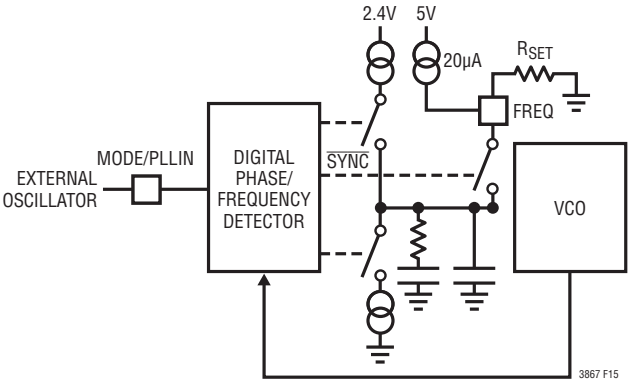


Figure 15. Phase-Locked Loop Block Diagram

Typically, the external clock (on the MODE/PLLIN pin) input high threshold is 1.6V, while the input low threshold is 1V.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC3867 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

APPLICATIONS INFORMATION

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the voltage ripple and current ripple will increase. The minimum on-time for the LTC3867 is approximately 65ns, with good PCB layout, minimum 30% inductor current ripple and at least 10mV ripple on the current sense signal. The minimum on-time can be affected by PCB switching noise in the voltage and current loop. As the peak sense voltage decreases the minimum on-time gradually increases to about 100ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3867 circuits: 1) IC V_{IN} current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. V_{IN} current typically results in a small (<0.1%) loss.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs. Supplying $INTV_{CC}$ power through $EXTV_{CC}$ from an output-derived source will scale the V_{IN} current required for the driver and control circuits by a factor of (duty cycle)/(efficiency). For example, in a 20V to 5V application, 10mA of $INTV_{CC}$ current results in approximately 2.5mA of V_{IN} current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor and current sense resistor. In continuous mode, the average output current flows through L and R_{SENSE}, but is *chopped* between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)} = 10m\Omega$, $R_L = 10m\Omega$, $R_{SENSE} = 5m\Omega$, then the total resistance is $25m\Omega$. This results in losses ranging from 2% to 8% as the output current increases from 3A to 15A for a 5V output, or a 3% to 12% loss for a 3.3V output.

   Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

APPLICATIONS INFORMATION

4. Transition losses apply only to the topside MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} = (1.7)\, V_{IN}^2 \bullet I_{O(MAX)} \bullet C_{RSS} \bullet f$$

Other *hidden* losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these *system* level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. Other losses including Schottky conduction losses during dead time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

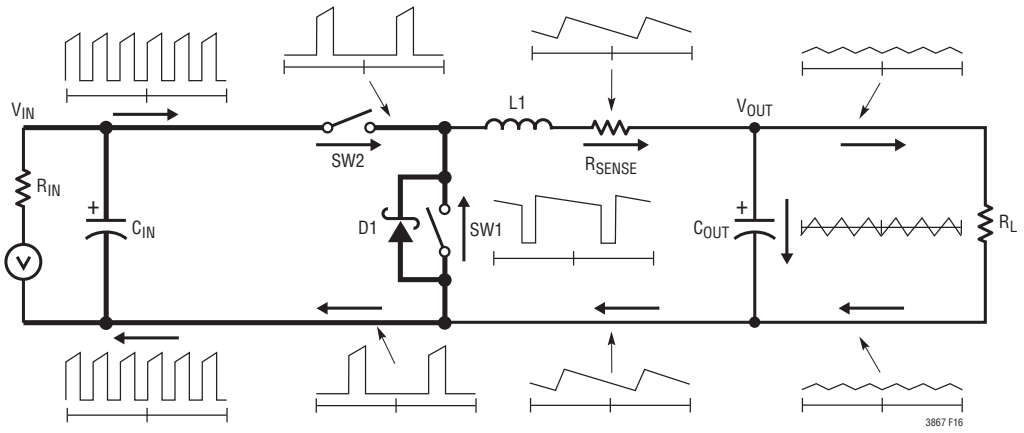
The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \bullet$ ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the I_{TH} pin not only allows optimization of control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in the Typical Application circuit will provide an adequate starting point for most applications. The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the I_{TH} pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately $25 \bullet C_{LOAD}$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

APPLICATIONS INFORMATION

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 16. Check the following in the PC layout:

1. The $INTV_{CC}$ decoupling capacitor should be placed immediately adjacent to the IC between the $INTV_{CC}$ pin and PGND plane. A 1µF ceramic capacitor of the X7R or X5R type is small enough to fit very close to the IC to minimize the ill effects of the large current pulses drawn to drive the bottom MOSFETs. An additional 4.7µF to 10µF of ceramic, tantalum or other very low ESR capacitance is recommended in order to keep the internal IC supply quiet.
2. Place the feedback divider between the + and – terminals of COUT. Route $DIFF^+$ and $DIFF^-$ with minimum PC trace spacing from the IC to the feedback divider.
3. Are the $SENSE^+$ and $SENSE^-$ printed circuit traces routed together with minimum PC trace spacing? The filter capacitors between $SENSE^+$ and $SENSE^-$ should be as close as possible to the pins of the IC. Connect the $SENSE^+$ and $SENSE^-$ pins to the pads of the sense resistor as illustrated in Figure 2.
4. Do the (+) plates of C_{IN} connect to the drain of the topside MOSFET as closely as possible? This capacitor provides the pulsed current to the MOSFET.
5. Keep the switching nodes, SW, BOOST and TG away from sensitive small-signal nodes ($SENSE^+$, $SENSE^-$, $DIFF^+$, $DIFF^-$, V_{FB}). Ideally the SW, BOOST and TG printed circuit traces should be routed away and separated from the IC and especially the *quiet* side of the IC. Separate the high dv/dt traces from sensitive small-signal nodes with ground traces or ground planes.
6. Use a low impedance source such as a logic gate to drive the MODE/PLLIN pin and keep the lead as short as possible.
7. The 47pF to 330pF ceramic capacitor between the I_{TH} pin and signal ground should be placed as close as possible to the IC. Figure 16 illustrates all branch currents in a switching regulator. It becomes very clear after studying the current waveforms why it is critical to keep the high switching current paths to a small physical size. High electric and magnetic fields will radiate from these *loops* just as radio stations transmit signals. The output capacitor ground should return to the negative terminal of the input capacitor and not share a common ground path with any switched current paths. The left half of the circuit gives rise to the *noise* generated by a switching regulator. The ground terminations of the synchronous MOSFET and Schottky diode should return to the bottom plate(s) of the input capacitor(s) with a short isolated PC trace since very high switched currents are present. External OPTI-LOOP® compensation allows overcompensation for PC layouts which are not optimized but this is not the recommended design procedure.



BOLD LINES INDICATE HIGH, SWITCHING CURRENTS. KEEP LINES TO A MINIMUM LENGTH

Figure 16. Branch Current Waveforms

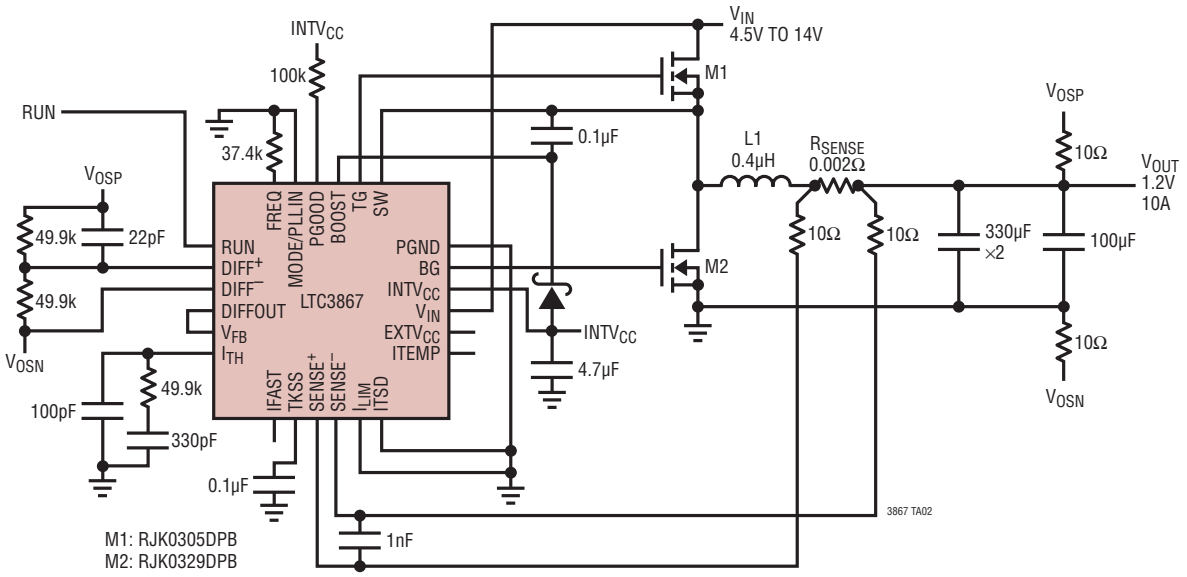
APPLICATIONS INFORMATION

8. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The V_{FB} and I_{TH} traces should be as short as possible. The path formed by the top N-channel MOSFET, Schottky diode and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.

9. Use a modified "star ground" technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the SGND pin of the IC.

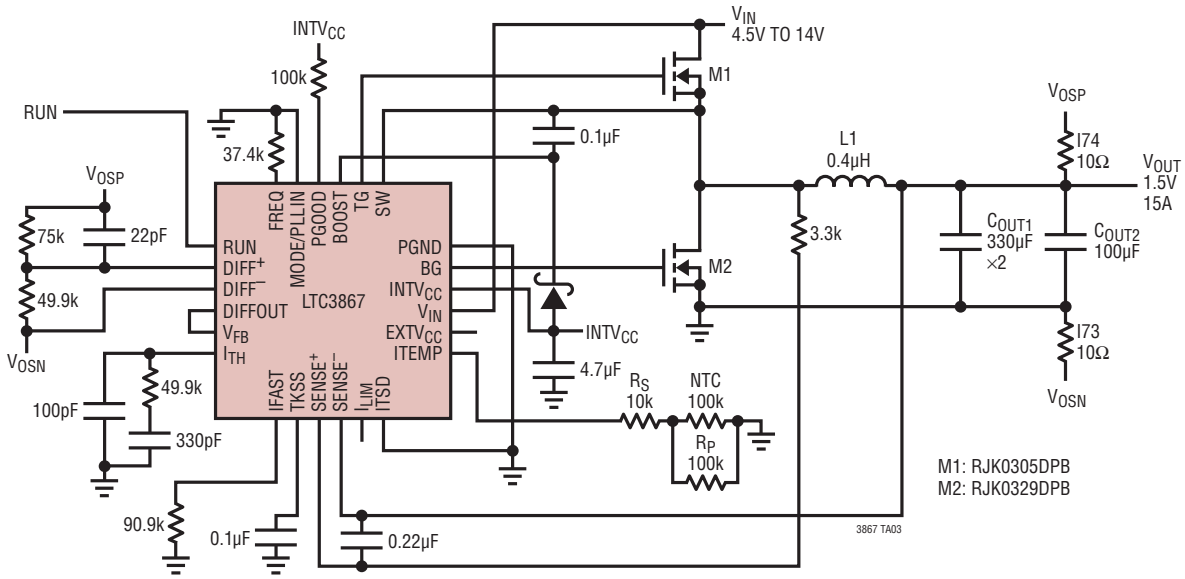
TYPICAL APPLICATIONS

1.2V, 10A Output with R_{SENSE}



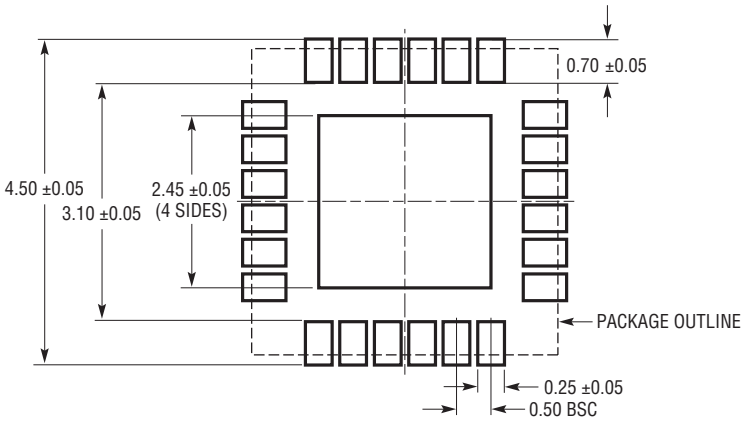
TYPICAL APPLICATIONS

1.5V, 15A Output with DCR Sense, Nonlinear Control and DCR Temperature Compensation

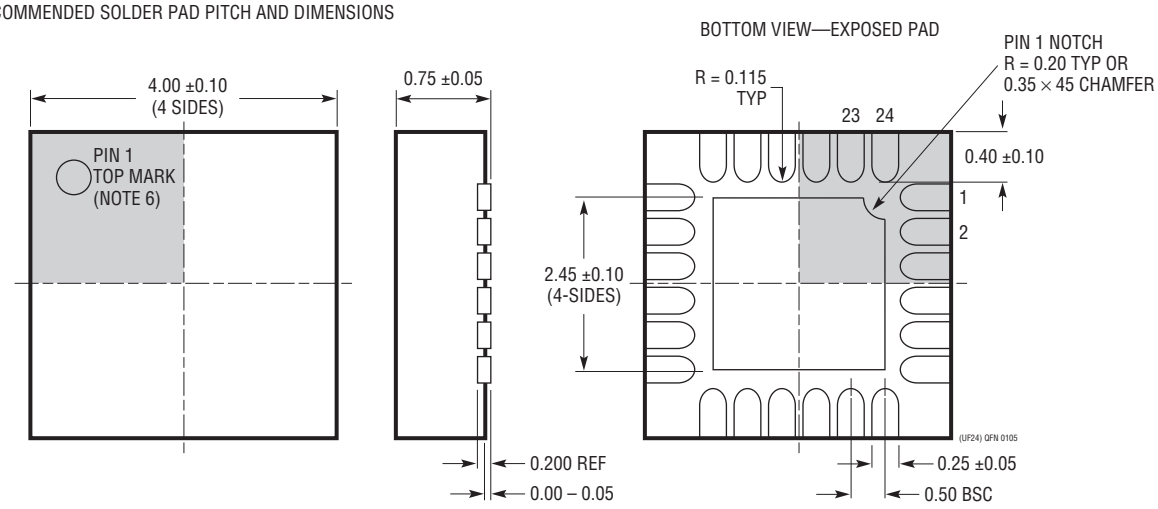


PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE