8-Channel Parallelable 1A Buck DC/DCs

FEATURES

- **8-Channel Independent Step-Down DC/DCs**
- **Master-Slave Configurable for Up to 4A per Output Rail with a Single Inductor**
- **Independent V_{IN} Supplies for Each DC/DC (2.25V to 5.5V)**
- **All DC/DCs Have 0.8V to V_{IN} Output Range**
- **Precision Enable Pin Thresholds for Autonomous Sequencing**
- 1MHz to 3MHz Programmable/Synchronizable Oscillator Frequency (2MHz Default)
- Die Temperature Monitor Output
- Thermally-Enhanced 38-Lead QFN (5mm × 7mm) and TSSOP Packages

APPLICATIONS

- General Purpose Multichannel Power Supplies
- Industrial/Automotive/Communications

DESCRIPTION

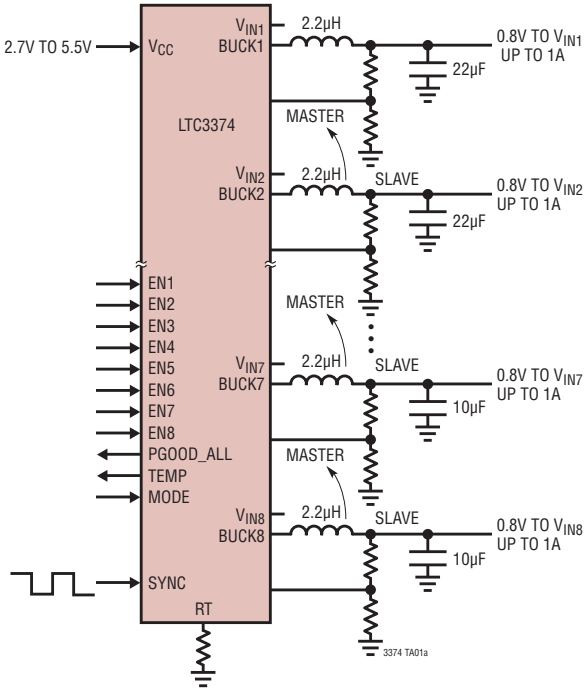
The LTC®3374 is a high efficiency multioutput power supply IC. The DC/DCs consist of eight synchronous buck converters (1A each) all powered from independent 2.25V to 5.5V input supplies.

The DC/DCs may be used independently or in parallel to achieve higher currents of up to 4A per output with a shared inductor. The common buck switching frequency may be programmed with an external resistor, synchronized to an external oscillator, or set to a default internal 2MHz clock. The operating mode for all DC/DCs may be programmed via the MODE pin.

To reduce input noise the buck converters are phased in 90° steps. Precision enable pin thresholds provide reliable power-up sequencing. The LTC3374 is available in a compact 38-lead 5mm × 7mm QFN package as well as a 38-lead TSSOP package.

TYPICAL APPLICATION

8-Channel 1A Multioutput Buck Regulator



Buck Efficiency vs I_{LOAD}

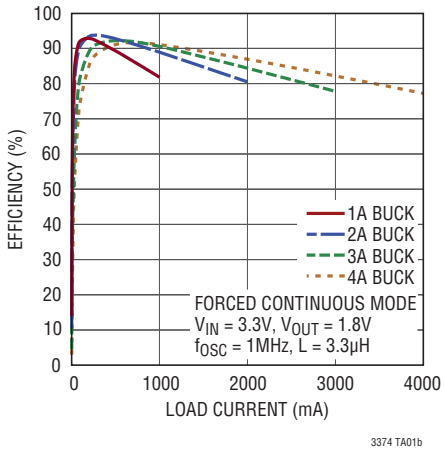


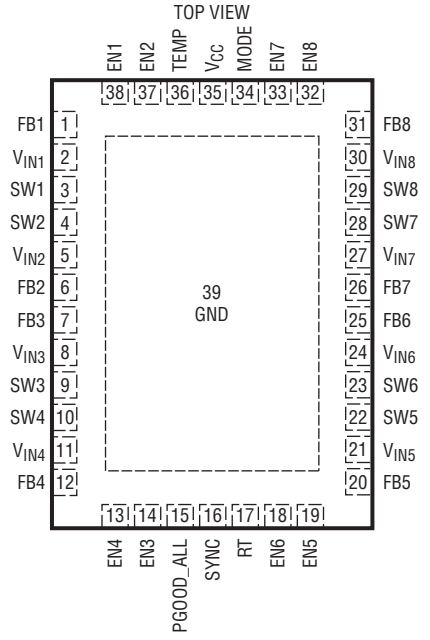
TABLE OF CONTENTS

ABSOLUTE MAXIMUM RATINGS (Note 1)

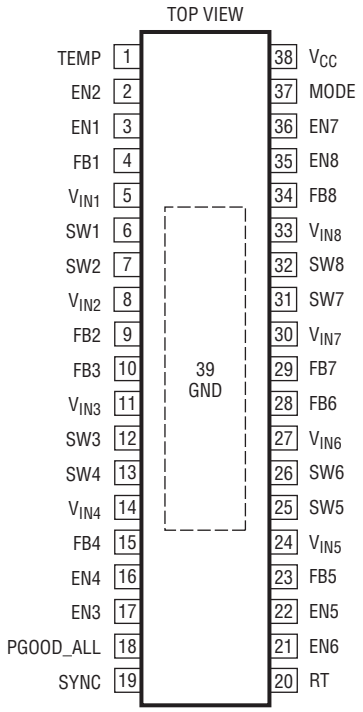
V_{IN1-8}, FB1-8, EN1-8, V_{CC}, PGOOD_ALL, SYNC, RT, MODE ..... –0.3V to 6V
TEMP ..... –0.3V to Lesser of (V_{CC} + 0.3V) or 6V
I_{PGOOD_ALL} 5mA

Operating Junction Temperature Range (Notes 2, 3) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB



FE PACKAGE
38-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JA} = 25°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3374EUHF#PBF	LTC3374EUHF#TRPBF	3374	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3374IUHF #PBF	LTC3374IUHF#TRPBF	3374	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3374HUHF #PBF	LTC3374HUHF#TRPBF	3374	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 150°C
LTC3374EFE #PBF	LTC3374EFE#TRPBF	LTC3374FE	38-Lead Plastic TSSOP	–40°C to 125°C
LTC3374IFE #PBF	LTC3374IFE#TRPBF	LTC3374FE	38-Lead Plastic TSSOP	–40°C to 125°C
LTC3374HFE #PBF	LTC3374HFE#TRPBF	LTC3374FE	38-Lead Plastic TSSOP	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{IN1-8} = 3.3V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{VCC}	V_{CC} Voltage Range		●	2.7		5.5	V
V_{VCC_UVLO}	Undervoltage Threshold on V_{CC}	V_{CC} Voltage Falling V_{CC} Voltage Rising	● ●	2.35 2.45	2.45 2.55	2.55 2.65	V V
I_{VCC_ALLOFF}	V_{CC} Input Supply Current	All Switching Regulators in Shutdown			8	18	µA
I_{VCC}	V_{CC} Input Supply Current	At Least 1 Buck Active SYNC = 0V, R_T = 400k, V_{FB_BUCK} = 0.85V SYNC = 2MHz			 45 200	 75 275	 µA µA
f_{OSC}	Internal Oscillator Frequency	V_{RT} = V_{CC}, SYNC = 0V V_{RT} = V_{CC}, SYNC = 0V R_{RT} = 400k, SYNC = 0V	 ● ●	1.8 1.75 1.8	2 2 2	2.2 2.25 2.2	MHz MHz MHz
f_{SYNC}	Synchronization Frequency	t_{LOW}, t_{HIGH} > 40ns		1		3	MHz
V_{SYNC}	SYNC Level High SYNC Level Low		● ●	1.2		 0.4	V V
V_{RT}	RT Servo Voltage	R_{RT} = 400k	●	780	800	820	mV
Temperature Monitor							
$V_{TEMP(ROOM)}$	TEMP Voltage at 25°C				150		mV
ΔV_{TEMP}/°C	V_{TEMP} Slope				6.75		mV/°C
OT	Overtemperature Shutdown	Temperature Rising			165		°C
OT Hyst	Overtemperature Hysteresis				10		°C
1A Buck Regulators							
V_{BUCK}	Buck Input Voltage Range		●	2.25		5.5	V
V_{OUT}	Buck Output Voltage Range			V_{FB}		V_{IN}	V
V_{IN_UVLO}	Undervoltage Threshold on V_{IN}	V_{IN} Voltage Falling V_{IN} Voltage Rising	● ●	1.95 2.05	2.05 2.15	2.15 2.25	V V
I_{VIN_BUCK}	Burst Mode® Operation Forced Continuous Mode Operation Shutdown Input Current Shutdown Input Current	V_{FB_BUCK} = 0.85V (Note 4) I_{SW_BUCK} = 0µA, V_{FB_BUCK} = 0V All Switching Regulators in Shutdown At Least One Other Buck Active			18 400 0 1	50 550 1 2	µA µA µA µA
I_{FWD}	PMOS Current Limit	(Note 5)		2.0	2.3	2.7	A
V_{FB}	Feedback Regulation Voltage		●	780	800	820	mV
I_{FB}	Feedback Leakage Current	V_{FB_BUCK} = 0.85V		–50		50	nA
DMAX	Maximum Duty Cycle	V_{FB_BUCK} = 0V	●	100			%
R_{PMOS}	PMOS On-Resistance	I_{SW_BUCK} = 100mA			300		mΩ
R_{NMOS}	NMOS On-Resistance	I_{SW_BUCK} = 100mA			300		mΩ
I_{LEAKP}	PMOS Leakage Current	EN_BUCK = 0		–2		2	µA
I_{LEAKN}	NMOS Leakage Current	EN_BUCK = 0		–2		2	µA
t_{SS}	Soft-Start Time	(Note 6)	●	0.25	1	3	ms
$V_{PGOOD(FALL)}$	Falling PGOOD Threshold Voltage	% of Regulated V_{FB}			92.5		%
$V_{PGOOD(HYS)}$	PGOOD Hysteresis	% of Regulated V_{FB}			1		%
Buck Regulators Combined							
I_{FWD2}	PMOS Current Limit	2 Buck Converters Combined (Note 5)			4.6		A
I_{FWD3}	PMOS Current Limit	3 Buck Converters Combined (Note 5)			6.9		A
I_{FWD4}	PMOS Current Limit	4 Buck Converters Combined (Note 5)			9.2		A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{IN1-8} = 3.3V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Interface Logic Pins (PGOOD_ALL, MODE)							
I_{OH}	Output High Leakage Current	PGOOD_ALL 5.5V at Pin		–1		1	µA
V_{OL}	Output Low Voltage	PGOOD_ALL 3mA into Pin			0.1	0.4	V
V_{IH}	Input High Threshold	MODE	●	1.2			V
V_{IL}	Input Low Threshold	MODE	●			0.4	V
Interface Logic Pins (EN1, EN2, EN3, EN4, EN5, EN6, EN7, EN8)							
V_{HI_ALLOFF}	Enable Rising Threshold	All Regulators Disabled	●	400	730	1200	mV
V_{EN_HYS}	Enable Falling Hysteresis				60		mV
V_{HI}	Enable Rising Threshold	At Least One Regulator Enabled	●	380	400	420	mV
I_{EN}	Enable Pin Leakage Current	EN = V_{CC} = V_{IN} = 5.5V		–1		1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3374 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3374E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3374I is guaranteed over the –40°C to 125°C operating junction temperature range and the LTC3374H is guaranteed over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J in °C) is calculated from ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: The LTC3374 includes overtemperature protection which protects the device during momentary overload conditions. Junction temperatures will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

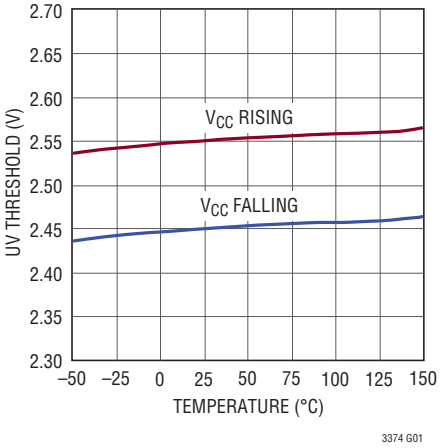
Note 4: Static current, switches not switching. Actual current may be higher due to gate charge losses at the switching frequency.

Note 5: The current limit features of this part are intended to protect the IC from short term or intermittent fault conditions. Continuous operation above the maximum specified pin current rating may result in device degradation over time.

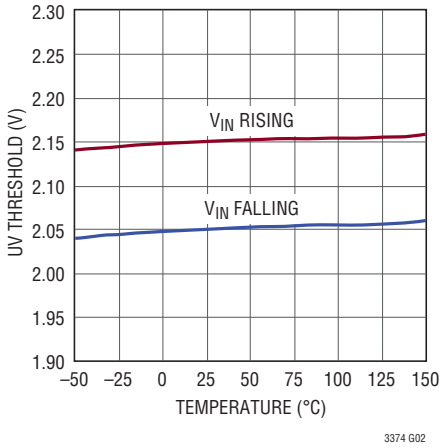
Note 6: The soft-start is the time from the first top switch turn on, after an enable rising, until the feedback has reached 90% of its nominal regulation voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

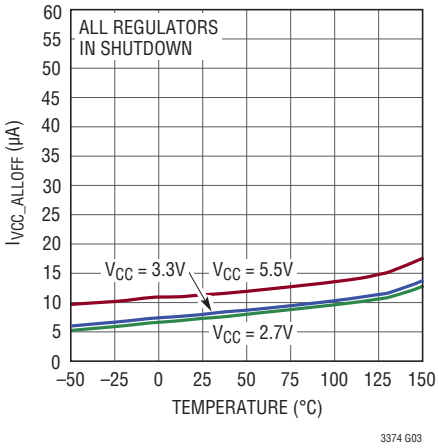
V_{CC} Undervoltage Threshold vs Temperature



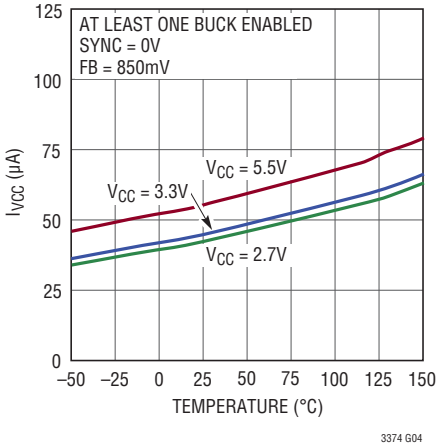
Buck V_{IN} Undervoltage Threshold vs Temperature



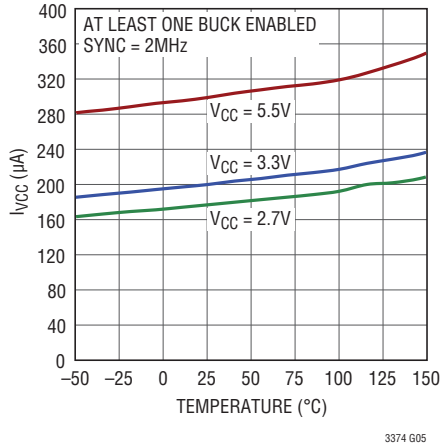
V_{CC} Supply Current vs Temperature



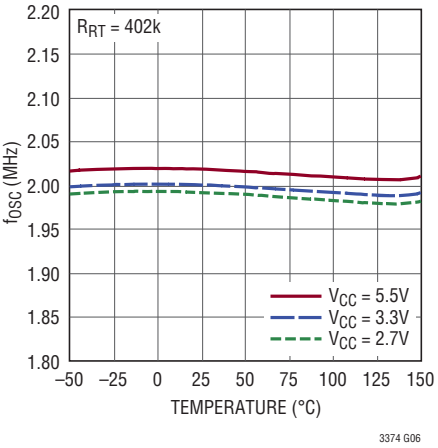
V_{CC} Supply Current vs Temperature



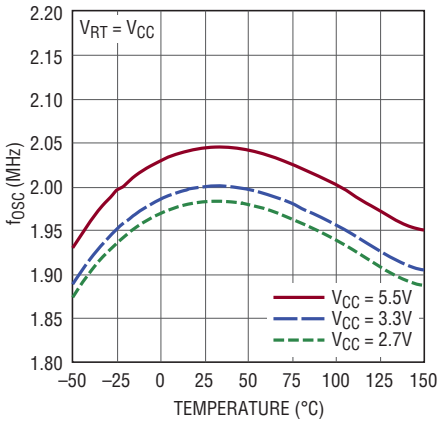
V_{CC} Supply Current vs Temperature



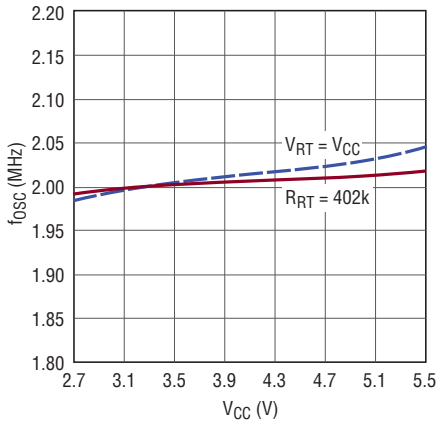
RT Programmed Oscillator Frequency vs Temperature



Default Oscillator Frequency vs Temperature

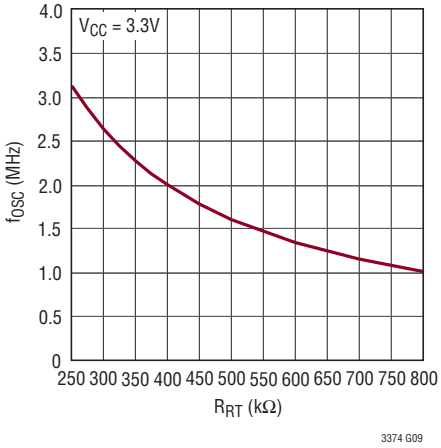


Oscillator Frequency vs V_{CC}



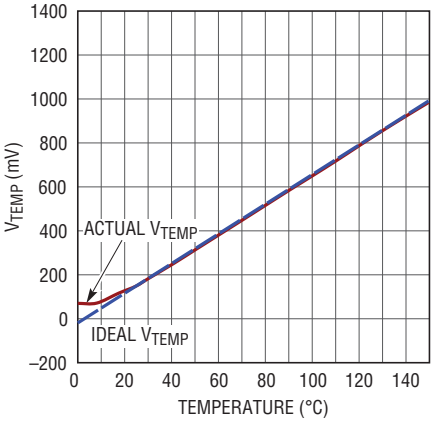
TYPICAL PERFORMANCE CHARACTERISTICS

Oscillator Frequency vs R_T



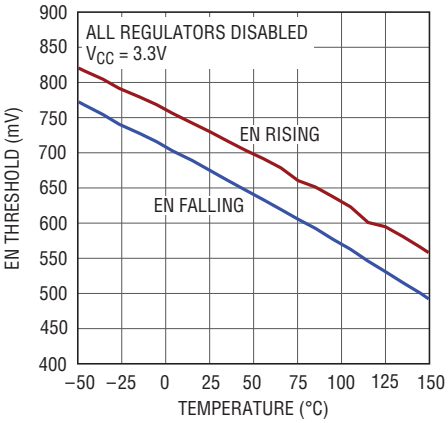
3374 G09

V_{TEMP} vs Temperature



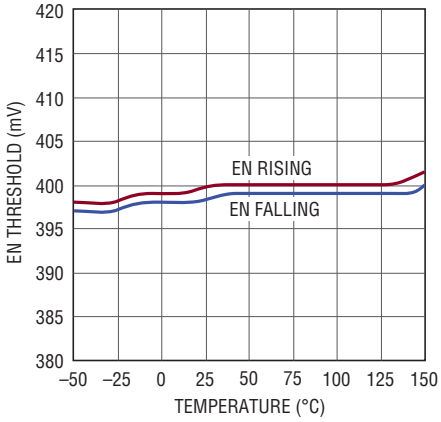
3374 G10

Enable Threshold vs Temperature



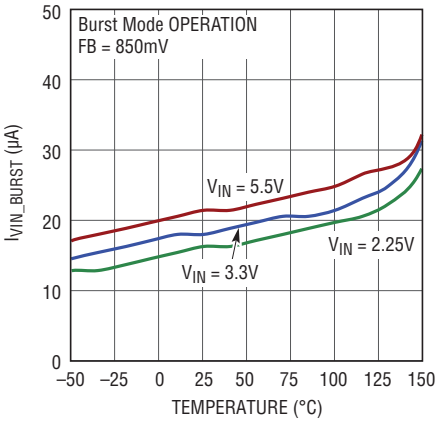
3374 G11

Enable Pin Precision Threshold vs Temperature



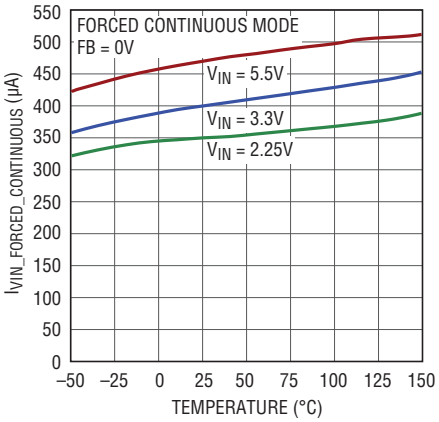
3374 G12

Buck V_{IN} Supply Current vs Temperature



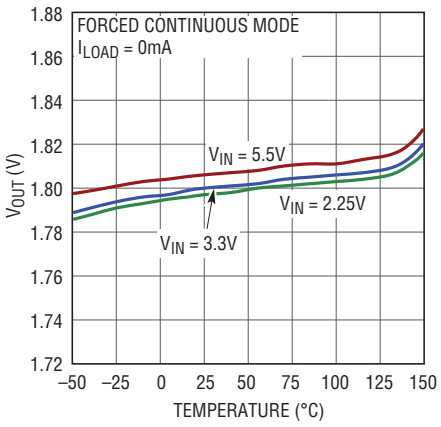
3374 G13

Buck V_{IN} Supply Current vs Temperature



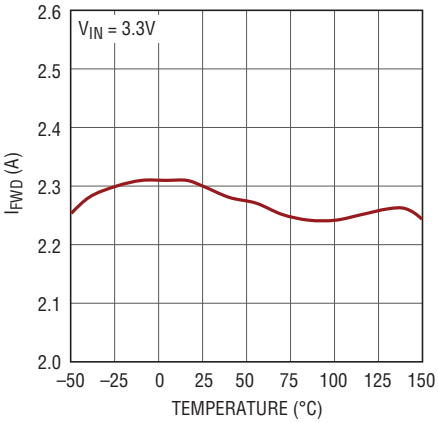
3374 G14

V_{OUT} vs Temperature



3374 G15

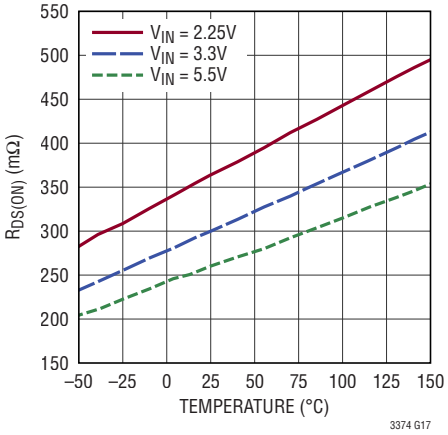
PMOS Current Limit vs Temperature



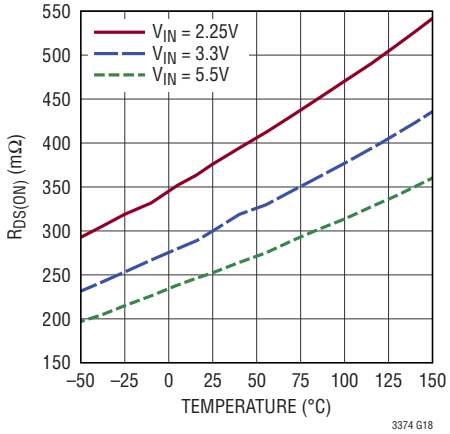
3374 G16

TYPICAL PERFORMANCE CHARACTERISTICS

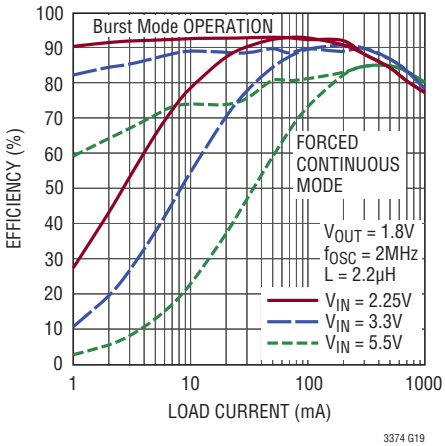
PMOS $R_{DS(ON)}$ vs Temperature



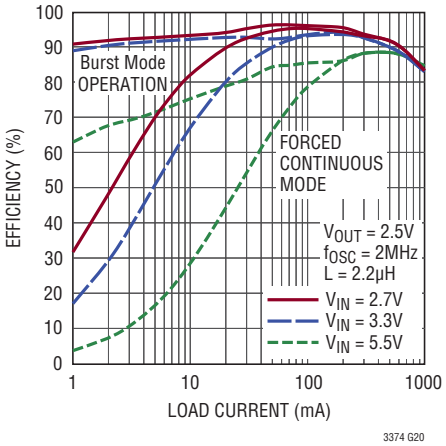
NMOS $R_{DS(ON)}$ vs Temperature



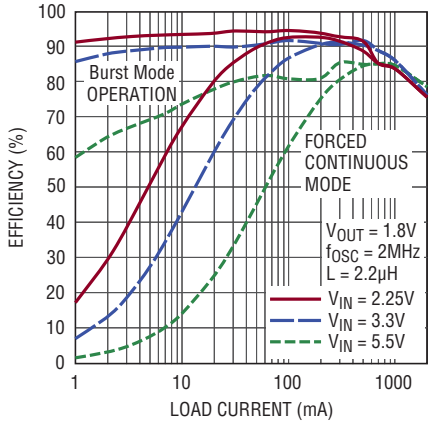
1A Buck Efficiency vs I_{LOAD}, V_{OUT} = 1.8V



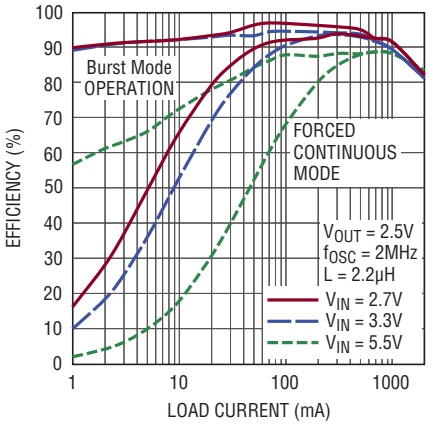
1A Buck Efficiency vs I_{LOAD}, V_{OUT} = 2.5V



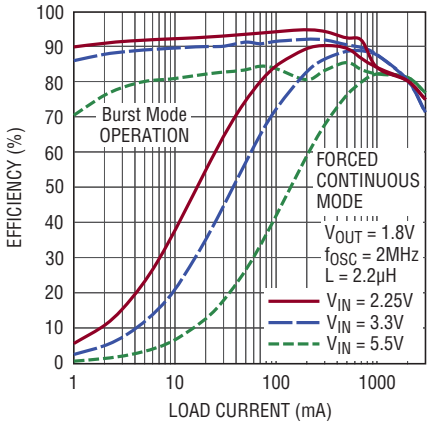
2A Buck Efficiency vs I_{LOAD}, V_{OUT} = 1.8V



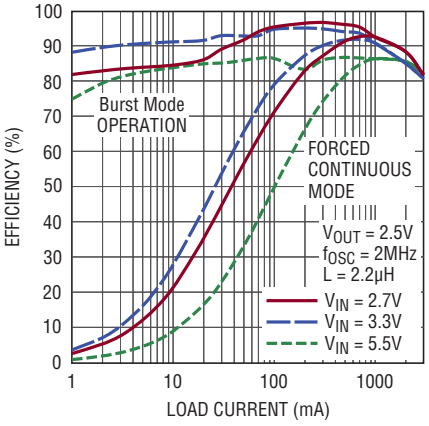
2A Buck Efficiency vs I_{LOAD}, V_{OUT} = 2.5V



3A Buck Efficiency vs I_{LOAD}, V_{OUT} = 1.8V

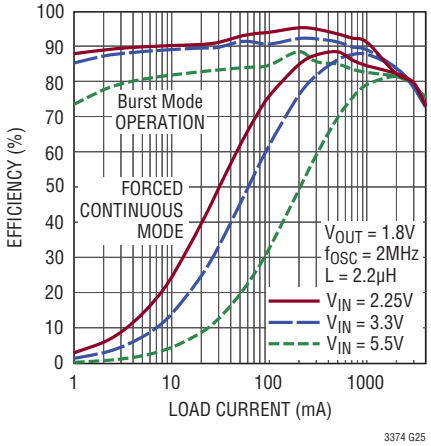


3A Buck Efficiency vs I_{LOAD}, V_{OUT} = 2.5V

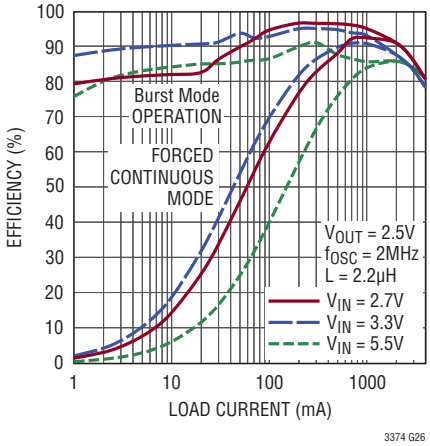


TYPICAL PERFORMANCE CHARACTERISTICS

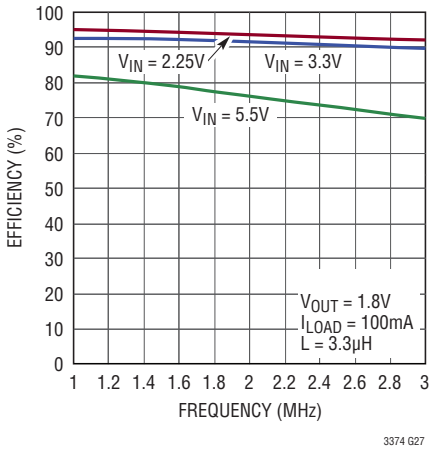
4A Buck Efficiency vs I_{LOAD}, V_{OUT} = 1.8V



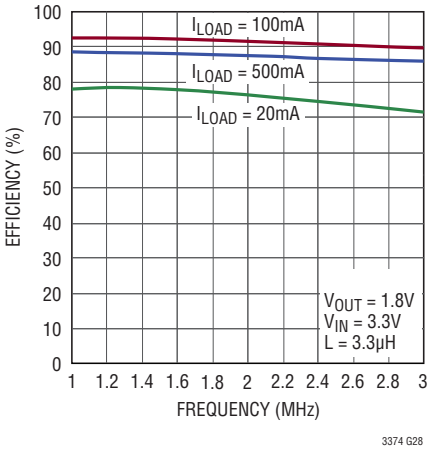
4A Buck Efficiency vs I_{LOAD}, V_{OUT} = 2.5V



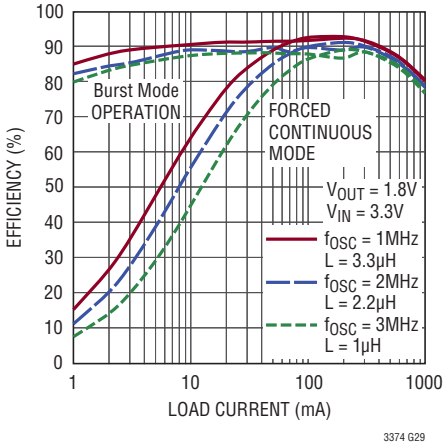
1A Buck Efficiency vs Frequency (Forced Continuous Mode)



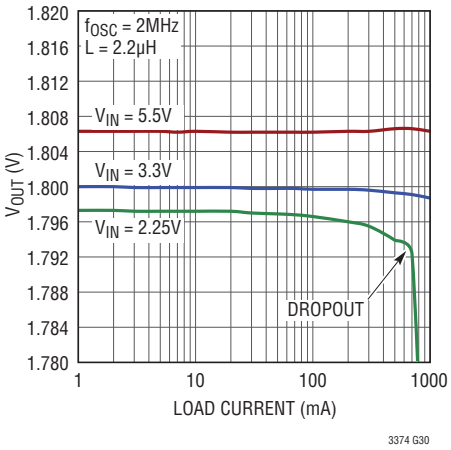
1A Buck Efficiency vs Frequency (Forced Continuous Mode)



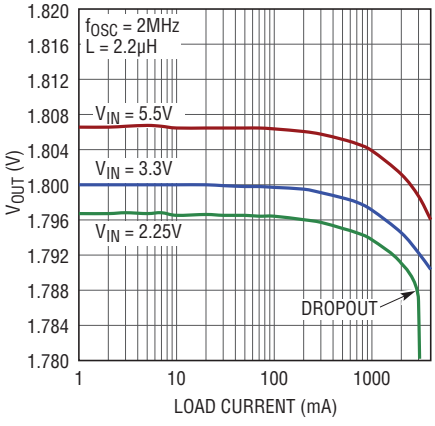
1A Buck Efficiency vs I_{LOAD} (Across Operating Frequency)



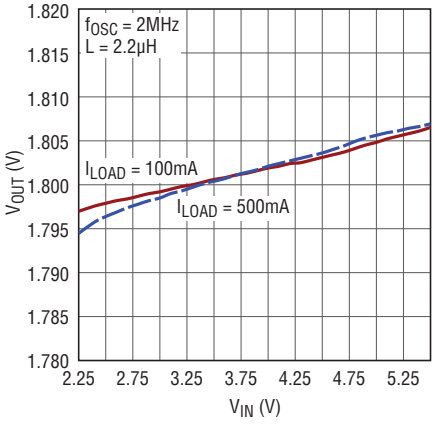
1A Buck Regulator Load Regulation (Forced Continuous Mode)



4A Buck Regulator Load Regulation (Forced Continuous Mode)

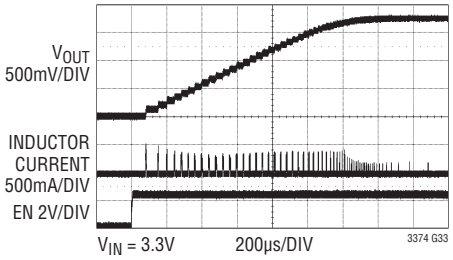


1A Buck Regulator Line Regulation (Forced Continuous Mode)

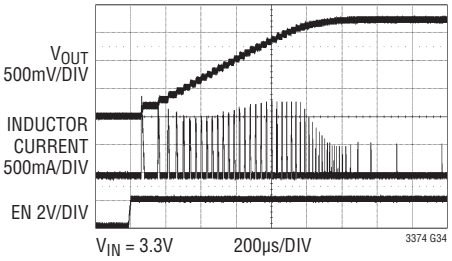


TYPICAL PERFORMANCE CHARACTERISTICS

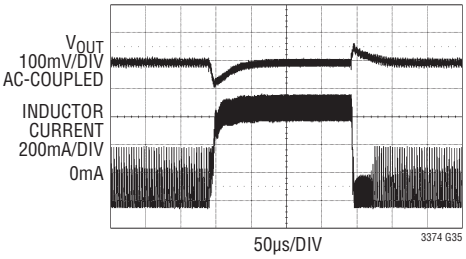
1A Buck Regulator No-Load Start-Up Transient (Burst Mode Operation)



4A Buck Regulator No-Load Start-Up Transient (Forced Continuous Mode)

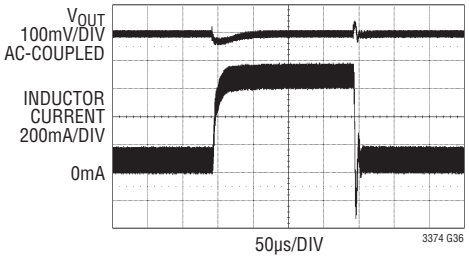


1A Buck Regulator, Transient Response (Burst Mode Operation)



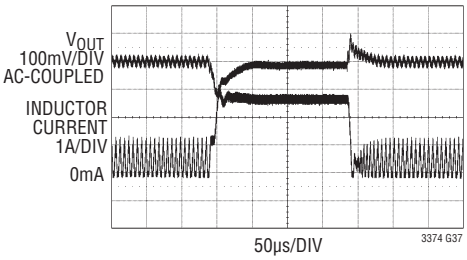
LOAD STEP = 100mA TO 700mA
V_{IN} = 3.3V
V_{OUT} = 1.8V

1A Buck Regulator, Transient Response (Forced Continuous Mode)



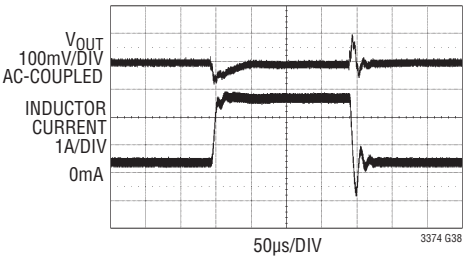
LOAD STEP = 100mA TO 700mA
V_{IN} = 3.3V
V_{OUT} = 1.8V

4A Buck Regulator, Transient Response (Burst Mode Operation)



LOAD STEP = 400mA TO 2.8A
V_{IN} = 3.3V
V_{OUT} = 1.8V

4A Buck Regulator, Transient Response (Forced Continuous Mode)



LOAD STEP = 400mA TO 2.8A
V_{IN} = 3.3V
V_{OUT} = 1.8V

PIN FUNCTIONS (QFN/TSSOP)

FB1 (Pin 1/Pin 4): Buck Regulator 1 Feedback Pin. Receives feedback by a resistor divider connected across the output.

V_{IN1} (Pin 2/Pin 5): Buck Regulator 1 Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

SW1 (Pin 3/Pin 6): Buck Regulator 1 Switch Node. External inductor connects to this pin.

SW2 (Pin 4/Pin 7): Buck Regulator 2 Switch Node. External inductor connects to this pin.

V_{IN2} (Pin 5/Pin 8): Buck Regulator 2 Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor. May be driven by an independent supply or must be shorted to V_{IN1} when buck regulator 2 is combined with buck regulator 1 for higher current.

FB2 (Pin 6/Pin 9): Buck Regulator 2 Feedback Pin. Receives feedback by a resistor divider connected across the output. Connecting FB2 to V_{IN2} combines buck regulator 2 with buck regulator 1 for higher current. Up to four converters may be combined in this way.

FB3 (Pin 7/Pin 10): Buck Regulator 3 Feedback Pin. Receives feedback by a resistor divider connected across the output. Connecting FB3 to V_{IN3} combines buck regulator 3 with buck regulator 2 for higher current. Up to four converters may be combined in this way.

V_{IN3} (Pin 8/Pin 11): Buck Regulator 3 Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor. May be driven by an independent supply or must be shorted to V_{IN2} when buck regulator 3 is combined with buck regulator 2 for higher current.

SW3 (Pin 9/Pin 12): Buck Regulator 3 Switch Node. External inductor connects to this pin.

SW4 (Pin 10/Pin 13): Buck Regulator 4 Switch Node. External inductor connects to this pin.

V_{IN4} (Pin 11/Pin 14): Buck Regulator 4 Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor. May be driven by an independent supply or must be shorted to V_{IN3} when buck regulator 4 is combined with buck regulator 3 for higher current.

FB4 (Pin 12/Pin 15): Buck Regulator 4 Feedback Pin. Receives feedback by a resistor divider connected across the output. Connecting FB4 to V_{IN4} combines buck regulator 4 with buck regulator 3 for higher current. Up to four converters may be combined in this way.

EN4 (Pin 13/Pin 16): Buck Regulator 4 Enable Input. Active high.

EN3 (Pin 14/Pin 17): Buck Regulator 3 Enable Input. Active high.

PGOOD_ALL (Pin 15/Pin 18): PGOOD Status Pin. Open-drain output. When the regulated output voltage of any enabled switching regulator is more than 7.5% below its programmed level, this pin is driven LOW. When all buck regulators are disabled PGOOD_ALL is driven LOW.

SYNC (Pin 16/Pin 19): Oscillator Synchronization Pin. Driving SYNC with an external clock signal will synchronize all switchers to the applied frequency. The slope compensation is automatically adapted to the external clock frequency. The absence of an external clock signal will enable the frequency programmed by the RT pin. SYNC should be held at ground if not used. Do not float.

RT (Pin 17/Pin 20): Oscillator Frequency Pin. This pin provides two modes of setting the switching frequency. Connecting a resistor from RT to ground will set the switching frequency based on the resistor value. If RT is tied to V_{CC} the internal 2MHz oscillator will be used. Do not float.

EN6 (Pin 18/Pin 21): Buck Regulator 6 Enable Input. Active high.

EN5 (Pin 19/Pin 22): Buck Regulator 5 Enable Input. Active high.

FB5 (Pin 20/Pin 23): Buck Regulator 5 Feedback Pin. Receives feedback by a resistor divider connected across the output. Connecting FB5 to V_{IN5} combines buck regulator 5 with buck regulator 4 for higher current. Up to four converters may be combined in this way.

PIN FUNCTIONS (QFN/TSSOP)

V_{IN5} (Pin 21/Pin 24): Buck Regulator 5 Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor. May be driven by an independent supply or must be shorted to V_{IN4} when buck regulator 5 is combined with buck regulator 4 for higher current.

SW5 (Pin 22/Pin 25): Buck Regulator 5 Switch Node. External inductor connects to this pin.

SW6 (Pin 23/Pin 26): Buck Regulator 6 Switch Node. External inductor connects to this pin.

V_{IN6} (Pin 24/Pin 27): Buck Regulator 6 Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor. May be driven by an independent supply or must be shorted to V_{IN5} when buck regulator 6 is combined with buck regulator 5 for higher current.

FB6 (Pin 25/Pin 28): Buck Regulator 6 Feedback Pin. Receives feedback by a resistor divider connected across the output. Connecting FB6 to V_{IN6} combines buck regulator 6 with buck regulator 5 for higher current. Up to four converters may be combined in this way.

FB7 (Pin 26/Pin 29): Buck Regulator 7 Feedback Pin. Receives feedback by a resistor divider connected across the output. Connecting FB7 to V_{IN7} combines buck regulator 7 with buck regulator 6 for higher current. Up to four converters may be combined in this way.

V_{IN7} (Pin 27/Pin 30): Buck Regulator 7 Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor. May be driven by an independent supply or must be shorted to V_{IN6} when buck regulator 7 is combined with buck regulator 6 for higher current.

SW7 (Pin 28/Pin 31): Buck Regulator 7 Switch Node. External inductor connects to this pin.

SW8 (Pin 29/Pin 32): Buck Regulator 8 Switch Node. External inductor connects to this pin.

V_{IN8} (Pin 30/Pin 33): Buck Regulator 8 Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor. May be driven by an independent supply or must be shorted to V_{IN7} when buck regulator 8 is combined with buck regulator 7 for higher current.

FB8 (Pin 31/Pin 34): Buck Regulator 8 Feedback Pin. Receives feedback by a resistor divider connected across the output. Connecting FB8 to V_{IN8} combines buck regulator 8 with buck regulator 7 for higher current. Up to four converters may be combined in this way.

EN8 (Pin 32/Pin 35): Buck Regulator 8 Enable Input. Active high.

EN7 (Pin 33/Pin 36): Buck Regulator 7 Enable Input. Active high.

MODE (Pin 34/Pin 37): Logic Input. MODE enables Burst Mode functionality for all the buck switching regulators when the pin is set low. When the pin is set high, all the buck switching regulators will operate in forced continuous mode.

V_{CC} (Pin 35/Pin 38): Internal Bias Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

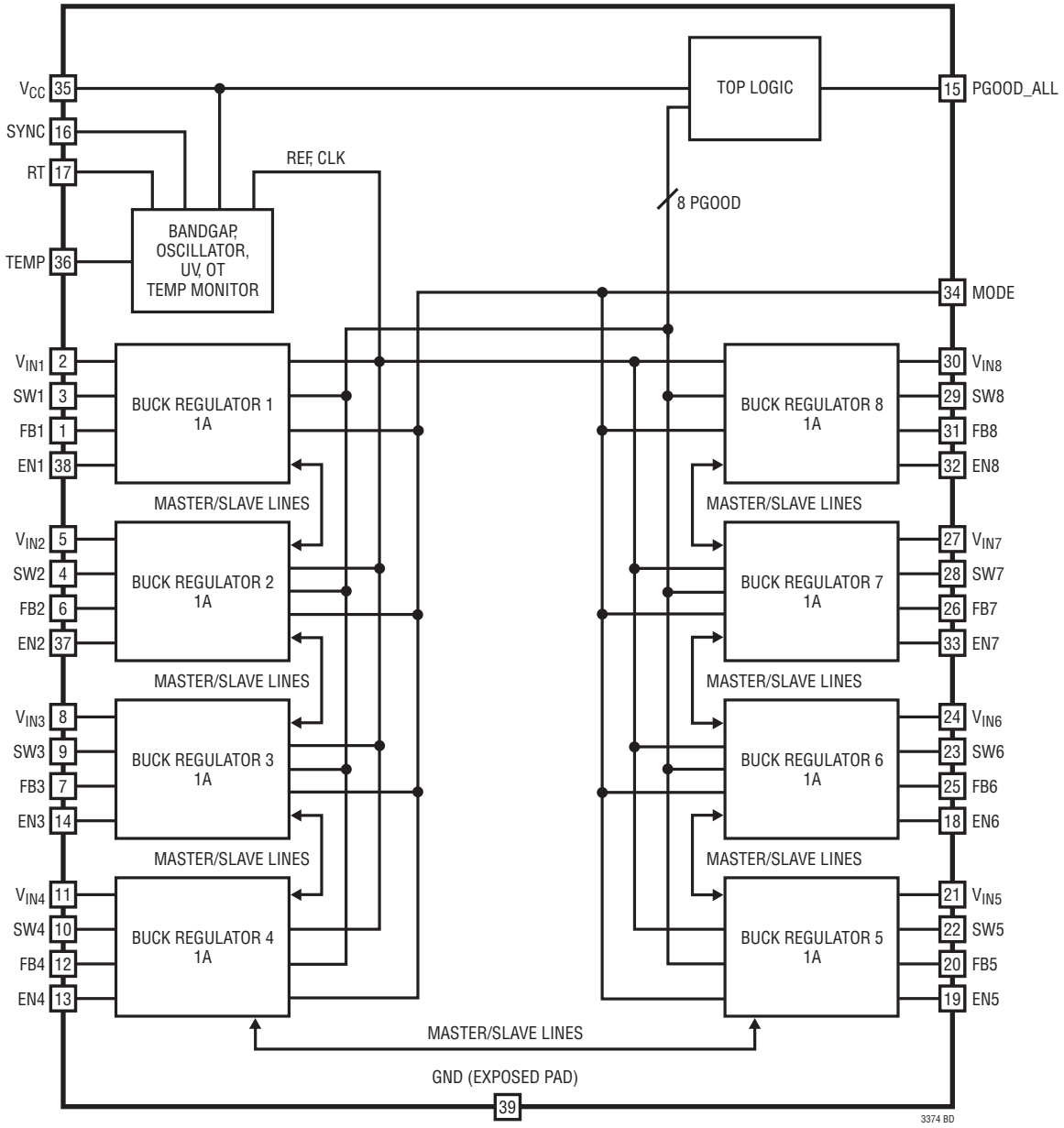
TEMP (Pin 36/Pin 1): Temperature Indication Pin. TEMP outputs a voltage of 150mV (typical) at room temperature. The TEMP voltage will change by 6.75mV/°C (typical) giving an external indication of the LTC3374 internal die temperature.

EN2 (Pin 37/Pin 2): Buck Regulator 2 Enable Input. Active high.

EN1 (Pin 38/Pin 3): Buck Regulator 1 Enable Input. Active high.

GND (Exposed Pad Pin 39/Exposed Pad Pin 39): Ground. The exposed pad must be connected to a continuous ground plane on the printed circuit board directly under the LTC3374 for electrical contact and rated thermal performance.

BLOCK DIAGRAM (Pin numbers reflect QFN package)



OPERATION

Buck Switching Regulators

The LTC3374 contains eight monolithic 1A synchronous buck switching regulators. All of the switching regulators are internally compensated and need only external feedback resistors to set the output voltage. The switching regulators offer two operating modes: Burst Mode operation (when the MODE pin is set low) for higher efficiency at light loads and forced continuous PWM mode (when the MODE pin is set high) for lower noise at light loads. The MODE pin collectively sets the operating mode for all enabled buck switching regulators. In Burst Mode operation at light loads, the output capacitor is charged to a voltage slightly higher than its regulation point. The regulator then goes into sleep mode, during which time the output capacitor provides the load current. In sleep most of the regulator's circuitry is powered down, helping conserve input power. When the output capacitor droops below its programmed value, the circuitry is powered on and another burst cycle begins. The sleep time decreases as load current increases. In Burst Mode operation, the regulator will burst at light loads whereas at higher loads it will operate at constant frequency PWM mode operation. In forced continuous mode, the oscillator runs continuously and the buck switch currents are allowed to reverse under very light load conditions to maintain regulation. This mode allows the buck to run at a fixed frequency with minimal output ripple.

Each buck switching regulator has its own V_{IN}, SW, FB and EN pins to maximize flexibility. The enable pins have two different enable threshold voltages that depend on the operating state of the LTC3374. With all regulators disabled, the enable pin threshold is set to 730mV (typical). Once any regulator is enabled, the enable pin thresholds of the remaining regulators are set to a bandgap-based 400mV and the EN pins are each monitored by a precision comparator. This precision EN threshold may be used to provide event-based sequencing via feedback from other previously enabled regulators. All buck regulators have forward and reverse-current limiting, soft-start to limit inrush current during start-up, and short-circuit protection.

The buck switching regulators are phased in 90° steps to reduce noise and input ripple. The phase step determines the fixed edge of the switching sequence, which is when the PMOS turns on. The PMOS off (NMOS on) phase is subject to the duty cycle demanded by the regulator. Bucks 1 and 2 are set to 0°, bucks 3 and 4 are set to 90°, bucks 5 and 6 are set to 180°, and bucks 7 and 8 are set to 270°. In shutdown all SW nodes are high impedance. The buck regulator enable pins may be tied to V_{OUT} voltages, through a resistor divider, to program power-up sequencing.

Buck Regulators with Combined Power Stages

Up to four adjacent buck regulators may be combined in a master-slave configuration by connecting their SW pins together, connecting their V_{IN} pins together, and connecting the higher numbered bucks' FB pin(s) to the input supply. The lowest numbered buck is always the master. In Figure 1, buck regulator 1 is the master. The feedback network connected to the FB1 pin programs the output voltage to 1.2V. The FB2 pin is tied to V_{IN1-2}, which configures buck regulator 2 as the slave. The SW1 and SW2 pins must be tied together, as must the V_{IN1} and V_{IN2} pins. The slave buck control circuitry draws no current. The enable of the master buck (EN1) controls the

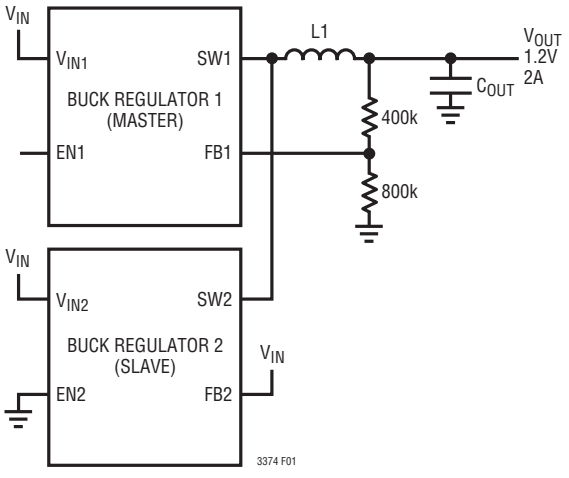


Figure 1. Buck Regulators Configured as Master-Slave

OPERATION

operation of the combined bucks; the enable of the slave regulator (EN2) must be tied to ground.

Any combination of 2, 3, or 4 adjacent buck regulators may be combined to provide either 2A, 3A, or 4A of average output load current. For example, buck regulator 1 and buck regulator 2 may run independently, while buck regulators 3 and 4 may be combined to provide 2A, while buck regulators 5 through 8 may be combined to provide 4A. Buck regulator 1 is never a slave, and buck regulator 8 is never a master. 15 unique output power stage configurations are possible to maximize application flexibility.

Power Failure Reporting Via PGOOD_ALL Pin

Power failure conditions are reported back via the PGOOD_ALL pin. All buck switching regulators have an internal power good (PGOOD) signal. When the regulated output voltage of an enabled switcher rises above 93.5% of its programmed value, the PGOOD signal will transition high. When the regulated output voltage falls below 92.5% of its programmed value, the PGOOD signal is pulled low. If any internal PGOOD signal stays low for greater than 100µs, then the PGOOD_ALL pin is pulled low, indicating to a microprocessor that a power failure fault has occurred. The 100µs filter time prevents the pin from being pulled low due to a transient.

An error condition that pulls the PGOOD_ALL pin low is not latched. When the error condition goes away, the PGOOD_ALL pin is released and is pulled high if no other error condition exists. If no buck switching regulators are enabled, then PGOOD_ALL will be pulled low.

Temperature Monitoring and Overtemperature Protection

To prevent thermal damage to the LTC3374 and its surrounding components, the LTC3374 incorporates an overtemperature (OT) function. When the LTC3374 die temperature reaches 165°C (typical) all enabled buck switching regulators are shut down and remain in shutdown until the die temperature falls to 155°C (typical).

The temperature may be read back by the user by sampling the TEMP pin analog voltage. The temperature, T, indicated by the TEMP pin voltage is given by:

$$T = \frac{V_{TEMP} + 19mV}{6.75mV} \bullet 1°C \quad (1)$$

If none of the buck switching regulators are enabled, then the temperature monitor is shut down to further reduce quiescent current.

Programming the Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output voltage ripple.

The operating frequency for all of the LTC3374 regulators is determined by an external resistor that is connected between the RT pin and ground. The operating frequency can be calculated by using the following equation:

$$f_{OSC} = \frac{8 \bullet 10^{11} \bullet \Omega Hz}{R_T} \quad (2)$$

While the LTC3374 is designed to function with operating frequencies between 1MHz and 3MHz, it has safety clamps that will prevent the oscillator from running faster than 4MHz (typical) or slower than 250kHz (typical). Tying the RT pin to V_{CC} sets the oscillator to the default internal operating frequency of 2MHz (typical).

The LTC3374's internal oscillator can be synchronized through an internal PLL circuit, to an external frequency by applying a square wave clock signal to the SYNC pin. During synchronization, the top MOSFET turn-on of buck switching regulators 1 and 2 are locked to the rising edge of the external frequency source. All other buck switching

OPERATION

regulators are locked to the appropriate phase of the external frequency source (see Buck Switching Regulators). The synchronization frequency range is 1MHz to 3MHz.

After detecting an external clock on the first rising edge of the SYNC pin, the PLL starts up at the current frequency being programmed by the RT pin. The internal PLL then requires a certain number of periods to gradually settle until the frequency at SW matches the frequency and phase of SYNC.

When the external clock is removed the LTC3374 needs approximately 5µs to detect the absence of the external clock. During this time, the PLL will continue to provide clock cycles before it recognizes the lack of a SYNC input. Once the external clock removal has been identified, the oscillator will gradually adjust its operating frequency to match the desired frequency programmed at the RT pin. SYNC should be connected to ground if not used.

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Buck Switching Regulator Output Voltage and Feedback Network

The output voltage of the buck switching regulators is programmed by a resistor divider connected from the switching regulator's output to its feedback pin and is given by $V_{OUT} = V_{FB}(1 + R2/R1)$ as shown in Figure 2. Typical values for R1 range from 40k to 1M. The buck regulator transient response may improve with optional capacitor C_{FF} that helps cancel the pole created by the feedback resistors and the input capacitance of the FB pin. Experimentation with capacitor values between 2pF and 22pF may improve transient response.

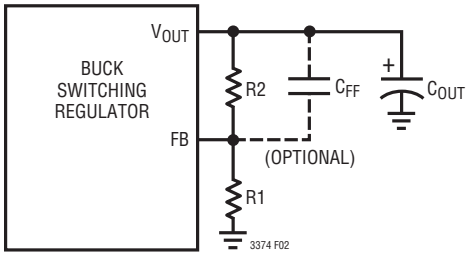


Figure 2. Feedback Components

Buck Regulators

All eight buck regulators are designed to be used with inductors ranging from 1µH to 3.3µH depending on the lowest switching frequency that the buck regulator must operate at. To operate at 1MHz a 3.3µH inductor should be used, while to operate at 3MHz a 1µH inductor may be used. Table 1 shows some recommended inductors for the buck regulators.

The input supply needs to be decoupled with a 10µF capacitor while the output needs to be decoupled with a 22µF capacitor. Refer to the Capacitor Selection section for details on selecting a proper capacitor.

Combined Buck Regulators

A single 2A buck regulator is available by combining two adjacent 1A buck regulators together. Likewise a 3A or 4A buck regulator is available by combining any three or four adjacent buck regulators respectively. Tables 2, 3, and 4 show recommended inductors for these configurations.

The input supply needs to be decoupled with a 22µF capacitor while the output needs to be decoupled with a 47µF capacitor for a 2A combined buck regulator. Likewise for 3A and 4A configurations the input and output capacitance must be scaled up to account for the increased load. Refer to the Capacitor Selection section for details on selecting a proper capacitor.

In many cases, any extra unused buck converters may be used to increase the efficiency of the active regulators. In general the efficiency will improve for any regulators running close to their rated load currents. If there are unused regulators, the user should look at their specific applications and current requirements to decide whether to add extra stages.

Input and Output Decoupling Capacitor Selection

The LTC3374 has individual input supply pins for each buck switching regulator and a separate V_{CC} pin that supplies power to all top level control and logic. Each of these pins must be decoupled with low ESR capacitors to GND. These capacitors must be placed as close to the pins as possible. Ceramic dielectric capacitors are a good compromise between high dielectric constant and stability versus temperature and DC bias. Note that the capacitance of a capacitor deteriorates at higher DC bias. It is important to consult manufacturer data sheets and obtain the true capacitance of a capacitor at the DC bias voltage it will be operated at. For this reason, avoid the use of Y5V dielectric capacitors. The X5R/X7R dielectric capacitors offer good overall performance.

The input supply voltage Pins 2/5, 5/8, 8/11, 11/14, 21/24, 24/27, 27/30, 30/33, and 35/38 (QFN/TSSOP packages) all need to be decoupled with at least 10µF capacitors.

APPLICATIONS INFORMATION

Table 1. Recommended Inductors for 1A Buck Regulators

PART NUMBER	L (µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
IHLP1212ABER1R0M-11	1.0	3	38	3 × 3.6 × 1.2	Vishay
1239AS-H-1R0N	1	2.5	65	2.5 × 2.0 × 1.2	Toko
XFL4020-222ME	2.2	3.5	23.5	4 × 4 × 2.1	CoilCraft
1277AS-H-2R2N	2.2	2.6	84	3.2 × 2.5 × 1.2	Toko
IHLP1212BZER2R2M-11	2.2	3	46	3 × 3.6 × 1.2	Vishay
XFL4020-332ME	3.3	2.8	38.3	4 × 4 × 2.1	CoilCraft
IHLP1212BZER3R3M-11	3.3	2.7	61	3 × 3.6 × 1.2	Vishay

Table 2. Recommended Inductors for 2A Buck Regulators

PART NUMBER	L (µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
XFL4020-102ME	1.0	5.1	11.9	4 × 4 × 2.1	CoilCraft
74437324010	1	5	27	4.45 × 4.06 × 1.8	Wurth Elektronik
XAL4020-222ME	2.2	5.6	38.7	4 × 4 × 2.1	CoilCraft
FDV0530-2R2M	2.2	5.3	15.5	6.2 × 5.8 × 3	Toko
IHLP2020BZER2R2M-11	2.2	5	37.7	5.49 × 5.18 × 2	Vishay
XAL4030-332ME	3.3	5.5	28.6	4 × 4 × 3.1	CoilCraft
FDV0530-3R3M	3.3	4.1	34.1	6.2 × 5.8 × 3	Toko

Table 3. Recommended Inductors for 3A Buck Regulators

PART NUMBER	L (µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
XAL4020-102ME	1.0	8.7	14.6	4 × 4 × 2.1	CoilCraft
FDV0530-1R0M	1	8.4	11.2	6.2 × 5.8 × 3	Toko
XAL5030-222ME	2.2	9.2	14.5	5.28 × 5.48 × 3.1	CoilCraft
IHLP2525CZER2R2M-01	2.2	8	20	6.86 × 6.47 × 3	Vishay
74437346022	2.2	6.5	20	7.3 × 6.6 × 2.8	Wurth Elektonik
XAL5030-332ME	3.3	8.7	23.3	5.28 × 5.48 × 3.1	CoilCraft
SPM6530T-3R3M	3.3	7.3	27	7.1 × 6.5 × 3	TDK

Table 4. Recommended Inductors for 4A Buck Regulators

PART NUMBER	L (µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
XAL5030-122ME	1.2	12.5	9.4	5.28 × 5.48 × 3.1	CoilCraft
SPM6530T-1R0M120	1	14.1	7.81	7.1 × 6.5 × 3	TDK
XAL5030-222ME	2.2	9.2	14.5	5.28 × 5.48 × 3.1	CoilCraft
SPM6530T-2R2M	2.2	8.4	19	7.1 × 6.5 × 3	TDK
IHLP2525EZER2R2M-01	2.2	13.6	20.9	6.86 × 6.47 × 5	Vishay
XAL6030-332ME	3.3	8	20.81	6.36 × 6.56 × 3.1	CoilCraft
FDVE1040-3R3M	3.3	9.8	10.1	11.2 × 10 × 4	Toko

APPLICATIONS INFORMATION

PCB Considerations

When laying out the printed circuit board, the following list should be followed to ensure proper operation of the LTC3374:

1. The exposed pad of the package (Pin 39) should connect directly to a large ground plane to minimize thermal and electrical impedance.
2. All the input supply pins should each have a decoupling capacitor.
3. The connections to the switching regulator input supply pins and their respective decoupling capacitors should be kept as short as possible. The GND side of these capacitors should connect directly to the ground plane of the part. These capacitors provide the AC current to the internal power MOSFETs and their drivers. It is important to minimize inductance from these capacitors to the V_{IN} pins of the LTC3374.
4. The switching power traces connecting SW1, SW2, SW3, SW4, SW5, SW6, SW7, and SW8 to their respective inductors should be minimized to reduce radiated EMI and parasitic coupling. Due to the large voltage swing of the switching nodes, high input impedance sensitive nodes, such as the feedback nodes, should be kept far away or shielded from the switching nodes or poor performance could result.
5. The GND side of the switching regulator output capacitors should connect directly to the thermal ground plane of the part. Minimize the trace length from the output capacitor to the inductor(s)/pin(s).
6. In a combined buck regulator application the trace length of switch nodes to the inductor must be kept equal to ensure proper operation.

APPLICATIONS INFORMATION

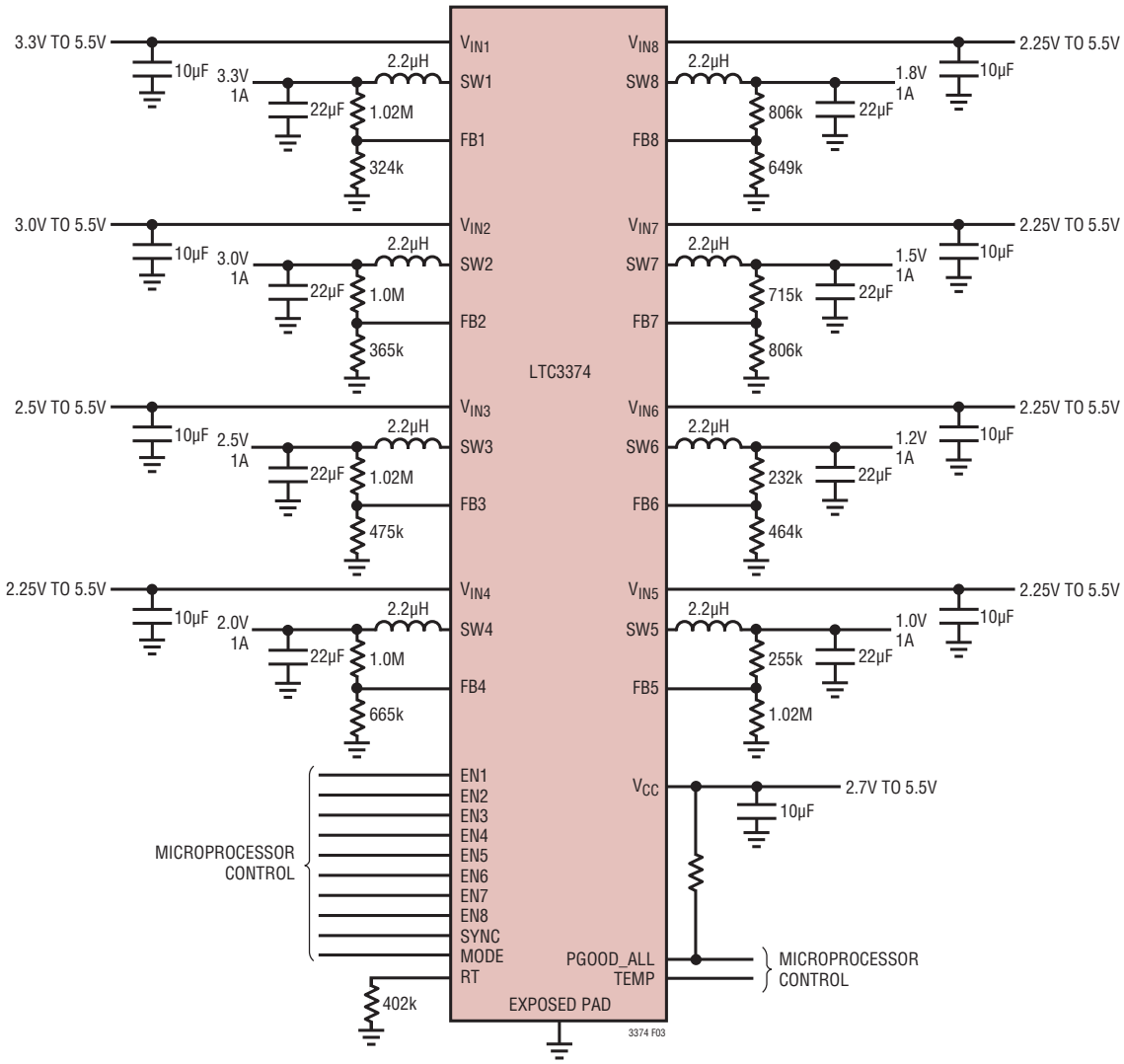


Figure 3. Detailed Front Page Application

APPLICATIONS INFORMATION

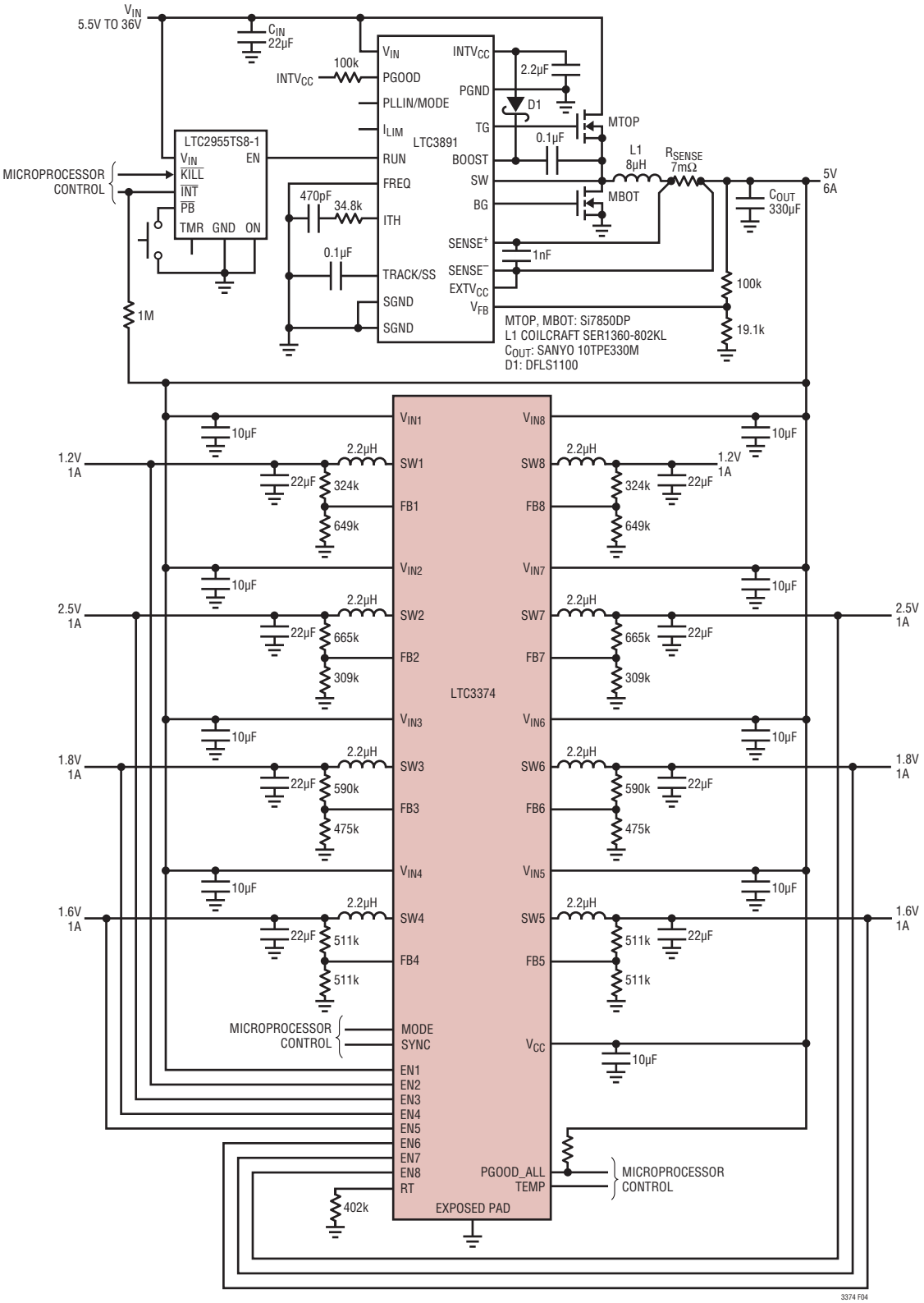


Figure 4. Buck Regulators with Sequenced Start-Up Driven from a High Voltage Upstream Buck Converter

APPLICATIONS INFORMATION

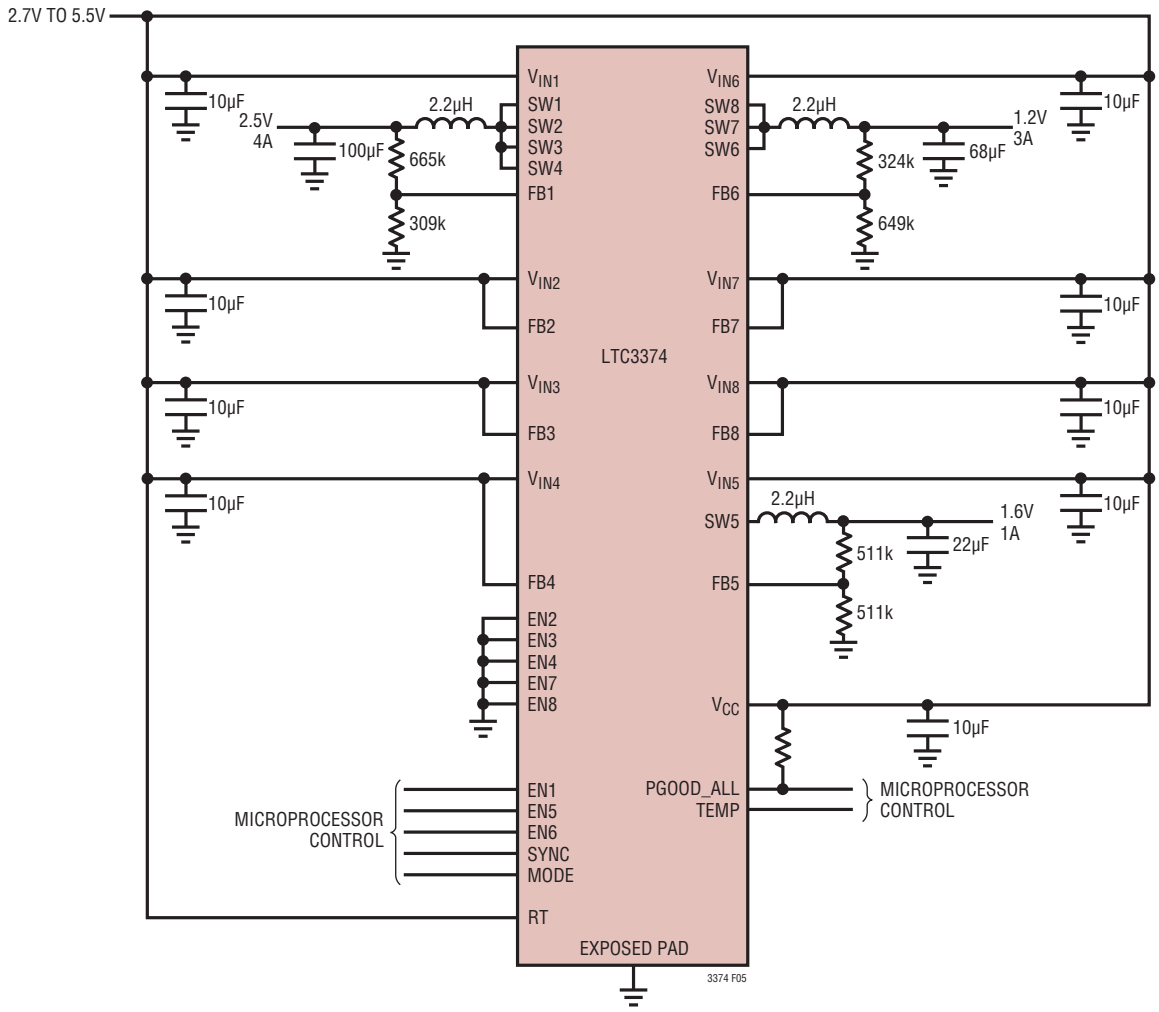
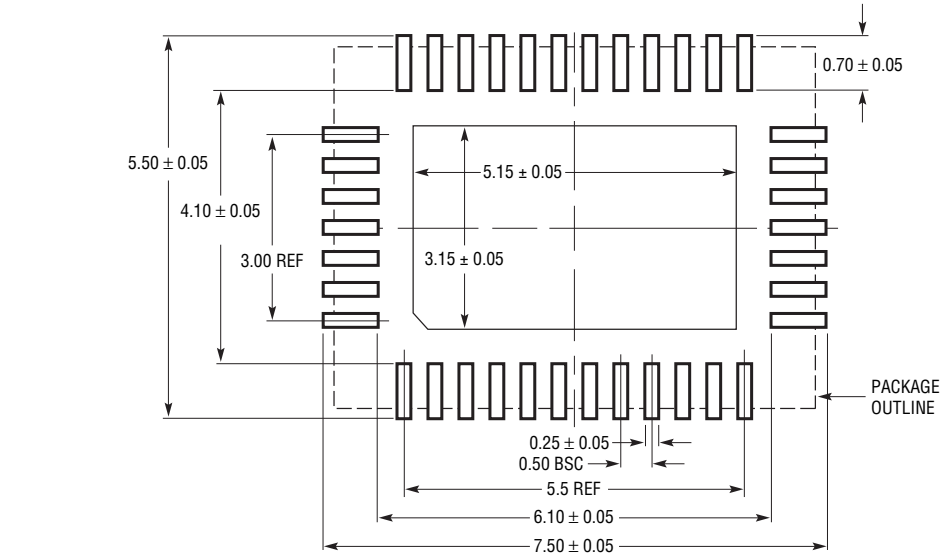


Figure 5. Combined Buck Regulators with Common Input Supply

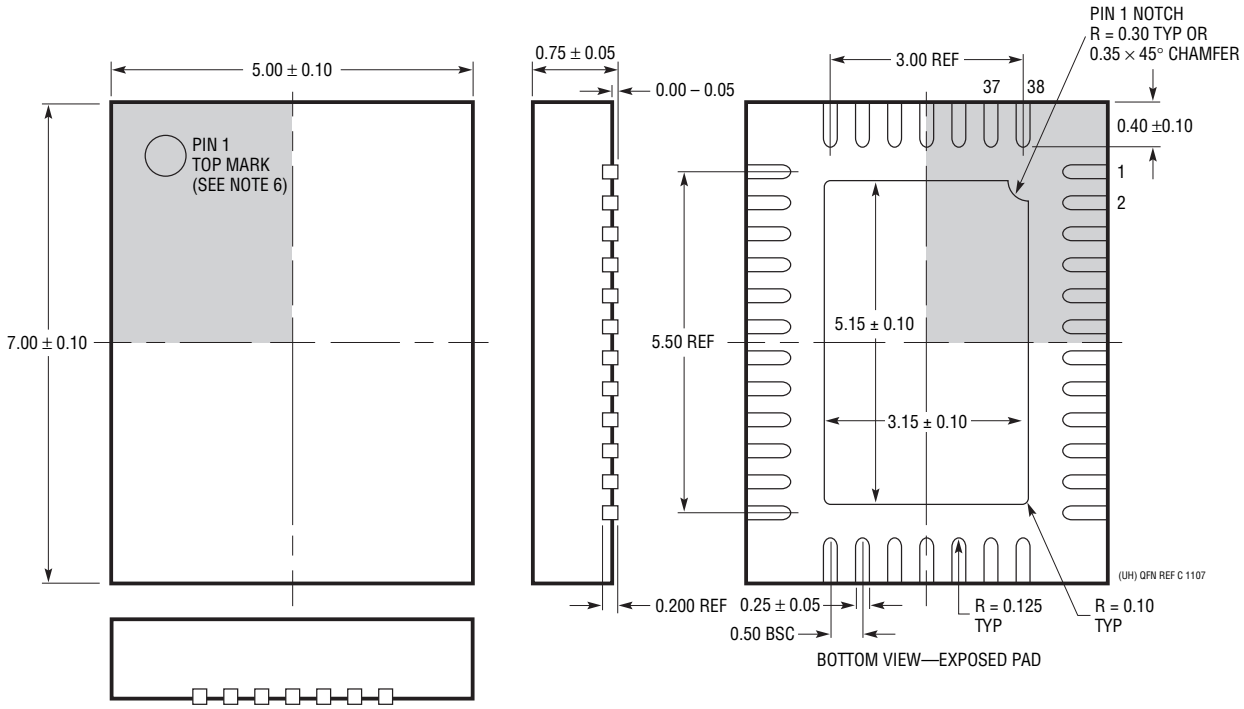
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3374#packaging for the most recent package drawings.

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701 Rev C)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

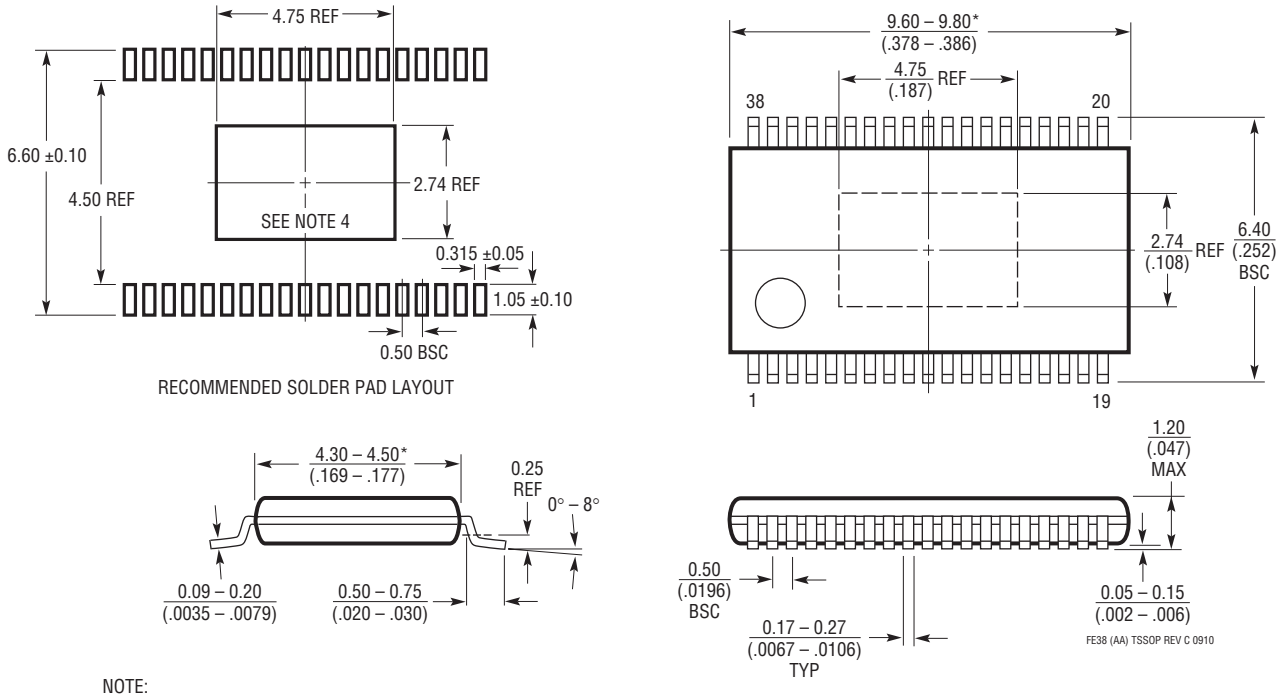


NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3374#packaging for the most recent package drawings.

FE Package
38-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1772 Rev C)
Exposed Pad Variation AA



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/13	Modified Figure 5 – removed a resistor.	22
B	06/15	Modified Typical Application circuit	1
		Changed part marking on TSSOP package	3
		Changed typical specifications: R_{PMOS} and R_{NMOS}	4
		Added conditions for V_{PGOOD} specifications	4
		Modified various curves	8, 9
		Modified Temperature Monitoring section	15
		Modified 2A inductor table	18
		Added Related Parts	26
C	10/15	Added Note 6 to t_{SS} specification	4, 5
		Modified conditions graphs G27, G28	9