Boost DC/DC Converter with APD Current Monitor

FEATURES

- **65V, 350mA Internal DMOS Switch**
- **Integrated Schottky Diode**
- **2% Accurate APD Current Monitoring Over the 3μA to 3mA Range**
- **Single Resistor Programs Maximum APD Current**
- **Fast APD Current Limiter with Indicator**
- **Programmable Loss-of-Signal Indicator**
- CTRL Pin Adjusts Output Voltage
- Programmable V_{IN} Undervoltage Lockout
- High Efficiency Step-Up Converter
- Selectable 1MHz/2MHz Switching Frequency
- Internally Compensated
- Internal Soft-Start
- 2.7V to 12V V_{IN} Range
- Low Shutdown Current: <1μA

APPLICATIONS

- APD Bias
- PIN Diode Bias
- Optical Receivers and Modules
- Fiber Optic Network Equipment

DESCRIPTION

The LT®3905 is a fixed frequency current-mode step-up converter designed to bias avalanche photodiodes (APD) in optical receivers. The LT3905 features high side APD current monitoring over four decades of dynamic range with better than 2% relative accuracy over the 3μA to 3mA range.

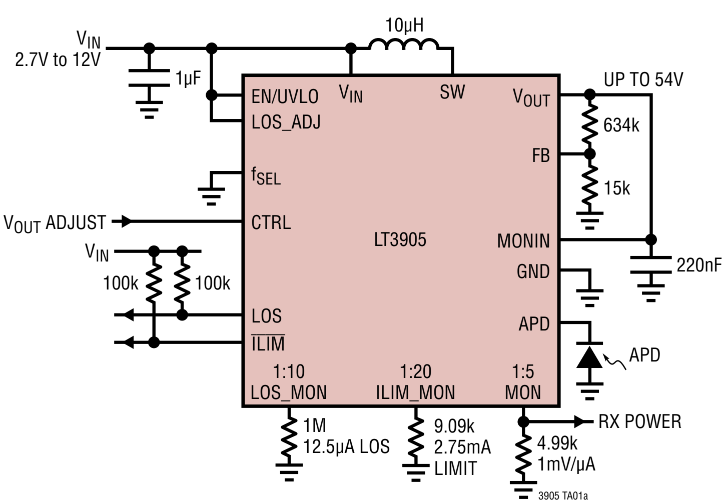
The maximum APD current is programmed with a single resistor, and a fast current limiter with indicator protects the APD during overload conditions. Adjustable output voltage provides dynamic bias control, and an adjustable loss-of-signal indicator flags low APD current.

Coupled with the integrated DMOS power switch and Schottky rectifier, the LT3905 provides a compact total solution with few external components and low solution cost. Constant switching frequency results in predictable output noise that is easy to filter.

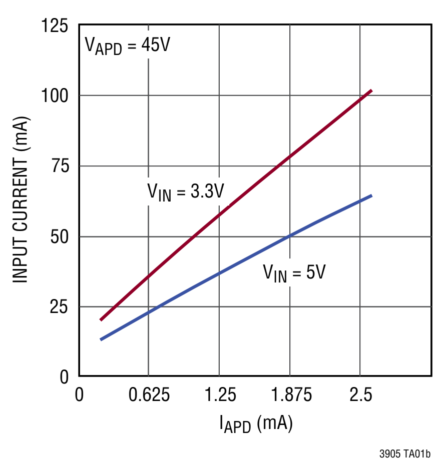
The LT3905 is available in the tiny footprint (3mm × 3mm) 16-Lead QFN Package.

TYPICAL APPLICATION

Adjustable APD Bias Supply



Input Current vs APD Current

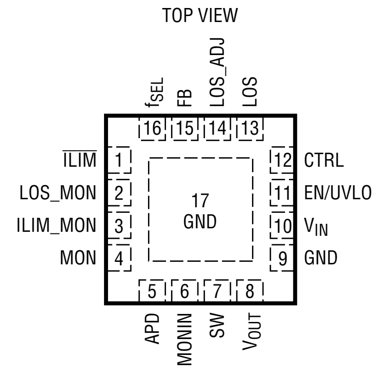


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, FB, EN/UVLO, CTRL, f_{SEL},
LOS_ADJ, LOS, $\overline{ILIM}$..12V
V_{OUT}, SW, MONIN, APD 65V
MON, LOS_MON, ILIM_MON 2.5V
Operating Ambient Temperature Range
(Note 2)...–40 to 125°C
Operating Junction Temperature Range
(Note 2)...–40 to 125°C
Storage Temperature Range ....–65 to 125°C

PIN CONFIGURATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
θ_{JA} = 68°C/W, θ_{JC} = 7.5°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3905EUD#PBF	LT3905EUD#TRPBF	LGGP	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LT3905IUD#PBF	LT3905IUD#TRPBF	LGGP	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{ENUVLO} = V_{CTRL} = 3.3V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range			2.7		12	V
Supply Current	V_{ENUVLO} = 0V, Device in Shutdown V_{ENUVLO} = 1.1V, Before Trip Point V_{ENUVLO} = 1.3V, V_{FB} = 2V, Switcher Standby V_{ENUVLO} = 1.3V, V_{FB} = 1.5V, Not Switching			0.1 6 250 650	1 10 350 750	µA µA µA µA
Feedback Voltage (V_{FB})	V_{CTRL} = 1.5V	 ●	1.238 1.223	1.248	1.258 1.273	V V
Feedback Line Regulation	2.7V ≤ V_{IN} ≤ 12V			0.005	0.025	%/V
FB Pin Bias Current		●		15	75	nA
FB Standby Threshold	V_{FB} Rising		1.65	1.80	1.95	V
FB Standby Threshold Hysteresis				50		mV
CTRL to FB Offset	V_{CTRL} = 0.5V	●	–13	0	13	mV
CTRL Input Bias Current	Current Out of Pin, V_{CTRL} = 0.5V	●		15	75	nA
MON Pin Voltage Clamp	I_{APD} = 300µA, R_{MON} = Open	●		2.35	2.5	V
LOS_MON Pin Voltage Clamp	I_{APD} = 300µA, R_{LOS_MON} = Open	●		2.35	2.5	V
MON Pin Bias Current	Current Out of Pin, I_{APD} = 0A, V_{MON} = 1V			0		nA
LOS_MON Pin Bias Current	Current Out of Pin, I_{APD} = 0A, V_{LOS_MON} = 1V			10	50	nA
ILIM_MON Pin Bias Current	Current Out of Pin, I_{APD} = 0A, V_{ILIM_MON} = 1V			35	175	nA
APD Monitor (MON) Current Gain	300nA ≤ I_{APD} ≤ 3µA, 12V ≤ MONIN ≤ 65V 3µA ≤ I_{APD} ≤ 3mA, 12V ≤ MONIN ≤ 65V	● ●	0.185 0.196	0.20 0.20	0.215 0.204	
APD Loss of Signal Monitor (LOS_MON) Current Gain	3µA ≤ I_{APD} ≤ 30µA, 12V ≤ MONIN ≤ 65V 30µA ≤ I_{APD} ≤ 3mA, 12V ≤ MONIN ≤ 65V	● ●	0.092 0.096	0.10 0.10	0.108 0.104	
APD Current Limit Monitor (ILIM_MON) Current Gain	30µA ≤ I_{APD} ≤ 300µA, 12V ≤ MONIN ≤ 65V 300µA ≤ I_{APD} ≤ 3mA, 12V ≤ MONIN ≤ 65V	● ●	0.045 0.048	0.05 0.05	0.055 0.052	
APD Monitor Voltage Drop	MONIN – APD at I_{APD} = 3mA, MONIN = 65V		3.7	3.95	4.2	V
Boost Converter						
Switching Frequency	f_{SEL} = 0V f_{SEL} = 2V	● ●	0.9 1.8	1 2	1.1 2.2	MHz MHz
Maximum Duty Cycle	f_{SEL} = 0V f_{SEL} = 2V		90 80	95 90		% %
Switch Current Limit			350	400	450	mA
Switch On-Resistance	I_{SW} = 150mA			0.75		Ω
Switch Leakage Current	SW = 65V			0.1	3	µA
Schottky Forward Voltage	$I_{SCHOTTKY}$ = 150mA			780		mV
Schottky Reverse Leakage	V_{OUT} – SW = 65V				3	µA
Loss Of Signal Comparator						
Loss of Signal Comparator Internal Threshold	LOS_ADJ = 1.5V, LOS_MON Falling		1.185	1.248	1.310	V
Loss of Signal Comparator External Threshold	LOS_ADJ = 1.0V, LOS_MON Falling	●	0.950		1.050	V
Loss of Signal Comparator Hysteresis	LOS_MON Rising			20		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $V_{IN} = V_{ENUVLO} = V_{CTRL} = 3.3V$ unless otherwise noted.

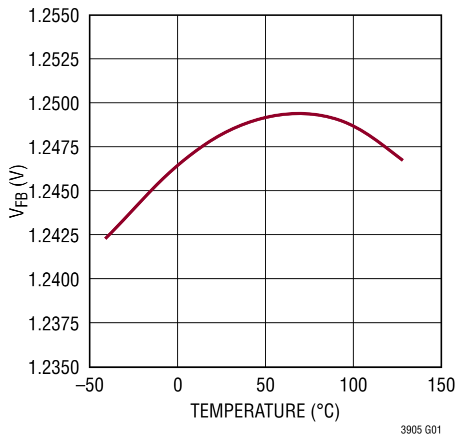
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Regulation Buffer Amplifier						
ILIM_MON Voltage Regulation Threshold (V_{IFB})	V_{FB} = 0.5V	 ●	1.223 1.211	1.248	1.273 1.285	V V
ILIM_MON APD Current Limit Threshold (V_{ILIM})		 ●	1.323 1.311	1.348	1.373 1.385	V V
ILIM_MON APD Current Limit Line Regulation	V_{APD} = 0V, $\Delta I_{APD}/\Delta V_{MONIN}$, 5V < V_{MONIN} < 65V			10		µA/V
ILIM_MON Indicator Threshold	V_{ILIM_MON} Rising	●	V_{ILIM} – 30	V_{ILIM} – 10	V_{ILIM} – 2	mV
ILIM_MON Indicator Hysteresis				30		mV
Inputs/Outputs						
EN/UVLO Threshold	V_{ENUVLO} Falling	 ●	1.128 1.104	1.200 1.200	1.272 1.296	V V
EN/UVLO Internal Hysteresis	V_{ENUVLO} Rising			25		mV
EN/UVLO Hysteresis Current	V_{ENUVLO} = 1.1V, Device in Shutdown V_{ENUVLO} = 1.3V, Device in Operation			3 0		µA µA
f_{SEL} Voltage Threshold	f_{SEL} Rising		0.700	0.900	1.100	V
f_{SEL} Threshold Hysteresis				50		mV
f_{SEL} Input Bias Current				0		µA
LOS Open Drain ON Resistance	I_{LOS} = 1mA			100		Ω
LOS Output Low Voltage	I_{LOS} = 2mA				0.3	V
LOS Off-State Leakage	$V_{IN} = V_{LOS}$ = 12V				1	µA
$\overline{\text{ILIM}}$ Open Drain ON Resistance	$I_{\overline{ILIM}}$ = 1mA			100		Ω
$\overline{\text{ILIM}}$ Output Low Voltage	$I_{\overline{ILIM}}$ = 2mA				0.3	V
$\overline{\text{ILIM}}$ Off-State Leakage	$V_{\overline{ILIM}}$ = 12V				1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

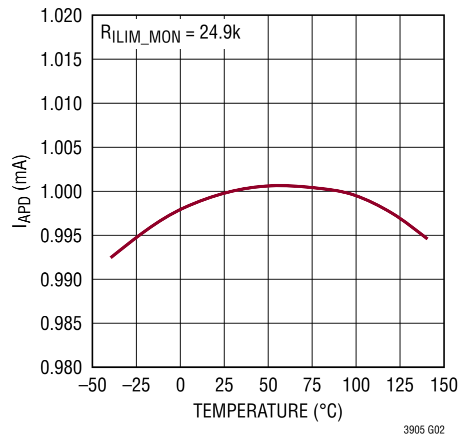
Note 2: The LT3905E is guaranteed to meet specified performance from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LT3905I is guaranteed to meet performance specifications over the –40°C to 125°C operating junction temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

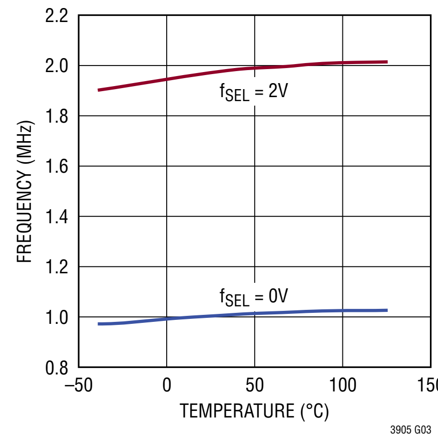
FB Voltage vs Temperature



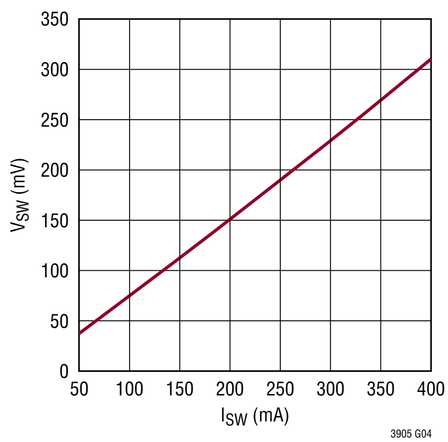
APD Current Regulation vs Temperature



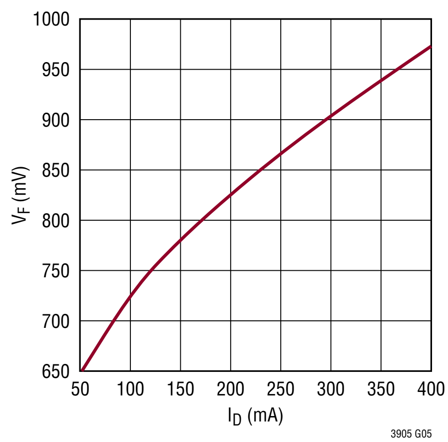
Oscillator Frequency vs Temperature



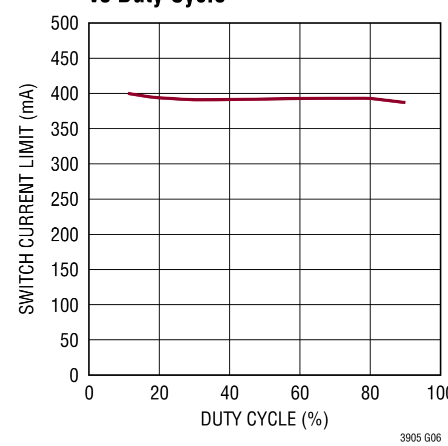
Switch Resistive Drop vs Switch Current



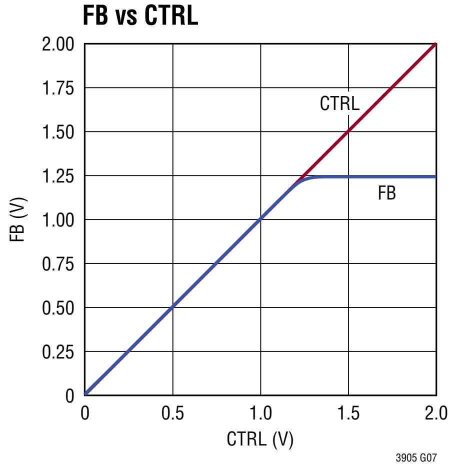
Diode Forward Drop vs Diode Current



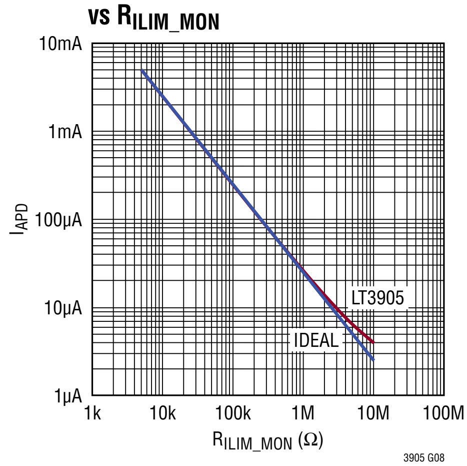
Switch Current Limit vs Duty Cycle



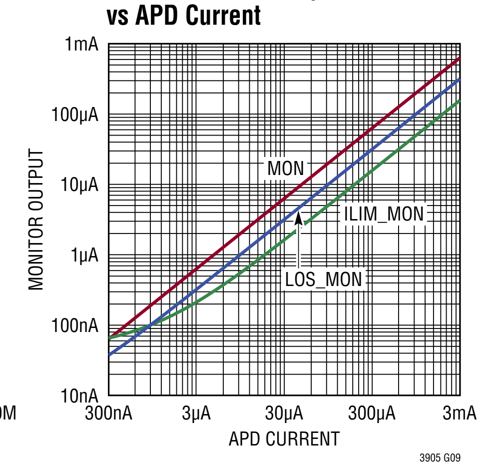
FB vs CTRL



LT3905 Current Regulation vs R_{ILIM_MON}

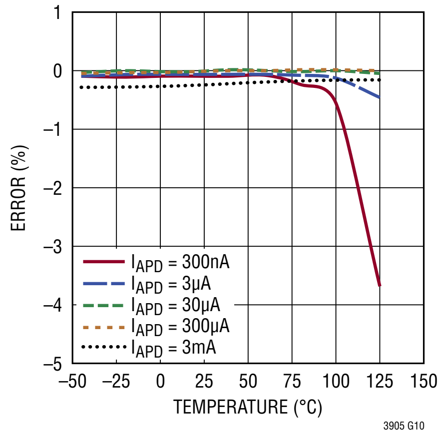


Current Monitor Outputs vs APD Current

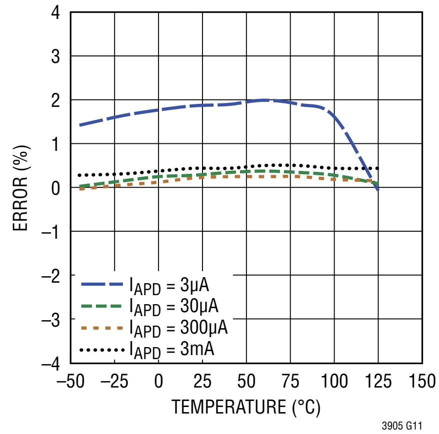


TYPICAL PERFORMANCE CHARACTERISTICS

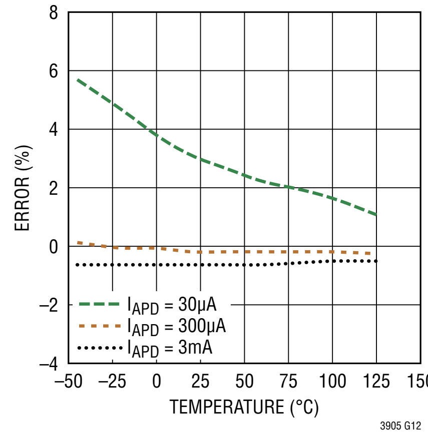
MON Accuracy vs Temperature



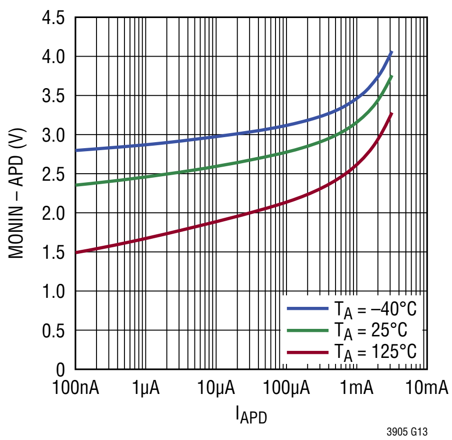
LOS_MON Accuracy vs Temperature



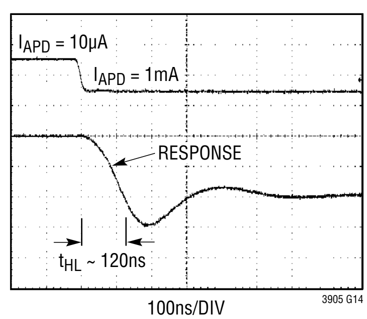
ILIM_MON Accuracy vs Temperature



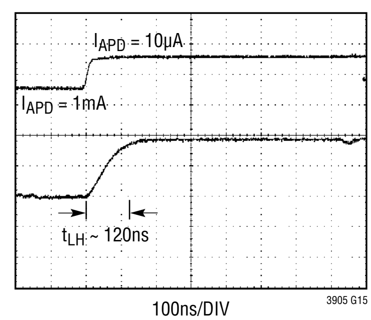
Current Monitor Voltage Drop vs APD Current



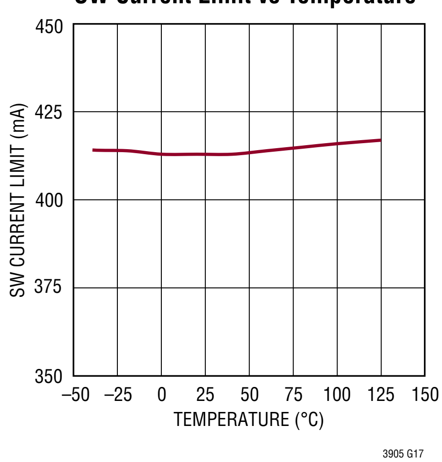
Current Monitor Transient Response (Rising Edge)



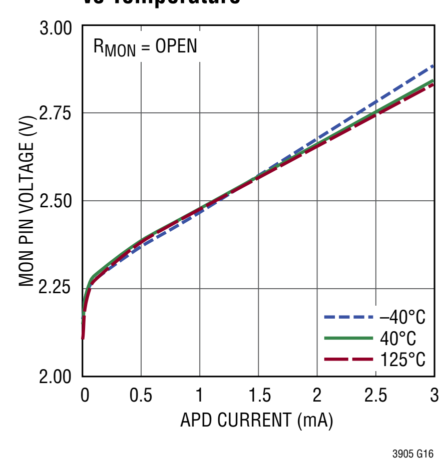
Current Monitor Transient Response (Falling Edge)



SW Current Limit vs Temperature



MON Clamp Voltage vs Temperature



PIN FUNCTIONS

$\overline{\text{ILIM}}$ (Pin 1): Open Drain Overload Indicator. $\overline{\text{ILIM}}$ pulls low when the voltage on ILIM_MON reaches the 1.348V threshold, and releases when ILIM_MON drops by 50mV. Tie this pin to desired logic high voltage with an external pull-up resistor. The maximum recommended sink current is 2mA to prevent excess power dissipation. Leave this pin open if unused.

LOS_MON (Pin 2): Loss of Signal Monitor. This pin sources a current proportional to 10% of the APD current, and acts as the positive input for the Loss of Signal comparator. It is clamped to 2.25V through an internal diode. Tie a resistor from LOS_MON to GND to set the Loss of Signal gain. Tie this pin to GND if unused.

ILIM_MON (Pin 3): APD Overload Monitor. This pin sources a current proportional to 5% of the APD current, and acts as the negative input for the current regulation loop and the APD current limiter. It is clamped to 2.25V through an internal diode. Tie a resistor from ILIM_MON to GND to set the gain. If ILIM_MON exceeds the 1.248V setpoint, the current regulation loop will first throttle back the boost converter output voltage. If ILIM_MON reaches the 1.348V threshold, the $\overline{\text{ILIM}}$ indicator is pulled low and the APD current is actively limited. This pin cannot be allowed to float, tie this pin to GND if unused.

MON (Pin 4): Current Monitor Output Pin. This pin sources a current proportional to 20% of the APD current for external current monitoring. It is clamped to 2.25V through an internal diode. Tie a resistor from MON to GND to set the current monitor gain.

APD (Pin 5): Connect APD cathode to this pin. The maximum current of this pin is 7mA (typ).

MONIN (Pin 6): Power Supply for the APD and All Current Monitors. Connect to V_{OUT} through an external lowpass filter for lowest noise operation.

SW (Pin 7): Switch Pin. Drain of internal power FET and anode of internal power Schottky. Connect to switching side of inductor. Minimize the trace length on this pin to reduce EMI.

V_{OUT} (Pin 8): Boost Converter Output Pin. Cathode of internal power Schottky. Connect an output voltage smoothing capacitor from V_{OUT} to GND.

GND (Pin 9, Exposed Pad Pin 17): Ground. Tie to the exposed pad. The exposed pad must be soldered to a large PCB copper area for proper functionality and heat sinking.

V_{IN} (Pin 10): Input Supply Pin. Bypass this pin with a capacitor to GND as close to the IC as possible.

EN/UVLO (Pin 11): Master Enable and V_{IN} Undervoltage Lockout. When low, the IC is put into shutdown mode and quiescent current is reduced to <1µA. This pin contains a 1.2V comparator with 25mV internal hysteresis and a 3µA hysteresis current source for programmable external hysteresis. Connect to a resistor divider between V_{IN} and GND to program the enable/disable thresholds, or drive with a digital signal greater than 1.5V for simple ON/OFF control.

CTRL (Pin 12): External Reference Input. When CTRL is lower than 1.248V, it acts as an external reference to the FB error amp. If unused, tie CTRL to V_{IN}.

LOS (Pin 13): Open Drain Loss of Signal Indicator. LOS goes high when the voltage on LOS_MON is below the voltage on LOS_ADJ. Tie this pin to desired logic high voltage with an external pull-up resistor. The maximum recommended sink current is 2mA to prevent excess power dissipation. Leave this pin open if unused.

LOS_ADJ (Pin 14): External Reference Input for the Loss of Signal Indicator. This pin feeds the negative input of the loss of signal comparator, and provides 20mV internal hysteresis. For additional external hysteresis, use a resistor network between LOS and LOS_ADJ. Tie this pin to V_{IN} for a fixed 1.248V threshold, or if unused.

FB (Pin 15): Feedback Pin. Connect to a resistor divider between V_{OUT} and GND to limit the output voltage. The internal reference for this pin is 1.248V. Pull this pin above 1.8V to disable the step-up converter and operate the Loss of Signal monitor standalone.

f_{SEL} (Pin 16): Frequency Selector. Tie to V_{IN} for 2MHz operation, or tie to GND for 1MHz operation.

BLOCK DIAGRAM

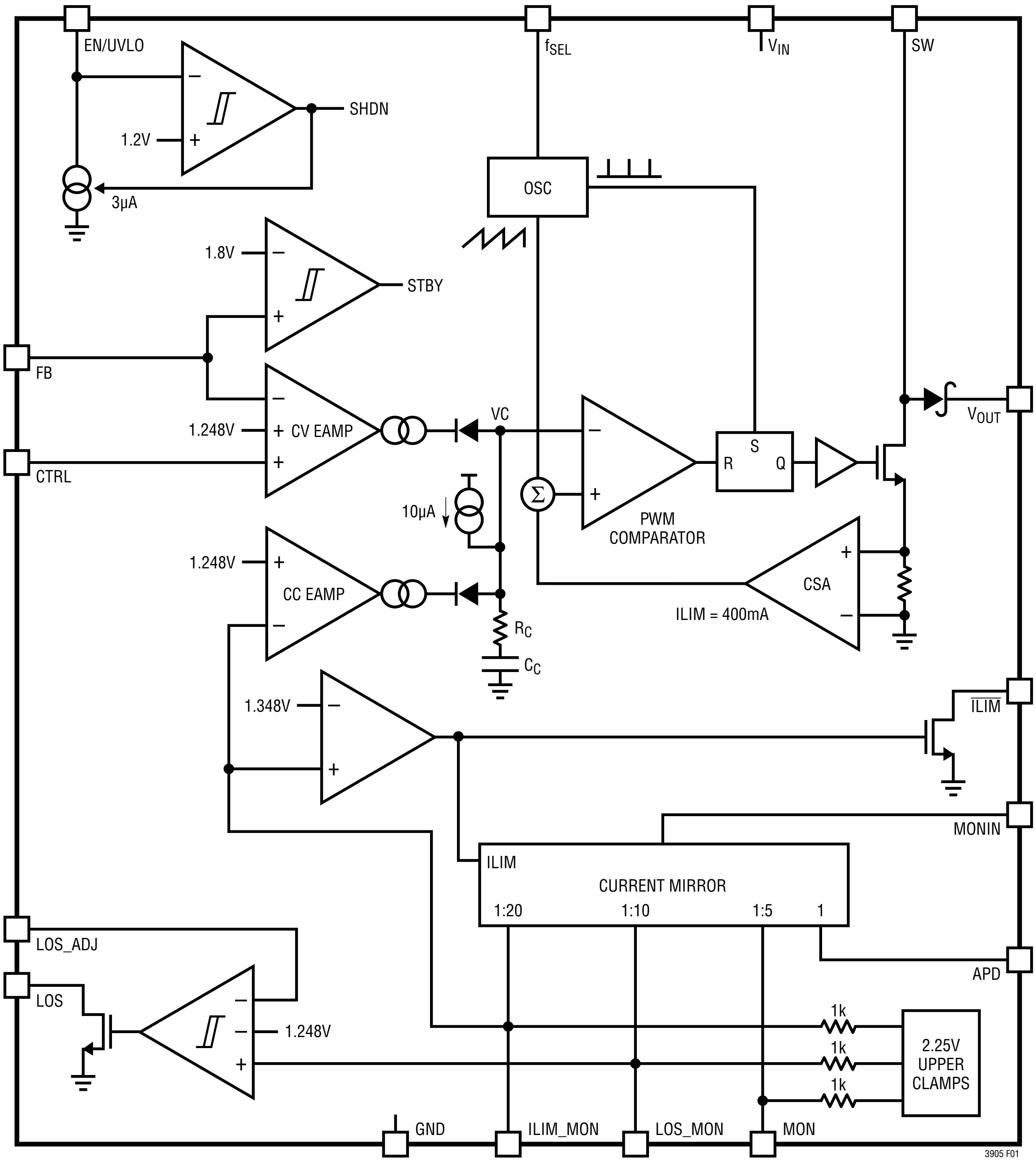


Figure 1. Block Diagram

OPERATION

Overview

The LT3905 combines a 65V current mode step-up DC/DC converter with a combination APD current monitor and regulator to provide accurate monitoring and efficient supply while offering additional flexibility and protection.

The step-up converter utilizes a 65V, 0.75Ω DMOS power switch and integrated Schottky diode to convert a low input voltage to a higher voltage appropriate for powering the APD. The operation of the step-up converter is a fixed frequency, current mode topology with internal compensation and accurate current limit. Operation is best understood by referring to the Block Diagram in Figure 1.

At the start of each oscillator cycle, the SR latch is set, which turns on the internal DMOS power switch. Current begins to rise in the inductor and power switch, and this switch current is sensed and added to a stabilizing ramp. The resulting sum is fed to the positive terminal of the PWM comparator. The level at the negative terminal of the PWM comparator is set by the integrated error signal, VC. When the current sense signal exceeds the VC threshold or the fixed 400mA current limit, the SR latch is reset and the power switch turns off for the remainder of the cycle. The stored energy in the inductor transfers through the Schottky diode to the output capacitor, raising the output voltage.

This output voltage is externally filtered and returned to the current monitor through the MONIN pin. The avalanche photodiode is then biased from the APD pin, which allows the monitor to both sense the APD current as well as to limit it in an overload condition.

The monitor provides three currents proportional to APD current on the MON (1:5), LOS_MON (1:10), and ILIM_MON (1:20) pins. Resistors at these pins convert the output currents to voltages suitable for monitoring and regulating the APD current. In addition, the LOS_MON and ILIM_MON have special functions used for loss-of-signal and overload cases. These functions are described in detail in the sections regarding these pins.

The step-up converter output is controlled through either the FB or ILIM_MON voltages. A fixed or maximum output voltage is programmed using the FB pin, and an adaptive output voltage for fixed APD current is programmed using the ILIM_MON pin.

The reference voltage for the FB pin can also be supplied externally through the CTRL pin, for external adjustment of output voltage.

APPLICATIONS INFORMATION

Switching Frequency

The LT3905 allows selection between 1MHz and 2MHz switching frequency. Tie the f_{SEL} pin to a voltage greater than 0.9V to select 2MHz mode, or tie to GND to select 1MHz mode.

Inrush Current

Due to the Schottky diode in the boost converter, a DC path exists from V_{IN} to V_{OUT} through the power inductor. When supply voltage is applied to the V_{IN} pin, an inrush current will flow through the inductor to charge the output capacitor.

The selection of inductor and capacitor should be chosen to keep the peak inrush current below 1A. The peak in-rush current is estimated as follows:

$$I_p = \frac{V_{IN} - 0.9}{\mathrm{sqrt}\left(\frac{L}{C} - 1\right)} \bullet e\left(\frac{-pi}{2 \bullet \mathrm{sqrt}\left(\frac{L}{C} - 1\right)}\right)$$

Where L is the power inductor value, and C is the output capacitor value.

Table 1 gives inrush peak currents for some typical component values.

APPLICATIONS INFORMATION

Table 1. Inrush Peak Current

V_{IN} (V)	L (µH)	C (µF)	I_P (A)
3.3	10	1	0.47
3.3	22	1	0.37
5	10	1	0.81
5	22	1	0.63

Voltage Feedback

The LT3905 error amplifier is equipped with both a fixed internal reference of 1.248V and an adjustable external reference input (CTRL). This feature allows users to select between using the built-in reference and an external reference voltage when programming the output voltage. It is possible to adjust the voltage at the CTRL pin while the device is operating, in order to alter the output voltage of LT3905 and therefore the bias voltage of the APD.

To choose the fixed internal reference, tie the CTRL pin to a voltage higher than 1.5V, such as the input voltage. The FB pin is regulated to 1.248V. When the CTRL pin is below 1.248V, the FB pin is regulated to the voltage at the CTRL pin.

To set the output voltage, tie FB to a resistor divider between MONIN and GND. The R2 value can be selected to provide a minimum load to the device, to maintain a constant switching frequency when the APD current is very low. Preventing entry into pulse-skipping mode is an important consideration for post-filtering the regulator output.

The value of R1 is determined using the desired output voltage and the reference voltage, V_{REF}. Where V_{REF} is either the internal or external reference voltage as defined by the state of the CTRL pin, and R2 is the resistor value previously selected for minimum load.

$$R1 = R2\left(\frac{V_{MONIN}}{V_{REF}} - 1\right)$$

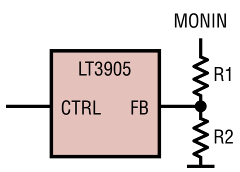


Figure 2. Output Voltage Feedback

Converter Standby

It is also possible to put the switching converter in standby mode by driving FB to a voltage higher than 1.8V. In this mode, only the internal reference and the LOS_MON circuitry remain active, and quiescent current drops to 250µA.

Inductor Selection

The inductor used with LT3905 should have a saturation rating of 400mA or greater. If the device is used in an application where the input supply is hot-plugged, the saturation current should exceed the peak inrush current.

For best loop stability, the inductance value selected should provide a ripple current of 20% of current limit, or 80mA. For a given V_{IN} and V_{OUT}, the inductor value to use in continuous conduction mode is calculated by:

$$L = D \bullet \frac{V_{IN}}{f \bullet 80mA}$$

where:

$$D = \frac{V_{OUT} + 1 - V_{IN}}{V_{OUT} + 1}$$

and f is the switching frequency in Hz.

To force the LT3905 to operate in discontinuous conduction mode (DCM), select a smaller value inductor. The following inequality is true when the LT3905 is operating in discontinuous conduction mode.

$$L < \frac{D \bullet V_{IN}}{f \bullet 400mA}$$

Operating in DCM reduces the maximum output current and the conversion efficiency.

Capacitor Selection

Use low ESR capacitors at the output to minimize output voltage ripple. Use only X5R and X7R types, which retain their capacitance over wider voltage and temperature ranges than other types. High output voltages typically require less capacitance for loop stability. Typically use a 1µF capacitor for output voltage less than 25V and 0.22µF

APPLICATIONS INFORMATION

capacitor for output voltage beyond 25V. Place the output capacitor as close as possible to the V_{OUT} lead and to the GND of the IC.

Either ceramic or solid tantalum capacitors may be used for the input decoupling capacitor, which should be placed as close as possible to the LT3905. A 1µF capacitor is sufficient for most applications.

Phase Lead Capacitor

A small value capacitor (i.e., 10pF to 22pF) can be added in parallel with the R1 resistor between the output and the FB pin to reduce output perturbation due to a load step and to improve transient response. This phase lead capacitor introduces a pole-zero pair to the feedback that boosts phase margin near the crossover frequency. The APD is very sensitive to a noisy bias supply. To lowpass filter noise from the internal reference and error amplifier, a 0.1µF phase lead capacitor can be used. The corner frequency of the noise filter is R1 • CPL.

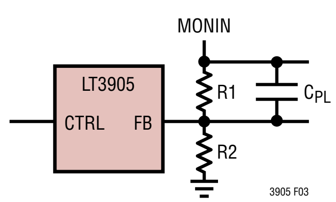


Figure 3. Phase Lead Capacitor

APD Current Monitor

The APD current Monitor is supplied from the MONIN pin. It provides a current-limited power supply for the avalanche photodiode on the APD pin, and outputs three monitor currents proportional to the APD current on the MON, LOS_MON, and ILIM_MON pins. Each of the monitor outputs is diode-clamped to a 2.25V internal voltage.

The largest output current is the MON output, at 20% of the APD current. This output is typically used for precise system monitoring of the APD bias point, and is tied either to a resistor to GND or to the input of a transimpedance amplifier. In either case, it is important to keep the MON voltage lower than 2.1V, as forward-biasing the internal diode will clamp the MON voltage and compromise accuracy.

Loss of Signal Monitor

The second largest output current is the LOS_MON output, at 10% of the APD current. This is typically used for detecting a loss of signal condition by sensing a drop in the APD current. The LOS_MON pin is an input to the comparator that drives the open-drain LOS pin. This comparator uses either a fixed internal threshold of 1.248V, activated by pulling the LOS_ADJ pin to V_{IN}, or an adjustable external threshold, activated by driving the LOS_ADJ pin with a voltage lower than 1.248V. In either case, the open-drain LOS pin goes high when the voltage on LOS_MON falls below the threshold.

To program the loss of signal monitor, set a resistor from LOS_MON to ground such that the LOS_MON voltage reaches the loss of signal threshold at the point the APD current has dropped to the desired loss of signal threshold, $IAPD_{LOS}$.

For the case of internal threshold:

$$R_{LOS\_MON} = \frac{10 \bullet 1.248V}{IAPD_{LOS}}$$

For the case of external threshold, simply replace 1.248V in the above equation with the external threshold applied to the LOS_ADJ pin:

$$R_{LOS\_MON} = \frac{10 \bullet V_{LOS\_ADJ}}{IAPD_{LOS}}$$

Loss of Signal Hysteresis

The LOS_MON comparator contains internal hysteresis of typically 20mV on the rising edge of the LOS_MON voltage. When using an external threshold, additional external hysteresis can be generated with the addition of the resistors R7 and R8 shown in Figure 4, where R10 is the standard pull-up resistor for the LOS signal.

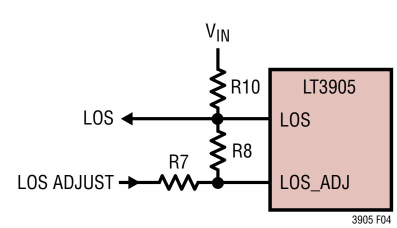


Figure 4. Additional LOS Hysteresis

APPLICATIONS INFORMATION

To compute the values of R7 and R8, start by setting R8 at least 10 times the value of the pull-up resistor R10. This will prevent undue loading of the LOS signal itself.

Next, compute the total hysteresis using the voltage divider generated by R7/R8:

$$V_H = V_{IN}\left(\frac{R7}{R7+R8}+20mV\right)$$

This hysteresis is composed of two parts, the hysteresis when LOS_MON is rising (leaving loss of signal) and that when LOS_MON is falling (entering loss of signal).

Use the formulas below with the value of external threshold applied to LOS ADJUST to calculate the new rising and falling thresholds of LOS_MON when using external hysteresis. Adjust the LOS_MON resistor if necessary to achieve a desired threshold with respect to APD current.

$$V_{LOS\_MON(FALL)} = V_{LOS\_ADJUST}\left(\frac{R8}{R7+R8}\right)$$

$$V_{LOS\_MON(RISE)} = V_{LOS\_ADJUST} + 20mV + \left(R7 \bullet \frac{V_{IN} - V_{LOS\_ADJUST}}{R7+R8}\right)$$

Current Limit Monitor

The smallest output current is the ILIM_MON output, at 5% of the APD current. This output is used for regulating the boost converter to provide a fixed APD current, as well as detecting and limiting of overload conditions.

When the voltage at ILIM_MON reaches the first threshold of 1.248V, an auxiliary error amplifier limits the boost converter output voltage. In this manner, the LT3905 can regulate a fixed APD current with a single resistor at the ILIM_MON pin. In this mode, use the FB function to set a maximum output voltage limit. The FB resistor divider should be set for an output voltage higher than the expected output voltage required for the APD and monitor drop. The ILIM_MON error amplifier is the dominant regulation path, and the FB error amplifier will only take over to limit the output voltage in the case of a disconnected APD.

For this strategy, the ILIM_MON resistor is selected so the ILIM_MON pin reaches 1.248V at the desired APD regulation current, $IAPD_{REG}$.

$$R_{ILIM\_MON} = \frac{20 \bullet 1.248V}{IAPD_{REG}}$$

Although this loop will effectively limit the output voltage to that which is needed to regulate the APD current, the fast overload case must be considered as well. The regulation of the boost converter output is comparatively slow with respect to an APD overload condition. Additionally, substantial energy is stored in the charged output capacitor that should be prevented from flowing into the APD during a condition of optical flooding. To protect against this type of overload, the ILIM_MON pin has a fast current regulator which limits the output current of the APD pin itself. This current limiting loop has a threshold 100mV above the 1.248V boost regulation threshold, and two actions are taken if this threshold is reached.

First, the output current of the APD pin is limited to the value corresponding to 1.348V on ILIM_MON. For a shorted or optically flooded APD, the voltage at the APD pin will drop to any level necessary to limit the current to the programmed value. Even for the case of the APD pin shorted to GND, the current will remain limited to the programmed value and ILIM_MON will continue to indicate an accurate measurement of APD current.

The second action that is taken in response to an overload condition is assertion of the open-drain $\overline{ILIM}$ flag to indicate the overload condition to the user. It is asserted once the ILIM_MON voltage exceeds 1.348V and enters active limiting, and will remain asserted until the ILIM_MON voltage has dropped by 50mV, indicating that the device is no longer in active limiting.

The response of the APD current limiter is shown in Figure 5. When the overload is applied, the APD voltage drops abruptly while the output voltage decays slowly due to the regulated current load. As the output voltage reaches the new operating point, the $\overline{ILIM}$ indicator is released and the boost converter begins regulating to 1.248V on ILIM_MON.

APPLICATIONS INFORMATION

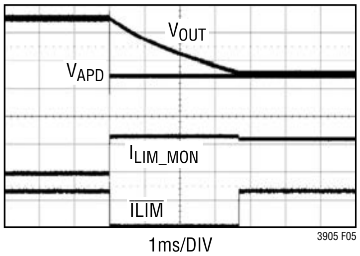


Figure 5. APD Current Limiter Response

Although this greatly reduces the energy dissipated in the APD during overload, care must be taken that any bypass capacitors directly on the APD do not cause the overload surge to exceed recommended values.

In the case of a hard short on the APD pin, the APD pin current is regulated and the boost converter will not switch, but for high input voltages, the DC path from the input through the inductor and Schottky rectifier will continue to supply current to the shorted load. If this current is larger than the programmed current limit, the device will continue to regulate the output current of the APD pin, and to assert the $\overline{\text{ILIM}}$ flag until the short on the APD pin is removed.

APD Current Monitor Transient Response

The transient response of the APD current monitor is a key performance characteristic. It is essentially a function of the signal levels, since the small signal bandwidth increases with the input signal.

At greater than 10µA, the LT3905 APD current mirror typically has several hundred nanosecond response time. To measure such fast transient response, a wideband transimpedance amplifier is implemented using the LT6210 as shown in Figure 6. Operating in a shunt configuration, the amplifier buffers the MON output and dramatically reduces the effective output impedance. Note that there is an inversion and DC reference offset in the final measurement.

Layout Hints

The high speed operation of the LT3905 demands careful attention to board layout. You will not get advertised performance with careless layout. To prevent radiation

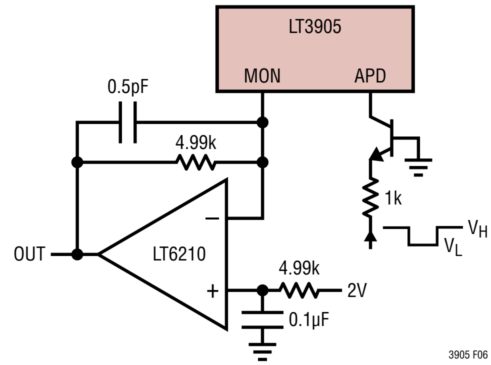


Figure 6. Transient Response Measurement Setup

and high frequency resonance problems, proper layout of the high frequency switching path is essential. Keep the output capacitor as close to the Schottky diode (V_{OUT} pin) as possible. Minimize the length and area of all traces connected to the switch pin, and always use a ground plane under the switching regulator to minimize interplane coupling. The high speed switching current path is shown in Figure 8. The signal path including the switch, output diode and output capacitor contains nanosecond rise and fall times and should be kept as short as possible.

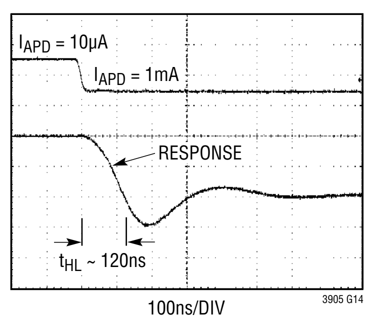


Figure 7. Typical 10µA to 1mA Step Transient Response

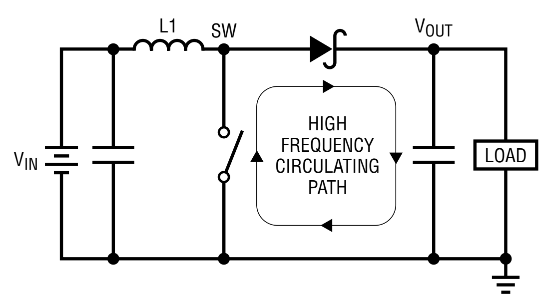
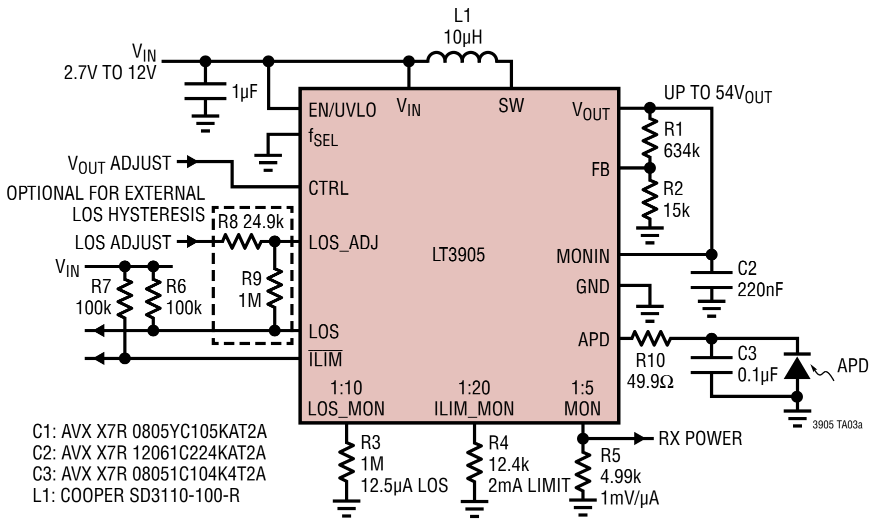


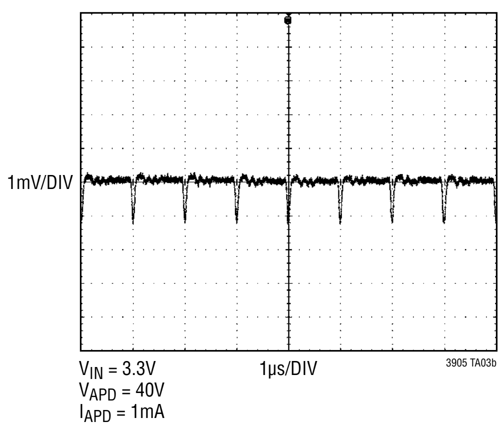
Figure 8. High Frequency Path

TYPICAL APPLICATIONS

Low Noise APD Bias with External LOS Threshold

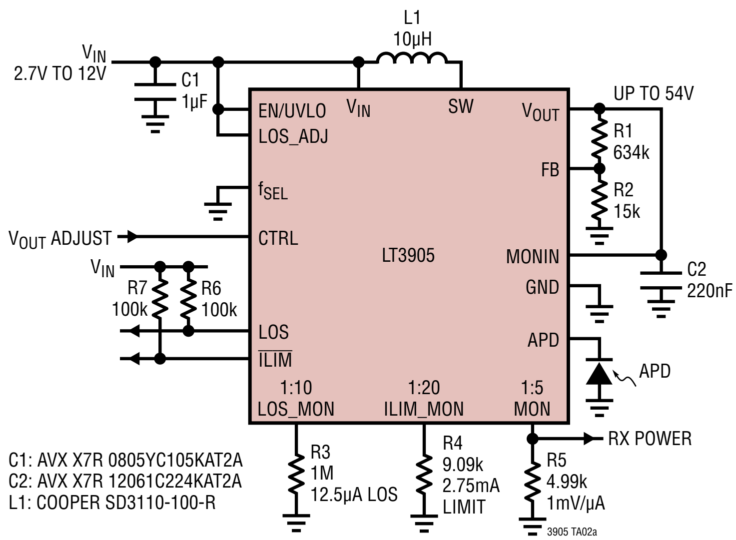


APD Bias Ripple

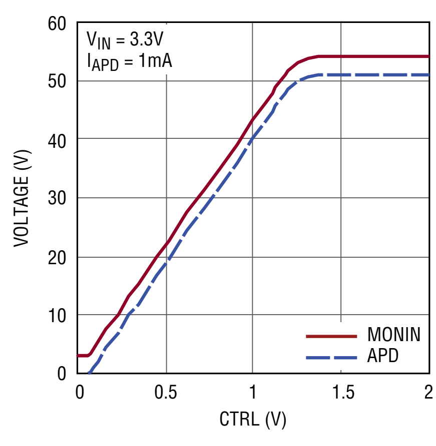


TYPICAL APPLICATIONS

Adjustable APD Bias Supply



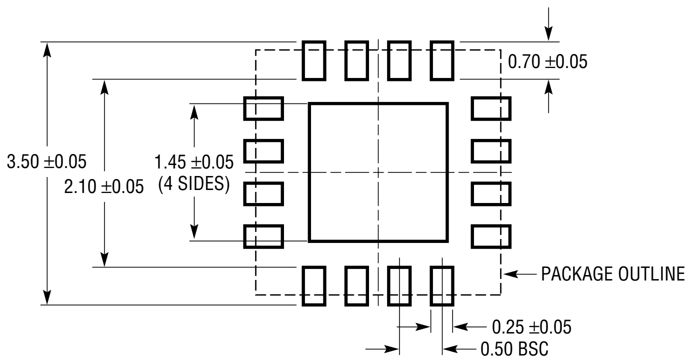
Output Voltage Adjustment Using CTRL



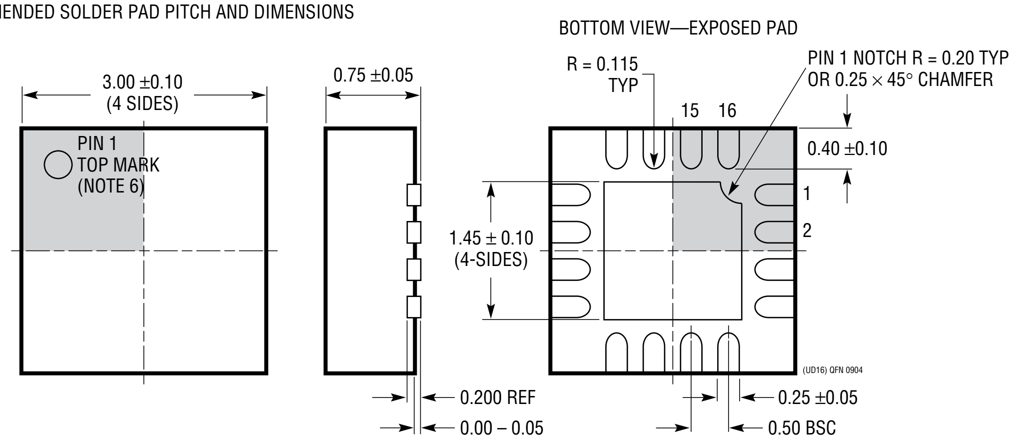
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/14	Clarified Description	1
		Clarified Block Diagram	8
		Clarified Applications Information	12
		Clarified APD Voltage Adjustment graph	15