USB 5V 2.5A Output, 42V Input Synchronous Buck with Cable Drop Compensation

FEATURES

- **Wide Input Range: 5V to 42V**
- **Low Dropout Under All Conditions: 450mV at 2.1A**
- **Accurate 5V Output: ±1.3% Over Full Temperature Range**
- **Programmable Cable Drop Compensation**
- **Programmable Output Current Limit**
- **Output Current Monitor**
- **Dual Input Feedback Permits Regulation on Output of USB Switch**
- **Forced Continuous Mode for Fast Load Step Response**
- High Efficiency Synchronous Operation at 2MHz:
  93% Efficiency at 2.1A, $5V_{OUT}$ from $12V_{IN}$
  95% Efficiency at 0.9A, $5V_{OUT}$ from $12V_{IN}$
- Fast Minimum Switch-On Time: 45ns
- Adjustable Output from 5.0V to 5.25V
- Adjustable and Synchronizable: 300kHz to 2.2MHz
- Small Thermally Enhanced 3mm × 5mm 24-Lead QFN Package

APPLICATIONS

- Automotive and Industrial USB
- Precision 5V Supply

DESCRIPTION

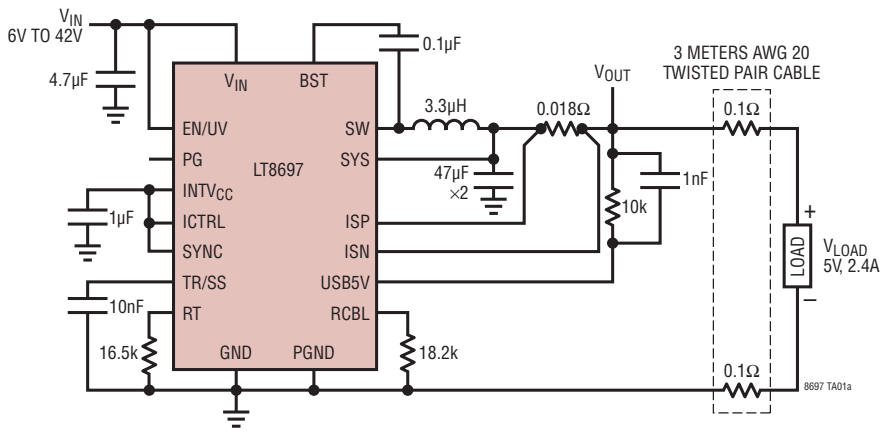
The LT®8697 is a compact, high efficiency, high speed synchronous monolithic step-down switching regulator designed to power 5V USB applications. A precise output voltage and programmable cable drop compensation maintain accurate 5V regulation at the USB socket connected to the end of a long cable. Forced continuous operation allows the LT8697 to sink current, further enhancing accurate 5V regulation during load transients.

Accurate and programmable output current limit, a power good indicator pin and an output current monitor pin improve system reliability and safety, allow the user to implement latch-off or auto-retry functionality and can eliminate the need for a USB switch IC. Dual feedback allows regulation on the output of a USB switch and limits cable drop compensation to a maximum of 5.8V output, protecting USB devices during fault conditions. Thermal shutdown provides additional protection by limiting power dissipation in the IC during an overtemperature fault.

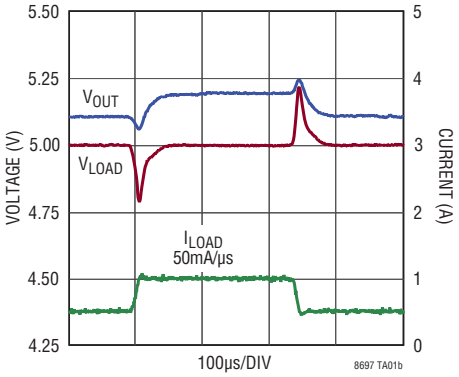
The LT8697 is available in a small 24-lead 3mm × 5mm package with an exposed pad for low thermal resistance.

TYPICAL APPLICATION

2MHz 5V Step-Down Converter with Cable Drop Compensation



Transient Response Through 3 Meters AWG 20 Twisted-Pair Cable

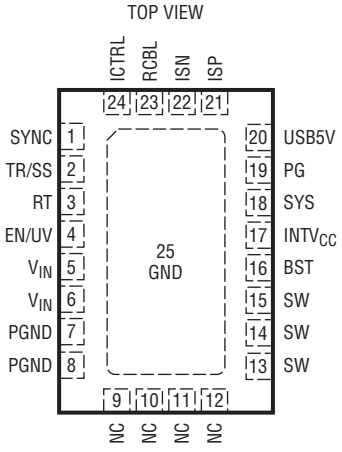


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, EN/UV, PG, ISP, ISN 42V
SYS 30V
USB5V 3mA
BST Above SW 4V
TR/SS, ICTRL 4V
RT, RCBL 2V
SYNC 6V
Operating Junction Temperature Range (Notes 2, 3)
LT8697E ..... –40°C to 125°C
LT8697I ..... –40°C to 125°C
LT8697H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UDD PACKAGE
24-LEAD (3mm × 5mm) PLASTIC QFN

θ_{JA} = 46°C/W, θ_{JC} = 5°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8697EUDD#PBF	LT8697EUDD#TRPBF	LGGW	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 125°C
LT8697IUDD#PBF	LT8697IUDD#TRPBF	LGGW	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 125°C
LT8697HUDD#PBF	LT8697HUDD#TRPBF	LGGW	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 2, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} Undervoltage Lockout		●		2.9	3.4	V
V_{IN} Shutdown Current	$V_{EN/UV}$ = 0.3V	 ●		1	3 8	µA µA
V_{IN} Current in Regulation	V_{IN} = 12V, I_{LOAD} = 100µA, R_T = 56.2k	●		9	12	mA
V_{IN} to Disable Forced Continuous Mode	V_{IN} Rising	●	27	29	31	V
Output Sink Current in Forced Continuous Mode	V_{USB5V} = 5.5V, L = 6.8µH, R_T = 56.2k		0.6	1	1.7	A
USB5V Voltage	V_{IN} = 12V	 ●	4.96 4.91	4.99 4.99	5.02 5.04	V V
USB5V Voltage Line Regulation	V_{IN} = 6V to 42V	●		6	25	mV
Regulated Load Voltage Through 0.3Ω	V_{IN} = 12V, I_{LOAD} = 2.1A, Voltage at Point of Load (End of Cable), R_{CBL} = 13.7k, R_{CDC} = 10k, R_{SENSE} = 20mΩ	●	4.925	5	5.075	V
USB5V Clamp Voltage	I_{USB5V} = 3mA			9		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 2, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
USB5V Current	V_{ISN} = 5V, $V_{ISP} - V_{ISN}$ = 40mV, R_{CBL} = 13.7k	●	57.5	60	62.5	µA
	V_{ISN} = 5V, $V_{ISP} - V_{ISN}$ = 10mV, R_{CBL} = 13.7k	●	12	15	23	µA
	V_{ISN} = 5V, $V_{ISP} - V_{ISN}$ = 0V, R_{CBL} = 13.7k	●	0	2	8	µA
	R_{CBL} = Open	●	0	1	2	µA
Current Sense Voltage ($V_{ISP} - V_{ISN}$)	V_{CTRL} = 1.5V, V_{ISN} = 5V	●	45	48	51	mV
	V_{CTRL} = 1.5V, V_{ISN} = 0V	●	43	48.5	54	mV
	V_{CTRL} = 800mV, V_{ISN} = 5V	●	34.5	39.5	44.5	mV
	V_{CTRL} = 800mV, V_{ISN} = 0V	●	34	40	46	mV
	V_{CTRL} = 200mV, V_{ISN} = 5V	●	4.5	9.5	14.5	mV
	V_{CTRL} = 200mV, V_{ISN} = 0V	●	3.5	10	16.5	mV
RCBL Monitor Voltage	$V_{ISP} - V_{ISN}$ = 40mV, R_{CBL} = 13.7k	●	720	800	880	mV
	$V_{ISP} - V_{ISN}$ = 10mV, R_{CBL} = 13.7k	●	115	205	305	mV
RCBL Output Current Limit	$V_{ISP} - V_{ISN}$ = 50mV, V_{RCBL} = 0V		–2	–3	–4	mA
ISP, ISN Bias Current	V_{ISP} = V_{ISN} = 0V, 5V		–20		20	µA
ICTRL Current	V_{ICTRL} = 1.5V		–0.5	–2	–3	µA
$INTV_{CC}$ Voltage	V_{SYS} = 0V, 5V			3.4		V
$INTV_{CC}$ Undervoltage Lockout			2.6	2.9	3.15	V
SYS Voltage in SYS Regulation	V_{IN} = 12V	●	5.63	5.8	5.92	V
SYS Voltage to Disable Forced Continuous Mode				7.5		V
SYS Current in Regulation	V_{SYS} = 5V, R_T = 56.2k	●	3	4	5	mA
Dropout Voltage ($V_{IN} - V_{SYS}$)	V_{SYS} = 5V, I_{LOAD} = 2.1A			450		mV
Maximum Duty Cycle in Dropout			96	97.5	99	%
Minimum On-Time	I_{LOAD} = 1A	●	30	45	70	ns
Minimum Off-Time	I_{LOAD} = 0.5A			80	110	ns
Minimum V_{IN} for SYS Regulation at Full Frequency	R_T = 16.5k, V_{USB5V} = 0V, I_{LOAD} = 0.5A		6.2	7	7.9	V
Oscillator Frequency	R_T = 140k	●	250	300	340	kHz
	R_T = 56.2k	●	620	700	750	kHz
	R_T = 16.5k	●	1.85	2.00	2.05	MHz
Top Power NMOS On-Resistance	I_{SW} = 1A			120		mΩ
Top Power NMOS Current Limit	E-, I-Grades	●	3.2	4.8	6	A
	H-Grade	●	2.9	4.8	6	A
Bottom Power NMOS On-Resistance	V_{INTVCC} = 3.4V, I_{SW} = 1A			65		mΩ
Bottom Power NMOS Current Limit	V_{INTVCC} = 3.4V		3.5	4.5	5.8	A
SW Leakage Current	V_{IN} = 42V, V_{SW} = 0V, 42V			0.1	5	µA
EN/UV Threshold	$V_{EN/UV}$ Rising	●	0.94	1.0	1.06	V
EN/UV Hysteresis				40		mV
EN/UV Bias Current	$V_{EN/UV}$ = 2V		–20		20	nA
PG Upper Threshold Offset from V_{USB5V}	V_{USB5V} Falling	●	6	9	12	%
PG Lower Threshold Offset from V_{USB5V}	V_{USB5V} Rising	●	–6	–9	–12	%
PG Hysteresis				1.3		%
PG Pull-Down Resistance	V_{PG} = 0.1V	●		680	2000	Ω
PG Transition Delay	V_{USB5V} from 5V to 4V			40		µs
SYNC Threshold	V_{SYNC} Falling		0.8	1.1	1.4	V
	V_{SYNC} Rising		1.6	2.0	2.4	V
SYNC Pin Current	V_{SYNC} = 2V		–1		1	µA
TR/SS Current	$V_{TR/SS}$ = 0V		–1.2	–2.2	–3.2	µA
TR/SS Pull-Down Resistance	Fault Condition, $V_{TR/SS}$ = 0.1V			230		Ω

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

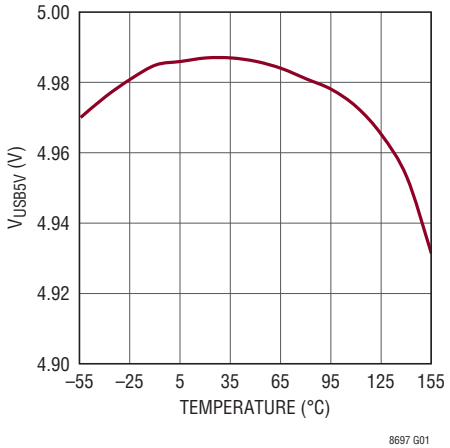
Note 2: The LT8697E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LT8697I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT8697H is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures above 125°C.

Note 3: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

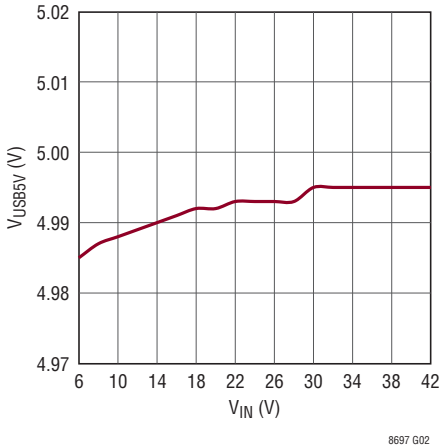
Note 4: Polarity specification for current into a pin is positive and out of a pin is negative. All voltages are referenced to GND unless otherwise specified. MAX and MIN refer to absolute values.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

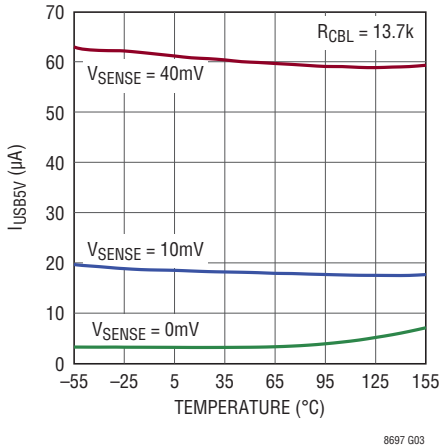
V_{USB5V} vs Temperature



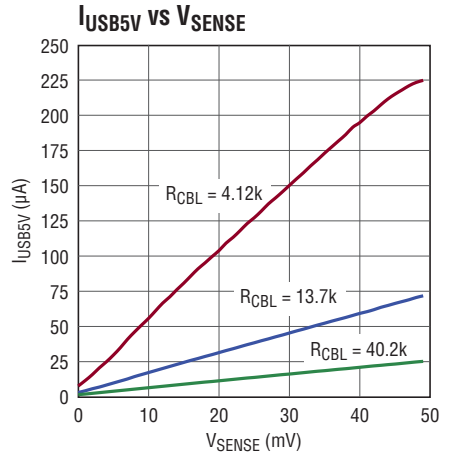
V_{USB5V} vs V_{IN}



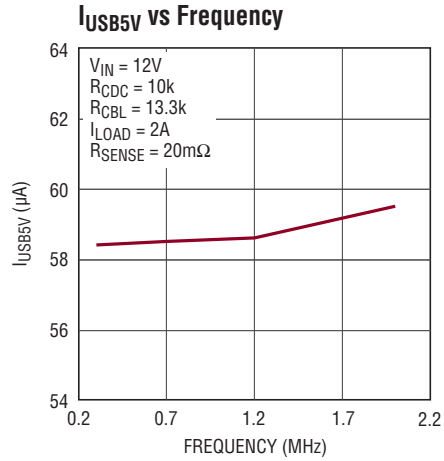
I_{USB5V} vs Temperature



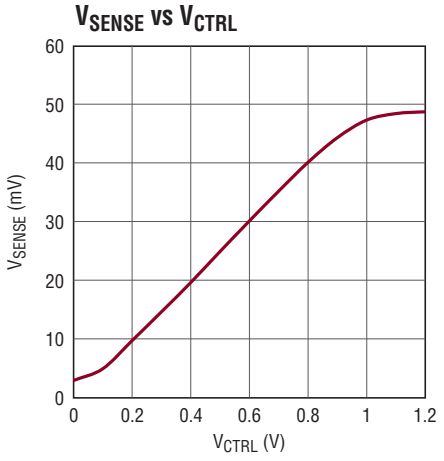
I_{USB5V} vs V_{SENSE}



I_{USB5V} vs Frequency

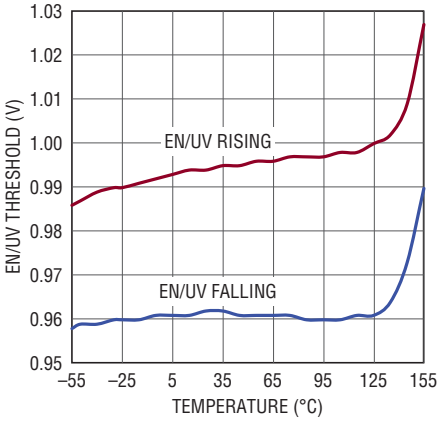


V_{SENSE} vs V_{CTRL}



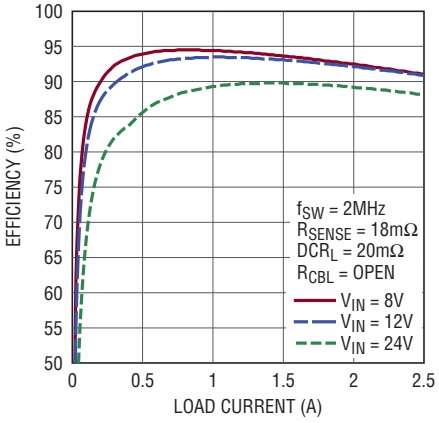
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

V_{EN} vs Temperature



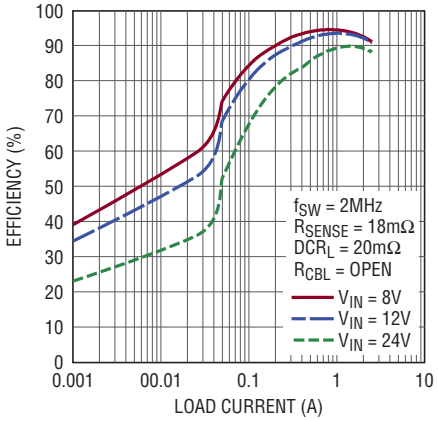
8697 G07

Efficiency vs I_{LOAD}



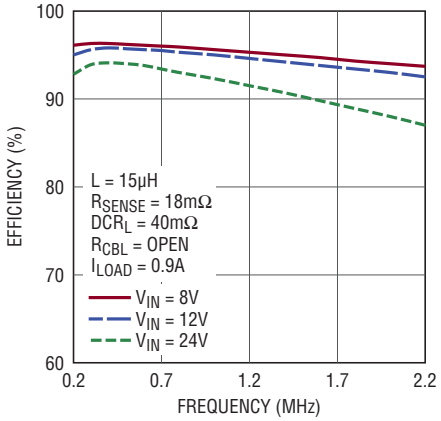
8697 G08

Efficiency vs I_{LOAD}



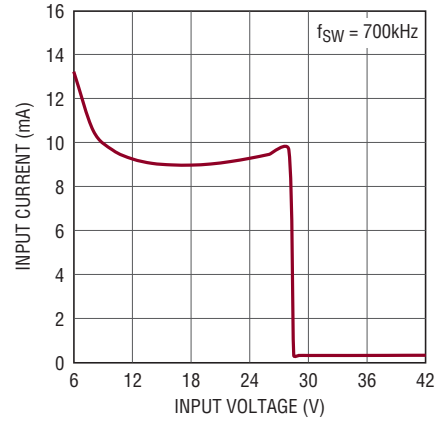
8697 G09

Efficiency vs Frequency



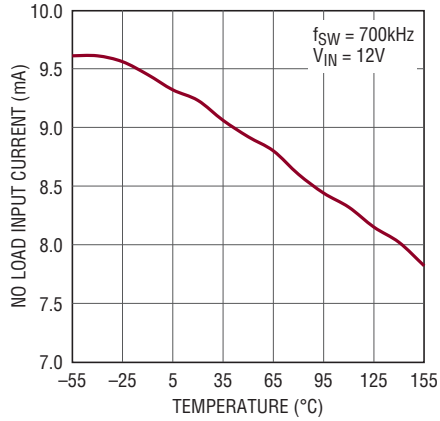
8697 G10

No Load Supply Current vs V_{IN}



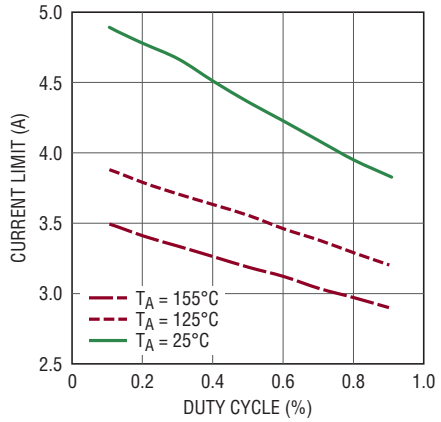
8697 G11

No Load Supply Current vs Temperature



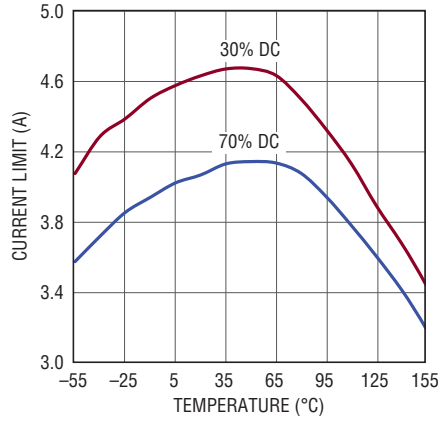
8697 G12

Top FET Current Limit vs Duty Cycle



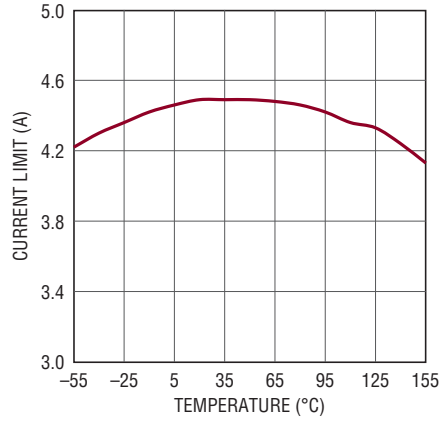
8697 G13

Top FET Current Limit vs Temperature



8697 G14

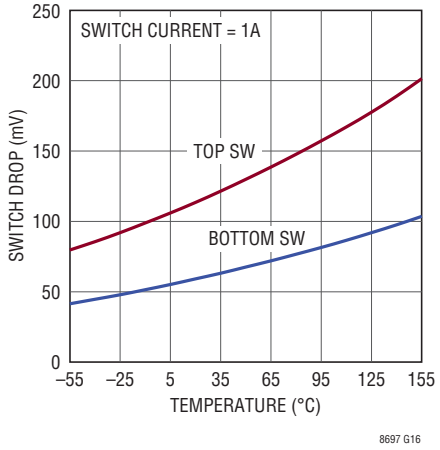
Bottom FET Current Limit vs Temperature



8697 G15

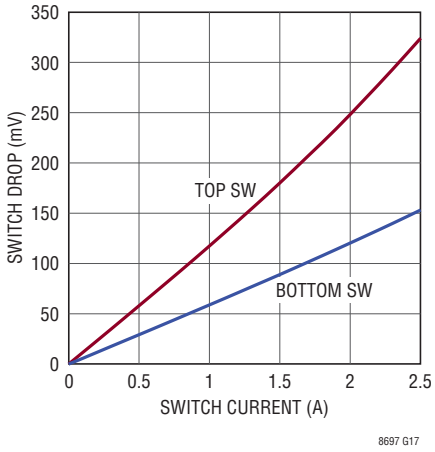
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Switch Drop vs Temperature



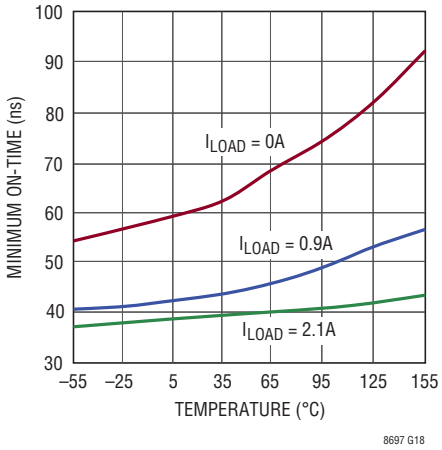
8697 G16

Switch Drop vs I_{SW}



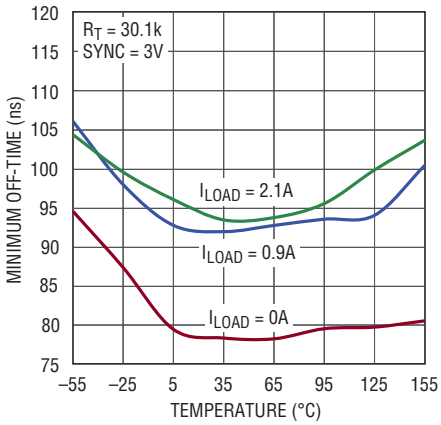
8697 G17

Minimum On-Time vs Temperature



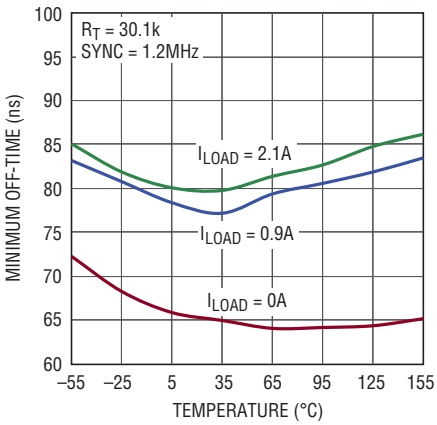
8697 G18

Minimum Off-Time vs Temperature



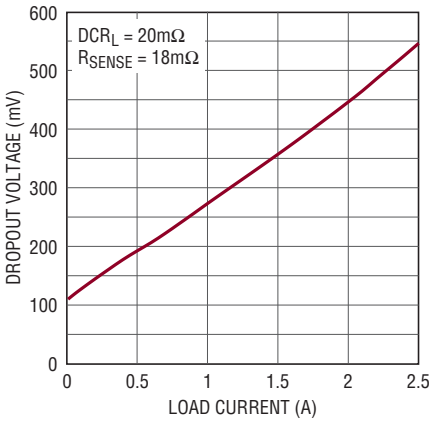
8697 G19

Minimum Off-Time vs Temperature



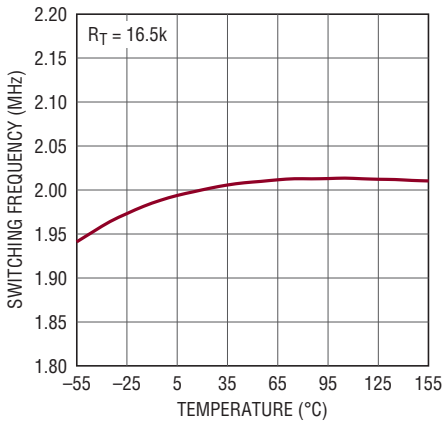
8697 G20

Dropout Voltage vs I_{LOAD}



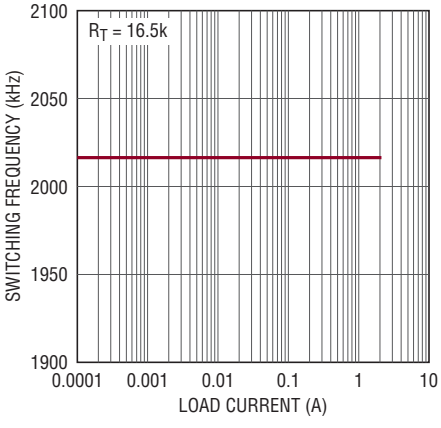
8697 G21

Switching Frequency vs Temperature



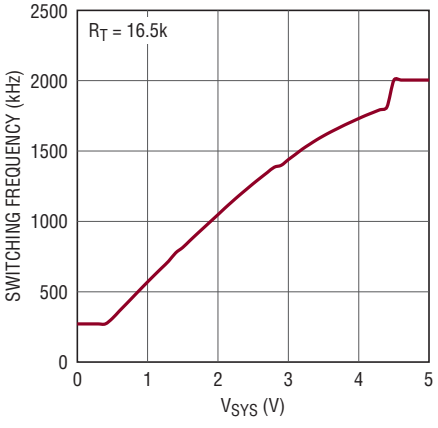
8697 G22

Switching Frequency vs I_{LOAD}



8697 G23

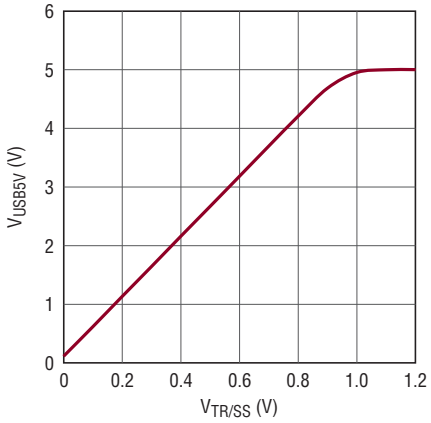
Switching Frequency vs V_{SYS}



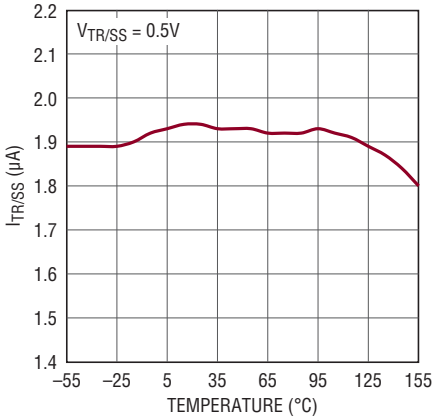
8697 G24

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

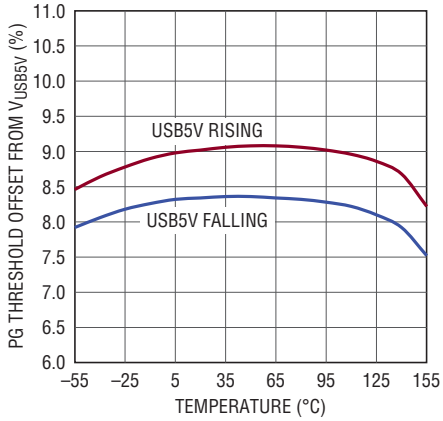
V_{USB5V} vs $V_{TR/SS}$



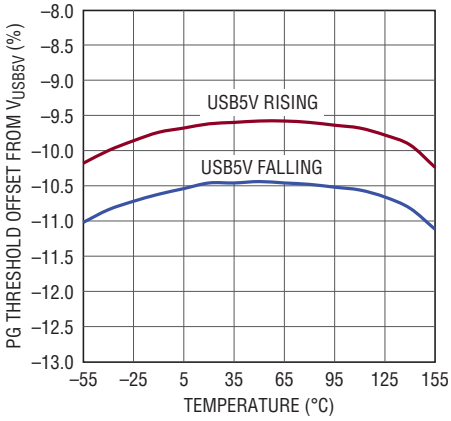
$I_{TR/SS}$ vs Temperature



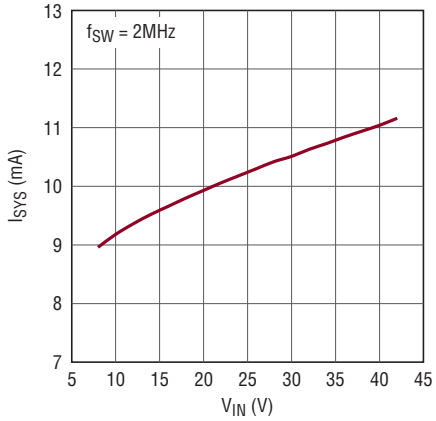
PG High Thresholds



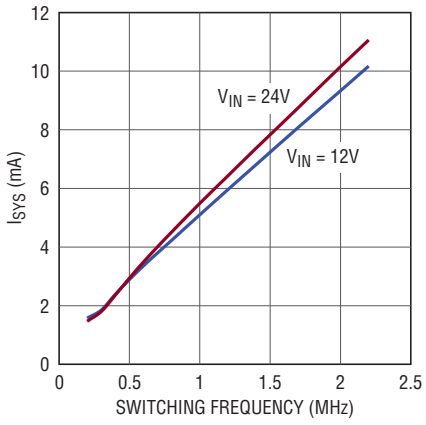
PG Low Thresholds



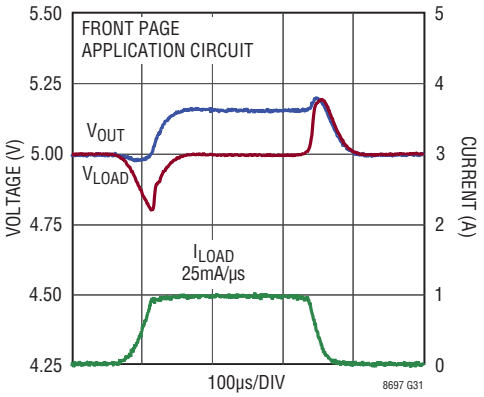
I_{SYS} vs V_{IN}



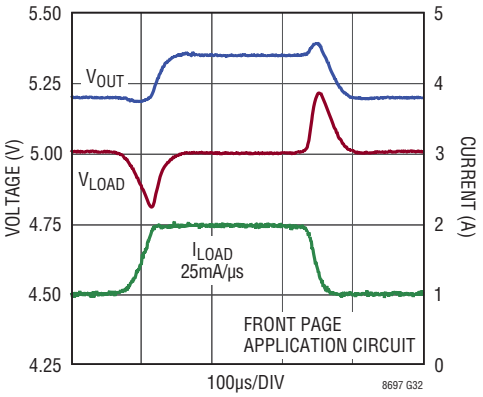
I_{SYS} vs Switching Frequency



Transient Response 0A to 1A Load Step

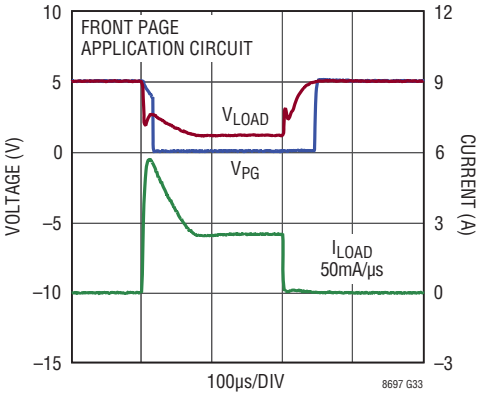


Transient Response 1A to 2A Load Step

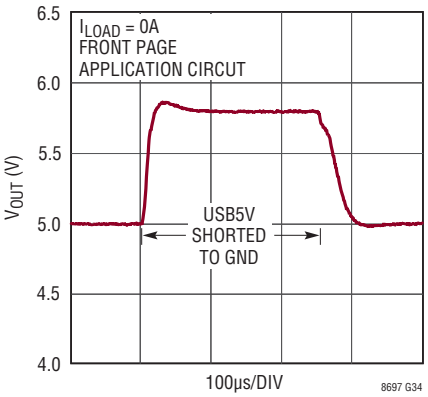


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

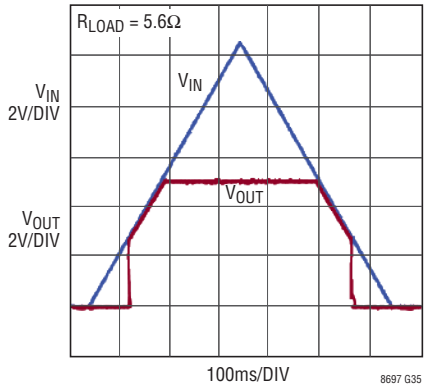
Transient Response Output Current Limit



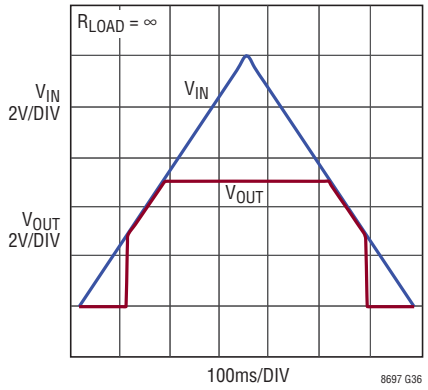
Transient Response USB5V Shorted to GND



Start-Up Dropout Performance



Start-Up Dropout Performance



PIN FUNCTIONS

SYNC (Pin 1): External Clock Synchronization Input. Tie to a clock source for synchronization to an external frequency and forced continuous mode. Tie to $INTV_{CC}$ if not used. Do not float.

TR/SS (Pin 2): Output Tracking and Soft-Start Pin. This pin allows user control of output voltage ramp rate during start-up. A TR/SS voltage below 0.97V forces the LT8697 to regulate V_{USB5V} to 5 times the TR/SS voltage. When TR/SS is above 0.97V, the tracking function is disabled and the internal reference resumes control of the error amplifier. An internal 2.2µA pull-up current from $INTV_{CC}$ on this pin allows a capacitor to program output voltage slew rate. This pin is pulled to ground when EN/UV is low, during thermal shutdown and when V_{IN} below its undervoltage lockout threshold; use a series resistor of at least 10k if driving from a low impedance output.

RT (Pin 3): Tie a resistor between RT and ground to set the switching frequency.

EN/UV (Pin 4): The LT8697 is shut down when this pin is low and active when this pin is high. The hysteretic threshold voltage is 1.00V going up and 0.96V when going down. Tie to V_{IN} if the shutdown feature is not used. An external resistor divider from V_{IN} can be used to program a V_{IN} threshold below which the LT8697 will shut down.

V_{IN} (Pins 5, 6): The V_{IN} pins supply current to the LT8697 internal circuitry and to the internal topside power switch. These pins must be tied together and be locally bypassed. Place the positive terminal of the input capacitor as close as possible to the V_{IN} pins, and the negative terminal as close as possible to the PGND pins.

PGND (Pins 7, 8): Power Switch Ground. These pins are the return path of the internal bottom side power switch and must be tied together. Place the negative terminal of the input capacitor as close as possible to the PGND pins.

NC (Pins 9-12): No Connect. These pins are floating and are not connected to the LT8697. Tie these pins to the same copper as the exposed pad. See Figure 8.

SW (Pins 13, 14, 15): The SW pins are the outputs of the internal power switches. Tie these pins together and connect them to the inductor and boost capacitor. This node should be kept small on the PCB for good performance. Do not drive these pins above V_{IN}.

BST (Pin 16): This pin is used to provide a drive voltage, higher than the input voltage, to the topside power switch. Place a 0.1µF boost capacitor between this pin and SW as close as possible to the LT8697 IC.

$INTV_{CC}$ (Pin 17): Internal 3.4V Regulator Bypass Pin. The internal power drivers and control circuits are powered from this voltage. The $INTV_{CC}$ maximum output current is 20mA. $INTV_{CC}$ current will be supplied from SYS if V_{SYS} > 3.1V, otherwise current will be drawn from V_{IN}. Decouple this pin to power ground with at least a 1µF low ESR ceramic capacitor. Do not load the $INTV_{CC}$ pin with external circuitry.

SYS (Pin 18): The internal regulator will draw current from SYS instead of V_{IN} when SYS is tied to a voltage higher than 3.3V. The SYS pin must be tied to the side of the inductor opposite the SW pin and must be bypassed by the output capacitor. SYS is also the secondary input to the error amp and regulates to a maximum of 5.8V.

PIN FUNCTIONS

PG (Pin 19): The PG pin is the open-drain output of an internal window comparator. PG remains low until the USB5V pin is within ±9% of the final regulation voltage and there are no fault conditions. The PG transition delay is approximately 40µs. PG is valid when V_{IN} is above 3.4V regardless of the EN/UV state.

USB5V (Pin 20): The LT8697 regulates the USB5V pin to 5V. For cable drop compensation, the USB5V pin input current is proportional to the sensed output current. The USB5V ESD cell clamps to 9V. To allow the LT8697 output to survive a short to 30V, the 10k R_{CDC} resistor must be in place between the USB5V pin and the output to limit the current into this pin.

ISP (Pin 21): Current Sense (+) Pin. This is the non-inverting input to the current sense amplifier.

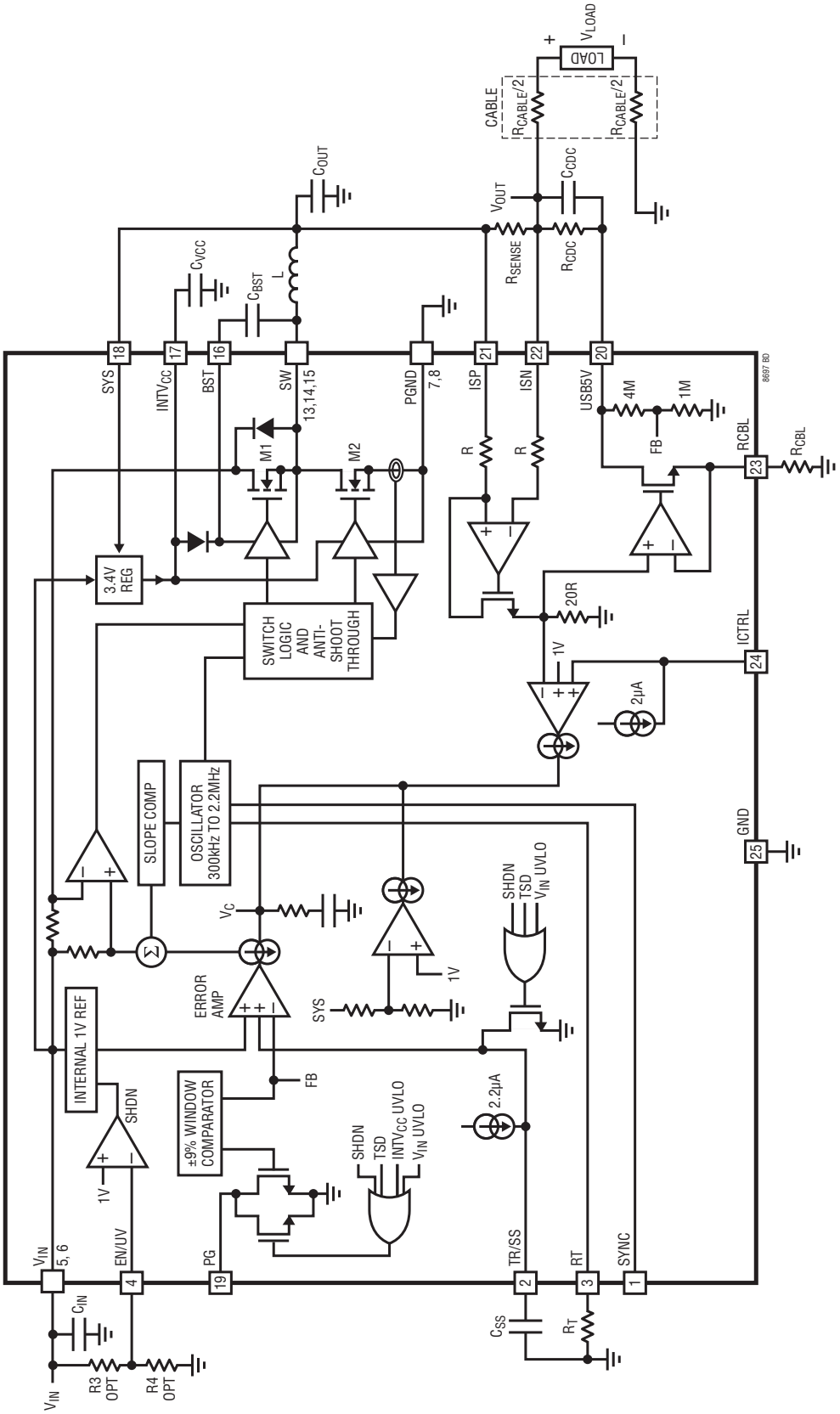
ISN (Pin 22): Current Sense (–) Pin. This is the inverting input to the current sense amplifier.

RCBL (Pin 23): Cable Drop Compensation Program Pin. A resistor R_{CBL} tied from RCBL to ground programs cable drop compensation by setting the USB5V input current. RCBL can source 1mA. Excessive capacitive loading on RCBL can degrade load transient response. Isolate load capacitance on this pin by tying a 100k resistor between RCBL and the capacitive load. The RCBL load monitor output is valid when the LT8697 is enabled, otherwise the output is zero. Float RCBL if neither the current monitor nor the cable drop compensation feature is desired.

ICTRL (PIN 24): Current Adjustment Pin. ICTRL adjusts the maximum $V_{ISP} – V_{ISN}$ drop before the LT8697 limits the output current. Connect directly to $INTV_{CC}$ or float for a full scale $V_{ISP} – V_{ISN}$ threshold of 48mV or apply values between ground and 1V to modulate the output current limit. There is an internal 2µA pull-up current on this pin. Float or tie to $INTV_{CC}$ when unused.

GND (Exposed Pad Pin 25): Ground. The exposed pad must be connected to the negative terminal of the input capacitor and soldered to the PCB for proper operation and in order to lower the thermal resistance.

BLOCK DIAGRAM



OPERATION

The LT8697 is a monolithic, constant frequency, current mode step-down DC/DC converter. An oscillator, with frequency set using a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch current comparator trips and turns off the switch. The peak inductor current is controlled by the voltage on the internal VC node. When the top power switch turns off, the synchronous power switch turns on until the next clock cycle begins or inductor current falls to zero. If overload conditions result in more than 4.2A flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

To control the output voltage, the LT8697's error amplifier servos the VC node by comparing the voltage on the USB5V pin, divided down about 5:1, with an internal 0.97V reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference. This differential error makes the error amplifier raise the VC voltage which raises the top switch peak current limit. The feedback process continues until the average inductor current matches the new load current and the output voltage is in regulation.

To implement cable drop compensation, the LT8697 drives the RCBL pin to $20(V_{ISP} – V_{ISN})$. Current sourced from the RCBL pin is derived from the USB5V pin, creating an output offset above the 5V USB5V pin voltage through R_{CDC} that is proportional to the load current and the R_{CDC}/R_{CBL} resistor ratio. The output voltage therefore increases with increasing load current. This negative output impedance compensates for resistive drops in wiring for remote loads.

The LT8697 error amp has two additional feedback paths that can override the USB5V pin control of the VC node. For output current limit, the voltage $V_{ISP} – V_{ISN}$ across the output current sense resistor is not allowed to exceed the lower of 48mV or $V_{ICTRL}/20$. Also, the SYS pin limits the output voltage to 5.8V. When regulation is determined by either the output current limit or the SYS pin, USB5V is not regulated to 5V and the output voltage falls below its programmed value.

If the EN/UV pin is low, the LT8697 is shut down and draws 1µA from the input. When the EN/UV pin is above 1V, the switching regulator will become active.

The LT8697 operates in forced continuous mode (FCM) for fast transient response and full frequency operation over a wide load range. If a clock is applied to the SYNC pin the part will synchronize to the external clock frequency and operate in FCM.

To improve efficiency across all loads, supply current to internal circuitry is sourced from the SYS pin when biased at 3.3V or above. Else, the internal circuitry will draw current from V_{IN}.

When in FCM the oscillator operates continuously and positive SW transitions are aligned to the clock. Negative inductor current is allowed. The LT8697 can sink current from the output and return this charge to the input in this mode, improving load step transient response. FCM is disabled if the V_{IN} pin is held above 29V or if the SYS pin is held above 7.5V. When FCM is disabled in these ways, negative inductor current is not allowed and the LT8697 skips SW cycles in light load conditions.

Comparators monitoring the USB5V pin voltage will pull the PG pin low if the output voltage varies more than ±9% (typical) from the set point, or if a fault condition is present.

The oscillator reduces the LT8697's operating frequency when the voltage at the SYS pin is below 4V. This frequency foldback helps to control the inductor current when the output voltage is lower than the programmed value during start-up or overcurrent conditions.

APPLICATIONS INFORMATION

Cable Drop Compensation

The LT8697 includes the necessary circuitry to implement cable drop compensation. Cable drop compensation allows the regulator to maintain 5V regulation on the USB V_{LOAD} despite high cable resistance. The LT8697 increases its local output voltage V_{OUT} above 5V as the load increases to keep V_{LOAD} regulated to 5V. This compensation does not require running an additional pair of Kelvin sense wires from the regulator to the load, but does require the system designer to know the cable resistance R_{CABLE} as the LT8697 does not sense this value.

Program the cable drop compensation using the following ratio:

$$R_{CBL} = 20.55 \bullet \frac{R_{SENSE} \bullet R_{CDC}}{R_{CABLE}}$$

where R_{CDC} is a resistor tied between the regulator output and the USB5V pin, R_{CBL} is a resistor tied between the RCBL pin and GND, R_{SENSE} is the sense resistor tied between the ISP and ISN pins in series between the regulator output and the load, and R_{CABLE} is the cable resistance. R_{SENSE} is typically chosen based on the desired current limit and is typically 20mΩ for 2.1A systems and 50mΩ for 0.9A. See the Setting the Current Limit section for more information.

The current flowing into the USB5V pin through R_{CDC} is identical to the current flowing out of the R_{CBL} resistor. While the ratio of these two resistors should be chosen per the equation above, choose the absolute values of these resistors to keep this current between 30µA and 200µA at full load current. This restriction results in R_{CBL} and R_{CDC} values between 5k and 33k. If I_{USB5V} is too low, capacitive loading on the USB5V and RCBL pins will degrade the load step transient performance of the regulator. If I_{USB5V} is too high, the RCBL pin will go into current limit and the cable drop compensation feature will not work.

Capacitance across the remote load to ground downstream of R_{SENSE} forms a zero in the LT8697's feedback loop due to cable drop compensation. C_{CDC} reduces the cable drop compensation gain at high frequency. The 1nF C_{CDC} capacitor tied across the 10k R_{CDC} is required for stability of the LT8697's output. If R_{CDC} is changed, C_{CDC} should also be changed to maintain roughly the same 10µs RC time constant. If the capacitance across the remote load is large compared to the LT8697 output capacitor tied to the SYS pin, a longer $R_{CDC} \bullet C_{CDC}$ time constant may be necessary for stability depending on the amount of cable drop compensation used. Output stability should always be verified in the end application circuit.

The LT8697 limits the maximum voltage of V_{OUT} by limiting the voltage on the SYS pin V_{SYS} to 5.8V. If the cable drop compensation is programmed to compensate for more than 0.8V of cable drop at the maximum I_{LOAD}, this V_{SYS} maximum will prevent V_{OUT} from rising higher and the voltage at the point of load will drop below 5V. The following equation shows how to derive the LT8697 output voltage V_{OUT}:

$$V_{OUT} = 5V + \frac{20.55 \bullet I_{LOAD} \bullet R_{SENSE} \bullet R_{CDC}}{R_{CBL}}$$

As stated earlier, the LT8697's cable drop compensation feature does not allow V_{OUT} to exceed the SYS regulation point of 5.8V. If additional impedance is placed in between the SYS pin and the OUT node such as R_{SENSE} or a USB Switch, the voltage drop through these impedances at the maximum I_{LOAD} must also be factored in to this maximum allowable V_{OUT} value. Refer to Figure 1 for load lines of V_{OUT} and V_{LOAD} to see how cable drop compensation works.

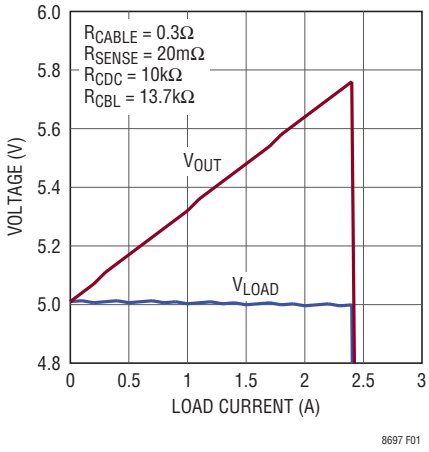


Figure 1. Cable Drop Compensation Load Line

APPLICATIONS INFORMATION

Cable Drop Compensation Over a Wide Temperature Range

Cable drop compensation with zero temperature variation may be used in many applications. However, matching the cable drop compensation temperature variation to the cable resistance temperature variation may result in better overall output voltage accuracy over a wide operating temperature range. For example, in an application with 0.26Ω of wire resistance and a maximum output current of 2.1A, cable drop compensation adds 0.55V at 25°C to the output at max load for a fully compensated wire resistance. If the wire in this example is copper, the copper resistance temperature coefficient of about 4000ppm/°C results in an output voltage error of –130mV at 85°C and 55mV at 0°C. Figure 2a shows this behavior.

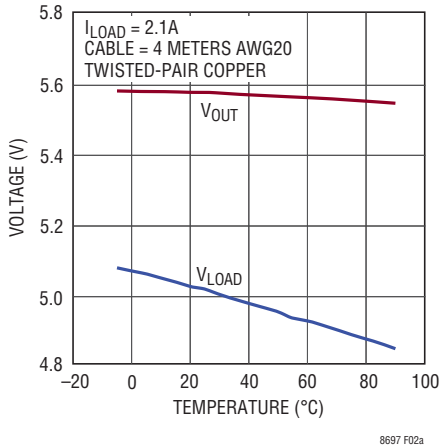


Figure 2a. Cable Drop Compensation Through 4m of AWG 20 Twisted-Pair Cable (260mΩ) without Temperature Compensation

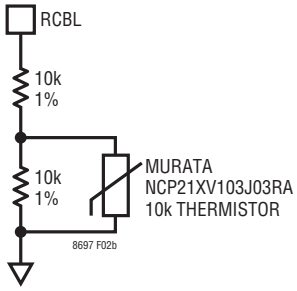


Figure 2b. R_{CBL} Resistor Network for Matching Copper Wire Temperature Coefficient

See Table 1 for a list of copper wire resistances vs gauge.

Table 1. Copper Wire Resistance vs Wire Gauge

AWG	RESISTANCE OF Cu WIRE AT 20°C (mΩ/m)
15	10.4
16	13.2
17	16.6
18	21.0
19	26.4
20	33.3
21	42.0
22	53.0
23	66.8
24	84.2
25	106
26	134
27	169
28	213
29	268
30	339
31	427
32	538
33	679
34	856
35	1080
36	1360
37	1720
38	2160
39	2730
40	3440

Cable drop compensation can be made to vary positively versus temperature with the addition of a negative temperature coefficient (NTC) resistor as a part of the RCBL resistance. This circuit idea assumes the NTC resistor is at the same temperature as the cable. Figure 2b shows an example resistor network for R_{CBL} that matches copper resistance variation over a wide –40°C to 125°C temperature range. Figure 2c shows the resultant cable drop compensation output at several temperatures using RCBL with negative temperature variation.

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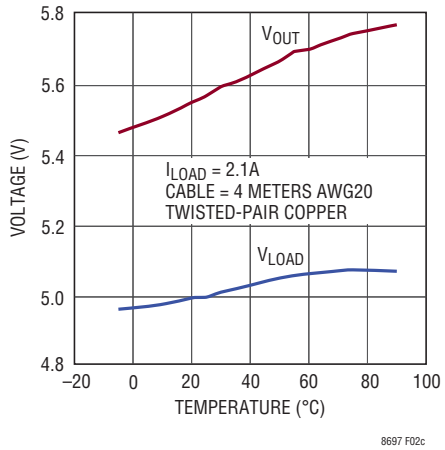

Figure 2c. Cable Drop Compensation Through 4m of AWG 20 Twisted-Pair Cable (260mΩ) with Temperature Compensation Using NTC R_{CBL}

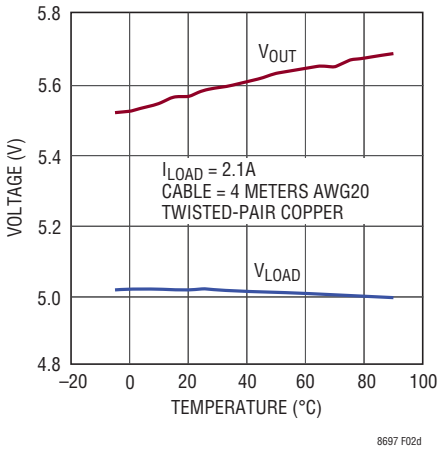

Figure 2d. Cable Drop Compensation Through 4m of AWG 20 Twisted-Pair Cable (260mΩ) with Temperature Compensation Using Copper R_{SENSE}

The NTC resistor does not give a perfectly linear transfer function versus temperature. Here, for typical component values, the worse case error is <10% of the cable compensation output, or <1% of the total output voltage accuracy. Better output voltage accuracy versus temperature can be achieved if R_{CBL} resistor values are optimized for a narrower temperature range. Contact LTC for help designing an R_{CBL} resistor network.

Choosing an R_{SENSE} resistor with a temperature coefficient that matches the cable resistance temperature coefficient can reduce this output voltage error overtemperature if the sense resistor is at roughly the same ambient temperature as R_{SENSE}. Small value copper wire inductors can be used in this way if the inductor resistance is well specified. Figure 2d shows the resultant cable drop compensation output at several temperatures using a copper R_{SENSE}.

Use of an R_{SENSE} that varies over temperature will make the LT8697 output current limit vary over temperature. To achieve the rated output current over the full operating temperature range, a higher room temperature output current limit may be necessary. Table 2 shows the manufacturer specified DCR of several copper wire inductors that may be used for R_{SENSE}.

Table 2. Copper Wire Inductors for Use as Sense Resistors

VENDOR	PART NUMBER	DC RESISTANCE (mΩ)
Coilcraft	NA5931-AL	15.7 ±5%
Coilcraft	NA5932-AL	21.8 ±5%
Coilcraft	NA5933-AL	32.4 ±5%
Coilcraft	NA5934-AL	34.3 ±5%
Coilcraft	NA5935-AL	44.1 ±5%
Coilcraft	NA5936-AL	47.2 ±5%

Effect of Cable Inductance on Load Step Transient Response

The inductance of long cabling limits the peak-to-peak transient performance of a 2-wire sense regulator to fast load steps. Since a 2-wire sense regulator like the LT8697 detects the output voltage at its local output and not at the point of load, the load step response degradation due to cable inductance is present even with cable resistance compensation. The local regulator output capacitor and the input capacitor of the remote load form a LC tank circuit through the inductive cabling between them. Fast load steps through long cabling show a large peak-to-peak transient response and ringing at the resonant frequency of the circuit. This ringing is a property of the LC tank circuit and does not indicate regulator instability.

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Figure 3 shows the LT8697 load step transient response to a 50mA/µs, 0.5A load step. Two cable impedances are compared: resistive only and then resistive plus inductive. First, a surface mount 0.2Ω resistor is tied between the LT8697 output and the load step generator. This resistor stands in for a purely resistive "cable". Second, actual AWG 20 twisted-pair cabling 3 meters long with 0.2Ω of total resistance and about 2.3µH of inductance is connected between the LT8697 output and the load step generator. Even though the resistance in these two circuits is the same, the transient load step response in the cable is worse due to the inductance.

The degree that cable inductance degrades LT8697 load transient response performance depends on the inductance of the cable and on the load step rate. Long cables have higher inductance than short cables. Cables with less separation between supply and return conductor pairs show lower inductance per unit length than those with separated conductors. Faster load step rate exacerbates the effect of inductance on load step response.

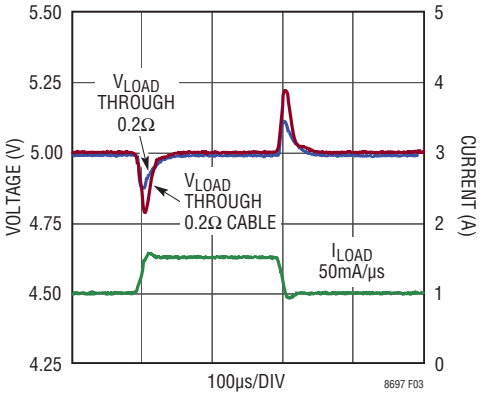

Figure 3. Effect of Cable Inductance on Load Step Transient Response

Since the local ground at the LT8697 is separated by a current carrying cable from the remote ground at the point of load, the ground reference points for these two locations are different.

Use a differential probe across the remote output at the end of the cable to measure output voltage at that point. Do not simultaneously tie an oscilloscope's probe ground leads to both the local LT8697 ground and the remote point of load ground. Doing so will result in high current flow in the probe ground lines and a strange and incorrect measurement. Figure 4 shows this behavior. A 1A/µs, 0.5A load step is applied to the LT8697 output through 3 meters of AWG 20 twisted-pair cable. On one curve, the resultant output voltage is measured correctly using a differential probe tied across the point of load. On the other curve, the oscilloscope ground lead is tied to the remote ground. This poor probing causes both a DC error due to the lower ground return resistance and an AC error showing increased overshoot and ringing. Do not add your oscilloscope, lab bench, and input power supply ground lines into your measurement of the LT8697 remote output.

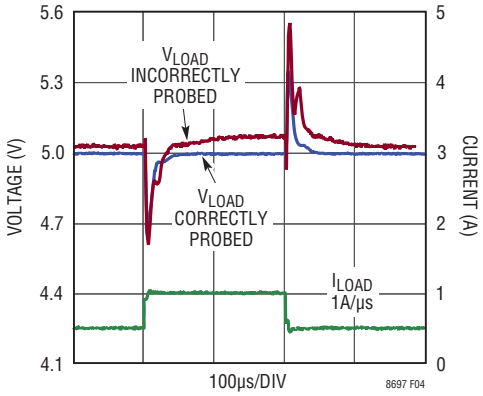

Figure 4. Effect of Probing Remote Output Incorrectly

Probing a Remote Output Correctly

Take care when probing the LT8697's remote output to obtain correct results. The whole point of cable drop compensation is that the local regulator output has a different voltage than the remote output at the end of a cable due to the cable resistance and high load current. The same is true for the ground return line which also has resistance and carries the same current as the output.

Reducing Output Overshoot

A consequence of the use of cable drop compensation is that the local output voltage at the LT8697 SYS pin is regulated to a voltage that is higher than the remote output voltage at the point of load. Several hundred mΩ of cable resistance can separate these two outputs, so at 2A of load current, the SYS pin voltage may be significantly higher than the nominal 5V output at the point of load.

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Ensure that any components tied to the LT8697 output can withstand this increased voltage.

The LT8697 has several features designed to mitigate any effects of higher output voltage due to cable drop compensation. First, the LT8697 error amplifier, in addition to regulating the voltage on the USB5V pin to 5V for the primary output, also regulates the SYS pin voltage to less than 5.8V. For $V_{SYS} < 5.8V$, the USB5V feedback input runs the LT8697 control loop, and for $V_{SYS} > 5.8V$, the SYS feedback input runs the LT8697 control loop. This 5.8V upper limit on the maximum SYS voltage protects components tied to the LT8697 output, such as a USB device or a USB Switch, from an overvoltage condition, but limits the possible amount of cable drop compensation to 0.8V.

Additionally, the LT8697 can sink current from the output and return the charge to the input when in forced continuous mode (FCM). This feature improves the step response for a load step from high to low. Cable drop compensation adds voltage to the output to compensate for voltage drop across the line resistance at high load. Since most DC/DC convertors can only source current, a load step from high to near zero current leaves the output voltage high and out of regulation.

The LT8697 fixes this problem by allowing the regulator to sink current from the output when USB5V is too high using FCM. Figure 5 shows the output voltage of the front page application circuit with and without FCM.

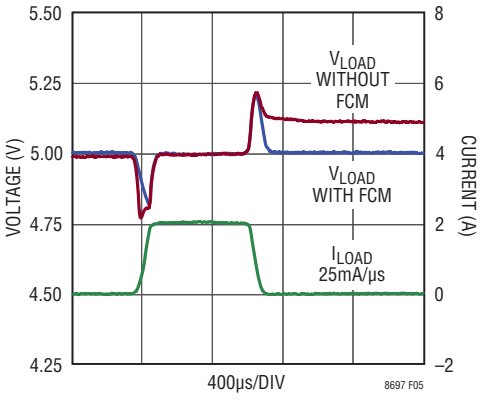

Figure 5. Load Step Response with and without Forced Continuous Mode

The load step response from high current to zero without the FCM is extremely slow and is limited by the SYS pin bias current. However, with FCM enabled, the output slews quickly back into regulation. If V_{IN} is above 29V or V_{SYS} is above 7.5V, FCM is disabled.

Interfacing with a USB Switch

A USB or similar electronic switch can be tied between the LT8697 output and the point of load. The switch on resistance can be included in the cable drop compensation calculation. Alternately, to improve load regulation, tie the USB5V feedback input through R_{CDC} to the output of the USB Switch so the USB Switch impedance is removed from the DC load response. Tie the output to the USB Switch input. The SYS pin regulates to a maximum of 5.8V, so the USB Switch should be chosen accordingly.

The LT8697 has output current limit. Many USB Switches implement current limit as well. For well controlled and predicable behavior, ensure that only one chip sets the output current limit, and the other chip has current limit that exceeds the desired current limit over all operating conditions.

The LT8697 has many of the features of USB Switches: programmable output current limit, filtered fault reporting and on/off functionality. In addition, unlike many USB Switches, the LT8697 output can survive shorts to 30V, enhancing system robustness. Therefore, in many cases a USB Switch is not necessary and the LT8697 can provide both the functionality of a voltage regulator and a USB Switch.

Using SYS as a Secondary Output

For some applications, the SYS pin can be used as a secondary voltage output in addition to the primary voltage output regulated by the USB5V pin. The SYS pin voltage varies between 5V and 5.8V depending on the load current if cable drop compensation is used on the primary output. A 3.3V low dropout regulator can be tied to SYS to provide a secondary regulated output such as to power a USB µcontroller. The SYS output will not have cable drop compensation, but will rise above 5V depending on the USB output load current. The load on the SYS pin should

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be designed to limit load current. Also, an electronic switch may be necessary to prevent an output overcurrent condition on the USB5V output from bringing down the SYS output. See the Inductor Selection and Maximum Output Current discussion below to determine how much total load current can be drawn from the outputs for a given LT8697 application.

Setting the Current Limit

In addition to regulating the output voltage, the LT8697 includes a current regulation loop for setting the average output current limit. The LT8697 measures the voltage drop across an external current sense resistor R_{SENSE} using the ISP and ISN pins. This resistor should be connected in series with the load current after the output capacitor. The current loop modulates the cycle-by-cycle top switch switch current limit such that the average voltage across the ISP–ISN pins does not exceed its regulation point.

The LT8697 current limit can be programmed by forcing a voltage on the ICTRL pin between 0V and 1V. Program the current limit using the following equation:

$$I_{LIM} = \frac{V_{CTRL}}{R_{SENSE} \bullet 20.3}$$

The preceding I_{LIM} equation is valid for $V_{ISP} - V_{ISN} <$ 48mV. At 48mV V_{SENSE}, the internal current limit loop takes over output current regulation from the ICTRL pin. The maximum programmable output current ($I_{LIM(MAX)}$) is therefore found by the following equation:

$$I_{LIM(MAX)} = \frac{48mV}{R_{SENSE}}$$

The internal 2µA pull-up on the ICTRL pin allows this pin to be floated if unused, in which case the $I_{LIM(MAX)}$ would be the output current limit.

When in forced continuous mode, the LT8697's ability to regulate the output current is limited by its $t_{ON(MIN)}$. In this scenario, at very low output voltage the output current can exceed the programmed output current limit and is limited by the bottom switch current limit of 4.5A plus 1/2 the ripple current. To help mitigate this effect, at low output voltage the LT8697 folds back the switching frequency by 10:1 to allow regulation at very low duty cycle. Also, above V_{IN} = 29V the LT8697 disables forced continuous mode so the part can pulse skip to maintain regulation at any low V_{OUT} to V_{IN} ratio. For V_{IN} < 29V, use the following equation to find the minimum output voltage ($V_{OUT(MIN)}$) where the LT8697 can regulate the output current limit:

$$V_{OUT(MIN)} = 0.1 \bullet f_{SW} \bullet t_{ON(MIN)} \bullet (V_{IN} - V_{SW(TOP)} + V_{SW(BOT)}) - V_{SW(BOT)} - V_{SENSE} - V_L$$

where f_{SW} is the switching frequency, $t_{ON(MIN)}$ is the minimum on-time, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.3V and ~0.15V) respectively at maximum load), V_{SENSE} is voltage across the R_{SENSE} at the programmed output current and V_L is the resistive drop across the inductor ESR at the programmed output current. If the calculated $V_{OUT(MIN)}$ is negative or is less than the IR drop across the resistive short on the output at the programmed current limit, then the LT8697 can regulate the output current limit.

In practical applications, the resistances of the cable, inductor and sense resistor are more than adequate to allow the LT8697 to regulate to the output current limit for any switching frequency and input voltage. For a 400kHz application in a worst-case condition, the programmed output current can be regulated into V_{OUT} = 0V for any input voltage up to 42V. For a 2MHz application in a worst-case condition, the programmed output current can be regulated into V_{OUT} = 0.3V or higher. Refer to Figure 6 to see how the front page application circuit responds to a short directly on the regulator output without a cable.

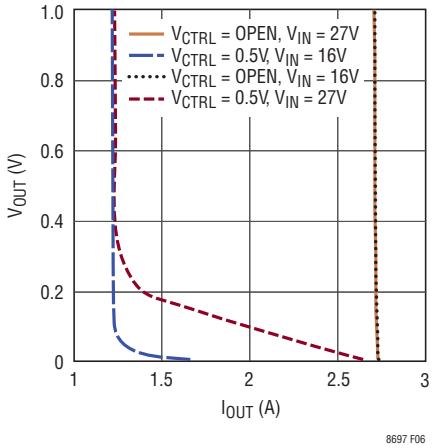

Figure 6. Output Current Regulation vs V_{OUT} at f_{SW} = 2MHz, R_{SENSE} = 18mΩ

APPLICATIONS INFORMATION

Using RCBL as an Output Current Monitor

The primary function of the RCBL pin is to set the cable drop compensation as discussed in the cable drop compensation section earlier. However, the RCBL pin produces an output voltage that is proportional to the output load current. The RCBL pin can therefore be used as an output load monitor. The voltage on the RCBL pin obeys the following relation to USB load current:

$$V_{CBL} = I_{LOAD} \bullet R_{SENSE} \bullet 20.55$$

V_{CBL} is valid when the LT8697 is switching.

Since the RCBL pin current is part of the cable drop compensation control loop, excessive capacitive loading on the RCBL pin can cause USB output voltage overshoot during load steps. Keep the capacitive loading on the RCBL pin below 100pF or isolate the load capacitance with 100kΩ in series between the RCBL pin and the input it is driving, as shown in Figure 7.

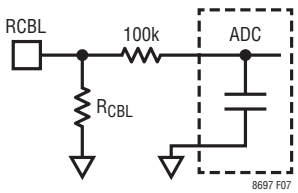

Figure 7. Using the RCBL Pin as Output Current Monitor

Setting the Switching Frequency

The LT8697 uses a constant frequency PWM architecture that can be programmed to switch from 300kHz to 2.2MHz by using a resistor tied from the RT pin to ground. A table showing the necessary R_T value for a desired switching frequency is in Table 3. The R_T resistor required for a desired switching frequency can be calculated using the following equation:

$$R_T = \frac{43}{f_{SW}} - 5.2$$

where R_T is in kΩ and f_{SW} is the desired switching frequency in MHz.

Table 3. SW Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.3	140
0.4	102
0.5	80.6
0.6	66.5
0.7	56.2
0.8	47.5
1.0	37.4
1.2	30.1
1.4	25.5
1.6	21.5
1.8	18.7
2.0	16.5
2.2	14.7

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency and a reduced input voltage range with constant frequency operation.

The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{5V + V_{SW(BOT)}}{t_{ON(MIN)} \bullet \left(V_{IN} - V_{SW(TOP)} + V_{SW(BOT)}\right)}$$

where V_{IN} is the typical input voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.3V and ~0.15V respectively, at maximum load) and $t_{ON(MIN)}$ is the minimum top switch on-time (see the Electrical Characteristics section). This equation shows that a slower switching frequency is necessary to accommodate a high V_{IN}/V_{OUT} ratio.

For transient operation, V_{IN} may go as high as the absolute maximum rating of 42V regardless of the R_T value. However, the LT8697 will reduce switching frequency as necessary to maintain control of inductor current to assure safe operation.

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The LT8697 can operate at very high duty cycle, thus maintaining the output voltage in regulation with the input voltage only several hundred mV higher. This dropout voltage depends on load current and the $R_{DS(ON)}$ of the top switch. However, the LT8697 skips off-times in very high duty cycle conditions, reducing the switching frequency below that programmed by R_T. In this dropout mode, the maximum allowable on-time is about 18µs. If this 18µs on-time threshold is reached, the LT8697 enforces a 400ns off-time to keep the BST capacitor charged at light loads. This behavior limits the maximum duty cycle to 97.5%, but guarantees good dropout performance across all loads and any start-up condition.

For applications that cannot allow deviation from the programmed switching frequency at low V_{IN}/V_{OUT} ratios, use the following formula to set switching frequency:

$$f_{SW(MAX)} = \frac{1}{t_{OFF(MIN)}}\left(\frac{V_{IN(MIN)} - 5.8 - V_{SW(TOP)}}{V_{IN(MIN)} + V_{SW(BOT)} - V_{SW(TOP)}}\right)$$

where $V_{IN(MIN)}$ is the minimum input voltage without skipped cycles, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.3V, ~0.15V, respectively at maximum load), f_{SW} is the switching frequency (set by R_T), and $t_{OFF(MIN)}$ is the minimum switch off-time. Note that higher switching frequency will increase the minimum input voltage below which cycles will be dropped to achieve higher duty cycle.

Inductor Selection and Maximum Output Current

The LT8697 is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. During overload or short-circuit conditions the LT8697 safely tolerates operation with a saturated inductor through the use of a high speed peak-current mode architecture.

A good first choice for the inductor value is as follows:

$$L = \frac{5.8V + V_{SW(BOT)}}{f_{SW}}$$

where f_{SW} is the switching frequency in MHz, $V_{SW(BOT)}$ is the bottom switch drop (~0.15V) and L is the inductor value in µH.

To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus 1/2 of the inductor ripple current:

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

where ΔI_L is the inductor ripple current as calculated below and $I_{OUT(MAX)}$ is the maximum output load for a given application.

As a quick example, an application requiring 1A output should use an inductor with an RMS rating of greater than 1A and an I_{SAT} of greater than 1.3A. During long duration overload or short-circuit conditions, the inductor RMS current rating requirement is greater to avoid overheating of the inductor. To keep the efficiency high, the series resistance (DCR) should be less than 0.04Ω, and the core material should be intended for high frequency applications.

The LT8697 limits the peak switch current in order to protect the switches and the system from overload faults. The top switch current limit (I_{LIM}) is 4.8A at low duty cycles and decreases linearly to 4A at DC = 0.8. The inductor value must then be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the switch current limit (I_{LIM}) and the ripple current.

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2}$$

The peak-to-peak ripple current in the inductor can be calculated as follows:

$$\Delta I_L = \frac{5V}{L \bullet f_{SW}} \bullet \left(1 - \frac{5V}{V_{IN(MAX)}}\right)$$

where f_{SW} is the switching frequency of the LT8697 and L is the value of the inductor. Therefore, the maximum output current that the LT8697 will deliver depends on the switch current limit, the inductor value, and the input and output voltages. The inductor value may have to be increased if the inductor ripple current does not allow sufficient maximum output current ($I_{OUT(MAX)}$) given the

APPLICATIONS INFORMATION

switching frequency and maximum input voltage used in the desired application. Note that the LT8697 peak switch current decreases in the 125°C to 150°C H-grade junction temperature range. The maximum output current that the LT8697 can deliver at 150°C junction temperature and maximum duty cycle may be less than 2.5A depending on the inductor value.

The optimum inductor for a given application may differ from the one indicated by this design guide. A larger value inductor provides a higher maximum load current and reduces the output voltage ripple. For applications requiring smaller load currents, the value of the inductor may be lower and the LT8697 may operate with higher ripple current. This allows use of a physically smaller inductor, or one with a lower DCR resulting in higher efficiency.

For more information about maximum output current and discontinuous operation, see Linear Technology's Application Note 44.

Finally, for duty cycles greater than 50% (V_{OUT}/V_{IN} > 0.5), a minimum inductance L_{MIN} is required to avoid sub-harmonic oscillation:

$$L_{MIN} = \frac{5.8V + V_{SW(BOT)}}{f_{SW}} \bullet 0.8$$

For robust operation over a wide V_{IN} and V_{OUT} range, use at least an inductor value as specified above.

Input Capacitor

Bypass the input of the LT8697 circuit with a ceramic capacitor of X7R or X5R type placed as close as possible to the V_{IN} and PGND pins. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 4.7µF to 10µF ceramic capacitor is adequate to bypass the LT8697 and will easily handle the ripple current. Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT8697 and to force this very high frequency switching current into a tight local loop, minimizing EMI. A 4.7µF capacitor is capable of this task, but only if it is placed close to the LT8697 (see the PCB Layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT8697. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT8697 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8697's voltage rating. This situation is easily avoided (see Linear Technology Application Note 88).

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT8697 to produce the DC output. In this role it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT8697's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. For good starting values, see the Typical Applications section.

Use X5R or X7R types. This choice will provide low output ripple and good transient response. Increasing the output capacitance will also decrease the output voltage ripple. A lower value of output capacitor can be used to save space and cost but this may cause loop instability if the output capacitor is too small. Since cable drop compensation slews the voltage across the output capacitor in response to transient load steps, a smaller output capacitor can give faster response time. See the Typical Applications in this data sheet for suggested capacitor values.

When choosing a capacitor, special attention should be given to the data sheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

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Enable Pin

The LT8697 is in shutdown when the EN/UV pin is low and active when the pin is high. The rising threshold of the EN comparator is 1.0V, with 40mV of hysteresis. The EN/UV pin can be tied to V_{IN} if the shutdown feature is not used, or tied to a logic level if shutdown control is required.

Adding a resistor divider from V_{IN} to EN/UV programs the LT8697 to regulate the output only when V_{IN} is above a desired voltage (see the Block Diagram). Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. This threshold can be adjusted by setting the values R3 and R4 such that they satisfy the following equation:

$$V_{IN(EN)} = \left(\frac{R3}{R4} + 1\right) \bullet 1.0V$$

where the LT8697 will remain off until V_{IN} is above $V_{IN(EN)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $V_{IN(EN)}$.

$INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces the 3.4V supply from V_{IN} that powers the drivers and the internal bias circuitry. The $INTV_{CC}$ can supply enough current for the LT8697's circuitry and must be bypassed to ground with a minimum capacitance of 1µF. Use an X5R or an X7R ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. To improve efficiency the internal LDO can also draw current from the SYS pin when the SYS pin is at 3.3V or higher. SYS must be tied to the LT8697 output capacitor. If the SYS pin is below 3.3V, the internal LDO will consume current from V_{IN}. Do not load $INTV_{CC}$ with more than 100µA.

Output Voltage Tracking and Soft-Start

The LT8697 allows the user to program its output voltage ramp rate by means of the TR/SS pin. An internal 2.2µA source pulls up the TR/SS pin to $INTV_{CC}$. Putting an external capacitor on TR/SS enables soft starting the output to prevent a current surge on the input supply. During the soft-start ramp the output voltage will proportionally track the TR/SS pin voltage. For output tracking applications, TR/SS can be externally driven by another voltage source. From 0V to 0.97V, the TR/SS voltage will override the internal 0.97V reference input to the error amplifier, thus regulating the USB5V pin voltage to 5× that of TR/SS pin. When TR/SS is above 0.97V, tracking is disabled and USB5V will regulate to 5V. The TR/SS pin may be left floating if the function is not needed.

An active pull-down circuit is connected to the TR/SS pin which will discharge the external soft-start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the EN/UV pin transitioning low, V_{IN} voltage falling too low or thermal shutdown.

Output Power Good

When the LT8697's output voltage is within the ±9% window of the regulation point, which is V_{USB5V} in the range of 4.55V to 5.45V (typical), the output voltage is considered good and the open-drain PG pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal pull-down device will pull the PG pin low. To prevent glitching, both the upper and lower thresholds include 1.3% of hysteresis.

The PG pin is also actively pulled low during several fault conditions: EN/UV pin is below 1V, $INTV_{CC}$ has fallen too low, V_{IN} is too low, or thermal shutdown.

Synchronization

To synchronize the LT8697 oscillator to an external frequency, connect a square wave (with 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 2.4V (up to 6V).

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The LT8697 may be synchronized over a 300kHz to 2.2MHz range. The R_T resistor should be chosen to set the LT8697 switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the R_T should be selected for 500kHz. The slope compensation is set by the RT value, while the minimum slope compensation required to avoid subharmonic oscillations is established by the inductor size, input voltage, and output voltage. Since the synchronization frequency will not change the slopes of the inductor current waveform, if the inductor is large enough to avoid subharmonic oscillations at the frequency set by RT, then the slope compensation will be sufficient for all synchronization frequencies.

Output Short Protection

The LT8697 will tolerate a shorted output. Several features are used for protection during output short-circuit and brownout conditions. The first is the switching frequency will be folded back while the output is lower than the set point to maintain inductor current control. Second, the bottom switch current is monitored such that if inductor current is beyond safe levels, switching of the top switch will be delayed until the inductor current falls to safe levels.

The LT8697 withstands a short between its output and 12V or 24V automotive battery voltage. The USB5V pin draws current when held above 9V. A minimum 10k R_{CDC} resistor must be tied from USB5V to V_{OUT} for robust operation with V_{OUT} above its regulation point. The remaining pins SW, ISP, ISN, PG and SYS tied at or near the output voltage have at least a 30V maximum rating. The output capacitor C_{OUT} absorbs ESD events on the LT8697 output.

If V_{IN} is held low or floated while V_{OUT} is held high, the body diode of the LT8697 internal top power switch will conduct high current from the SW pin to the V_{IN} pin, regardless of the state of the EN/UV pin, causing damage to the LT8697. V_{OUT} must remain equal to or lower than V_{IN} to avoid this damage to the LT8697.

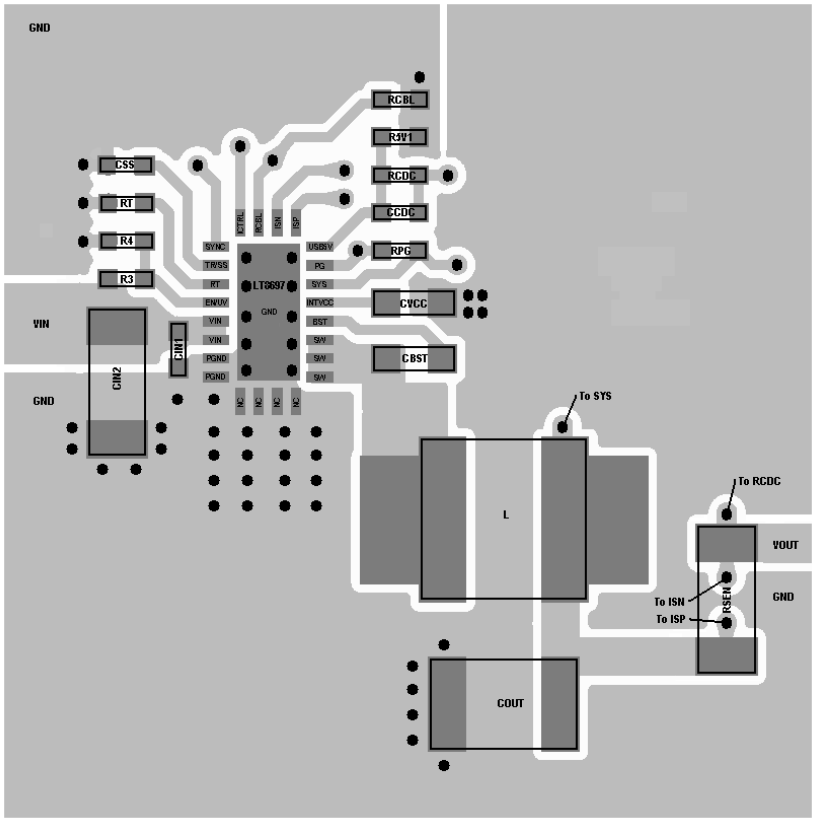


Figure 8. Recommended PCB Layout for the LT8697

APPLICATIONS INFORMATION

PCB Layout

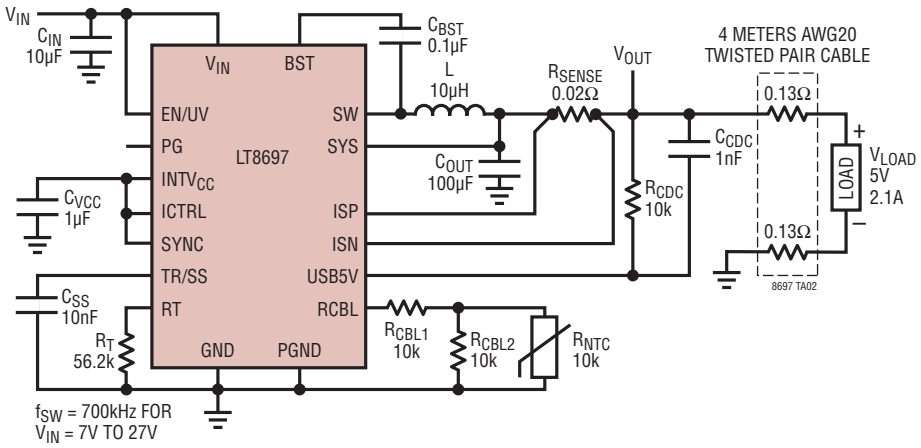
For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 8 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT8697's V_{IN} pins, PGND pins, and the input capacitors (C_{IN1} and C_{IN2}). The loop formed by the input capacitor should be as small as possible by placing the capacitor adjacent to the V_{IN} and PGND pins. When using a physically large input capacitor the resulting loop may become too large in which case using a small case/value capacitor placed close to the V_{IN} and PGND pins plus a larger capacitor further away is preferred. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local ground plane under the application circuit on the layer closest to the surface layer. The SW and BST nodes should be as small as possible. Finally, keep the USB5V and RT nodes small so that the ground traces will shield them from the SW and BST nodes. The exposed pad on the bottom of the package must be soldered to ground so that the pad is connected to ground electrically and also acts as a heat sink thermally. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT8697 to additional ground planes within the circuit board and on the bottom side.

High Temperature Considerations

For applications with higher ambient temperatures, lay out the PCB to ensure good heat sinking of the LT8697. The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT8697. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LT8697 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The die temperature is calculated by multiplying the LT8697 power dissipation by the thermal resistance from junction to ambient. The LT8697 will stop switching and indicate a fault condition if safe junction temperature is exceeded.

TYPICAL APPLICATIONS

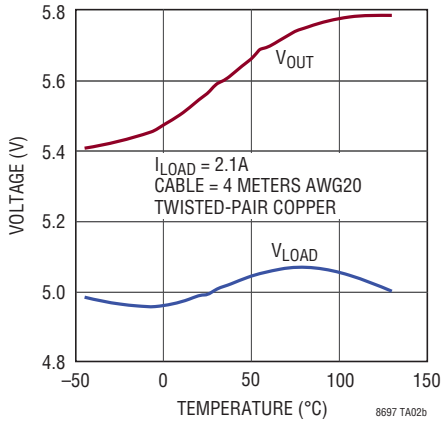
5V Step-Down Converter with Cable Drop Compensation for Copper Cabling Over Wide Temperature Range



CIN : X7R OR X5R
COUT: 1210 CASE SIZE, X7R OR X5R
CVCC: X7R OR X5R
CBST: X7R OR X5R

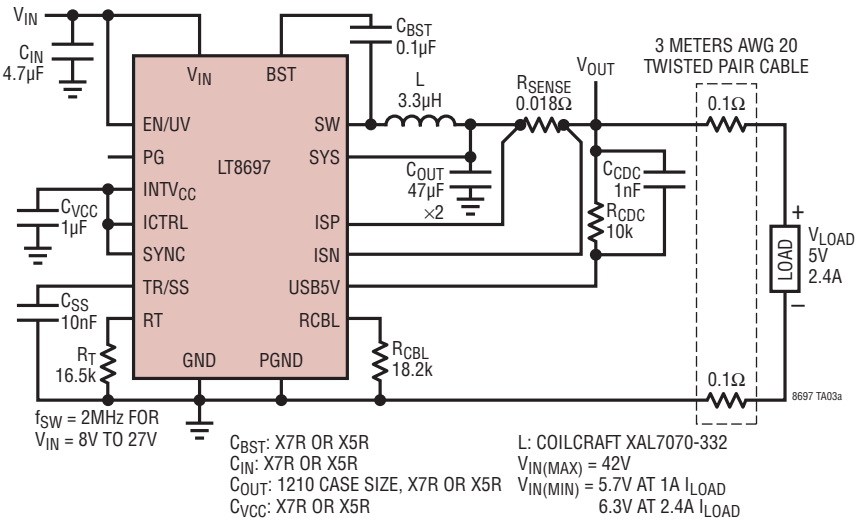
L: WÜRTH 74437368100
RNTC: MURATA NCP21XV103J03RA
VIN(MAX) = 42V
VIN(MIN) = 5.8V AT 1A ILOAD
6.6V AT 2.1A ILOAD

Temperature Correction for Cable Drop Compensation Through Copper Cabling

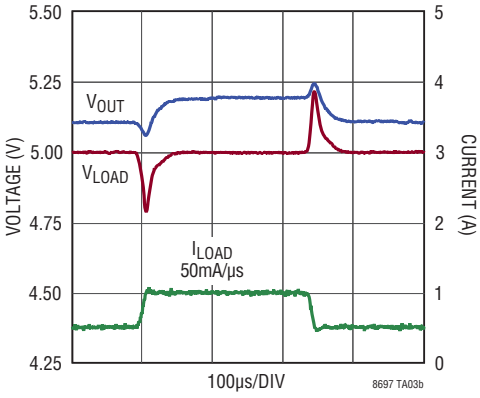


TYPICAL APPLICATIONS

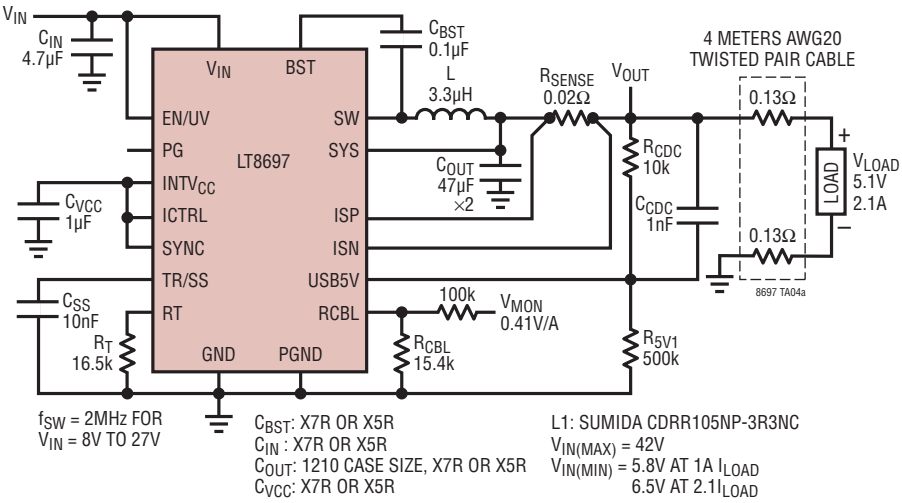
2MHz 5V Step-Down Converter with Cable Drop Compensation



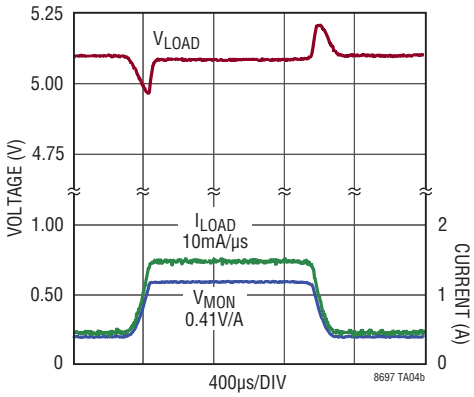
Transient Response Through 3 Meters AWG 20 Twisted-Pair Cable



2MHz 5.1V Step-Down Converter with Cable Drop Compensation and Output Current Monitor

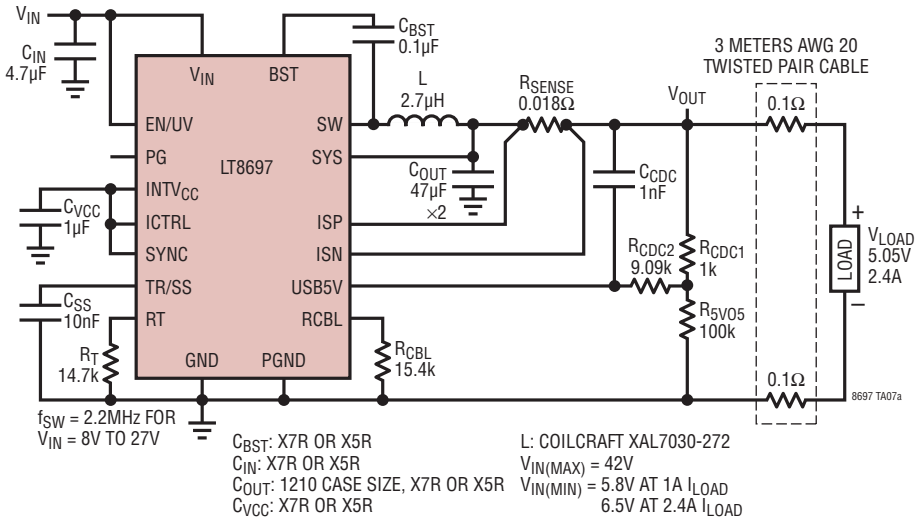


Transient Response 0.5A to 1.5A Load Step

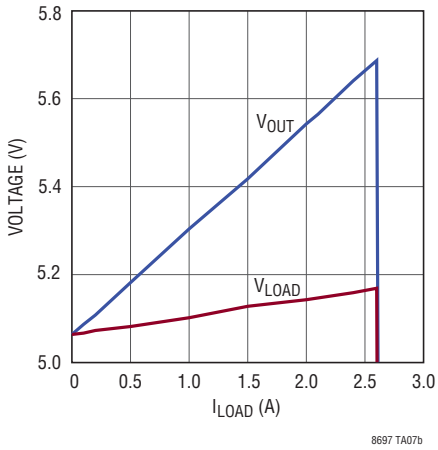


TYPICAL APPLICATIONS

2.2MHz, 5.05V Step-Down Converter with Negative Output Resistance



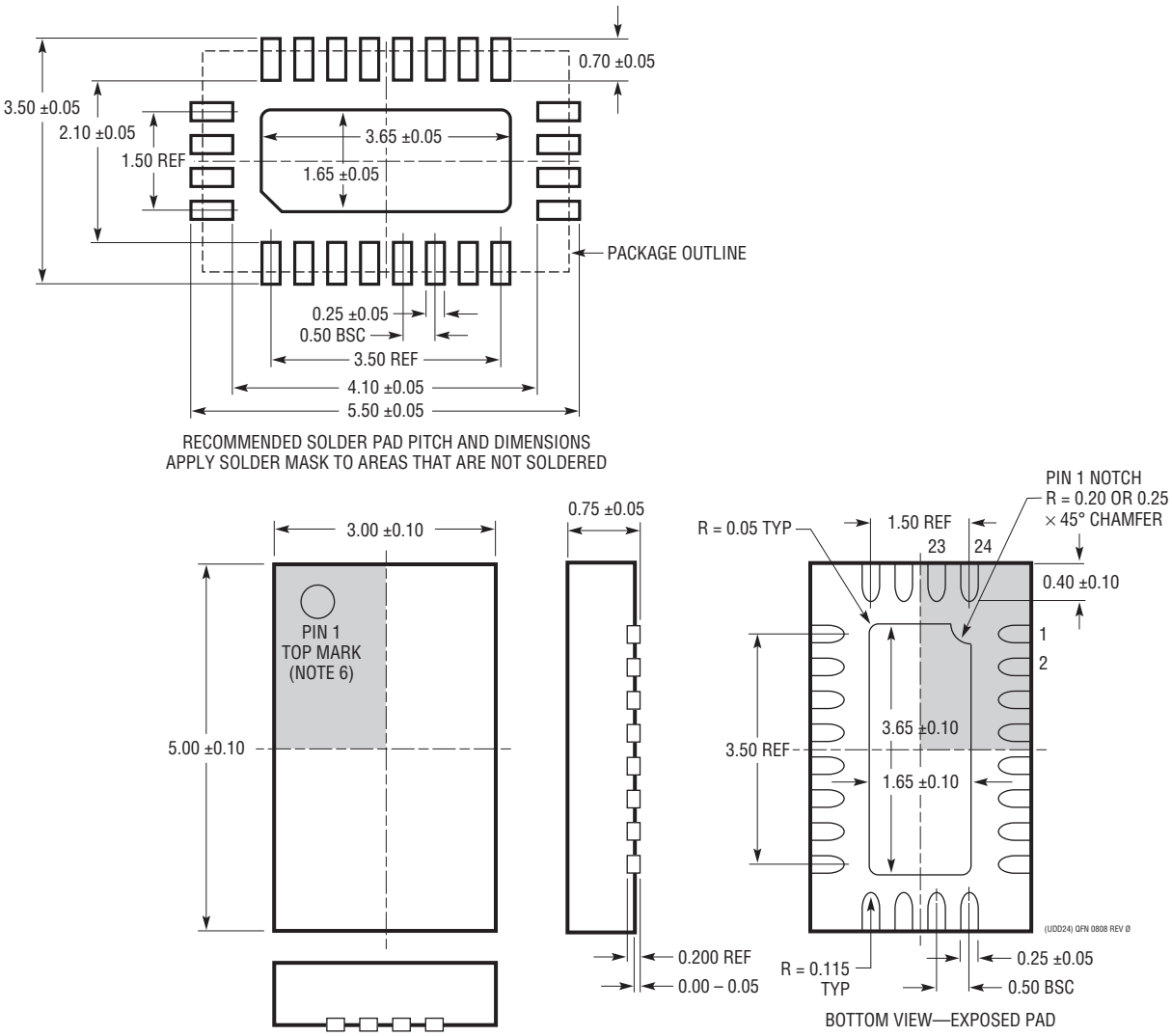
Output Voltage vs Load Current



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UDD Package
24-Lead Plastic QFN (3mm × 5mm)
(Reference LTC DWG # 05-08-1833 Rev Ø)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/15	Added H-Grade in Absolute Maximum Ratings and Order Information.	2
		Clarified Electrical Specifications.	3
		Added H-Grade in Note 2.	4
		Updated V_{USB5V} vs Temperature Graph.	4
		Updated V_{EN} vs Temperature, Top FET Current Limit vs Duty Cycle and Top FET Current Limit vs Temperature Graphs.	5
		Clarified Applications Information.	20
		Added LT4180 to Related Parts List.	28
B	06/15	Added Storage Temperature Range.	2
		Clarified SYNC Pin Current specifications.	3