36V_{IN}, 5.4A Buck-Boost µModule Regulator

FEATURES

- **Complete Buck-Boost Switch Mode Power Supply**
- **Wide Input Voltage Range: 5V to 36V**
- **Wide Output Voltage Range: 1.2V to 36V**
- **V_{IN} May Be Greater than, Equal to or Less than V_{OUT}**
- **12V/1.8A Output from 6V_{IN}**
- **12V/3.4A Output from 12V_{IN}**
- **12V/5.4A Output from 24V_{IN}**
- **Up to 94% Efficient**
- **Adjustable Input and Output Average Current Limits**
- **Input and Output Current Monitors**
- Parallelable for Increased Output Current
- Selectable Switching Frequency: 100kHz to 800kHz
- Synchronization from 200kHz to 700kHz
- 11.25mm × 15mm × 3.42mm BGA Package

APPLICATIONS

- High Power Battery-Operated Devices
- Industrial Control
- Solar Powered Voltage Regulator
- Solar Powered Battery Charging

DESCRIPTION

The LTM®8054 is a 36V_{IN}, buck-boost µModule® (micromodule) regulator. Included in the package are the switching controller, power switches, inductor and support components. A resistor to set the switching frequency, a resistor divider to set the output voltage, and input and output capacitors are all that are needed to complete the design. Other features such as input and output average current regulation may be implemented with just a few components. The LTM8054 operates over an input voltage range of 5V to 36V, and can regulate output voltages between 1.2V and 36V. The SYNC input and CLKOUT output allow easy synchronization.

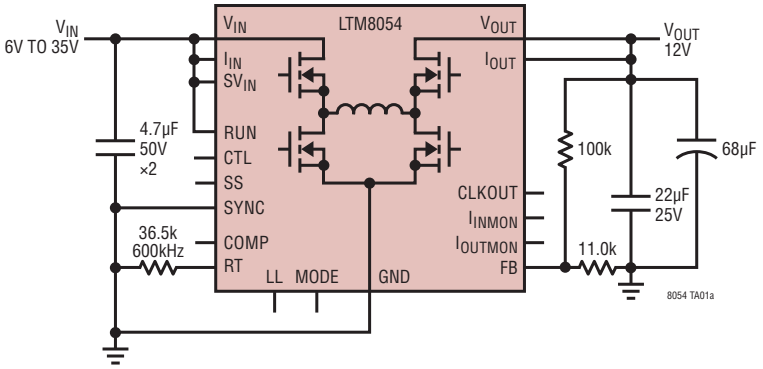
The LTM8054 is housed in a compact overmolded ball grid array (BGA) package suitable for automated assembly by standard surface mount equipment. The LTM8054 is RoHS compliant.

Buck Boost Selection Table

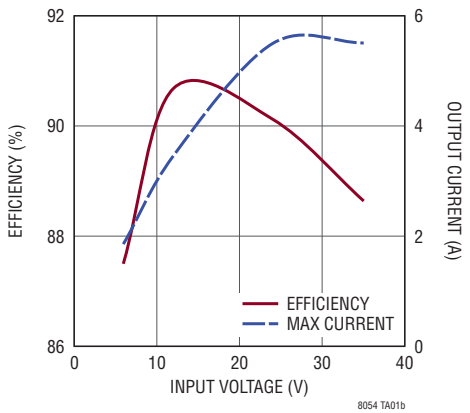
	LTM8054	LTM8055	LTM8056
V_{IN} (Operation)	36	36	58
V_{IN} Abs Max	40	40	60
V_{OUT} Abs Max	40	40	60
I_{OUT} (Peak) 24V_{IN}, 12V_{OUT}	5.4	8.5	5.5
Package	15 x 11.25mm x 3.42mm BGA	15 x 15mm x 4.92mm BGA	15 x 15mm x 4.92mm BGA

TYPICAL APPLICATION

12V_{OUT} from 5V to 35V_{IN} Buck Boost Regulator



Maximum Output Current and Efficiency vs Input Voltage

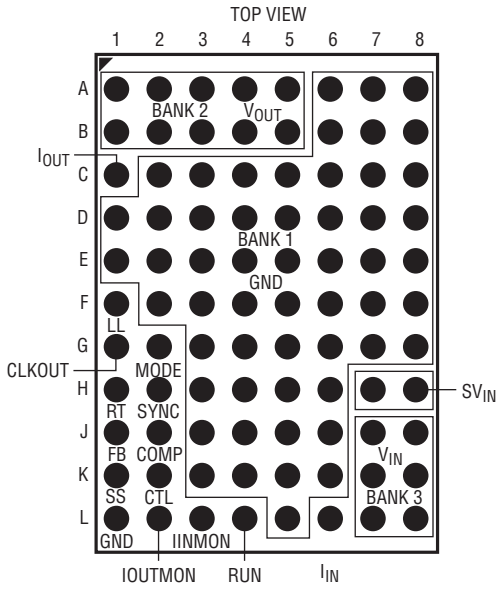


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, SV_{IN}, V_{OUT}, RUN, I_{IN}, I_{OUT} Voltage 40V
FB, SYNC, CTL, MODE Voltage 6V
I_{INMON}, I_{OUTMON} Voltage 6V
LL Voltage.....15V
Maximum Junction Temperature (Notes 2, 3)..... 125°C
Storage Temperature.....–55 to 125°C
Peak Solder Reflow Body Temperature ..... 245°C

PIN CONFIGURATION



BGA PACKAGE
88-LEAD (15mm × 11.25mm × 3.42mm)

T_{JMAX} = 125°C, θ_{JA} = 17.6°C/W, $\theta_{JCbottom}$ = 5.9°C/W, θ_{JCtop} = 10.7°C/W, θ_{JB} = 7.8°C/W,
WEIGHT = 1.4g, θ VALUES DETERMINED PER JEDEC 51-9, 51-12

ORDER INFORMATION

http://www.linear.com/product/LTM8054#orderinfo

PART NUMBER	TERMINAL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM8054EY#PBF	SAC305 (RoHS)	LTM8054Y	e1	BGA	3	–40°C to 125°C
LTM8054IY#PBF	SAC305 (RoHS)	LTM8054Y	e1	BGA	3	–40°C to 125°C
LTM8054IY	SnPb(63/37)	LTM8054Y	e0	BGA	3	–40°C to 125°C
LTM8054MPY#PBF	SAC305 (RoHS)	LTM8054Y	e1	BGA	3	–55°C to 125°C
LTM8054MPY	SnPb(63/37)	LTM8054Y	e0	BGA	3	–55°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Terminal Finish Part Marking: www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings: www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. RUN = 1.5V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage	$V_{IN} = SV_{IN}$	●			5.0	V
Output DC Voltage	FB = V_{OUT} Through 100k R_{FB} = 100k/3.40k			1.2 36		V V
Output DC Current	V_{IN} = 6V, V_{OUT} = 12V V_{IN} = 24V, V_{OUT} = 12V			1.8 5.4		A A
Quiescent Current Into V_{IN} (Tied to SV_{IN})	RUN = 0.3V (Disabled) No Load, MODE = 0.3V (DCM) No Load, MODE = 1.5V (FCM)			0.1 8 45	1 30 100	µA mA mA
Output Voltage Line Regulation	5V < V_{IN} < 36V, I_{OUT} = 1A			0.5		%
Output Voltage Load Regulation	V_{IN} = 24V, 0.1A < I_{OUT} < 3A			0.5		%
Output RMS Voltage Ripple	V_{IN} = 24V, I_{OUT} = 3A			25		mV
Switching Frequency	R_T = 453k R_T = 24.9k			100 800		kHz kHz
Voltage at FB Pin		 ●	1.188 1.176	1.2	1.212 1.220	V V
RUN Falling Threshold	LTM8054 Stops Switching	●	1.15		1.25	V
RUN Hysteresis	LTM8054 Starts Switching			25		mV
RUN Low Threshold	LTM8054 Disabled				0.3	V
RUN Pin Current	RUN = 1V RUN = 1.6V		2	3	5 100	µA nA
I_{IN} Bias Current				90		µA
Input Current Sense Threshold (I_{IN}-V_{IN})		●	44		56	mV
I_{OUT} Bias Current				20		µA
Output Current Sense Threshold (V_{OUT}-I_{OUT})	V_{CTL} = Open	●	53		63	mV
I_{INMON} Voltage	LTM8054 in Input Current Limit		0.96		1.04	V
I_{OUTMON} Voltage	LTM8054 in Output Current Limit		1.14		1.26	V
CTL Input Bias Current	V_{CTL} = 0V			22		µA
SS Pin Current	V_{SS} = 0V			35		µA
CLKOUT Output High	10k to GND		4			V
CLKOUT Output Low	10k to 5V				0.7	V
SYNC Input Low Threshold					0.3	V
SYNC Input High Threshold			1.5			V
SYNC Bias Current	SYNC = 1V			11		µA
MODE Input Low Threshold					0.3	V
MODE Input High Threshold			1.5			V

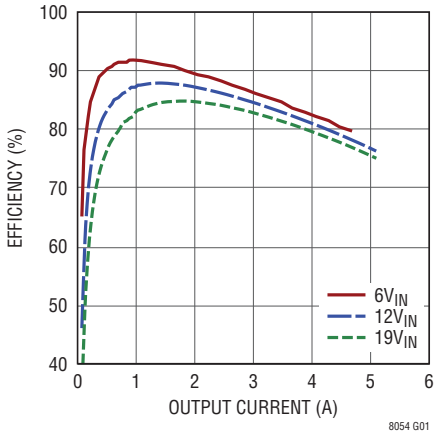
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM8054E is guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8054I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM8054MP is guaranteed to meet specifications over the full –55°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

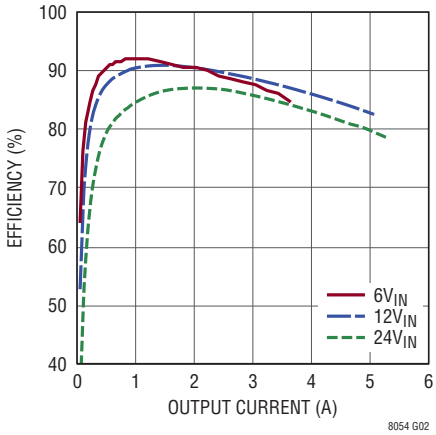
Note 3: The LTM8054 contains overtemperature protection that is intended to protect the device during momentary overload conditions. The internal temperature exceeds the maximum operating junction temperature when the overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

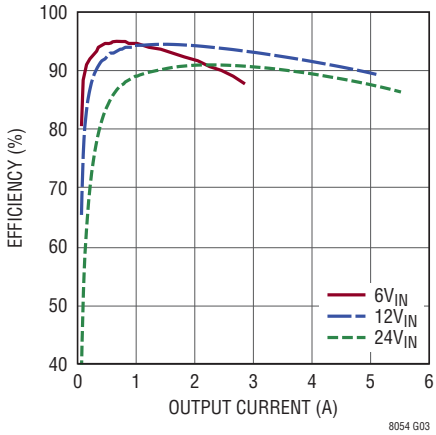
3.3V_{OUT} Efficiency



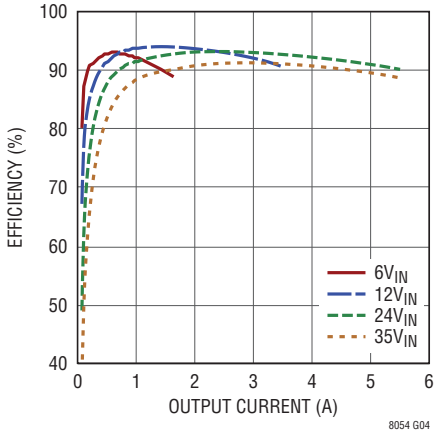
5V_{OUT} Efficiency



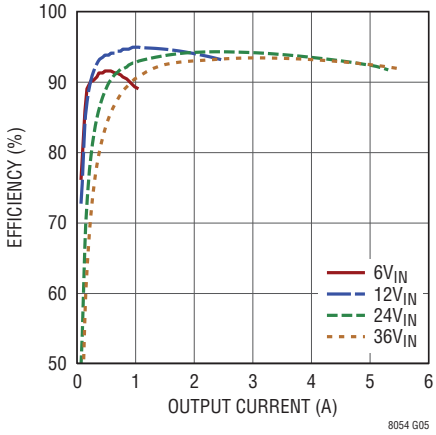
8V_{OUT} Efficiency



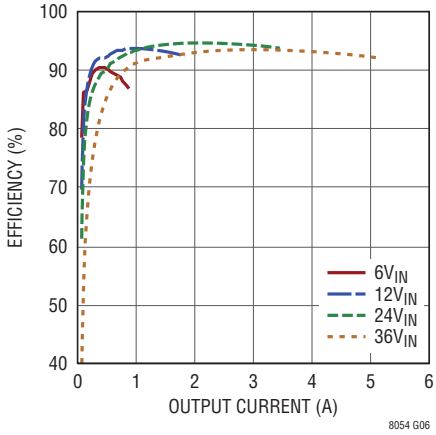
12V_{OUT} Efficiency



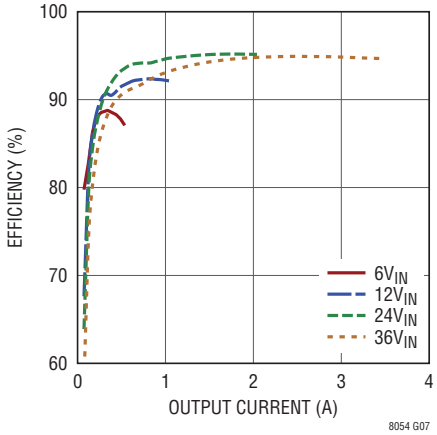
18V_{OUT} Efficiency



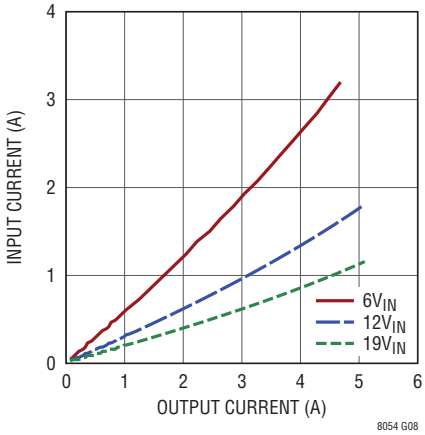
24V_{OUT} Efficiency



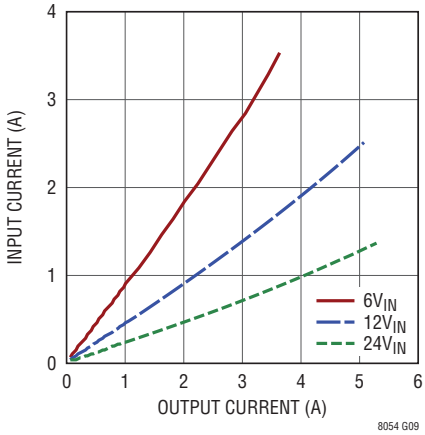
36V_{OUT} Efficiency



Input Current vs Output Current (3.3V_{OUT})

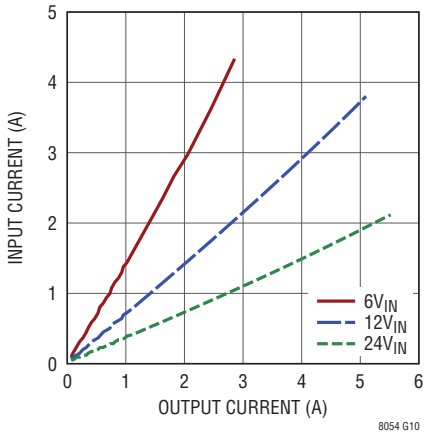


Input Current vs Output Current (5V_{OUT})

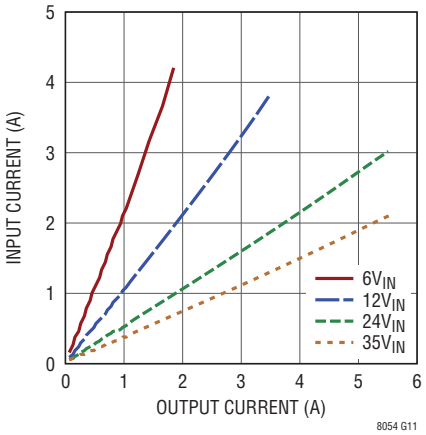


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

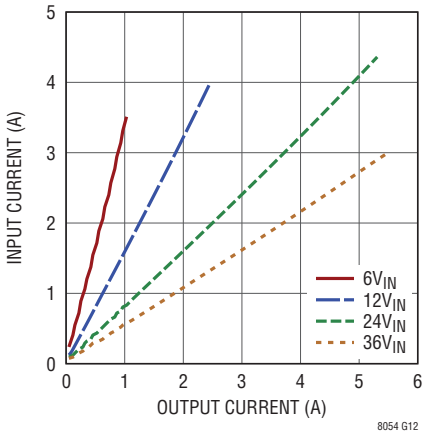
Input Current vs Output Current ($8V_{OUT}$)



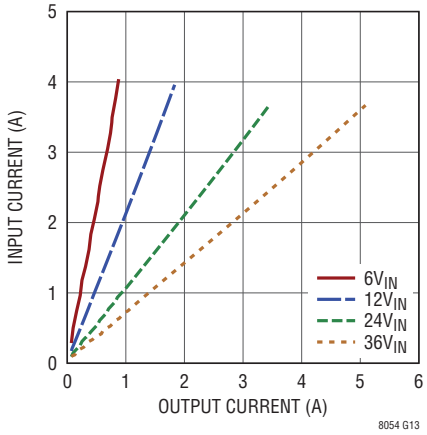
Input Current vs Output Current ($12V_{OUT}$)



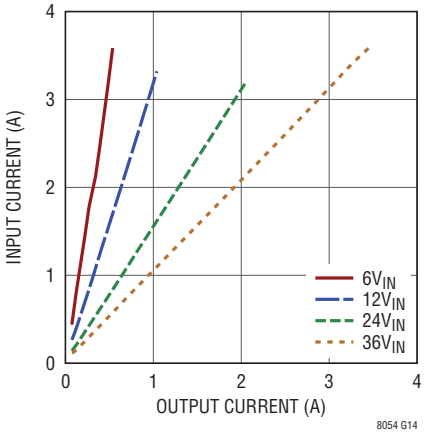
Input Current vs Output Current ($18V_{OUT}$)



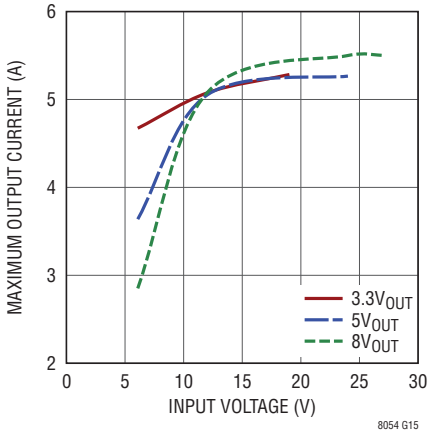
Input Current vs Output Current ($24V_{OUT}$)



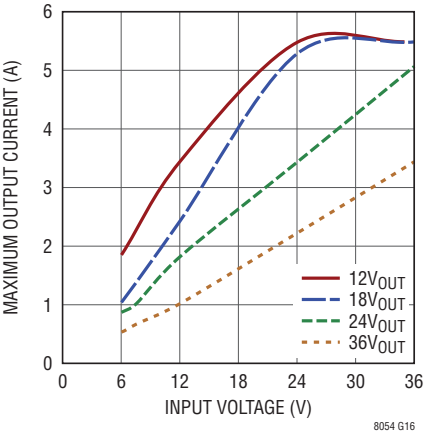
Input Current vs Output Current ($36V_{OUT}$)



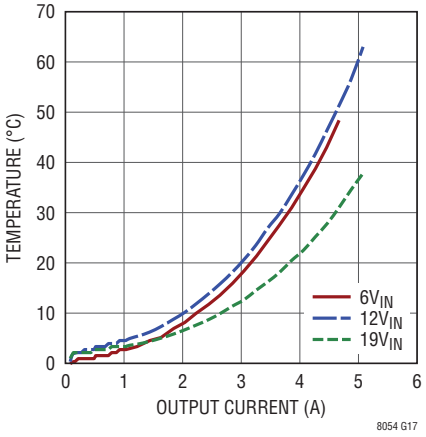
Maximum Output Current vs Input Voltage ($3.3V_{OUT}$, $5V_{OUT}$, $8V_{OUT}$)



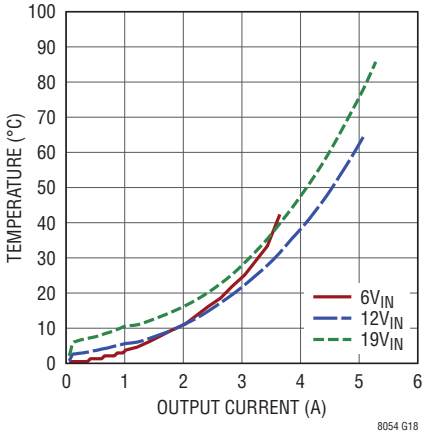
Maximum Output Current vs Input Voltage ($12V_{OUT}$, $18V_{OUT}$, $24V_{OUT}$, $36V_{OUT}$)



Junction Temperature Rise vs Output Current ($3.3V_{OUT}$)

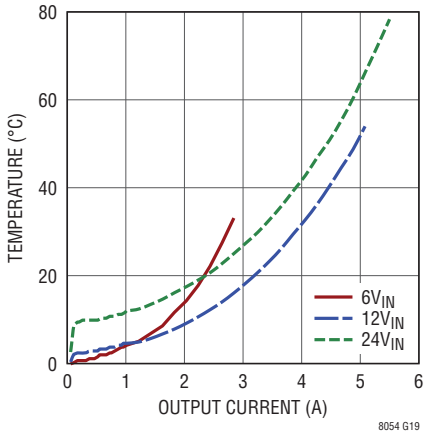


Junction Temperature Rise vs Output Current ($5V_{OUT}$)

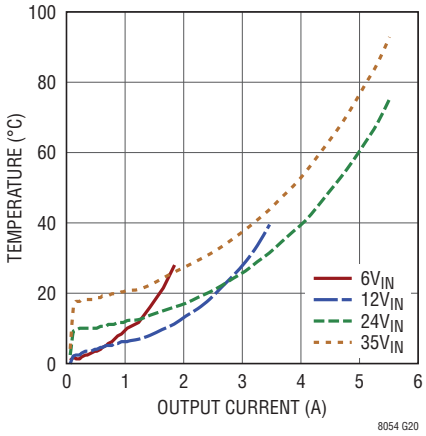


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

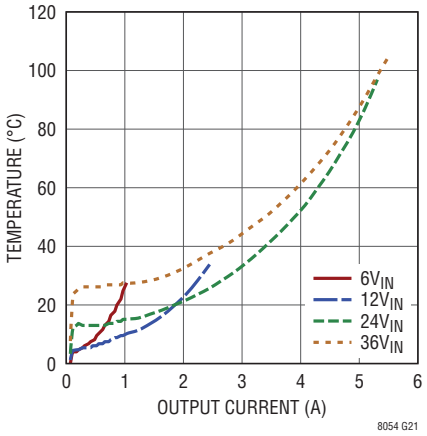
Junction Temperature Rise vs Output Current ($8V_{OUT}$)



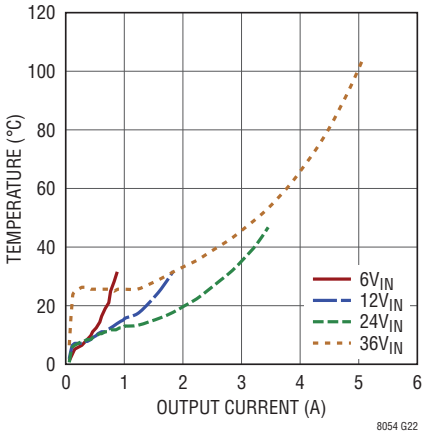
Junction Temperature Rise vs Output Current ($12V_{OUT}$)



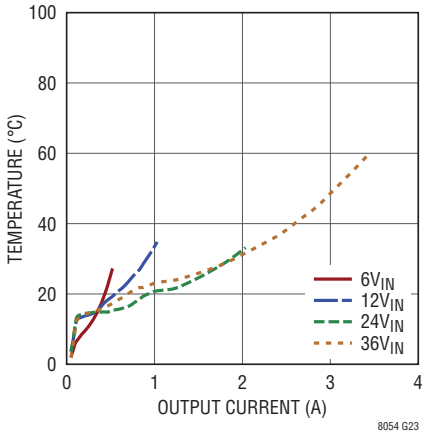
Junction Temperature Rise vs Output Current ($18V_{OUT}$)



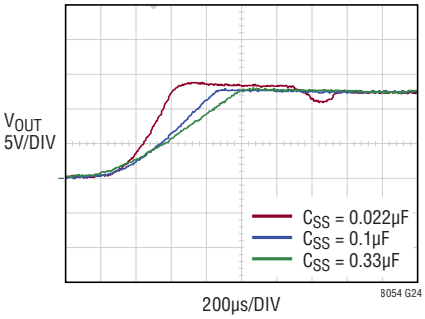
Junction Temperature Rise vs Output Current ($24V_{OUT}$)



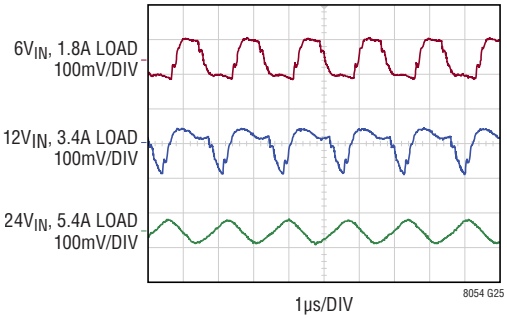
Junction Temperature Rise vs Output Current ($36V_{OUT}$)



Turn-On Response, Demo Board DC2016A, 3A Resistive Load



Output Voltage Ripple, $12V_{OUT}$ Stock DC2016A Demo Board



20MHz BW LIMIT, MEASURED ACROSS C8

PIN FUNCTIONS

GND (Bank 1, Pin L1): Tie these GND pins to a local ground plane below the LTM8054 and the circuit components. In most applications, the bulk of the heat flow out of the LTM8054 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details. Return the R_{FB1}/R_{FB2} feedback divider to this net.

V_{OUT} (Bank 2): Power Output Pins. Apply output filter capacitors between these pins and GND pins.

V_{IN} (Bank 3): Input Power. The V_{IN} pin supplies current to the LTM8054's internal power switches and to one terminal of the optional input current sense resistor. This pin must be locally bypassed with an external, low ESR capacitor; see Table 1 for recommended values.

I_{OUT} (Pin C1): Output Current Sense. Tie this pin to the output current sense resistor. The output average current sense threshold is 58mV, so the LTM8054 will regulate the output current to $58mV/R_{SENSE}$, where R_{SENSE} is the value of the output current sense resistor in ohms. The load is powered through the sense resistor connected at this pin. Tie this pin to V_{OUT} if no output current sense resistor is used. Keep this pin within ±0.5V of V_{OUT} under all conditions.

LL (Pin F1): Light Load Indicator. This open-drain pin indicates that the output current, as sensed through the resistor connected between V_{OUT} and I_{OUT}, is approximately equivalent to 6mV or less. Its state is meaningful only if a current sense resistor is applied between V_{OUT} and I_{OUT}. This is useful to change the switching behavior of the LTM8054 in light loads. LL is typically tied to MODE or left open, but not connected to other loads or signal sources.

SV_{IN} (Pins H7, H8): Controller Power Input. Apply a separate voltage above 5V if the LTM8054 is required to operate when the main power input (V_{IN}) is below 5V. Bypass these pins with a high quality, low ESR capacitor. If a separate supply is not used, connect these pins to V_{IN}.

CLKOUT (Pin G1): Clock Output. Use this pin as a clock source when synchronizing other devices to the switching frequency of the LTM8054. When this function is not used, leave this pin open.

MODE (Pin G2): Switching Mode Input. The LTM8054 operates in forced continuous mode when MODE is open, and can operate in discontinuous switching mode when MODE is low. In discontinuous switching mode, the LTM8054 will block reverse inductor current. This pin is normally left open or tied to LL. This pin may be tied to GND for the purpose of blocking reverse current if no output current sense resistor is used.

RT (Pin H1): Timing Resistor. The RT pin is used to program the switching frequency of the LTM8054 by connecting a resistor from this pin to ground. The range of oscillation is 100kHz to 800kHz. The Applications Information section of the data sheet includes a table to determine the resistance value based on the desired switching frequency. Minimize capacitance at this pin. A resistor to ground must be applied under all circumstances.

SYNC (Pin H2): External Synchronization Input. The SYNC pin has an internal pull-down resistor. See the Synchronization section in Applications Information for details. Tie this pin to GND when not used.

FB (Pin J1): Output Voltage Feedback. The LTM8054 regulates the FB pin to 1.2V. Connect the FB pin to a resistive divider between the output and GND to set the output voltage. The output voltage is determined by the equation

$$V_{OUT} = 1.2 \bullet \left(\frac{R_{TOP}}{R_{BOT}} + 1 \right)$$

where R_{TOP} and R_{BOT} are the top and bottom feedback resistors, respectively. See Table 1 for recommended FB divider resistor values.

COMP (Pin J2): Compensation Pin. The LTM8054 is equipped with internal compensation that works well with most applications. In some cases, the performance of the LTM8054 can be enhanced by modifying the control loop compensation by applying a capacitor or RC network to this pin.

PIN FUNCTIONS

SS (Pin K1): Soft-Start. Connect a capacitor from this pin to GND to increase the soft-start time. Soft-start reduces the input power source's surge current by gradually increasing the controller's current limit. Larger values of the soft-start capacitor result in longer soft-start times. If no soft-start is required, leave this pin open.

CTL (Pin K2): Current Sense Adjustment. Apply a voltage below 1.2V to reduce the current limit threshold of I_{OUT}. Drive CTL to less than about 50mV to stop switching. The CTL pin has an internal pull-up resistor to 2V. If not used, leave open.

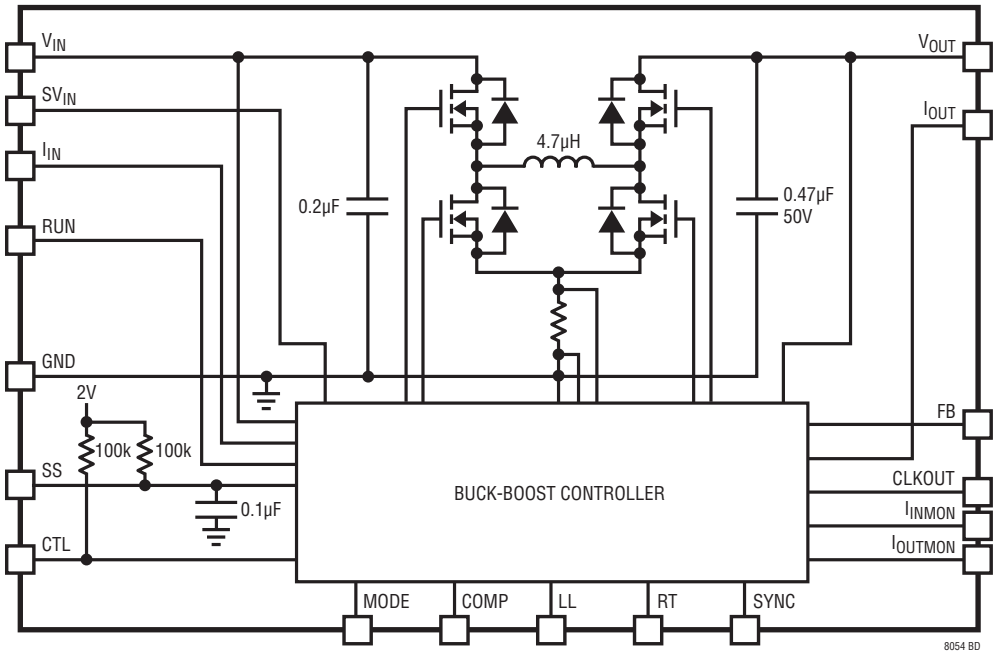
I_{OUTMON} (Pin L2): Output Current Monitor. This pin produces a voltage that is proportional to the voltage between V_{OUT} and I_{OUT}. I_{OUTMON} will equal 1.2V when $V_{OUT} - I_{OUT}$ = 58mV. This feature is generally useful only if a current sense resistor is applied between V_{OUT} and I_{OUT}.

I_{INMON} (Pin L3): Input Current Monitor. This pin produces a voltage that is proportional to the voltage between I_{IN} and V_{IN}. I_{INMON} will equal 1V when $I_{IN} - V_{IN}$ = 50mV. This feature is generally useful only if a current sense resistor is applied between V_{IN} and I_{IN}. This is a high impedance output. Use a buffer to drive a load.

RUN (Pin L4): LTM8054 Enable. Raise the RUN pin voltage above 1.2V for normal operation. Above 1.2V (typical), but below 6V, the RUN pin input bias current is less than 1µA. Below 1.2V and above about 0.3V, the RUN pin sinks 3µA so the user can define the hysteresis with the external resistor selection. This will also reset the soft-start function. If RUN is 0.3V or less, the LTM8054 is disabled and the input quiescent current is below 1µA.

I_{IN} (Pin L6): Input Current Sense. Tie this pin to the input current sense resistor. The input average current sense threshold is 50mV, so the LTM8054 will regulate the input current to 50mV/R_{SENSE}, where R_{SENSE} is the value of the input current sense resistor in ohms. Tie to V_{IN} when not used. Keep this pin within ±0.5V of V_{IN} under all conditions.

BLOCK DIAGRAM



OPERATION

The LTM8054 is a standalone nonisolated buck-boost switching DC/DC power supply. The buck-boost topology allows the LTM8054 to regulate its output voltage for input voltages both above and below the magnitude of the output, and the maximum output current depends upon the input voltage. Higher input voltages yield higher maximum output current.

This converter provides a precisely regulated output voltage programmable via an external resistor divider from 1.2V to 36V. The input voltage range is 5V to 36V, but the LTM8054 may be operated at lower input voltages if SV_{IN} is powered by a voltage source above 5V. A simplified block diagram is given on the previous page.

The LTM8054 contains a current mode controller, power switching elements, power inductor and a modest amount of input and output capacitance. The LTM8054 is a fixed frequency PWM regulator. The switching frequency is set by connecting the appropriate resistor value from the RT pin to GND.

The output voltage of the LTM8054 is set by connecting the FB pin to a resistor divider between V_{OUT} and GND.

In addition to regulating its output voltage, the LTM8054 is equipped with average current control loops for both the input and output. Add a current sense resistor between I_{IN} and V_{IN} to limit the input current below some maximum value. The I_{INMON} pin reflects the current flowing though the sense resistor between I_{IN} and V_{IN}.

A current sense resistor between V_{OUT} and I_{OUT} allows the LTM8054 to accurately regulate its output current to a maximum value set by the value of the sense resistor.

In general, the LTM8054 should be used with an output sense resistor to limit the maximum output current, as buck-boost regulators are capable of delivering large currents when the output voltage is lower than the input, if demanded.

Furthermore, while the LTM8054 does not require an output sense resistor to operate, it uses information from the sense resistor to optimize its performance. If an output sense resistor is not used, the efficiency or output ripple may degrade, especially if the current through the integrated inductor is discontinuous. In some cases, an output sense resistor is required to adequately protect the LTM8054 against output overload or short-circuit.

A voltage less than 1.2V applied to the CTL pin reduces the maximum output current. The current flowing through the sense resistor is reflected by the output voltage of the I_{OUTMON} pin. Drive CTL to less than about 50mV to stop switching.

Driving the SYNC pin will synchronize the LTM8054 to an external clock source. The CLKOUT pin sources a signal that is the same frequency but approximately 180° out of phase with the internal oscillator.

If more output current is required than a single LTM8054 can provide, multiple devices may be operated in parallel. Refer to the Parallel Operation section of Applications Information for more details.

An internal regulator provides power to the control circuitry and the gate driver to the power MOSFETs. This internal regulator draws power from the SV_{IN} pin. The RUN pin is used to place the LTM8054 in shutdown, disconnecting the output and reducing the input current to less than 1µA.

The LTM8054 is equipped with a thermal shutdown that inhibits power switching at high junction temperatures. The activation threshold of this function is above 125°C to avoid interfering with normal operation, so prolonged or repetitive operation under a condition in which the thermal shutdown activates may damage or impair the reliability of the device.

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For most applications, the design process is straight forward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT}, R_{FB1}/R_{FB2} and R_T values.
3. Apply the output sense resistor to set the output current limit. The output current is limited to $58mV/R_{SENSE}$, where R_{SENSE} is the value of the output current sense resistor in ohms.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions. Bear in mind that the maximum output current is limited by junction temperature, the relationship between the input and output voltage magnitude and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

The maximum frequency (and attendant R_T value) at which the LTM8054 should be allowed to switch is given in Table 1 in the f_{MAX} column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the $f_{OPTIMAL}$ column. There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Synchronization section for details.

Note that Table 1 calls out both ceramic and electrolytic output capacitors. Both of the capacitors called out in the table must be applied to the output. The electrolytic capacitors in Table 1 are described by voltage rating, value and ESR. The voltage rating of the capacitor may be increased if the application requires a higher voltage stress derating. The LTM8054 can tolerate variation in the ESR; other capacitors with different ESR may be used, but the user must verify proper operation over line, load and environmental conditions. Table 2 gives the description and part numbers of electrolytic capacitors used in the LTM8054 development testing and design validation.

Table 1. Table 1. Recommended Component Values and Configuration (T_A = 25°C)

V_{IN} Range	V_{OUT}	C_{IN}	C_{OUT}	R_{ADJ}	$f_{OPTIMAL}$ (kHz)	$R_{T(OPTIMAL)}$	f_{MAX} (kHz)	$R_{T(MIN)}$
5V to 19V	3.3V	2 × 4.7µF, 50V, X5R, 0805	47µF, 4V, X5R, 1206 100µF, 6V, 75mΩ, Electrolytic C Case	100k/56.2k	600	36.5k	800	24.9k
5V to 25V	5V	2 × 4.7µF, 50V, X5R, 0805	22µF, 6.3V, X5R, 0805 100µF, 6V, 75mΩ, Electrolytic C Case	100k/31.6k	550	39.2k	800	24.9k
5V to 27V	8V	2 × 4.7µF, 50V, X5R, 0805	22µF, 10V, X7R, 1206 100µF, 16V, 100mΩ, Electrolytic D Case	100k/17.4k	500	45.3k	800	24.9k
5V to 35V	12V	2 × 4.7µF, 50V, X5R, 0805	22µF, 25V, X5R, 0805 68µF, 16V, 200mΩ, Electrolytic C Case	100k/11k	600	36.5k	800	24.9k
5.9V to 36V	18V	2 × 4.7µF, 50V, X5R, 0805	22µF, 25V, X5R, 0805 47µF, 25V, 900mΩ, Electrolytic D Case	100k/6.98k	500	45.3k	800	24.9k
7.5V to 36V	24V	2 × 4.7µF, 50V, X5R, 0805	22µF, 25V, X5R, 0805 33µF, 35V, 300mΩ, Electrolytic D Case	100k/5.23k	650	31.6k	800	24.9k
7.5V to 36V	36V	2 × 4.7µF, 50V, X5R, 0805	10µF, 50V, X5R, 1206 10µF, 50V, 120mΩ, Electrolytic 6.3mm × 6mm Case	100k/3.40k	650	31.6k	800	24.9k

Notes: A input bulk capacitor is required.
The output capacitance uses a combination of a ceramic and electrolytic in parallel.
Other combinations of resistor values for the RFB network are acceptable.

Table 2. Table 2. Electrolytic Caps Used in LTM8054 Testing

DESCRIPTION	MANUFACTURER	PART NUMBER
100µF, 6V, 75mΩ, Tantalum C Case	AVX	TPSC107M006R0075
100µF, 16V, 100mΩ, Tantalum Y Case	AVX	TPSY107M016R0100
68µF, 16V, 200mΩ, Tantalum C Case	AVX	TPSC686M016R0200
47µF, 25V, 900mΩ, Tantalum D Case	AVX	TAJD476M025R
33µF, 35V, 300mΩ, Tantalum D Case	AVX	TPSD336M035R0300
10µF, 50V, 120mΩ, Aluminum 6.3mm × 6mm case	SunCon	50HVP10M

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Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended, and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8054. A ceramic input capacitor combined with trace or cable inductance forms a high Q (underdamped) tank circuit. If the LTM8054 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Frequency Selection

The LTM8054 uses a constant frequency PWM architecture that can be programmed to switch from 100kHz to 800kHz by tying a resistor from the RT pin to ground. Table 3 provides a list of R_T resistor values and their resultant frequencies.

Table 3. Switching Frequency vs R_T Value

FREQUENCY	R_T VALUE (kΩ)
100	453
200	147
300	84.5
400	59
500	45.3
600	36.5
700	29.4
800	20.5

An external resistor from RT to GND is required. Do not leave this pin open, even when synchronizing to an external clock. When synchronizing the switching of the LTM8054 to an external signal source, the frequency range is 200kHz to 700kHz.

Operating Frequency Trade-Offs

It is recommended that the user apply the optimal R_T value given in Table 1 for the input and output operating condition. System level or other considerations, however, may necessitate another operating frequency. While the LTM8054 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat or even damage the LTM8054 if the output is overloaded or short circuited. A frequency that is too low can result in a final design that has too much output ripple, too large of an output capacitor or is unstable.

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Parallel Operation

Two or more LTM8054s may be combined to provide increased output current by configuring them as a master and a slave, as shown in Figure 1. Each LTM8054 is equipped with an I_{OUTMON} and a CTL pin. The I_{OUTMON} pin's 0 to 1.2V signal reflects the current passing through the output sense resistor, while a voltage less than 1.2V applied to the CTL pin will limit the current passing through the output sense resistor. By applying the voltage of the master's I_{OUTMON} pin to the slave's CTL pin, the two units will source the same current to the load, assuming each LTM8054 output current sense resistor is the same value.

The design of a master-slave configuration is straightforward:

1. Apply the FB resistor network to the master, choosing the proper values for the desired output voltage. Suggested values for popular output voltages are provided in Table 1.
2. Apply a FB resistor network to the individual slaves so that the resulting output is higher than the desired output voltage.
3. Apply the appropriate output current sense resistors between V_{OUT} and I_{OUT}. If the same value is used for the master and slave units, they will share current equally.
4. Connect the master I_{OUTMON} to the slaves' CTL pin through a unity gain buffer. The unity gain buffer is required to isolate the output impedance of the LTM8054 from the integrated pull-up on the CTL pins.
5. Tie the outputs together.

Note that this configuration does not require the inputs to be tied together, making it simple to power a single heavy load from multiple input sources. Ensure that each input power source has sufficient voltage and current sourcing capability to provide the necessary power. Please refer to the Maximum Output Current vs V_{IN} and Input Current vs Output Current curves in the Typical Performance Characteristics section for guidance.

Paralleled LTM8054s should normally be allowed to switch in discontinuous mode to prevent current from flowing from the output of one unit into another; that is, the MODE pin should be tied to LL. In some cases, operating the master in forced continuous (MODE open) and the slaves in discontinuous mode (MODE = LL) is desirable. If so, current from the output can flow into the master's input. Please refer to Input Precaution in this section for a discussion of this behavior.

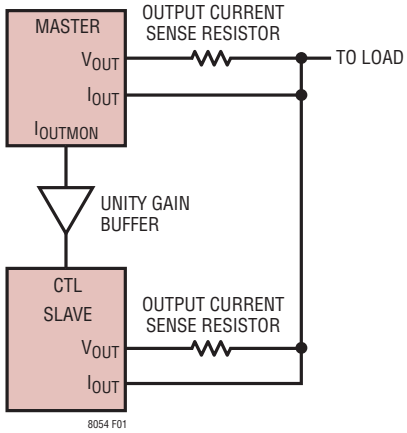

Figure 1. Two or More LTM8054s May Be Connected in a Master/Slave Configuration for Increased Output Current

Minimum Input Voltage and RUN

The LTM8054 needs a minimum of 5V for proper operation, but system parameters may dictate that the device operate only above some higher input voltage. For example, a LTM8054 may be used to produce $12V_{OUT}$, but the input power source may not be budgeted to provide enough current if the input supply voltage is below 8V.

The RUN pin has a typical falling voltage threshold of 1.2V and a typical hysteresis of 25mV. In addition, the pin sinks 3µA below the RUN threshold. Based upon the above information and the circuit shown in Figure 2, the V_{IN} rising (turn-on) threshold is:

$$V_{IN} = (3\mu A \bullet R1) + 1.225V\frac{R1+R2}{R2}$$

and the V_{IN} falling turn-off threshold is:

$$V_{IN} = 1.2\frac{R1+R2}{R2}$$

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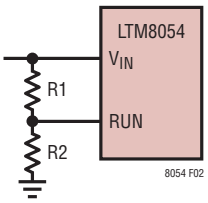

Figure 2. This Simple Resistor Network Sets the Minimum Operating Input Voltage Threshold with Hysteresis

Minimum Input Voltage and SV_{IN}

The minimum input voltage of the LTM8054 is 5V, but this is only if V_{IN} and SV_{IN} are tied to the same voltage source. If SV_{IN} is powered from a power source at or above 5VDC, V_{IN} can be allowed to fall below 5V and the LTM8054 can still operate properly. Some examples of this are provided in the Typical Applications section.

Soft-Start

Soft-start reduces the input power sources' surge currents by gradually increasing the controller's current. As indicated in the Block Diagram, the LTM8054 has an internal soft-start RC network. Depending upon the load and operating conditions, the internal network may be sufficient for the application. To increase the soft-start time, simply add a capacitor from SS to GND.

Output Current Limit (I_{OUT})

The LTM8054 features an accurate average output current limit set by an external sense resistor placed between V_{OUT} and I_{OUT} as shown in Figure 3. V_{OUT} and I_{OUT} internally connect to a differential amplifier that limits the current when the voltage $V_{OUT} – I_{OUT}$ reaches 58mV. The current limit is:

$$I_{OUT(LIM)} = \frac{58mV}{R_{SENSE}}$$

where R_{SENSE} is the value of the sense resistor in ohms.

Most applications should use an output sense resistor as shown in Figure 3, if practical. The internal buck-boost power stage is current limited, but is nonetheless capable of delivering large amounts of current in an overload condition, especially when the output voltage is much lower than the input and the power stage is operating as a buck converter.

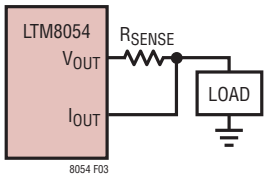

Figure 3. Set The LTM8054 Output Current Limit with an External Sense Resistor

When the voltage across the output sense resistor falls to about 1/10th of full scale, the LL pin pulls low. If there is no output sense resistor, and I_{OUT} is tied to V_{OUT}, LL will be active low. Applying an output sense resistor and tying the LL and MODE pins together can improve performance—see Switching Mode in this section.

In high step-down voltage regulator applications, the internal current limit can be quite high to allow proper operation. This can potentially damage the LTM8054 in overload or short-circuit conditions. Apply an output current sense resistor to set an appropriate current limit to protect the LTM8054 against these fault conditions.

Output Current Limit Control (CTL)

Use the CTL input to reduce the output current limit from the value set by the external sense resistor applied between V_{OUT} and I_{OUT}. The typical control range is between 0V and 1.2V. The CTL pin does not directly affect the input current limit. If this function is not used, leave CTL open. Drive CTL to less than about 50mV to stop switching. The CTL pin has an internal pull-up resistor to 2V.

Input Current Limit (I_{IN})

Some applications require that the LTM8054 draw no more than some predetermined current from the power source. Current limited power sources and power sharing are two examples. The LTM8054 features an accurate input current limit set by an external sense resistor placed between I_{IN} and V_{IN} as shown in Figure 4. V_{IN} and I_{IN} internally con-

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nect to a differential amplifier that limits the current when the voltage $I_{IN} – V_{IN}$ reaches 50mV. The current limit is:

$$I_{IN(LIM)} = \frac{50mV}{R_{SENSE}}$$

where R_{SENSE} is the value of the sense resistor in ohms.

If input current limiting is not required, simply tie I_{IN} to V_{IN}.

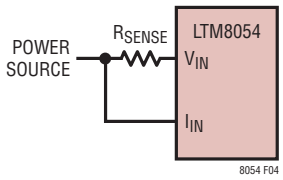

Figure 4. Set the LTM8054 Input Current Limit with an External Sense Resistor

Input Current Monitor (I_{INMON})

The I_{INMON} pin produces a voltage equal to approximately 20 times the voltage of $I_{IN} – V_{IN}$. Since the LTM8054 input current limit engages when $I_{IN} – V_{IN}$ = 50mV, I_{INMON} will be 1V at maximum input current.

Output Current Monitor (I_{OUTMON})

The I_{OUTMON} pin produces a voltage proportional to the voltage of $V_{OUT} – I_{OUT}$. When output current limit engages at maximum output current, $V_{OUT} – I_{OUT}$ = 58mV and I_{OUTMON} will be 1.2V.

Synchronization

The LTM8054 switching frequency can be synchronized to an external clock using the SYNC pin. Driving SYNC with a 50% duty cycle waveform is a good choice, otherwise maintain the duty cycle between about 10% and 90%. When synchronizing, a valid resistor value (that is, a value that results in a free-running frequency of 100kHz to 800kHz) must be connected from RT to GND. While an RT resistor is required for proper operation, the value of this resistor is independent of the frequency of the externally applied SYNC signal. Be aware, however, that the LTM8054 will switch at the frequency prescribed by the RT value if the SYNC signal terminates, so choose an appropriate resistor value.

CLKOUT

The CLKOUT signal reflects the internal switching clock of the LTM8054. It is phase shifted by approximately 180° with respect to the leading edge of the internal clock. If CLKOUT is connected to the SYNC input of another LTM8054, the two devices will switch 180° out of phase.

Input Precaution

In applications where the output voltage is deliberately pulled up above the set regulation voltage or the FB pin is abruptly driven to a new voltage, the LTM8054 may attempt to regulate the voltage by removing energy from the load for a short period of time after the output is pulled up. Since the LTM8054 is a synchronous switching converter, it delivers this energy to the input. If there is nothing on the LTM8054 input to consume this energy, the input voltage may rise. If the input voltage rises without intervention, it may rise above the absolute maximum rating, damaging the part. Carefully examine the input voltage behavior to see if the application causes it to rise.

In many cases, the system load on the LTM8054 input bus will be sufficient to absorb the energy delivered by the µModule regulator. The power required by other devices will consume more than enough to make up for what the LTM8054 delivers. In cases where the LTM8054 is the largest or only power converter, this may not be true and some means may need to be devised to prevent the LTM8054's input from rising too high. Figure 5a shows a passive crowbar circuit that will dissipate energy during momentary input overvoltage conditions. The break-down voltage of the Zener diode is chosen in conjunction with the resistor R to set the circuit's trip point. The trip point is typically set well above the maximum V_{IN} voltage under normal operating conditions. This circuit does not have a precision threshold, and is subject to both part-to-part and temperature variations, so it is most suitable for applications where the maximum input voltage is much less than the $40V_{IN}$ absolute maximum. As stated earlier, this type of circuit is best suited for momentary overvoltages.

Figure 5a is a crowbar circuit, which attempts to prevent the input voltage from rising above some level by dumping energy to GND through a power device. In some cases,

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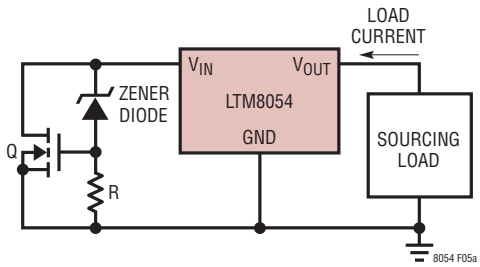

Figure 5a. The MOSFET Q Dissipates Momentary Energy to GND. The Zener Diode and Resistor Are Chosen to Ensure That the MOSFET Turns On Above the Maximum V_{IN} Voltage Under Normal Operation

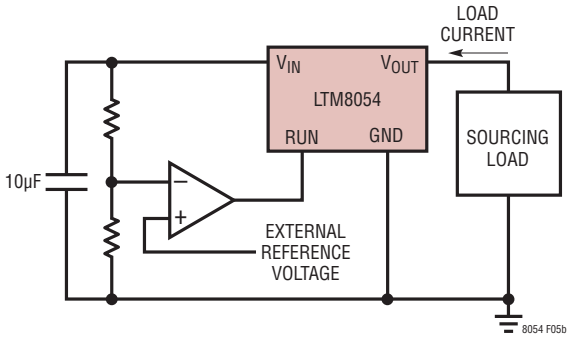

Figure 5b. This Comparator Circuit Turns Off the LTM8054 if the Input Rises Above a Predetermined Threshold. When the LTM8054 Turns Off, the Energy Stored in the Internal Inductor Will Raise V_{IN} a Small Amount Above the Threshold

it is possible to simply turn off the LTM8054 when the input voltage exceeds some threshold. An example of this circuit is shown in Figure 5b. When the power source on the output drives V_{IN} above a predetermined threshold, the comparator pulls down on the RUN pin and stops switching in the LTM8054. When this happens, the input capacitance needs to absorb the energy stored within the LTM8054's internal inductor, resulting in an additional voltage rise. This voltage rise depends upon the input capacitor size and how much current is flowing from the LTM8054 output to input.

Switching Mode

The MODE pin allows the user to select either discontinuous mode or forced continuous mode switching operation. In forced continuous mode, the LTM8054 will not skip cycles, even when the internal inductor current falls to zero or even reverses direction. This has the advantage of operating at the same fixed frequency for all load conditions, which can be useful when designing to EMI or output noise specifications. Forced continuous mode, however, uses more current at light loads, and allows current to flow from the load back into the input if the output is raised above the regulation point. This reverse current can raise the input voltage and be hazardous if the input is allowed to rise uncontrollably. Please refer to Input Precautions in this section for a discussion of this behavior.

Forced continuous operation may provide improved output regulation when the LTM8054 transitions from buck, buck-boost or boost operating modes, especially at lighter loads. In such a case, it can be desirable to operate in forced continuous mode except when the internal inductor current is about to reverse. If so, apply a current sense resistor between V_{OUT} and I_{OUT} and tie the LL and MODE pins together. The LL pin is low when the current through the output sense resistor is about one-tenth the full-scale maximum. When the output current falls to this level, the LL pin will pull the MODE pin down, putting the LTM8054 in discontinuous mode, preventing reverse current from flowing from the output to the input. In the case where MODE and LL are tied together, a small capacitor (~0.1µF) from these pins to GND may improve the light load transient response by delaying the transition from the discontinuous to forced continuous switching modes. MODE may be tied to GND for the purpose of blocking reverse current if no output current sense resistor is used.

FB Resistor Divider and Load Regulation

The LTM8054 regulates its FB pin to 1.2V, using a resistor divider to sense the output voltage. The location at which the output voltage is sensed affects the load regulation. If there is a current sense resistor between V_{OUT} and I_{OUT}, and the output is sensed at V_{OUT}, the voltage at the load will drop by the value of the current sense resistor multiplied by the output current. If the output voltage can be sensed at I_{OUT}, the load regulation may be improved.

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PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8054. The LTM8054 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 6 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

A few rules to keep in mind are:

1. Place the R_{FB} and R_T resistors as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8054.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM8054.
4. Minimize the trace resistance between the optional output current sense resistor, R_{OUT}, and V_{OUT}. Minimize the loop area of the I_{OUT} trace and the trace from V_{OUT} to R_{OUT}.
5. Minimize the trace resistance between the optional input current sense resistor, R_{IN} and V_{IN}. Minimize the loop area of the I_{IN} trace and the trace from V_{IN} to R_{IN}.
6. Place the C_{IN} and C_{OUT} capacitors such that their ground current flow directly adjacent or underneath the LTM8054.
7. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8054.
8. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 6. The LTM8054 can benefit from the heat sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

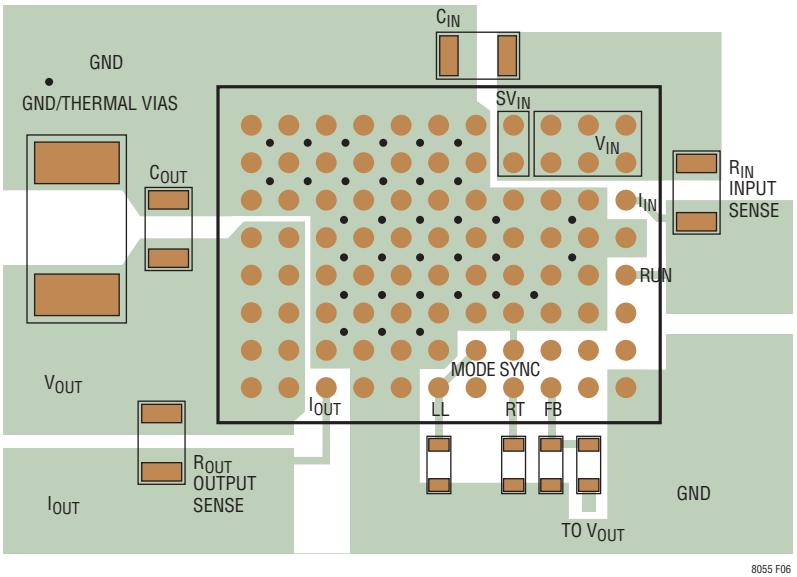

Figure 6. Layout Showing Suggested External Components, GND Plane and Thermal Vias

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Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8054. However, these capacitors can cause problems if the LTM8054 is plugged into a live supply (see Linear Technology Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8054 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8054's rating and damaging the part. If the input supply is poorly controlled or the LTM8054 is hot-plugged into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series with V_{IN}, but the most popular method of controlling input voltage overshoot is to add an electrolytic bulk capacitor to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit.

Thermal Considerations

The LTM8054 output current may need to be derated if it is required to operate in a high ambient temperature or deliver a large amount of continuous power. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by a LTM8054 mounted to a 58cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

The thermal resistance numbers listed in the Pin Configuration of the data sheet are based on modeling the µModule package mounted on a test board specified per JESD 51-9 (Test Boards for Area Array Surface Mount Package Thermal Measurements). The thermal coefficients provided on this page are based on JESD 51-12 (Guidelines for Reporting and Using Electronic Package Thermal Information).

For increased accuracy and fidelity to the actual application, many designers use FEA to predict thermal performance. To that end, the Pin Configuration of the data sheet typically gives four thermal coefficients:

θ_{JA} – Thermal resistance from junction to ambient.

$\theta_{JCbottom}$ – Thermal resistance from junction to the bottom of the product case.

θ_{JCtop} – Thermal resistance from junction to top of the product case.

θ_{JB} – Thermal resistance from junction to the printed circuit board.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased below:

θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

$\theta_{JCbottom}$ is the thermal resistance between the junction and bottom of the package with all of the component power dissipation flowing through the bottom of the package. In the typical µModule converter, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule converter are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this

APPLICATIONS INFORMATION

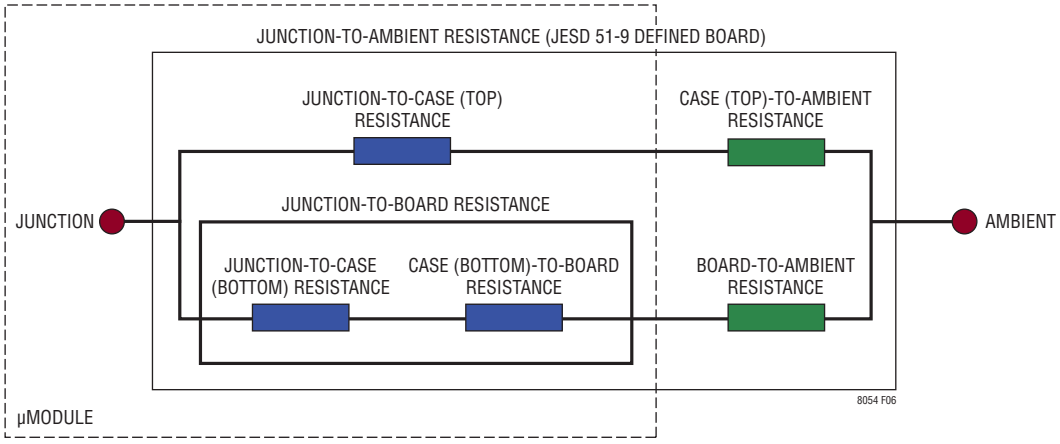


Figure 7

value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JB} is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule converter and into the board, and is usually the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a 2-sided, 2-layer board. This board is described in JESD 51-9.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule converter. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature versus load graphs given in the product's data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

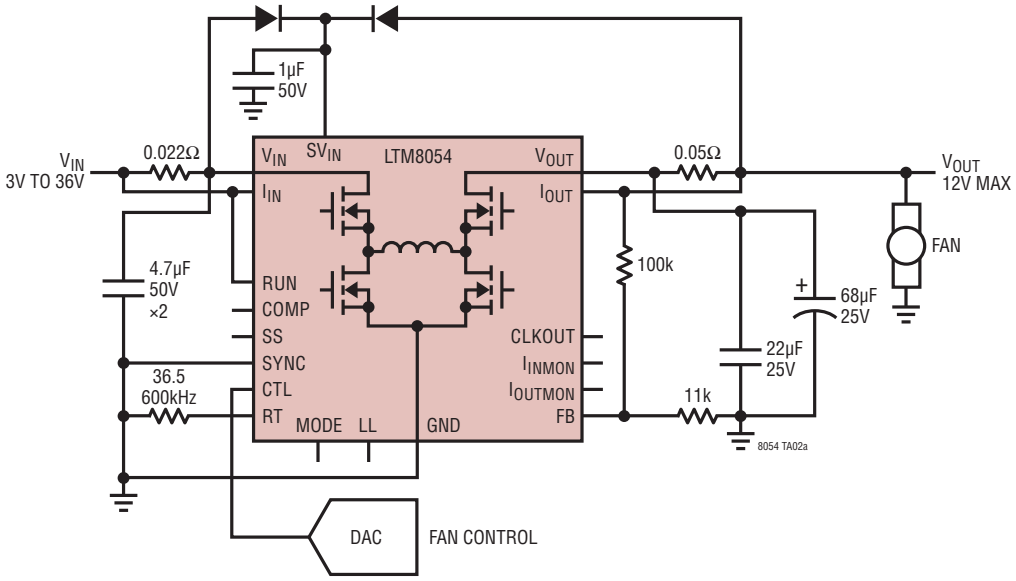
A graphical representation of these thermal resistances is given in Figure 7.

The blue resistances are contained within the µModule converter, and the green are outside.

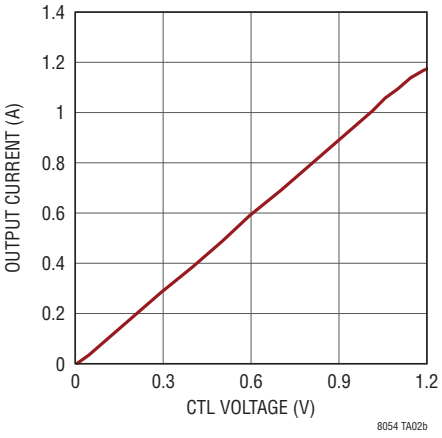
The die temperature of the LTM8054 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8054. The bulk of the heat flow out of the LTM8054 is through the bottom of the µModule converter and the BGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

TYPICAL APPLICATIONS

12V_{OUT} Fan Power from 3V_{IN} to 36V_{IN} with Analog Current Control and 2A Input Current Limiting

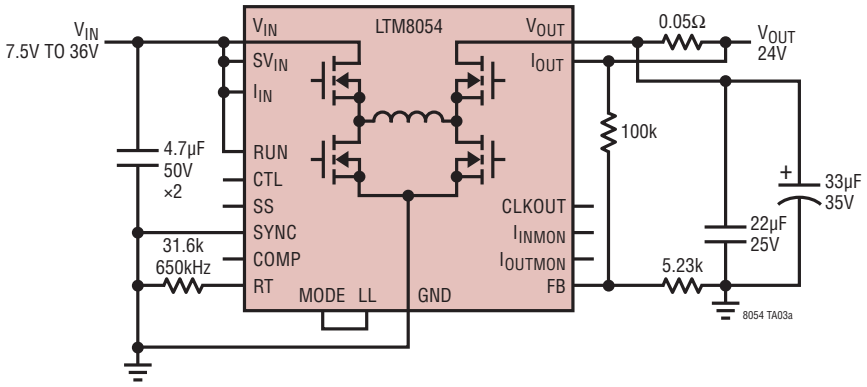


Maximum Output Current vs CTL Voltage, 12V_{IN}

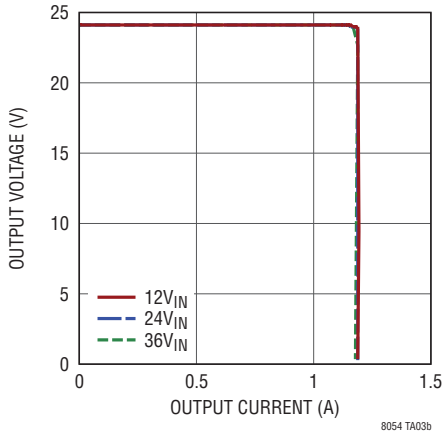


TYPICAL APPLICATIONS

24V_{OUT} from 7.5V_{IN} to 36V_{IN} with 1.2A Accurate Current Limit

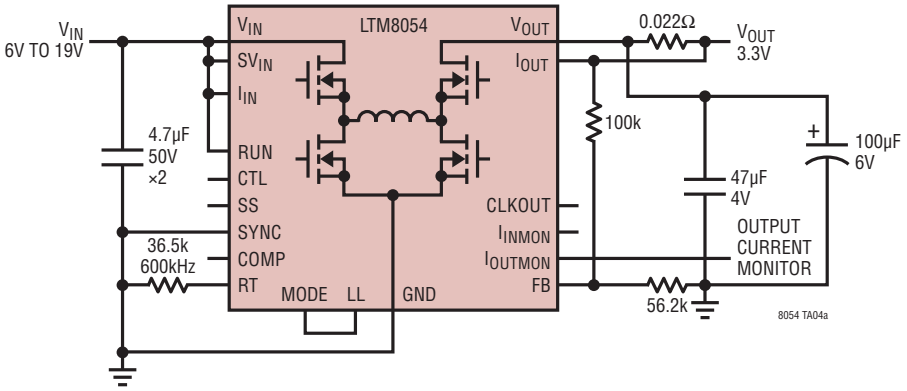


Output Voltage vs Output Current

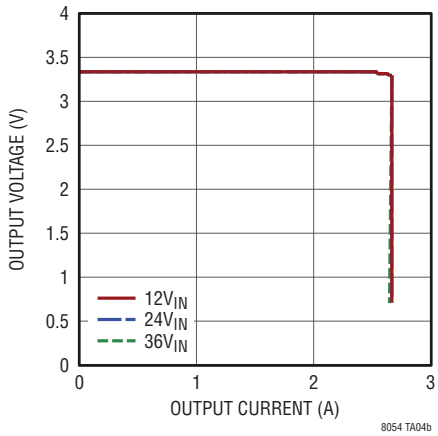


TYPICAL APPLICATIONS

3.3V_{OUT} from 6V_{IN} to 19V_{IN} with 2.6A Accurate Current Limit and Output Current Monitor

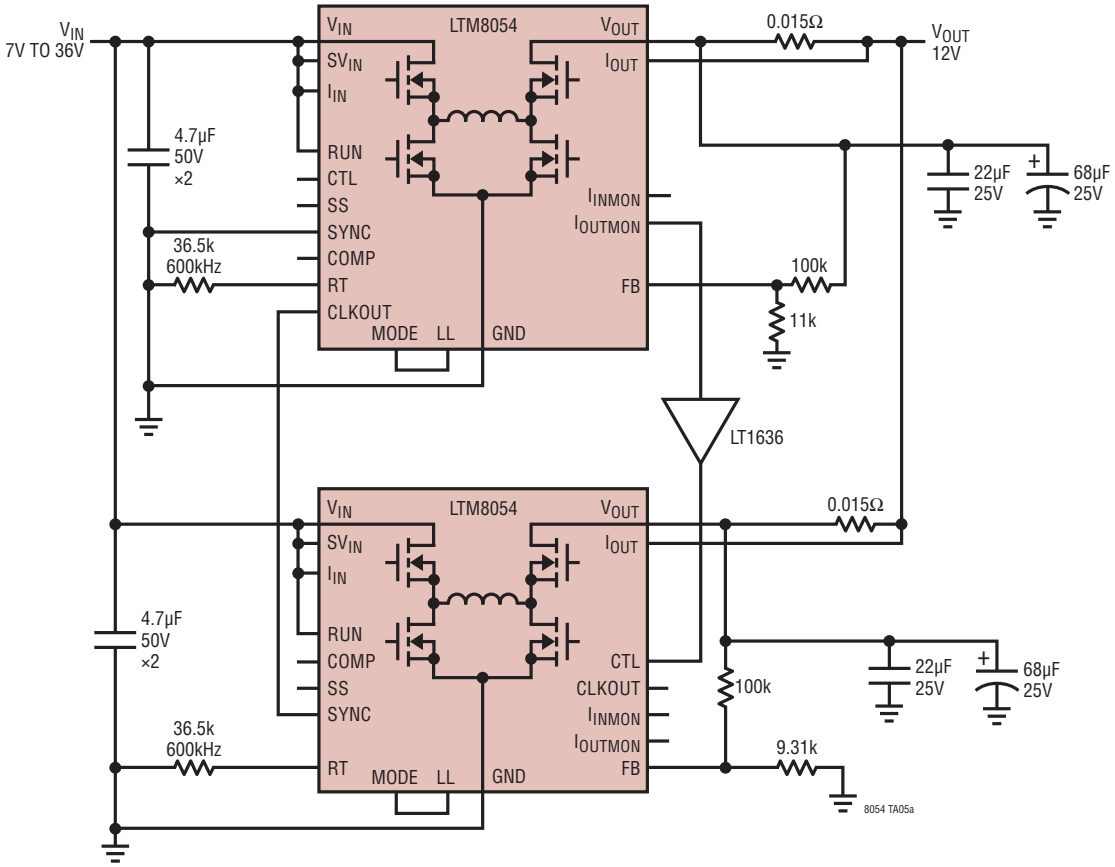


Output Voltage vs Output Current

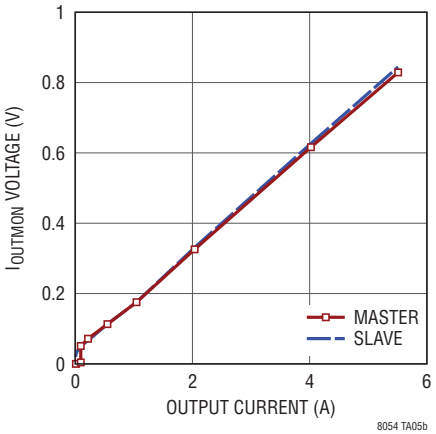


TYPICAL APPLICATIONS

Two LTM8054s Paralleled to Get More Output Current. The Two µModules Are Synchronized and Switching 180° Out Of Phase

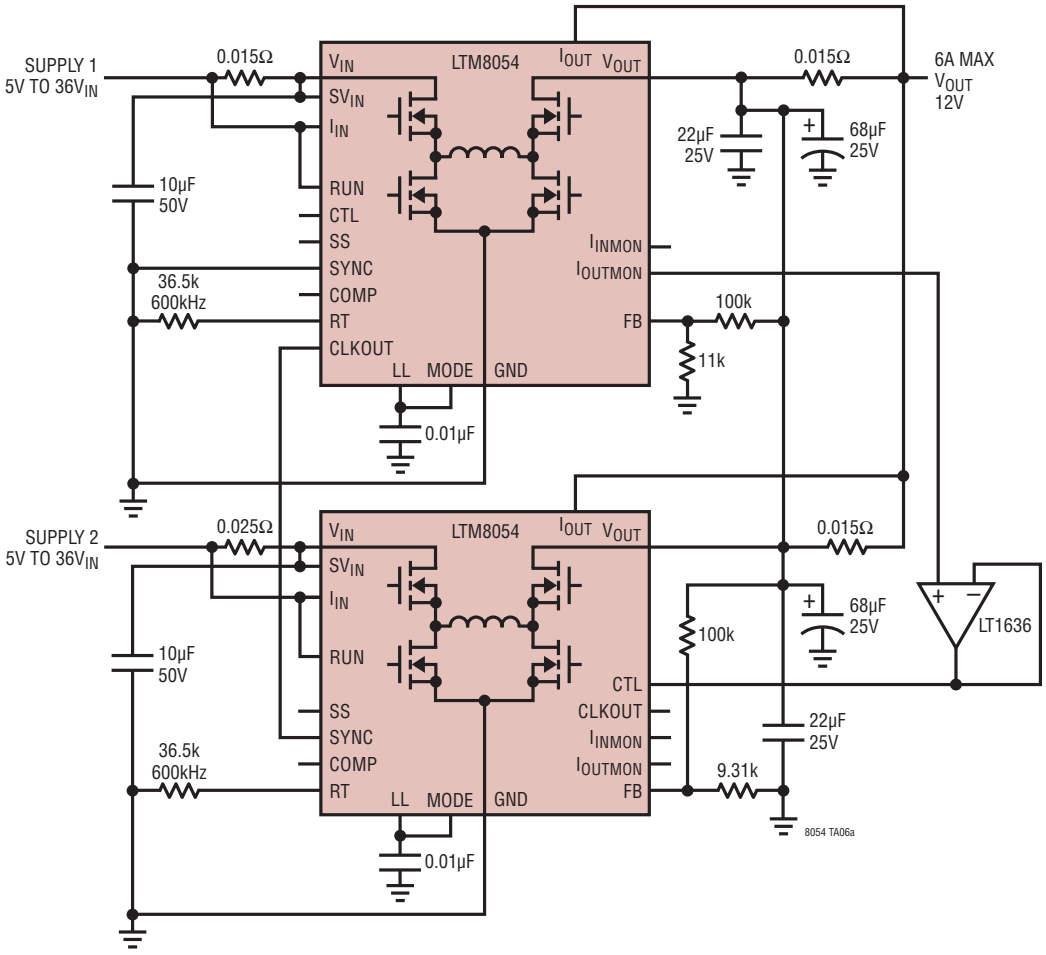


I_{OUTMON} Voltage vs Output Current, 24V_{IN}

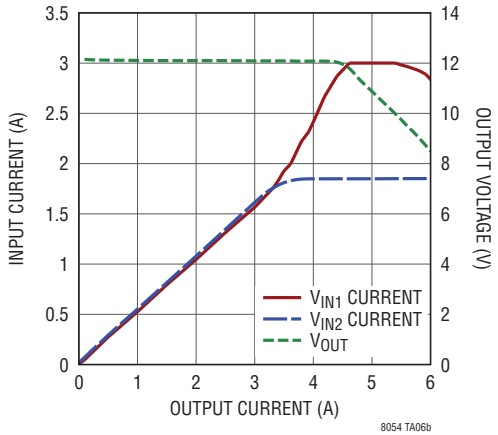


TYPICAL APPLICATIONS

Two LTM8054s Powered from Input Sources with Different Current Capabilities Share Output Current to Run a Single Load. Each LTM8054 Draws No More Than 3.1A and 1.9A from Input Supply 1 and Input Supply 2, Respectively, and Are Synchronized 180° Out Of Phase with Each Other



Input Current and Output Voltage vs Output Current 12V_{IN} for both LTM8054s



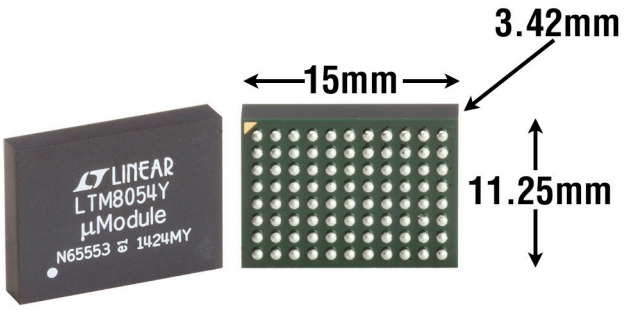
PACKAGE DESCRIPTION

Table 3. LTM8054 Pin Assignment (Arranged by Pin Number)

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT}	B1	V_{OUT}	C1	I_{OUT}	D1	GND	E1	GND	F1	LL
A2	V_{OUT}	B2	V_{OUT}	C2	GND	D2	GND	E2	GND	F2	GND
A3	V_{OUT}	B3	V_{OUT}	C3	GND	D3	GND	E3	GND	F3	GND
A4	V_{OUT}	B4	V_{OUT}	C4	GND	D4	GND	E4	GND	F4	GND
A5	V_{OUT}	B5	V_{OUT}	C5	GND	D5	GND	E5	GND	F5	GND
A6	GND	B6	GND	C6	GND	D6	GND	E6	GND	F6	GND
A7	GND	B7	GND	C7	GND	D7	GND	E7	GND	F7	GND
A8	GND	B8	GND	C8	GND	D8	GND	E8	GND	F8	GND

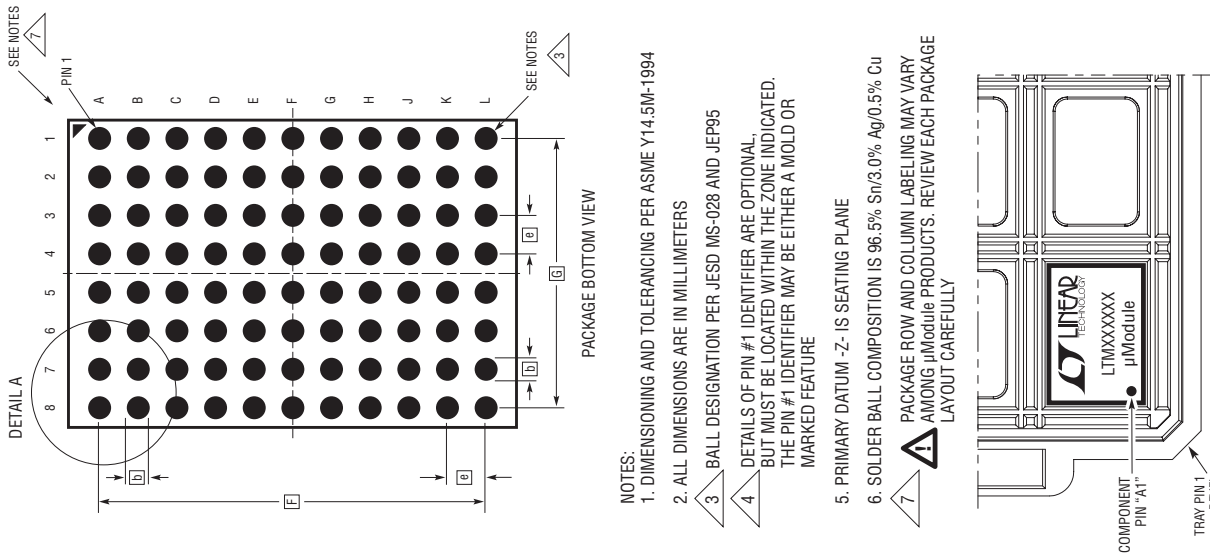
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	CLKOUT	H1	RT	J1	FB	K1	SS	L1	GND
G2	MODE	H2	SYNC	J2	COMP	K2	CTL	L2	I_{OUTMON}
G3	GND	H3	GND	J3	GND	K3	GND	L3	I_{INMON}
G4	GND	H4	GND	J4	GND	K4	GND	L4	RUN
G5	GND	H5	GND	J5	GND	K5	GND	L5	GND
G6	GND	H6	GND	J6	GND	K6	GND	L6	I_{IN}
G7	GND	H7	SV_{IN}	J7	V_{IN}	K7	V_{IN}	L7	V_{IN}
G8	GND	H8	SV_{IN}	J8	V_{IN}	K8	V_{IN}	L8	V_{IN}

PACKAGE PHOTO

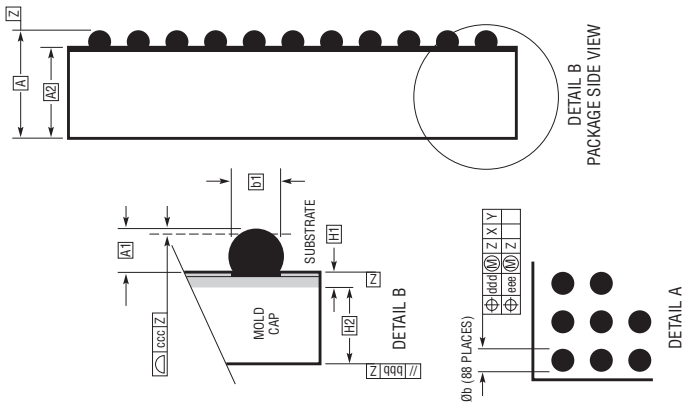


PACKAGE DESCRIPTION

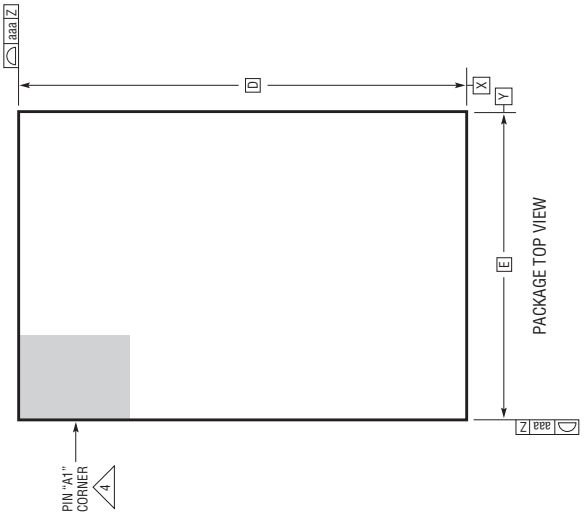
Please refer to http://www.linear.com/product/LTM8054#packaging for the most recent package drawings.

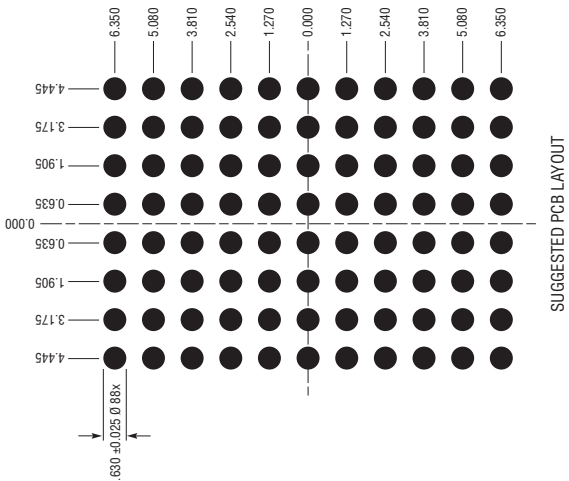


BGA Package
88-Lead (15mm × 11.25mm × 3.42mm)
(Reference LTC DWG # 05-08-1928 Rev B)



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	3.22	3.42	3.62	
A1	0.50	0.60	0.70	
A2	2.72	2.82	2.92	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		15.00		
E		11.25		
e		1.27		
F		12.70		
G		8.89		
H1	0.27	0.32	0.37	
H2	2.45	2.50	2.55	
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	





REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/16	Changed recommended maximum V_{IN} of the Typical Application on Page 22 from 36V to 19V	22