# 20V 1A Buck DC/DC with Integrated SCAP Charger and Backup Regulator

## FEATURES

- **$V_{IN}$ Voltage Range: 3V to 20V**
- **$V_{OUT}$ Voltage Range: 2.7V to 5V**
- **1A Current Mode Buck Main Regulator**
- **5A Boost Backup Regulator Powered from Single Supercapacitor**
- **Boost Regulator Operates Down to 0.5V for Maximum Utilization of Supercapacitor Energy**
- **Programmable Supercapacitor Charge Current to 1A with Overvoltage Protection**
- Charger Supports Single Cell CC/CV Battery Charging
- Programmable $V_{IN}$ Current Limit
- Programmable Boost Current Limit
- $V_{IN}$ Power Fail Indicator
- $V_{CAP}$ Power Good Indicator
- $V_{OUT}$ Power On Reset Output
- Compact 20-Lead 4mm × 4mm QFN Package

## APPLICATIONS

- Ride-Through "Dying Gasp" Supplies
- Power Meters/Industrial Alarms/Solid State Drives

## DESCRIPTION

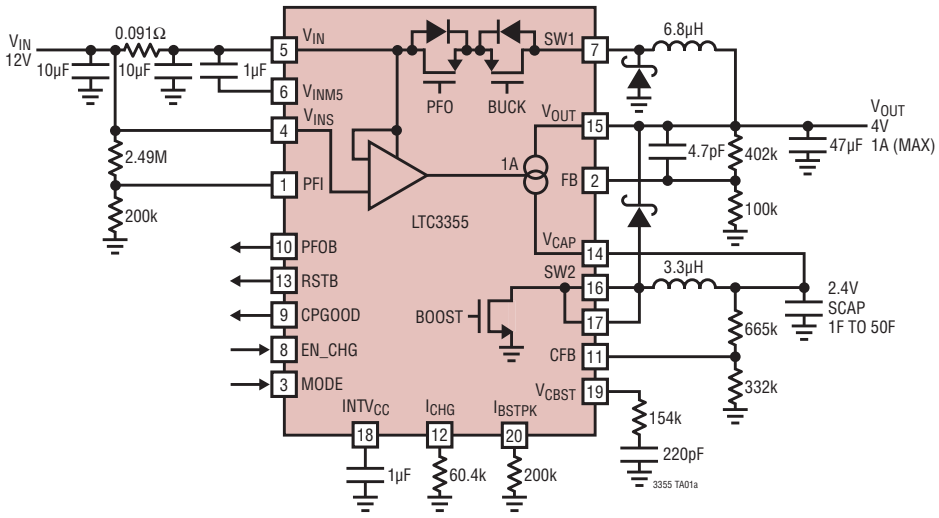
The LTC®3355 is a complete input power interrupt ride-through DC/DC system. The part charges a supercapacitor while delivering load current to $V_{OUT}$, and uses energy from the supercapacitor to provide continuous $V_{OUT}$ backup power when $V_{IN}$ power is lost. The LTC3355 contains a nonsynchronous constant frequency current mode monolithic 1A buck switching regulator to provide a 2.7V to 5V regulated output voltage from an input supply of up to 20V.

A 1A programmable CC/CV linear charger charges the supercapacitor from $V_{OUT}$. When the $V_{IN}$ supply drops below the PFI threshold, the devices's constant frequency nonsynchronous current mode 5A boost switching regulator delivers power from the supercapacitor to $V_{OUT}$. A thermal regulation loop maximizes charge current while limiting the die temperature to 110°C. The IC has boost, charger and $V_{IN}$ programmable current limits. The LTC3355 is available in a 20-lead 4mm × 4mm QFN surface mount package.

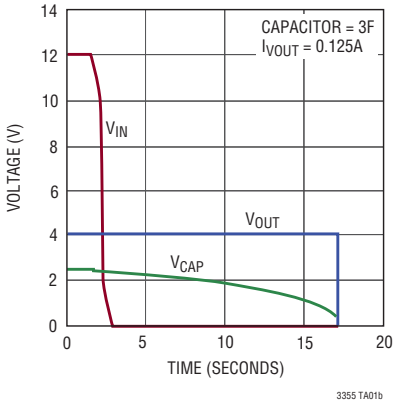


## TYPICAL APPLICATION

**Supercapacitor Charger and Ride-Through Power Supply**




**Backup Operation**

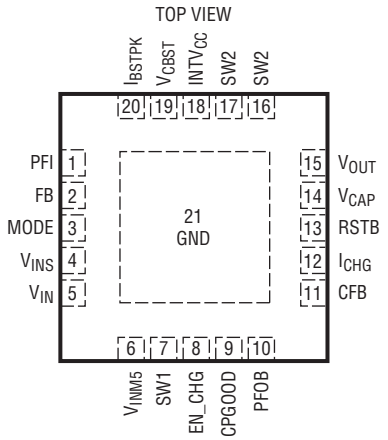


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$V_{IN}$, $V_{INS}$, $V_{INM5}$ .....22V
$V_{IN}$ ±$V_{INS}$..... 0.1V
$V_{SW1}$ ..... –0.4V to 22V
$V_{SW2}$ ..... –0.4V to 6V
$V_{OUT}$, $INTV_{CC}$, PFOB, RSTB,
CPGOOD, $V_{CAP}$..... –0.3V to 6V
PFI, EN_CHG, MODE, FB..... –0.3V to 6V
CFB .....–0.3V to $INTV_{CC}$ + 0.3V
$I_{CPGOOD}$, $I_{PFOB}$, $I_{RSTB}$.....1mA
Operating Junction Temperature Range
(Notes 2, 3)..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

## PIN CONFIGURATION




UF PACKAGE
20-LEAD (4mm × 4mm) PLASTIC QFN

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 47°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC3355EUF#PBF | LTC3355EUF#TRPBF | 3355 | 20-Lead (4mm × 4mm) Plastic QFN | –40°C to 125°C |
| LTC3355IUF#PBF | LTC3355IUF#TRPBF | 3355 | 20-Lead (4mm × 4mm) Plastic QFN | –40°C to 125°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 12V unless otherwise noted. (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | $V_{IN}$ Operating Voltage Range | | ● | 3 | | 20 | V |
| $I_Q$ | $V_{IN}$ Quiescent Current<br>$V_{OUT}$ Quiescent Current | Charger Off, Not Switching, $V_{OUT}$ = 3.3V, No Load, In Regulation, Supercapacitor Charged | ●<br>● | 60<br>110 | 120<br>265 | 215<br>420 | µA<br>µA |
| $V_{FB}$ | FB Reference Voltage | | ● | 0.775 | | 0.825 | V |
| | FB Line Regulation | $V_{OUT}$ = 2.7V to 5V | | | 0.1 | | %/V |
| $I_{FB}$ | FB Input Bias Current | | | –20 | | 20 | nA |
| $V_{VOUT}$ | $V_{OUT}$ Voltage Range | | ● | 2.7 | | 5 | V |
| | $V_{OUT}$ Overvoltage Limit | Buck or Boost Enabled | | 5.4 | 5.65 | 5.95 | V |
| | $V_{OUT}$ Undervoltage Lockout Threshold | Boost Enabled | | 1.8 | 2 | 2.2 | V |
| $V_{INM5}$ | $V_{IN}$-$V_{INM5}$ | $V_{IN}$ > 7V | | | 4.65 | | V |
| $V_{INTVCC}$ | $INTV_{CC}$ Internal Voltage Power Supply | | | 2 | | 5 | V |
| $V_{VCAP}$ | $V_{CAP}$ Voltage Range | | | 0 | | 5 | V |
| $I_{VCAP}$ | $V_{CAP}$ Current Accuracy | $V_{CAP}$ = 2V, $V_{OUT}$ = 3.3V, $I_{VCAP}$ = 1A<br>EN_CHG = High | | –10 | | 10 | % |
| | $V_{CAP}$ Programmable Current Range | EN_CHG = High | | 0.1 | | 1 | A |
| $V_{ICHG}$ | $I_{CHG}$ Reference Voltage | EN_CHG = High | | 0.78 | | 0.82 | V |
| $R_{ICHG}$ | $I_{CHG}$ Set Resistor Range | | | 60.4 | | 604 | kΩ |
| $I_{CFB}$ | CFB Input Bias Current | | | –20 | | 20 | nA |
| $V_{CFB}$ | CFB Reference Voltage | EN_CHG = High | | 0.78 | 0.8 | 0.82 | V |
| | CFB Hysteresis | EN_CHG = High | | | 30 | | mV |
| | CFB Overvoltage Hysteretic Comparator Switch Point | CFB Rising<br>CFB Falling | | | $V_{CFB}$+0.035<br>$V_{CFB}$ | | V<br>V |
| $I_{ICL}$ | $V_{IN}$ Input Current Limit | $V_{INS}$-$V_{IN}$ to Disable Charger<br>$V_{INS}$-$V_{IN}$ to Disable Buck | | 37<br>42 | | 43<br>50 | mV<br>mV |
| $V_{INS(CMI)}$ | $V_{INS}$ Common Mode Range | | | 3.0 | | 20 | V |
| $f_{SW}$ | Switching Frequency | FB ≥ 0.5V | | 0.75 | 1 | 1.25 | MHz |
| | Foldback Frequency (Buck Only) | FB ≤ 0.3V | | | 100 | | kHz |
| $V_{PFI}$ | PFI Falling Threshold | | ● | 0.775 | 0.8 | 0.825 | V |
| | PFI Hysteresis | | | | 17 | | mV |
| $I_{PFI}$ | PFI Leakage Current | | | –20 | | 20 | nA |
| **1A Buck Regulator** | | | | | | | |
| $I_{SW1}$ | SW1 Peak Current | PWM Mode (Note 5)<br>Burst Mode® (Note 5) | | 1.3 | 1.65<br>0.5 | 2 | A<br>A |
| $t_{SS}$ | Soft-Start Time | | | | 1000 | | µs |
| DC Max | Maximum Duty Cycle | FB = 0V | | 100 | | | % |
| $R_{PMOS}$ | PMOS On-Resistance | | | | 0.5 | 1 | Ω |
| $I_{LEAKP}$ | PMOS Leakage Current | Buck Disabled | | –2 | | 2 | µA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 12V unless otherwise noted. (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **5A Boost Regulator** | | | | | | | |
| $I_{VOUT}$ | $V_{OUT}$ Quiescent Current | $V_{OUT}$ = 3.3V, No Load, In Regulation, No Switching, Burst Mode | ● | 80 | 160 | 280 | µA |
| $I_{SW2}$ | SW2 Peak Current | $R_{IBSTPK}$ = 200k, PWM Mode<br>$R_{IBSTPK}$ = 200k, Burst Mode | | 4.5 | 5<br>1.5 | 5.5 | A<br>A |
| $R_{NMOS}$ | NMOS On-Resistance | | | | 70 | | mΩ |
| $I_{LEAKN}$ | NMOS Leakage Current | Boost Disabled | | –5 | | 5 | µA |
| DC Max | Boost Maximum Duty Cycle | | | 88 | 92 | 98 | % |
| $V_{SBOOST}$ | Boost Input Supply Voltage Range | | | 0.75 | | 5 | V |
| | Boost Minimum Input Supply | $V_{OUT(MAX)}$ = 4V | | 0.5 | | | V |
| $A_V$ | Boost Error Amplifier Voltage Gain | (Note 5) | | | 850 | | V/V |
| $g_m$ | Boost Error Amplifier Transconductance | | | | 27 | | µS |
| $V_{IBSTPK}$ | $I_{BSTPK}$ Reference Voltage | | | 0.775 | | 0.825 | V |
| $R_{IBSTPK}$ | $I_{BSTPK}$ Set Resistor Range | | | 200 | | 1000 | kΩ |
| **Logic (MODE, EN_CHG, CPGOOD, RSTB, PFOB)** | | | | | | | |
| $V_{IL}$ | Input Low Logic Voltage | MODE, EN_CHG | | | | 0.4 | V |
| $V_{IH}$ | Input High Logic Voltage | MODE, EN_CHG | | 1.2 | | | V |
| $I_{IL}$, $I_{IH}$ | Input Low/High Current | MODE, EN_CHG | | -1 | | 1 | µA |
| $V_{OL}$ | Output Logic Low Voltage | PFOB, CPGOOD, RSTB; Sink 100µA | | | | 50 | mV |
| $I_{OH}$ | Logic High Leakage Current | PFOB, CPGOOD, RSTB; 5V | | | | 1 | µA |
| | CPGOOD Rising Threshold | $V_{CAP}$ as a % of Final Target | | 90 | 92.5 | 95 | % |
| | CPGOOD Hysteresis | $\Delta V_{CAP}$ as a % of Final Value | | | 2.5 | | % |
| | RSTB Falling Threshold | $V_{OUT}$ as a % of Final Target | | 90 | 92.5 | 95 | % |
| | RSTB Hysteresis | $\Delta V_{OUT}$ as a % of Final Value | | | 2.5 | | % |
| | RSTB Delay | | | | 250 | | ms |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3355 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3355E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3355I is guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature ($T_J$, in °C) is calculated from the ambient temperature ($T_A$, in °C) and power dissipation ($P_D$, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where $\theta_{JA}$ = 47°C/W for the UF package.

**Note 3:** The LTC3355 has a thermal regulation loop that limits the maximum junction temperature to 110°C by limiting the charger current.

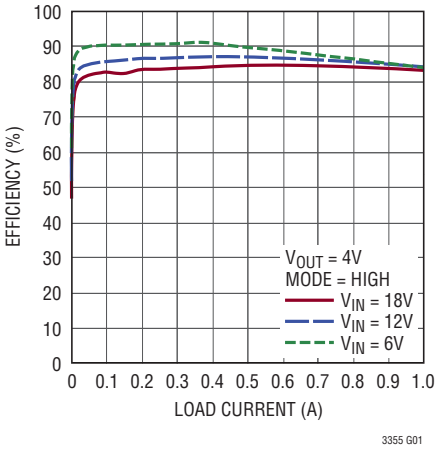
**Note 4:** The current limit features of this part are intended to protect the IC from short-term or intermittent fault conditions. Continuous operation above the maximum specified pin current may result in device degradation or failure.

**Note 5:** Guaranteed by design and/or correlation to static test.

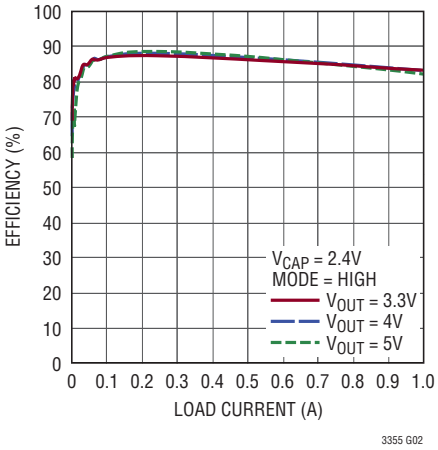
**Note 6:** The LTC3355 has a thermal shutdown that will shut down the part when the die temperature reaches 155°C.

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C unless otherwise noted

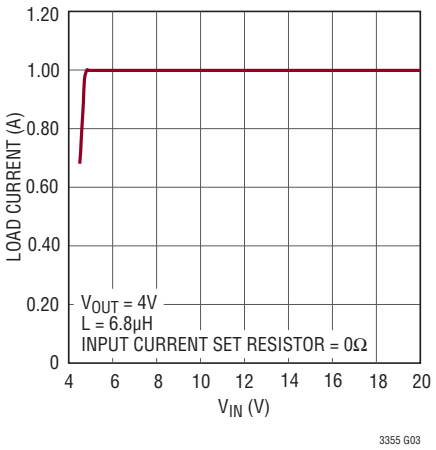
### Buck Efficiency



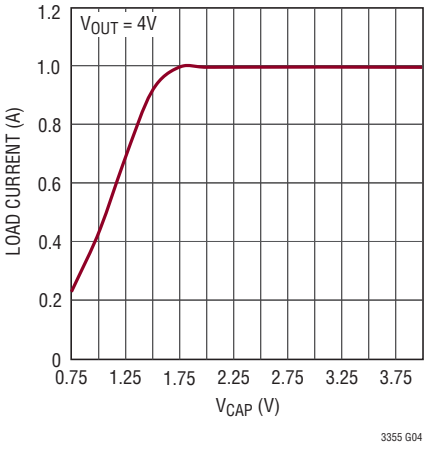

### Boost Efficiency



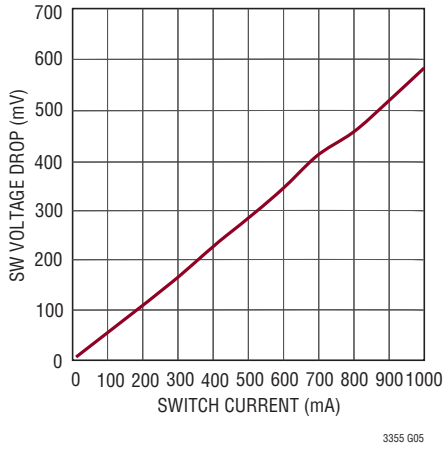

### Maximum Buck Load Current



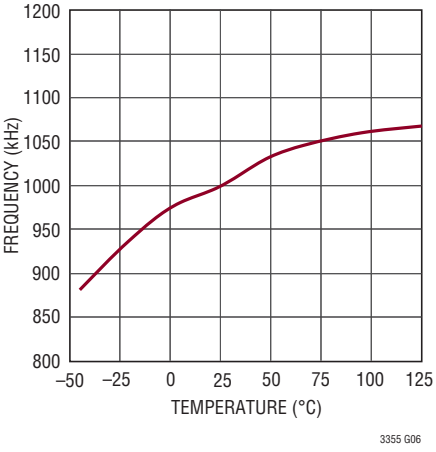

### Maximum Boost Load Current



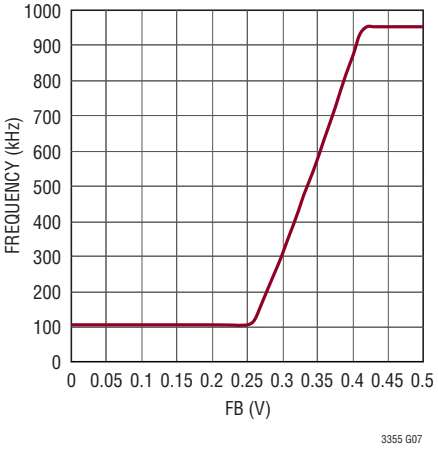

### Buck Switch Voltage Drop



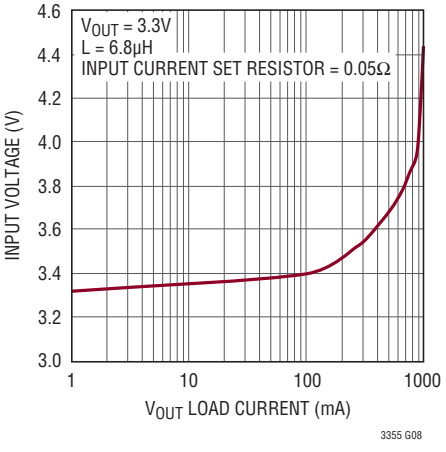

### Oscillator Frequency vs Temperature



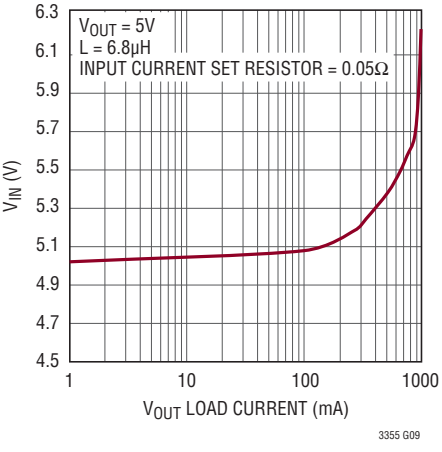

### Buck Frequency vs Feedback Voltage




### Typical Minimum Buck Input Voltage ($V_{OUT}$ = 3.3V)

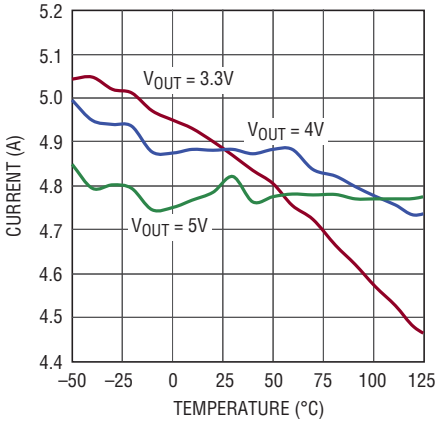



### Typical Minimum Buck Input Voltage ($V_{OUT}$ = 5V)



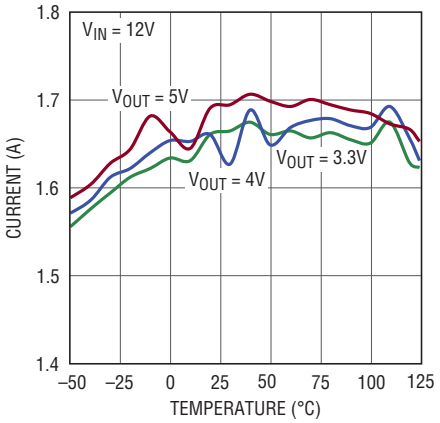
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C unless otherwise noted

### Boost Switch Current Limit vs Temperature



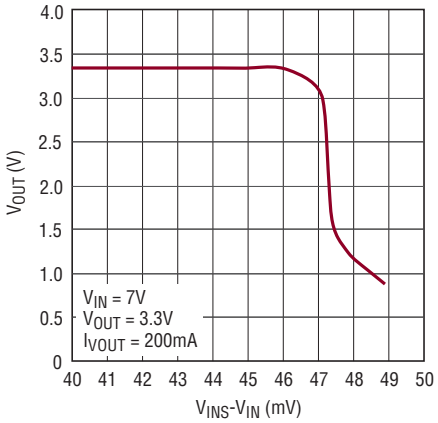

3355 G10

### Buck Switch Current Limit vs Temperature



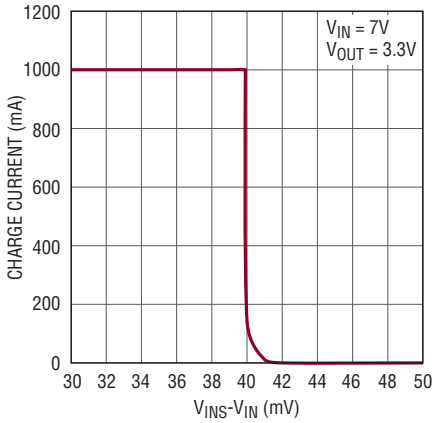

3355 G11

### VOUT vs VINS-VIN



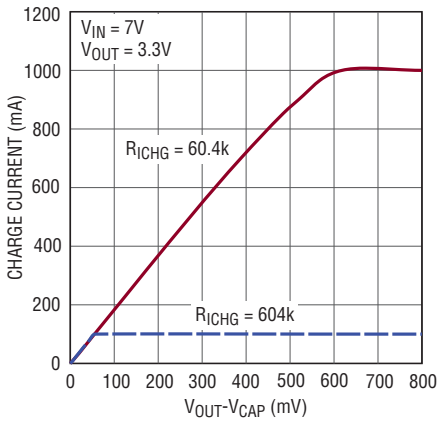

3355 G12

### Charge Current vs VINS-VIN



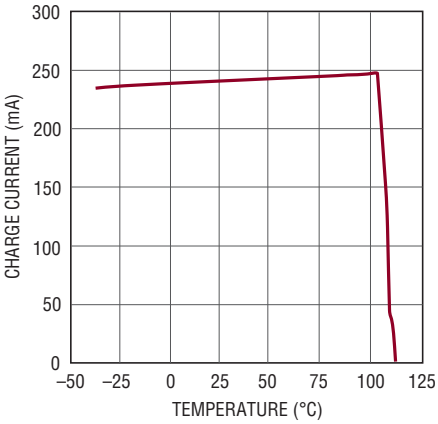

3355 G13

### Charge Current vs VOUT-VCAP



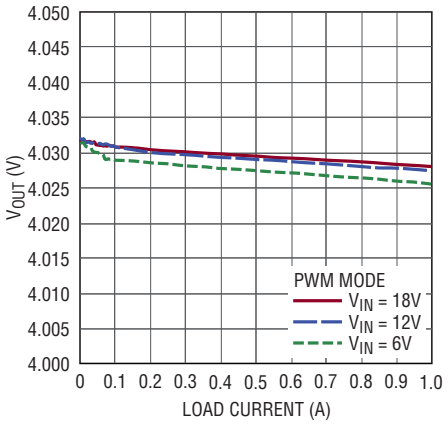

3355 G14

### Charge Current vs Junction Temperature



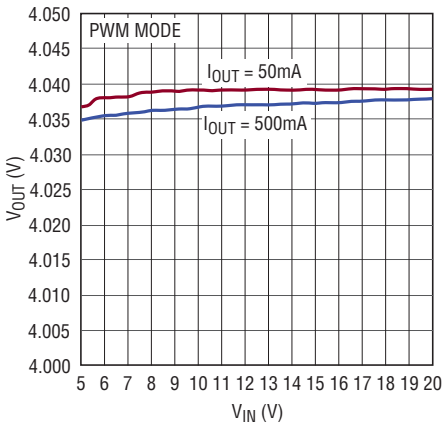

3355 G15

### Buck Load Regulation



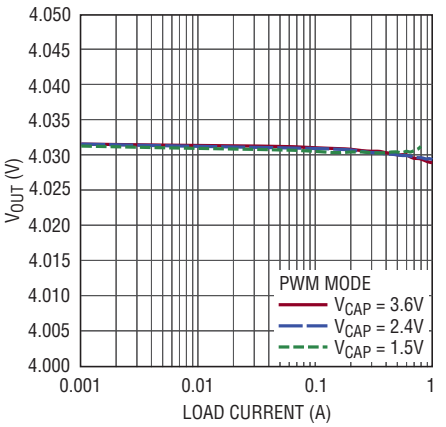

3355 G16

### Buck Line Regulation




3355 G17

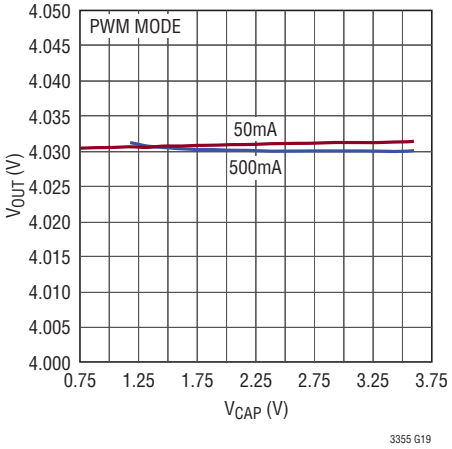
### Boost Load Regulation



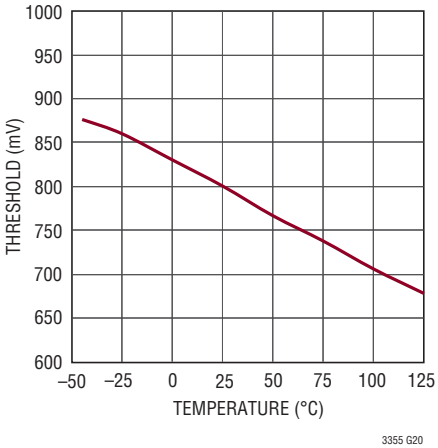

3355 G18

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C unless otherwise noted

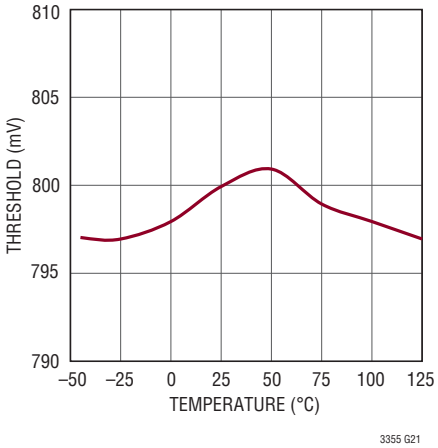
### Boost Line Regulation



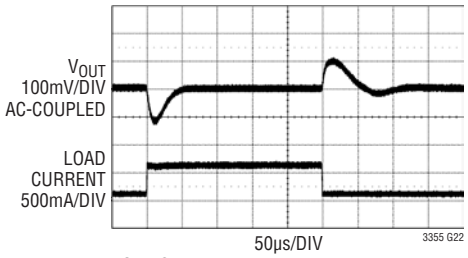

### Logic Input Threshold vs Temperature (EN_CHG, MODE)




### PFI Threshold vs Temperature

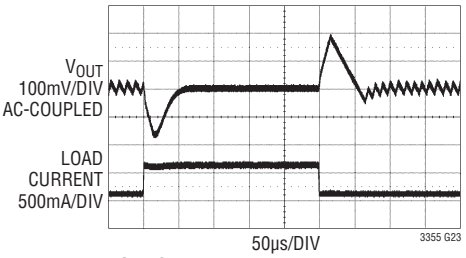



### Buck Load Step PWM




LOAD STEP = 100mA to 600mA
$V_{IN}$ = 12V
$V_{OUT}$ = 4V

### Buck Load Step Burst Mode Operation




LOAD STEP = 100mA to 600mA
$V_{IN}$ = 12V
$V_{OUT}$ = 4V

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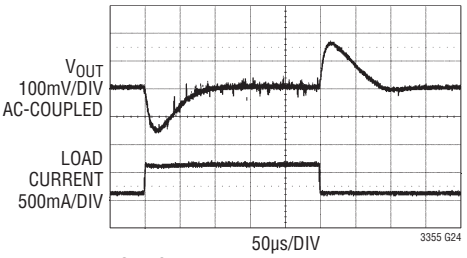
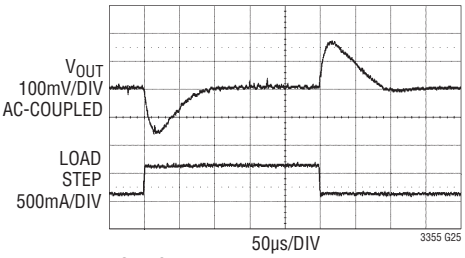


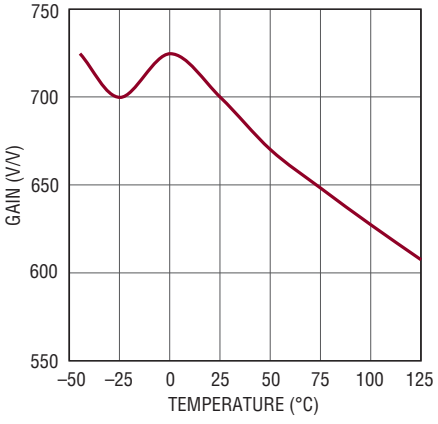

LOAD STEP = 100mA to 600mA
$V_{CAP}$ = 2.4V
$V_{OUT}$ = 4V

### Boost Load Step Burst Mode Operation

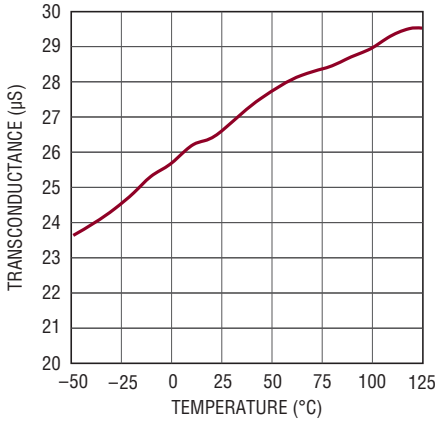



LOAD STEP = 100mA to 600mA
$V_{CAP}$ = 2.4V
$V_{OUT}$ = 4V

### Boost Error Amplifier Voltage Gain vs Temperature




### Boost Error Amplifier Transconductance vs Temperature



## PIN FUNCTIONS

**PFI (Pin 1):** Input to the Power-Fail Comparator. The input voltage below which the PFOB pin indicates a power-fail condition can be programmed by connecting this pin to an external resistor divider between $V_{IN}$ and ground.

**FB (Pin 2):** Sets the $V_{OUT}$ voltage for both the buck and boost voltage control loops via an external resistor divider. The reference voltage is 0.8V.

**MODE (Pin 3):** This pin sets the buck and boost switching modes. A low is PWM mode, a high is Burst Mode operation.

**$V_{INS}$ (Pin 4):** Input Current Limit Sense Voltage Pin. Connect a sense resistor from $V_{INS}$ to $V_{IN}$. Must be locally bypassed with a low ESR ceramic capacitor. Connect to $V_{IN}$ if input current limit is not needed.

**$V_{IN}$ (Pin 5):** Input Power Pin Supplies Current to the Internal Regulator and Buck Power Switch. Must be locally bypassed with a low ESR ceramic capacitor.

**$V_{INM5}$ (Pin 6):** This pin is used to filter an internal supply regulator which generates a voltage of $V_{IN}$ – 4.65V. Connect a 1µF ceramic capacitor from $V_{INM5}$ to $V_{IN}$.

**SW1 (Pin 7):** Buck Output of the Internal Power Switch. Connect this pin to the catch diode and inductor. Minimize trace area at this pin to reduce EMI.

**EN_CHG (Pin 8):** A high on this pin enables the supercapacitor charger.

**CPGOOD (Pin 9):** Open-drain output is high impedance when the $V_{CAP}$ voltage is higher than 92.5% of the programmed voltage.

**PFOB (Pin 10):** Open Drain of the Power-Fail Comparator. Pulled low and enables the boost converter when the PFI input has determined that the input supply has dropped out.

**CFB (Pin 11):** This pin is used to program the $V_{CAP}$ voltage via an external resistor divider. The reference voltage is 0.8V.

**$I_{CHG}$ (Pin 12):** This pin programs the $V_{CAP}$ charge current by connecting a resistor to ground.

**RSTB (Pin 13):** Open-drain reset output is high impedance when the $V_{OUT}$ voltage is higher than 92.5% of the programmed regulation voltage.

**$V_{CAP}$ (Pin 14):** This pin is the constant current, constant voltage linear charger output and connects to the supercapacitor.

**$V_{OUT}$ (Pin 15):** The Output Voltage Supply. The buck powers this supply from $V_{IN}$ when the input voltage is present and the boost powers this supply from $V_{CAP}$ when the input voltage has dropped out.

**SW2 (Pin 16, 17):** Boost Output of the Internal Power Switch. Connect these pins to the rectifier diode and inductor. Minimize trace area at these pins to reduce EMI.

**$INTV_{CC}$ (Pin 18):** This pin is used to filter an internal supply. Connect a 1µF ceramic capacitor from this pin to ground. $INTV_{CC}$ is 2.5V during start-up until $V_{OUT}$ exceeds 2.5V then $INTV_{CC}$ follows $V_{OUT}$.

**$V_{CBST}$ (Pin 19):** This pin is the output of the boost internal error amplifier. The voltage on this pin controls the peak switch current for the boost regulator. Connect an RC series network from this pin to ground to compensate the boost control loop.

**$I_{BSTPK}$ (Pin 20):** This pin programs the boost peak current limit by connecting a resistor to ground.

**GND (Exposed Pad Pin 21):** Ground. The exposed pad must be connected to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the part to achieve optimum thermal conduction.

# SIMPLIFIED BLOCK DIAGRAM

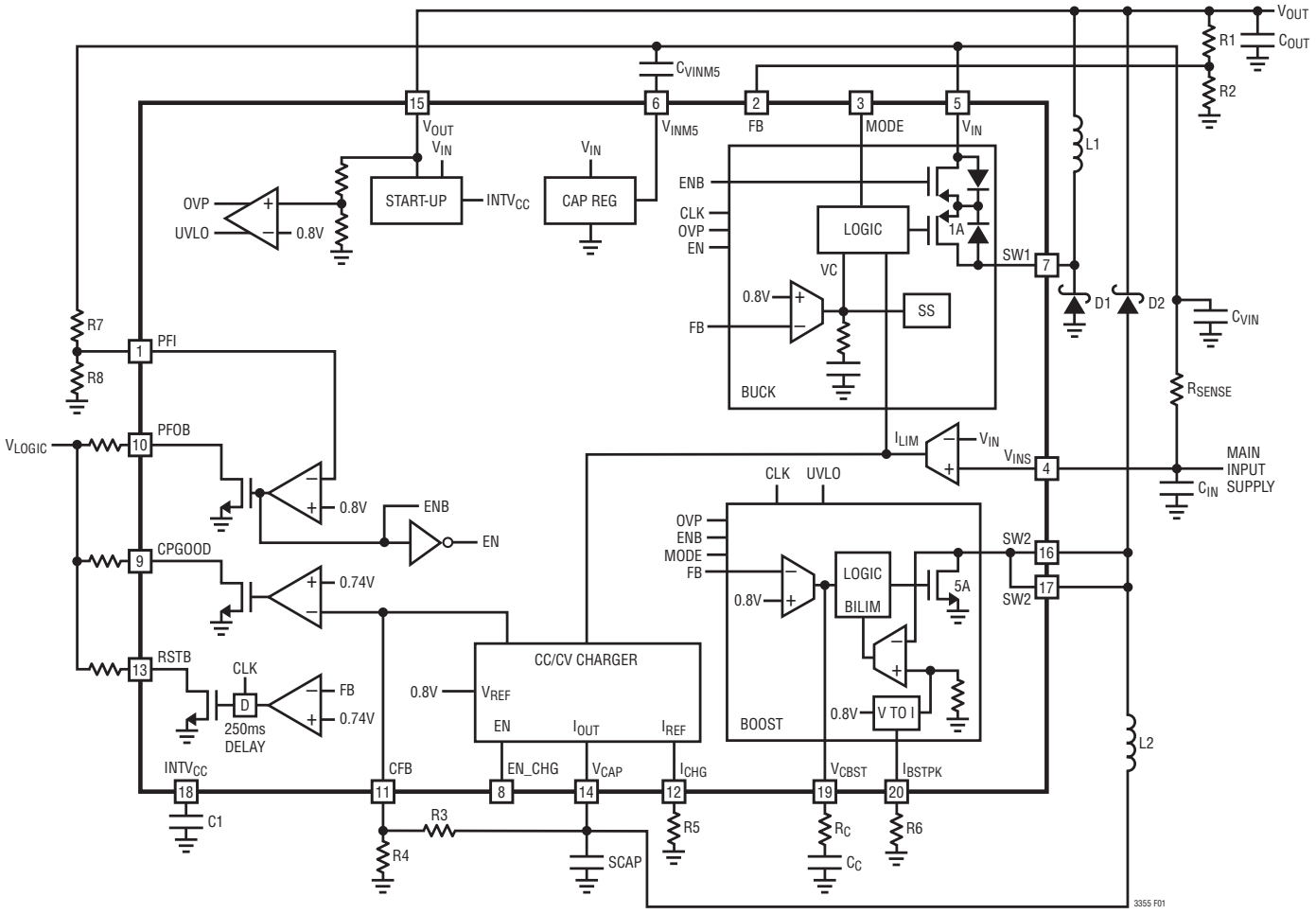



**Figure 1. LTC3355 Block Diagram**

## OPERATION

The LTC3355 is a 1A buck regulator with a built-in backup boost converter to allow temporary backup, or ride-through, of $V_{OUT}$ during a sudden loss of $V_{IN}$ power. The device contains all functions necessary to provide seamless charging of a supercapacitor (or other storage element), monitoring of $V_{IN}$, $V_{OUT}$ and $V_{CAP}$, and automatic switch-over to backup power. When the buck is disabled an internal circuit blocks reverse current between $V_{OUT}$ and $V_{IN}$.

### Start-Up

When the part first starts up the only voltage available is $V_{IN}$ since $V_{OUT}$ and $V_{CAP}$ are at zero volts. An internal 2.5V regulator powers $INTV_{CC}$ from $V_{IN}$ during start-up. $INTV_{CC}$ powers all of the low voltage circuits. The buck regulator is enabled and will drive $V_{OUT}$ positive through an inductor until the feedback voltage at FB equals 0.8V. When $V_{OUT}$ exceeds 2.5V $INTV_{CC}$ will exactly track $V_{OUT}$ and the current for the internal low voltage circuits will now be supplied from $V_{OUT}$ instead of $V_{IN}$. A 1µF external ceramic capacitor is required for $INTV_{CC}$ to filter internal switching noise.

### Buck Switching Regulator

The LTC3355 uses a 1MHz constant frequency peak current mode nonsynchronous monolithic buck regulator with internal slope compensation to control the voltage at $V_{OUT}$ when $V_{IN}$ is available. An error amplifier compares the divided output voltage at FB with a reference voltage of 0.8V and adjusts the peak inductor current accordingly. Burst Mode operation can also be selected to optimize efficiency at low load currents via the MODE pin. The buck is in PWM mode when the MODE pin is low and in Burst Mode operation when the MODE pin is high. The buck is internally compensated and can operate over an input voltage range of 3V to 20V. An internal soft-start ramp limits inrush current during start-up. Frequency foldback protection helps to prevent inductor current runaway during start-up or short-circuit conditions.

### Input Current Limit

The (optional) input current limit is programmed via an external sense resistor connected between $V_{INS}$ and $V_{IN}$. As the input current limit is reached the charge current will be reduced. If the charge current has been reduced to zero and the input current continues to increase the buck regulator current drive capability will be reduced. The maximum sense voltage is 50mV. The input current limit includes the LTC3355 quiescent current for high accuracy over a wide current range.

### Boost Switching Regulator

When $V_{IN}$ is not available, a monolithic 1MHz constant frequency peak current mode boost regulator with internal slope compensation is enabled and the buck regulator is disabled via the PFI pin. The boost regulator uses the voltage stored at $V_{CAP}$ as an input supply and regulates the $V_{OUT}$ voltage. An error amplifier compares the divided output voltage at FB with a reference voltage of 0.8V and adjusts the peak inductor current accordingly. The $I_{BSTPK}$ pin sets the peak boost current over a range of 1A to 5A allowing for lower current backup applications. The boost switching regulator is compensated by adding a series RC network from the $V_{CBST}$ pin to ground. The boost regulator can operate over an input voltage range ($V_{CAP}$) of 0.5V to 5V. The boost regulator uses the same feedback pin and error amplifier as the buck and regulates to the same $V_{OUT}$ voltage. The MODE pin is used to control the boost switching regulator mode. The boost is in PWM mode when the MODE pin is low and in Burst Mode operation when the MODE pin is high. In PWM mode as the load current is decreased, the switch turns on for a shorter period each cycle. If the load current is further decreased, the boost converter will skip cycles to maintain output voltage regulation.

### Charger

The supercapacitor is charged by an internal 1A constant current/constant voltage linear charger that supplies current from $V_{OUT}$ to $V_{CAP}$. The charger will be enabled when $V_{IN}$ is above a programmable voltage via the PFI pin, when the EN_CHG pin is high and when $V_{OUT}$ is in regulation. The value of the resistor on the $I_{CHG}$ pin determines the charger current. An internal amplifier servos the $I_{CHG}$ voltage to 0.8V to create the reference current for the charge. The $V_{CAP}$ voltage is divided down by an external resistor divider that is connected to the CFB pin. A hysteretic comparator compares the CFB voltage to a

## OPERATION

0.8V reference voltage and turns the charger off when these voltages are the same. The $V_{CAP}$ voltage represents the fully charged supercapacitor voltage available to supply the boost regulator when $V_{IN}$ has dropped out. When CFB decays to 30mV below the CFB reference voltage the charger will be turned on. The LTC3355 includes a soft-start circuit to minimize the inrush current at the start of charge. When the charger is enabled, the charge current ramps from zero to full-scale over a period of approximately 1ms. This has the effect of minimizing the transient load current on $V_{OUT}$.

The $V_{CAP}$ output also has an overvoltage protection circuit which monitors the CFB voltage. If the CFB voltage increases above the CFB reference voltage by 35mV a hysteretic comparator switches in an 8k resistor from $V_{CAP}$ to ground. This will bleed any excess charge from the supercapacitor. When the CFB voltage decays to the CFB reference voltage the comparator will remove the 8k bleed resistor. Excess charge can come from leakage currents associated with the boost rectifier diode.

### $V_{IN}$ Status Monitor

The PFI input always monitors the $V_{IN}$ voltage and determines when $V_{IN}$ is in dropout. $V_{IN}$ is divided down by an external resistor divider and this voltage is then compared to a reference voltage of 0.8V. If the PFI voltage is below the reference voltage the buck regulator and the charger will be disabled and the boost regulator will be enabled. The PFOB pin is a 5V open-drain output. This pin is driven internally by the PFI comparator. When the PFI comparator determines that $V_{IN}$ has dropped out the PFOB output switches low. PFOB is normally connected to a low voltage supply, via an external pull-up resistor. The pull-up resistor for this output can be connected to $V_{OUT}$ if another supply is not available.

### $V_{OUT}$ Status Monitor

The RSTB pin is a 5V open-drain output. An internal comparator determines when $V_{OUT}$ has reached 92.5% of the programmed regulation voltage which then switches the RSTB pin high. RSTB is normally connected to a low voltage supply ($V_{OUT}$) via an external pull-up resistor.

### $V_{CAP}$ Status Monitor

The CPGOOD pin is a 5V open-drain output. An internal comparator determines when $V_{CAP}$ has reached 92.5% of the programmed regulation voltage which then switches the CPGOOD pin high. CPGOOD is normally connected to a low voltage supply ($V_{OUT}$) via an external pull-up resistor.

### Thermal Regulation

As the die temperature increases due to internal power dissipation, a thermal regulator will limit the die temperature to 110°C by reducing the charger current. The thermal regulation protects the LTC3355 from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without the risk of damaging the LTC3355. Another feature is that the charge current can be set according to typical, rather than worst-case ambient temperatures for a given application with the assurance that the charger will automatically reduce the charge current in worst-case conditions.

### Thermal Shutdown

The LTC3355 includes a thermal shutdown circuit in addition to the thermal regulator. If for any reason, the die temperature exceeds 155°C, the entire part shuts down. The part will resume normal operation once the temperature drops about 15°C, to approximately 140°C.

### $V_{OUT}$ Overvoltage, Undervoltage Lockout

The LTC3355 includes an overvoltage protection circuit to ensure that $V_{OUT}$ does not exceed 5.65V (nominal). An internal resistor divider from $V_{OUT}$ is connected to an amplifier that will regulate $V_{OUT}$ as the overvoltage limit is reached. The LTC3355 includes undervoltage lockout which disables the boost when $V_{OUT}$ is < 2V typical.

## APPLICATIONS INFORMATION

### FB Resistor Network

The $V_{OUT}$ voltage is programmed with a resistor divider between the $V_{OUT}$ pin and the FB pin. Choose the resistor values according to:

$$R1 = R2\left(\frac{V_{OUT}}{0.8V} - 1\right)$$

Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy.

### CFB Resistor Network

The $V_{CAP}$ voltage is programmed with a resistor divider between the $V_{CAP}$ pin and the CFB pin. Choose the resistor values according to:

$$R3 = R4\left(\frac{V_{CAP}}{0.8V} - 1\right)$$

Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain the capacitor float voltage accuracy.

### $I_{CHG}$ Set Resistor

The charge current at $V_{CAP}$ is set by connecting a resistor from $I_{CHG}$ to ground. Choose the resistor value according to:

$$\text{Charger Current (Amps)} = \frac{60400}{R5}$$

Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain charge current accuracy.

### $I_{BSTPK}$ Set Resistor

The boost peak current limit is set by connecting a resistor from $I_{BSTPK}$ to ground. Choose the resistor value according to:

$$\text{Boost Peak Current Limit (Amps)} = \frac{1E6}{R6}$$

Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain boost peak current accuracy.

### PFI Resistor Network

The $V_{IN}$ dropout voltage is programmed with a resistor divider between the $V_{IN}$ pin and PFI pin. Choose the resistor values according to:

$$R7 = R8\left(\frac{V_{IN}}{0.8V} - 1\right)$$

Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain the PFI threshold voltage accuracy.

The $V_{IN}$ voltage must be greater than the buck dropout voltage (100% duty cycle) when the PFI level is reached to ensure that $V_{OUT}$ stays in regulation.

### Input Voltage Range

The minimum input voltage is determined by the dropout of the buck regulator. The dropout is dependent on the maximum load current and the buck internal switch resistance. The minimum input voltage due to buck dropout is:

$$V_{IN(MIN)} = V_{OUT} + (I_{SW(PEAK)} \bullet 1\Omega)$$

## APPLICATIONS INFORMATION

### Buck Inductor L1 Selection and Maximum Output Current

A good starting point for the inductor value is:

$$L = (V_{OUT} + V_D) \bullet \frac{1.8}{f_{SW}}$$

where $f_{SW}$ is the switching frequency in MHz, $V_{OUT}$ is the buck output voltage, $V_D$ is the catch diode drop (~0.5V) and L is the inductor value in µH.

The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be 30% higher. To keep the efficiency high, the series resistance (DCR) should be less than 0.1Ω, and the core material should be intended for high frequency applications. Table 1 lists several inductor vendors.

For robust operation and fault conditions (start-up or short-circuit) and high input voltage (>15V), the saturation current should be chosen high enough to ensure that the inductor peak current does not exceed 2.2A.

The current in the inductor is a triangle wave with an average value equal to the load current. The peak inductor and switch current is:

$$I_{SW(PEAK)} = I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

where $I_{L(PEAK)}$ is the peak inductor current, $I_{OUT(MAX)}$ is the maximum output load current and $\Delta I_L$ is the inductor ripple current. The LTC3355 limits the switch current in order to protect the part. Therefore, the maximum output current that the buck will deliver depends on the switch current limit, the inductor value, the input and output voltages.

When the switch is off, the potential across the inductor is the output voltage plus the catch diode drop. This gives the peak-to-peak ripple current in the inductor:

$$\Delta I_L = (1 - DC) \bullet \frac{V_{OUT} + V_D}{L \bullet f_{SW}}$$

where $f_{SW}$ is the switching frequency of the buck, DC is the duty cycle and L is the value of the inductor.

To maintain output regulation, the inductor peak current must be less than the buck switch current limit. The maximum output current is:

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2}$$

Choosing an inductor value so that the ripple current is small will allow a maximum output current near the switch current limit.

**Table 1. Inductor Vendors**

| VENDOR | URL | PART SERIES | TYPE |
|---|---|---|---|
| Murata | www.murata.com | LQH5BPB | Shielded |
| TDK | www.tdk.com | LTF5022T | Shielded |
| Toko | www.toko.com | FDS50xx | Shielded |
| Coilcraft | www.coilcraft.com | XAL40xx, LPS40xx | Shielded |
| Sumida | www.sumida.com | DCRH5D, CDRH6D | Shielded |
| Viashay | www.vishay.com | IHLP2020 | Shielded |

One approach to choosing the inductor is to start with the simple rule above, look at the available inductors, and choose one to meet cost or space goals. Then use the equations to check that the buck will be able to deliver the required output current. These equations assume that the inductor current is continuous. Discontinuous operation occurs when $I_{OUT}$ is less than $\Delta I_L/2$.

## APPLICATIONS INFORMATION

### Buck Input Capacitor

Bypass $V_{IN}$ and $V_{INS}$ with a ceramic capacitor of X7R or X5R type. A 10µF to 22µF ceramic capacitor is adequate for bypassing. Note that a larger $V_{INS}$ bypass capacitor may be required if the input power supply source impedance is high or there is significant inductance due to long wires or cables. This can be provided with a lower performance electrolytic capacitor in parallel with the ceramic capacitor.

Buck regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitors are required to reduce the resulting voltage ripple at $V_{INS}$ and $V_{IN}$ and to force this very high frequency switching into a tight local loop, minimizing EMI. The capacitors must be placed close to the LTC3355 pins.

### Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the buck regulator to produce the DC output. In this role it determines the output ripple, and low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the buck regulator control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. A good starting value is:

$$C_{OUT} = f_{SW}\left(\frac{100}{V_{OUT}}\right)$$

where $f_{SW}$ is in MHz and $C_{OUT}$ is the recommended output capacitance in µF. Use X5R or X7R types. This choice will provide low output ripple and good transient response.

When choosing a capacitor look carefully through the data sheet to find out what the actual capacitance is under operating conditions (applied voltage and temperature). A physically larger capacitor, or one with a higher voltage rating, may be required. High performance tantalum or electrolytic capacitors can be used for the output capacitor.

Low ESR is important, so choose one that is intended for use in switching regulators. The ESR should be specified by the supplier, and should be 0.05Ω or less. Table 2 lists several capacitor vendors.

**Table 2. Capacitor Vendors**

| VENDOR | URL | PART SERIES | COMMANDS |
|---|---|---|---|
| Panasonic | www.panasonic.com | Ceramic, Polymer, Tantalum | EEF Series, POSCAP |
| Kemet | www.kemet.com | Ceramic, Tantalum | T494, T495 |
| Murata | www.murata.com | Ceramic | |
| AVX | www.avxcorp.com | Ceramic, Tantalum | TPS Series |
| Taiyo Yuden | www.taiyo-yuden.com | Ceramic | |

### Buck Catch Diode Selection

The catch diode (D1 in the Block Diagram) conducts current only during the switch-off time. The average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = I_{OUT}(1 - DC)$$

where DC is the duty cycle. The only reason to consider a diode with a larger current rating than necessary for nominal operation is for the case of shorted or overloaded output conditions. For the worst case of shorted output the diode average current will then increase to a value that depends on the switch current limit.

If operating at high temperatures select a Schottky diode with low reverse leakage current.

## APPLICATIONS INFORMATION

### Audible Noise

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can sometimes cause problems when used with switching regulators. Both the buck and boost can run in Burst Mode operation and the switching frequency will depend on the load current which at very light loads can excite the ceramic capacitors at audio frequencies, generating audible noise. Since the buck and boost operate at lower current limits in Burst Mode operation, the noise is typically very quiet. Use a high performance tantalum or electrolytic at the output if the noise level is unacceptable.

### Buck Soft-Start

When the buck is enabled soft-start is engaged. Soft-start reduces the inrush current by taking more time to reach the final output voltage. This is achieved by limiting the buck output current over a 1ms period.

### Boost Rectifier Diode

A Schottky rectifier diode (D2 in the Block Diagram) is recommended for the boost rectifier diode. The diode should have low forward drop at the peak operating current, low reverse current and fast reverse recovery times. The current rating should take into account power dissipation as well as output current requirements. The diode current rating should be equal to or greater than the average forward current which is normally equal to the output current. The reverse breakdown voltage should be greater than the $V_{OUT}$ voltage plus the peak ringing voltage that is generated at the SW2 pin. Generally higher reverse breakdown diodes will have lower reverse currents. Refer to Table 3 for Schottky diode vendors.

**Table 3. Schottky Diode Vendors**

| PART NUMBER | $V_R$ (V) | $I_{AVE}$ (A) | $V_F$ AT 1A (mV) | $V_F$ AT 2A (mV) | $I_R$ AT 5V 85°C (µA) |
|---|---|---|---|---|---|
| **Diodes Inc.** | | | | | |
| B130 | 30 | 1 | 460 | | 20 |
| B230 | 30 | 2 | | 430 | 100 |
| **Rohm** | | | | | |
| RSX201VA-30 | 30 | 1 | 360 | | 600 |
| **Vishay** | | | | | |
| VS-20MQ060 | 60 | 2.1 | | | |

### Boost Inductor L2 Selection and Maximum Output Current

The boost inductor L2 should be 3.3µH to ensure fast transfer of power from the buck to the boost after a $V_{IN}$ power outage. Refer to Table 1 for inductor vendors.

### Boost Frequency Compensation

The LTC3355 boost switching regulator uses current mode control to regulate $V_{OUT}$. This simplifies loop compensation and ceramic output capacitors can be used. The boost regulator does not require the ESR of the output capacitor for stability. Frequency compensation is provided by the components connected to the $V_{CBST}$ pin. Generally a capacitor ($C_C$) and resistor ($R_C$) in series to ground are used as shown in the Block Diagram.

Loop compensation determines the stability and transient performance. Optimizing the design of the compensation network depends on the application and type of output capacitor. A practical approach is to start with one of the circuits in this data sheet that is similar to your application and tune the compensation network to optimize the performance. Stability should then be checked across all

## APPLICATIONS INFORMATION

operating conditions, including load current, input voltage and temperature. Figure 2 shows an equivalent circuit for the boost regulator control loop. The error amplifier is a transconductance amplifier with a finite output impedance. The power section consisting of a modulator, power switch and inductor, is modeled as a transconductance amplifier generating an output current proportional to the voltage at the $V_{CBST}$ pin. Note that the output capacitor integrates this current, and that the capacitor on the $V_{CBST}$ pin ($C_C$) integrates the error amplifier output current, resulting in two poles in the loop. In most cases a zero is required and comes from either the ESR of the output capacitor or from a resistor $R_C$ in series with $C_C$. This simple model works well as long as the inductor value is not too high and the loop crossover frequency is much lower than the switching frequency. A phase lead capacitor across the feedback divider may improve the transient response. A small capacitor from $V_{CBST}$ to ground may have to be added if phase lead is used.

### Low Ripple Burst Mode Operation

To enhance efficiency at light loads the buck and boost regulator can run in low ripple Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. Setting the MODE pin high sets both the buck and boost into Burst Mode operation. During Burst Mode operation, the enabled regulator delivers single cycle bursts of current to the output capacitor followed by sleep periods where the power is delivered to the load by the output capacitor. Since the power to the output is delivered with single, low current pulses, the output ripple is kept below 15mV for typical applications. As the load current falls towards a no-load condition, the percentage of time in sleep mode increases and the average input current is greatly reduced resulting in high efficiency even at very light loads. At higher load currents the regulators will seamlessly transition into PWM mode.

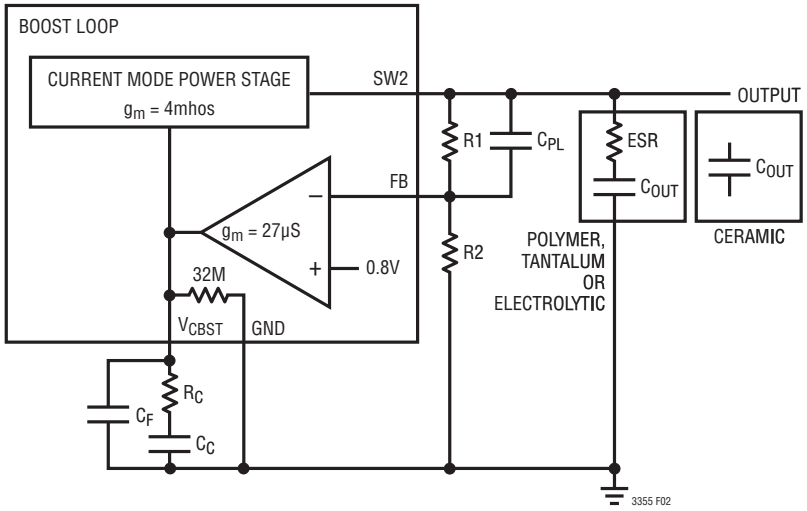



**Figure 2. Model for Boost Loop Response**

# APPLICATIONS INFORMATION

### PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Large switched currents flow in the $V_{IN}$, SW1, SW2 and paddle ground pins, the buck catch diode, boost rectifier diode and the input capacitor. The loop formed by these components should be as small as possible. These components, along with the inductors and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. All connections to GND should be made at a common star ground point or directly to a local, unbroken ground plane below these components. SW1 and SW2 nodes should be laid out carefully to avoid interference. Keep the FB, PFI, $I_{CHG}$, $I_{BSTPK}$, $V_{CBST}$ and CFB nodes small so that the ground traces will shield them from the switching nodes. To keep thermal resistance low, extend the ground plane as much as possible and add thermal vias under and near the paddle. Keep in mind that the thermal design must keep the junctions of the LTC3355 below the specified absolute maximum temperature.

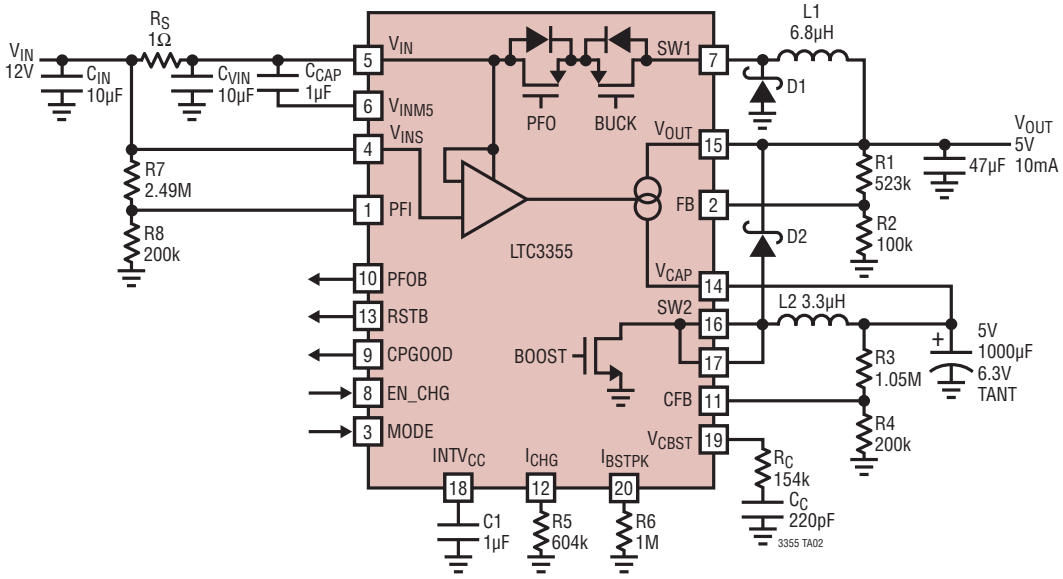
### High Temperature Considerations

The PCB must provide heat sinking to keep the LTC3355 cool. The exposed pad on the bottom of the package may be soldered to a copper area which should be tied to large copper layers below with thermal vias; these layers will spread the heat dissipated by the LTC3355. Place additional vias to reduce thermal resistance further. With these steps, the thermal resistance from the die (or junction) to ambient can be reduced to $\theta_{JA}$ = 47°C/W or less. With 100 LFPM airflow, this resistance can fall by another 25%.

The LTC3355 has two thermal circuits. The first thermal circuit is operational when the buck and charger are enabled. If the die temperature exceeds 110°C the charge current will be reduced. When the LTC3355 is in boost mode the high current thermal shutdown will turn the boost off when the die temperature reaches 155°C. The high temperature shutdown is active in all modes of operation.

# TYPICAL APPLICATIONS

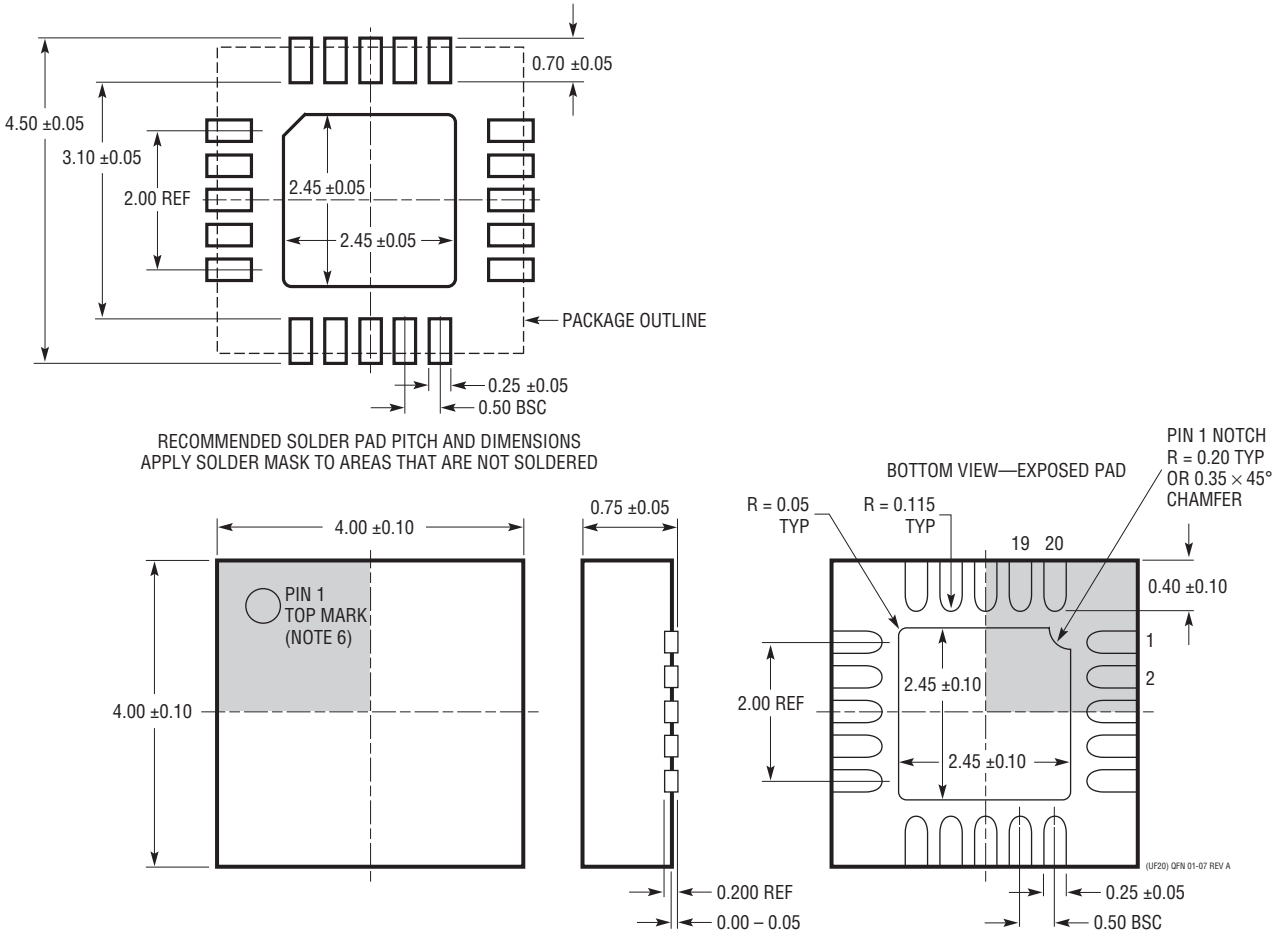
**Tantalum Capacitor Charger and Ride-Through Backup Supply**



# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

**UF Package**
**20-Lead Plastic QFN (4mm × 4mm)**
(Reference LTC DWG # 05-08-1710 Rev A)




NOTE:
1. DRAWING IS PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-1)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 08/14 | Modified $V_{OUT}$ Overvoltage, Undervoltage Lockout section | 11 |
| | | Modified Input Voltage Range equation | 12 |
| | | Modified $I_{CHG}$ Set Resistor section | 12 |
| | | Modified $I_{BSTPK}$ Set Resistor section | 12 |
| B | 4/15 | Updated conditions for $I_{SW1}$, $I_{SW2}$ and $I_{VOUT}$ | 3 and 4 |
| | | Updated units for Boost Error Amplifier Transconductance | 4 |
| | | Updated units for Boost Error Amplifier Transconductance vs Temperature Graph | 7 |
| | | Update TSTB (Pin 13), CPGOOD (Pin 9), PFOB (Pin 10) | 8 |
| | | Updated Block Diagram | 9 |
| | | Updated CFB Resistor Network and PFI Resistor Network | 12 |
| | | Updated Table 2: Capacitor Vendors | 14 |
| | | Updated Boost Error Amplifier Transconductance unit in Figure 2 | 16 |