Lead-Acid Battery Balancer

FEATURES

- **Single IC Balances Up to Four 12V Lead-Acid Batteries in Series**
- **All NFET Design**
- **Stackable to Balance Larger Series Battery Packs**
- **Standalone Balancing Operation: Requires No External µP or Additional Control Circuitry**
- **Balancing Current Limited by External PTC Thermistor**
- Continuous Mode and Timer Mode
- Programmable UV and OV Fault Thresholds
- Programmable Termination Time and Termination Voltage
- Thermally Enhanced 38-Lead TSSOP Package

APPLICATIONS

- Telecom Backup Systems
- Home Battery Powered Backup Systems
- Industrial Electric Vehicles
- Energy Storage Systems (ESS)
- Medical Equipment

DESCRIPTION

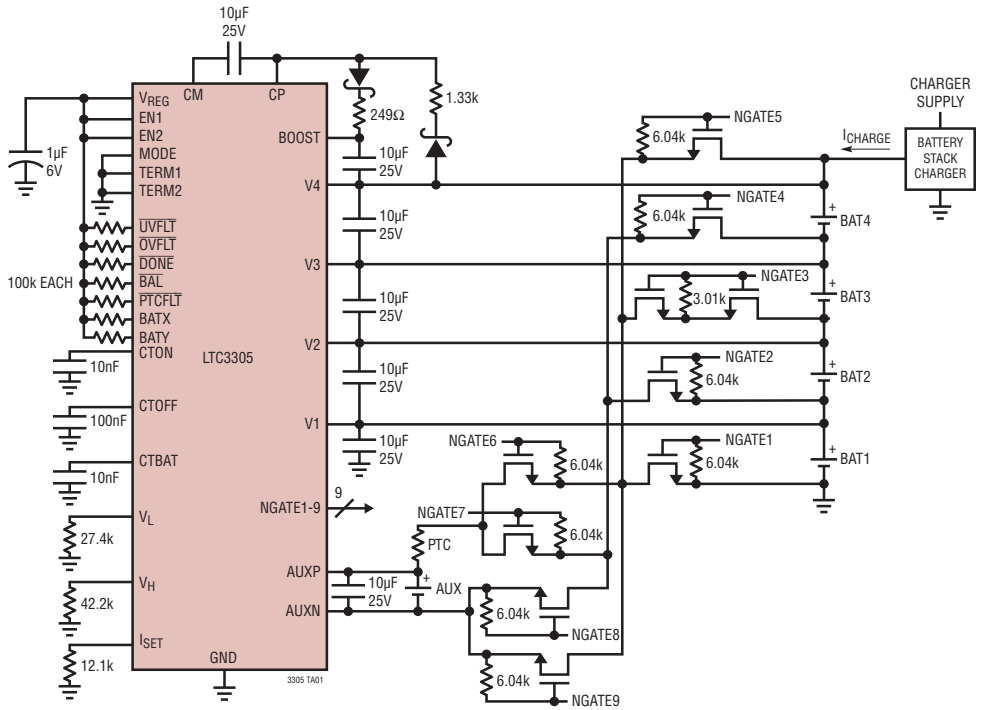
The LTC®3305 balances up to 4 lead-acid batteries connected in series. It is intended to be used in conjunction with a separate pre-existing battery charger as part of a high performance battery system. All voltage monitoring, gate drive, and fault detection circuitry is integrated.

The LTC3305 employs an auxiliary battery or an alternative storage cell to transfer charge to or from each individual battery in the stack. A mode pin provides two operating modes, timer mode and continuous mode. In timer mode, once the balancing operation is completed, the LTC3305 goes into a low power state for a programmed time and then periodically rebalances the batteries. In continuous mode, the balancing operation continues even after the batteries are balanced to their programmed termination voltage.

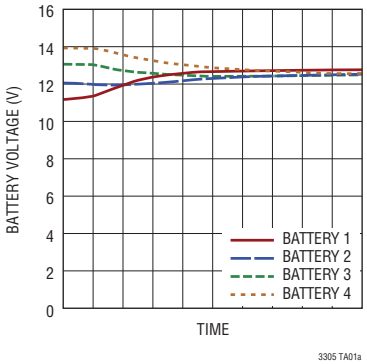
The LTC3305 is available in a thermally enhanced 38-lead TSSOP package.

TYPICAL APPLICATION

4-Battery Balancer with Programmed High and Low Battery Voltage Faults



Battery Voltages Converge Over Time



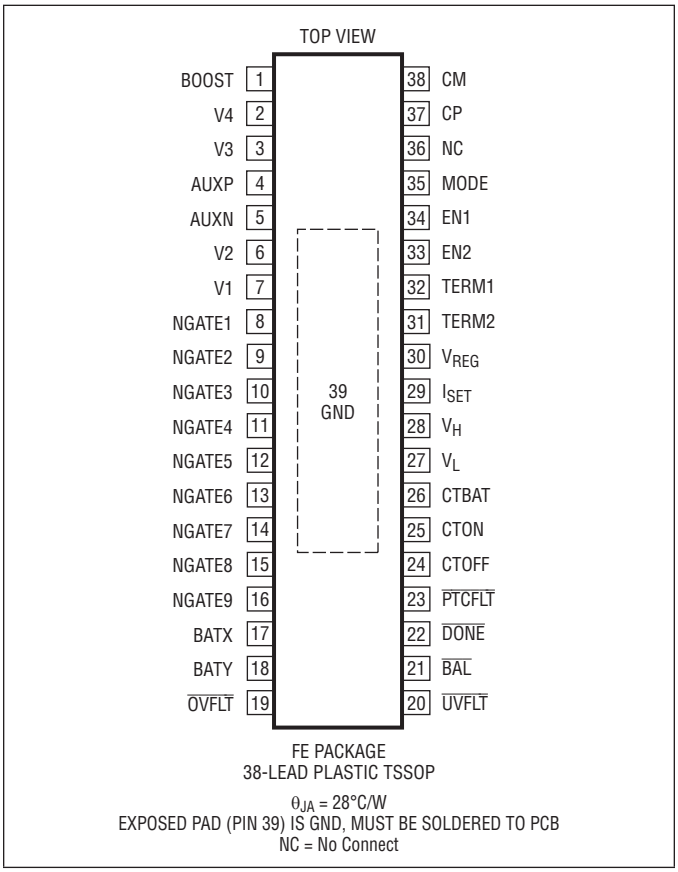
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Stack Voltage, V4 to GND 68V
Battery Voltages, V4 to V3, V3 to V2, V2 to V1, V1 to GND ..... –0.3V to 20V
Auxiliary Cell Voltage, AUXP to AUXN ..... –0.3V to 20V
V_{REG} Voltage ..... –0.3V to 6V
V_H, V_L Voltage ..... –0.3V to Lesser of 6V or (V_{REG}+0.3V)
$\overline{UVFLT}$, $\overline{OVFLT}$, $\overline{PTCFLT}$, $\overline{BAL}$, $\overline{DONE}$, BATX, BATY Voltage ..... –0.3V to 6V
EN1, EN2, MODE, TERM1, TERM2 Voltage ..... –0.3V to Lesser of 6V or (V_{REG}+0.3V)
NGATE1, NGATE2, NGATE3, NGATE4, NGATE8, NGATE9 Voltage ..... –0.3V to Lesser of 68V or (V4+0.3V)
NGATE5, NGATE6, NGATE7 Voltage ..... (Greater of –0.3V or BOOST–68V) to (BOOST+0.3V)*
$\overline{UVFLT}$, $\overline{OVFLT}$, $\overline{PTCFLT}$, $\overline{BAL}$, $\overline{DONE}$, BATX, BATY Current 10mA
I_{SET} Current 1mA
CP, CM Current 50mA
Operating Junction Temperature Range (Notes 2, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

*The BOOST voltage is generated by the LTC3305 and is typically 8.45V higher than V4.

PIN CONFIGURATION



FE PACKAGE
38-LEAD PLASTIC TSSOP

θ_{JA} = 28°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB
NC = No Connect

ORDER INFORMATION

(http://www.linear.com/product/LTC3305#orderinfo)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3305EFE#PBF	LTC3305EFE#TRPBF	LTC3305 FE	38-Lead Plastic TSSOP	–40°C to 125°C
LTC3305IFE#PBF	LTC3305IFE#TRPBF	LTC3305 FE	38-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V1 = 13.2V, V2 = 26.4V, V3 = 39.6V, V4 = 52.8V, AUXP - AUXN = 13.2V, R_{ISET} = 12.1kΩ

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{BAT}	Individual Battery Voltage		●	4		16	V
V4	Voltage at the Top of the Battery Stack		●	12		64	V
V_{REG}	Regulator Output Voltage	I_{VREG} = 200µA	●	2.4	2.5	2.6	V
$V_{REG,UV}$	Regulator Undervoltage Threshold	Regulator Voltage Falling	●	1.7	2.1		V
	Hysteresis				125		mV
	Maximum Guaranteed Load Current	$V_{REG} > V_{REG,UV}$	●	3			mA
	Regulator Short Circuit Current Limit	V_{REG} = 0V		8	15	22	mA
	Shutdown Current	Measured at V4, BOOST-V4 = 0V Measured at V3, V2, V1, AUXP, BOOST	 ●	16	33 0	50 1	µA µA
	Supply Current While Balancing Battery 1 (Notes 4, 5)	Measured at V4 Measured at V3 Measured at V2 Measured at V1			900 0 0 150	1350 1 1 225	µA µA µA µA
	Supply Current While Balancing Battery 2 (Notes 4, 5)	Measured at V4 Measured at V3 Measured at V2 Measured at V1		 –70	900 0 150 –45	1350 1 225	µA µA µA µA
	Supply Current While Balancing Battery 3 (Notes 4, 5)	Measured at V4 Measured at V3 Measured at V2 Measured at V1		 –70	900 150 –45 0	1350 225 1	µA µA µA µA
	Supply Current While Balancing Battery 4 (Notes 4, 5)	Measured at V4 Measured at V3 Measured at V2 Measured at V1		 –70 	1050 –45 0 0	1575 1 1	µA µA µA µA
	Supply Current While Balancing any Battery	Measured at AUXP Measured at AUXN		 –195	165 –130	245	µA µA
	Supply Current in OFF State (MODE = 0)	Measured at V4, BOOST-V4 = 0V Measured at V3, V2, V1, AUXP, BOOST			100 0	150 1	µA µA
	Boost Pin Current While Balancing any Battery (Notes 4, 5)				220	330	µA
V_{ISET}	I_{SET} Servo Voltage	50µA< I_{ISET}< 150µA	●	1.18	1.2	1.22	V
I_{VH}, I_{VL}	Current Out of V_H and V_L Pins	I_{ISET} = 100µA	●	31.3	33.3	35.3	µA
I_{NGATE}	Current For External NMOS Turn On (Note 5) Leakage Current in Shutdown	NGATE3 Current, I_{ISET} = 100µA All Other NGATE Currents, I_{ISET} = 100µA EN1 = EN2 = 0	● ● ●	2.0 1.0 –2	2.2 1.1	2.4 1.2 2	mA mA µA
	Current Programmable Range	NGATE3 Current All Other NGATE Currents	● ●	1 0.5		3 1.5	mA mA
$V_{BAT,UV}$	Undervoltage Falling Battery Threshold (Note 6)	V_L = 0.4V V_L = 1.6V	● ●	3.9 15.6	4 16	4.1 16.4	V V
	Undervoltage Hysteresis				120		mV
	Undervoltage Falling Programmable Range		●	4		16	V
$V_{BAT,OV}$	Overvoltage Rising Battery Threshold (Note 6)	V_H = 0.4V V_H = 1.6V	● ●	3.9 15.6	4 16	4.1 16.4	V V
	Overvoltage Hysteresis				150		mV
	Overvoltage Rising Programmable Range		●	4		16	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V1 = 13.2V, V2 = 26.4V, V3 = 39.6V, V4 = 52.8V, AUXP - AUXN = 13.2V, R_{ISET} = 12.1kΩ

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	PTC Fault Threshold	|BAT-AUXP| Falling		0.8	1	1.2	V
	Hysteresis				100		mV
$V_{TERMINATE}$	|BAT-AUXP| for Which Balancing Is Terminated	TERM2 = 0, TERM1 = 0 TERM2 = 0, TERM1 = 1 TERM2 = 1, TERM1 = 0 TERM2 = 1, TERM1 = 1	● ● ● ●	5.0 17.5 40 85	12.5 25 50 100	20.0 32.5 60 115	mV mV mV mV
	Minimum (BOOST-V4) Voltage for Operation		●	6.7	6.95	7.2	V
	Hysteresis				180		mV
	Maximum (BOOST-V4) Voltage Regulated		●		8.45	8.75	V
	Hysteresis				200		mV
R_{NMOS}	Charge Pump NMOS Switch ON Resistance	Measured at 10mA			20		Ω
R_{PMOS}	Charge Pump PMOS Switch ON Resistance	Measured at 10mA			55		Ω
t_{BAT}	Maximum Time a Single Battery Stays Connected to the Auxiliary Battery	CTBAT = 10nF		4.5	5	5.5	sec
t_{ON}	Maximum Stack Balancing Termination Time	MODE = 0, CTON = 10nF		0.43	0.48	0.53	hrs
t_{OFF}	Off Time After Stack Balance Termination	MODE = 0, $\overline{DONE}$ = 0, CTOFF = 10nF		0.43	0.48	0.53	hrs
V_{IH}	Digital Input High Voltage	EN1, EN2, MODE, TERM1, TERM2 Pins	●	1.2			V
V_{IL}	Digital Input Low Voltage	EN1, EN2, MODE, TERM1, TERM2 Pins	●			0.4	V
I_{IH}, I_{IL}	Leakage Current	EN1, EN2, MODE, TERM1, TERM2 Pins; 2.5V at Pin	●	–1		1	µA
V_{OL}	Output Low Voltage	BATX, BATY, $\overline{BAL}$, $\overline{DONE}$, $\overline{UVFLT}$, $\overline{OVFLT}$, $\overline{PTCFLT}$ Pins; 3mA Into Pin	●		27.5	150	mV
I_{OH}	Output High Leakage Current	BATX, BATY, $\overline{BAL}$, $\overline{DONE}$, $\overline{UVFLT}$, $\overline{OVFLT}$, $\overline{PTCFLT}$ Pins; 6V at Pin				1	µA
	Thermal Shutdown Threshold (Note 7)	Rising Temperature			155		°C
	Thermal Shutdown Hysteresis				10		°C

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. The LTC3305 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3305E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3305I is guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Note 4. The NGATE pin currents are not included in this number.

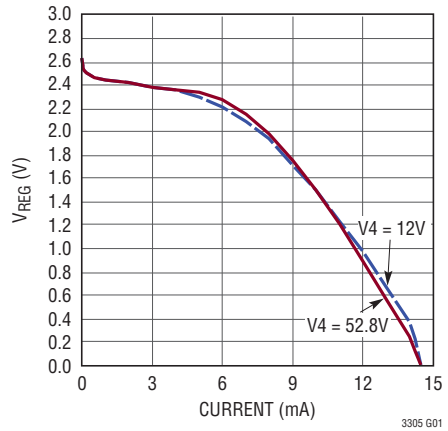
Note 5. The NGATE5, NGATE6, NGATE7 pin currents are drawn from the BOOST pin. All other NGATE pin currents are drawn from the V4 pin. The NGATE pin currents add to the currents drawn by V4 and BOOST.

Note 6. The voltage programmed at the V_H and V_L pins are gained up to set the undervoltage and overvoltage thresholds of each battery.

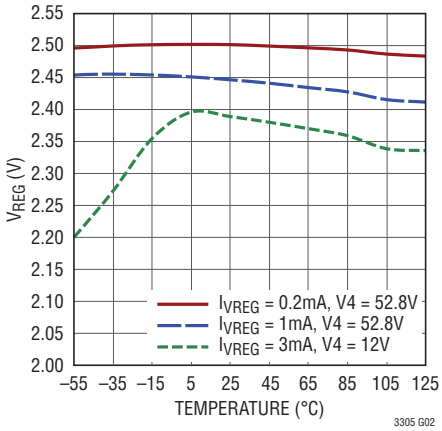
Note 7: This IC includes overtemperature protection intended to protect the device during momentary overload conditions. The maximum junction temperature may be exceeded when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

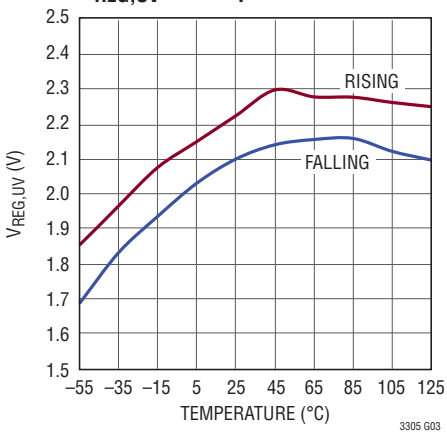
V_{REG} Line and Load Regulation



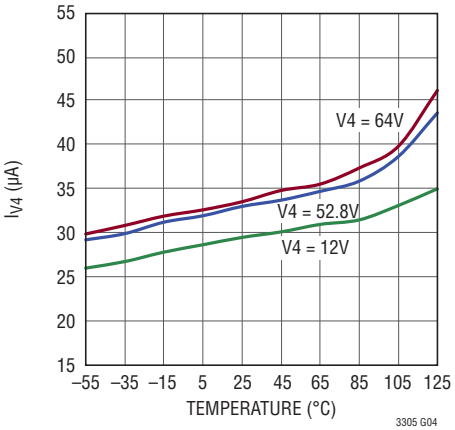
V_{REG} vs Temperature



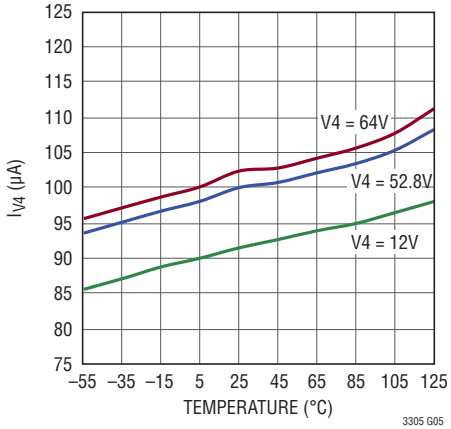
$V_{REG,UV}$ vs Temperature



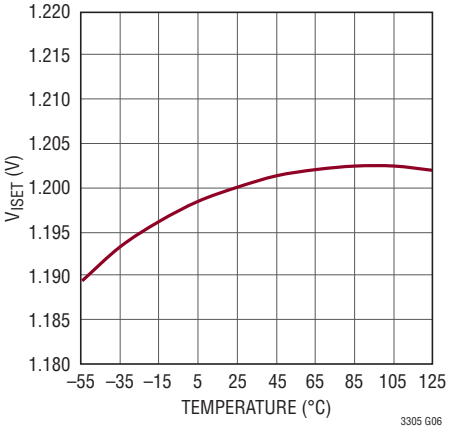
Shutdown Current vs Temperature



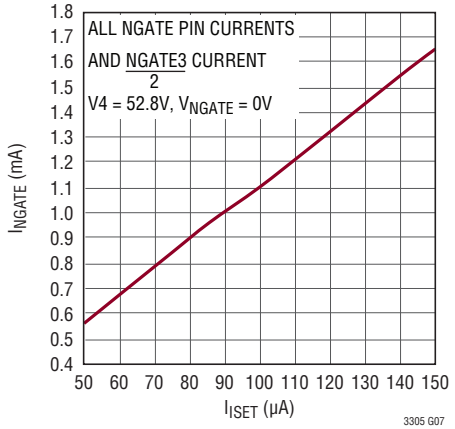
OFF State Current vs Temperature



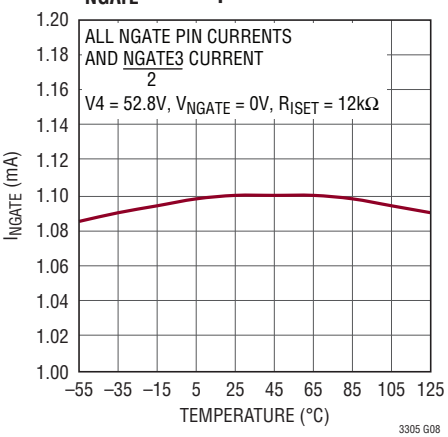
V_{ISET} vs Temperature



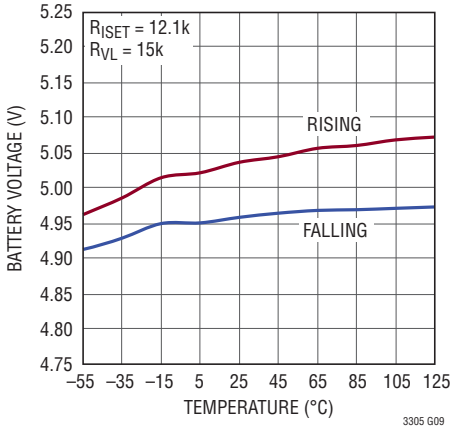
I_{NGATE} vs I_{ISET}



I_{NGATE} vs Temperature

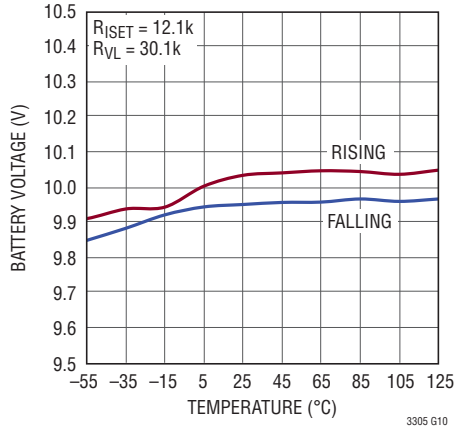


UV Threshold vs Temperature

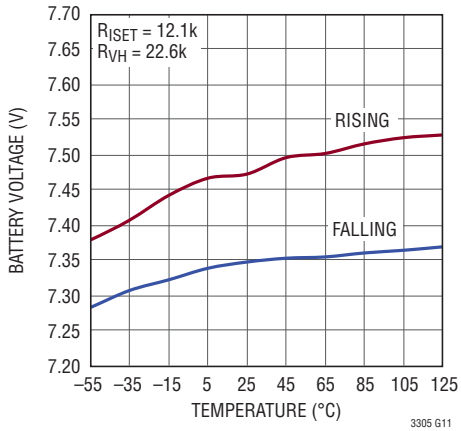


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

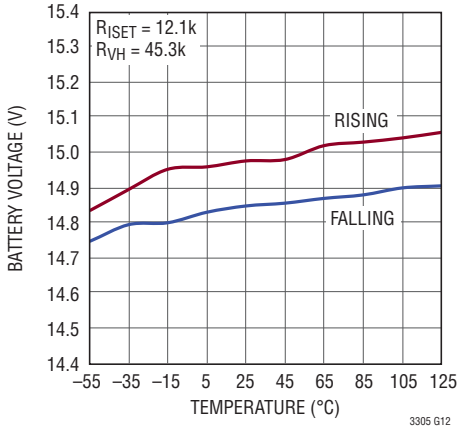
UV Threshold vs Temperature



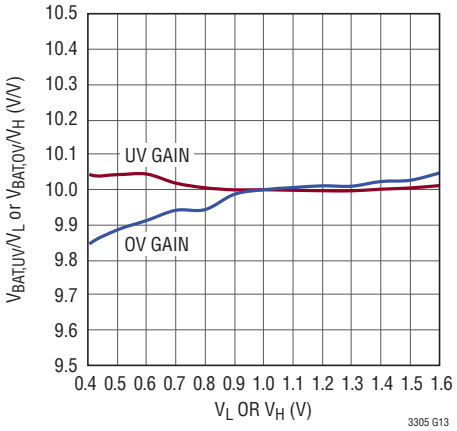
OV Threshold vs Temperature



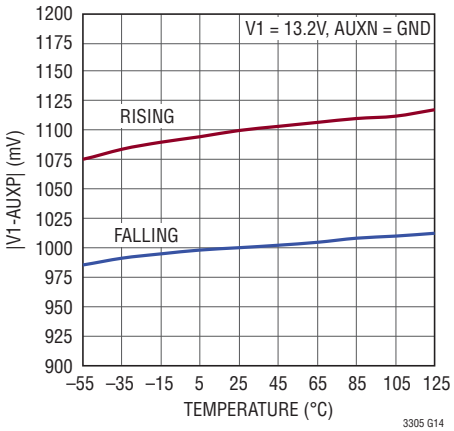
OV Threshold vs Temperature



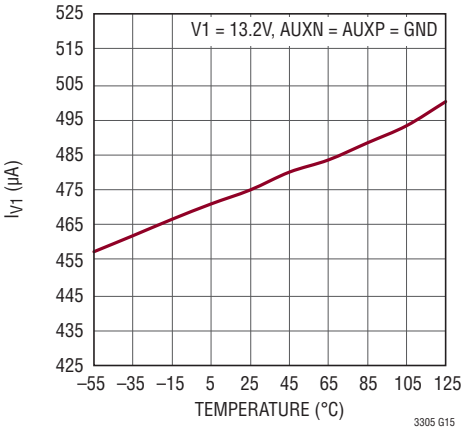
UV and OV Programming Gain



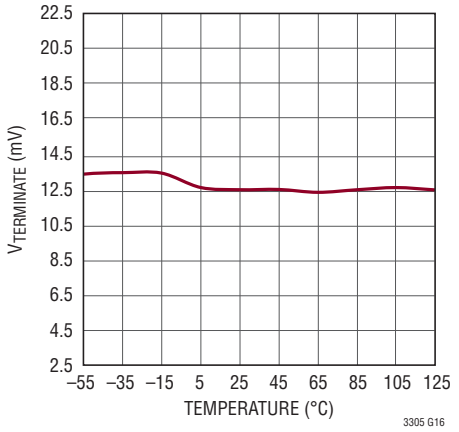
PTC Fault Threshold vs Temperature



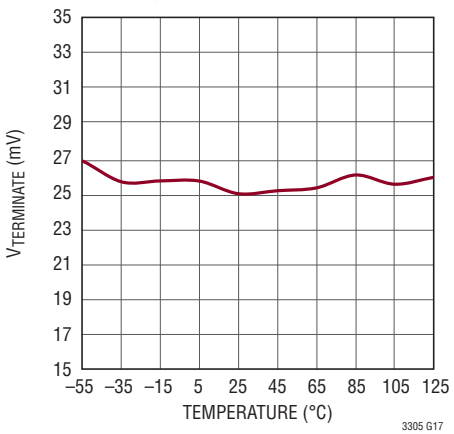
Maximum Battery Current During PTC Fault Condition



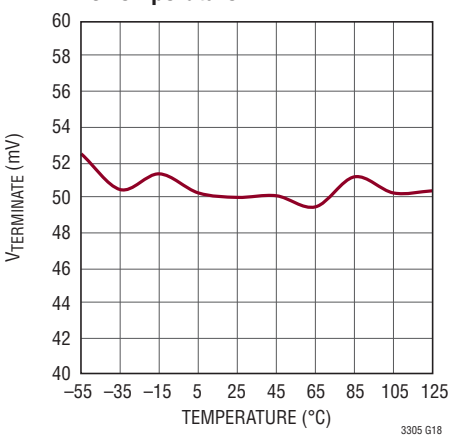
12.5mV Termination Threshold vs Temperature



25mV Termination Threshold vs Temperature

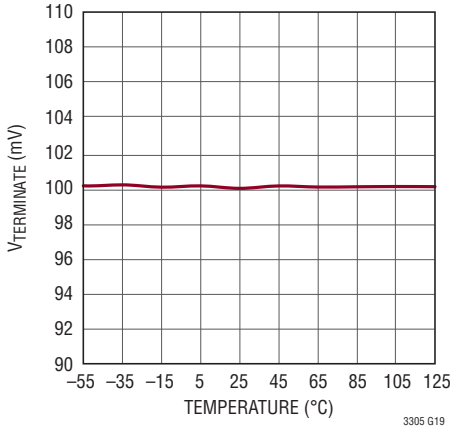


50mV Termination Threshold vs Temperature

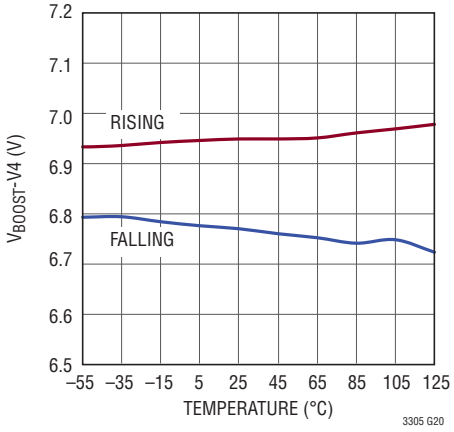


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

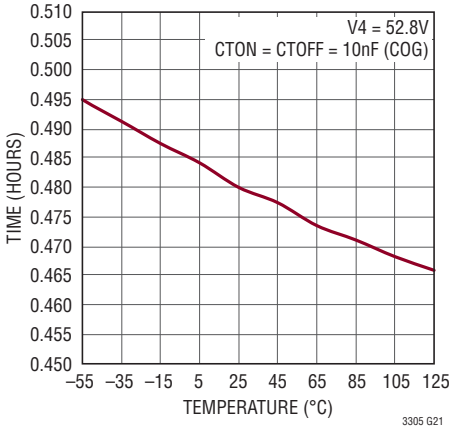
100mV Termination Threshold vs Temperature



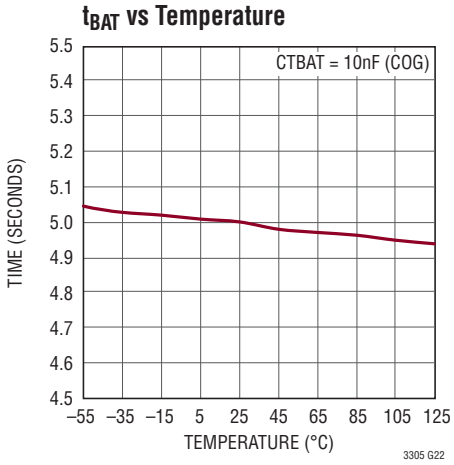
Minimum Boost Voltage vs Temperature



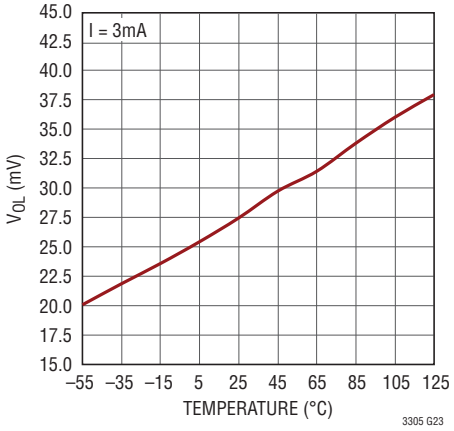
t_{ON}, t_{OFF} vs Temperature



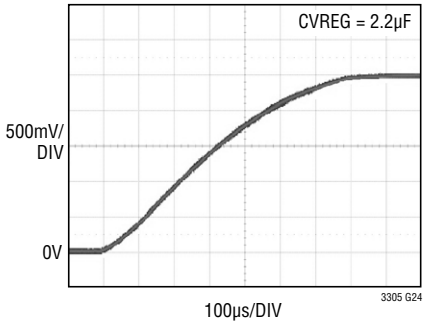
t_{BAT} vs Temperature



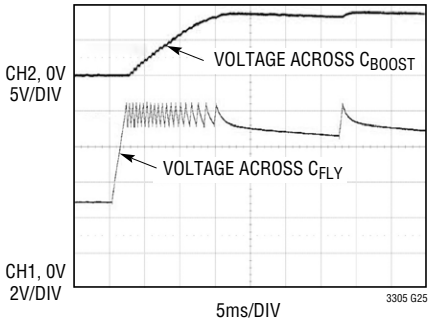
V_{OL} vs Temperature



V_{REG} Start-Up



Boost Charge Pump Start-Up



PIN FUNCTIONS

BOOST (Pin 1): Charge Pump Output. Decouple with a 10µF capacitor to V4.

V4 (Pin 2): Positive terminal of Battery 4 connects to this pin. Battery 4 is connected between V4 and V3. Decouple with at least a 10µF capacitor to V3.

V3 (Pin 3): Positive terminal of Battery 3 connects to this pin. Battery 3 is connected between V3 and V2. Decouple with at least a 10µF capacitor to V2.

AUXP (Pin 4): Positive terminal of the auxiliary cell connects to this pin. Decouple with at least a 10µF capacitor to AUXN.

AUXN (Pin 5): Negative Terminal of the auxiliary cell connects to this pin.

V2 (Pin 6): Positive terminal of Battery 2 connects to this pin. Battery 2 is connected between V2 and V1. Decouple with at least a 10µF capacitor to V1.

V1 (Pin 7): Positive terminal of Battery 1 connects to this pin. Battery 1 is connected between V1 and GND. Decouple with at least a 10µF capacitor to GND.

NGATE1 (Pin 8): NMOS1 Gate. Connect to the gate terminal of external NMOS switch.

NGATE2 (Pin 9): NMOS2 Gate. Connect to the gate terminal of external NMOS switch.

NGATE3 (Pin 10): NMOS3 Gate. Connect to the gate terminal of external NMOS switch.

NGATE4 (Pin 11): NMOS4 Gate. Connect to the gate terminal of external NMOS switch.

NGATE5 (Pin 12): NMOS5 Gate. Connect to the gate terminal of external NMOS switch.

NGATE6 (Pin 13): NMOS6 Gate. Connect to the gate terminal of external NMOS switch.

NGATE7 (Pin 14): NMOS7 Gate. Connect to the gate terminal of external NMOS switch.

NGATE8 (Pin 15): NMOS8 Gate. Connect to the gate terminal of external NMOS switch.

NGATE9 (Pin 16): NMOS9 Gate. Connect to the gate terminal of external NMOS switch.

BATX (Pin 17): This pin along with BATY indicates which battery in the stack is currently being balanced and to which the fault outputs apply. Open Drain Output.

BATY (Pin 18): This pin along with BATX indicates which battery in the stack is currently being balanced and to which the fault outputs apply. Open Drain Output.

$\overline{\text{OVFLT}}$ (Pin 19): Overvoltage Fault. This pin is pulled low when an overvoltage fault condition is detected on a battery. Open Drain Output.

$\overline{\text{UVFLT}}$ (Pin 20): Undervoltage Fault. This pin is pulled low when an undervoltage fault condition is detected on a battery. Open Drain Output.

$\overline{\text{BAL}}$ (Pin 21): Balancing Indicator. This pin is pulled low while the balancing operation is being performed and is in its high impedance state when the part is disabled or the part is in the sleep state. Open Drain Output.

$\overline{\text{DONE}}$ (Pin 22): Done Indicator. This pin is pulled low when all the batteries in the stack are balanced. This pin is in its high impedance state in shutdown. Open Drain Output.

$\overline{\text{PTCFLT}}$ (Pin 23): PTC Fault. This pin is pulled low when the voltage across the PTC thermistor exceeds 1V. It is in its high impedance state at all other times. Open Drain Output.

CTOFF (Pin 24): A capacitor from this pin to GND programs the retry time in timer mode. Connect to GND if MODE = 1.

CTON (Pin 25): A capacitor from this pin to GND programs the maximum time for the balancing operation in timer mode. Connect to GND if MODE = 1.

CTBAT (Pin 26): A capacitor from this pin to GND programs the maximum time an individual battery in the stack is connected to the auxiliary cell during the balancing operation.

V_L (Pin 27): Low Voltage Fault Threshold. A resistor from this pin to GND programs the low voltage fault threshold for each battery in the series stack. Works in conjunction with the I_{SET} pin.

V_H (Pin 28): High Voltage Fault Threshold. A resistor from this pin to GND programs the high voltage fault threshold for each battery in the series stack. Works in conjunction with the I_{SET} pin.

PIN FUNCTIONS

I_{SET} (Pin 29): Reference Current Pin that Servos to 1.2V. A resistor from this pin to GND programs the gate charge current for the external NMOS switches. The reference current is also used to program the undervoltage and overvoltage thresholds.

V_{REG} (Pin 30): Low Voltage Regulated Output. An internally generated voltage of 2.5V is always present at this pin. The voltage at this pin may be overdriven by a higher external voltage up to 5.5V. This pin has limited current sink capability and will not pull down a higher externally applied voltage. All logic input pins must be referenced to this pin. Decouple with a 1µF capacitor to GND.

TERM2 (Pin 31): Termination Threshold Select. This pin along with TERM1 is used to set the voltage difference between the battery and auxiliary cell at which a battery is deemed balanced. High input impedance pin, do not float.

TERM1 (Pin 32): Termination Threshold Select. This pin along with TERM2 is used to set the voltage difference between the battery and auxiliary cell at which a battery is deemed balanced. High input impedance pin, do not float.

EN2 (Pin 33): Enable Input. The state of the EN1 and EN2 pins is used to indicate the number of batteries in the stack. With both pins at GND, the part is in shutdown. High input impedance pin, do not float.

EN1 (Pin 34): Enable Input. The state of the EN1 and EN2 pins is used to indicate the number of batteries in the stack. With both pins at GND, the part is in shutdown. High input impedance pin, do not float.

MODE (Pin 35): Mode Select. When held high, continuous mode is selected. When held low, timer mode is selected. High input impedance pin, do not float.

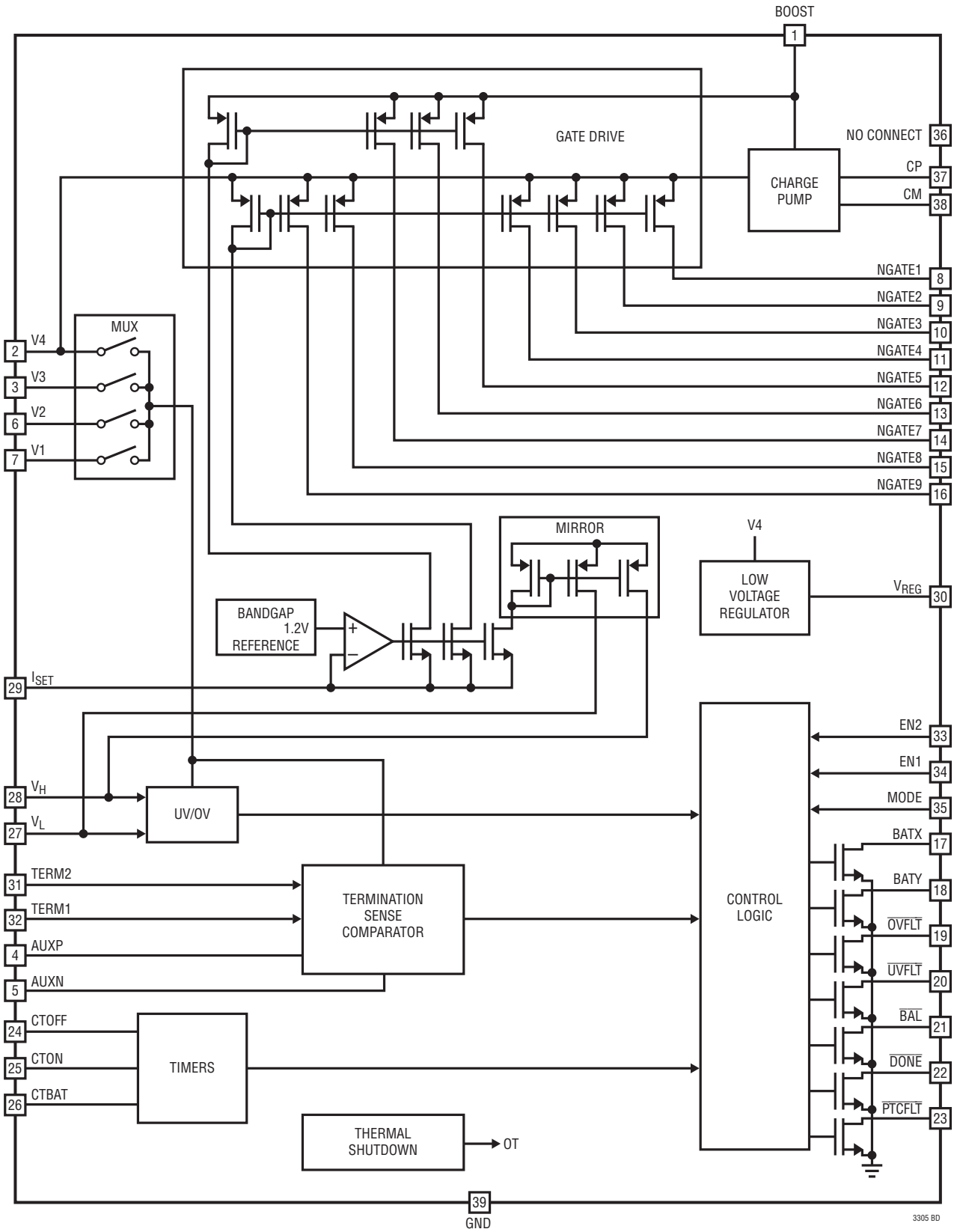
No Connect (Pin 36): This pin is not connected internally. Solder this pin to a pad electrically isolated from all other circuit nodes.

CP (Pin 37): Positive Terminal of Charge Pump Flying Capacitor. Connect a 10µF capacitor from this pin to CM for charge pump operation.

CM (Pin 38): Negative Terminal of Charge Pump Flying Capacitor. Connect a 10µF capacitor from this pin to CP for charge pump operation.

GND (Pin 39): The exposed pad is ground and must be soldered to PCB ground for electrical connectivity and rated thermal performance.

BLOCK DIAGRAM



OPERATION

The LTC3305 balancer is intended to be used in conjunction with a separate pre-existing battery stack charger as part of a high performance battery system. The balancing operation itself is stand-alone and can operate independent of whether the battery stack is being charged, discharged, or both. That being said, because the LTC3305 balances voltages, it works best if the voltage readings are stable, which is more true when the battery stack is not being charged or discharged. Nevertheless, it will properly balance the battery voltages when the stack is being concurrently charged and/or discharged, since the voltage across the batteries will average out over time as the LTC3305 repeatedly cycles through them. Like all balancers, the LTC3305 will slightly net-discharge the stack in the absence of a separate charger.

The LTC3305 balances batteries using an auxiliary cell or an alternate storage cell as a charge reservoir. External NMOS switches are controlled in a preprogrammed sequence to connect each battery in the stack to an auxiliary cell. Charge is transferred to or from the auxiliary cell when it is connected to a battery.

The LTC3305 can operate in one of two modes programmable via the MODE pin.

Timer Mode (MODE = 0)

The balancing operation begins once the C_{BOOST} capacitor is charged to at least 6.95V. The $\overline{BAL}$ pin is pulled low, indicating that the part is enabled and balancing the battery stack.

The termination voltage, $V_{TERMINATE}$, is the difference in voltage between the auxiliary cell and the battery connected to the auxiliary cell for which a battery is considered to be balanced. $V_{TERMINATE}$ is programmed via the TERM1 and TERM2 pins to one of four preset voltages as shown in Table 1.

Table 1. Termination Voltages

TERM1	TERM2	$V_{TERMINATE}$
0	0	±12.5mV
1	0	±25mV
0	1	±50mV
1	1	±100mV

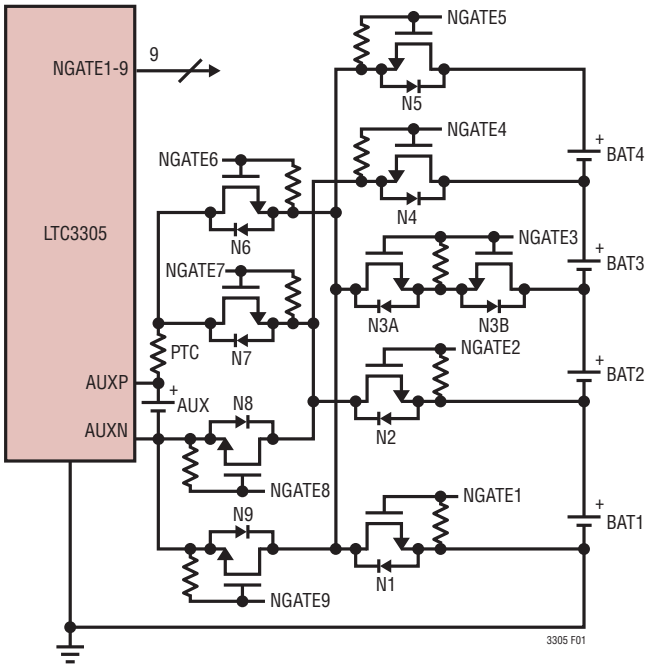


Figure 1. External Switch Arrangement for a 4- Battery Balancing Application

The balancing operation begins with the negative terminal of the auxiliary cell connected to the negative terminal of BAT1, the lowest battery in the stack. Referring to Figure 1, the bottom switches N1 and N9 that connect the negative terminal of BAT1 to the auxiliary cell's negative terminal are first turned on. To turn on an external NMOS switch, the current source at the NGATE pin connected to the gate of the external NMOS is turned on and a gate source voltage is developed across an external resistor.

After an internally set delay of 35ms, the voltages across the auxiliary cell and BAT1 are compared by the termination sense comparator.

If the voltage difference between the auxiliary cell and BAT1 is less than the selected termination voltage, the battery is deemed to be balanced with respect to the auxiliary cell and the bottom switches are turned off by turning off the corresponding NGATE pin currents. The next battery in the stack is then connected to the auxiliary cell.

OPERATION

If the voltage difference between the auxiliary cell and BAT1 is greater than the selected termination voltage, the top NMOS switches N2 and N7 that connect the positive terminal of BAT1 to the auxiliary cell's positive terminal through the PTC thermistor are turned on. After a second internally set delay of 35ms, the termination sense comparator starts monitoring the voltages across the auxiliary cell and the battery. The battery stays connected to the auxiliary cell until the voltage difference decreases to $V_{TERMINATE}$ or a t_{BAT} timeout occurs (t_{BAT} is the maximum time that a battery remains connected to the auxiliary cell and is programmed by a capacitor on the CTBAT pin). This timer is reset each time the auxiliary cell is connected to a different battery.

At this point, all switches are turned off and the next battery in the stack is connected to the auxiliary cell. After the switches have been turned off, an internal 40ms delay provides a break-before-make time after which the negative terminal of the next battery in the stack is connected to the negative terminal of the auxiliary cell via its bottom switches. Table 2 shows the top and bottom switches used to connect each battery for different battery stack configurations. When only the bottom switches are on, there is a conduction path between the auxiliary cell and the battery through the body diodes of the top switches. Current will flow through this conduction path if the auxiliary cell and the battery are more than two diode drops apart. The current is limited by the PTC resistor.

Table 2. Top and Bottom Switch Arrangement

EN1, EN2	BATTERY BEING BALANCED	TOP SWITCHES	BOTTOM SWITCHES
1,1 (4 Bat App)	Battery 1	N2, N7	N1, N9
	Battery 2	N3, N6	N2, N8
	Battery 3	N4, N7	N3, N9
	Battery 4	N5, N6	N4, N8
1,0 (3 Bat App)	Battery 1	N2, N7	N1, N8
	Battery 2	N4, N6	N2, N9
	Battery 3	N5, N7	N4, N8
0,1 (2 Bat App)	Battery 1	N7	N9
	Battery 2	N5	N8

In this fashion each battery in the stack is connected to the auxiliary cell and the batteries in the stack will be balanced.

An internal clamp circuit protects the LTC3305 when the voltage difference between the battery being balanced and the auxiliary cell is greater than 1V. With a 13.2V difference, the clamp draws 475µA of current. In the worst case scenario, a 16V difference may appear between the auxiliary cell and a battery. The internal clamp draws 600µA of current in this scenario.

In the state when both the top and bottom side switches are turned on, the $\overline{PTCFLT}$ pin will be pulled low if the voltage difference between the battery being balanced and the auxiliary cell is greater than 1V. If during the balancing operation the voltage difference becomes less than 1V, the $\overline{PTCFLT}$ pin returns to its high impedance state.

The BATX and BATY pins indicate which battery in the stack is currently connected to the auxiliary cell as shown in Table 3. In shutdown, the BATX and BATY pins are in a High Z state and the $\overline{BAL}$ pin is also in a High Z state.

Table 3. State of BATX and BATY Pins

STATE OF OPERATION	BATX	BATY
Battery 1 Connected	High Z	High Z
Battery 2 Connected	High Z	0
Battery 3 Connected	0	0
Battery 4 Connected	0	High Z

Once all batteries in the stack are balanced the $\overline{DONE}$ pin is pulled low, the $\overline{BAL}$ pin is in its high impedance state and the part is put in a low power OFF state.

A four-battery stack is deemed balanced when the termination sense comparator detects $V_{TERMINATE}$ on five consecutive cycles that connect each of the batteries to the auxiliary cell using the bottom switches only.

OPERATION

In timer mode, a capacitor at the CTON pin programs the maximum time, t_{ON}, that the balancing operation can run for. The balancing operation is terminated either when the batteries in the stack are deemed to be balanced or a t_{ON} time out occurs. After the balancing operation has been terminated, the LTC3305 is put in a low power OFF state for a fixed time, t_{OFF}. The t_{OFF} time is programmed by a capacitor at the CTOFF pin. In the OFF state, the $\overline{BAL}$ pin is put in its high impedance state. Once t_{OFF} times out, the LTC3305 is put back in its ON state and the balancing operation begins again. The t_{ON} timer may be defeated by tying the CTON pin to GND. In this scenario, the LTC3305 will enter the OFF state only when all the batteries in the stack are deemed to be balanced.

Continuous Mode (MODE = 1)

In the continuous mode of operation the part functions in much the same way as in timer mode with the following differences.

1. There is no ON or OFF state. The CTON and CTOFF pins must be tied to GND in continuous mode. The balancing operation continues even if the stack is in balance. The balancing operation is terminated only if the part is put in shutdown. The $\overline{BAL}$ pin is always pulled low in continuous mode.
2. In timer mode, if the termination comparator senses that a battery is balanced to the auxiliary cell with only the bottom plates connected, the balancing operation on that battery is terminated. This is not the case in continuous mode. In continuous mode the top switches are turned on and the balancing operation on a battery is terminated only by a t_{BAT} time out. Since the auxiliary cell remains connected to the battery until a t_{BAT} time out occurs, its voltage can change before it connects to the next battery in the stack. As a result, when the stack is balanced and the $\overline{DONE}$ pin is pulled low, the voltages across the individual batteries in the stack may differ by more than the programmed $V_{TERMINATE}$. In the worst case when the capacity of the auxiliary cell is much smaller than the battery, the individual battery voltages could differ by up to twice the programmed $V_{TERMINATE}$ when balanced.

Charge Pump Operation

The LTC3305 uses external NMOS devices as switches to connect a battery to the auxiliary cell. The LTC3305 has a charge pump that generates the higher voltage required to turn on some of the external NMOS switches.

Two external capacitors C_{FLY} and C_{BOOST}, two diodes D1 and D2, and resistors R1 and R2 are required for charge pump operation as shown in Figure 2. When the LTC3305 is enabled, the charge pump is turned on. C_{FLY} initially charges with a current I_{CHG} through external diode D1, resistor R1, and the internal NMOS switch N1 to GND. When C_{FLY} is charged to 10.5V, an internal comparator switches the internal NMOS switch off and turns on switch P1. C_{FLY} connects to C_{BOOST} through diode D2, resistor R2 and the internal PMOS switch P1. Charge is transferred from C_{FLY} to C_{BOOST} with a current I_{DISCHG}. When C_{FLY} is discharged to 9.5V, it is disconnected from C_{BOOST}, recharged back up to 10.5V, and then reconnected to C_{BOOST}. In this fashion the voltage across C_{BOOST} is built up.

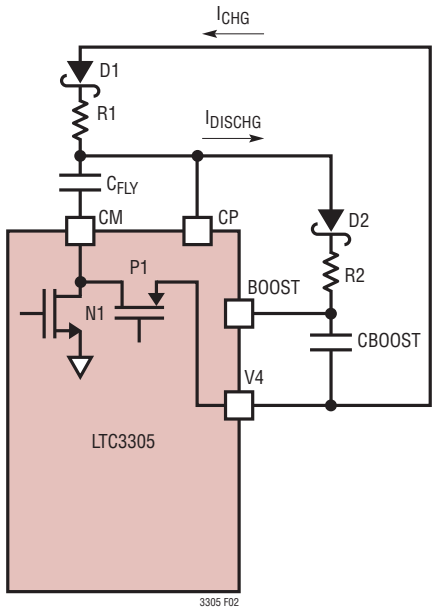


Figure 2. Charge Pump Operation

OPERATION

Once the C_{BOOST} capacitor has 6.95V across it, balancing begins. When C_{BOOST} is charged to 8.45V, the charge pump operation is disabled and C_{FLY} remains connected to C_{BOOST}. Charge pump operation resumes when C_{BOOST} discharges to 8.25V.

Undervoltage and Overvoltage Fault Detection

The undervoltage and overvoltage thresholds can be programmed using the resistor at the I_{SET} pin in conjunction with resistors at the V_L and V_H pins. The voltage present at the V_L or V_H pin programs the corresponding fault threshold to 10× that voltage for each battery in the stack. An internal amplifier accurately gains up the voltage at the V_L and V_H pins and shifts the threshold voltage to the appropriate battery common mode level. The V_L and V_H pins have a programming range from 0.4V to 1.6V. The internal undervoltage and overvoltage comparators may not trip correctly for a program voltage outside this range. An internal clamp prevents the thresholds from being programmed to greater than 20V.

When an undervoltage or overvoltage fault condition is detected, the corresponding $\overline{UVFLT}$ or $\overline{OVFLT}$ pin is pulled to GND. The balancing operation is not interrupted during this time. If an undervoltage or overvoltage fault condition goes away during the balancing operation, the corresponding fault pin returns to its high impedance state.

If the undervoltage and overvoltage fault detection is not needed, the V_L and V_H pins must be tied to GND. The $\overline{UVFLT}$ and $\overline{OVFLT}$ pins may either be tied to GND or left floating.

Low Voltage Regulator

The LTC3305 has an always on regulator that provides 2.5V at the V_{REG} pin. The V_{REG} pin may be driven externally up to 5.5V. The V_{REG} pin cannot sink current and will not pull down an externally applied voltage. The regulator can source up to 3mA of current. If more than 3mA of current is drawn from the regulator, the V_{REG} voltage will drop below its undervoltage threshold, disabling the LTC3305 and terminating the balancing operation. The balancing operation restarts when the regulator recovers from its undervoltage state. In short circuit, the V_{REG} current is limited to 15mA. The V_{REG} pin should be decoupled with at least a 1µF capacitor to GND.

Thermal Shutdown

The LTC3305 has an overtemperature detect circuit that shuts down the balancing operation when the internal silicon junction temperature exceeds 155°C. The LTC3305 resumes balancing when the temperature drops to 145°C. In thermal shutdown, the low voltage regulator remains powered.

Balancing Battery Stacks with Two or Three Batteries

The LTC3305 can also be configured to balance battery stacks of two or three batteries. The state of the enable pins tells the LTC3305 to select the correct switch sequencing. For a two battery stack, the LTC3305 must be enabled with EN1 = 0 and EN2 = 1. For a three battery stack, the LTC3305 must be enabled with EN1 = 1 and EN2 = 0. The external NMOS switch arrangements for a two-battery and three-battery application are shown in Figures 3 and 4 respectively. If pin NGATE6 is unused, it must be connected to the BOOST pin. All other unused NGATE pins must be connected to V4 as shown in Figures 3 and 4.

A two battery stack is deemed balanced if the termination sense comparator senses the voltage difference between the auxiliary cell and the battery is less than $V_{TERMINATE}$ on three successive cycles when the auxiliary cell and a battery are connected using only the bottom switches.

In the case of a three battery stack, four successive cycles are required to deem the stack balanced.

OPERATION

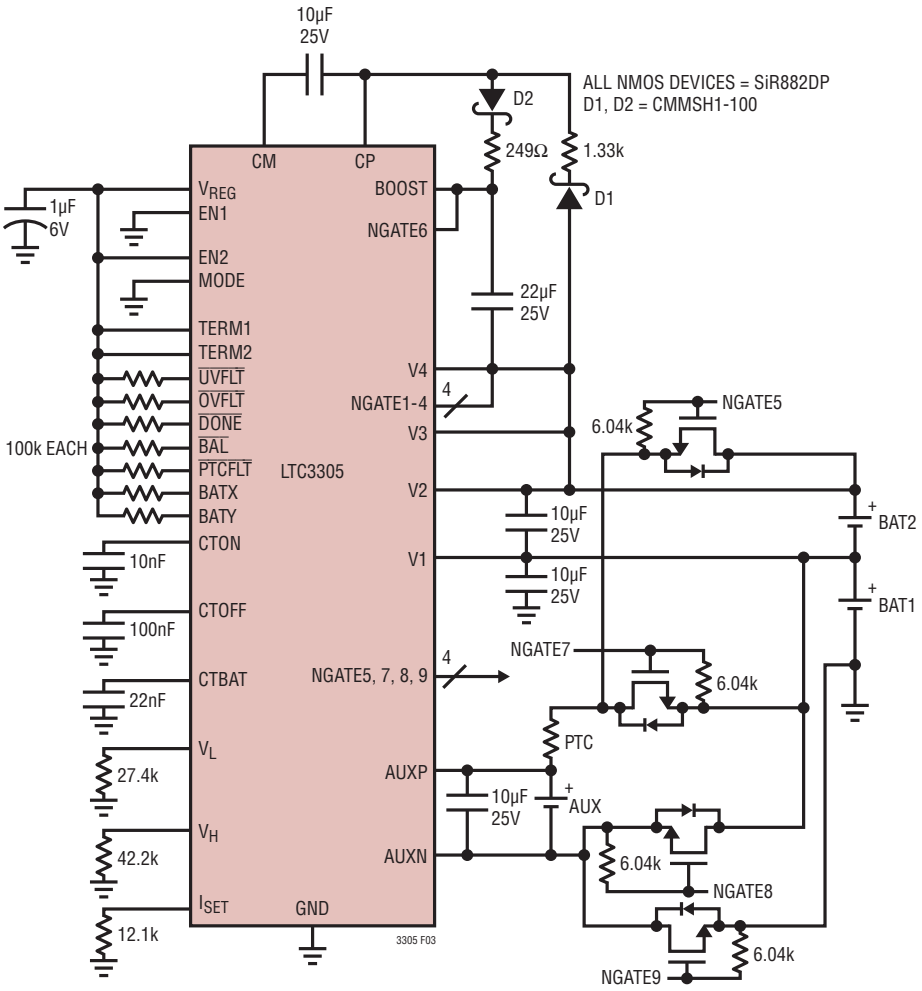


Figure 3. Two-Battery Application Showing External Switch Arrangement

OPERATION

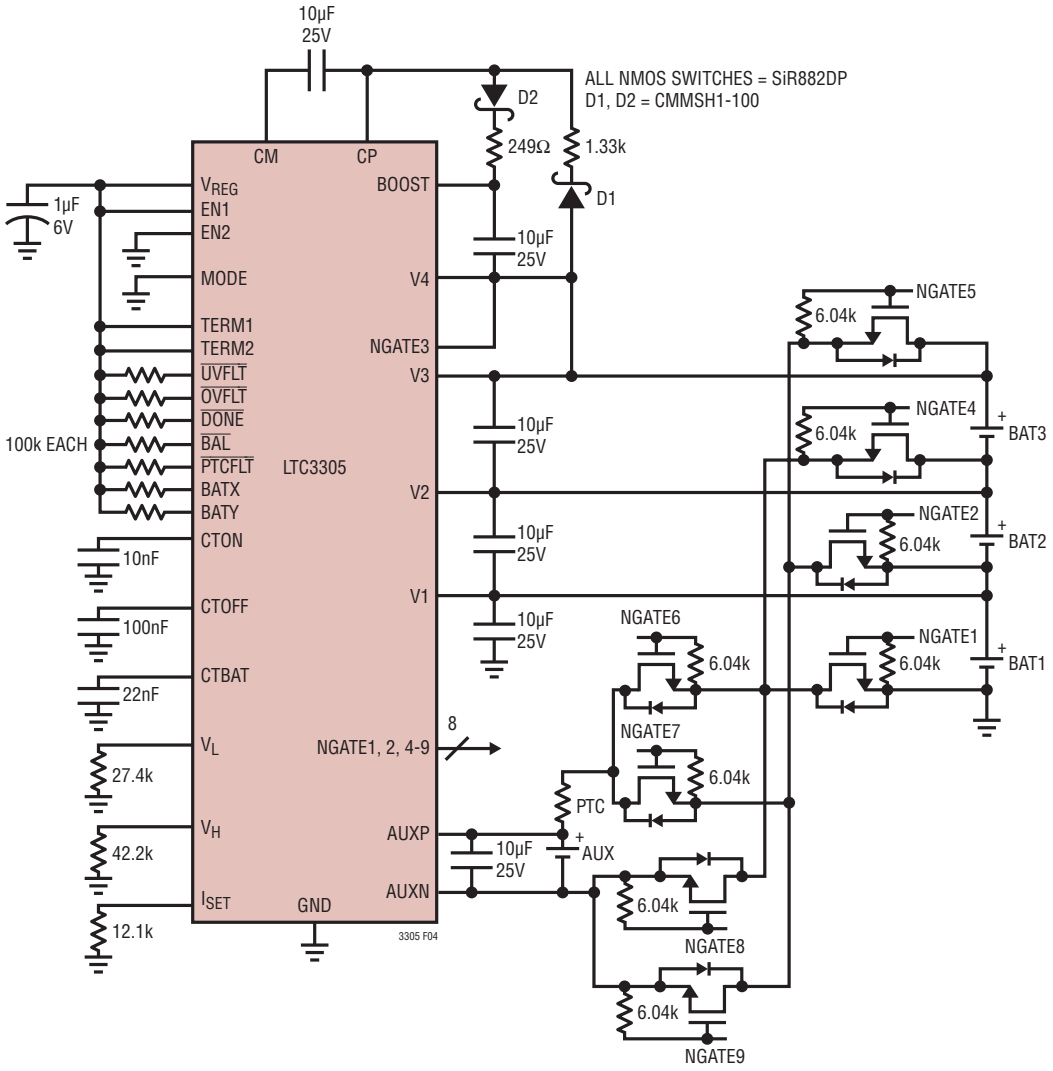


Figure 4. Three-Battery Application Showing External Switch Arrangement

APPLICATIONS INFORMATION

Selecting the PTC Thermistor

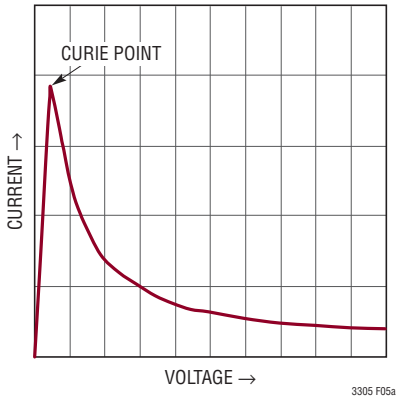
A PTC thermistor is a type of resistor with a Positive Temperature Coefficient that serves as a protection device by limiting its current above a certain threshold. The PTC device limits the peak current that transfers charge between the auxiliary cell and the battery. When the voltage across the PTC is small, the power dissipated in the PTC is small and the PTC resistance remains constant. As the voltage across the PTC increases, power dissipation in the PTC increases which causes the PTC temperature to rise. When the temperature reaches the Curie Temperature, further increases in voltage will cause the PTC resistance to increase rapidly, which limits the current through the device and thus limits the power dissipation in the PTC. This behavior is shown in the PTC Current Voltage Characteristics in Figure 5a. In this fashion the PTC serves to protect the external NMOS switches from operating outside of their SOA region.

As seen in the PTC Current Voltage Characteristics in Figure 5a, when the PTC has a small voltage or a high voltage across it, the current flowing through it is small. For small voltages, this is OK since the battery and the auxiliary cell are close to balance. For high voltages, this slows down balancing. To increase balance currents at high voltages a power resistor can be placed in parallel with the PTC device, as shown in Figure 5b. Additionally, multiple PTC resistors may be connected in parallel to increase current flow at all voltages.

PTC devices are manufactured in two styles: ceramic and poly fuse. Only a ceramic style PTC device should be used in this application. Poly fuse devices have a very limited number of lifetime trip cycles and are not suitable in a balancing application.

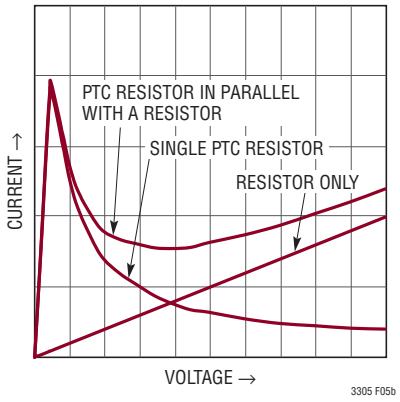
The PTC must be selected such that power dissipation through the external NMOS switches never exceeds their rated SOA power dissipation value. Refer to Table 4 for a list of recommended PTC thermistors.

PTC Current Voltage Characteristics



(a)

Increasing Current at Large Voltage



(b)

Figure 5. PTC Behavior

Table 4. Recommended Ceramic PTC Thermistors

PART NUMBER	MANUFACTURER	VOLTAGE	RESISTANCE (Ω)
PTGL7SARR47M1B51B0	Murata	16V	0.47
PTGLASARR27M1B51B0	Murata	16V	0.27
PTGLESARR15M1B51B0	Murata	16V	0.15
PTGL12AR1R2H2B51B0	Murata	30V	1.2
2381 663 51121	Vishay	30V	0.7
2381 663 51321	Vishay	30V	0.5
2381 664 52021	Vishay	30V	0.3

APPLICATIONS INFORMATION

Selecting the Auxiliary Cell

The auxiliary cell must be capable of sourcing and sinking current and withstand the maximum voltage of any individual battery in the stack. The ESR of the auxiliary cell must be small compared to the PTC thermistor. Any voltage dropped across the auxiliary cell ESR appears as an offset voltage at the input of the termination comparator.

The auxiliary cell used may be a lead-acid battery, a stacked supercapacitor, or a low leakage, high voltage capacitor. When using a supercapacitor stack, the voltage across each individual supercapacitor must not exceed its rated operating voltage.

Figure 6a shows a battery stack made of 4 batteries, each with a nominal capacity of 50Ah, but with a 10% capacity mismatch. With no balancing, the stack capacity is determined by the weakest battery in the stack and is limited to 45Ah.

In Figure 6b, a small capacity auxiliary cell, such as a supercapacitor stack, is used to balance the battery stack. When balanced the stack capacity can be made to approach the nominal capacity of 50Ah despite the 10% mismatch.

In Figure 6c, the auxiliary cell has the same capacity as the batteries in the stack. Each of the batteries in Figure 6c has a nominal capacity of only 40Ah but the stack capacity approaches 50Ah since the auxiliary cell supplements the capacity of the battery stack. Using a large capacity auxiliary cell supplements stack capacity. Smaller capacity batteries may be used in the stack which helps reduce system costs.

Precharging the Auxiliary Cell

When using stacked supercapacitors or a single high voltage capacitor as the auxiliary cell, the auxiliary cell may be initially discharged with a voltage of 0V. At startup, a large voltage exists across the PTC resistor, which will cause the PTC resistance to increase. This limits the current and hence the charge transfer between the auxiliary cell and the battery it is connected to. The auxiliary cell will be charged very slowly with an indeterminate time, as it sequentially connects to each battery in the stack. Once the auxiliary cell has been charged to a point where the PTC device operates as a low resistance device, the balancing process is sped up.

A more time efficient solution is to precharge the auxiliary cell to the average voltage of the batteries in the stack. Figure 7a shows a circuit using a high voltage buck regulator to precharge the auxiliary cell to V4/4 volts. NMOS devices N2A and N2B eliminate a parasitic charging path from BATTERY1 to the auxiliary cell when AUXN is connected to GND through N10. Figures 7b and 7c are scope photos showing a complete precharging and balancing operation.

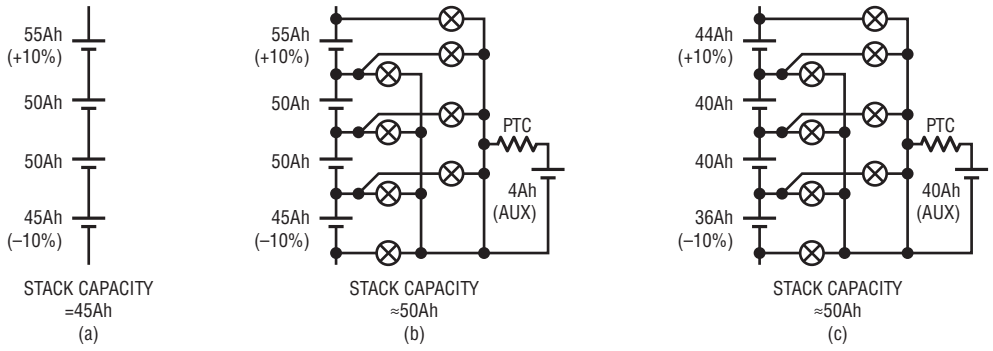
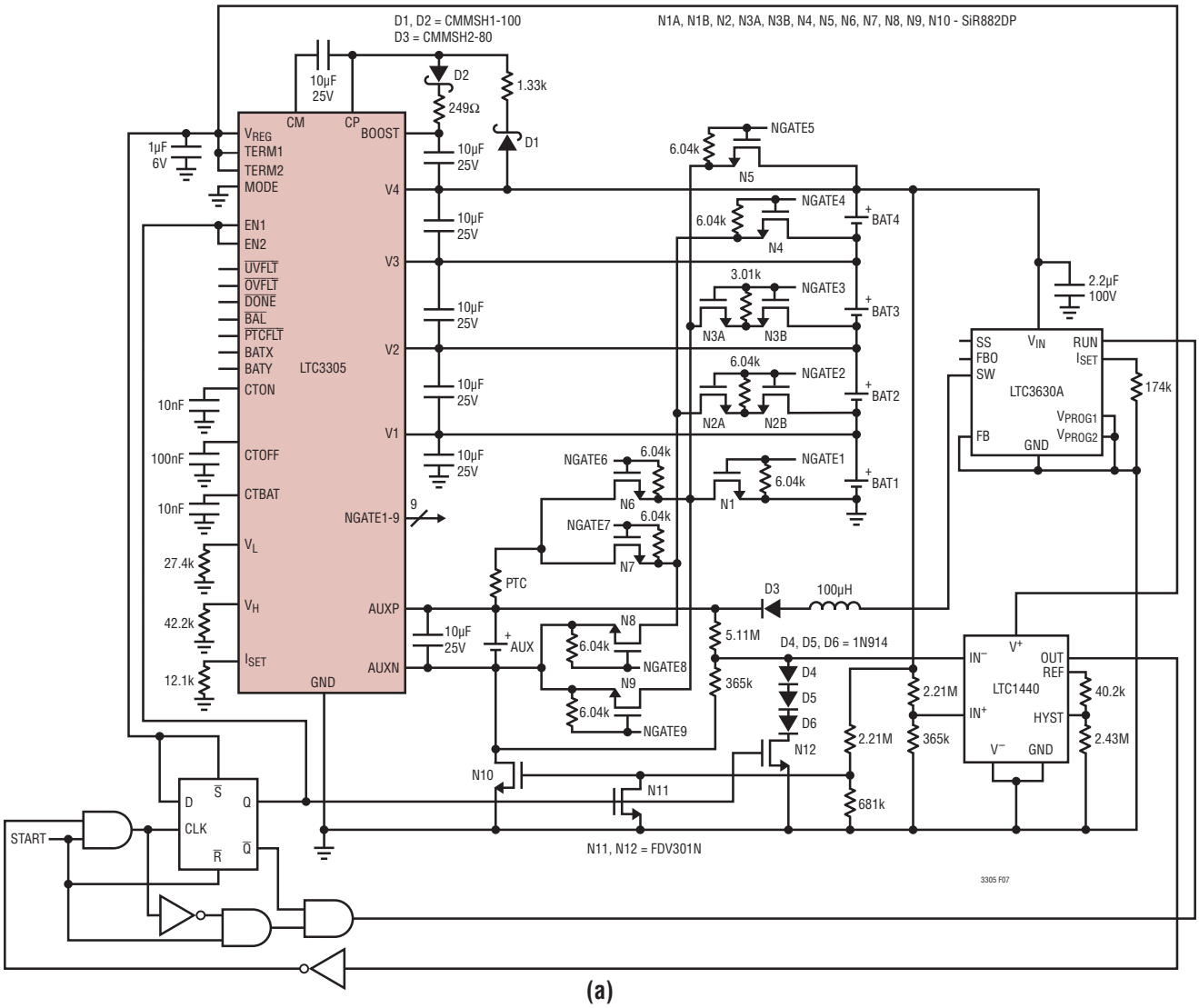


Figure 6. Increasing Stack Capacity with an Auxiliary Cell

APPLICATIONS INFORMATION



(a)

BAT1, BAT2, BAT3, BAT4, AUXP-AUXN = 2V/DIV
AUXN = 10V/DIV; START, EN_3305 = 5V/DIV
TIME = 20s/DIV

(b)

AUXP-AUXN = 2V/DIV
AUXN = 10V/DIV; START, EN_3305 = 5V/DIV
TIME = 5s/DIV

(c)

Figure 7. Precharging the Auxiliary Cell Using the LTC3630A and LTC1440

APPLICATIONS INFORMATION

Selection of External NMOS Switches

The external NMOS switches must be capable of withstanding a reverse voltage equal to the battery stack voltage. They should also be capable of carrying DC current up to the PTC thermistor trip point. The maximum power dissipated in the NMOS should not cause it to operate outside of its Safe Operating Area. Refer to Table 5 for a list of recommended NMOS switches.

Table 5. Recommended NMOS Switches

PART NUMBER	MANUFACTURER	$I_{DS(MAX)}$	$V_{DC(MAX)}$
SiR882DP	Vishay	60A	100V
SiS892DN	Vishay	25A	100V
IPD70N10S3-12	Infineon	70A	100V
IPB35N10S3L-26	Infineon	35A	100V
RJK1051DPB	Renesas	60A	100V
RJK1054DPB	Renesas	92A	100V

Programming NMOS Turn On

The NMOS switches are turned on by developing a voltage across an external resistor from the gate to the source. The current through the resistor is delivered from the NGATE pins and is programmed by the current at the I_{SET} pin. The internal current sources that provide the NGATE pin currents operate from the V4 and BOOST supplies as shown in the Block Diagram. The BOOST pin voltage is regulated at 8.45V greater than V4. It is recommended that the gate turn on voltage be set to no more than 7.5V. The current flowing through the gate turn on resistor connected to the NGATE3 pin is given by:

$$I_{NGATE3} = \frac{26.4V}{R_{ISET}}$$

The current flowing through the other NGATE pins is given by:

$$I_{NGATE} = \frac{13.2V}{R_{ISET}}$$

The NGATE3 current has a programmed range from 1mA to 3mA. All other NGATE currents have a programmed range from 500µA to 1.5mA.

The NGATE current initially charges the gate capacitor of the NMOS device to turn it on. The external gate source resistor maintains a constant gate to source voltage on the NMOS device. Programming a higher current reduces the NMOS device turn on time. Programming a large gate source voltage reduces the on resistance of the NMOS device. During turn off, the gate capacitor discharges through the gate source resistor.

Programming Undervoltage and Overvoltage Thresholds

Referring to the Block Diagram, the voltage at the I_{SET} pin is servoed to 1.2V. An external resistor, R_{ISET}, from this pin to GND programs a current which is divided down and mirrored to the V_L and V_H pins. The I_{SET} pin current has a programmed range from 50µA to 150µA.

The I_{SET} pin current is given by:

$$I_{ISET} = \frac{1.2V}{R_{ISET}}$$

The current out of the V_L and V_H pins is given by:

$$I_{VL} = I_{VH} = \frac{I_{ISET}}{3}$$

External resistors R_{VL} from the V_L pin to GND and R_{VH} from the V_H pin to GND program the undervoltage and overvoltage thresholds for each battery. The undervoltage threshold for a battery is given by:

$$V_{BAT,UV} = 4V \bullet \frac{R_{VL}}{R_{ISET}}$$

The overvoltage threshold for a battery is given by:

$$V_{BAT,OV} = 4V \bullet \frac{R_{VH}}{R_{ISET}}$$

Programming the t_{BAT} Parameter

The t_{BAT} parameter is programmed using a capacitor from the CTBAT pin to GND. t_{BAT} is given by:

$$t_{BAT} = 5sec \bullet \frac{C_{TBAT}}{10nF}$$

A C0G type capacitor is recommended due to its superior temperature characteristics.

Programming the t_{ON} and t_{OFF} Parameters

The t_{ON} parameter is programmed by a capacitor from the CTON pin to GND. t_{ON} is given by:

$$t_{ON} = 0.48hrs \bullet \frac{C_{TON}}{10nF}$$

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The t_{OFF} parameter is programmed by a capacitor from the CTOFF pin to GND. t_{OFF} is given by:

$$t_{OFF} = 0.48hrs \bullet \frac{C_{TOFF}}{10nF}$$

C0G type capacitors are recommended due to their superior temperature characteristics.

In the continuous operation mode (MODE = 1), the CTON and CTOFF pins are unused and should be connected to GND.

Selecting Charge Pump Components

Referring to Figure 2, recommended values for R1, R2 and C_{FLY} are 249Ω, 1.33k & 10µF respectively for all applications. For applications in which V4 is no lower than 32V a 10µF capacitor is recommended for C_{BOOST}. For applications which may have lower voltages at V4, the recommended value for C_{BOOST} is 22µF. Schottky diodes with a breakdown voltage larger than the maximum V4 voltage are recommended for diodes D1 and D2.

Selecting Decoupling Capacitors

Decoupling capacitors of at least 10µF must be placed across each battery, from the BOOST pin to V4 and from the AUXP pin to the AUXN pin. These capacitors must be placed as close as possible to the LTC3305. The capacitors must be capable of withstanding the maximum voltage across each battery. Capacitors with an X5R or X7R type dielectric should be used.

Thermal Considerations and Limiting On-Chip Power Dissipation

Excessive on-chip power dissipation will cause the LTC3305 to enter thermal shutdown. It is important to understand the source of the power dissipation and how power dissipation can be reduced. The two contributions of on-chip power dissipation on the LTC3305 that may be controlled by the user are the loading on the low voltage regulator and the power dissipated through the current sources that provide the NGATE pin currents.

The low voltage linear regulator provides a 2.5V output. Any current provided by the regulator will cause power dissipation in the internal switch connected from V4 to V_{REG}, which causes die temperature to increase. In Figure 8, an external switching regulator generates a 3.3V rail that back drives the V_{REG} pin and provides power to the external microprocessor and other low voltage circuits. There is no on-chip loading on the V_{REG} pin and thus no on chip power dissipation in the low voltage regulator.

In Figure 8, external resistors R1, R2, R3, R4, and R5 are in series with the on-chip current sources that provide NGATE pin current. These resistors reduce the voltage across the on-chip current sources and thus reduce on-chip power dissipation. As an example, the current source at NGATE1 delivers current from the V4 pin. When this current source is turned on, the voltage across it is V4-V_{NGATE1}. For a typical application with V4 = 52.8V, programmed I_{NGATE} = 506µA and V_{NGATE1} = 6.12V, the on-chip power dissipated in the current source is 23mW. In Figure 8, resistor R1 operates with approximately 30.5V across it. The on-chip power dissipated in the current source is reduced to approximately 8mW. In similar fashion resistors R2, R3, R4, and R5 reduce the on-chip power dissipation on the respective current sources. When choosing these resistors it is recommended to have the internal current sources biased with at least 6V across them under all operating conditions. Power dissipation through the on-chip current sources may be further reduced by programming a lower gate current through the NGATE pins.

Balancing Battery Stacks with more than Four Batteries

To balance battery stacks that have more than four batteries, multiple LTC3305 devices may be stacked together. In this scenario, it is recommended that each LTC3305 be run in continuous mode and at least one battery in each sub-stack of four is common to two LTC3305s. Each LTC3305 needs an auxiliary cell for the balancing operation. Figure 9 shows an eight battery stack being balanced using three LTC3305 devices connected together. Figure 10 shows a stack of six batteries being balanced using two LTC3305 devices. To balance a battery stack with *n* batteries, the minimum number of LTC3305 devices required is [(*n*-1)/3] rounded up to the nearest integer. In this calculation, each LTC3305 is assumed to be used in a four-battery configuration and at least one battery interleaves two LTC3305 devices.

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When multiple LTC3305 devices are stacked, the logic output pins may need to be level shifted and ground referred. In Figure 9, optical isolators are used for level shifting.

Figure 11 shows an application in which an eight battery stack is balanced using two LTC3305 devices and two auxiliary cells. BAT1, BAT2, BAT3, and BAT4 are balanced to each other using the lower LTC3305 whereas BAT5, BAT6, BAT7, and BAT8 are balanced to each other by the upper LTC3305.

PCB Considerations

In operation the LTC3305 can dissipate large amounts of power which can increase die temperature and cause the part to enter thermal shutdown. The exposed pad of LTC3305 must be well soldered to the PCB to provide adequate heat sinking. The exposed pad also provides an electrical GND to the LTC3305.

The no-connect pin on the LTC3305 must be soldered to a pad on the PCB and must be electrically isolated from any other circuit node.

The trace that connects the AUXP pin to the positive terminal of the auxiliary source must be as close to the auxiliary source positive terminal as possible. Otherwise the trace impedance adds to the ESR of the auxiliary cell which manifests itself as an offset at the internal termination comparator.

The V1, V2, V3 and V4 traces must be Kelvin connected directly to the battery terminal and must not share a common trace through which high balance current will flow. Any voltage drop in these traces also manifests itself as an offset voltage at the termination comparator input.

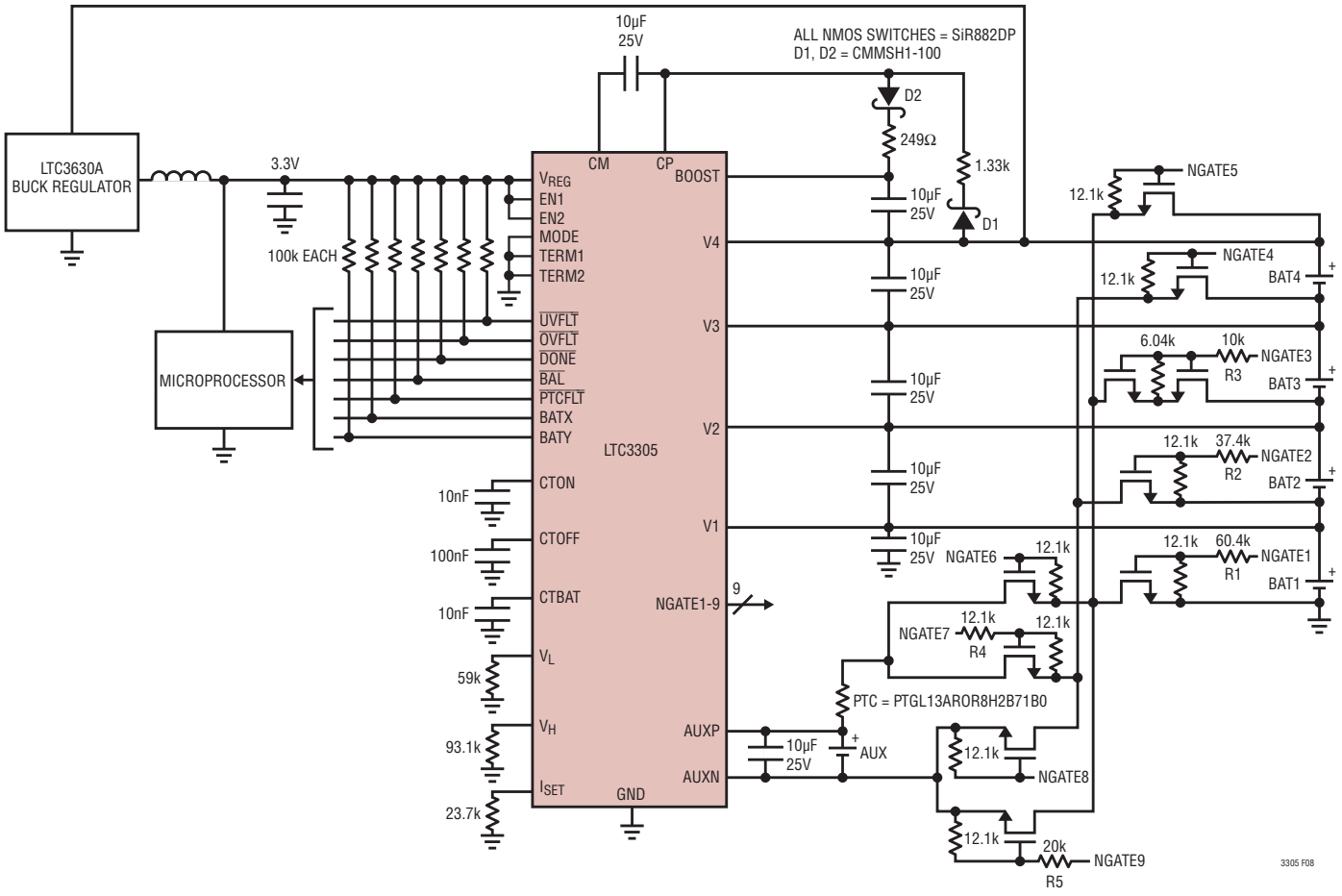

Figure 8. 4-Battery Application with External Resistors to Limit Power Dissipation

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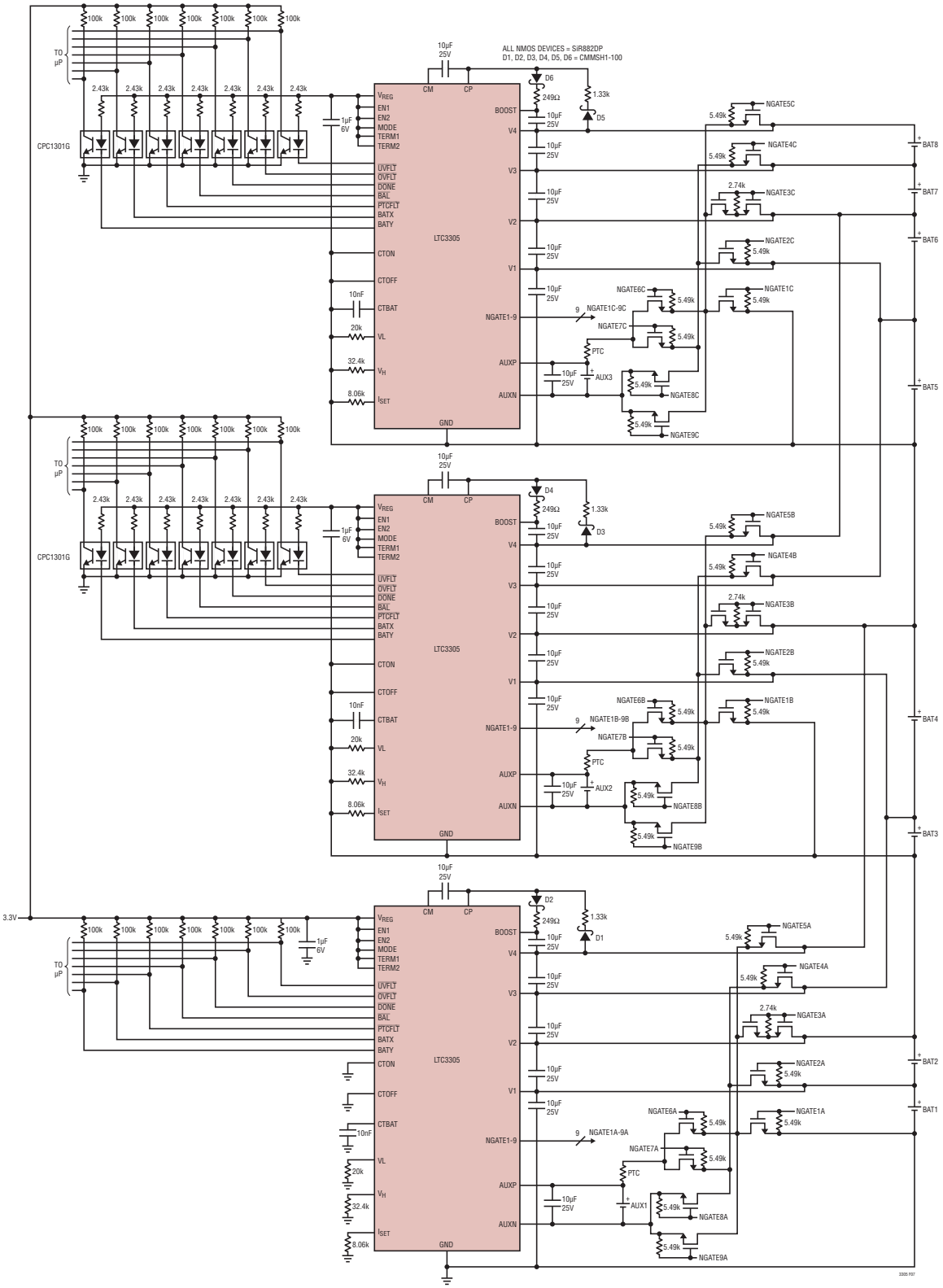


Figure 9. Three LTC3305 Devices Connected to Balance Eight Lead-Acid Batteries

APPLICATIONS INFORMATION

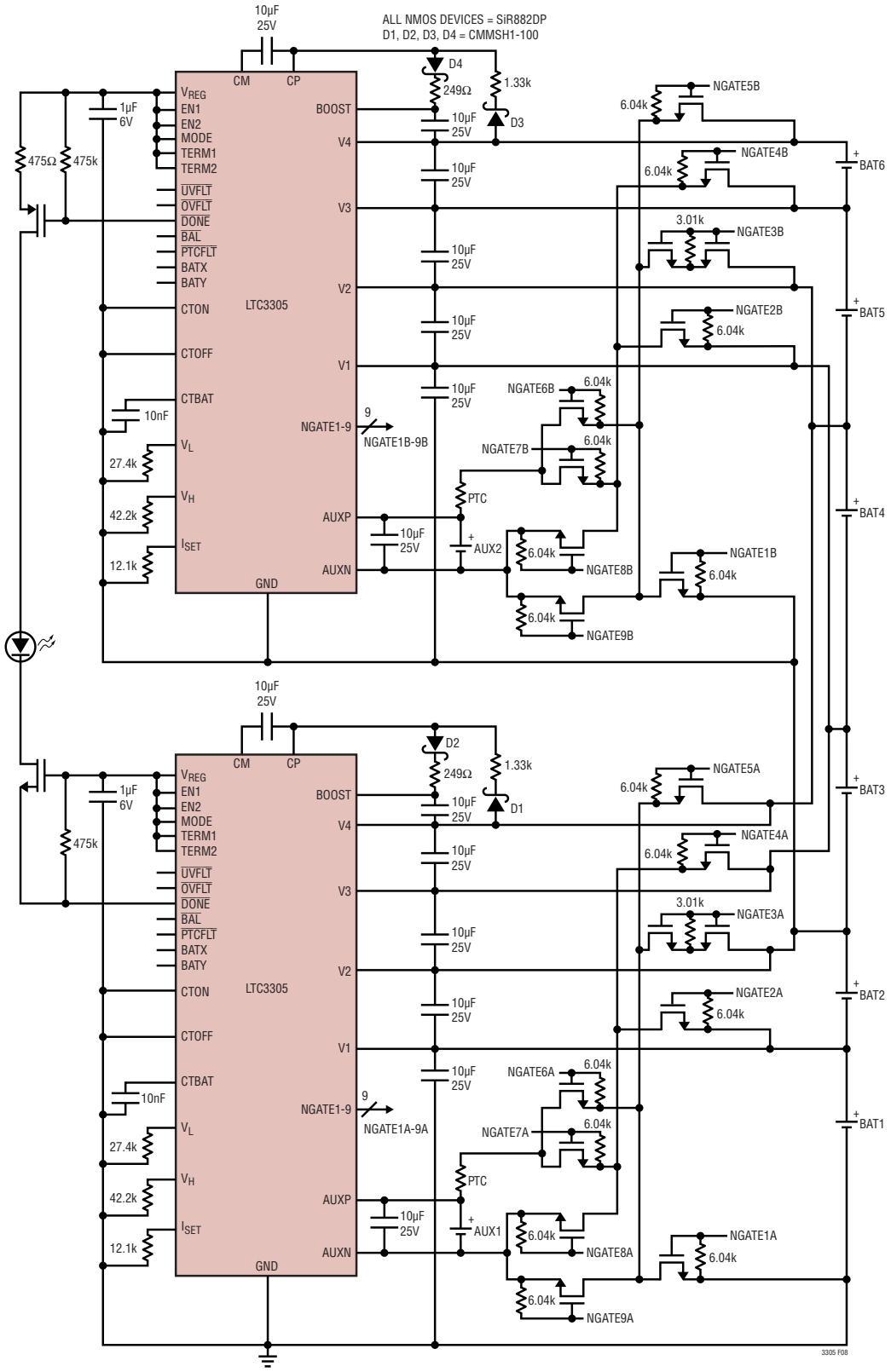


Figure 10. Two LTC3305 Devices Connected to Balance Six Lead-Acid Batteries with AND'd DONE Indicator

APPLICATIONS INFORMATION

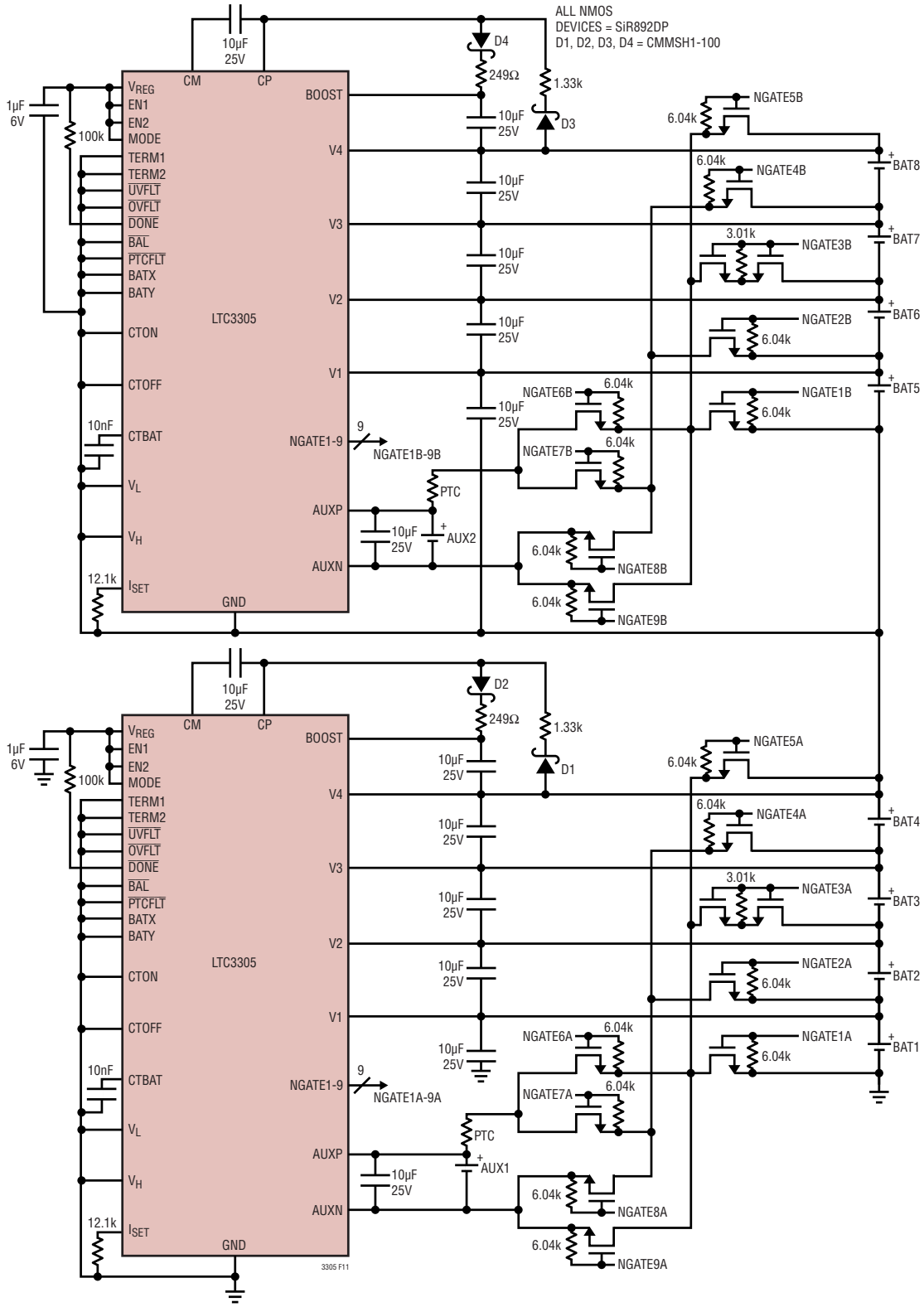
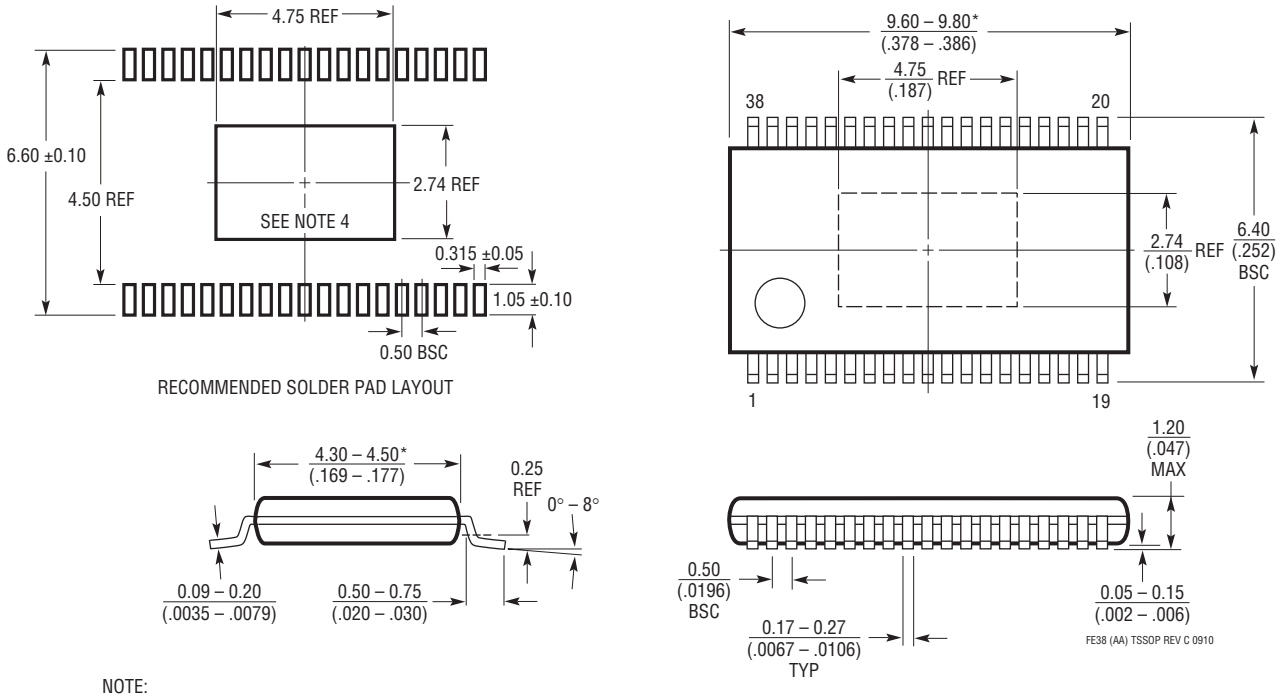


Figure 11. Eight Battery Balancer Using Two LTC3305 Devices

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3305#packaging for the most recent package drawings.

FE Package
38-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1772 Rev C)
Exposed Pad Variation AA



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/15	Added timer mode section.	13
		Modified Figure 6 schematic.	16
		Modified Figure 8 schematic.	22
		Modified Figure 9 schematic.	23
B	03/16	Updated Feature bulleted items and description	1
		Updated Application schematic	1
		Enhanced Operation section	11