17MHz to 170MHz Resistor Set SOT-23 Oscillator

FEATURES

- **One External Resistor Sets the Frequency**
- **Fast Start-Up Time: 100µs Typical**
- **Frequency Range: 17MHz to 170MHz**
- Frequency Error ±0.5% Typ 17MHz to 170MHz (T_A = 0°C to 70°C, Over All Settings)
- ±20ppm/°C Temperature Stability
- Rise Time: 0.5ns, C_L = 5pF
- Timing Jitter: 7.2ps RMS at 170MHz
- 50% ±2.5% Duty Cycle
- 6mA Typical Supply Current, f_{OSC} = 100MHz
- CMOS Output Drives 500Ω Load (V_S = 3V)
- Operates from a Single 2.7V to 5.5V Supply
- Low Profile (1mm) ThinSOT™ Package

APPLICATIONS

- High Frequency Precision Oscillator
- High Speed Data Bus Clock
- Fixed Crystal Oscillator Replacement
- Ceramic Oscillator Replacement

DESCRIPTION

The LTC®6905 precision, programmable silicon oscillator is easy to use and occupies very little board space. It requires only a single resistor to set the output frequency from 17MHz to 170MHz with a typical frequency error of 0.5% or less.

The LTC6905 operates with a single 2.7V to 5.5V power supply and provides a rail-to-rail, 50% duty cycle square wave output. The CMOS output driver ensures fast rise/fall times and rail-to-rail switching. Operation is simple: A single resistor, R_{SET}, between 10k to 25k is used to set the frequency, and an internal three-state divider (DIV input) allows for division of the master clock by 1, 2 or 4, providing three frequencies for each R_{SET} value.

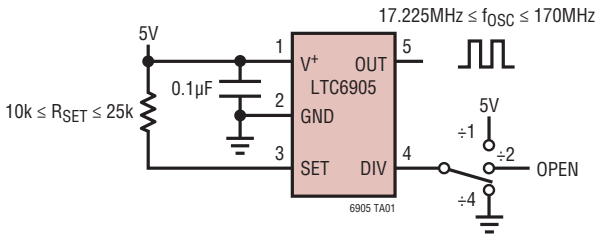
The LTC6905 features a proprietary feedback loop that linearizes the relationship between R_{SET} and frequency, eliminating the need for tables to calculate frequency. The oscillator can be easily programmed using the simple formula outlined below:

$$f_{OSC} = \left(\frac{168.5MHz \bullet 10k\Omega}{R_{SET}} + 1.5MHz\right) \bullet \frac{1}{N},\ N = \begin{cases} 1, \text{ DIV Pin} = V^+ \\ 2, \text{ DIV Pin} = \text{Open} \\ 4, \text{ DIV Pin} = \text{GND} \end{cases}$$

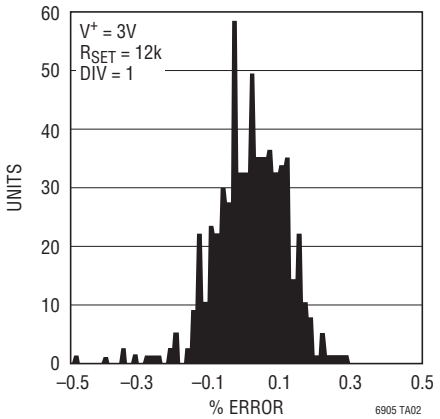
For higher accuracy, fixed frequency versions that include an internal frequency-setting resistor, see the LTC6905-XXX Series data sheet.

TYPICAL APPLICATION

Basic Connection



Typcial Distribution of Frequency Error, T_A = 25°C



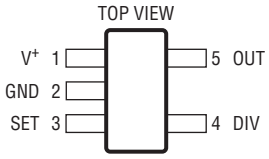
NOTE: RESISTOR, R_{SET}, TOLERANCE WILL ADD TO THE FREQUENCY ERROR

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V^+) to GND .....–0.3V to 6V
DIV to GND ..... –0.3V to (V^+ + 0.3V)
SET to GND ..... –0.3V to (V^+ + 0.3V)
Output Short-Circuit Duration (Note 6) ..... Indefinite
Operating Temperature Range (Note 7)
LTC6905C, I .....–40°C to 85°C
LTC6905H .....–40°C to 125°C
LTC6905MP .....–55°C to 125°C
Specified Temperature Range (Note 8)
LTC6905C ..... 0°C to 70°C
LTC6905I.....–40°C to 85°C
LTC6905H .....–40°C to 125°C
LTC6905MP .....–55°C to 125°C
Storage Temperature Range.....–65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



S5 PACKAGE
5-LEAD PLASTIC SOT-23

T_{JMAX} = 125°C, θ_{JA} = 160°C/W

ORDER INFORMATION

LEAD FREE FINISH

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6905CS5#TRMPBF	LTC6905CS5#TRPBF	LTBJC	5-Lead Plastic SOT-23	0°C to 70°C
LTC6905IS5#TRMPBF	LTC6905IS5#TRPBF	LTBJC	5-Lead Plastic SOT-23	–40°C to 85°C
LTC6905HS5#TRMPBF	LTC6905HS5#TRPBF	LTBJC	5-Lead Plastic SOT-23	–40°C to 125°C
LTC6905MPS5#TRMPBF	LTC6905MPS5#TRPBF	LTDVW	5-Lead Plastic SOT-23	–55°C to 125°C

LEAD BASED FINISH

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6905MPS5#TRM	LTC6905MPS5#TR	LTDVW	5-Lead Plastic SOT-23	–55°C to 125°C

TRM = 500 pieces. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C or as noted. V^+ = 2.7V to 5.5V, R_L = 15k, C_L = 5pF, Pin 4 = V^+ unless otherwise noted. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Δf	Frequency Accuracy (Notes 2, 9)	V^+ = 2.7V, 17.225MHz < f < 170MHz				±0.5	±1.4	%
		V^+ = 5V, 17.225MHz < f < 170MHz					±2.2	%
		LTC6905CS5						
		V^+ = 2.7V, 17.225MHz < f < 170MHz		●			±1.7	%
		V^+ = 5V, 17.225MHz < f < 170MHz		●			±2.5	%
		LTC6905MPS5 (25°C ≤ T ≤ 125°C), LTC6905HS5 (25°C ≤ T ≤ 125°C), LTC6905IS5 (25°C ≤ T ≤ 85°C)						
		V+ = 2.7V, 17.225MHz < f < 170MHz					±1.9	%
		V+ = 5V, 17.225MHz < f < 170MHz					±2.9	%
		LTC6905MPS5 (–55°C < T < 125°C), LTC6905HS5 (–40°C ≤ T ≤ 125°C), LTC6905IS5 (–40°C ≤ T ≤ 85°C)						
		V^+ = 2.7V, 17.225MHz < f < 170MHz		●			±3.5	%
		V^+ = 5V, 17.225MHz < f < 170MHz		●			±3.5	%
Δf	Frequency Accuracy (Notes 2, 9)							
R_{SET}	Frequency-Setting Resistor Range				10		25	kΩ
f_{MAX}	Maximum Frequency	Pin 4 = V^+, N = 1				170		MHz
f_{MIN}	Minimum Frequency	Pin 4 = 0V, N = 4				17.225		MHz
Δf/ΔT	Freq Drift Over Temp (Note 2)	R_{SET} = 10k		●		±20		ppm/°C
Δf/ΔV	Freq Drift Over Supply (Notes 2, 9)	V^+ = 2.7V to 5.5V, R_{SET} = 10k		●		0.5		%/V
	Peak-to-Peak Timing Jitter (Note 3)					0.8		%
	Long-Term Stability of Output Frequency					300		ppm/√kHr
	Duty Cycle			●	47.5	50	52.5	%
V^+	Operating Supply Range			●	2.7		5.5	V
I_S	Power Supply Current	R_{SET} = 10k, N = 1, R_L = ∞, f_{OSC} = 170MHz, C_L = 5pF	V^+ = 5.5V	●		14	20	mA
			V^+ = 2.7V	●		7	12	mA
		R_{SET} = 20k, N = 4, R_L = ∞, f_{OSC} = 21.44MHz, C_L = 5pF	V^+ = 5.5V	●		5	7	mA
			V^+ = 2.7V	●		3	5	mA
V_{IH}	High Level DIV Input Voltage			●	V^+ – 0.15			V
V_{IL}	Low Level DIV Input Voltage			●			0.2	V
I_{DIV}	DIV Input Current (Note 4)	Pin 4 = V^+	V^+ = 5.5V	●		15	40	µA
		Pin 4 = 0V	V^+ = 5.5V		–40	–11		µA
V_{OH}	High Level Output Voltage (Note 4)	V^+ = 5.5V, Pin 4 = 0V	I_{OH} = –1mA	●	5.25	5.45		V
			I_{OH} = –4mA	●	5.20	5.30		V
		V^+ = 2.7V, Pin 4 = 0V	I_{OH} = –1mA	●	2.5	2.6		V
			I_{OH} = –4mA	●	2.4	2.4		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C or as noted. V^+ = 2.7V to 5.5V, R_L = 15k, C_L = 5pF, Pin 4 = V^+ unless otherwise noted. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Low Level Output Voltage (Note 4)	V^+ = 5.5V, Pin 4 = 0V, I_{OL} = 1mA	●		0.05	0.25	V
		V^+ = 5.5V, Pin 4 = 0V, I_{OL} = 4mA	●		0.2	0.3	V
		V^+ = 2.7V, Pin 4 = 0V, I_{OL} = 1mA	●		0.1	0.3	V
		V^+ = 2.7V, Pin 4 = 0V, I_{OL} = 4mA	●		0.4	0.5	V
t_r, t_f	OUT Rise/Fall Time (Note 5)				0.5		ns
V_{SET}	Voltage at R_{SET} Pin	V^+ = 5.5V	●	4.27	4.5	4.73	V
		V^+ = 2.7V	●	1.61	1.7	1.79	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Frequency accuracy is defined as the deviation from the f_{OSC} equation. Accuracy is tested with DIV = V^+, N = 1 and other divide ratios are guaranteed by design.

Note 3: Jitter is the ratio of the peak-to-peak distribution of the period to the mean of the period. This specification is based on characterization and is not 100% tested.

Note 4: To conform with the Logic IC Standard convention, current out of a pin is arbitrarily given as a negative value.

Note 5: Output rise and fall times are measured between the 10% and 90% power supply levels.

Note 6: A heat sink may be required to keep the junction temperature below the absolute maximum when the output is shorted indefinitely.

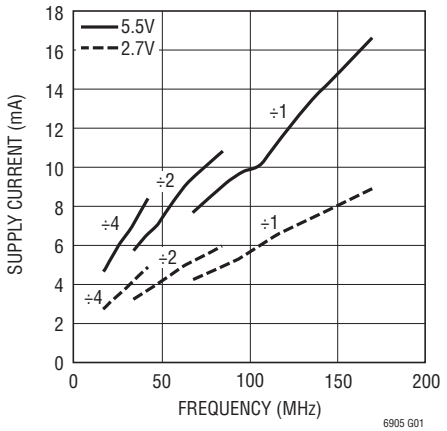
Note 7: The LTC6905C is guaranteed functional over the operating temperature range.

Note 8: The LTC6905C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6905C-XXX is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6905I-XXX is guaranteed to meet specified performance from –40°C to 85°C.

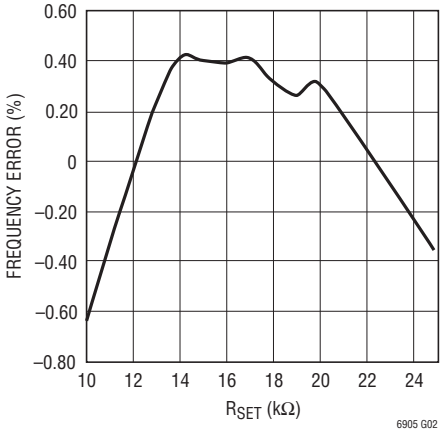
Note 9: The LTC6905 is optimized for the performance with a 3V power supply voltage. Please consult LTC Marketing for parts optimized for 5V operation.

TYPICAL PERFORMANCE CHARACTERISTICS

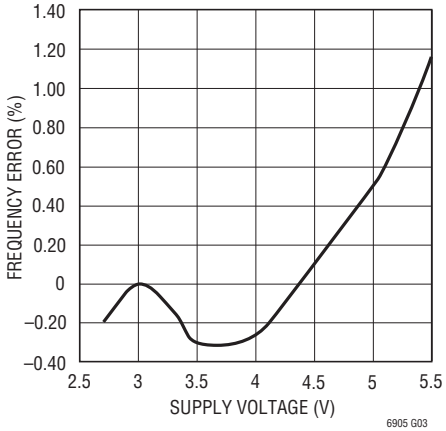
Supply Current vs Frequency



Frequency Error vs R_{SET}

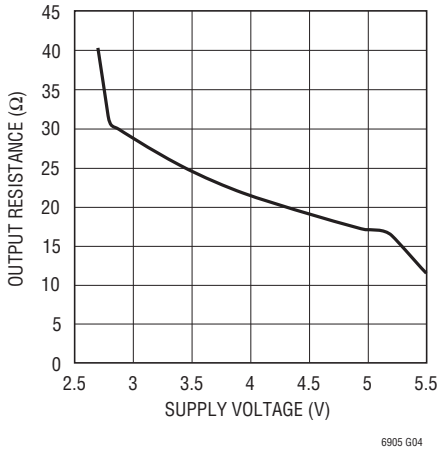


Frequency Error vs Supply Voltage

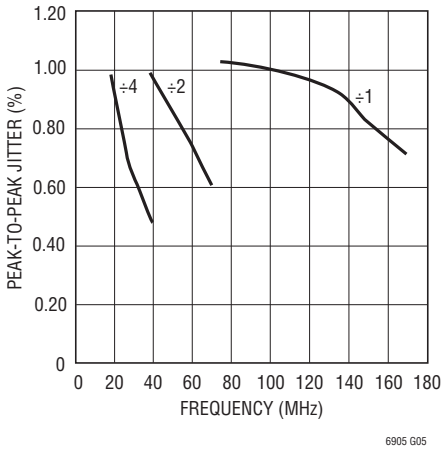


TYPICAL PERFORMANCE CHARACTERISTICS

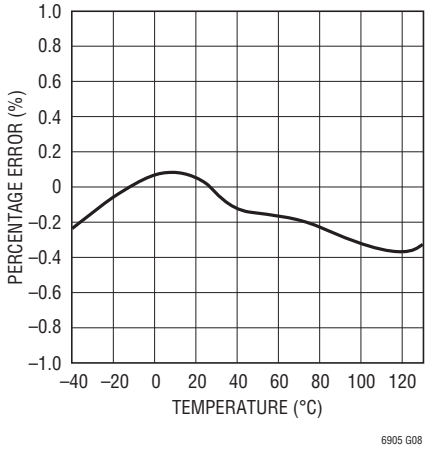
R_{OUT} vs V^+



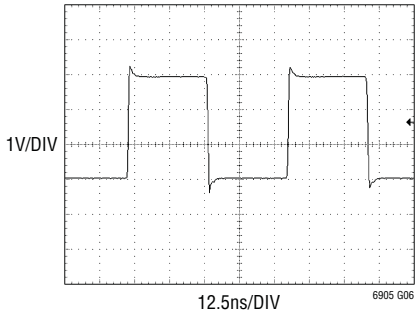
Jitter vs Frequency



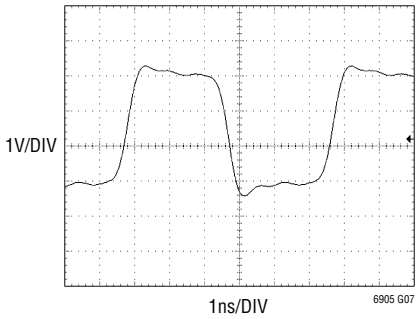
Frequency vs Temperature



LTC6905 Output Operating at 17.5MHz, V_S = 3V



LTC6905 Output Operating at 170MHz, V_S = 3V



PIN FUNCTIONS

V^+ (Pin 1): Voltage Supply ($2.7V \le V^+ \le 5.5V$). This supply must be kept free from noise and ripple. It should be bypassed directly to the GND (Pin 2) with a 0.1µF capacitor or higher.

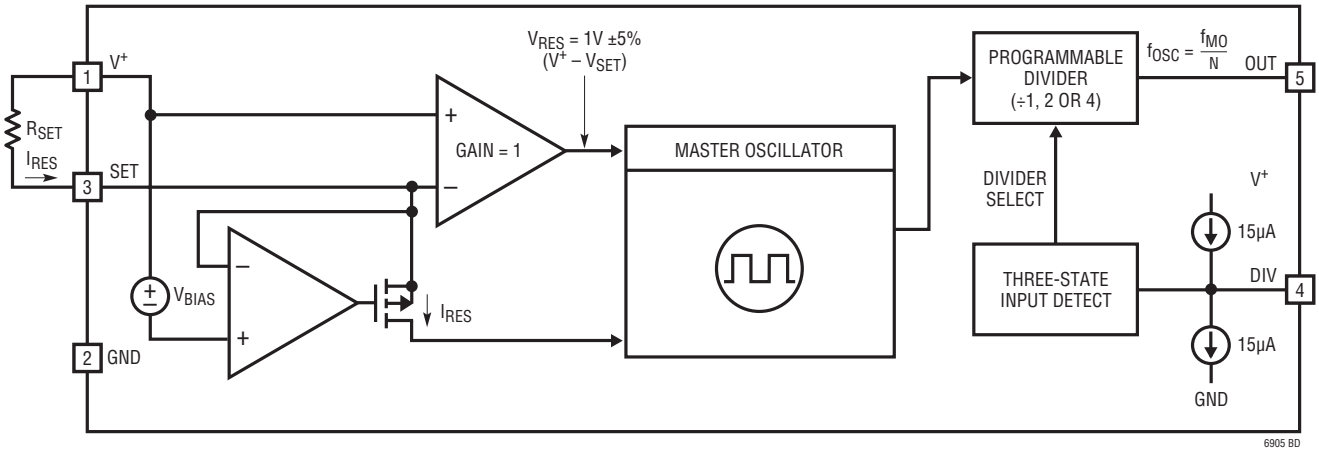
GND (Pin 2): Ground. Should be tied to a ground plane for best performance.

SET (Pin 3): Frequency-Setting Resistor Input. The value of the resistor connected between this pin and V^+ determines the oscillator frequency. The voltage on this pin is held by the LTC6905 to approximately 1V below the V^+ voltage. For best performance, use a precision metal film resistor with a value between 10k and 25k and limit the capacitance on this pin to less than 10pF.

DIV (Pin 4): Divider-Setting Input. This three-state input selects among three divider settings, determining the value of N in the frequency equation. Pin 4 should be tied to V^+ for the ÷1 setting, the highest frequency range. Floating Pin 4 divides the master oscillator by 2. Pin 4 should be tied to GND for the ÷4 setting, the lowest frequency range. To detect a floating DIV pin, the LTC6905 attempts to pull the pin toward midsupply. This is realized with two internal current sources, one tied to V^+ and Pin 4 and the other one tied to ground and Pin 4. Therefore, driving the DIV pin high requires sourcing approximately 15µA. Likewise, driving DIV low requires sinking 11µA. When Pin 4 is floated, it should be bypassed by a 1nF capacitor to ground or it should be surrounded by a ground shield to prevent excessive coupling from other PCB traces.

OUT (Pin 5): Oscillator Output. This pin can drive 5kΩ and/or 5pF loads. For larger loads, refer to the Applications Information section.

BLOCK DIAGRAM



THEORY OF OPERATION

As shown in the Block Diagram, the LTC6905's master oscillator is controlled by the ratio of the voltage between the V^+ and SET pins and the current entering the SET pin (I_{RES}). The voltage on the SET pin is forced to approximately 1V below V^+ by the PMOS transistor and its gate bias voltage.

A resistor R_{SET}, connected between the V^+ and SET pins, "locks together" the voltage ($V^+ – V_{SET}$) and current, I_{RES}, variation. This provides the LTC6905's high precision. The master oscillation frequency reduces to:

$$f_{MO} = \frac{168.5MHz \bullet 10k\Omega}{R_{SET}} + 1.5MHz$$

To extend the output frequency range, the master oscillator signal is divided by 1, 2 or 4 before driving OUT (Pin 5). The LTC6905 is optimized for use with resistors between 10k and 25k, corresponding to oscillator frequencies between 17.225MHz and 170MHz. The divide-by value is determined by the state of the DIV input (Pin 4). Tie DIV to V^+ or drive it to within 0.4V of V^+ to select ÷1. This is the highest frequency range, with the master output frequency passed directly to OUT. The DIV pin may be floated or driven to midsupply to select ÷2, the intermediate frequency range. The lowest frequency range, ÷4, is selected by tying DIV to GND or driving it below 0.5V. Figure 1 shows the relationship between R_{SET}, divider setting and output frequency, including the overlapping frequencies.

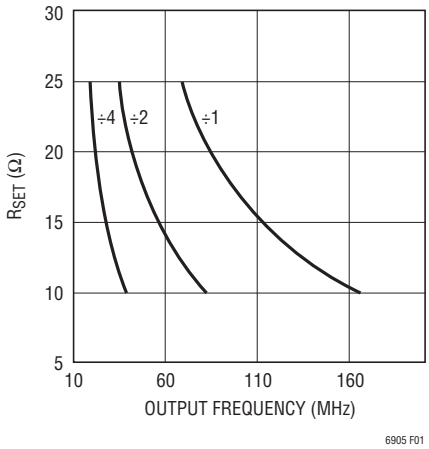


Figure 1. R_{SET} vs Output Frequency

APPLICATIONS INFORMATION

SELECTING THE DIVIDER SETTING AND RESISTOR

The LTC6905's master oscillator has a frequency range spanning 68.9MHz to 170MHz. A programmable divider extends the frequency range from 17.225MHz to 170MHz. Table 1 describes the recommended frequencies for each divider setting. Note that the ranges overlap; at some frequencies there are two divider/resistor combinations that result in the same frequency. Choosing a higher divider setting will result in less jitter at the expense of slightly higher supply current.

Table 1. Frequency Range vs Divider Setting

DIVIDER SETTING			FREQUENCY RANGE
÷1	⇒	DIV (Pin 4) = V^+	68.9MHz to 170MHz
÷2	⇒	DIV (Pin 4) = Floating	34.45MHz to 85MHz
÷4	⇒	DIV (Pin 4) = GND	17.225MHz to 43MHz

After choosing the proper divider setting, determine the correct frequency-setting resistor. Because of the linear correspondence between oscillation period and resistance, a simple equation relates resistance with frequency.

$$R_{SET} = 10k \bullet \left(\frac{168.5MHz}{f_{OSC} \bullet N - 1.5MHz} \right), N = \begin{cases} 1 \\ 2 \\ 4 \end{cases}$$

(R_{SETMIN} = 10k, R_{SETMAX} = 25k)

Any resistor, R_{SET}, tolerance adds to the inaccuracy of the oscillator. f_{OSC}.

START-UP TIME

The start-up time and settling time to within 1% of the final frequency is typically 100µs.

MAXIMUM OUTPUT LOAD

The LTC6905 output (Pin 5) can drive a capacitive load (C_{LOAD}) of 5pF or more. Driving a C_{LOAD} greater than 5pF depends on the oscillator's frequency (f_{OSC}) and output resistance (R_{OUT}). The output rise time or fall time due to R_{OUT} and C_{LOAD} is equal to 2.2 • R_{OUT} • C_{LOAD} (from 10% to 90% of the rise or fall transition). If the total output rise time plus fall time is arbitrarily specified to be equal to or less than 20% of the oscillator's period ($1/f_{OSC}$), then the maximum output C_{LOAD} in picofarads (pF) should be equal to or less than [45454/(R_{OUT} • f_{OSC})] (R_{OUT} in ohms and f_{OSC} in MHz).

Example: An LTC6905 is operating with a 3V power supply and is set for a f_{OSC} = 50MHz.

R_{OUT} with V^+ = 3V is 27Ω (using the R_{OUT} vs V^+ graph in the Typical Performance Characteristics).

The maximum output C_{LOAD} should be equal to or less than [45454/(27 • 50)] = 33.6pF.

The lowest resistive load Pin 5 can drive can be calculated using the minimum high level output voltage in the Electrical Characteristics. With a V^+ equal to 5.5V and 4mA output current, the minimum high level output voltage is 5V and the lowest resistive load Pin 5 can drive is 1.25k (5V/4mA). With a V^+ equal to 2.7V and 4mA output current, the minimum high level output voltage is 1.9V and the lowest resistive load Pin 5 can drive is 475Ω (1.9V/4mA).

FREQUENCY ACCURACY AND POWER SUPPLY NOISE

The frequency accuracy of the LTC6905 may be affected when its power supply generates noise with frequency contents equal to $f_{MO}/64$ or its multiples (f_{MO} is the internal LTC6905 master oscillator frequency before the divider and $f_{MO}/64$ is the master oscillator control loop frequency). If for example, the master oscillator frequency is set equal to 80MHz and the LTC6905 is powered by a switching regulator, then the oscillator frequency may show an additional error if the switching frequency is 1.4MHz (80MHz/64).

JITTER AND POWER SUPPLY NOISE

If the LTC6905 is powered by a supply that has frequency contents equal to the output frequency then the oscillators jitter may increase. In addition, power supply ripple in excess of 20mV at any frequency may increase jitter.

APPLICATIONS INFORMATION

JITTER AND DIVIDE RATIO

At a given output frequency, a higher master oscillator frequency and a higher divide ratio will result in lower jitter and higher power supply dissipation. Indeterminate jitter percentage will decrease by a factor of slightly less than the square root of the divider ratio, while determinate jitter will not be similarly attenuated. Please consult the specification tables and Jitter vs Frequency graph showing jitter at various divider ratios.

JITTER AND STRAY CAPACITANCE ON THE SET PIN (PIN 3)

The stray capacitance on the SET pin (Pin 3) should be limited to 10pF or less to avoid increased jitter or unstable oscillation.

LTC6905 SUGGESTED CRITICAL COMPONENT LAYOUT

In order to provide the specified performance, it is required that the frequency setting resistor R_{SET} and the supply bypass capacitor be placed as close as possible to the LTC6905. The following additional rules should be followed for best performance:

1) The bypass capacitor must be placed as close as possible to the LTC6905, and no vias should be placed between the capacitor and the LTC6905. The bypass capacitor must be on the same side of the circuit board as the LTC6905.
2) The resistor R_{SET} should be placed as close as possible to the LTC6905, and the connection of R_{SET} to V_{CC} should be closely shared with the bypass capacitor. The resistor R_{SET} may be placed on the opposite side of the board from the LTC6905, directly underneath the bypass capacitor.
3) If a ground plane is used, the connection of the LTC6905 to the ground plane should be as close as possible to the LTC6905 GND pin and should be composed of multiple, high current capacity vias.

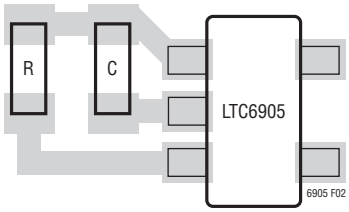


Figure 2. LTC6905 Suggested Critical Component Layout

APPLICATIONS INFORMATION

ALTERNATIVE METHODS OF SETTING THE OUTPUT FREQUENCY OF THE LTC6905

The LTC6905 may be programmed by any method that sources a current into the SET pin (Pin 3). The accuracy of the programming is best with a simple resistor because the LTC6905 takes into account both the voltage at the SET pin and the current into the SET pin when generating the output frequency. Since the voltage at the SET pin can vary by as much as 5%, setting the frequency using a current rather than a resistor will result in as much as 5% additional inaccuracy in the output frequency.

Figure 3 shows a method to control the frequency of the LTC6905 using a current source. R_{SET}, in this case, sets a maximum frequency according to the regular expression for f_{OSC}. The current source will subtract current from the SET pin to lower the frequency.

Figure 4 shows a method for controlling the frequency of the LTC6905 using a voltage source. In this case, R_{SET} sets a constant current into the SET pin, and R_{CNTRL} will subtract from this current in order to change the frequency. Increasing V_{CNTRL} will increase the output frequency.

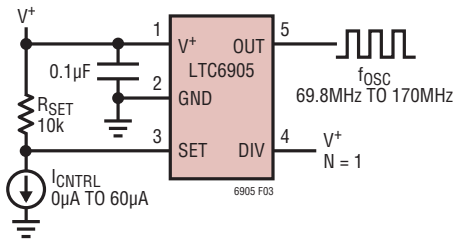


Figure 3. Current Controlled Oscillator

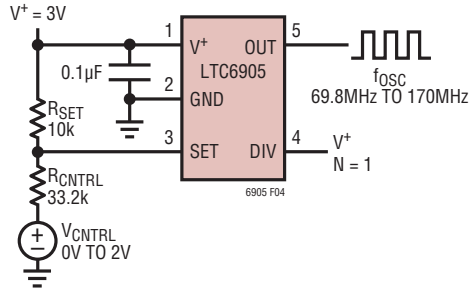


Figure 4. Voltage Controlled Oscillator

$$f_{OSC} = \frac{1}{N}\left[\frac{168.5MHz \bullet 10k\Omega \bullet \left[\frac{V^+ - V_{SET}}{R_{SET}} - I_{CNTRL}\right]}{V^+ - V_{SET}} + 1.5MHz\right]$$

I_{CNTRL} Frequency ≤ 100kHz

Example (Figure 3): $V_{SET} = (V^+ - 1V)$, $R_{SET} = 10k$, $N = 1$

$$f_{OSC} = [168.5MHz \bullet (1 - 10k\Omega \bullet I_{CNTRL}) + 1.5MHz$$

$$f_{OSC} = \frac{1}{N}\left[\frac{168.5MHz \bullet 10k\Omega \bullet \left[\frac{V^+ - V_{SET}}{R_{SET}} - \frac{V_{SET} - V_{CNTRL}}{R_{CNTRL}}\right]}{V^+ - V_{SET}} + 1.5MHz\right]$$

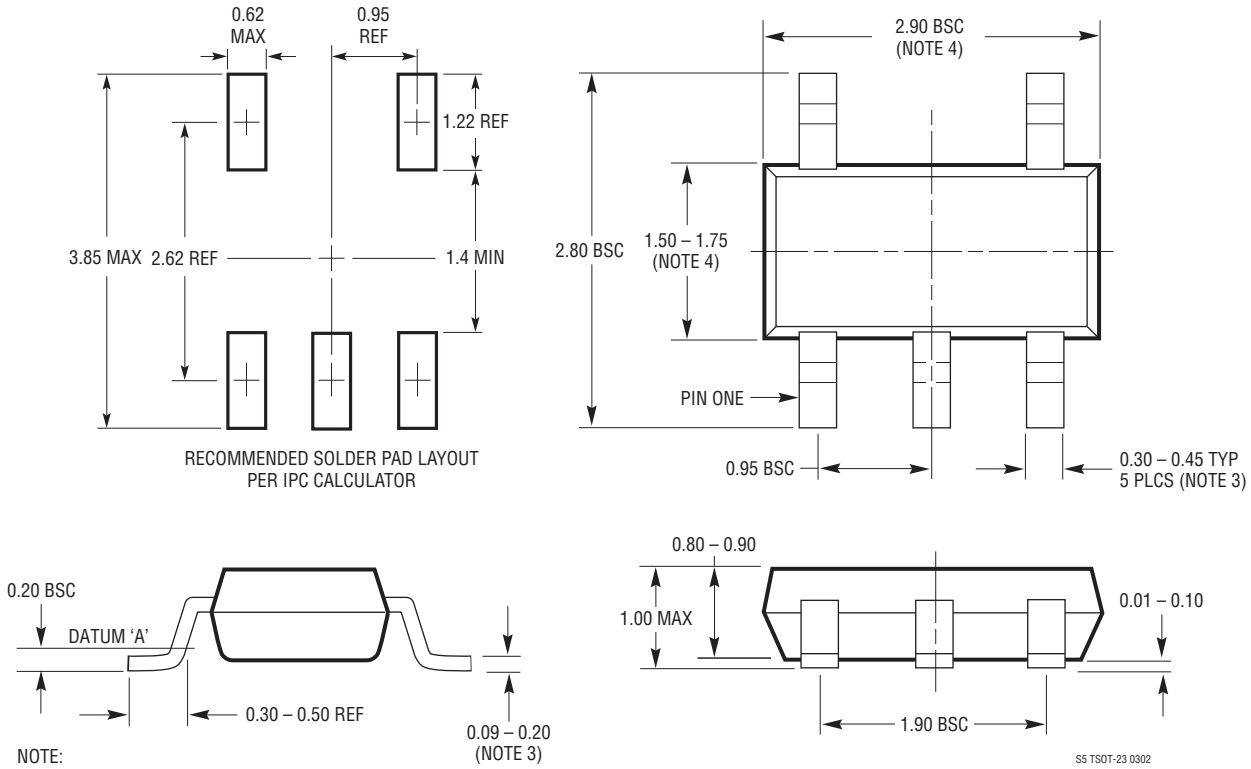
V_{CNTRL} Frequency ≤ 100kHz

Example (Figure 4): $V_{SET} = (V^+ - 1V)$, $R_{SET} = 10k$, $R_{CNTRL} = 33.2k$, $N = 1$, $V^+ = 3V$

$$f_{OSC} = \left[168.5MHz \bullet 10k\Omega \bullet \left[\frac{1}{10k\Omega} - \frac{2V - V_{CNTRL}}{33.2k\Omega}\right] + 1.5MHz\right]$$

PACKAGE DESCRIPTION

S5 Package
5-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1635)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193