16-/14-/11-Bit 2.5Gsps DACs

FEATURES

- 80dBc SFDR at 70MHz f_{OUT}
- >68dBc SFDR from DC to 1000MHz f_{OUT}
- 40mA Nominal Full-Scale, ±1V Output Compliant
- 10mA to 60mA Adjustable Full-Scale Current Range
- Single or Dual Port DDR LVDS and DHSTL Interface
- Low Latency (7.5 Cycles for Single Port, 11 Cycles for Dual Port)
- >78dBc 2-Tone IMD from DC to 1000MHz f_{OUT}
- –165dBc/Hz Additive Phase Noise at 1MHz Offset for 65MHz f_{OUT}
- 170-Lead (9mm × 15mm) BGA Package

APPLICATIONS

- Broadband Communication Systems
- DOCSIS CMTS
- Direct RF Synthesis
- Radar
- Instrumentation
- Automatic Test Equipment

DESCRIPTION

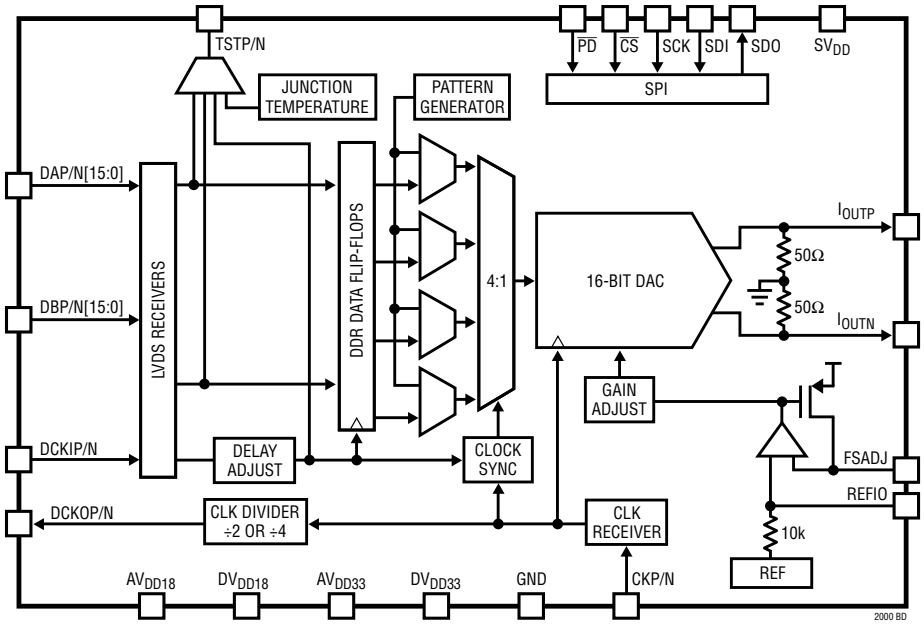
The LTC®2000 is a family of 16-/14-/11-bit 2.5Gsps current steering DACs with exceptional spectral purity.

The single (1.25Gsps mode) or dual (2.5Gsps mode) port source synchronous LVDS interface supports data rates of up to 1.25Gbps using a 625MHz DDR data clock, which can be either in quadrature or in phase with the data. An internal synchronizer automatically aligns the data with the DAC sample clock.

Additional features such as pattern generation, LVDS loopout and junction temperature sensing simplify system development and testing.

A serial peripheral interface (SPI) port allows configuration and read back of internal registers. Operating from 1.8V and 3.3V supplies, the LTC2000 consumes 2.2W at 2.5Gsps and 1.3W at 1.25Gsps.

BLOCK DIAGRAM



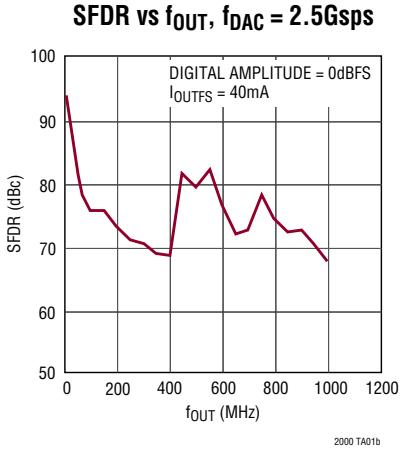


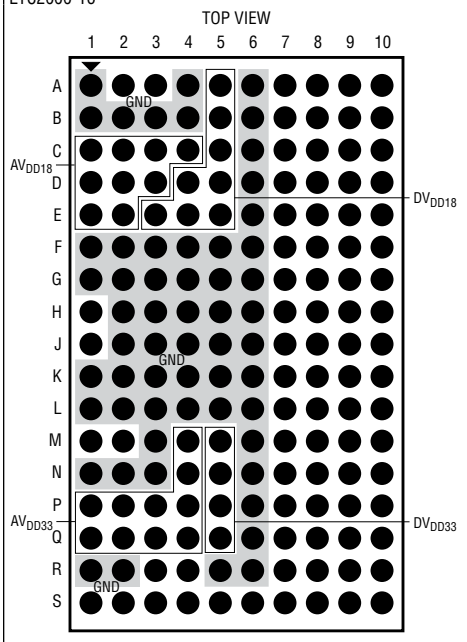
TABLE OF CONTENTS

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

AV_{DD33}, DV_{DD33}, SV_{DD} ..... –0.3V to 4V
AV_{DD18}, DV_{DD18} ..... –0.3V to 2V
I_{OUTP}, I_{OUTN} ..... –1.2V to Min (AV_{DD33} + 0.3V, 4V)
FSADJ, REFIO ..... –0.3V to Min (AV_{DD33} + 0.3V, 4V)
DCKIP, DCKIN ..... –0.3V to Min (DV_{DD33} + 0.3V, 4V)
DCKOP, DCKON ..... –0.3V to Min (DV_{DD33} + 0.3V, 4V)
DAP/N, DBP/N ..... –0.3V to Min (DV_{DD33} + 0.3V, 4V)
TSTP, TSTN ..... –0.3V to Min (AV_{DD33} + 0.3V, 4V)
CKP, CKN ..... –0.3V to Min (AV_{DD18} + 0.3V, 2V)
$\overline{CS}$, $\overline{PD}$, SCK, SDI, SDO ... –0.3V to Min (SV_{DD} + 0.3V, 4V)
Operating Temperature Range
  LTC2000C ..... 0°C to 70°C
  LTC2000I ..... –40°C to 85°C
Maximum Junction Temperature ..... 125°C
Storage Temperature Range ..... –55°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

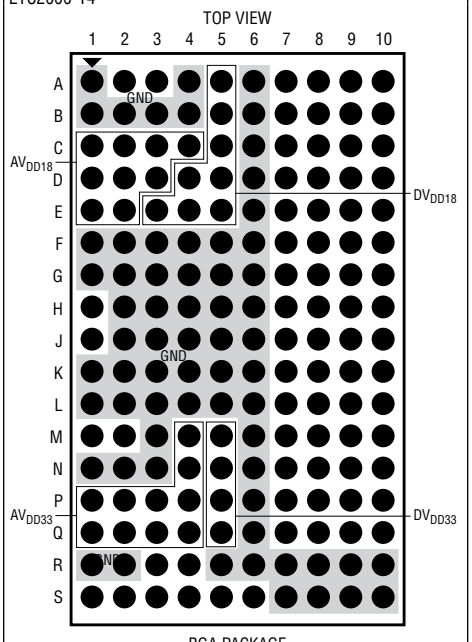
PIN CONFIGURATION

LTC2000-16



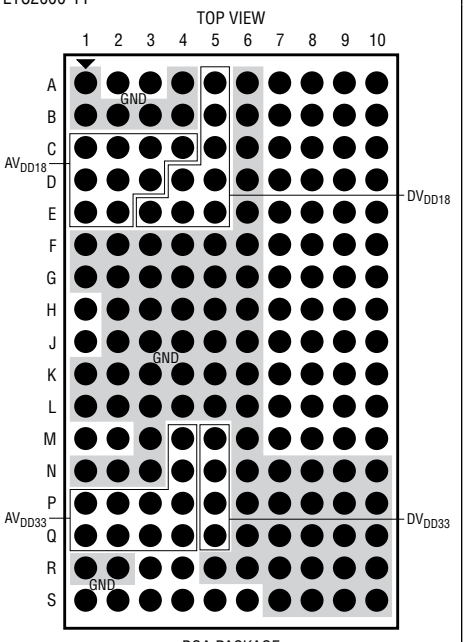
BGA PACKAGE
170-LEAD (9mm × 15mm × 1.54mm)
T_{JMAX} = 125°C, θ_{JA} = 20°C/W, θ_{JB} = 8°C/W,
θ_{JCtop} = 9°C/W, $\theta_{JCbottom}$ = 3°C/W

LTC2000-14



BGA PACKAGE
170-LEAD (9mm × 15mm × 1.54mm)
T_{JMAX} = 125°C, θ_{JA} = 20°C/W, θ_{JB} = 8°C/W,
θ_{JCtop} = 9°C/W, $\theta_{JCbottom}$ = 3°C/W

LTC2000-11



BGA PACKAGE
170-LEAD (9mm × 15mm × 1.54mm)
T_{JMAX} = 125°C, θ_{JA} = 20°C/W, θ_{JB} = 8°C/W,
θ_{JCtop} = 9°C/W, $\theta_{JCbottom}$ = 3°C/W

ORDER INFORMATION http://www.linear.com/product/LTC2000#orderinfo

LTC2000 C Y –16 #PBF

LEAD FREE DESIGNATOR
PBF = Lead Free

RESOLUTION
16 = 16-Bit Resolution
14 = 14-Bit Resolution
11 = 11-Bit Resolution

PACKAGE TYPE
170-Lead (15mm × 9mm × 1.54mm) BGA

TEMPERATURE GRADE
C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (–40°C to 85°C)

PRODUCT PART NUMBER

PART NUMBER	BALL FINISH	PART MARKING*	PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE
LTC2000CY-16#PBF	SAC305 (RoHS)	LTC2000Y-16	BGA	3	0°C to 70°C
LTC2000CY-14#PBF	SAC305 (RoHS)	LTC2000Y-14	BGA	3	0°C to 70°C
LTC2000CY-11#PBF	SAC305 (RoHS)	LTC2000Y-11	BGA	3	0°C to 70°C
LTC2000IY-16#PBF	SAC305 (RoHS)	LTC2000Y-16	BGA	3	–40°C to 85°C
LTC2000IY-14#PBF	SAC305 (RoHS)	LTC2000Y-14	BGA	3	–40°C to 85°C
LTC2000IY-11#PBF	SAC305 (RoHS)	LTC2000Y-11	BGA	3	–40°C to 85°C
LTC2000IY-16	Sn/Pb	LTC2000Y-16	BGA	3	–40°C to 85°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AV_{DD18}, DV_{DD18} = 1.71V to 1.89V, AV_{DD33}, DV_{DD33} = 3.135V to 3.465V, SV_{DD} = 1.71V to 3.465V, R_{FSADJ} = 500Ω, 12.5Ω load from $I_{OUTP/N}$ to GND including internal 50Ω termination, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Performance							
	Resolution	LTC2000-16	●	16			Bits
		LTC2000-14	●	14			Bits
		LTC2000-11	●	11			Bits
DNL	Differential Nonlinearity	LTC2000-16	●		±0.5	±2.7	LSB
		LTC2000-14	●		±0.2	±1	LSB
		LTC2000-11	●		±0.1	±0.5	LSB
INL	Integral Nonlinearity	LTC2000-16	●		±1	±4	LSB
		LTC2000-14	●		±0.5	±2	LSB
		LTC2000-11	●		±0.2	±1	LSB
	Offset Error	LTC2000-16	●			±0.05	% FSR
		LTC2000-14	●			±0.06	% FSR
		LTC2000-11	●			±0.09	% FSR
	Offset Error Drift				1		ppm/°C
	Gain Error				±0.5		% FSR
	Gain Error Drift				5		ppm/°C
	Power Supply Rejection Ratio	Full-Scale; AV_{DD33} = 3.135V to 3.465V			69		dB
Analog Output							
	Full-Scale Output Current	R_{FSADJ} = 500Ω			40		mA
	Output Compliance Range		●	–1		1	V
	Output Resistance	$I_{OUTP/N}$ to GND	●	42	50	58	Ω
	Output Capacitance				6		pF
	Output Bandwidth	$R_{IOUTP/N}$ = 12.5Ω, –3dB Excluding sin(x)/x			2.1		GHz
AC Performance							
	Maximum Update Rate	Dual-Port Mode Single-Port Mode	● ●	2.5 1.25			Gsps Gsps
SFDR	Spurious Free Dynamic Range f_{DAC} = 1.25Gsps, 0dBFS	f_{OUT} = 50MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 100MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 250MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 500MHz, LIN_DIS = 0, LIN_GN = 75%			82 82 74 74		dBc dBc dBc dBc
	Spurious Free Dynamic Range f_{DAC} = 2.5Gsps, 0dBFS	f_{OUT} = 100MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 200MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 500MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 1000MHz, LIN_DIS = 0, LIN_GN = 75%	 ● 	 67 	76 74 72 68		dBc dBc dBc dBc
		f_{OUT} = 500MHz, LIN_DIS = 1 f_{OUT} = 1000MHz, LIN_DIS = 1			66 62		dBc dBc
IMD	2-Tone Intermodulation Distortion $f_{OUT2} = f_{OUT1} + 1.25MHz$ f_{DAC} = 1.25Gsps, –6dBFS	f_{OUT} = 50MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 100MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 250MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 500MHz, LIN_DIS = 0, LIN_GN = 75%			100 90 90 82		dBc dBc dBc dBc
	2-Tone Intermodulation Distortion $f_{OUT2} = f_{OUT1} + 1.25MHz$ f_{DAC} = 2.5Gsps, –6dBFS	f_{OUT} = 100MHz, LIN_DIS = 1 f_{OUT} = 200MHz, LIN_DIS = 1 f_{OUT} = 500MHz, LIN_DIS = 1 f_{OUT} = 1000MHz, LIN_DIS = 1			87 86 84 78		dBc dBc dBc dBc
		f_{OUT} = 500MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 1000MHz, LIN_DIS = 0, LIN_GN = 75%			80 67		dBc dBc

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AV_{DD18}, DV_{DD18} = 1.71V to 1.89V, AV_{DD33}, DV_{DD33} = 3.135V to 3.465V, SV_{DD} = 1.71V to 3.465V, R_{FSADJ} = 500Ω, 12.5Ω load from $I_{OUTP/N}$ to GND including internal 50Ω termination, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
NSD	Noise Spectral Density 0dBFS Single Tone, f_{DAC} = 2.5Gsps, I_{OUTFS} = 40mA	LTC2000-16, f_{OUT} = 100MHz LTC2000-16, f_{OUT} = 350MHz LTC2000-16, f_{OUT} = 550MHz LTC2000-16, f_{OUT} = 950MHz			–166 –161 –158 –156		dBm/Hz dBm/Hz dBm/Hz dBm/Hz
		LTC2000-14, f_{OUT} = 100MHz LTC2000-14, f_{OUT} = 350MHz LTC2000-14, f_{OUT} = 550MHz LTC2000-14, f_{OUT} = 950MHz			–164 –160 –158 –155		dBm/Hz dBm/Hz dBm/Hz dBm/Hz
		LTC2000-11, f_{OUT} = 100MHz LTC2000-11, f_{OUT} = 350MHz LTC2000-11, f_{OUT} = 550MHz LTC2000-11, f_{OUT} = 950MHz			–156 –155 –154 –153		dBm/Hz dBm/Hz dBm/Hz dBm/Hz
	Phase Noise f_{DAC} = 2.5Gsps, f_{OUT} = 65MHz 0dBFS Single Tone, I_{OUTFS} = 40mA	10kHz Offset 1MHz Offset			–147 –165		dBc/Hz dBc/Hz
WCDMA ACLR	WCDMA ACLR (Single Carrier) Adjacent/Alternate Adjacent Channel	f_{DAC} = 2.5Gsps, f_{OUT} = 350MHz f_{DAC} = 2.5Gsps, f_{OUT} = 950MHz			77/79 72/75		dBc dBc
Latency							
	Latency (Note 5)	Single-Port Mode Dual-Port Mode, DAP/N Data Dual-Port Mode, DBP/N Data			7.5 10 11		Cycles Cycles Cycles
	Aperture Delay	CKP/N Rising to $I_{OUTP/N}$ Transition			3		ns
	Settling Time				2.2		ns
Reference							
	Output Voltage		●	1.225	1.25	1.275	V
	Input Voltage		●	1.1		1.4	V
	Reference Temperature Coefficient				±25		ppm/°C
	Output Impedance				10		kΩ
DAC Clock Inputs (CKP, CKN)							
	Differential Input Voltage Range		●	±0.3		±1.8	V
	Common-Mode Input Voltage	Set Internally			1		V
	Sampling Clock Frequency		●	50		2500	MHz
	Input Impedance				5		kΩ
LVDS Inputs (DCKIP, DCKIN, DAP/N, DBP/N)							
	Differential Input Voltage Range		●	±0.2		±0.6	V
	Common-Mode Voltage Range		●	0.4		1.8	V
	Differential Input Impedance		●	95	120	145	Ω
	Maximum Data Rate		●			1250	Mbps
	LVDS Clock Frequency		●	25		625	MHz

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS Output (DCKOP, DCKON)							
	Differential Output Voltage	100Ω Differential Load, DCKO_ISEL = 0 50Ω Differential Load, DCKO_ISEL = 1	● ●	0.24 0.24	0.36 0.36	0.48 0.48	V V
	Common-Mode Output Voltage		●	1.075	1.2	1.325	V
	Internal Termination Resistance	DCKO_TRM = 1			100		Ω
CMOS Digital Inputs ($\overline{CS}$, $\overline{PD}$, SCK, SDI)							
V_{IH}	Digital Input High Voltage		●	70			$\%V_{SVDD}$
V_{IL}	Digital Input Low Voltage		●			30	$\%V_{SVDD}$
I_{LK}	Digital Input Leakage	V_{IN} = GND or SV_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				8		pF
CMOS Digital Output (SDO)							
V_{OH}	Digital Output High Voltage	I_{SOURCE} = 0.2mA	●	85			$\%V_{SVDD}$
V_{OL}	Digital Output Low Voltage	I_{SINK} = 1.6mA	●			15	$\%V_{SVDD}$
	Hi-Z Output Leakage		●			±10	µA
	Hi-Z Output Capacitance				8		pF
Power Supply							
V_{VDD33}	AV_{DD33}, DV_{DD33} Supply Voltage		●	3.135	3.3	3.465	V
V_{VDD18}	AV_{DD18}, D_{VDD18} Supply Voltage		●	1.71	1.8	1.89	V
V_{SVDD}	SV_{DD} SPI Supply Voltage		●	1.71		3.465	V
I_{AVDD33}	AV_{DD33} Supply Current, AV_{DD33} = 3.3V	$\overline{PD}$ = SV_{DD} $\overline{PD}$ = GND	● ●		68 0.1	72 10	mA µA
I_{DVDD33}	DV_{DD33} Supply Current, DV_{DD33} = 3.3V	$\overline{PD}$ = SV_{DD} $\overline{PD}$ = GND	● ●		8 0.1	12 5	mA µA
I_{AVDD18}	AV_{DD18} Supply Current, AV_{DD18} = 1.8V	f_{DAC} = 2500MHz f_{DAC} = 1250MHz f_{DAC} = 0Hz, $\overline{PD}$ = SV_{DD} f_{DAC} = 0Hz, $\overline{PD}$ = GND	● ● ● ●		720 375 23 3	790 420 27 180	mA mA mA µA
I_{DVDD18}	DV_{DD18} Supply Current, DV_{DD18} = 1.8V	f_{DAC} = 2500MHz f_{DAC} = 1250MHz f_{DAC} = 0Hz, $\overline{PD}$ = SV_{DD} f_{DAC} = 0Hz, $\overline{PD}$ = GND	● ● ● ●		350 190 10 0.1	395 215 14 240	mA mA mA µA
I_{SVDD}	SV_{DD} Supply Current (Note 4), SV_{DD} = 3.3V	f_{SCK} = 0Hz	●		0.1	5	µA
	Total Power Dissipation	f_{DAC} = 2500MHz f_{DAC} = 1250MHz f_{DAC} = 0Hz, $\overline{PD}$ = SV_{DD} f_{DAC} = 0Hz, $\overline{PD}$ = GND			2180 1270 310 6		mW mW mW µW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AV_{DD18}, DV_{DD18} = 1.71V to 1.89V, AV_{DD33}, DV_{DD33} = 3.135V to 3.465V, SV_{DD} = 1.71V to 3.465V, R_{FSADJ} = 500Ω, output load 50Ω double terminated, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_1	SDI Valid to SCK Setup	(Note 3)	●	4			ns
t_2	SDI Valid to SCK Hold	(Note 3)	●	4			ns
t_3	SCK High Time	(Note 3)	●	9			ns
t_4	SCK Low Time	(Note 3)	●	9			ns
t_5	$\overline{CS}$ Pulse Width	(Note 3)	●	10			ns
t_6	SCK High to $\overline{CS}$ High	(Note 3)	●	7			ns
t_7	$\overline{CS}$ Low to SCK High	(Note 3)	●	7			ns
t_{10}	$\overline{CS}$ High to SCK High	(Note 3)	●	7			ns
t_{13}	SCK Low to SDO Valid	Unloaded (Note 3)	●	10			ns
	SCK Frequency	50% Duty Cycle (Note 3)	●			50	MHz
t_{11}	LVDS DAP/N, DBP/N to DCKI Setup Time (Note 3)	DCKI_Q = 1 DCKI_Q = 0, DCKI_TADJ = 000	● ●	200 600			ps ps
t_{12}	LVDS DAP/N, DBP/N to DCKI Hold Time (Note 3)	DCKI_Q = 1 DCKI_Q = 0, DCKI_TADJ = 000	● ●	200 –200			ps ps

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are with respect to GND.

Note 3: Guaranteed by design and not production tested.

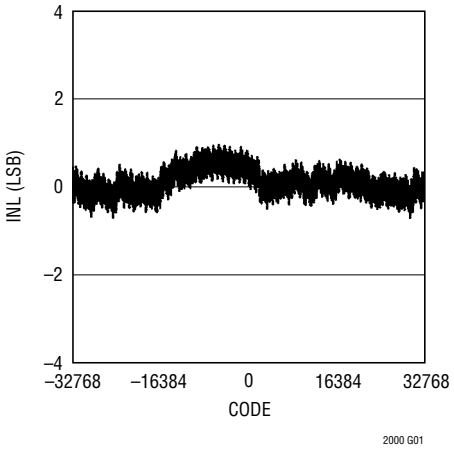
Note 4: Digital inputs at 0V or SV_{DD}.

Note 5: Latency is the delay from a transition on DCKIP/N until the CKP/N transition which causes the sample on DAP/N or DBP/N to appear at the DAC output $I_{OUTP/N}$, as measured in DAC sample clock (CKP/N) cycles.

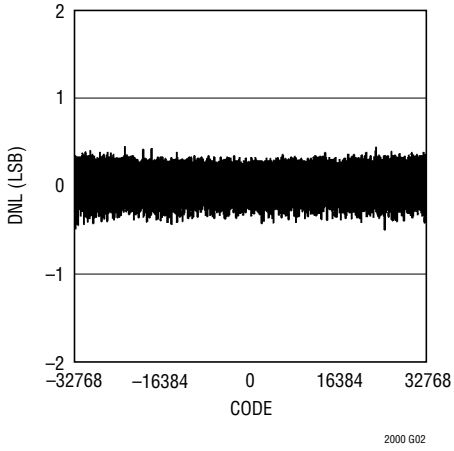
TYPICAL PERFORMANCE CHARACTERISTICS

I_{OUTFS} = 40mA, T_A = 25°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD33} = DV_{DD33} = 3.3V, R_{LOAD} = 12.5Ω, unless otherwise noted.

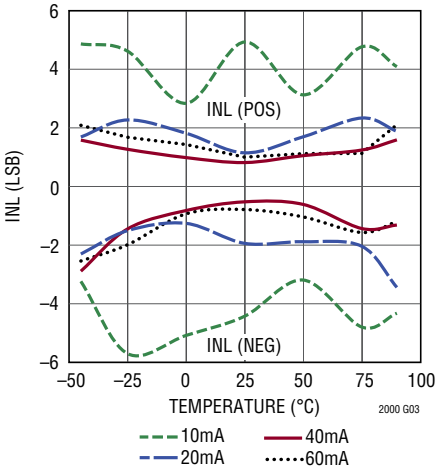
LTC2000-16 Integral Nonlinearity (INL)



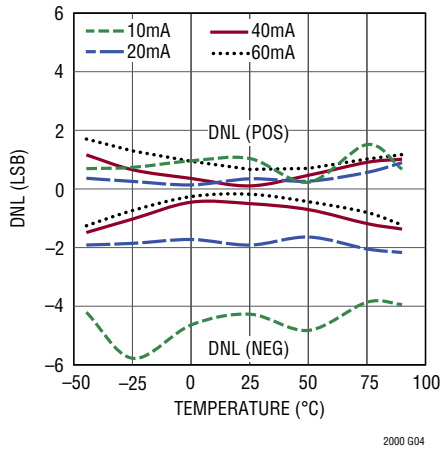
LTC2000-16 Differential Nonlinearity (DNL)



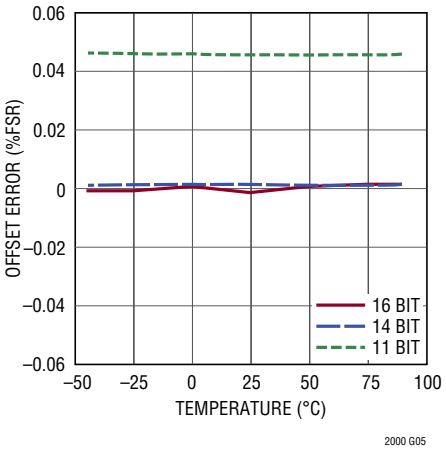
INL vs I_{OUTFS} and Temperature



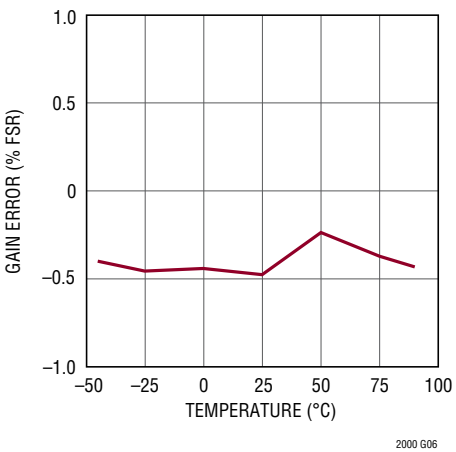
DNL vs I_{OUTFS} and Temperature



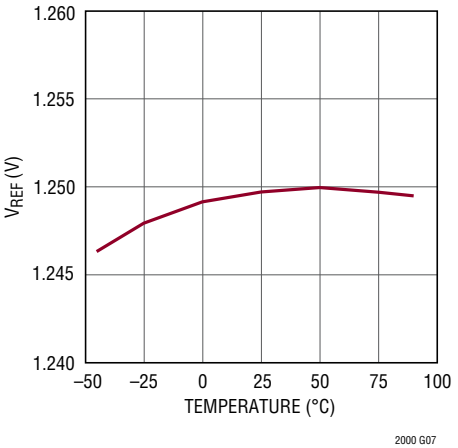
Offset Error vs Temperature



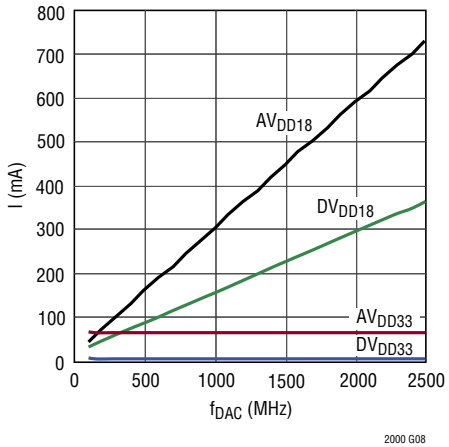
Gain Error vs Temperature



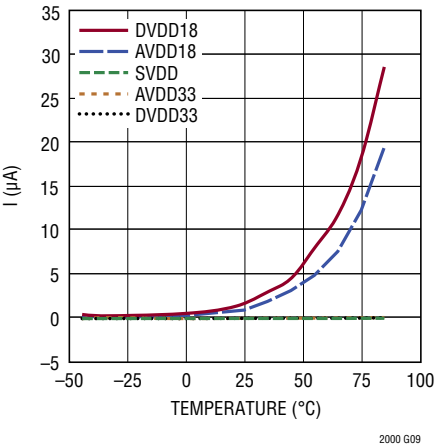
Reference Output Voltage vs Temperature



Supply Current vs f_{DAC}



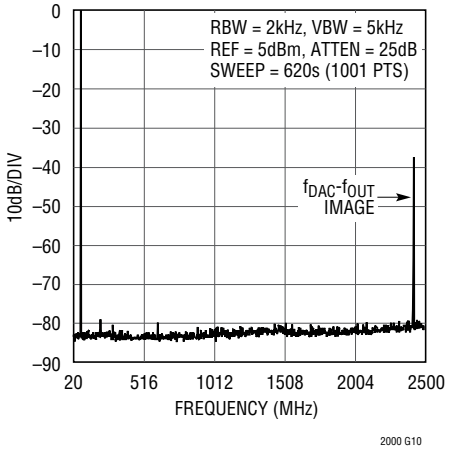
Shutdown Current vs Temperature



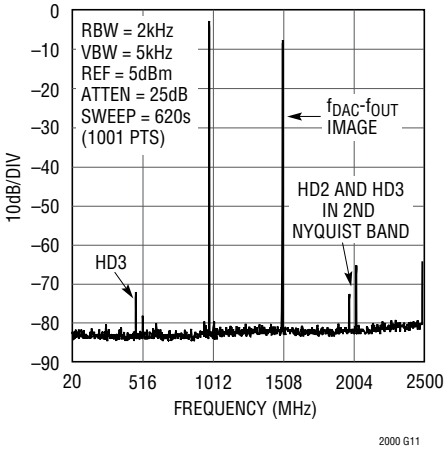
TYPICAL PERFORMANCE CHARACTERISTICS

I_{OUTFS} = 40mA, T_A = 25°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD33} = DV_{DD33} = 3.3V, R_{LOAD} = 12.5Ω, LIN_DIS = 0, LIN_ GN = 75% unless otherwise noted.

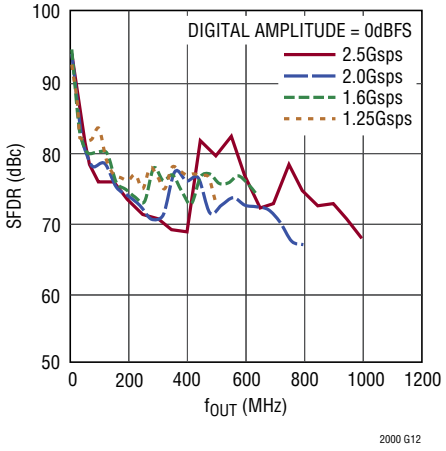
Single-Tone Spectrum at f_{OUT} = 70MHz, f_{DAC} = 2.5Gsps



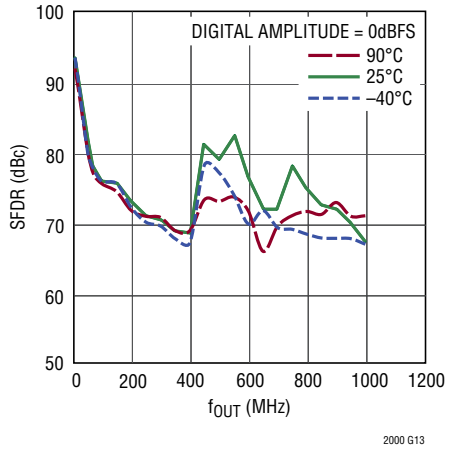
Single-Tone Spectrum at f_{OUT} = 990MHz, f_{DAC} = 2.5Gsps



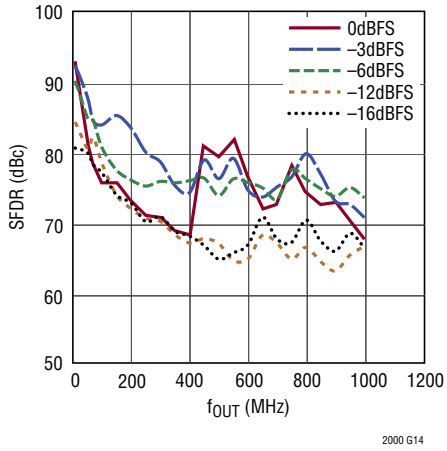
SFDR vs f_{OUT} and f_{DAC}



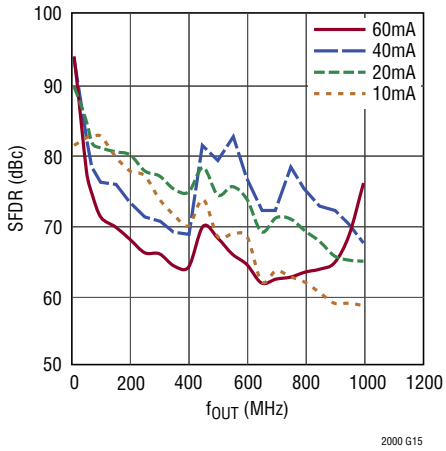
SFDR vs f_{OUT} and Temperature, f_{DAC} = 2.5Gsps



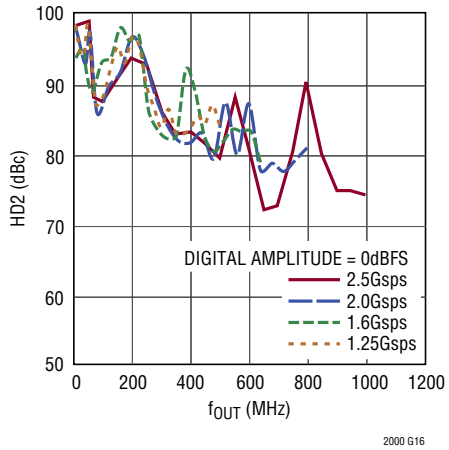
SFDR vs f_{OUT} and Digital Amplitude (dBFS), f_{DAC} = 2.5Gsps



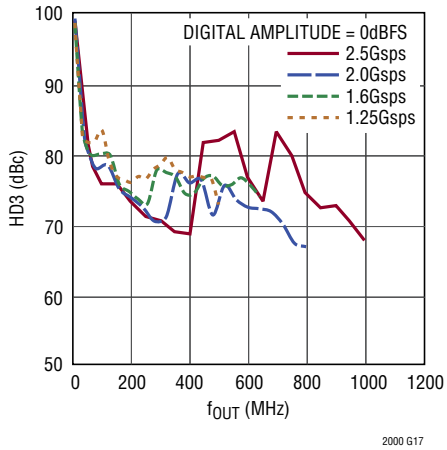
SFDR vs f_{OUT} and I_{OUTFS}, f_{DAC} = 2.5Gsps



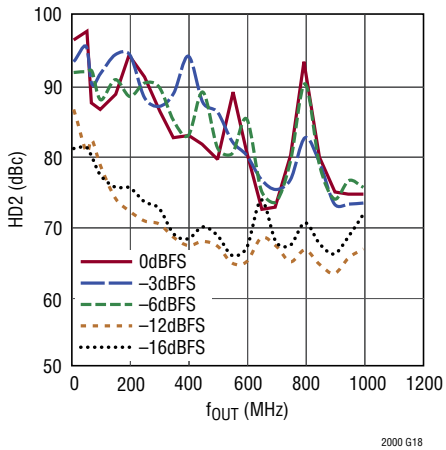
HD2 vs f_{OUT} and f_{DAC}



HD3 vs f_{OUT} and f_{DAC}



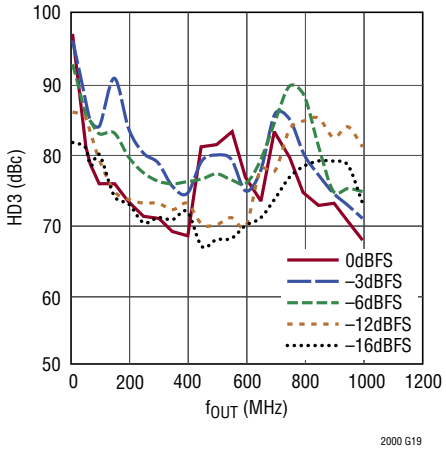
HD2 vs f_{OUT} and Digital Amplitude (dBFS), f_{DAC} = 2.5Gsps



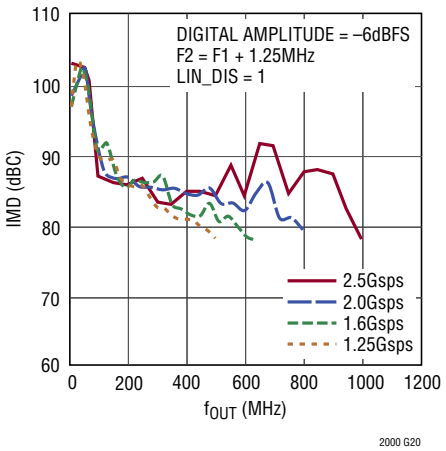
TYPICAL PERFORMANCE CHARACTERISTICS

I_{OUTFS} = 40mA, T_A = 25°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD33} = DV_{DD33} = 3.3V, R_{LOAD} = 12.5Ω, LIN_DIS = 0, LIN_ GN = 75% unless otherwise noted.

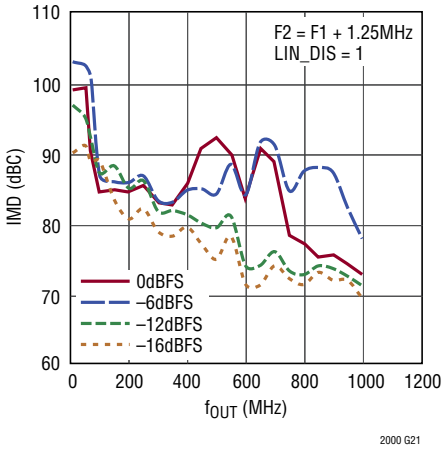
HD3 vs f_{OUT} and Digital Amplitude (dBFS), f_{DAC} = 2.5Gsps



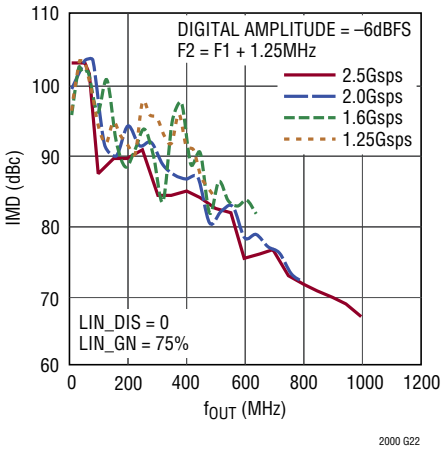
2-Tone IMD vs f_{OUT} and f_{DAC}



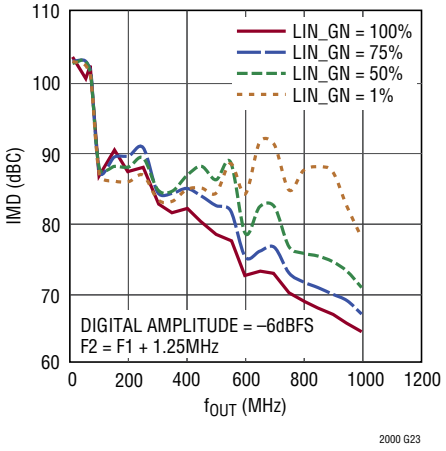
2-Tone IMD vs f_{OUT} and Digital Amplitude, f_{DAC} = 2.5Gsps



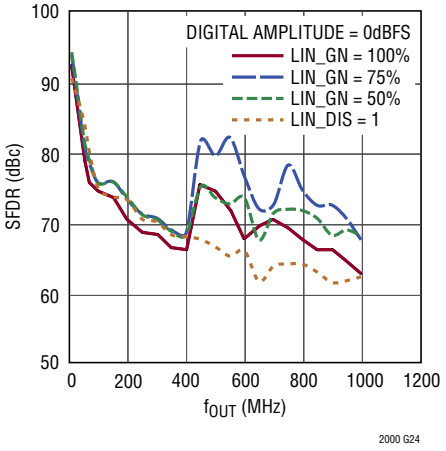
2-Tone IMD vs f_{OUT} and f_{DAC} with Default Linearization



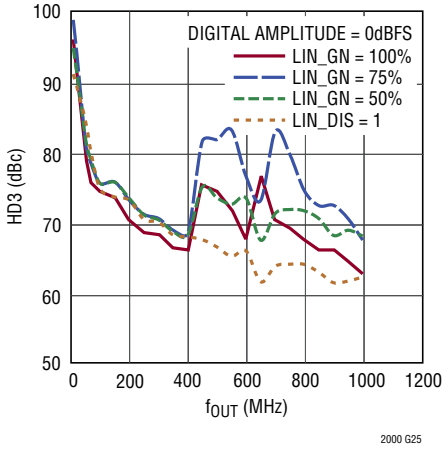
2-Tone IMD vs f_{OUT} and Linearization Setting, f_{DAC} = 2.5Gsps



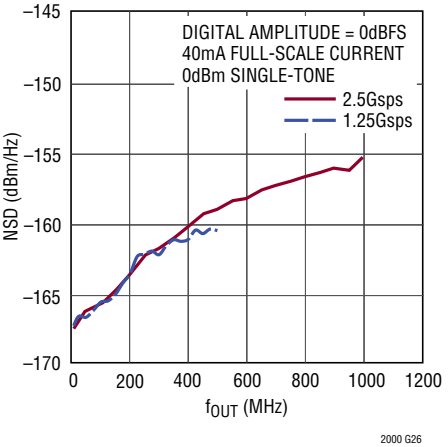
SFDR vs f_{OUT} and Linearization Setting, f_{DAC} = 2.5Gsps



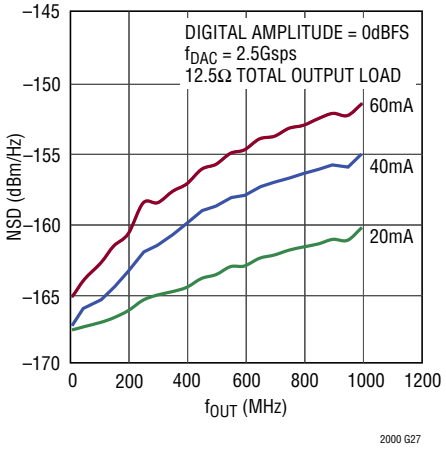
HD3 vs f_{OUT} and Linearization Setting, f_{DAC} = 2.5Gsps



LTC2000-16 Single-Tone NSD vs f_{OUT} and f_{DAC}



LTC2000-16 Single-Tone NSD vs f_{OUT} and I_{OUTFS}

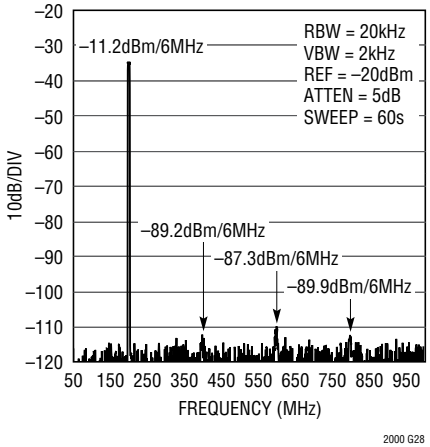


TYPICAL PERFORMANCE CHARACTERISTICS

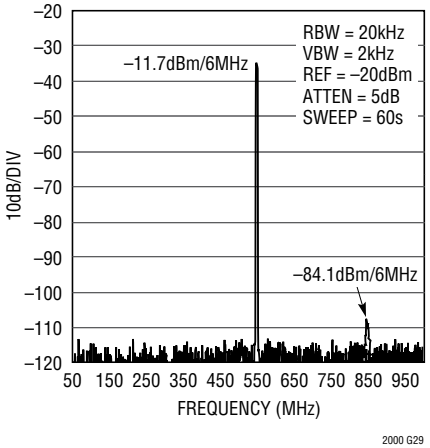
I_{OUTFS} = 40mA, T_A = 25°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD33} = DV_{DD33} = 3.3V, R_{LOAD} = 12.5Ω, LIN_DIS = 0, LIN_ GN = 75% unless otherwise noted.

LTC2000-16

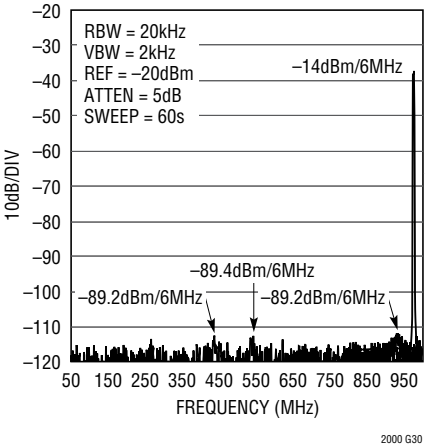
Single Carrier DOCSIS Low Band Wideband ACLR, f_{DAC} = 2.5Gsps



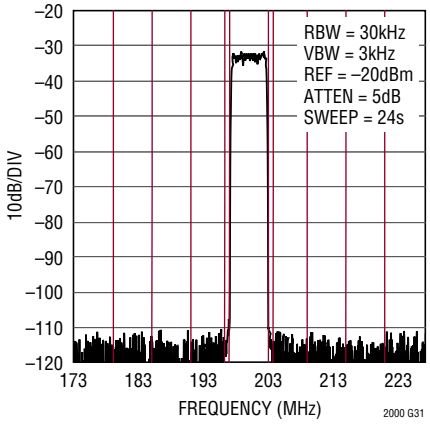
Single Carrier DOCSIS Mid Band Wideband ACLR, f_{DAC} = 2.5Gsps



Single Carrier DOCSIS High Band Wideband ACLR, f_{DAC} = 2.5Gsps



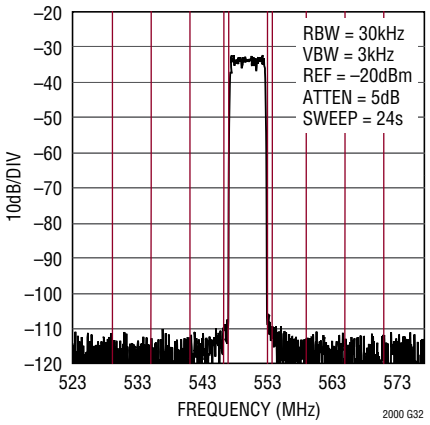
Single Carrier DOCSIS Low Band Narrowband ACLR, f_{DAC} = 2.5Gsps



CARRIER POWER = –11.16dBm, CENTER FREQ = 200MHz

OFFSET FREQ	BW	LOWER	UPPER
3.375MHz	750kHz	–100.31dBm	–94.84dBm
6.375MHz	5.25MHz	–96.02dBm	–94.67dBm
12.00MHz	6MHz	–96.47dBm	–95.48dBm
18.00MHz	6MHz	–96.40dBm	–96.29dBm
24.00MHz	6MHz	–96.40dBm	–96.57dBm

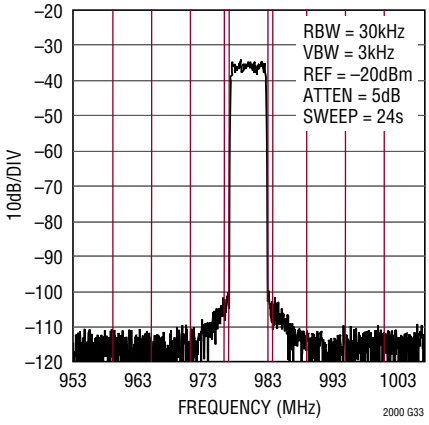
Single Carrier DOCSIS Mid Band Narrowband ACLR, f_{DAC} = 2.5Gsps



CARRIER POWER = –11.66dBm, CENTER FREQ = 550MHz

OFFSET FREQ	BW	LOWER	UPPER
3.375MHz	750kHz	–95.63dBm	–93.62dBm
6.375MHz	5.25MHz	–93.01dBm	–92.97dBm
12.00MHz	6MHz	–94.66dBm	–94.51dBm
18.00MHz	6MHz	–95.19dBm	–94.87dBm
24.00MHz	6MHz	–94.97dBm	–95.15dBm

Single Carrier DOCSIS High Band Narrowband ACLR, f_{DAC} = 2.5Gsps



CARRIER POWER = –14.04dBm, CENTER FREQ = 980MHz

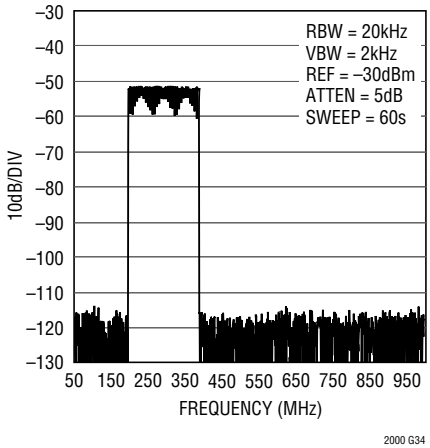
OFFSET FREQ	BW	LOWER	UPPER
3.375MHz	750kHz	–89.47dBm	–89.52dBm
6.375MHz	5.25MHz	–87.24dBm	–87.00dBm
12.00MHz	6MHz	–93.04dBm	–92.94dBm
18.00MHz	6MHz	–93.52dBm	–92.51dBm
24.00MHz	6MHz	–93.33dBm	–92.03dBm

TYPICAL PERFORMANCE CHARACTERISTICS

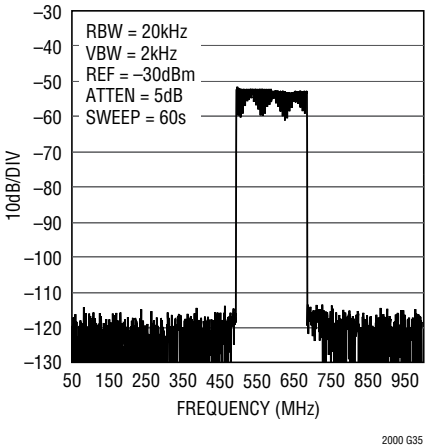
I_{OUTFS} = 40mA, T_A = 25°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD33} = DV_{DD33} = 3.3V, R_{LOAD} = 12.5Ω, LIN_DIS = 0, LIN_ GN = 75% unless otherwise noted.

LTC2000-16

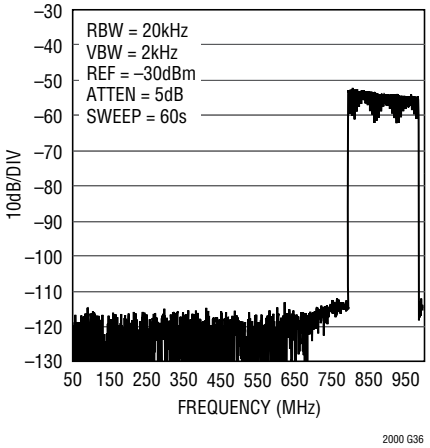
32-Carrier DOCSIS Low Band Wideband ACLR, f_{DAC} = 2.5Gsps



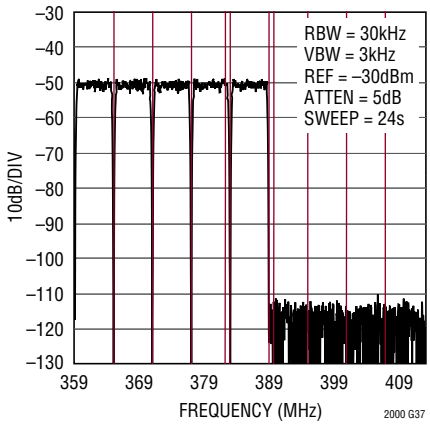
32-Carrier DOCSIS Mid Band Wideband ACLR, f_{DAC} = 2.5Gsps



32 Carrier DOCSIS High Band Wideband ACLR, f_{DAC} = 2.5Gsps



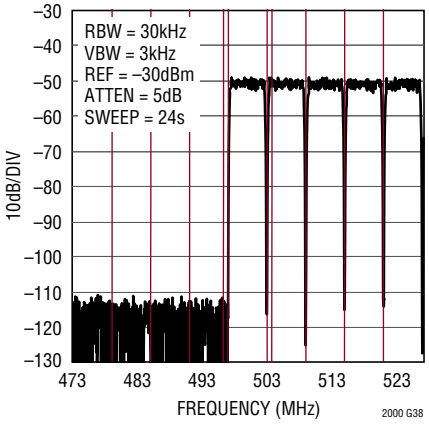
32-Carrier DOCSIS Low Band Narrowband ACLR, f_{DAC} = 2.5Gsps



CARRIER POWER = –28.64dBm, CENTER FREQ = 386MHz

OFFSET FREQ	BW	LOWER	UPPER
3.375MHz	750kHz	–39.32dBm	–103.86dBm
6.375MHz	5.25MHz	–29.01dBm	–95.18dBm
12.00MHz	6MHz	–28.68dBm	–94.68dBm
18.00MHz	6MHz	–28.54dBm	–94.97dBm
24.00MHz	6MHz	–28.49dBm	–95.08dBm

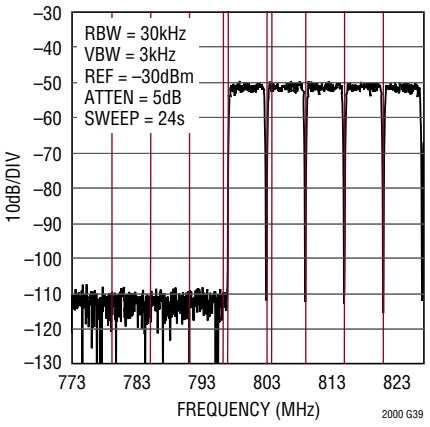
32 Carrier DOCSIS Mid Band Narrowband ACLR, f_{DAC} = 2.5Gsps



CARRIER POWER = –28.42dBm, CENTER FREQ = 500MHz

OFFSET FREQ	BW	LOWER	UPPER
3.375MHz	750kHz	–102.49dBm	–39.23dBm
6.375MHz	5.25MHz	–94.71dBm	–28.92dBm
12.00MHz	6MHz	–94.02dBm	–28.69dBm
18.00MHz	6MHz	–94.36dBm	–28.71dBm
24.00MHz	6MHz	–93.72dBm	–28.74dBm

32 Carrier DOCSIS High Band Narrowband ACLR, f_{DAC} = 2.5Gsps



CARRIER POWER = –29.31dBm, CENTER FREQ = 800MHz

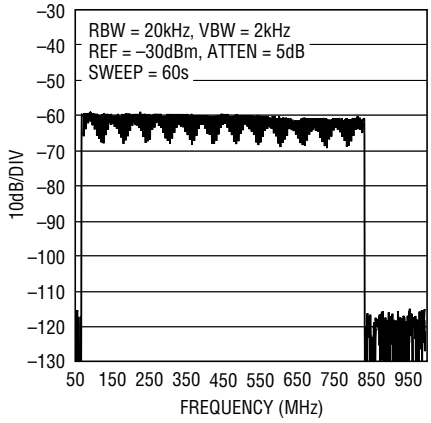
OFFSET FREQ	BW	LOWER	UPPER
3.375MHz	750kHz	–98.23dBm	–40.42dBm
6.375MHz	5.25MHz	–90.00dBm	–29.56dBm
12.00MHz	6MHz	–89.76dBm	–29.20dBm
18.00MHz	6MHz	–89.72dBm	–29.25dBm
24.00MHz	6MHz	–89.76dBm	–29.55dBm

TYPICAL PERFORMANCE CHARACTERISTICS

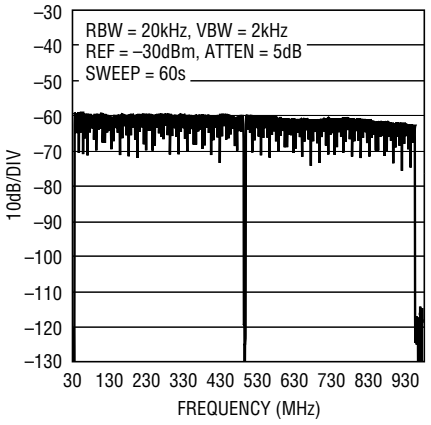
I_{OUTFS} = 40mA, T_A = 25°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD33} = DV_{DD33} = 3.3V, R_{LOAD} = 12.5Ω, LIN_DIS = 0, LIN_ GN = 75% unless otherwise noted.

LTC2000-16

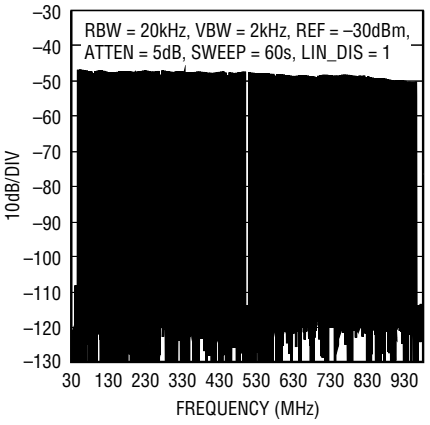
128 Carrier DOCSIS Low Band Wideband ACLR, f_{DAC} = 2.5Gsps



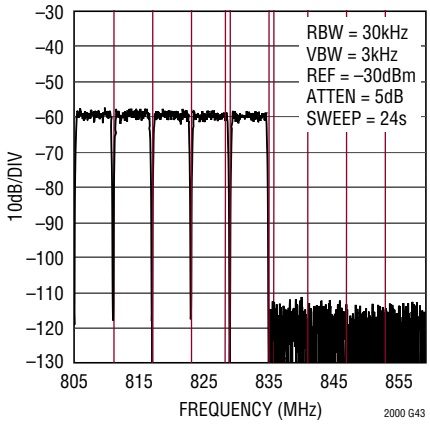
157 Carrier DOCSIS Gap Channel Wideband ACLR, f_{DAC} = 2.5Gsps



157 Carrier Tones with Gap Channel Wideband ACLR, f_{DAC} = 2.5Gsps



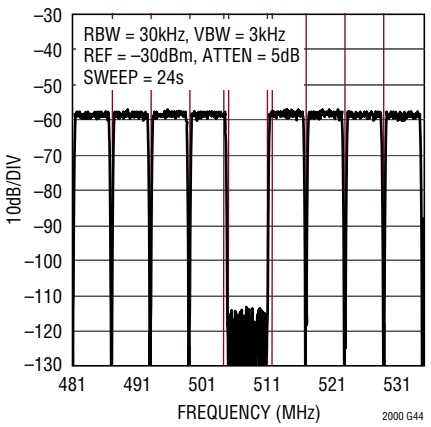
128 Carrier DOCSIS Low Band Narrowband ACLR, f_{DAC} = 2.5Gsps



CARRIER POWER = –37.59dBm, CENTER FREQ = 832MHz

OFFSET FREQ	BW	LOWER	UPPER
3.375MHz	750kHz	–48.37dBm	–103.39dBm
6.375MHz	5.25MHz	–37.97dBm	–95.72dBm
12.00MHz	6MHz	–37.33dBm	–95.55dBm
18.00MHz	6MHz	–37.13dBm	–96.33dBm
24.00MHz	6MHz	–37.15dBm	–95.91dBm

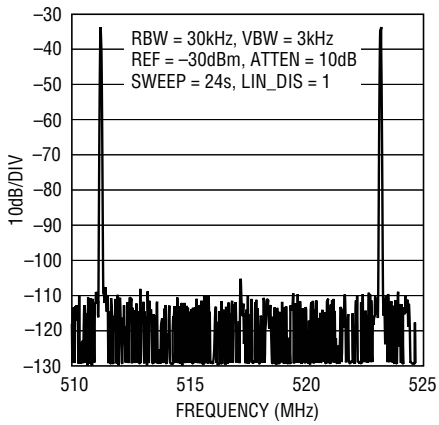
157 Carrier DOCSIS Gap Channel Narrowband ACLR, f_{DAC} = 2.5Gsps



GAP CHANNEL POWER = –96.45dBm, CENTER FREQ = 508MHz

OFFSET FREQ	BW	LOWER	UPPER
3.375MHz	750kHz	–48.05dBm	–47.93dBm
6.375MHz	5.25MHz	–36.61dBm	–36.50dBm
12.00MHz	6MHz	–36.32dBm	–36.27dBm
18.00MHz	6MHz	–36.48dBm	–36.45dBm
24.00MHz	6MHz	–36.54dBm	–36.57dBm

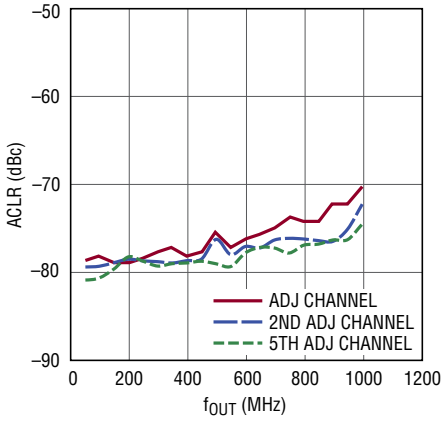
157 Carrier Tones with Gap Channel Narrowband ACLR, f_{DAC} = 2.5Gsps



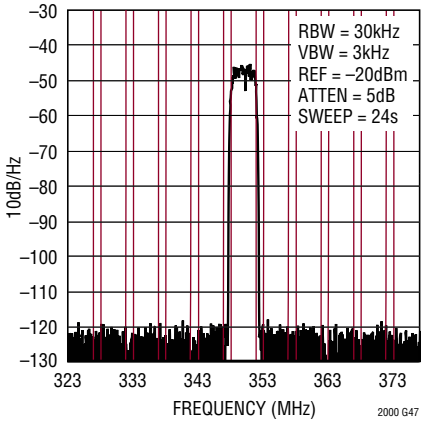
TYPICAL PERFORMANCE CHARACTERISTICS

I_{OUTFS} = 40mA, T_A = 25°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD33} = DV_{DD33} = 3.3V, R_{LOAD} = 12.5Ω, LIN_DIS = 0, LIN_ GN = 75% unless otherwise noted.

LTC2000-16 Single Carrier WCDMA ACLR vs f_{OUT}, f_{DAC} = 2.5Gsps



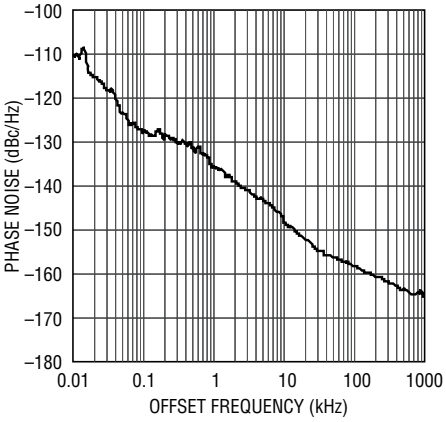
LTC2000-16 Single Carrier WCDMA ACLR at 350MHz, f_{DAC} = 2.5Gsps



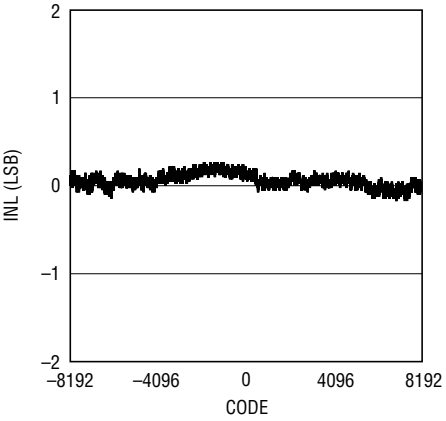
CARRIER POWER = –17.06dBm, CENTER FREQ = 350MHz

OFFSET FREQ	BW	LOWER	UPPER
5.00MHz	3.84MHz	–94.15dBm	–94.40dBm
10.00MHz	3.84MHz	–95.61dBm	–94.99dBm
15.00MHz	3.84MHz	–95.72dBm	–95.55dBm
20.00MHz	3.84MHz	–96.97dBm	–96.37dBm
25.00MHz	3.84MHz	–96.07dBm	–96.50dBm

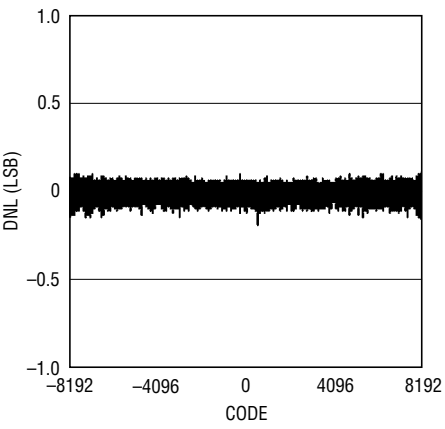
Additive Phase Noise, f_{OUT} = 65MHz, f_{DAC} = 2.5Gsps



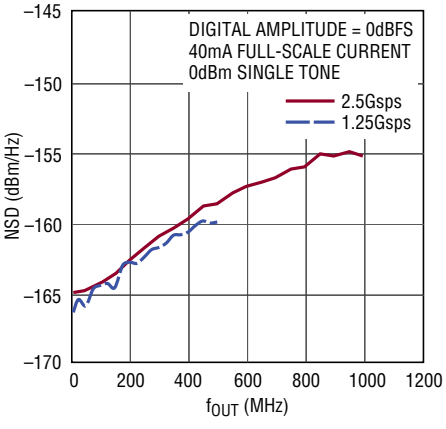
LTC2000-14 Integral Nonlinearity (INL)



LTC2000-14 Differential Nonlinearity (DNL)



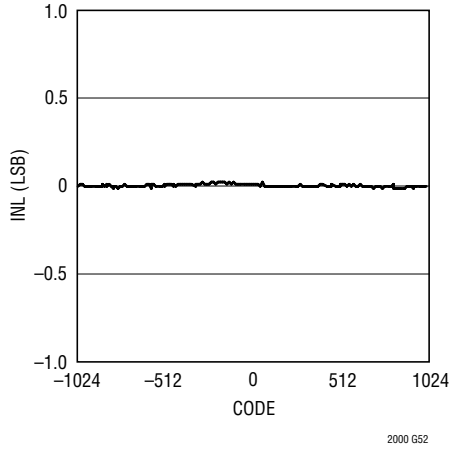
LTC2000-14 Single-Tone NSD vs f_{OUT} and f_{DAC}



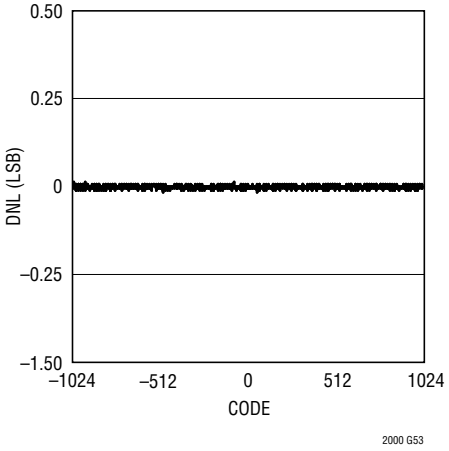
TYPICAL PERFORMANCE CHARACTERISTICS

I_{OUTFS} = 40mA, T_A = 25°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD33} = DV_{DD33} = 3.3V, R_{LOAD} = 12.5Ω, LIN_DIS = 0, LIN_ GN = 75% unless otherwise noted.

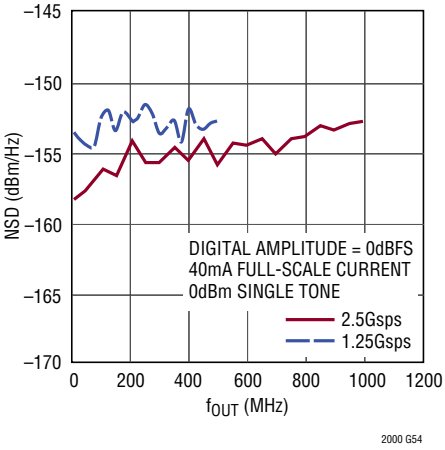
LTC2000-11 Integral Nonlinearity (INL)



LTC2000-11 Differential Nonlinearity (DNL)



LTC2000-11 Single-Tone NSD vs f_{OUT} and f_{DAC}



PIN FUNCTIONS

AV_{DD18}: 1.8V Analog Supply Voltage Input. 1.71V to 1.89V.

AV_{DD33}: 3.3V Analog Supply Voltage Input. 3.135V to 3.465V.

CKP, CKN: DAC Sample Clock Inputs. Maximum clock frequency (f_{DAC}) is 2500MHz. Clock signal should be AC coupled.

$\overline{CS}$: Serial Interface Chip Select Input. When $\overline{CS}$ is low, SCK is enabled for shifting data on SDI into the register. When $\overline{CS}$ is taken high, SCK is disabled and SDO is high impedance.

DAP[15:0], DAN[15:0]: Port A LVDS Data Inputs. Maximum data rate is 1.25Gbps. Port A is used only in dual-port mode. Connect to GND if not used. The data input format is two's complement.

DBP[15:0], DBN[15:0]: Port B LVDS Data Inputs. Maximum data rate is 1.25Gbps. In single-port mode, only Port B is used. In dual-port mode, the sample from Port B appears at $I_{OUTP/N}$ one cycle after the sample from Port A. The data input format is two's complement.

DCKIP, DCKIN: LVDS Data Clock Inputs. Maximum frequency (f_{DCKI}) is 625MHz. In dual-port mode, $f_{DCKI} = f_{DAC}/4$. In single-port mode, $f_{DCKI} = f_{DAC}/2$

DCKOP, DCKON: LVDS Data Clock Outputs. Maximum frequency is 625MHz. Select frequency ($f_{DAC}/4$ or $f_{DAC}/2$), output current (3.5mA or 7mA), and termination (none or 100Ω) using register 0x02.

DV_{DD18}: 1.8V Digital Supply Voltage Input. 1.71V to 1.89V.

DV_{DD33}: 3.3V Digital Supply Voltage Input. 3.135V to 3.465V.

FSADJ: Full-Scale Adjust Pin. The DAC full-scale current is 16 • (V_{REFIO}/R_{FSADJ}). Connect a 500Ω resistor from FSADJ to GND to set the full-scale current to 40mA.

GND: Ground.

I_{OUTP}, I_{OUTN}: DAC Analog Current Outputs. Differential output is nominally ±40mA. Maximum update rate is 2.5Gsps. The output current is evenly divided between I_{OUTP} and I_{OUTN} when the two's compliment DAC code is set to mid-scale (all zeros).

$\overline{PD}$ (Pin S1): Active Low Power-Down Input. When $\overline{PD}$ is low, the LTC2000 supply current is less than 440µA. To exit power-down mode switch $\overline{PD}$ high to SV_{DD}.

REFIO: Reference Voltage Input or Output. The 1.25V internal reference is available at the pin through a 10k internal resistor. May be overdriven with an external reference voltage between 1.1V and 1.4V.

SCK: Serial Interface Clock Input. Maximum frequency is 50MHz.

SDI: Serial Interface Data Input. Data on SDI is clocked in on the rising edge of SCK.

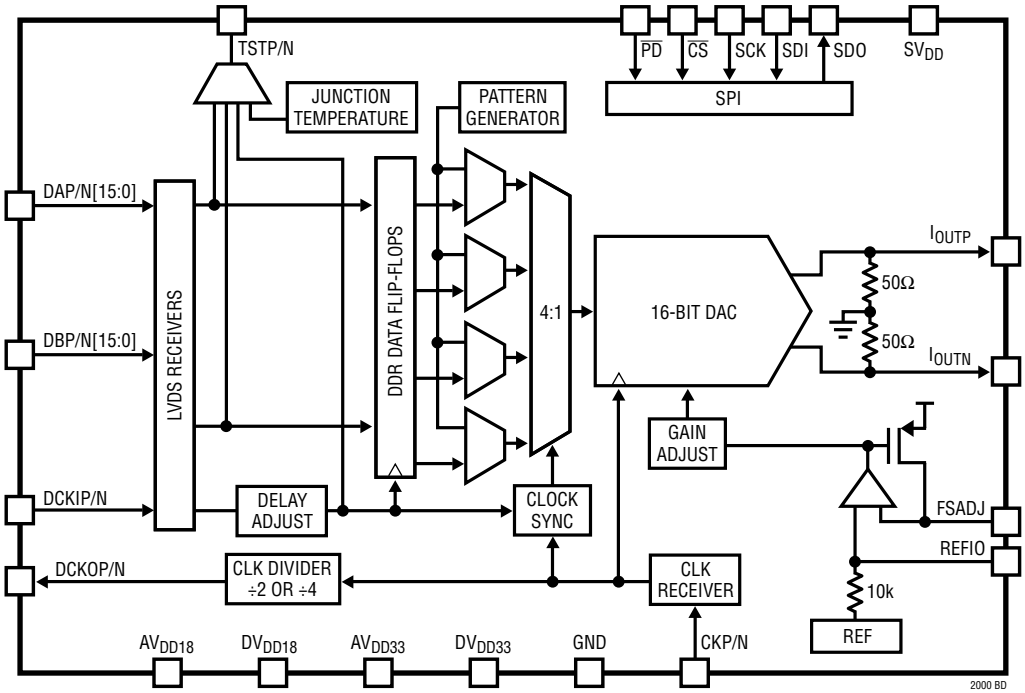
SDO: Serial Interface Data Output. Data is clocked out onto SDO by the falling edge of SCK. SDO is high impedance when $\overline{CS}$ is high.

SV_{DD}: SPI Supply Voltage Input. 1.71V to 3.465V.

TSTP, TSTN: Test Output Pins. May be optionally used to measure internal temperature or timing of LVDS inputs. See Measuring Internal Junction Temperature and Measuring LVDS Input Timing Skew sections in Applications Information. Use SPI internal registers 0x18 and 0x19 to control TSTP/N. Connect to GND if not used.

Note: For pin locations, refer to the Pin Locations section of this data sheet.

BLOCK DIAGRAM



TIMING DIAGRAMS

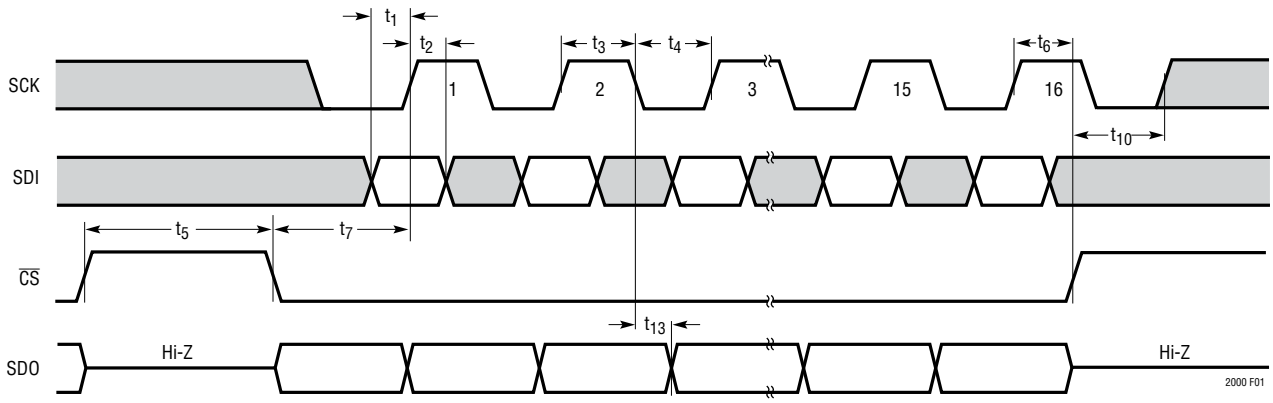


Figure 1. Serial Interface Timing

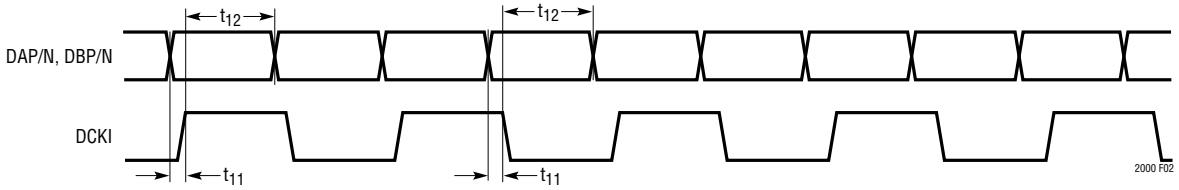


Figure 2. LVDS Interface Timing (DCKI_Q = 0, DCK_TADJ = 000)

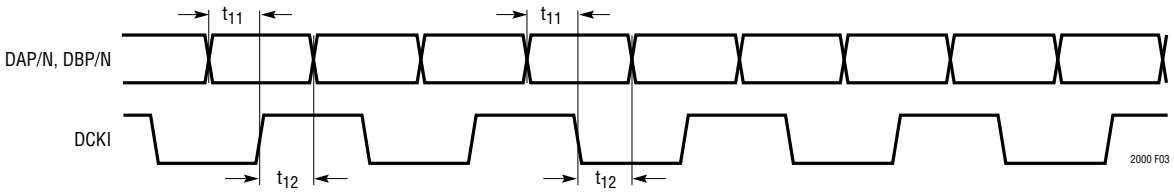


Figure 3. LVDS Interface Timing (DCKI_Q = 1)

OPERATION

Introduction

The LTC2000 is a family of 2.5Gsps current steering DACs. Three resolutions (16-, 14-, 11-bit) are available in a 170-lead BGA package. The LTC2000 features high output bandwidth and output current, while maintaining a clean output spectrum with low spurs, making it ideal for generating high frequency or broadband signals. The LTC2000 output current is nominally 40mA and is a scaled (16x) replica of the current flowing out of the FSADJ pin (nominally 2.5mA). The high output current allows flexibility in the output impedance, and the high FSADJ current and low scaling factor give excellent close-in phase noise performance.

The LTC2000 has two 16-, 14-, 11-bit wide LVDS or DHSTL-compatible parallel data input ports (DAP/N, DBP/N). Each data input port is capable of receiving two's complement data at up to 1.25Gbps using a double data rate (DDR) data input clock (DCKIP/N) at up to 625MHz. The DDR data input clock may be either in quadrature or in phase with the data arriving on the data input ports.

OPERATION

After incoming data is sampled by DCKIP/N, an internal multiplexer interleaves the data for resampling by the DAC sample clock (CKP/N). See Figures 4a and 4b. After a pipeline delay (latency) of up to 11 DAC sample clock cycles, the rising edges of CKP/N update the DAC code and a proportional differential output current is steered between the two outputs ($I_{OUTP/N}$). Note it takes about 3ns (aperture delay) from the CKP/N rising edge that updates a DAC code to the actual $I_{OUTP/N}$ transition for that DAC code.

An internal clock synchronizer monitors the incoming phase of DCKIP/N and chooses the appropriate phase for the multiplexer control signals to ensure that the data is sampled correctly by CKP/N. The LTC2000 also generates an LVDS clock output (DCKOP/N) by dividing the sample clock frequency to simplify clocking of the host FPGA or ASIC. Additional features such as pattern generation, LVDS loopout, and junction temperature sensing simplify system development and testing.

The serial peripheral interface (SPI) port allows configuration and read back of the internal registers which control the above functions.

Dual-Port Mode

In dual-port mode, data is written to both ports A and B simultaneously and then subsequently interleaved inside the LTC2000, allowing DAC output sampling rates of up to 2.5Gsps. Figures 4a and 4b show a simplified block diagram and sample waveforms for dual-port operation.

The LVDS data input ports A and B are sampled on both the falling and rising edges of the DDR data input clock (DCKIP/N) by four groups of flip-flops. The contents of these flip-flops are then interleaved by the 4:1 MUX and sampled by the DAC sample clock (CKP/N) at frequencies up to 2.5GHz, with data from port A (DAP/N) preceding data from port B (DBP/N) at the DAC output.

Note that the sample clock (CKP/N) frequency is always four times the DDR data input clock (DCKIP/N) frequency in dual-port mode. For example, to use the DAC at 2.5Gsps, apply a 2.5GHz clock to CKP/N and a 625MHz clock to DCKIP/N and send data into both ports A and B (DAP/N, DBP/N) at 1.25Gsps per port.

Latency is defined as the delay from the DCKIP/N transition that samples a DAC code to the CKP/N rising transition which causes that sample to appear at the DAC output $I_{OUTP/N}$. In dual-port mode the latency from DAP/N to $I_{OUTP/N}$ is 10 sample clock cycles and the latency from DBP/N to $I_{OUTP/N}$ is 11 cycles, starting from the CKP/N rising edge that immediately follows the DCKIP/N transition that sampled the DAC code (Figure 4b).

Single-Port Mode

In single-port mode, data is written to port B (DBP/N) only, allowing DAC output sampling rates of up to 1.25Gsps. Figures 4c and 4d show a block diagram and sample waveforms representing single-port operation. Samples are written to port B (DBP/N) and sampled on both the falling and rising edges of the DDR data input clock (DCKIP/N) by two groups of flip-flops. The contents of these flip-flops are then interleaved into a single data stream by the 2:1 MUX and sampled by the DAC sample clock (CKP/N) at frequencies up to 1.25GHz.

Note that in single-port mode the sample clock (CKP/N) frequency is always twice the DDR data input clock (DCKIP/N) frequency. For example, to use the DAC at 1.25Gsps, apply a 1.25GHz clock to CKP/N and a 625MHz clock to DCKIP/N and send data into port B (DBP/N) at 1.25Gsps. In single-port mode, port A (DAP/N) should be grounded. Due to the design of the internal clock synchronizer in single port mode, there is a half cycle shift in the single port latency. The latency from DBP/N to $I_{OUTP/N}$ in single-port mode is 7.5 sample clock cycles, starting from the CKP/N falling edge that immediately follows the DCKIP/N transition that sampled the DAC code (Figure 4d).

OPERATION

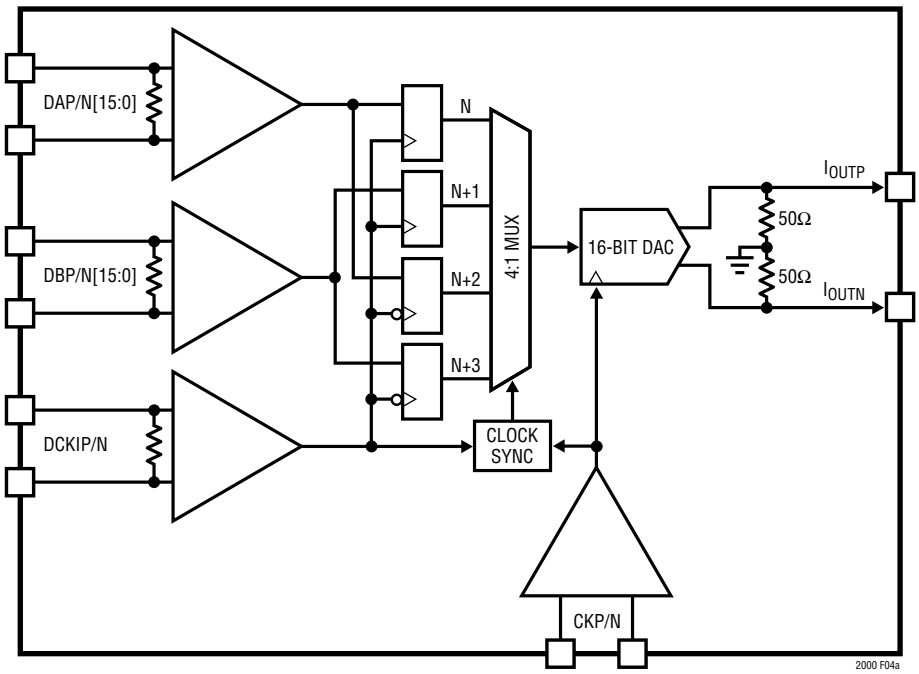


Figure 4a. Simplified Block Diagram – Dual-Port Operation

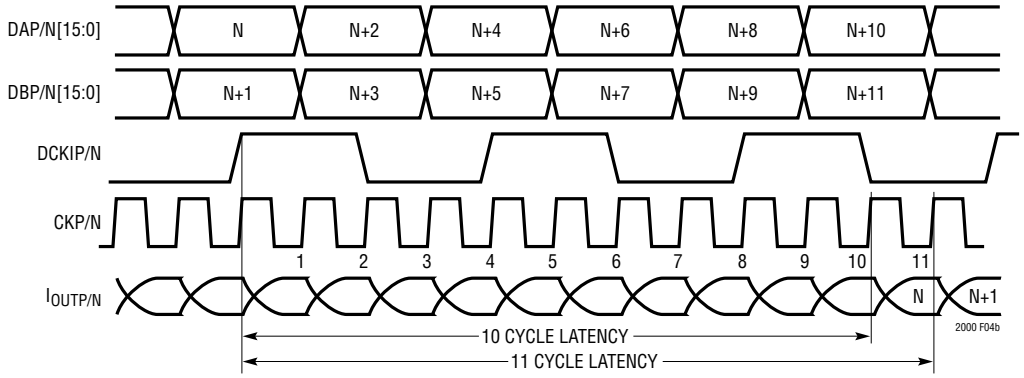


Figure 4b. Sample Waveforms – Dual-Port Operation

OPERATION

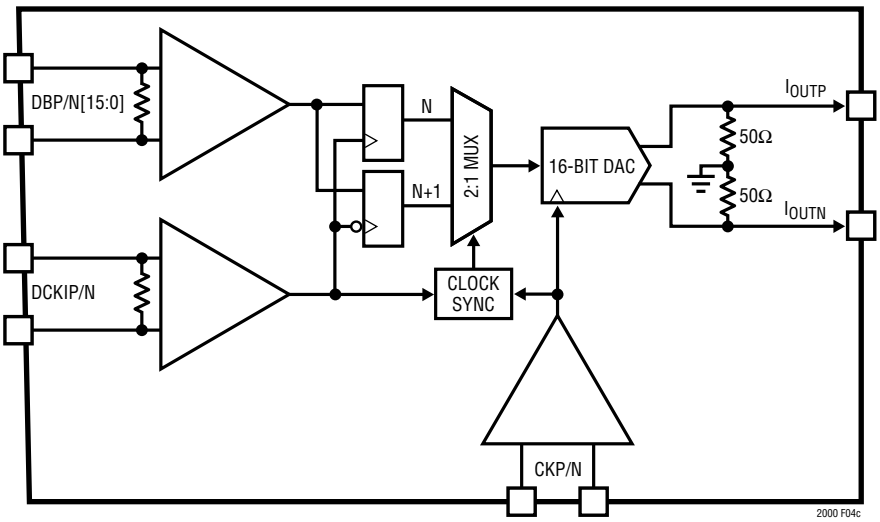


Figure 4c. Simplified Block Diagram – Single-Port Operation

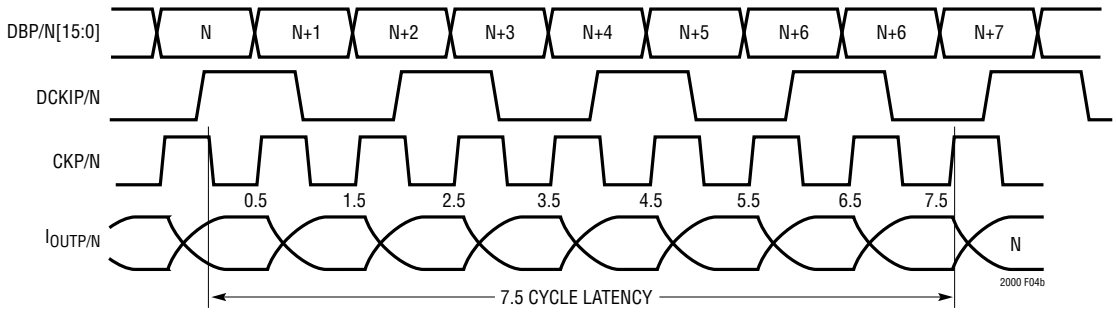


Figure 4d. Sample Waveforms – Single-Port Operation

OPERATION

Serial Peripheral Interface (SPI)

The LTC2000 uses an SPI/MICROWIRE-compatible 3-wire serial interface to configure and read back internal registers. The SV_{DD} pin is the power supply for the SPI interface (nominally 1.8V or 3.3V). The $\overline{CS}$ input is level triggered. When this input is taken low, it acts as a chip-select signal, enabling the SDI and SCK buffers and the SPI input register. After the falling edge of $\overline{CS}$, the first data byte clocked into SDI by the rising edges of SCK is the command byte. The first bit of the command byte signifies a read (R/W = 1) or write (R/W = 0) operation. The next seven bits contain the register address, which completes the command byte.

The next byte transferred after the command byte is the data byte. For write operations, the data byte is written to the SPI register specified by the register address set in the command byte. During read operations, the data byte is ignored, and the contents of the selected SPI register are clocked out onto the SDO pin by the falling edges of SCK. During write operations, SDO will be low. When $\overline{CS}$ goes high, SDO is high impedance. Figure 5 shows the SPI command and data input.

Users wishing to transfer multiple bytes of data at once may do so, with the address for each subsequent byte automatically incremented internally. The address will continue to increment until $\overline{CS}$ goes high or until address bits A[4:0] reach 0x1F, after which subsequent bytes will continue to be written to the same address.

Reserved address and bit locations should not be written with any value other than zero. Table 11 contains a full description of all internal SPI registers and can be found in the SPI Register Summary section.

Power-On Reset

The internal power-on reset circuit will reset the LTC2000 upon power up and clear the output to mid-scale when power is first applied, making system initialization consistent and repeatable. All internal registers are reset to 0x00, with the exception of register address 0x08, which resets to 0x08. A software reset can also be applied by using the SPI interface to load 0x01 into register address 0x01, setting SW_RST to 1 (see Table 1). Note that the SW_RST bit is automatically cleared when $\overline{CS}$ returns high. It is recommended that users perform a software reset once all power supplies are stable.

Power Down

Users wishing to save power when the DAC is not being used may reduce the supply current to less than 440µA by pulling the $\overline{PD}$ pin to GND or by writing to register 0x01 to set FULL_PD = 1. Alternatively, users may power down unused portions of the chip individually using DAC_PD, CK_PD, DCKO_DIS, DCKI_EN, DA_EN, and DB_EN in registers 0x01, 0x02, 0x03, and 0x04 (see Table 1).

Reference Operation

The LTC2000 has a 1.25V internal bandgap voltage reference that drives the REFIO pin through a 10k internal resistor, and should be buffered if driving any additional external load. For noise performance, a 0.1µF capacitor to GND is recommended on the REFIO pin, but is not required for stability.

In the case where an external reference would be preferred, the external reference is simply applied to the REFIO pin and overdrives the internal reference. The acceptable external reference range is 1.1V to 1.4V.

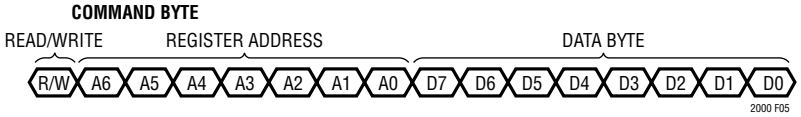


Figure 5. SPI Command and Data Input

OPERATION

Table 1. Power-On Reset and Power-Down SPI Registers

ADDRESS	BIT	NAME	DESCRIPTION
0x01	0	SW_RST	Software Reset. Set SW_RST = 1 to restore all registers to their power-on reset state. SW_RST is automatically cleared when $\overline{CS}$ returns high. All registers reset to 0x00, except address 0x08 which resets to 0x08.
	1	DAC_PD	DAC Power Down. Set DAC_PD = 1 to power down the DAC and FSADJ bias circuits.
	2	FULL_PD	Full Power Down. Set FULL_PD = 1 to power down all active circuits on the chip and reduce the supply current to less than 100µA.
0x02	0	CK_PD	CKP/N Clock Receiver Power Down. CKP/N clock receiver is powered down when CK_PD = 1.
	4	DCKO_DIS	DCKOP/N Output Disable. Set DCKO_DIS = 1 to power down the DCKO LVDS transmitter. For DCKO_DIS = 1, DCKOP/N are high impedance.
0x03	0	DCKI_EN	DCKIP/N Clock Receiver Enable. Set DCKI_EN = 1 to enable the DCKI clock receiver.
0x04	0	DA_EN	DAC Data Port A LVDS Receiver Enable. Set DA_EN = 1 to enable port A (DAP/N) LVDS receivers. For DA_EN = 0, port A LVDS receivers are powered down and port A data will be zeroes.
	1	DB_EN	DAC Data Port B LVDS Receiver Enable. Set DB_EN = 1 to enable port B (DBP/N) LVDS receivers. For DB_EN = 0, port B LVDS receivers are powered down and port B data will be zeroes.

Note: Registers 0x01 to 0x04 reset to 0x00 (default).

Setting the Full-Scale Current

The full-scale DAC output current (I_{OUTFS}) is nominally 40mA, but can be adjusted as low as 10mA or as high as 60mA. The full-scale current is set by placing an external resistor (R_{FSADJ}) between the FSADJ pin and GND. An internal reference control loop amplifier sets the current flowing through R_{FSADJ} such that the voltage at FSADJ is equal to the voltage at REFIO, which is typically 1.25V. I_{OUTFS} is set as a scaled replica of the current flowing out of the FSADJ pin (I_{FSADJ}):

$$I_{FSADJ} = \frac{V_{REFIO}}{R_{FSADJ}}$$

$$I_{OUTFS} = 16 \bullet I_{FSADJ} \bullet \frac{256}{256 + GAIN\_ADJ}$$

where GAIN_ADJ is a 6-bit two's complement number from –32 to 31 (nominally 0) which can be programmed using SPI register 0x09 as shown in Table 2. For example, for R_{FSADJ} = 500Ω, V_{REFIO} = 1.25V, and GAIN_ADJ = 0x00, the control loop will force 1.25V at the FSADJ pin, causing 2.5mA to flow through R_{FSADJ}. I_{OUTFS} will then be set to 16 • 2.5mA = 40mA.

Changing GAIN_ADJ to 0x1F (+31) will decrease the current by 10.8% to 35.7mA. Changing GAIN_ADJ to 0x20 (–32) will increase the current by 14.3% to 45.7mA.

Note that GAIN_ADJ appears in the denominator of the equation for I_{OUTFS}, so the adjustment resolution varies from 0.5% to 0.3% per step. The circuit shown in Figure 6 may be used to vary the full-scale output current beyond the range of the GAIN_ADJ register.

DAC linearity and harmonic distortion may be degraded when using full-scale currents other than 40mA. The full-scale current must not exceed 60mA, and is recommended to be at least 10mA.

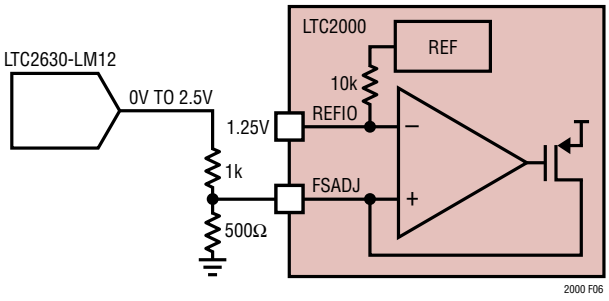


Figure 6. LTC2000 Full-Scale Adjust from 20mA to 60mA

OPERATION

Table 2. Full-Scale Gain Adjustment

ADDRESS	BIT	NAME	DESCRIPTION			
			GAIN_ADJ (HEX)	GAIN_ADJ (DECIMAL)	GAIN ADJUSTMENT	FULL-SCALE CURRENT (R_{FSADJ} = 500Ω, V_{REFIO} = 1.25V)
0x09	[5:0]	GAIN_ADJ	0x1F	+31	89.2%	35.68mA
			0x1E	+30	89.5%	35.80mA
			—	—	—	—
			0x01	+1	99.6%	39.84mA
			0x00	0	100.0%	40.00mA
			0x3F	–1	100.4%	40.16mA
			—	—	—	—
			0x21	–31	113.8%	45.51mA
			0x20	–32	114.3%	45.71mA

Note: Register 0x09 resets to 0x00 (default).

DAC Transfer Function

The LTC2000 contains an array of current sources that are steered through differential switches to either I_{OUTP} or I_{OUTN}, depending on the DAC code programmed through the LVDS parallel interface. The LTC2000 uses a 16-/14-/11-bit two's complement DAC code. The complementary current outputs, I_{OUTP} and I_{OUTN}, source current from 0mA to I_{OUTFS}. For I_{OUTFS} = 40mA (nominal), I_{OUTP} swings from 0mA (for zero-scale DAC code) to 40mA (for full-scale DAC code). I_{OUTN} is complementary to I_{OUTP}. When the DAC code is set to mid-scale (all zeros), I_{OUTFS} is evenly divided between I_{OUTP} and I_{OUTN}. I_{OUTP} and I_{OUTN} are given by the following formulas:

LTC2000-16:

$I_{OUTP} = I_{OUTFS} \bullet (CODE + 32768)/65536 + I_{OUTCM}$

$I_{OUTN} = I_{OUTFS} \bullet (32768 – CODE – 1)/65536 + I_{OUTCM}$

LTC2000-14:

$I_{OUTP} = I_{OUTFS} \bullet (CODE + 8192)/16384 + I_{OUTCM}$

$I_{OUTN} = I_{OUTFS} \bullet (8192 – CODE – 1/4)/16384 + I_{OUTCM}$

LTC2000-11:

$I_{OUTP} = I_{OUTFS} \bullet (CODE + 1024)/2048 + I_{OUTCM}$

$I_{OUTN} = I_{OUTFS} \bullet (1024 – CODE – 1/32)/2048 + I_{OUTCM}$

The DAC code ranges from $–2^{N-1}$ to $2^{N-1} – 1$, with N being the DAC resolution (16/14/11). I_{OUTCM} is a small, constant common-mode output current that is equal to approximately 0.2% full-scale, or 80µA for I_{OUTFS} = 40mA.

The LTC2000 differential output currents typically drive a resistive load either directly or drive an equivalent resistive load through a transformer (see the Output Configurations section). The voltage outputs generated by the I_{OUTP} and I_{OUTN} outputs currents are then:

$V_{OUTP} = I_{OUTP} \bullet R_{LOAD}$

$V_{OUTN} = I_{OUTN} \bullet R_{LOAD}$

$V_{DIFF} = V_{OUTP} – V_{OUTN} = (I_{OUTP}\text{-}I_{OUTN}) \bullet R_{LOAD}$

Substituting the values above gives:

LTC2000-16:

$V_{DIFF} = V_{REFIO} \bullet (R_{LOAD}/R_{FSADJ}) \bullet (2 \bullet CODE + 1)/4096$

LTC2000-14:

$V_{DIFF} = V_{REFIO} \bullet (R_{LOAD}/R_{FSADJ}) \bullet (2 \bullet CODE + 1/4)/1024$

LTC2000-11:

$V_{DIFF} = V_{REFIO} \bullet (R_{LOAD}/R_{FSADJ}) \bullet (2 \bullet CODE + 1/32)/128$

Note that the gain of the DAC depends on the ratio of R_{LOAD} to R_{FSADJ}, and the gain error tempco is affected by the temperature tracking of R_{LOAD} with R_{FSADJ}.

Analog Outputs ($I_{OUTP/N}$)

The two complementary analog outputs ($I_{OUTP/N}$) have low output capacitance that, with appropriate R_{LOAD} values, can achieve high output bandwidths of 2.1GHz. The analog outputs also have an internal impedance of 50Ω to GND that will affect the calculation of R_{LOAD} and the

OPERATION

output voltage swing of the DAC. For example, loading both I_{OUTP} and I_{OUTN} with external 50Ω resistors to GND will cause R_{LOAD} to equal 25Ω. Assuming an I_{OUTFS} of 40mA, V_{DIFF} will swing between 1V and –1V.

The specified output compliance voltage range is ±1V. Above 1V, the differential current steering switches will start to approach the transition from saturation to linear region and degrade DAC linearity. Below –1V protection diodes will limit the swing of the DAC. Small voltage swings and low common-mode voltages typically result in the best distortion performance.

DAC Sample Clock (CKP/N)

The DAC sample clock (CKP/N) is used to update the LTC2000 outputs at rates of up to 2.5Gsps. Provide a clean, low jitter differential clock at up to 2.5GHz on pins CKP/N (see Generating the DAC Sample Clock section). The DC bias point of CKP/N is set internally through a 5kΩ impedance. A 0dBm DAC sample clock should be sufficient to obtain the performance shown in the Typical Performance Characteristics section. For best jitter and phase noise, AC couple a differential clock onto CKP/N with balanced duty cycle and the highest possible amplitude and slew rate.

Use SPI register 0x02 to control the DAC sample clock receiver (Table 3). The LTC2000 contains a clock detector which sets CK_OK = 1 if the DAC sample clock is present and f_{DAC} > 50MHz. When the sample clock is not present (CK_OK = 0), the DAC output is forced to mid-scale and the internal data path is held at reset. Set CK_PD = 1 to power down the clock receiver and save power when the DAC is not being used. Note that at power-on reset, the DAC sample clock receiver is on by default.

Divided Clock Output (DCKOP/N)

The LTC2000 contains a programmable clock divider and LVDS transmitter which provide a divided version (either $f_{DAC}/4$ or $f_{DAC}/2$) of the DAC sample clock for use by the host FPGA or ASIC. Use SPI register 0x02 to control DCKOP/N (Table 3). At power-on reset, the LVDS transmitter will provide a clock signal at $f_{DAC}/4$ with a 3.5mA differential output current.

If desired, set DCKO_DIV = 1 to change the divided clock output frequency to $f_{DAC}/2$. The output current can be increased to 7mA by setting DCKO_ISEL = 1, and an internal 100Ω differential termination can be enabled by setting DCKO_TRM = 1. Set DCKO_DIS = 1 to disable the LVDS transmitter and save power when not in use.

LVDS Data Clock Input (DCKIP/N)

The DAC code data written to the LTC2000 is captured on both the rising and falling edges of DCKIP/N. For single-port operation, provide a DDR clock at half the DAC sample clock frequency ($f_{DCKI} = f_{DAC}/2$). To use a 1.25GHz sample clock in single-port mode, provide a 625MHz clock on DCKIP/N. For dual-port operation, provide a DDR clock at one quarter the DAC sample clock frequency ($f_{DCKI} = f_{DAC}/4$). To use a 2.5GHz sample clock in dual-port mode, provide a 625MHz clock on DCKIP/N.

Table 3. DAC Sample Clock, and Divided Clock Output SPI Registers

ADDRESS	BIT	NAME	DESCRIPTION
0x02	0	CK_PD	CKP/N Clock Receiver Power Down When CK_PD = 1
	1	CK_OK	CKP/N Clock Present Indicator. When CK_OK = 1, clock is present at CKP/N pins and f_{DAC} > 50MHz. When CK_OK = 0, DAC output is forced to mid-scale. CK_OK is read only.
	4	DCKO_DIS	DCKOP/N Output Disable. Set DCKO_DIS = 1 to power down the DCKO LVDS transmitter. For DCKO_DIS = 1, DCKOP/N are high impedance.
	5	DCKO_DIV	DCKOP/N Divide Select. When DCKO_DIV = 0, $f_{DCKOP/N} = f_{DAC}/4$. When DCKO_DIV = 1, FDCKOP/N = $f_{DAC}/2$.
	6	DCKO_ISEL	DCKOP/N Output Current Select. When DCKO_ISEL = 0, output current is 3.5mA. When DCKO_ISEL = 1, output current is 7mA.
	7	DCKO_TRM	DCKOP/N Internal Termination On. When DCKO_TRM = 0, there is no internal termination at DCKOP/N. When DCKO_TRM = 1, there is 100Ω between DCKOP and DCKON.

Note: Register 0x02 resets to 0x00 (default).

OPERATION

Table 4. LVDS Clock SPI Registers

ADDRESS	BIT	NAME	DESCRIPTION		
0x03	0	DCKI_EN	DCKIP/N Clock Receiver Enable. DCKI_EN = 1 enables LVDS clock receiver.		
	1	DCKI_OK	DCKIP/N Clock Present Indicator. When DCKI_OK = 1, clock is present at DCKIP/N pins and $f_{DCKIP/N}$ > 25MHz. When DCKI_OK = 0, DAC output is forced to mid-scale unless pattern generator is enabled (PGEN_EN = 1). DCKI_OK is read only.		
	2	DCKI_Q	DCKIP/N Quadrature Phase Select. For DCKI_Q = 0, DCKIP/N should be in phase with DAP/N and DBP/N. Set DCKI_Q = 1 to use DCKI in quadrature with DAP/N and DBP/N.		
	[6:4]	DCKI_TADJ	DCKIP/N Delay Adjust. Use with DCKI_Q = 0 to adjust delay of DCKIP/N relative to DAP/N and DBP/N. For DCKI_Q = 1, DCKIP/N delay matches DAP/N and DBP/N and is unaffected by DCKI_TADJ.		
				NOMINAL DCKIP/N DELAY	
			DCKI_TADJ	DCKI_Q = 1	DCKI_Q = 0
			110	0ps	230ps
			111	0ps	315ps
			000	0ps	400ps (Default)
			001	0ps	485ps
			010	0ps	570ps

Note: Register 0x03 resets to 0x00 (default).

Use SPI register 0x03 to control the LVDS data clock input (see Table 4). Setting DCKI_EN=1 will enable the LVDS receiver at DCKIP/N. The LTC2000 contains a clock detector which sets DCKI_OK=1 if the data input clock is present and has a frequency greater than 25MHz (f_{DCKI} > 25MHz). When the data clock is not present (DCKI_OK = 0), the DAC output is forced to mid-scale and the internal data path is held at reset.

For maximum setup/hold margin, set DCKI_Q = 1 and provide DCKIP/N in quadrature (90° out of phase) with the data on DAP/N and DBP/N (Figure 3 in the Timing Diagrams section). For DCKI_Q = 1, the internal delays on DCKIP/N, DAP/N, and DBP/N are nominally matched.

Alternatively, it is possible to leave DCKI_Q = 0 and provide the clock at DCKIP/N in phase with the data on DAP/N and DBP/N (see Figure 2 of the Timing Diagram section). In this case, an internal 400ps delay on DCKIP/N is used to provide setup/hold margin. Note that for DCKI_Q = 0, supply and temperature variation may reduce the setup/hold margin on the bus by up to 150ps. If desired, users may use the DCKI_TADJ bits in register 0x03 to adjust the 400ps internal DCKIP/N delay with a typical resolution of 85ps.

Board trace lengths on DCKIP/N, DAP/N, and DBP/N must be carefully matched to ensure that phase alignment is maintained on all inputs. If desired during development, users may observe the relative timing of neighboring LVDS inputs on the TSTP/N pins (refer to the Measuring LVDS Input Timing Skew section).

LVDS Data Input Ports (DAP/N, DBP/N)

The LTC2000-16/LTC2000-14/LTC2000-11 allow for DAC Code Data to be applied through one or two parallel 16-/14-/11-bit LVDS ports (DAP/N, DBP/N). Each port can run up to 1.25Gbps using a double-data-rate (DDR) LVDS data clock (DCKIP/N) at frequencies up to 625MHz. The data input format is two's complement.

There are two modes of operation for applying the DAC code to the LTC2000 — single-port mode and dual-port mode. Single port operation uses only LVDS port B (DBP/N) and allows sample rates of up to 1.25Gsps. Dual port operation uses both LVDS ports (DAP/N and DBP/N) and allows sample rates up to 2.5Gsps.

Use SPI register 0x04 to control the LVDS data input ports (see Table 5). After the clocks have stabilized and the synchronizer has initialized itself, set DATA_EN = 1 to allow the data from ports A and B to be used to update the DAC code. Clear DATA_EN = 0 to mute the DAC and force the DAC code to mid-scale as desired.

OPERATION

Table 5. LVDS Data Input SPI Registers

ADDRESS	BIT	NAME	DESCRIPTION
0x04	0	DA_EN	DAC Data Port A LVDS Receiver Enable. DA_EN = 1 enables port A receivers. For DA_EN = 0, receivers are powered down and port A data is 0x0000.
	1	DB_EN	DAC Data Port B LVDS Receiver Enable. DB_EN = 1 enables port B receivers. For DB_EN = 0, receivers are powered down and port B data is 0x0000.
	2	DATA_SP	DAC Data Single Port Mode Select. DATA_SP = 1 sets single port mode and only port B data is used to update the DAC code. DATA_SP = 0 sets dual-port mode and data from both ports A and B are used.
	3	DATA_EN	DAC Data Enable. DATA_EN = 0 mutes the DAC output by forcing the DAC code to mid-scale. DATA_EN = 1 allows data from data ports A and B to be used to update the DAC code.

Note: Register 0x04 resets to 0x00 (default).

For single port operation, set DATA_SP = 1, DA_EN = 0, DB_EN = 1 and provide data to LVDS port B (DBP/N) only. For dual port operation leave DATA_SP = 0, set DA_EN = 1 and DB_EN = 1, and provide interleaved data to LVDS ports A and B (DAP/N, DBP/N). The data on port A will precede the data on port B at the DAC output.

Clock Synchronizer

Figure 7 shows a simplified block diagram of the internal clock synchronizer. The synchronizer monitors the incoming phase of DCKIP/N using a pair of internal phase comparators. The synchronizer then automatically adjusts the

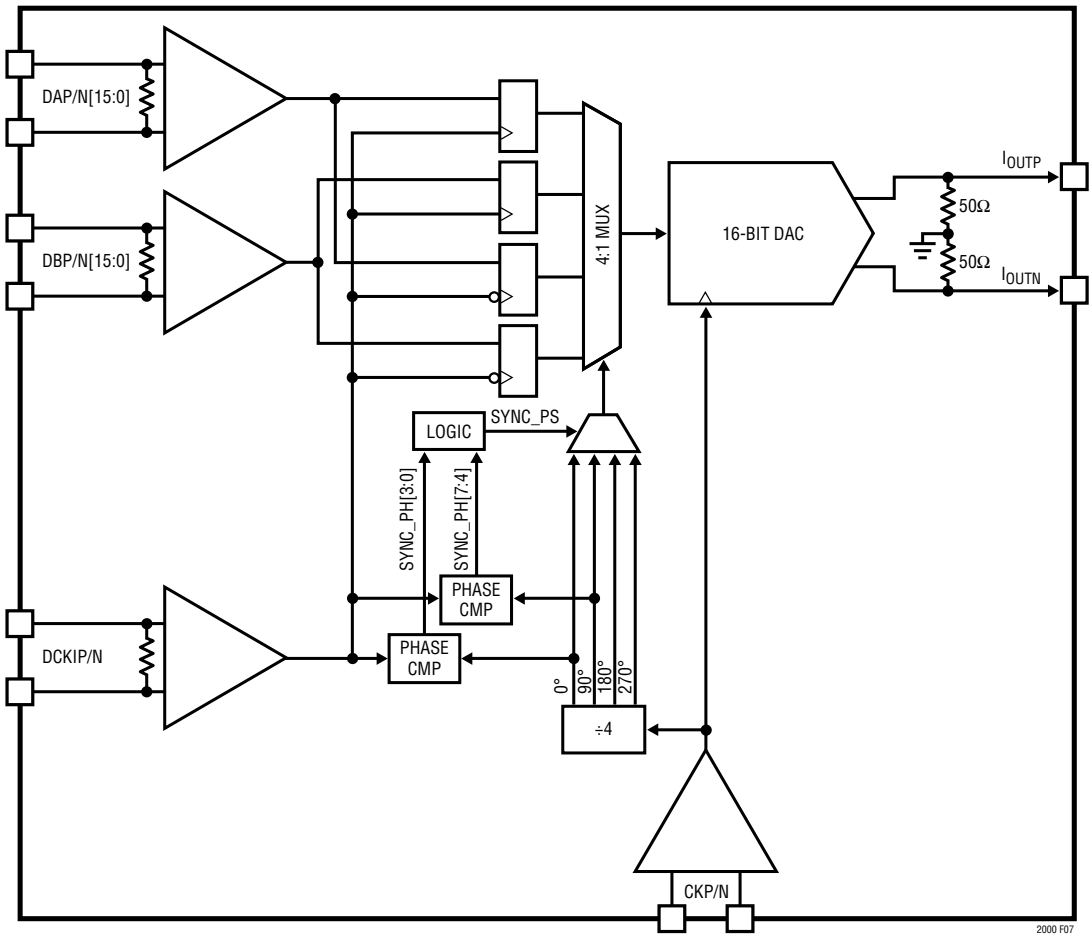


Figure 7. Simplified Block Diagram — Clock Synchronizer in Dual-Port Mode

OPERATION

phase of the MUX control signals as needed to track any slow drift in the phase between the DCKIP/N and CKP/N due to supply and temperature variation. This ensures that data is sampled correctly by CKP/N.

Use SPI registers 0x05 and 0x06 (Table 6) to observe and control the operation of the synchronizer. Upon power-up, apply clocks to CKP/N and DCKIP/N and set DCKI_EN = 1 (register 0x03) to enable the LVDS data clock receiver. Allow at least 1ms after the clocks have stabilized for the synchronizer to initialize, after which the LTC2000 is ready to accept LVDS input data.

The synchronizer uses phase comparators to monitor the phase of the data input clock relative to the sample clock divider which controls the MUX. The outputs of these phase comparators (SYNC_PH) may be observed in register 0x06.

The SYNC_PS bits control the phase of the data multiplexer. For SYNC_MSYN = 0, the SYNC_PS bits are read-only and are automatically adjusted by the synchronizer as needed, based upon the phase of DCKIP/N indicated by SYNC_PH.

Users may choose to override the automatic synchronizer by setting SYNC_MSYN = 1 and writing values manually to SYNC_PS to set the phase of the internal multiplexer. When using SYNC_MSYN = 1, users must monitor SYNC_PH and adjust SYNC_PS as needed according to Table 6. For further details see the Synchronizing Multiple LTC2000s section.

Table 6. Clock Synchronizer SPI Registers

ADDRESS	BIT	NAME	DESCRIPTION		
0x05	[1:0]	SYNC_PS	Synchronizer Phase Select. Selects phase of internal data multiplexer. SYNC_PS is read-only when SYNC_MSYN = 0.		
	2	SYNC_MSYN	Synchronizer Manual Mode Select. When SYNC_MSYN = 0, SYNC_PS is set automatically by the clock synchronizer based upon SYNC_PH. When SYNC_MSYN = 1, SYNC_PS must be set by the user.		
0x06	[7:0]	SYNC_PH	Synchronizer Phase Comparator Outputs. SYNC_PH indicates the phase of the LVDS data clock (DCKIP/N) relative to the DAC sample clock (CKP/N) divider used to control the data multiplexer. SYNC_PH is read only.		
				OPTIMAL SYNC_PS SETTING	
			SYNC_PH	DUAL-PORT MODE	SINGLE-PORT MODE
			0x03	10	00
			0x04	10	00
			0x05	10	00
			0x15	10	00
			0x25	10	00
			0x35	00	10
			0x45	00	10
			0x55	00	10
			0x54	00	10
			0x53	00	10
			0x52	01	10
			0x51	01	10
			0x50	01	10
			0x40	01	10
			0x30	01	10
			0x20	11	00
			0x10	11	00
			0x00	11	00
			0x01	11	00
			0x02	11	00

Note: Registers 0x05 and 0x06 reset to 0x00 (default).

OPERATION

Minimizing Harmonic Distortion

The LTC2000 contains proprietary dynamic linearization circuitry which dramatically reduces 3rd order harmonic distortion in the DAC output. SPI registers 0x07 and 0x08 are used to control these circuits (see Table 7). Optimal performance is normally achieved by setting LIN_VMX and LIN_VMN (register 0x08) to correspond to the maximum and minimum voltages expected at $I_{OUTP/N}$. At power-on reset the default values are 0b1000 and 0b0000, which are appropriate for $I_{OUTP/N}$ swinging between 500mV and GND. If an application requires a different voltage swing, LIN_VMX and LIN_VMN can be programmed by writing to register 0x08 (see Table 7). For applications in which $I_{OUTP/N}$ swing below GND, use LIN_VMN = 0b0000.

In some applications where 2-tone intermodulation distortion (IMD) is a critical specification, it may be desired to vary the amount of 3rd order harmonic correction. For high sampling frequencies (f_{DAC} > 2Gsps), adjusting LIN_GN in register 0x07 (see Table 7) can improve 2-tone intermodulation distortion at the expense of higher 3rd order harmonic distortion. For best IMD performance at high sampling frequencies, users may also choose to disable dynamic linearization by setting LIN_DIS = 1. SFDR and IMD curves in the Typical Performance Characteristics section show more detail regarding this effect. Note that for f_{DAC} < 2Gsps, it is recommended to leave the dynamic linearization enabled.

Measuring LVDS Input Timing Skew

It is important to ensure that the LVDS inputs (DCKIP/N, DAP/N, DBP/N) are well aligned. Skew between clock and data lines, for example due to board trace length mismatch or output timing mismatch inside the host FPGA or ASIC, will degrade the setup and hold margin of the incoming data. The LTC2000 includes an internal test multiplexer which may be used during development to verify timing alignment by comparing the timing of LVDS inputs one pair at a time through the TSTP/N pins.

Use SPI register 0x18 to control this test multiplexer (see Table 8). Be sure TDIO_EN = 0 in register 0x19 and then set LMX_EN = 1 to enable the test multiplexer output. The signal from the LVDS data input will be driven onto TSTP/N by an NMOS differential pair steering a 6.6mA sink current onto an external load. Connect a pair of 50Ω resistors from TSTP/N to 3.3V and observe TSTP/N on a high speed oscilloscope.

Apply clocks to CKP/N and DCKIP/N and apply the pattern shown in Figure 8 to port B for single-port mode or ports A and B for dual-port mode. This pattern is designed to simplify comparison of rising-to-rising and falling-to-falling edge timing for each input pair. Set LMX_ADR to select a pair of LVDS inputs for timing comparison. Set LMX_MSEL = 0 to observe the first signal at TSTP/N. Set LMX_MSEL = 1 to observe the second signal with inverted output polarity.

For example, to compare DB15P/N to DCKIP/N, first write 0x60 to register 0x18 to set LMX_EN = 1, LMX_ADR = 10000, and LMX_SEL = 0. The signal from DB15P/N will be driven onto TSTP/N. Write 0x61 to register 0x18 to set LMX_SEL = 1 and cause DCKIP/N to appear at TSTP/N with inverted polarity.

Record the skew between the two signals and repeat this measurement for each pair of inputs. After all pairs have been measured, add the skews to calculate the total skew from DCKIP/N to each data input (DAP/N, DBP/N). In this way the skew of all LVDS data inputs (DAP/N, DBP/N) relative to DCKIP/N can be accurately measured to within 100ps.

Note that due to internal delays inside the test multiplexer, it is only valid to compare timing between neighboring LVDS pairs using the same LMX_ADR setting. Similarly, the multiplexer itself contains up to 400ps of skew between rising and falling edges, so it is only valid to compare the timing of a rising edge at TSTP/N to another rising edge, and a falling edge to another falling edge.

Note that Figure 8 shows the suggested input pattern for the LTC2000-16. LTC2000-14 users should apply codes 0x1555 and 0x2AAA, and LTC2000-11 users should apply codes 0x555 and 0x2AA. Also note that for the LTC2000-14 and LTC2000-11 in dual-port mode, the timing skew of LVDS port A (DAP/N) cannot be compared to that of the LVDS clock (DCKIP/N) and LVDS port B (DBP/N), as there is no single test multiplexer address (LMX_ADR) that enables a timing comparison between signals DA0N/P and DCKIP/N (see Table 8). It is recommended to keep LMX_EN = 0 during normal operation.

OPERATION

Table 7. Dynamic Linearization SPI Registers

ADDRESS	BIT	NAME	DESCRIPTION	
0x07	0	LIN_DIS	Dynamic Linearization Disable. Disabled when LIN_DIS = 1.	
	[3:1]	LIN_GN	Dynamic Linearization Gain Select. Changing LIN_GN varies the amount of 3rd order harmonic correction applied to the DAC output. LIN_GN = 000 is normally optimal.	
			LIN_GN	**LINEARIZATION PERCENTAGE**
			110	50%
			111	63%
			000	75% (default)
			001	88%
			010	100%
			011	113%
			100	125%
			101	138%
0x08	[3:0]	LIN_VMX	Dynamic Linearization Max $I_{OUTP/N}$ Voltage Select. For optimal 3rd order harmonic performance, set LIN_VMX to correspond to the maximum voltage expected at $I_{OUTP/N}$. Reset state is LIN_VMX = 1000, which corresponds to 0.51V. LIN_VMX must be greater than LN_VMN.	
	[7:4]	LIN_VMN	Dynamic Linearization Min $I_{OUTP/N}$ Voltage Select. For optimal 3rd order harmonic performance, set LIN_VMN to correspond to the minimum voltage expected at $I_{OUTP/N}$. Reset state is LIN_VMN = 0000, which corresponds to 0.0V. LIN_VMN must be less than LN_VMX.	
			LIN_VMX/N	**MAX/MIN VOLTAGE EXPECTED AT IOUTP/N**
			0000	0.00V (Default for LIN_VMN)
			0001	0.16V
			0010	0.19V
			0011	0.22V
			0100	0.25V
			0101	0.31V
			0110	0.38V
			0111	0.44V
			1000	0.51V (Default for LIN_VMX)
			1001	0.63V
			1010	0.75V
			1011	0.87V
			1100	1.00V

Note: Register 0x07 resets to 0x00 (default). Register 0x08 resets to 0x08 (default).

OPERATION

Table 8. SPI Registers for Measuring LVDS Input Timing Skew

ADDRESS	BIT	NAME	DESCRIPTION
0x18	0	LMX_MSEL	LVDS Test MUX Select. Set LMX_MSEL high or low to select between a pair of neighboring LVDS signals for comparison at TSTP/N.
	[5:1]	LMX_ADR	LVDS Test MUX Address. Use LMX_ADR to select which pair of LVDS signals will be compared at TSTP/N (See Below).
	6	LMX_EN	LVDS Test MUX Enable. Set LMX_EN=1 to compare timing of neighboring signals at TSTP/N. Ensure TDIO_EN = 0 when LMX_EN = 1.

LMX_ADR	LTC2000-16		LTC2000-14		LTC2000-11	
	LMX_MSEL = 0	LMX_MSEL = 1 (INVERTED)	LMX_MSEL = 0	LMX_MSEL = 1 (INVERTED)	LMX_MSEL = 0	LMX_MSEL = 1 (INVERTED)
00000	DA14P/N	DA15N/P	DA12P/N	DA13N/P	DA9P/N	DA10N/P
00001…01001	DA[13:5]P/N	DA[14:6]N/P	DA[11:3]P/N	DA[12:4]N/P	DA[8:0]P/N	DA[9:1]N/P
01010	DA4P/N	DA5N/P	DA2P/N	DA3N/P	—	DA0N/P
01011	DA3P/N	DA4N/P	DA1P/N	DA2N/P	—	—
01100	DA2P/N	DA3N/P	DA0P/N	DA1N/P	—	—
01101	DA1P/N	DA2N/P	—	DA0N/P	—	—
01110	DA0P/N	DA1N/P	—	—	—	—
01111	DCKIP/N	DA0N/P	DCKIP/N	—	DCKIP/N	—
10000	DB15P/N	DCKIN/P	DB13P/N	DCKIN/P	DB10P/N	DCKIN/P
10001	DB14P/N	DB15N/P	DB12P/N	DB13N/P	DB9P/N	DB10N/P
10010…11010	DB[13:5]P/N	DB[14:6]N/P	DB[11:3]P/N	DB[12:4]N/P	DB[8:0]P/N	DB[9:1]N/P
11011	DB4P/N	DB5N/P	DB2P/N	DB3N/P	—	DB0N/P
11100	DB3P/N	DB4N/P	DB1P/N	DB2N/P	—	—
11101	DB2P/N	DB3N/P	DB0P/N	DB1N/P	—	—
11110	DB1P/N	DB2N/P	—	DB0N/P	—	—
11111	DB0P/N	DB1N/P	—	—	—	—

Note: Register 0x18 resets to 0x00 (default).

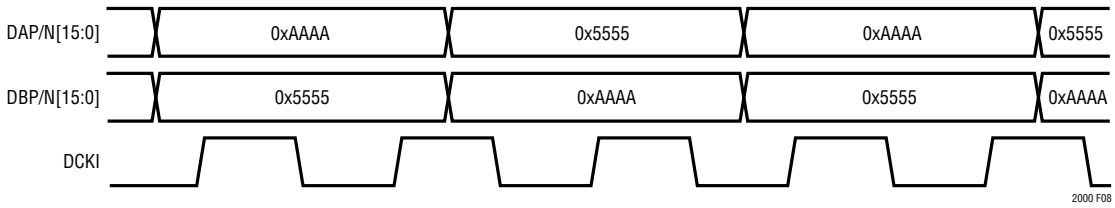


Figure 8. Sample Pattern for Measuring LVDS Input Timing Skew (LTC2000-16)

OPERATION

Measuring Internal Junction Temperature (T_J)

The LTC2000 test multiplexer may also be used to connect internal junction temperature measurement diodes to the TSTP/N pins. Ensure LMX_EN = 0 (register address 0x18) and use SPI register 0x19 to set TDIO_EN = 1 to enable this function (Table 9). There are two methods the user can choose from to measure internal junction temperature (T_J). For TDIO_SEL = 0, an unbiased NPN transistor is diode-connected between the TSTP/N pins with a series resistance of approximately 350Ω. This diode is suitable for use with external temperature sensors which offer series resistance cancellation such as the LTC2991 or LTC2997.

If such a temperature sensor is not available, set TDIO_SEL = 1 to directly observe a temperature dependent voltage between TSTP and TSTN. The typical expected voltage at TSTP is $V_{TSTP} = 2.02V – 5.5mV/°C • (T_J – 25°C)$. The junction temperature can be calculated as $T_J = 25°C + (2.02V – V_{TSTP})/(5.5mV/°C)$. For best accuracy with TDIO_SEL = 1, use TSTN to sense GND at the bottom of the diode and calibrate the voltage at a known temperature. Typical uncalibrated accuracy is ±5°C.

Pattern Generator

A 64 sample deep pattern generator is included in the LTC2000 to simplify system development and debug. The pattern generator allows the user to send a repeating 64 sample pattern to the DAC, completely independent of the presence or absence of valid signals on DCKIP/N, DAP/N, and DBP/N.

To use this feature, do the following:

1. Set DCKO_DIV = 0 in register 0x02, DATA_SP = 0 and DATA_EN = 0 in register 0x04, and PGEN_EN = 0 in register 0x1E.
2. Write 128 bytes of pattern data to address 0x1F (PGEN_D) to fill the pattern generator with 64 samples. Data is written MSB first, and will be applied to the DAC in the order written. Data may be written one byte at a time or in larger multi-byte words. For the LTC2000-14 and LTC2000-11, data should be left justified with zeros filling the remaining two (LTC2000-14) or five (LTC2000-11) bits.
3. Set PGEN_EN = 1 to start the pattern generator.
4. Wait at least 1ms to ensure that the synchronizer has initialized.
5. Set DATA_EN = 1 in register 0x04. The DAC will then begin to output the 64 sample pattern.

The pattern generator will send the repeating 64 sample pattern to the DAC until the user writes PGEN_EN = 0 or DATA_EN = 0.

To read back the pattern, set DATA_EN = 0 and PGEN_EN = 0 and then read 128 bytes from address 0x1F. Note that the starting point of the pattern may have changed while the pattern was running. To modify the pattern, set DATA_EN = 0 and PGEN_EN = 0 and write a new 64 sample pattern to address 0x1F. Ensure PGEN_EN = 0 when reading or writing to address 0x1F, and always read or write an entire 64 sample pattern prior to setting PGEN_EN = 1. See Table 10.

Table 9. Internal Junction Temperature SPI Registers

ADDRESS	BIT	NAME	DESCRIPTION
0x19	0	TDIO_EN	TSTP/N Junction Temperature Diode Enable. Set TDIO_EN = 1 to measure internal junction temperature (T_J) at TSTP/N. Ensure LMX_EN = 0 when TDIO_EN = 1.
	1	TDIO_SEL	Selects which internal temperature diode is observable at TSTP/N. For TDIO_SEL = 1, the typical voltage at TSTP with respect to TSTN is $V_{TSTP} = 2.02V – 5.5mV/°C • (T_J – 25°C)$. Junction temperature can be calculated as $T_J = 25°C + (2.02V – V_{TSTP})/(5.5mV/°C)$. Typical accuracy is ±5°C. For TDIO_SEL = 0, an unbiased diode is connected b/w TSTP/N for use with external temperature sensors.

Note: Register 0x19 resets to 0x00 (default).

SPI REGISTER SUMMARY

Table 10 – Pattern Generator SPI Registers

ADDRESS	BIT	NAME	DESCRIPTION
0x1E	0	PGEN_EN	Pattern Generator Enable. Set PGEN_EN = 1 to use the internal 64 sample pattern generator to provide data to the DAC. Set DATA_SP = 0, DCKO_DIV = 0, and DATA_EN = 1 when PGEN_EN = 1.
0x1F	[7:0]	PGEN_D	Pattern Generator Data. Write 128 bytes of data to this address to fill the pattern generator with 64 samples. Data is written MSB first. Reading this location causes the pattern generator data to be shifted out through SDO. Ensure PGEN_EN = 0 when reading or writing to address 0x1F. Read or write an even number of bytes to address 0x1F prior to setting PGEN_EN = 1 to avoid corrupting the data inside the pattern generator.

Note: Registers 0x1E and 0x1F reset to 0x00 (default).

Table 11. SPI Register List

ADDRESS	BIT	NAME	DESCRIPTION	RESET VALUE	R/W
0x00	[7:0]	Reserved	Reserved		
0x01	0	SW_RST	Software Reset. SW_RST = 1 resets all registers.	0	R/W
	1	DAC_PD	DAC Power Down. DAC_PD = 1 to power down DAC core.	0	R/W
	2	FULL_PD	Full Power Down. FULL_PD = 1 to power down LTC2000.	0	R/W
	3	Reserved	Reserved		
	[5:4]	DAC_RES	DAC Resolution Indicator. DAC_RES = 00 for LTC2000-16. DAC_RES = 01 for LTC2000-14. DAC_RES = 11 for LTC2000-11. Note that for $\overline{PD}$ = GND or FULL_PD = 1, DAC_RES = 00. DAC_RES is read only.	00-16b 01-14b 11-11b	R
	[7:6]	Reserved	Reserved		
0x02	0	CK_PD	CKP/N Clock Receiver Power Down. CK_PD = 1 disables	0	R/W
	1	CK_OK	CKP/N Clock Present Indicator. CK_OK = 1 clock present	0	R
	[3:2]	Reserved	Reserved		
	4	DCKO_DIS	DCKOP/N Output Disable. DCKO_DIS = 1 disables	0	R/W
	5	DCKO_DIV	DCKOP/N Divide Select. (0 = f_{DAC}/4, 1 = f_{DAC}/2).	0	R/W
	6	DCKO_ISEL	DCKOP/N Output Current Select. (0=3.5mA, 1 = 7mA)	0	R/W
	7	DCKO_TRM	DCKOP/N Internal Termination On. DCKO_TRM = 1 enables internal 100Ω termination	0	R/W
0x03	0	DCKI_EN	DCKIP/N Clock Receiver Enable. DCKI_EN = 1 enables.	0	R/W
	1	DCKI_OK	DCKIP/N Clock Present Indicator. DCKI_OK = 1 indicates clock present	0	R
	2	DCKI_Q	DCKIP/N Quadrature Phase Select. (0 = In Phase, 1 = Quadrature)	0	R/W
	3	Reserved	Reserved		
	[6:4]	DCKI_TADJ	DCKIP/N Delay Adjust. (See Table 4)	000	R/W
	7	Reserved	Reserved		
0x04	0	DA_EN	Port A LVDS Receiver Enable. DA_EN = 1 to enable	0	R/W
	1	DB_EN	Port B LVDS Receiver Enable. DB_EN = 1 to enable	0	R/W
	2	DATA_SP	Port Mode Select. (0 = Dual port, 1 = Single port)	0	R/W
	3	DATA_EN	DAC Data Enable. DATA_EN = 0 forces DAC output to mid-scale.	0	R/W
	[7:4]	Reserved	Reserved		
0x05	[1:0]	SYNC_PS	Clock Synchronizer Phase Select.	00	R/W
	2	SYNC_MSYN	Clock Synchronizer Manual Mode Select. SYNC_MSYN = 0: SYNC_PS is set automatically. SYNC_MSYN = 1: SYNC_PS is set by the user.	0	R/W
	[7:3]	Reserved	Reserved		
0x06	[7:0]	SYNC_PH	Clock Phase Comparator Outputs. (See Table 6)	0x00	R

SPI REGISTER SUMMARY

Table 11. SPI Register List

ADDRESS	BIT	NAME	DESCRIPTION	RESET VALUE	R/W
0x07	0	LIN_DIS	Dynamic Linearization Disable. LIN_DIS = 1 disables.	0	R/W
	[3:1]	LIN_GN	Dynamic Linearization Gain Select. (See Table 7)	000	R/W
	[7:4]	Reserved	Reserved		
0x08	[3:0]	LIN_VMX	Dynamic Linearization Max $I_{OUTP/N}$ Voltage Select. (See Table 7)	1000	R/W
	[7:4]	LIN_VMN	Dynamic Linearization Min $I_{OUTP/N}$ Voltage Select. (See Table 7)	0000	R/W
0x09	[5:0]	GAIN_ADJ	DAC Gain Adjustment. (See Table 2)	0x00	R/W
	[7:6]	Reserved	Reserved		
0x0A Thru 0x17	[7:0]	Reserved	Reserved		
0x18	0	LMX_MSEL	LVDS Test MUX Select. (See Table 8)	0	R/W
	[5:1]	LMX_ADR	LVDS Test MUX Address Select. (See Table 8)	0x00	R/W
	6	LMX_EN	LVDS Test MUX Enable. LMX_EN = 1 enables LVDS text MUX. Ensure TDIO_EN = 0 when LMX_EN = 1.		
	7	Reserved	Reserved		
0x19	0	TDIO_EN	TSTP/N Junction Temperature Diode Enable. TDIO_EN = 1 enables temperature (T_J) measurement. Ensure LMX_EN = 0 when TDIO_EN = 1.	0	R/W
	1	TDIO_SEL	Junction Temperature Select. TDIO_SEL = 0 uses a diode-connected unbiased NPN transistor. TDIO_SEL = 1 outputs a voltage to calculate internal die temperature using: $T_J = 25°C + (2.02V – V_{TSTP})/(5.5mV/°C)$. (See Table 9)	0	R/W
	[7:2]	Reserved	Reserved		
0x1A Thru 0x1D	[7:0]	Reserved	Reserved		
0x1E	0	PGEN_EN	Pattern Generator Enable. PGEN_EN = 1 enables.	0	R/W
	[7:1]	Reserved	Reserved		
0x1F	[7:0]	PGEN_D	Pattern Generator Data.	0x00	R/W
0x20 Thru 0x7F	[7:0]	Reserved	Reserved		

APPLICATIONS INFORMATION

Sample Start-Up Sequence

The following is an example of a common start-up sequence.

1. Apply valid supply voltages to AV_{DD33}, DV_{DD33}, AV_{DD18}, D_{VDD18} and SV_{DD}.
2. Write 0x01 to address 0x01 to perform a software reset.
3. Apply a clock to CKP/N at the desired f_{DAC} frequency. The LTC2000 will generate a clock at DCKOP/N at $f_{DAC}/4$.
4. Apply a clock to DCKIP/N at $f_{DAC}/4$ for dual-port mode or $f_{DAC}/2$ for single-port mode.
5. Apply zeroes to ports A and B (DAP/N, DBP/N) for dual-port mode, or only to port B for single-port mode.
6. Write to address 0x03 to enable the DCKIP/N LVDS receiver. Set address 0x03 to 0x01 if the LVDS clock (DCKI) and data (DA, DB) are in phase with each other. Set address 0x03 to 0x05 if they are in quadrature.

APPLICATIONS INFORMATION

7. Write 0x03 to address 0x04 for dual-port mode, or write 0x06 to address 0x04 for single-port mode to enable the DAP/N and DBP/N LVDS receivers.
8. Wait at least 1ms for the synchronizer to finish initializing.
9. Write 0x0B to address 0x04 for dual-port mode, or write 0x0E to address 0x04 for single-port mode to set DATA_EN = 1.
10. Apply desired data pattern to ports A and B (DAP/N, DBP/N) for dual-port mode, or only to port B for single-port mode. Port A samples will precede port B samples at the DAC output when using dual-port mode.

Output Configurations

The LTC2000's complementary current outputs ($I_{OUTP/N}$) source current into an external load referenced to GND. Output load configuration, component selection, and layout are critical to the performance of the LTC2000. For best AC performance, the output stages should be configured for differential (or balanced) operation.

A differential resistor loaded output is a very simple output stage. Well matched resistors are connected between GND and $I_{OUTP/N}$, with the resistance values setting both the output swing and non-zero output common-mode voltage (Figure 9). While it is economical, this type of output stage

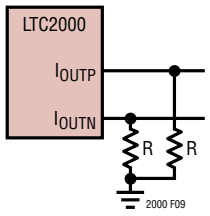


Figure 9. Differential Resistor Output Load

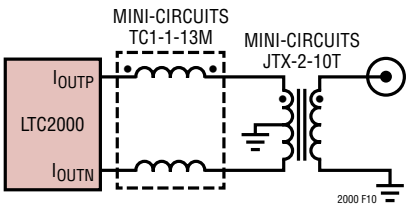


Figure 10. Transformer-Based Output Configuration for Differential to Single-Ended Conversion

can drive only differential loads with impedance levels and amplitudes appropriate for the DAC outputs.

Differential transformer-coupled output configurations usually give the best AC performance and provide excellent rejection of common mode distortion and noise over a broad frequency range. Figure 10 shows a transformer output configuration that uses a Mini-Circuits TC1-1-13M and a JTX-2-10T RF transformer for differential to single-ended conversion.

For any output configuration, any imbalances in the output impedance between the I_{OUTP} and I_{OUTN} pins results in asymmetrical signal swings that lead to distortion (mostly even order). Careful consideration is needed to select the best output configuration for a given application.

Generating the DAC Sample Clock

For best AC performance, it is important that the DAC sample clock waveforms be clean, with low phase noise and good jitter performance, as the phase noise and spurious content of the clock source will appear directly in the DAC output spectrum.

A differential clock should be AC coupled onto the CKP/N pins, since the DC bias point of CKP/N is set internally to 1V through a 5kΩ impedance. Figure 11 shows the DAC sample clock receiver input and common-mode voltage control. While the differential input voltage range of the clock receiver spans from ±300mV to ±1.8V, a signal with the highest possible slew rate and amplitude and a balanced duty cycle is recommended. Traces that carry

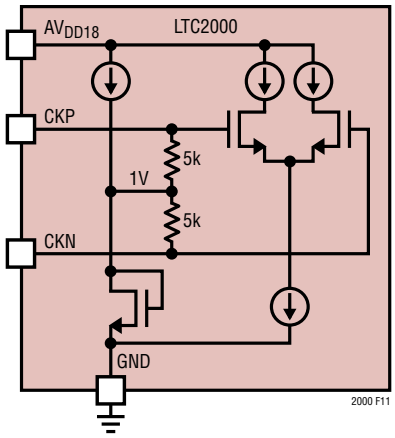


Figure 11. DAC Sample Clock Receiver

APPLICATIONS INFORMATION

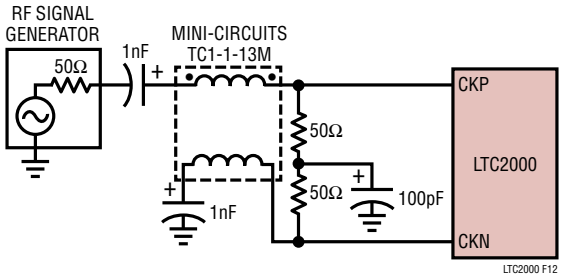


Figure 12. DAC Sample Clock Generation with an RF Signal Generator and a 1:1 Balun

the differential clock signal need to have accurately controlled impedance and accurate termination as close to the CKP/N pins of the LTC2000 as possible.

There are several ways to generate the DAC sample clock. For lab evaluation and testing, a high quality RF signal generator can provide a clean high frequency sine wave that is converted to the DAC sample clock with a 1:1 RF transformer or balun (see Figure 12).

A more integrated clock source is one based on a low phase noise, low jitter PLL. Figure 13 shows how the DAC sample clock can be generated from the LTC6946, a high performance PLL with an internal VCO that can provide output frequencies from 0.37GHz to 5.7GHz. See the LTC6946 data sheet for details.

Synchronizing Multiple LTC2000s in Dual-Port Mode

In some applications, it is necessary to synchronize multiple LTC2000s to each other such that related samples arrive at all DAC outputs simultaneously. Figures 14 and 15a show a block diagram and sample waveforms for such a system in which two DACs (X and Y) are to be synchronized in dual-port mode.

Note that in this example a small timing skew between the two data signals at the DCKIP/N pins of DACs X and Y has caused the DCKIP/N rising edges to arrive on opposite sides of a DAC sample clock (CKP/N) rising edge, and thus within different CKP/N clock cycles. As a result the default behavior is for the output of DAC Y to update with sample N one cycle earlier than the output of DAC X. It is possible to correct this misalignment and synchronize DACs X and Y by adjusting the clock synchronizer settings to subtract one cycle of latency from DAC X, as shown in the adjusted waveform at the bottom of Figure 15a. See the Clock Synchronizer section and Figure 7 for more details on the operation of the clock synchronizer.

In order to synchronize multiple DACs as shown in Figures 14 and 15a, distribute the DAC sample clock carefully with matched delays so that it arrives at the CKP/N pins of all DACs simultaneously. Any remaining timing mismatch between sample clocks will appear directly as mismatch in the DAC output timing. Ensure that the timing mismatch between LVDS data clock signals at the DCKIP/N pins of all DACs is less than 0.4 cycles of the DAC sample clock, minus any timing mismatch between the DAC sample clocks. Be sure to maintain sufficient matching between the timing of the LVDS data inputs (DAP/N, DBP/N) and DCKIP/N for each DAC to meet the setup and hold time specifications (t_{11}, t_{12}) in the Timing Characteristics section.

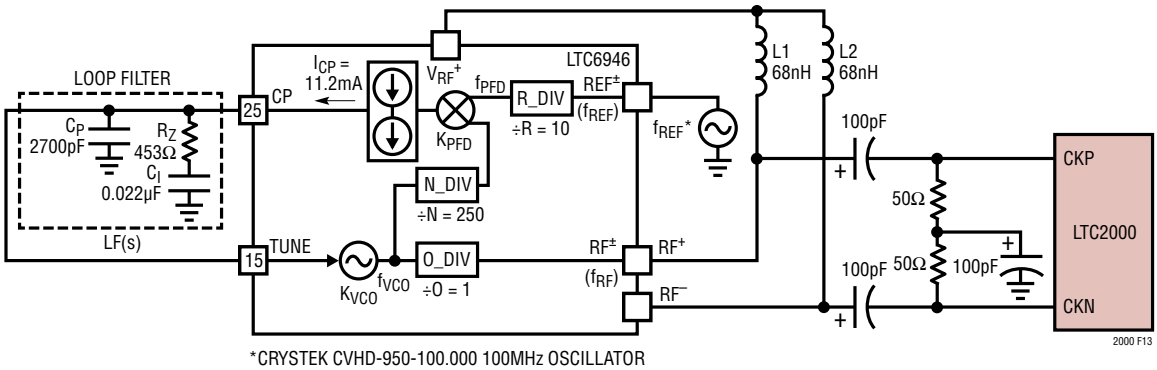


Figure 13. DAC Sample Clock Generation with the LTC6946

APPLICATIONS INFORMATION

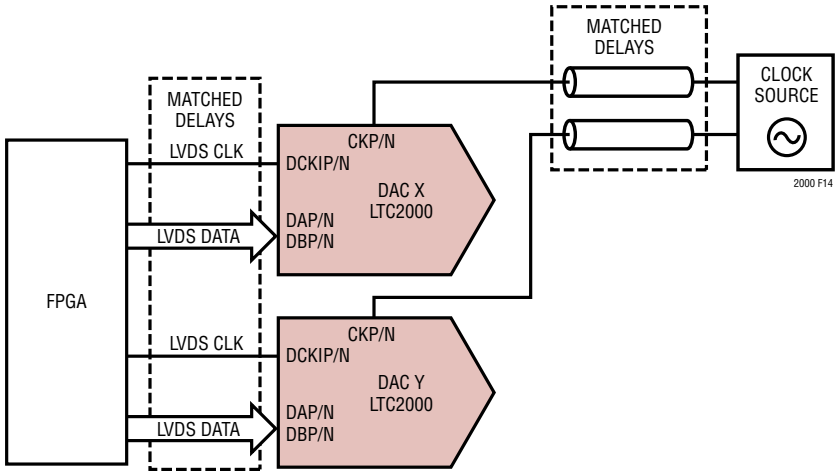


Figure 14. System with Multiple LTC2000 DACs Synchronized

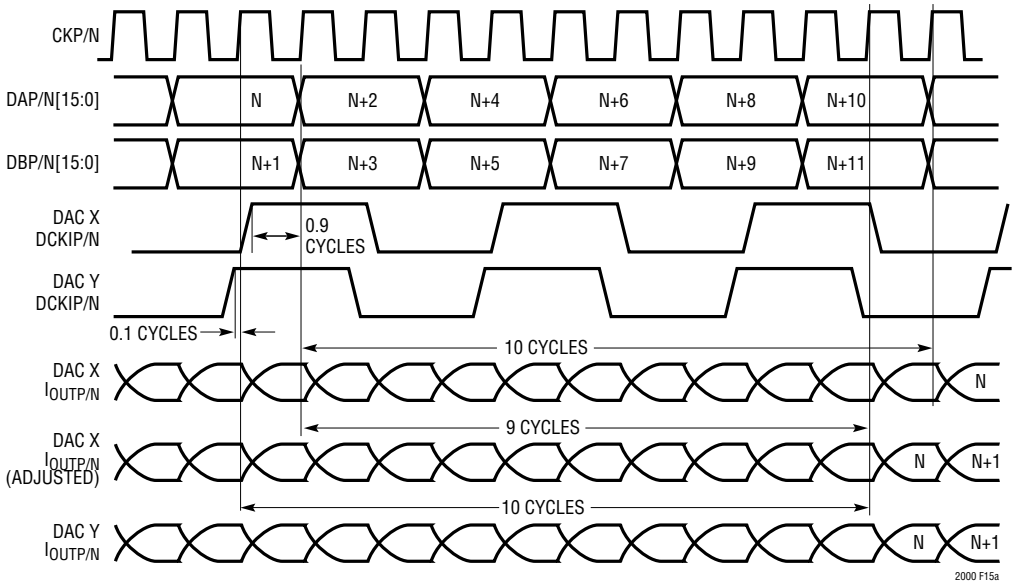


Figure 15a. Sample Waveforms — Synchronizing Multiple LTC2000s in Dual Port Mode

For example, let us consider a system using multiple DACs at 2.5Gsps in which the sample clock is designed to arrive at the CKP/N pins of all DACs within 30ps of one another. The sample clock period is 400ps, so the maximum allowable timing mismatch between the data clock signals at the DCKIP/N pins of all DACs will be (0.4 • 400ps) – 30ps = 130ps. For a system using multiple DACs at 1.25Gsps, the allowable mismatch between DCKIP/N pins will be (0.4 • 800ps) – 30ps = 290ps. In both cases, once the DACs are synchronized the mismatch in the DAC output timing will be limited to 30ps.

Once all the DAC sample clocks and LVDS data clocks are aligned, determine whether any DACs are being updated one cycle late (such as DAC X in Figure 15a) by determining whether DCKIP/N is arriving at the DACs within the same CKP/N clock cycle. To do this in dual-port mode, first use the phase comparator outputs SYNC_PH and Table 12 to determine the delay from the DCKIP/N rising edge to the next CKP/N rising edge for each DAC (measured in sample clock cycles).

Recall that the DCKIP/N timing mismatch must be kept below 0.4 cycles of the sample clock. If DCKIP/N arrives at

APPLICATIONS INFORMATION

both DACs within the same sample clock cycle, the difference in DCKIP/N to CKP/N delays indicated by SYNC_PH will equal the actual DCKIP/N timing mismatch, and thus will be less than 0.4 cycles. If DCKIP/N arrives at the DACs within different cycles, as in Figure 15a, the difference in the delays indicated by SYNC_PH will equal 1 cycle minus the actual DCKIP/N timing mismatch, and thus will be greater than 0.4 cycles. Thus if the difference between the delays indicated by SYNC_PH is greater than 0.4 cycles, the DCKIP/N rising edges are arriving in different sample clock cycles.

For the example in Figure 15a, we might read 0x25 for SYNC_PH on DAC X and 0x52 on DAC Y. Table 12 tells us that the DCKIP/N to CKP/N delay is greater than 0.8 cycles for DAC X and less than 0.2 cycles for DAC Y, and thus the difference between them is at least 0.6 cycles. We conclude that the DCKIP/N rising edge of DAC X must fall within a later sample clock cycle than that of DAC Y, and thus that DAC X is being updated one cycle later than DAC Y.

To correct any such misalignment and synchronize the DACs, consult Table 12 and adjust the SYNC_PS settings for those DACs which are being updated one cycle late (DAC X in the above example) by setting the synchronizer to manual mode (SYNC_MSYN = 1) and overwriting the SYNC_PS value.

In this example, reading register 0x06 of DAC X shows SYNC_PH = 0x25 and that the SYNC_PS setting needs to change from the default (10) to the desired adjusted value (00), subtracting one cycle from the latency of DAC X (refer to Table 12). Write 0x04 to register 0x05 of DAC X to set SYNC_MSYN = 1 and SYNC_PS = 00. The outputs of DAC X should now align with DAC Y as shown in Figure 15a. See Table 6 for details regarding the synchronizer registers 0x05 and 0x06. Sample verilog code implementing the synchronization of multiple LTC2000s using Tables 12 and 13 can be found at:

http://www.linear.com/docs/44845

Table 12. Adjusting Latency in Dual-Port Mode

PHASE COMPARATOR OUTPUTS SYNC_PH (REG 0x06)	DELAY FROM DCKIP/N RISING EDGE TO NEXT CKP/N RISING EDGE (CKP/N CYCLES)	SYNC_PS SETTING	
		(DEFAULT)	(ADJUSTED TO REDUCE LATENCY BY 1 CYCLE)*
0x03	0 to 0.2	10	N/A
0x04	0.2 to 0.4	10	N/A
0x05	0.4 to 0.6	10	N/A
0x15	0.6 to 0.8	10	00
0x25	0.8 to 1.0	10	00
0x35	0 to 0.2	00	N/A
0x45	0.2 to 0.4	00	N/A
0x55	0.4 to 0.6	00	N/A
0x54	0.6 to 0.8	00	01
0x53	0.8 to 1.0	00	01
0x52	0 to 0.2	01	N/A
0x51	0.2 to 0.4	01	N/A
0x50	0.4 to 0.6	01	N/A
0x40	0.6 to 0.8	01	11
0x30	0.8 to 1.0	01	11
0x20	0 to 0.2	11	N/A
0x10	0.2 to 0.4	11	N/A
0x00	0.4 to 0.6	11	N/A
0x01	0.6 to 0.8	11	10
0x02	0.8 to 1.0	11	10

*N/A indicate SYNC_PH values that should not occur if the timing mismatch requirements described above are met. If such a case occurs, keep SYNC_PS as the default value.

APPLICATIONS INFORMATION

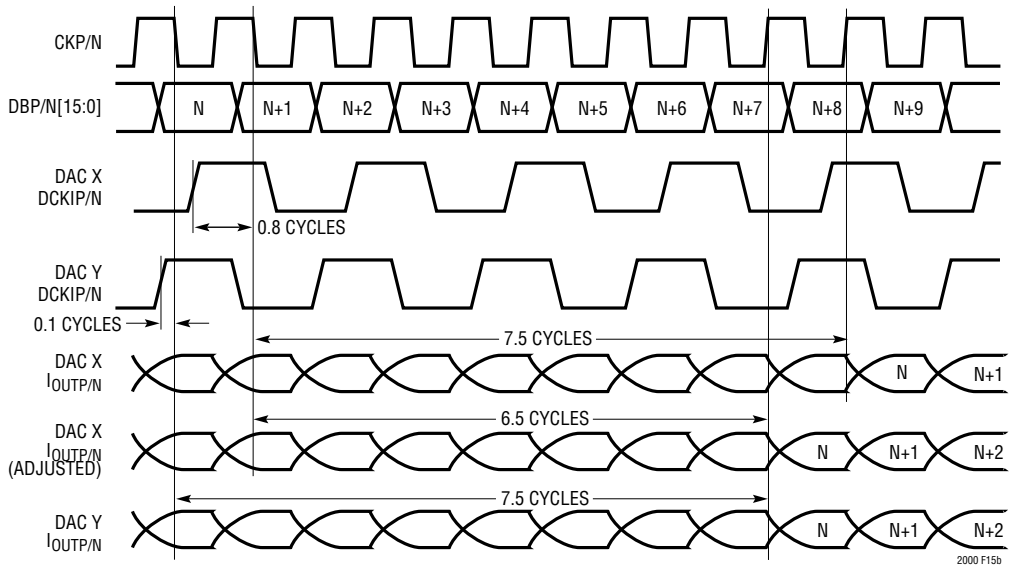


Figure 15b. Sample Waveforms — Synchronizing Multiple LTC2000s in Single Port Mode

Synchronizing Multiple LTC2000s in Single-Port Mode

Figure 15b shows sample waveforms for synchronizing two LTC2000s in single port mode. Synchronizing multiple LTC2000s in single port mode is essentially the same procedure as when operating in dual port mode—DAC sample clocks must all be aligned to arrive at the CKP/N pins of all DACs simultaneously and timing mismatch between LVDS data clock signals at the DCKIP/N pins of all DACs must be less than 0.4 cycles of the DAC sample clock, minus any timing mismatch between the DAC sample clocks.

To determine whether any DACs are being updated one cycle late in single port mode, first use the phase comparator outputs SYNC_PH and Table 13 to determine the delay from the DCKIP/N rising edge to the next CKP/N falling edge (as opposed to rising edge in dual port mode) for each DAC. If the difference between the delays indicated by SYNC_PH is greater than 0.4 cycles, the DCKIP/N rising edges are arriving in different sample clock cycles.

For the example in Figure 15b, we might read 0x15 for SYNC_PH on DAC X and 0x20 on DAC Y. Table 13 shows that the DCKIP/N to CKP/N delay is greater than 0.8 cycles for DAC X and less than 0.1 cycles for DAC Y, and thus the difference between them is at least 0.7 cycles. This indicates that DAC X is being updated one cycle later than DAC Y. Consult Table 13 and use the same procedure described above in the dual-port mode case to correct the SYNC_PS settings for those DACs that are updating one cycle late. In this single port example, writing 0x06 to register 0x05 of DAC X would set SYNC_MSYN = 1 and SYNC_PS = 10, reducing the latency of DAC X by one cycle and aligning its output with DAC Y, as shown in Figure 15b.

Note that variations in system temperature or supply voltage may cause the phase of the data clock (DCKIP/N) and sample clock (CKP/N) to vary with time. When using the LTC2000 with SYNC_MSYN = 1, it is recommended that users monitor SYNC_PH and adjust SYNC_PS using Tables 12 or 13 as needed to maintain proper alignment.

The synchronization procedures described above also work for systems with more than two DACs. Simply determine the minimum DCKIP/N to CKP/N delay of all DACs by reading SYNC_PH, and then adjust the SYNC_PS settings to subtract one cycle of latency to those DACs whose DCKIP/N to CKP/N delays are at least 0.4 cycles more than the minimum. Sample verilog code implementing the synchronization of multiple LTC2000s using Tables 12 and 13 can be found at:

http://www.linear.com/docs/44845

APPLICATIONS INFORMATION

Table 13. Adjusting Latency in Single-Port Mode

PHASE COMPARATOR OUTPUTS SYNC_PH (REG 0x06)	DELAY FROM DCKIP/N RISING EDGE TO NEXT CKP/N FALLING EDGE (CKP/N CYCLES)	SYNC_PS SETTING	
		(DEFAULT)	(ADJUSTED TO REDUCE LATENCY BY 1 CYCLE)*
0x03	0.5 to 0.6	00	N/A
0x04	0.6 to 0.7	00	10
0x05	0.7 to 0.8	00	10
0x15	0.8 to 0.9	00	10
0x25	0.9 to 1.0	00	10
0x35	0 to 0.1	10	N/A
0x45	0.1 to 0.2	10	N/A
0x55	0.2 to 0.3	10	N/A
0x54	0.3 to 0.4	10	N/A
0x53	0.4 to 0.5	10	N/A
0x52	0.5 to 0.6	10	N/A
0x51	0.6 to 0.7	10	00
0x50	0.7 to 0.8	10	00
0x40	0.8 to 0.9	10	00
0x30	0.9 to 1.0	10	00
0x20	0 to 0.1	00	N/A
0x10	0.1 to 0.2	00	N/A
0x00	0.2 to 0.3	00	N/A
0x01	0.3 to 0.4	00	N/A
0x02	0.4 to 0.5	00	N/A

*N/A indicate SYNC_PH values that should not occur if the timing mismatch requirements described above are met. If such a case occurs, keep SYNC_PS as the default value.

PCB Layout Considerations

The close proximity of high frequency digital data lines and high dynamic range, wideband analog signals make clean printed circuit board design and layout an absolute necessity. Figures 16 and 17 show a schematic and PCB layers for an evaluation circuit for the LTC2000. A single, solid ground plane should be used, while separate supply planes for AV_{DD18}, DV_{DD18}, AV_{DD33}, and DV_{DD33} should be kept all the way to the individual supply or LDO. All LVDS input (DCKIP/N, DAP/N, DBP/N) board traces must be carefully matched to ensure proper phase alignment. These LVDS inputs should be kept far away from both the $I_{OUTP/N}$ and CKP/N traces to avoid any data dependent coupling into the analog output and DAC sample clock.

The CKP/N traces should be routed either over the analog ground plane or over their own section on the ground plane. These traces also need to have accurately controlled impedance and should be well terminated near the LTC2000. The $I_{OUTP/N}$ traces should also be carefully matched to each other, routed over the ground plane, away from the LVDS inputs and CKP/N signals.

Bypass capacitors are required on AV_{DD18}, DV_{DD18}, AV_{DD33}, and DV_{DD33}, and should all be connected to the analog ground plane. 2.2µF ceramic capacitors with low ESR are recommended to be placed close to the LTC2000 with minimum trace lengths. A sample PCB layout and schematic can be found below.

APPLICATIONS INFORMATION

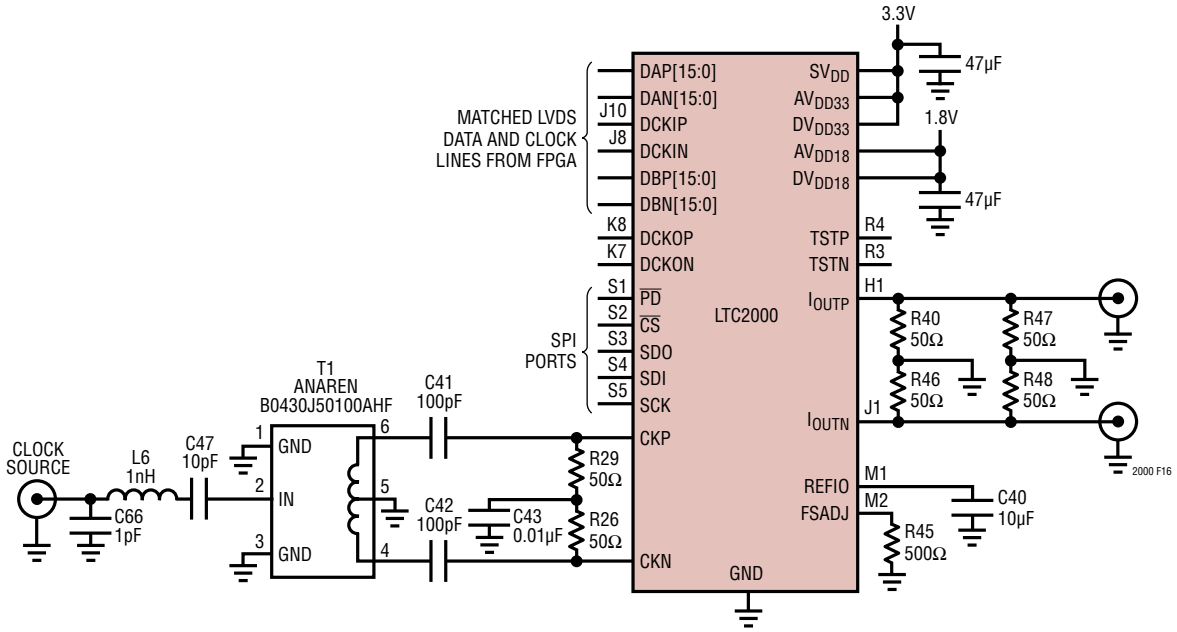
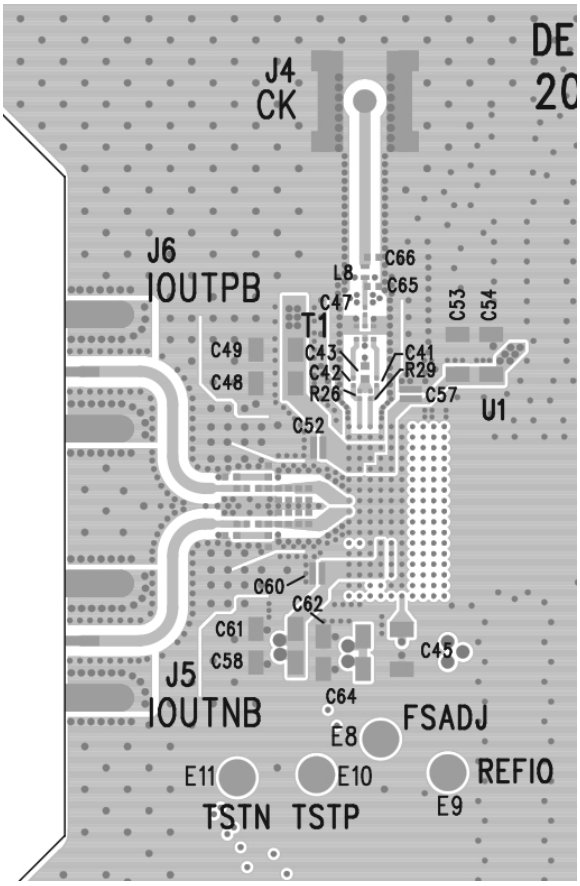
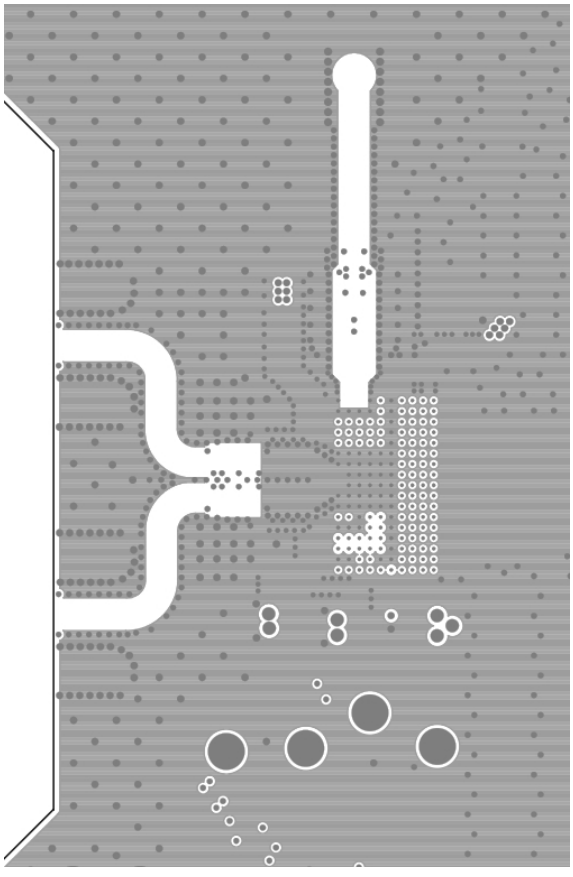


Figure 16



Layer 1



Layer 2

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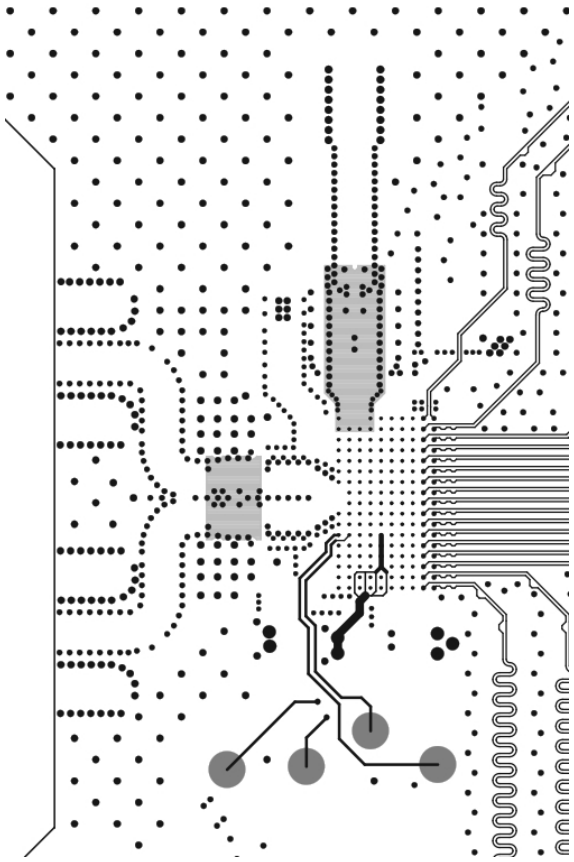

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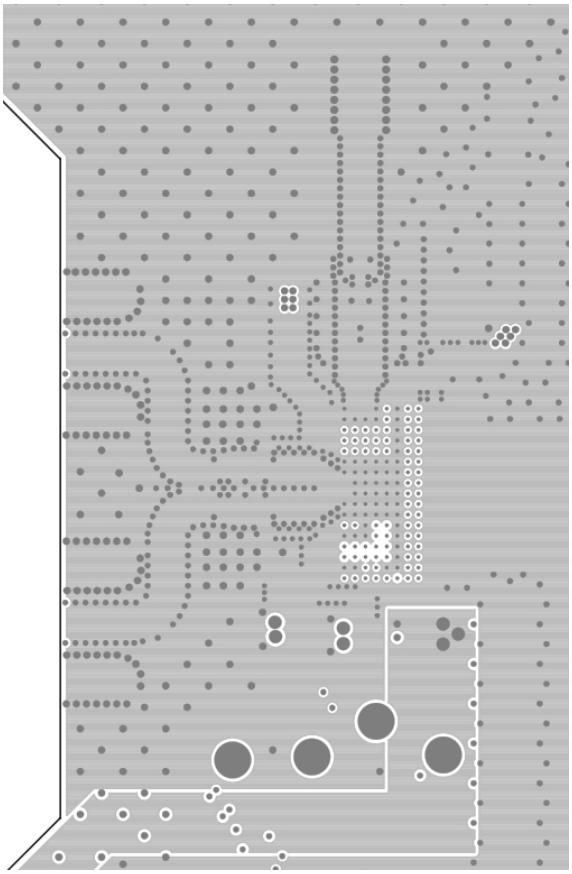

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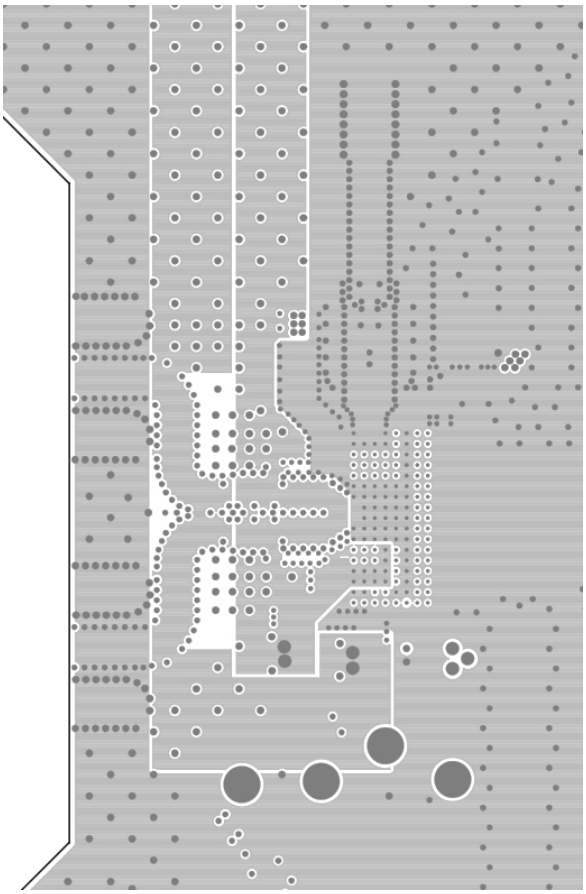

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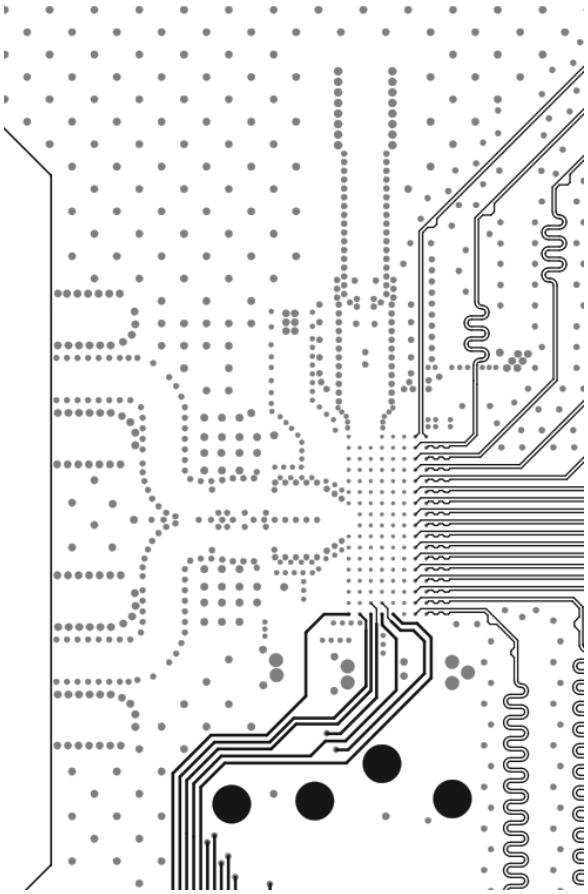

Layer 6

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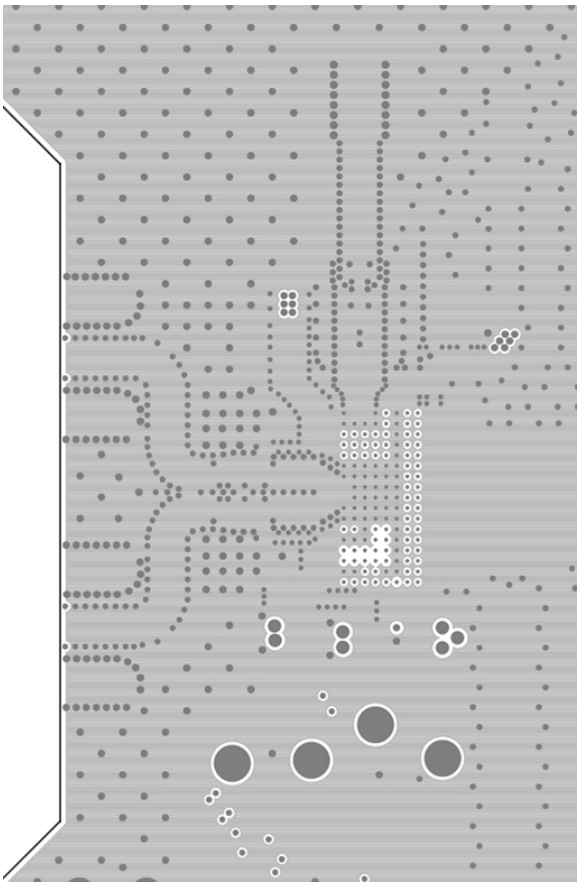

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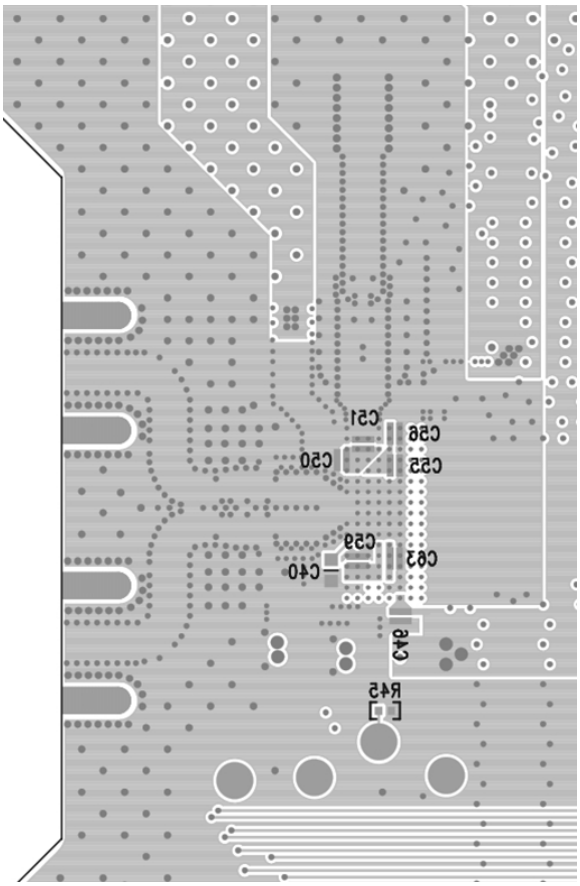


Layer 8

PIN LOCATIONS (LTC2000-16)

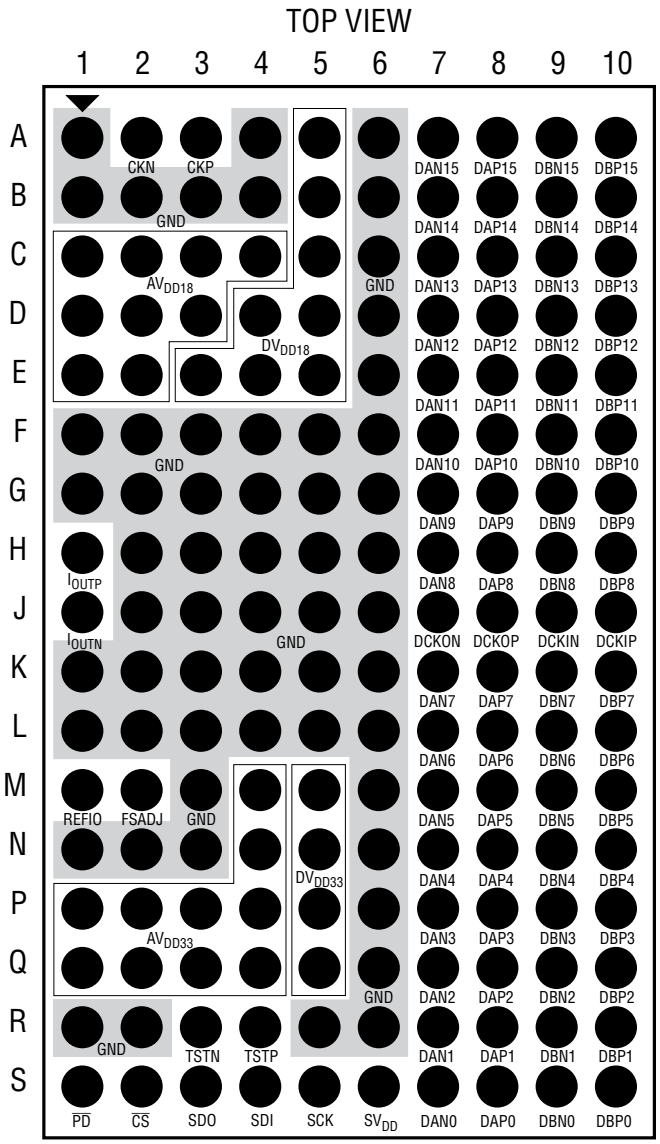
LTC2000-16 BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	GND	B1	GND	C1	AV_{DD18}	D1	AV_{DD18}	E1	AV_{DD18}	F1	GND
A2	CKN	B2	GND	C2	AV_{DD18}	D2	AV_{DD18}	E2	AV_{DD18}	F2	GND
A3	CKP	B3	GND	C3	AV_{DD18}	D3	AV_{DD18}	E3	DV_{DD18}	F3	GND
A4	GND	B4	GND	C4	AV_{DD18}	D4	DV_{DD18}	E4	DV_{DD18}	F4	GND
A5	DV_{DD18}	B5	DV_{DD18}	C5	DV_{DD18}	D5	DV_{DD18}	E5	DV_{DD18}	F5	GND
A6	GND	B6	GND	C6	GND	D6	GND	E6	GND	F6	GND
A7	DAN15	B7	DAN14	C7	DAN13	D7	DAN12	E7	DAN11	F7	DAN10
A8	DAP15	B8	DAP14	C8	DAP13	D8	DAP12	E8	DAP11	F8	DAP10
A9	DBN15	B9	DBN14	C9	DBN13	D9	DBN12	E9	DBN11	F9	DBN10
A10	DBP15	B10	DBP14	C10	DBP13	D10	DBP12	E10	DBP11	F10	DBP10

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	GND	H1	I_{OUTP}	J1	I_{OUTN}	K1	GND	L1	GND	M1	REFIO
G2	GND	H2	GND	J2	GND	K2	GND	L2	GND	M2	FSADJ
G3	GND	H3	GND	J3	GND	K3	GND	L3	GND	M3	GND
G4	GND	H4	GND	J4	GND	K4	GND	L4	GND	M4	AV_{DD33}
G5	GND	H5	GND	J5	GND	K5	GND	L5	GND	M5	DV_{DD33}
G6	GND	H6	GND	J6	GND	K6	GND	L6	GND	M6	GND
G7	DAN9	H7	DAN8	J7	DCKON	K7	DAN7	L7	DAN6	M7	DAN5
G8	DAP9	H8	DAP8	J8	DCKOP	K8	DAP7	L8	DAP6	M8	DAP5
G9	DBN9	H9	DBN8	J9	DCKIN	K9	DBN7	L9	DBN6	M9	DBN5
G10	DBP9	H10	DBP8	J10	DCKIP	K10	DBP7	L10	DBP6	M10	DBP5

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
N1	GND	P1	AV_{DD33}	Q1	AV_{DD33}	R1	GND	S1	$\overline{PD}$
N2	GND	P2	AV_{DD33}	Q2	AV_{DD33}	R2	GND	S2	$\overline{CS}$
N3	GND	P3	AV_{DD33}	Q3	AV_{DD33}	R3	TSTN	S3	SDO
N4	AV_{DD33}	P4	AV_{DD33}	Q4	AV_{DD33}	R4	TSTP	S4	SDI
N5	DV_{DD33}	P5	DV_{DD33}	Q5	DV_{DD33}	R5	GND	S5	SCK
N6	GND	P6	GND	Q6	GND	R6	GND	S6	SV_{DD}
N7	DAN4	P7	DAN3	Q7	DAN2	R7	DAN1	S7	DAN0
N8	DAP4	P8	DAP3	Q8	DAP2	R8	DAP1	S8	DAP0
N9	DBN4	P9	DBN3	Q9	DBN2	R9	DBN1	S9	DBN0
N10	DBP4	P10	DBP3	Q10	DBP2	R10	DBP1	S10	DBP0

PIN LOCATIONS (LTC2000-16)



PIN LOCATIONS (LTC2000-14)

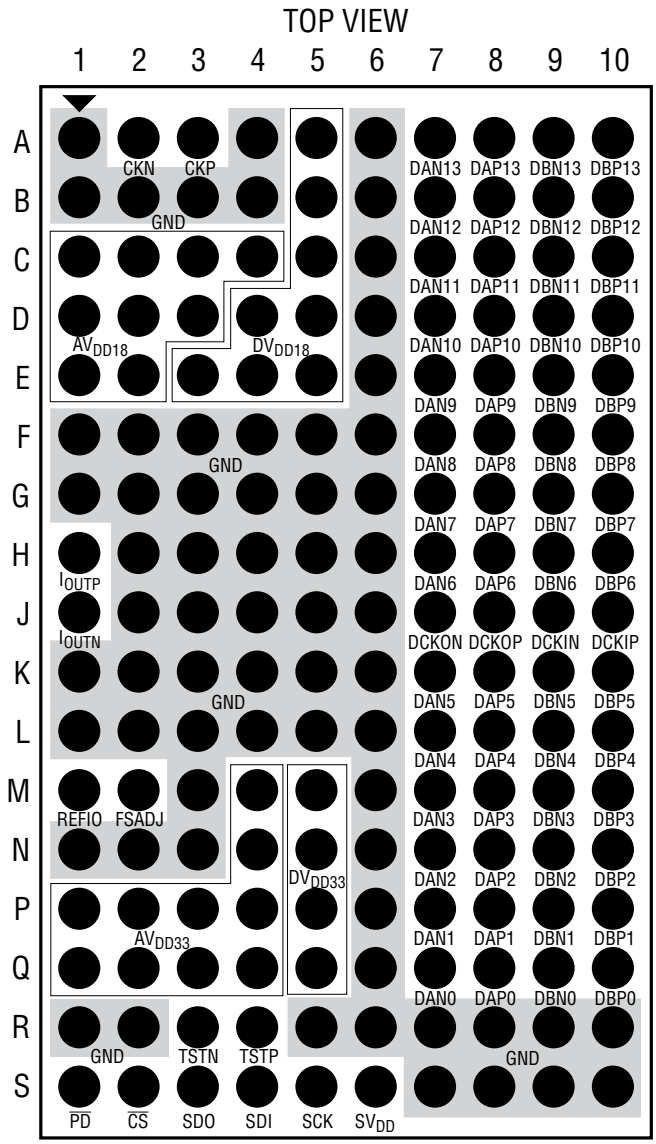
LTC2000-14 BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	GND	B1	GND	C1	AV_{DD18}	D1	AV_{DD18}	E1	AV_{DD18}	F1	GND
A2	CKN	B2	GND	C2	AV_{DD18}	D2	AV_{DD18}	E2	AV_{DD18}	F2	GND
A3	CKP	B3	GND	C3	AV_{DD18}	D3	AV_{DD18}	E3	DV_{DD18}	F3	GND
A4	GND	B4	GND	C4	AV_{DD18}	D4	DV_{DD18}	E4	DV_{DD18}	F4	GND
A5	DV_{DD18}	B5	DV_{DD18}	C5	DV_{DD18}	D5	DV_{DD18}	E5	DV_{DD18}	F5	GND
A6	GND	B6	GND	C6	GND	D6	GND	E6	GND	F6	GND
A7	DAN13	B7	DAN12	C7	DAN11	D7	DAN10	E7	DAN9	F7	DAN8
A8	DAP13	B8	DAP12	C8	DAP11	D8	DAP10	E8	DAP9	F8	DAP8
A9	DBN13	B9	DBN12	C9	DBN11	D9	DBN10	E9	DBN9	F9	DBN8
A10	DBP13	B10	DBP12	C10	DBP11	D10	DBP10	E10	DBP9	F10	DBP8

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	GND	H1	I_{OUTP}	J1	I_{OUTN}	K1	GND	L1	GND	M1	REFIO
G2	GND	H2	GND	J2	GND	K2	GND	L2	GND	M2	FSADJ
G3	GND	H3	GND	J3	GND	K3	GND	L3	GND	M3	GND
G4	GND	H4	GND	J4	GND	K4	GND	L4	GND	M4	AV_{DD33}
G5	GND	H5	GND	J5	GND	K5	GND	L5	GND	M5	DV_{DD33}
G6	GND	H6	GND	J6	GND	K6	GND	L6	GND	M6	GND
G7	DAN7	H7	DAN6	J7	DCKON	K7	DAN5	L7	DAN4	M7	DAN3
G8	DAP7	H8	DAP6	J8	DCKOP	K8	DAP5	L8	DAP4	M8	DAP3
G9	DBN7	H9	DBN6	J9	DCKIN	K9	DBN5	L9	DBN4	M9	DBN3
G10	DBP7	H10	DBP6	J10	DCKIP	K10	DBP5	L10	DBP4	M10	DBP3

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
N1	GND	P1	AV_{DD33}	Q1	AV_{DD33}	R1	GND	S1	$\overline{PD}$
N2	GND	P2	AV_{DD33}	Q2	AV_{DD33}	R2	GND	S2	$\overline{CS}$
N3	GND	P3	AV_{DD33}	Q3	AV_{DD33}	R3	TSTN	S3	SDO
N4	AV_{DD33}	P4	AV_{DD33}	Q4	AV_{DD33}	R4	TSTP	S4	SDI
N5	DV_{DD33}	P5	DV_{DD33}	Q5	DV_{DD33}	R5	GND	S5	SCK
N6	GND	P6	GND	Q6	GND	R6	GND	S6	SV_{DD}
N7	DAN2	P7	DAN1	Q7	DAN0	R7	GND	S7	GND
N8	DAP2	P8	DAP1	Q8	DAP0	R8	GND	S8	GND
N9	DBN2	P9	DBN1	Q9	DBN0	R9	GND	S9	GND
N10	DBP2	P10	DBP1	Q10	DBP0	R10	GND	S10	GND

PIN LOCATIONS (LTC2000-14)



PIN LOCATIONS (LTC2000-11)

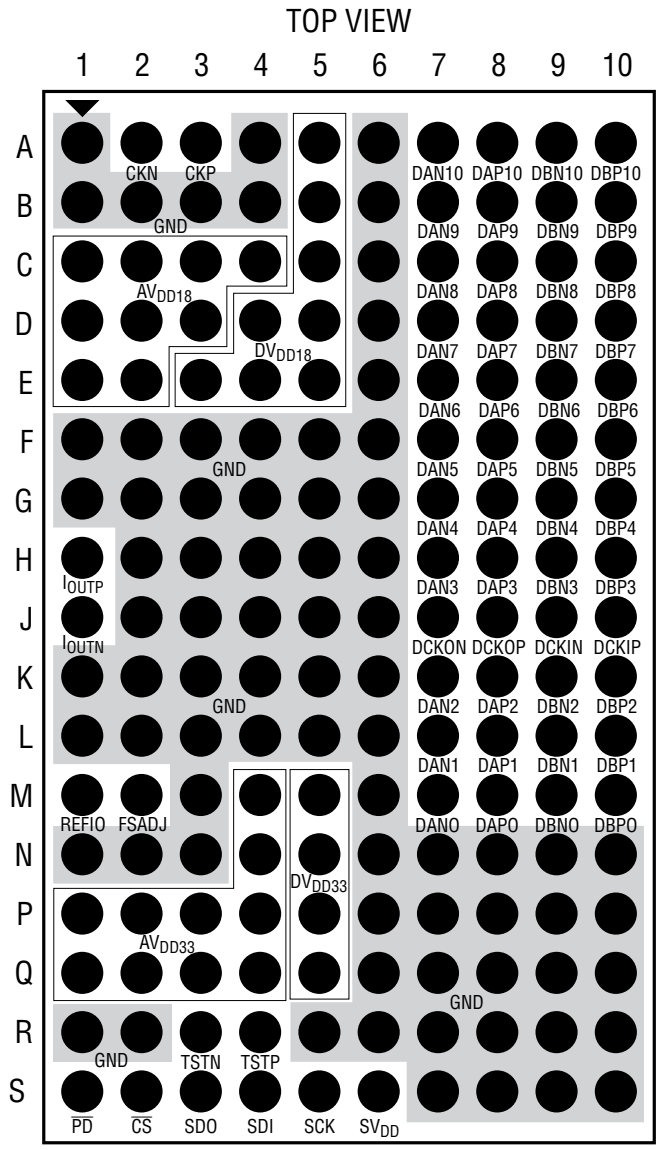
LTC2000-11 BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	GND	B1	GND	C1	AV_{DD18}	D1	AV_{DD18}	E1	AV_{DD18}	F1	GND
A2	CKN	B2	GND	C2	AV_{DD18}	D2	AV_{DD18}	E2	AV_{DD18}	F2	GND
A3	CKP	B3	GND	C3	AV_{DD18}	D3	AV_{DD18}	E3	DV_{DD18}	F3	GND
A4	GND	B4	GND	C4	AV_{DD18}	D4	DV_{DD18}	E4	DV_{DD18}	F4	GND
A5	DV_{DD18}	B5	DV_{DD18}	C5	DV_{DD18}	D5	DV_{DD18}	E5	DV_{DD18}	F5	GND
A6	GND	B6	GND	C6	GND	D6	GND	E6	GND	F6	GND
A7	DAN10	B7	DAN9	C7	DAN8	D7	DAN7	E7	DAN6	F7	DAN5
A8	DAP10	B8	DAP9	C8	DAP8	D8	DAP7	E8	DAP6	F8	DAP5
A9	DBN10	B9	DBN9	C9	DBN8	D9	DBN7	E9	DBN6	F9	DBN5
A10	DBP10	B10	DBP9	C10	DBP8	D10	DBP7	E10	DBP6	F10	DBP5

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	GND	H1	I_{OUTP}	J1	I_{OUTN}	K1	GND	L1	GND	M1	REFIO
G2	GND	H2	GND	J2	GND	K2	GND	L2	GND	M2	FSADJ
G3	GND	H3	GND	J3	GND	K3	GND	L3	GND	M3	GND
G4	GND	H4	GND	J4	GND	K4	GND	L4	GND	M4	AV_{DD33}
G5	GND	H5	GND	J5	GND	K5	GND	L5	GND	M5	DV_{DD33}
G6	GND	H6	GND	J6	GND	K6	GND	L6	GND	M6	GND
G7	DAN4	H7	DAN3	J7	DCKON	K7	DAN2	L7	DAN1	M7	DAN0
G8	DAP4	H8	DAP3	J8	DCKOP	K8	DAP2	L8	DAP1	M8	DAP0
G9	DBN4	H9	DBN3	J9	DCKIN	K9	DBN2	L9	DBN1	M9	DBN0
G10	DBP4	H10	DBP3	J10	DCKIP	K10	DBP2	L10	DBP1	M10	DBP0

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
N1	GND	P1	AV_{DD33}	Q1	AV_{DD33}	R1	GND	S1	$\overline{PD}$
N2	GND	P2	AV_{DD33}	Q2	AV_{DD33}	R2	GND	S2	$\overline{CS}$
N3	GND	P3	AV_{DD33}	Q3	AV_{DD33}	R3	TSTN	S3	SDO
N4	AV_{DD33}	P4	AV_{DD33}	Q4	AV_{DD33}	R4	TSTP	S4	SDI
N5	DV_{DD33}	P5	DV_{DD33}	Q5	DV_{DD33}	R5	GND	S5	SCK
N6	GND	P6	GND	Q6	GND	R6	GND	S6	SV_{DD}
N7	GND	P7	GND	Q7	GND	R7	GND	S7	GND
N8	GND	P8	GND	Q8	GND	R8	GND	S8	GND
N9	GND	P9	GND	Q9	GND	R9	GND	S9	GND
N10	GND	P10	GND	Q10	GND	R10	GND	S10	GND

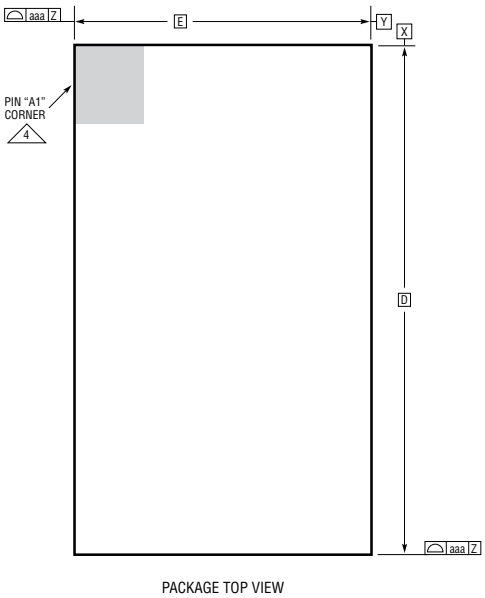
PIN LOCATIONS (LTC2000-11)



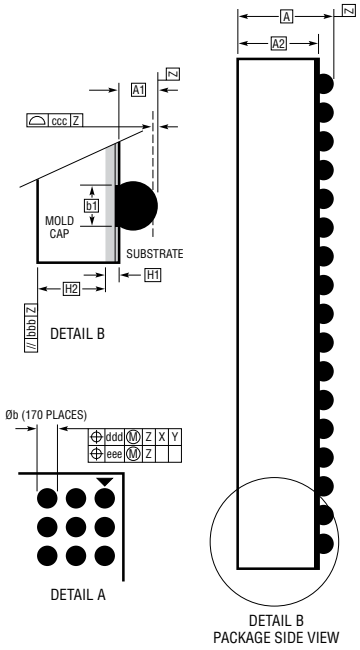
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2000#packaging for the most recent package drawings.

BGA Package
170-Lead (15.00mm × 9.00mm × 1.54mm)
(Reference LTC DWG# 05-08-1890 Rev C)

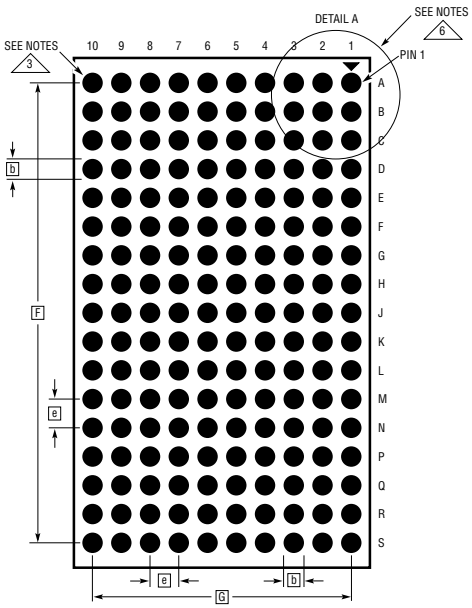


PACKAGE TOP VIEW

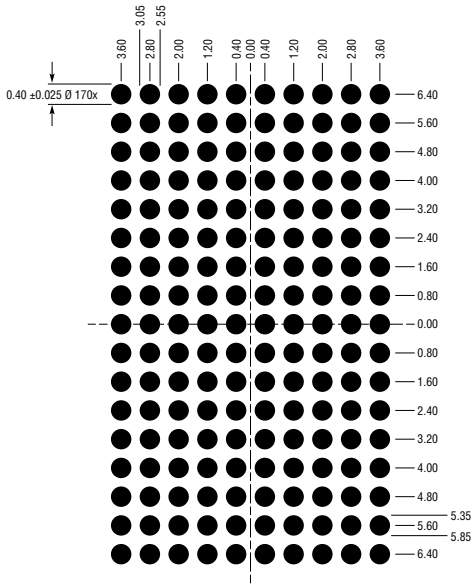


DETAIL A

DETAIL B
PACKAGE SIDE VIEW



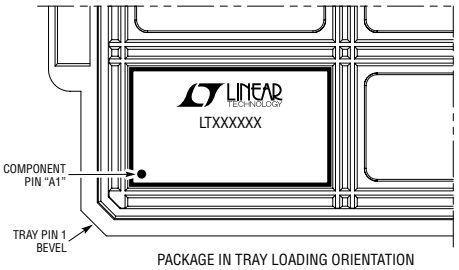
PACKAGE BOTTOM VIEW



SUGGESTED PCB LAYOUT
TOP VIEW

DIMENSIONS				
SYMBOL	**MIN**	**NOM**	**MAX**	**NOTES**
A	1.39	1.54	1.69	
A1	0.35	0.40	0.45	BALL HT
A2	1.04	1.14	1.24	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		15.00		
E		9.00		
e		0.80		
F		12.80		
G		7.20		
H1	0.39	0.44	0.49	SUBSTRATE THK
H2	0.65	0.70	0.75	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.12	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 170				

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



PACKAGE IN TRAY LOADING ORIENTATION

BGA 170 0517 REV C

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/17	Added lead-finish option	4
B	12/17	Update to text regarding series resistance requirement	33