32-Bit Oversampling ADC with Configurable Digital Filter

FEATURES

- **±0.5ppm INL (Typ)**
- **145dB Dynamic Range (Typ) at 61sps**
- **131dB Dynamic Range (Typ) at 4ksps**
- **Guaranteed 32-Bits No Missing Codes**
- **Configurable Digital Filter with Synchronization**
  - Relaxed Anti-Aliasing Filter Requirements
- **Dual Output 32-Bit SAR ADC**
  - 32-Bit Digitally Filtered Low Noise Output
  - 14-Bit Differential + 8-Bit Common Mode 1Msps No Latency Output
- **Wide Input Common Mode Range**
- Guaranteed Operation to 85°C
- 1.8V to 5V SPI-Compatible Serial I/O
- Low Power: 24mW at 1Msps
- 24-Lead 7mm × 4mm DFN Package

APPLICATIONS

- Seismology
- Energy Exploration
- Automated Test Equipment (ATE)
- High Accuracy Instrumentation

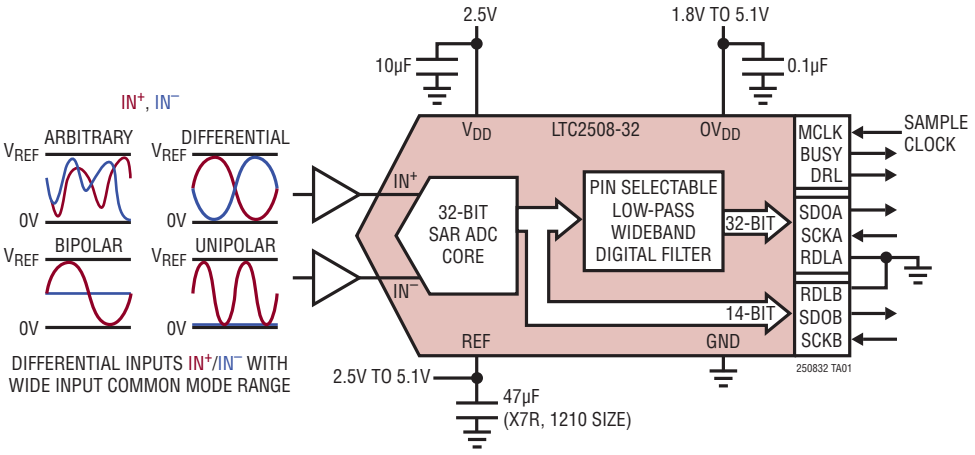
DESCRIPTION

The LTC®2508-32 is a low noise, low power, high performance 32-bit ADC with an integrated configurable digital filter. Operating from a single 2.5V supply, the LTC2508-32 features a fully differential input range up to $\pm V_{REF}$, with V_{REF} ranging from 2.5V to 5.1V. The LTC2508-32 supports a wide common mode range from 0V to V_{REF} simplifying analog signal conditioning requirements.

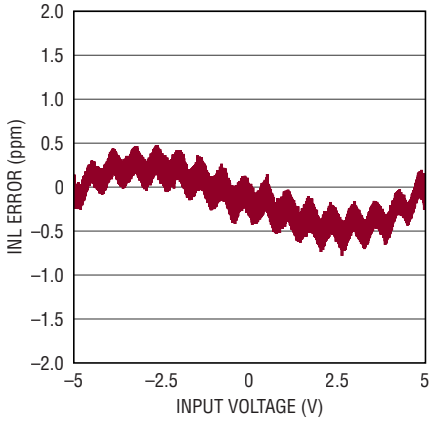
The LTC2508-32 simultaneously provides two output codes: (1) a 32-bit digitally filtered high precision low noise code, and (2) a 22-bit no latency composite code. The configurable digital filter reduces measurement noise by lowpass filtering and down-sampling the stream of data from the SAR ADC core, giving the 32-bit filtered output code. The 22-bit composite code consists of a 14-bit code representing the differential voltage and an 8-bit code representing the common mode voltage. The 22-bit composite code is available each conversion cycle, with no cycle of latency.

The digital filter can be easily configured for 4 different down-sampling factors by pin strapping. The configurations provide a dynamic range of 131dB at 3.9ksps and 145dB at 61sps. The digital lowpass filter relaxes the requirements for analog anti-aliasing. Multiple LTC2508-32 devices can be easily synchronized using the SYNC pin.

TYPICAL APPLICATION



Integral Nonlinearity vs Input Voltage

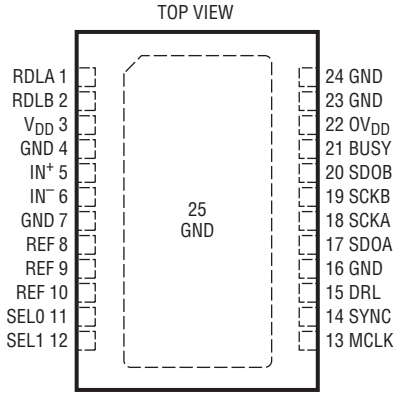


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) 2.8V
Supply Voltage (OV_{DD}) 6V
Reference Input (REF) 6V
Analog Input Voltage (Note 3)
IN^+, IN^- ..... (GND – 0.3V) to (REF + 0.3V)
Digital Input Voltage
(Note 3) ..... (GND – 0.3V) to (OV_{DD} + 0.3V)
Digital Output Voltage
(Note 3) ..... (GND – 0.3V) to (OV_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
LTC2508C-32 ..... 0°C to 70°C
LTC2508I-32 ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DKD PACKAGE
24-LEAD (7mm × 4mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC2508-32#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2508CDKD-32#PBF	LTC2508CDKD-32#TRPBF	250832	24-Lead (7mm × 4mm) Plastic DFN	0°C to 70°C
LTC2508IDKD-32#PBF	LTC2508IDKD-32#TRPBF	250832	24-Lead (7mm × 4mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}^+	Absolute Input Range (IN^+)	(Note 5)	●	0		V_{REF}	V
V_{IN}^-	Absolute Input Range (IN^-)	(Note 5)	●	0		V_{REF}	V
$V_{IN}^+ - V_{IN}^-$	Input Differential Voltage Range	$V_{IN} = V_{IN}^+ - V_{IN}^-$	●	$-V_{REF}$		V_{REF}	V
V_{CM}	Common-Mode Input Range		●	0		V_{REF}	V
I_{IN}	Analog Input Leakage Current				10		nA
C_{IN}	Analog Input Capacitance	Sample Mode Hold Mode			45 5		pF pF
CMRR	Input Common Mode Rejection Ratio	Filtered Output $V_{IN}^+ = V_{IN}^- = 4.5V_{P-P}$, 200Hz Sine			128		dB

CONVERTER CHARACTERISTICS FOR FILTERED OUTPUT (SDOA)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	32			Bits
	No Missing Codes		●	32			Bits
DF	Down-sampling Factor		●	256		16384	
	Transition Noise	DF = 256 (Note 6) DF = 1024 DF = 4096 DF = 16384			0.095 0.055 0.03 0.02		ppm ppm ppm ppm
INL	Integral Linearity Error	(Note 7)	●	–3.5	0.5	3.5	ppm
ZSE	Zero-Scale Error	(Note 9)	●	–13	0	13	ppm
	Zero-Scale Error Drift				±14		ppb/°C
FSE	Full-Scale Error	(Note 9)	●	–100	±10	100	ppm
	Full-Scale Error Drift				±0.05		ppm/°C

DYNAMIC ACCURACY FOR FILTERED OUTPUT (SDOA)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and A_{IN} = –20dBFS. (Notes 4, 10)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DR	Dynamic Range	V_{REF} = 5V, DF = 256 $IN^+ = IN^- = V_{CM}$, V_{REF} = 5V, DF = 1024 $IN^+ = IN^- = V_{CM}$, V_{REF} = 5V, DF = 4096 $IN^+ = IN^- = V_{CM}$, V_{REF} = 5V, DF = 16384	●	125	131 136 141 145		dB dB dB dB
THD	Total Harmonic Distortion	f_{IN} = 200Hz, V_{REF} = 2.5V, DF = 256 f_{IN} = 200Hz, V_{REF} = 5V, DF = 256	 ●		–118 –118	 –108	dB dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 200Hz, V_{REF} = 2.5V, DF = 256 f_{IN} = 200Hz, V_{REF} = 5V, DF = 256	 ●	 108	118 118		dB dB
	–3dB Input Bandwidth				34		MHz
	Aperture Delay				500		ps
	Aperture Jitter				4		ps_{RMS}
	Transient Response	Full-Scale Step			125		ns

CONVERTER CHARACTERISTICS FOR NO LATENCY OUTPUT (SDOB)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution: Differential Common Mode		 ● ●	 14 8			 Bits Bits
	No Missing Codes: Differential Common Mode		 ● ●	 14 8			 Bits Bits
	Transition Noise Differential Common Mode	(Note 6)			 1 1		 LSB_{RMS} LSB_{RMS}
INL	Integral Linearity Error Differential Common Mode	(Note 7)			 ±0.1 ±0.1		 LSB LSB
DNL	Differential Linearity Error Differential Common Mode				 ±0.1 ±0.1		 LSB LSB
ZSE	Zero Scale Error Differential Common Mode				 ±1 ±1		 LSB LSB
FSE	Zero Scale Error Differential Common Mode				 ±1 ±1		 LSB LSB

REFERENCE INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 4, 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	(Note 5)	●	2.5		5.1	V
I_{REF}	Reference Input Current	(Note 11)	●		0.7	1	mA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	0.8•OV_{DD}			V
V_{IL}	Low Level Input Voltage		●			0.2•OV_{DD}	V
I_{IN}	Digital Input Current	V_{IN} = 0V to OV_{DD}	●	–10		10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	I_O = –500µA	●	OV_{DD}–0.2			V
V_{OL}	Low Level Output Voltage	I_O = 500µA	●			0.2	V
I_{OZ}	Hi-Z Output Leakage Current	V_{OUT} = 0V to OV_{DD}	●	–10		10	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = OV_{DD}			10		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		●	2.375	2.5	2.625	V
OV_{DD}	Supply Voltage		●	1.71		5.25	V
I_{VDD}	Supply Current	1Msps Sample Rate	●		9.5	13	mA
I_{OVDD}	Supply Current	1Msps Sample Rate (C_L = 20pF)			1		mA
I_{PD}	Power Down Mode	Conversion Done (I_{VDD} + I_{OVDD} + I_{REF})	●		6	350	µA
P_D	Power Dissipation	1Msps Sample Rate (I_{VDD})			24	32.5	mW
	Power Down Mode	Conversion Done (I_{VDD} + I_{OVDD} + I_{REF})			15	875	µW

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SMPL}	Maximum Sampling Frequency		●			1	Msps
f_{DRA}	Output Data Rate at SDOA		●			3.9	ksps
f_{DRB}	Output Data Rate at SDOB		●			1	Msps
t_{CONV}	Conversion Time		●	578		652	ns
t_{ACQ}	Acquisition Time	$t_{ACQ} = t_{CYC} - t_{CONV} - t_{BUSYLH}$ (Note 8)	●	335			ns
t_{CYC}	Time Between Conversions		●	1000			ns
t_{MCLKH}	MCLK High Time		●	20			ns
t_{MCLKL}	Minimum Low Time for MCLK	(Note 12)	●	20			ns
t_{BUSYLH}	MCLK↑ to BUSY↑ Delay	C_L = 20pF	●			13	ns
t_{DRLLH}	MCLK to DRL↑ Delay	C_L = 20pF	●			18	ns
t_{QUIET}	SCKA, SCKB Quiet Time from MCLK↑	(Note 8)	●	10			ns
t_{SCKA}	SCKA Period	(Notes 12, 13)	●	10			ns
t_{SCKAH}	SCKA High Time		●	4			ns
t_{SCKAL}	SCKA Low Time		●	4			ns
t_{DSDOA}	SDOA Data Valid Delay from SCKA↑	C_L = 20pF, OV_{DD} = 5.25V	●			8.5	ns
		C_L = 20pF, OV_{DD} = 2.5V	●			8.5	ns
		C_L = 20pF, OV_{DD} = 1.71V	●			9.5	ns
t_{HSDOA}	SDOA Data Remains Valid Delay from SCKA↑	C_L = 20pF (Note 8)	●	1			ns
$t_{DSDOADRLL}$	SDOA Data Valid Delay from DRL↓	C_L = 20pF (Note 8)	●			5	ns
t_{ENAA}	Bus Enable Time After RDLA↓	(Note 12)	●			16	ns
t_{DISA}	Bus Relinquish Time After RDLA↑	(Note 12)	●			13	ns
t_{SCKB}	SCKB Period	(Notes 12, 13)	●	10			ns
t_{SCKBH}	SCKB High Time		●	4			ns
t_{SCKBL}	SCKB Low Time		●	4			ns
t_{DSDOB}	SDOB Data Valid Delay from SCKB↑	C_L = 20pF, OV_{DD} = 5.25V	●			8.5	ns
		C_L = 20pF, OV_{DD} = 2.5V	●			8.5	ns
		C_L = 20pF, OV_{DD} = 1.71V	●			9.5	ns
t_{HSDOB}	SDOB Data Remains Valid Delay from SCKB↑	C_L = 20pF (Note 8)	●	1			ns

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{DSDOBBUSYL}$	SDOB Data Valid Delay from BUSY↓	C_L = 20pF (Note 8)	●			5	ns
t_{ENB}	Bus Enable Time After RDLB↓	(Note 12)	●			16	ns
t_{DISB}	Bus Relinquish Time After RDLB↑	(Note 12)	●			13	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground.

Note 3: When these pin voltages are taken below ground or above REF or OV_{DD}, they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground or above REF or OV_{DD} without latch-up.

Note 4: V_{DD} = 2.5V, OV_{DD} = 2.5V, REF = 5V, V_{CM} = 2.5V, f_{SMPL} = 1MHz, DF = 256.

Note 5: Recommended operating conditions.

Note 6: Transition noise is defined as the noise level of the ADC with IN^+ and IN^- shorted.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Guaranteed by design, not subject to test.

Note 9: Bipolar zero-scale error is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 0000 0000 0000 0000 0000 and 1111 1111 1111 1111 1111 1111 1111 1111. Full-scale bipolar error is the worst-case of –FS or +FS untrimmed deviation from ideal first and last code transitions and includes the effect of offset error.

Note 10: All specifications in dB are referred to a full-scale ±5V input with a 5V reference voltage.

Note 11: f_{SMPL} = 1MHz, I_{REF} varies proportionally with sample rate.

Note 12: Parameter tested and guaranteed at OV_{DD} = 1.71V, OV_{DD} = 2.5V and OV_{DD} = 5.25V.

Note 13: t_{SCKA}, t_{SCKB} of 10ns maximum allows a shift clock frequency up to 100MHz for rising edge capture.

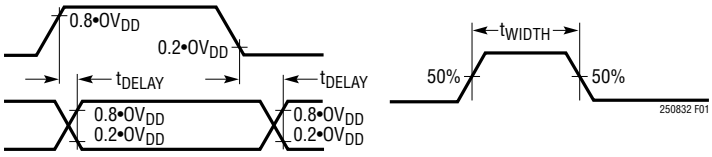
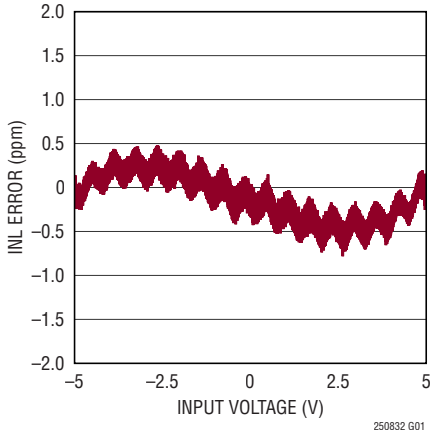


Figure 1. Voltage Levels for Specifications

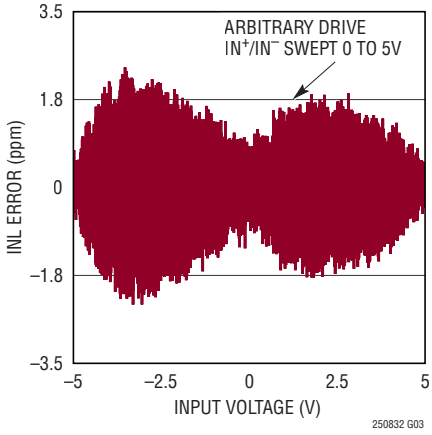
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 2.5V, OV_{DD} = 2.5V, V_{CM} = 2.5V, REF = 5V, f_{SMPL} = 1Msps, DF = 256, Filtered Output, unless otherwise noted.

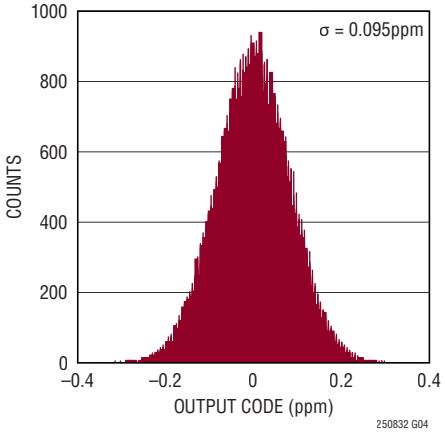
Integral Nonlinearity vs Input Voltage



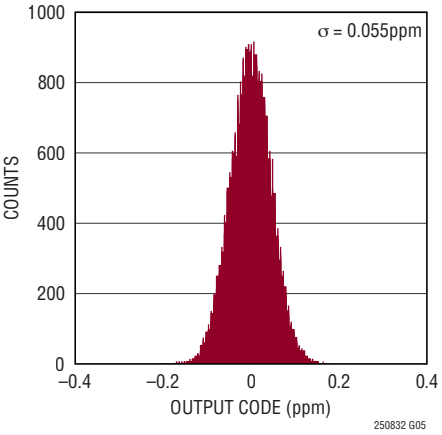
Integral Nonlinearity vs Input Voltage



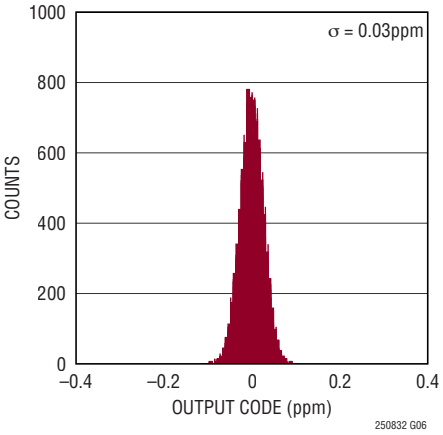
DC Histogram, DF = 256



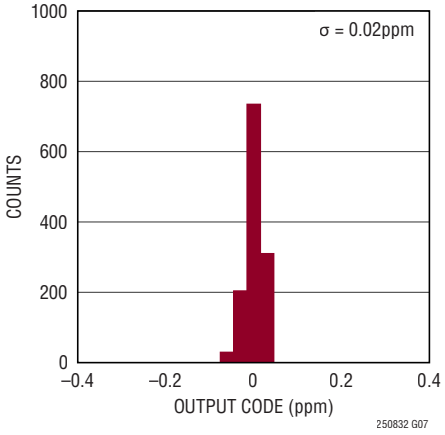
DC Histogram, DF = 1024



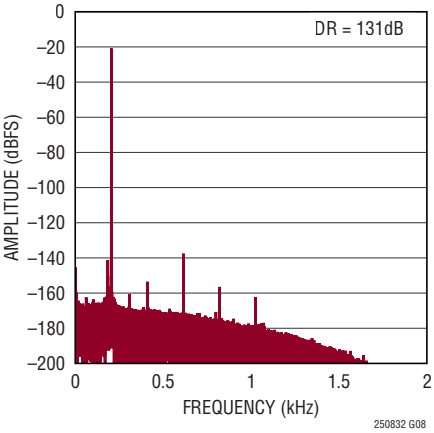
DC Histogram, DF = 4096



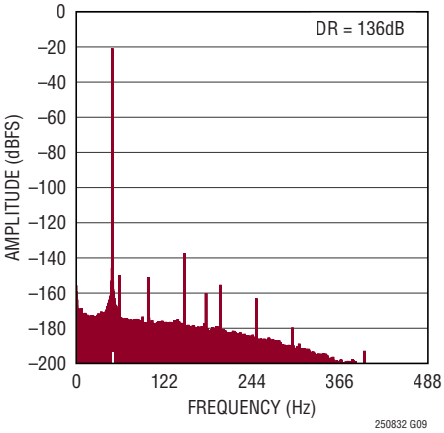
DC Histogram, DF = 16384



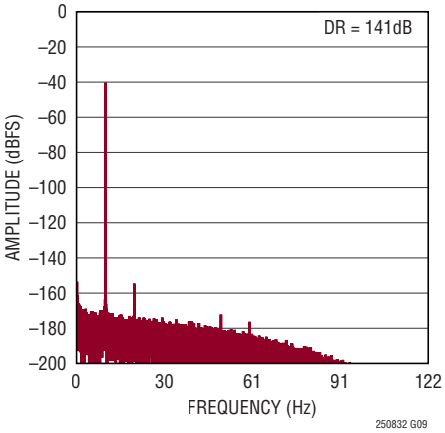
128k Point FFT f_{SMPL} = 1Msps, f_{IN} = 200Hz, DF = 256



128k Point FFT f_{SMPL} = 1Msps, f_{IN} = 50Hz, DF = 1024



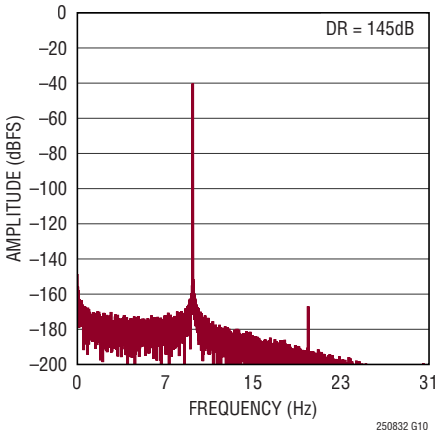
32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 10Hz, DF = 4096



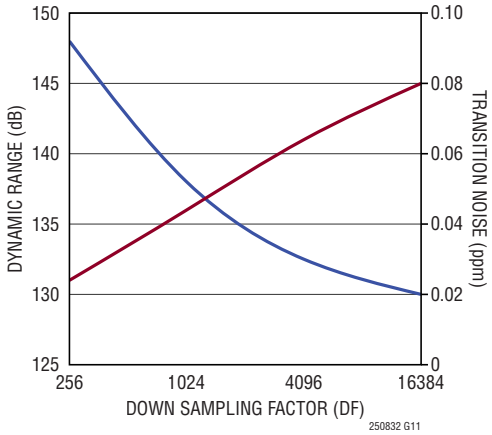
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 2.5V, OV_{DD} = 2.5V, V_{CM} = 2.5V, REF = 5V, f_{SMPL} = 1Msps, DF = 256, Filtered Output, unless otherwise noted.

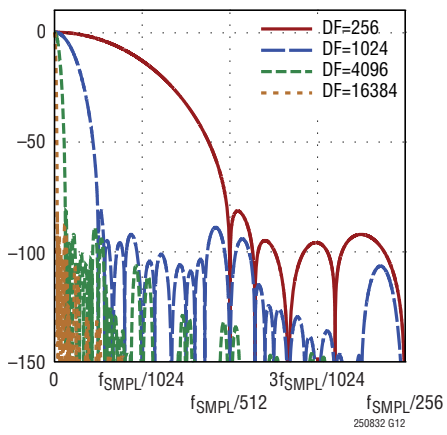
8k Point FFT f_{SMPL} = 1Msps, f_{IN} = 10Hz, DF = 16384



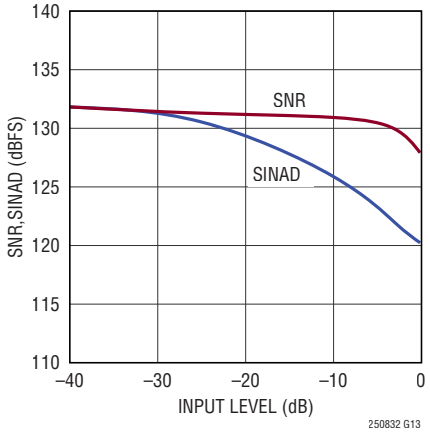
Dynamic Range, Transition Noise vs DF



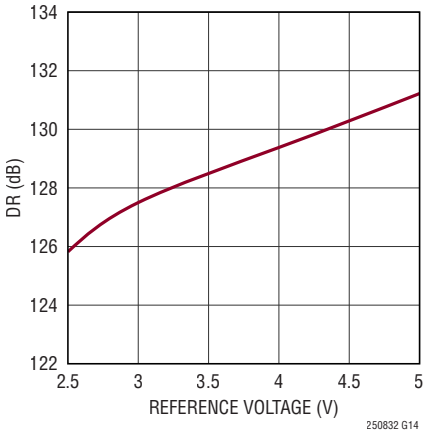
Frequency Response, DF = 256, 1024, 4096, 16384



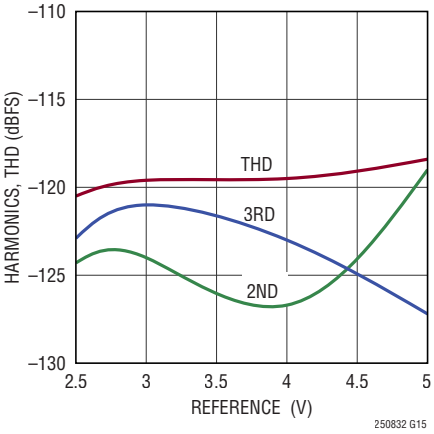
SNR, SINAD vs Input level, f_{IN} = 200Hz



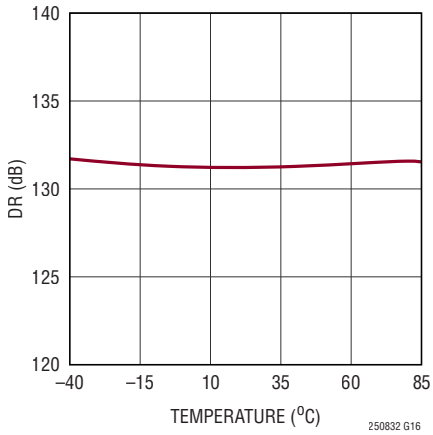
Dynamic Range vs Reference Voltage, f_{IN} = 200Hz, A_{IN} = –20dBFS



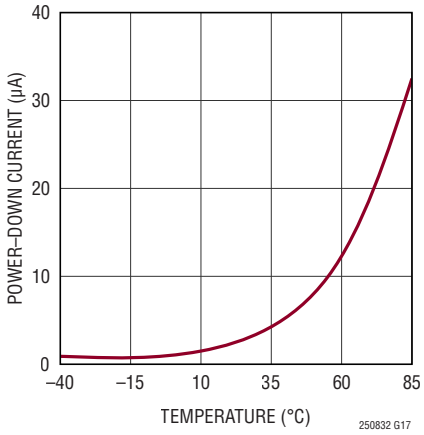
THD, Harmonics vs Reference Voltage, f_{IN} = 200Hz, A_{IN} = –1dBFS



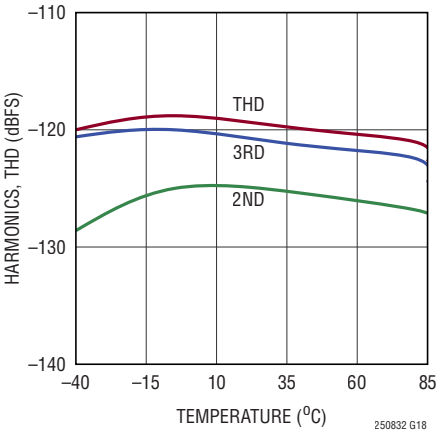
Dynamic Range vs Temperature, f_{IN} = 100Hz, A_{IN} = –20dBFS



Shutdown Current vs Temperature



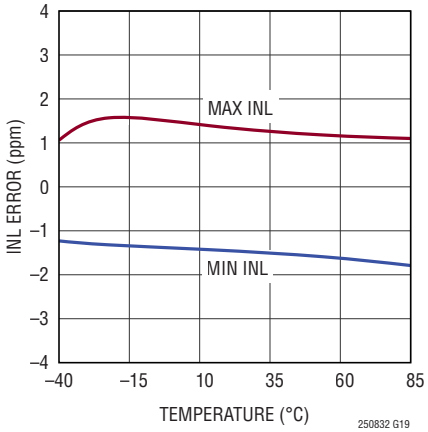
THD, Harmonics vs Temperature, f_{IN} = 200Hz, A_{IN} = –1dBFS



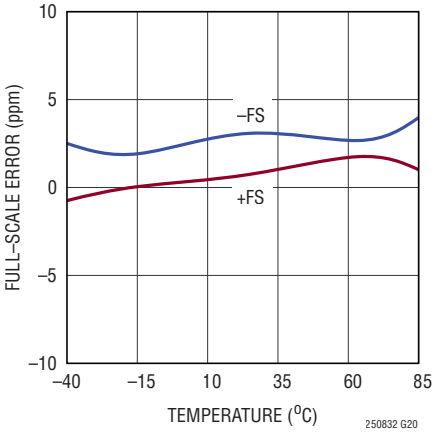
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 2.5V, OV_{DD} = 2.5V, V_{CM} = 2.5V, REF = 5V, f_{SMPL} = 1Msps, DF = 256, Filtered Output, unless otherwise noted.

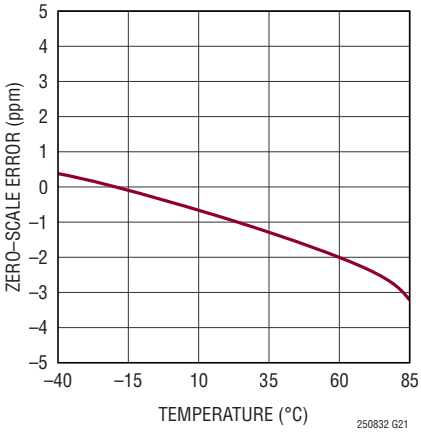
INL vs Temperature



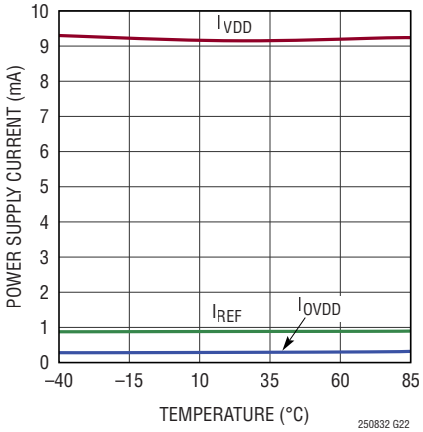
Full-Scale Error vs Temperature



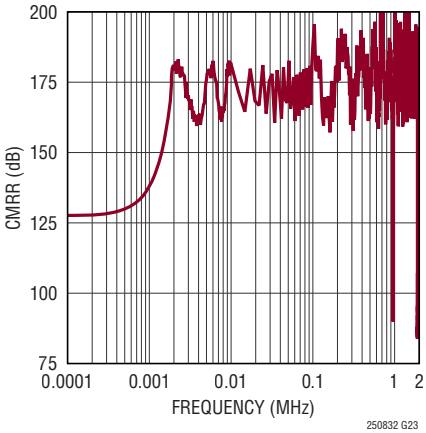
Offset Error vs Temperature



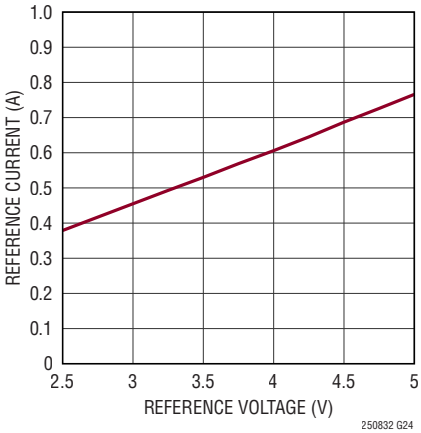
Supply Current vs Temperature



Common Mode Rejection vs Input Frequency



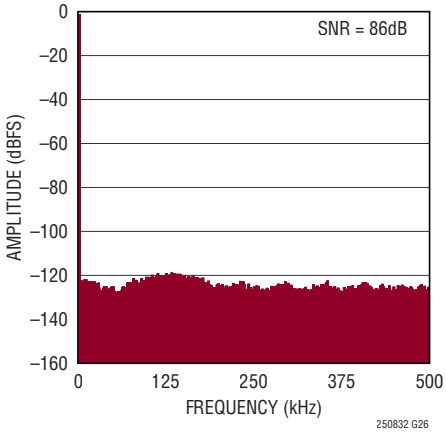
Reference Current vs Reference Voltage



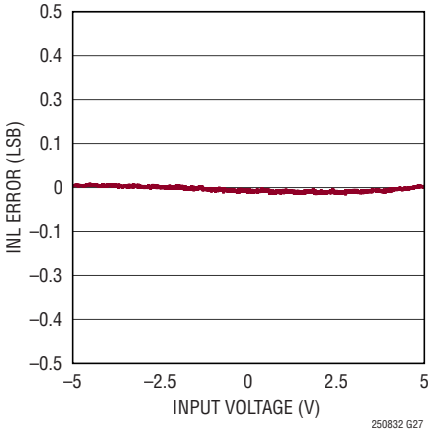
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 2.5V, OV_{DD} = 2.5V, V_{CM} = 2.5V, REF = 5V, f_{SMPL} = 1Msps, DF = 256, No Latency Output, unless otherwise noted.

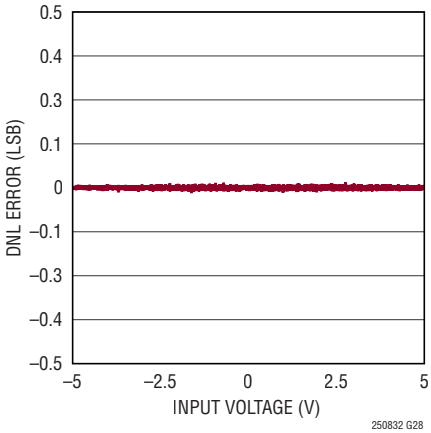
No Latency Differential Output 128k Point FFT



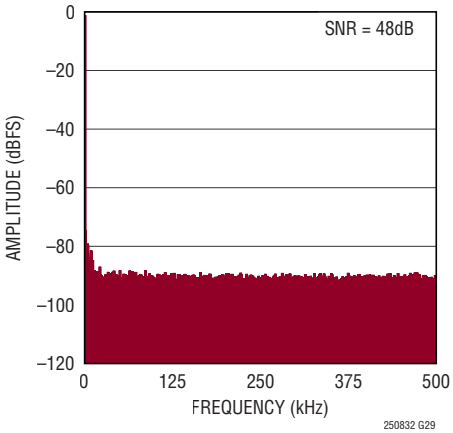
No Latency Differential Output INL vs Input Voltage



No Latency Differential Output DNL vs Input Voltage



No Latency Common Mode Output 128k Point FFT



PIN FUNCTIONS

RDLA (Pin 1): Read Low Input A (Filtered Output). When RDLA is low, the serial data output A (SDOA) pin is enabled. When RDLA is high, SDOA pin is in a high-impedance state. Logic levels are determined by OV_{DD}.

RDLB (Pin 2): Read Low Input B (No Latency Output). When RDLB is low, the serial data output B (SDOB) pin is enabled. When RDLB is high, SDOB pin is in a high-impedance state. Logic levels are determined by OV_{DD}.

V_{DD} (Pin 3): 2.5V Power Supply. The range of V_{DD} is 2.375V to 2.625V. Bypass V_{DD} to GND with a 10µF ceramic capacitor.

GND (Pins 4, 7, 16, 23, 24): Ground.

IN^+ (Pin 5): Positive Analog Input.

IN^- (Pin 6): Negative Analog Input.

REF (Pins 8, 9, 10): Reference Input. The range of REF is 2.5V to 5.1V. This pin is referred to the GND pin and should be decoupled closely to the pin with a 47µF ceramic capacitor (X7R, 1210 size, 10V rating).

SEL0, SEL1 (Pins 11, 12): Down-Sampling Factor Select Input 0, Down-Sampling Factor Select Input 1. Selects the down-sampling factor for the digital filter. Down-sampling factors of 256, 1024, 4096 and 16384 are selected for [SEL0 SEL1] combinations of 00, 01, 10 and 11 respectively. Logic levels are determined by OV_{DD}.

MCLK (Pin 13): Master Clock Input. A rising edge on this input powers up the part and initiates a new conversion. Logic levels are determined by OV_{DD}.

SYNC (Pin 14): Synchronization Input. A pulse on this input is used to synchronize the phase of the digital filter. Logic levels are determined by OV_{DD}.

DRL (Pin 15): Data Ready Low Output. A falling edge on this pin indicates that a new filtered output code is available in the output register of SDOA. Logic levels are determined by OV_{DD}.

SDOA (Pin 17): Serial Data Output A (Filtered Output). The filtered output code appears on this pin (MSB first) on each rising edge of SCKA. The output data is in 2's complement format. Logic levels are determined by OV_{DD}.

SCKA (Pin 18): Serial Data Clock Input A (Filtered Output). When SDOA is enabled, the filtered output code is shifted out (MSB first) on the rising edges of this clock. Logic levels are determined by OV_{DD}.

SCKB (Pin 19): Serial Data Clock Input B (No Latency Output). When SDOB is enabled, the no latency output code is shifted out (MSB first) on the rising edges of this clock. Logic levels are determined by OV_{DD}.

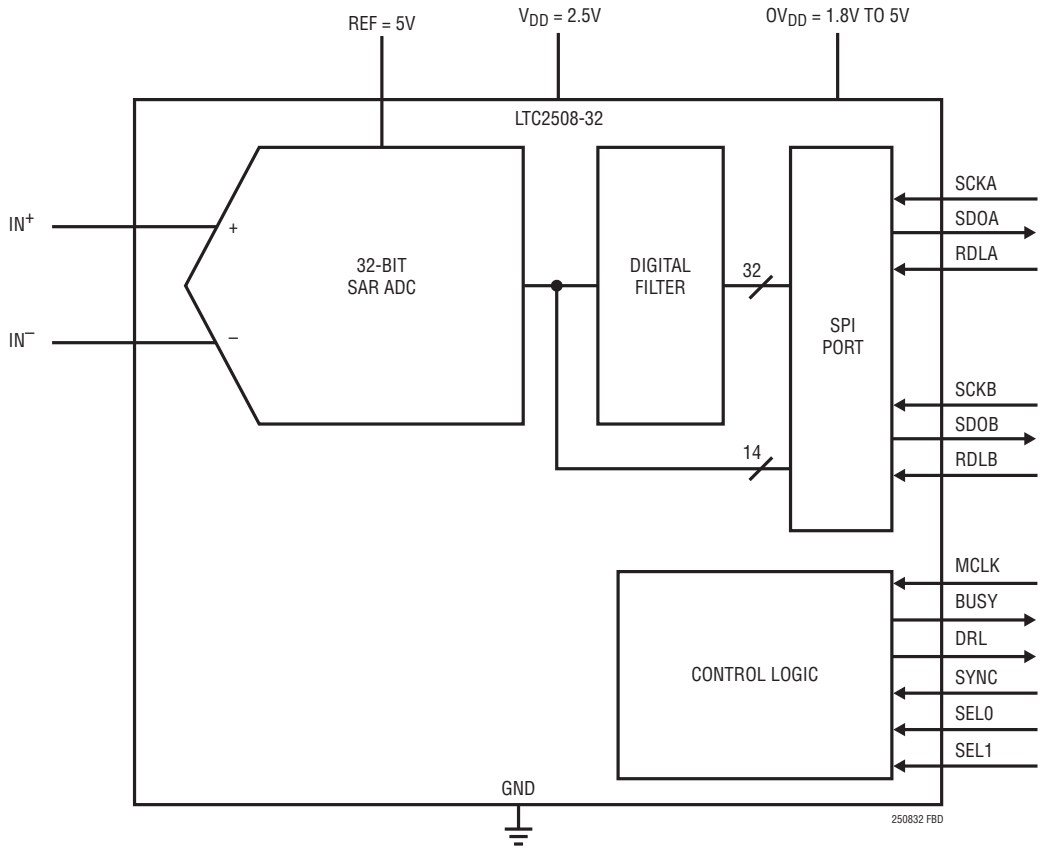
SDOB (Pin 20): Serial Data Output B (No Latency Output). The 22-bit no latency composite output code appears on this pin (MSB first) on each rising edge of SCKB. The output data is in 2's complement format. Logic levels are determined by OV_{DD}.

BUSY (Pin 21): BUSY Indicator. Goes high at the start of a new conversion and returns low when the conversion has finished. Logic levels are determined by OV_{DD}.

OV_{DD} (Pin 22): I/O Interface Digital Power. The range of OV_{DD} is 1.71V to 5.25V. This supply is nominally set to the same supply as the host interface (1.8V, 2.5V, 3.3V, or 5V). Bypass OV_{DD} to GND (Pin 23) close to the pin with a 0.1µF capacitor.

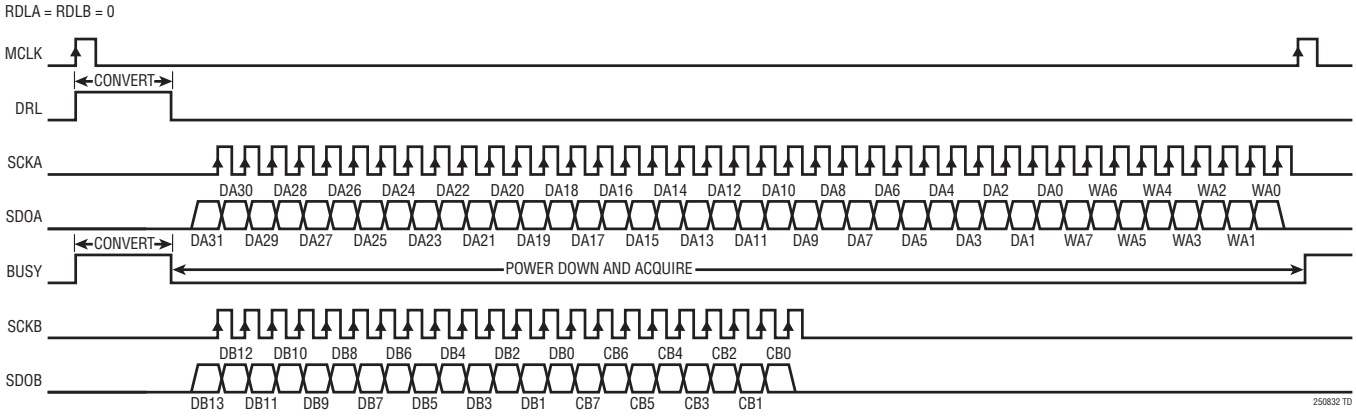
GND (Exposed Pad Pin 25): Ground. Exposed pad must be soldered directly to the ground plane.

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM

Conversion Timing Using the Serial Interface



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OVERVIEW

The LTC2508-32 is a low noise, low power, high-performance 32-bit ADC with an integrated configurable digital filter. Operating from a single 2.5V supply, the LTC2508-32 features a fully differential input range up to $\pm V_{REF}$, with V_{REF} ranging from 2.5V to 5.1V. The LTC2508-32 supports a wide common mode range from 0V to V_{REF} simplifying analog signal conditioning requirements.

The LTC2508-32 simultaneously provides two output codes: (1) a 32-bit digitally filtered high precision low noise code, and (2) a 22-bit no latency composite code. The configurable digital filter reduces measurement noise by lowpass filtering and down-sampling the stream of data from the SAR ADC core, giving the 32-bit filtered output code. The 22-bit composite code consists of a 14-bit code representing the differential voltage and an 8-bit code representing the common mode voltage. The 22-bit composite code is available each conversion cycle, with no cycle of latency.

The digital filter can be easily configured for 4 different down-sampling factors by pin strapping. The configurations provide a dynamic range of 131dB at 3.9ksps and 145dB at 61sps. The digital lowpass filter relaxes the requirements for analog anti-aliasing. Multiple LTC2508-32 devices can be easily synchronized using the SYNC pin.

CONVERTER OPERATION

The LTC2508-32 operates in two phases. During the acquisition phase, a 32-bit charge redistribution capacitor D/A converter (CDAC) is connected to the IN^+ and IN^- pins to sample the analog input voltages. A rising edge on the MCLK pin initiates a conversion. During the conversion phase, the 32-bit CDAC is sequenced through a successive approximation algorithm, effectively comparing the sampled inputs with binary-weighted fractions of the reference voltage (e.g. $V_{REF}/2$, $V_{REF}/4$ … $V_{REF}/4294967296$). At the end of conversion, the CDAC output approximates the sampled analog input. The ADC control logic then passes the 32-bit digital output code to the digital filter for further processing. A 14-bit code representing the differential voltage and an 8-bit code representing the common mode voltage are combined to form a 22-bit composite code. The 22-bit composite code is available each conversion cycle, without any cycle of latency.

TRANSFER FUNCTION

The LTC2508-32 digitizes the full-scale differential voltage of $2\times V_{REF}$ into 2^{32} levels, resulting in an LSB size of 2.3nV with a 5V reference. The ideal transfer function is shown in Figure 2. The output data is in 2's complement format.

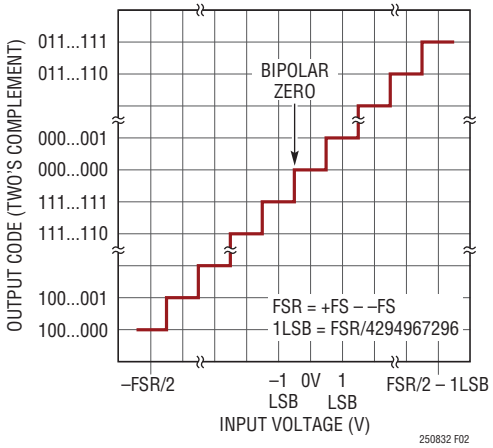

Figure 2. LTC2508-32 Transfer Function

ANALOG INPUT

The LTC2508-32 samples the voltage difference ($IN^+ – IN^-$) between its analog input pins over a wide common mode input range while attenuating unwanted signals common to both input pins by the common-mode rejection ratio (CMRR) of the ADC. Wide common mode input range coupled with high CMRR allows the IN^+/IN^- analog inputs to swing with an arbitrary relationship to each other, provided each pin remains between GND and V_{REF}. This unique feature of the LTC2508-32 enables it to accept a wide variety of signal swings, including traditional classes of analog input signals such as pseudo-differential unipolar, pseudo-differential true bipolar, and fully differential, thereby simplifying signal chain design.

In the acquisition phase, each input sees approximately 45pF (C_{IN}) from the sampling circuit in series with 40Ω (R_{ON}) from the on-resistance of the sampling switch.

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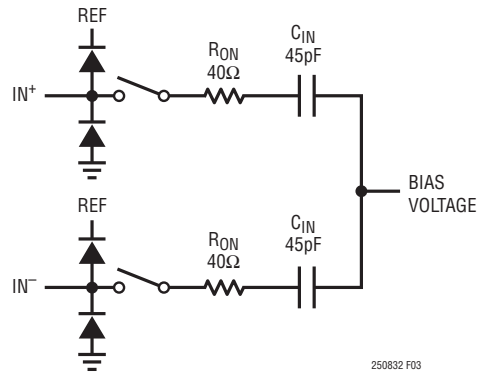

Figure 3. The Equivalent Circuit for the Differential Analog Input of the LTC2508-32

The inputs draw a current spike while charging the C_{IN} capacitors during acquisition. During conversion, the analog inputs draw only a small leakage current.

INPUT DRIVE CIRCUITS

A low impedance source can directly drive the high impedance inputs of the LTC2508-32 without gain error. A high impedance source should be buffered to minimize settling time during acquisition and to optimize ADC linearity. For best performance, a buffer amplifier should be used to drive the analog inputs of the LTC2508-32. The amplifier provides low output impedance, which produces fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the ADC inputs.

Noise and Distortion

The noise and distortion of an input buffer amplifier and other supporting circuitry must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the buffer amplifier with a low bandwidth filter to minimize noise. The simple one-pole RC lowpass filter (LPF1) shown in Figure 4 is sufficient for many applications.

A coupling filter network (LPF2) should be used between the buffer and ADC input to minimize disturbances reflected into the buffer from sampling transients. Long RC time constants at the analog inputs will slow down the settling of the analog inputs. Therefore, LPF2 typically requires wider bandwidth than LPF1. This filter also helps minimize the noise contribution from the buffer. A buffer amplifier with a low noise density must be selected to minimize degradation of SNR.

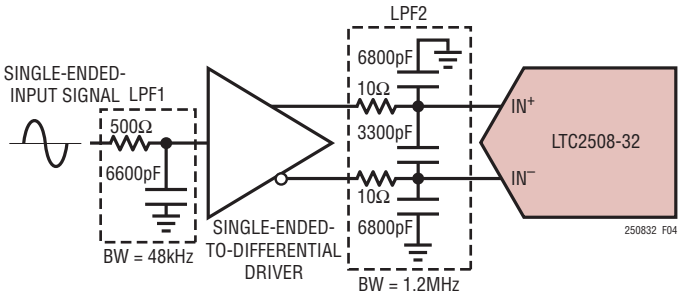

Figure 4. Filtering Input Signal

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self-heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Input Currents

An important consideration when coupling an amplifier to the LTC2508-32 is in dealing with current spikes drawn by the ADC inputs at the start of each acquisition phase. The ADC inputs may be modeled as a switched capacitor load of the drive circuit. A drive circuit may rely partially on attenuating switched-capacitor current spikes with small filter capacitors C_{FILT} placed directly at the ADC inputs, and partially on the driver amplifier having sufficient bandwidth to recover from the residual disturbance. Amplifiers optimized for DC performance may not have sufficient bandwidth to fully recover at the ADC's maximum conversion rate, which can produce nonlinearity and other errors. Coupling filter circuits may be classified in three broad categories:

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Fully Settled – This case is characterized by filter time constants and an overall settling time that is considerably shorter than the sample period. When acquisition begins, the coupling filter is disturbed. For a typical first order RC filter, the disturbance will look like an initial step with an exponential decay. The amplifier will have its own response to the disturbance, which may include ringing. If the input settles completely (to within the accuracy of the LTC2508-32), the disturbance will not contribute any error.

Partially Settled – In this case, the beginning of acquisition causes a disturbance of the coupling filter, which then begins to settle out towards the nominal input voltage. However, acquisition ends (and the conversion begins) before the input settles to its final value. This generally produces a gain error, but as long as the settling is linear, no distortion is produced. The coupling filter's response is affected by the amplifier's output impedance and other parameters. A linear settling response to fast switched-capacitor current spikes can NOT always be assumed for precision, low bandwidth amplifiers. The coupling filter serves to attenuate the current spikes' high-frequency energy before it reaches the amplifier.

Fully Averaged – If the coupling filter capacitors (C_{FILT}) at the ADC inputs are much larger than the ADC's sample capacitors (45pF), then the sampling glitch is greatly attenuated. The driving amplifier effectively only sees the average sampling current, which is quite small. At 1Msps, the equivalent input resistance is approximately 22kΩ (as shown in Figure 5), a benign resistive load for most precision amplifiers. However, resistive voltage division will occur between the coupling filter's DC resistance and the ADC's equivalent (switched-capacitor) input resistance, thus producing a gain error.

The input leakage currents of the LTC2508-32 should also be considered when designing the input drive circuit, because source impedances will convert input leakage currents to an added input voltage error. The input leakage currents, both common mode and differential, are typically extremely small over the entire operating temperature range. Figure 6 shows the input leakage currents over temperature for a typical part.

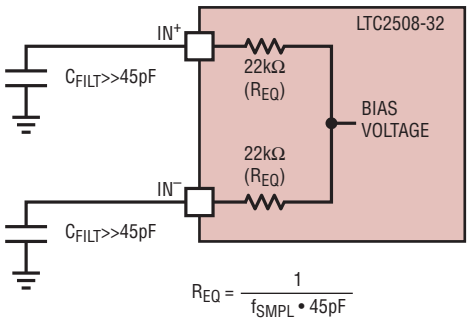

Figure 5. Equivalent Circuit for the Differential Analog Input of the LTC2508-32 at 1Msps

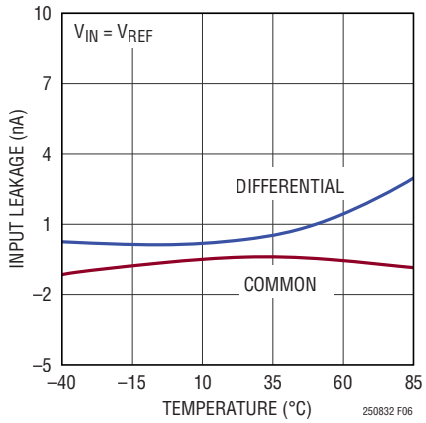

Figure 6. Common Mode and Differential Input Leakage Current Over Temperature

Let R_{S1} and R_{S2} be the source impedances of the differential input drive circuit shown in Figure 7, and let I_{L1} and I_{L2} be the leakage currents flowing out of the ADC's analog inputs. The differential voltage error, V_E, due to the leakage currents can be expressed as:

$$V_E = \frac{R_{S1}+R_{S2}}{2} \bullet (I_{L1}-I_{L2}) + (R_{S1}-R_{S2}) \bullet \frac{I_{L1}+I_{L2}}{2}$$

The common mode input leakage current, $(I_{L1} + I_{L2})/2$, is typically extremely small (Figure 6) over the entire operating temperature range and common mode input voltage range. Thus, any reasonable mismatch (below 5%) of the source impedances R_{S1} and R_{S2} will cause only a negligible error. The differential leakage current is also typically very small, and its nonlinear component is even smaller. Only the nonlinear component will impact the ADC's linearity.

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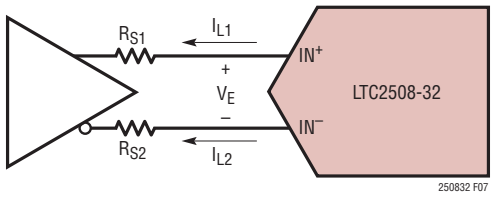

Figure 7. Source Impedances of a Driver and Input Leakage Currents of the LTC2508-32

For optimal performance, it is recommended that the source impedances, R_{S1} and R_{S2}, be between 5Ω and 50Ω and with 1% tolerance. For source impedances in this range, the voltage and temperature coefficients of R_{S1} and R_{S2} are usually not critical. The guaranteed AC and DC specifications are tested with 5Ω source impedances, and the specifications will gradually degrade with increased source impedances due to incomplete settling.

DC Accuracy

The LTC2508-32 has excellent INL specifications. This makes the LTC2508-32 ideal for applications which require high DC accuracy, including parameters such as offset and offset drift. To maintain high accuracy over the entire DC signal chain, amplifiers have to be selected very carefully. A large-signal open-loop gain of at least 126dB may be required to ensure 1ppm linearity for amplifiers configured for a gain of negative 1. However, less gain is sufficient if the amplifier's gain characteristic is known to be (mostly) linear. An amplifier's offset versus signal level must be considered for amplifiers configured as unity gain buffers. For example, 1ppm linearity may require that the offset is known to vary less than 5µV for a 5V swing. However, greater offset variations may be acceptable if the relationship is known to be (mostly) linear. Unity-gain buffer amplifiers typically require substantial headroom to the power supply rails for best performance. Inverting amplifier circuits configured to minimize swing at the amplifier input terminals may perform better with less headroom than unity-gain buffer amplifiers. The linearity and thermal properties of an inverting amplifier's feedback network should be considered carefully to ensure DC accuracy.

Buffering Input Signals

The wide common mode input range and high CMRR of the LTC2508-32 allow analog inputs IN^+ and $IN^–$ pins to swing with an arbitrary relationship to each other, provided that each pin remains between V_{REF} and GND. This unique feature of the LTC2508-32 enables it to accept a wide variety of signal swings, simplifying signal chain design.

Buffering DC Accurate Input Signals

Figure 8 shows a typical application where two analog input voltages are buffered using the LTC2057. The LTC2057 is a high precision zero drift amplifier which complements the low offset and offset drift of the LTC2508-32. The LTC2057 is shown in a non-inverting amplifier configura-

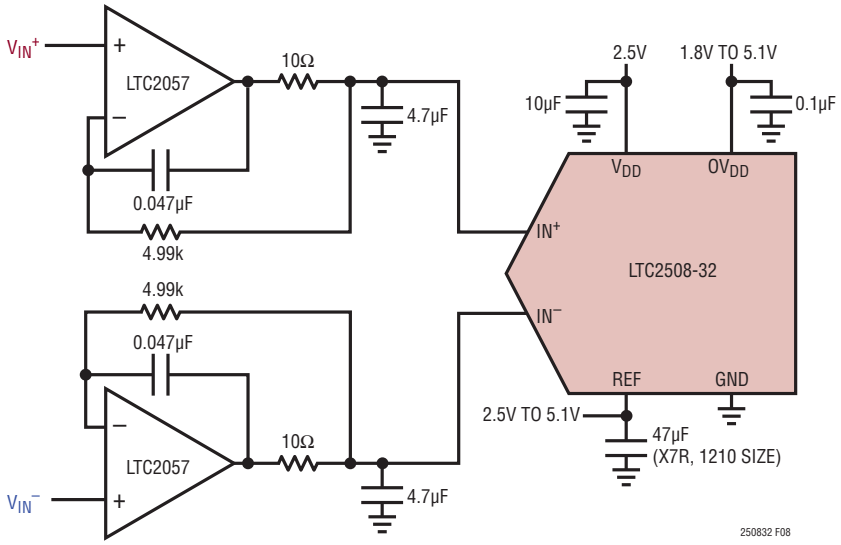

Figure 8. Buffering Two Analog Input Signals

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tion. The LTC2508-32 has a guaranteed maximum offset error of 130µV (typical drift ±0.014ppm/°C), and a guaranteed maximum full-scale error of 150ppm (typical drift ±0.05ppm/°C). Low drift is important to maintain accuracy over a wide temperature range in a calibrated system.

Buffering DC Accurate Single-Ended Input Signals

While the circuit shown in Figure 8 is capable of buffering single-ended input signals, the circuit shown in Figure 9 is preferable when the single-ended signal reference level is inherently low impedance and doesn't require buffering. This circuit eliminates one driver and one lowpass filter, reducing part count, power dissipation, and SNR degradation due to driver noise.

The LTC2057 has excellent DC characteristics, but limited output current drive, leading to a degradation in THD as the input frequency increases. Limit the input frequency to 10Hz to maintain full data sheet specified THD.

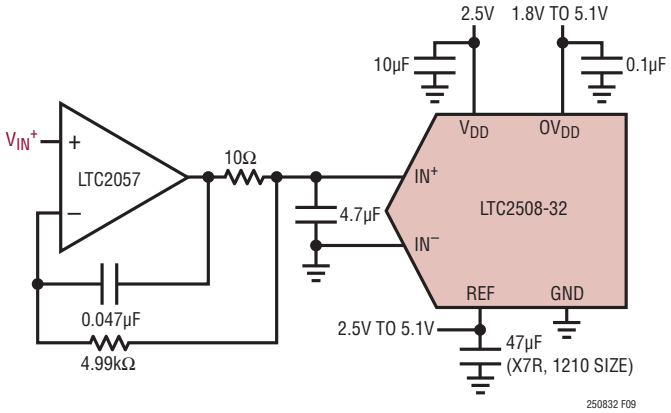

Figure 9. Buffering Single-Ended Signals

Buffering AC Input Signals

Many driver circuits presented in this data sheet emphasize performance for low bandwidth input signals, and the amplifiers are chosen accordingly. While the LTC2057 is characterized by excellent DC specifications, its output current drive is limited. This limits the range of input frequencies that the LTC2057 can drive to the full data sheet specifications of the LTC2508-32. The –3dB bandwidth of the filtered output of the LTC2508-32, while operating with a DF of 256, is equal to 480Hz. Therefore, an alternative driver solution is required while driving input signals with bandwidth greater than 10Hz.

The LTC6363 is a low power, low noise, fully differential op amp, and can be used to drive input signals with bandwidth greater than 10Hz. The LTC6363 may be configured to convert a single-ended input signal to a differential output signal or may be driven differentially.

Figure 10a shows the LTC6363 being used to buffer a 10V differential input signal. In this case, the amplifier is configured as a unity gain buffer using the LT5400-4 precision resistors. As shown in the FFT of Figure 10b, the LTC6363 drives the LTC2508-32 to near full data sheet performance.

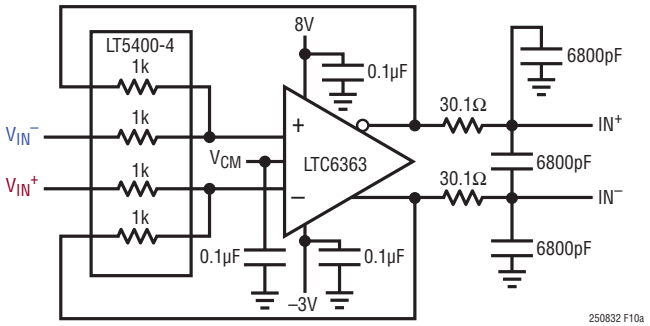

Figure 10a. Buffering AC Inputs

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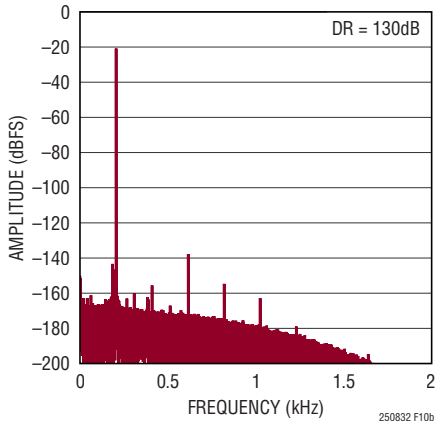

Figure 10b. 128k Point FFT with f_{IN} = 200Hz for Circuit Shown in Figure 10a

ADC REFERENCE

An external reference defines the input range of the LTC2508-32. A low noise, low temperature drift reference is critical to achieving the full data sheet performance of the ADC. Linear Technology offers a portfolio of high performance references designed to meet the needs of many applications. With its small size, low power and high accuracy, the LTC6655-5 is particularly well suited for use with the LTC2508-32. The LTC6655-5 offers 0.025% (max) initial accuracy and 2ppm/°C (max) temperature coefficient for high precision applications.

When choosing a bypass capacitor for the LTC6655-5, the capacitor's voltage rating, temperature rating, and package size should be carefully considered. Physically larger capacitors with higher voltage and temperature ratings tend to provide a larger effective capacitance, better filtering the noise of the LTC6655-5, and consequently facilitating a higher SNR. Therefore, we recommend bypassing the LTC6655-5 with a 47µF ceramic capacitor (X7R, 1210 size, 10V rating) close to the REF pin.

The REF pin of the LTC2508-32 draws charge (Q_{CONV}) from the 47µF bypass capacitor during each conversion cycle. The reference replenishes this charge with an average current, $I_{REF} = Q_{CONV}/t_{CYC}$. The current drawn from the REF pin, I_{REF}, depends on the sampling rate and output code. If the LTC2508-32 continuously samples a signal at a constant rate, the LTC6655-5 will keep the deviation of the reference voltage over the entire code span to less than 0.5ppm.

When idling, the REF pin on the LTC2508-32 draws only a small leakage current (< 1µA). In applications where a burst of samples is taken after idling for long periods as shown in Figure 11, I_{REF} quickly goes from approximately 0µA to a maximum of 1mA at 1Msps. This step in average current drawn causes a transient response in the reference that must be considered, since any deviation in the reference output voltage will affect the accuracy of the output code. In applications where the transient response of the reference is important, the fast settling LTC6655-5 reference is also recommended.

Reference Noise

The dynamic range of the ADC will increase approximately 6dB for every 4× increase in the down-sampling factor (DF). The SNR should also improve as a function of DF in the same manner. For large input signals near full-scale, however, any reference noise will limit the improvement of the SNR as DF increases, because any noise on the REF pin will modulate around the fundamental frequency of the input signal. Therefore, it is critical to use a low-noise reference, especially if the input signal amplitude approaches full-scale. For small input signals, the dynamic range will improve as described earlier in this section.

DYNAMIC PERFORMANCE

Fast Fourier Transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm,

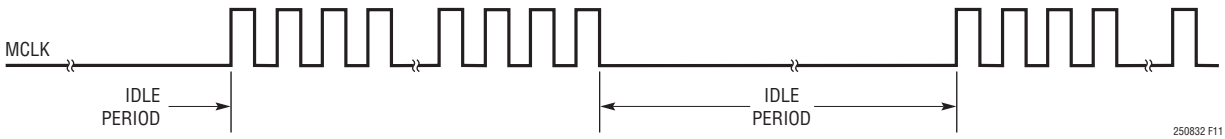

Figure 11. MCLK Waveform Showing Burst Sampling

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the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2508-32 provides guaranteed tested limits for both AC distortion and noise measurements.

Dynamic Range

The dynamic range is the ratio of the RMS value of a full scale input to the total RMS noise measured with the inputs shorted to $V_{REF}/2$. The dynamic range of the LTC2508-32 with DF = 256 is 131dB which improves with increase in the down-sampling factor.

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band-limited to frequencies from above DC and below half the sampling frequency. Figure 12 shows that the LTC2508-32 achieves a typical SINAD of 120dB at a 1MHz sampling rate with a 200Hz input, and DF = 256.

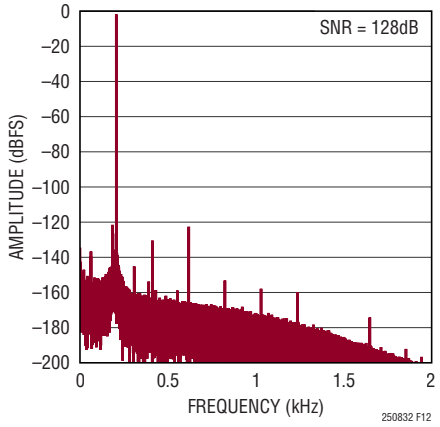

Figure 12. 128k Point FFT Plot of LTC2508-32 with DF = 256, f_{IN} = 200Hz and f_{SMPL} = 1MHz

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 12 shows that the LTC2508-32 achieves an SNR of 128dB when sampling a 200Hz input at a 1MHz sampling rate with DF = 256.

Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20LOG\frac{\sqrt{V2^2 + V3^2 + V4^2 + \cdots + VN^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through VN are the amplitudes of the second through Nth harmonics.

POWER CONSIDERATIONS

The LTC2508-32 has two power supply pins: the 2.5V power supply (V_{DD}), and the digital input/output interface power supply (OV_{DD}). The flexible OV_{DD} supply allows the LTC2508-32 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

Power Supply Sequencing

The LTC2508-32 does not have any specific power supply sequencing requirements. Care should be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2508-32 has a power-on-reset (POR) circuit that will reset the LTC2508-32 at initial power-up or whenever the power supply voltage drops below 1V. Once the supply voltage re-enters the nominal supply voltage range, the POR will reinitialize the ADC. No conversions should be initiated until 200µs after a POR event to ensure the reinitialization period has ended. Any conversions initiated before this time will produce invalid results.

TIMING AND CONTROL

MCLK Timing

A rising edge on MCLK will power up the LTC2508-32 and start a conversion. Once a conversion has been started, further transitions on MCLK are ignored until the conversion is complete. For best results, the falling edge

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of MCLK should occur within 40ns from the start of the conversion, or after the conversion has been completed. For optimum performance, MCLK should be driven by a clean low jitter signal. Converter status is indicated by the BUSY output which remains high while the conversion is in progress. Once the conversion has completed, the LTC2508-32 powers down and begins acquiring the input signal for the next conversion.

Internal Conversion Clock

The LTC2508-32 has internal timing circuity that is trimmed to achieve a maximum conversion time of 652ns. With a maximum sample rate of 1Msps, a minimum acquisition time of 335ns is guaranteed without any external adjustments.

Auto Power Down

The LTC2508-32 automatically powers down after a conversion has been completed and powers up once a new conversion is initiated on the rising edge of MCLK. During power-down, data from the last conversion can be clocked out. To minimize power dissipation during power-down, disable SDOA, SDOB and turn off SCKA, SCKB. The auto power-down feature will reduce the power dissipation of the LTC2508-32 as the sampling rate is reduced. Since power is consumed only during a conversion, the LTC2508-32 remains powered down for a larger fraction of the conversion cycle (t_{CYC}) at lower sample rates, thereby reducing the average power dissipation which scales with the sampling rate as shown in Figure 13.

DECIMATION FILTERS

Many ADC applications use digital filtering techniques to reduce noise. An FPGA or DSP is typically needed to implement a digital filter. The LTC2508-32 features an integrated decimation filter that provides 4 selectable digital filtering functions without any external hardware, thus simplifying the application solution. Figure 14 shows the LTC2508-32 digitally filtered output signal path, wherein the output $D_{ADC}(n)$ of the 32-bit SAR ADC core is passed on to the integrated decimation filter.

Digital Filtering

The input to the LTC2508-32 is sampled at a rate f_{SMPL}, and digital words $D_{ADC}(n)$ are transmitted to the digital filter at that rate. Noise from the 32-bit SAR ADC core is distributed uniformly in frequency from DC to $f_{SMPL}/2$. Figure 15 shows the frequency spectrum of $D_{ADC}(n)$ at the output of the SAR ADC core. In this example, the bandwidth of interest f_B is a small fraction of $f_{SMPL}/2$.

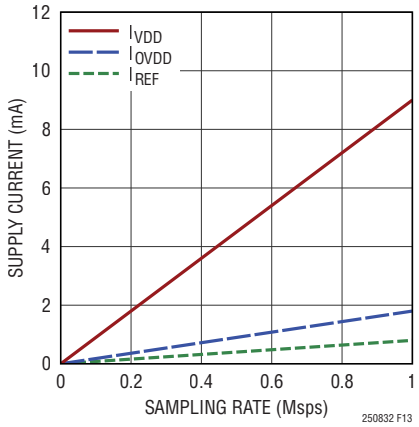

Figure 13. Power Supply Current of the LTC2508-32 vs Sampling Rate

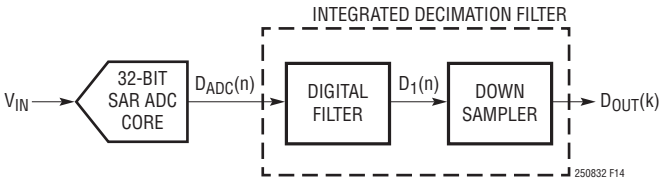

Figure 14. LTC2508-32 Digitally Filtered Output Signal Path

Figure 15. Frequency Spectrum of SAR ADC Core Output

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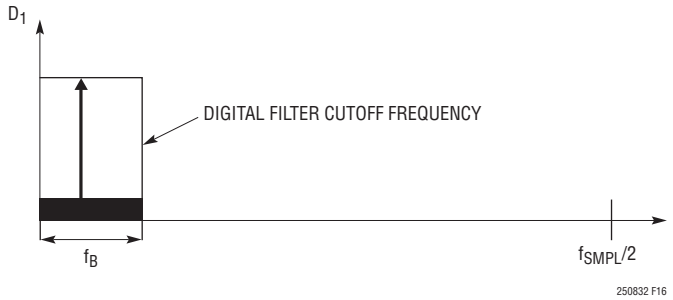

Figure 16. Frequency Spectrum of Digital Filter Core Output

The digital filter integrated in the LTC2508-32 suppresses out-of-band noise power, thereby lowering overall noise and increasing the dynamic range (DR). The lower the filter bandwidth, the lower the noise, and the higher the DR. Figure 16 shows the corresponding frequency spectrum of $D_1(n)$ at the output of the digital filter, where noise beyond the cutoff frequency is suppressed by the digital filter.

Down-Sampling

The output data rate of the digital filter is reduced by a down-sampler without causing spectral interference in the bandwidth of interest.

The down-sampler reduces the data rate by passing every DF^{th} sample to the output, while discarding all other samples. The sampling frequency f_O at the output of the down sampler is the ratio of f_{SMPL} and DF, i.e., $f_O = f_{SMPL}/DF$.

The LTC2508-32 enables the user to select DF according to a desired bandwidth of interest. The 4 available configurations can be selected by pin strapping pins SEL0 and SEL1. Table 1 summarizes the different decimation filter configurations and properties. When operating at 1.024Msps, the acquisition time (t_{ACQ}) of the LTC2508-32 is reduced to 308.5ns and the output data rate correspondingly increases. Note that the dynamic range is unchanged as it is only affected by DF and not by sampling rate.

Aliasing

The maximum bandwidth that a signal being sampled can have and be accurately represented by its samples is the Nyquist bandwidth. The Nyquist bandwidth ranges from DC to half the sampling frequency (a.k.a. the Nyquist frequency). An input signal whose bandwidth exceeds the Nyquist frequency, when sampled, will experience distortion due to an effect called "Aliasing".

When aliasing, frequency components greater than the Nyquist frequency undergo a frequency shift and appear within the Nyquist bandwidth. Figure 17 illustrates aliasing in the time domain. The solid line shows a sinusoidal input signal of a frequency greater than the Nyquist frequency ($f_O/2$). The circles show the signal sampled at f_O. Note that the sampled signal is identical to that of sampling another sinusoidal input signal of a lower frequency shown with the dashed line. To avoid aliasing, it is necessary to band-limit an input signal to the Nyquist bandwidth before sampling it. A filter that suppresses spectral components outside the Nyquist bandwidth is called an "Anti-Aliasing Filter"(AAF).

Anti-Aliasing Filters

Figure 18 shows a typical signal chain including a lowpass AAF and an ADC sampling at a rate of f_O. The AAF rejects input signal components exceeding $f_O/2$, thus avoiding aliasing. If the bandwidth of interest is close to $f_O/2$, then

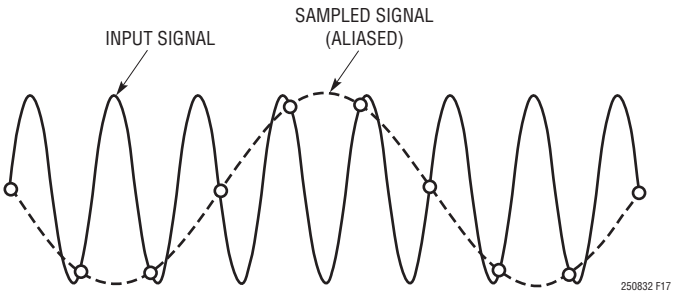

Figure 17. Time Domain View of Aliasing

Table 1. Properties of Filters in LTC2508-32

SEL1:SEL0	DOWN SAMPLING FACTOR (DF)	–3dB BANDWIDTH		OUTPUT DATA RATE (ODR)		DYNAMIC RANGE
		f_{SMPL} = 1Msps	f_{SMPL} = 1.024Msps	f_{SMPL} = 1Msps	f_{SMPL} = 1.024Msps	
00	256	480Hz	491.5Hz	3906sps	4000sps	131dB
01	1024	120Hz	122.8Hz	977sps	1000sps	136dB
10	4096	30Hz	30.7Hz	244sps	250sps	141dB
11	16384	7.5Hz	7.7Hz	61sps	62.5sps	145dB

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the AAF must have a very steep roll-off. The complexity of the analog AAF increases with the steepness of the roll-off, and it may be prohibitive if a very steep filter is required.

Alternatively, a simple low-order analog filter in combination with a digital filter can be used to create a mixed-mode equivalent AAF with a very steep roll-off. A mixed-mode filter implementation is shown in Figure 19 where an analog filter with a gradual roll-off is followed by the LTC2508-32 sampling at a rate of $f_{SMPL} = DF \bullet f_O$. The LTC2508-32 has an integrated digital filter at the output of the ADC core. The equivalent AAF, $H_{EQ}(f)$, is the product of the frequency responses of the analog filter $H_1(f)$ and digital filter $H_2(f)$, as shown in Figure 20. The digital filter provides a steep roll-off, allowing the analog filter to have a relatively gradual roll-off.

The digital filter in the LTC2508-32 operates at the ADC sampling rate f_{SMPL} and suppresses signals at frequencies exceeding $f_O/2$. The frequency response of the digital filter $H_2(f)$ repeats at multiples of f_{SMPL}, resulting in unwanted passbands at each multiple of f_{SMPL}. The analog filter should be designed to provide adequate suppression of the unwanted passbands, such that $H_{EQ}(f)$ has only one passband corresponding to the frequency range of interest. Larger DF settings correspond to less bandwidth of the digital filter, allowing for the analog filter to have a more gradual roll-off. A simple first- or second-order analog filter will provide adequate suppression for most systems.

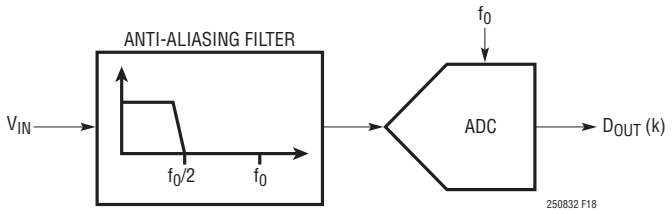

Figure 18. ADC Signal Chain with AAF

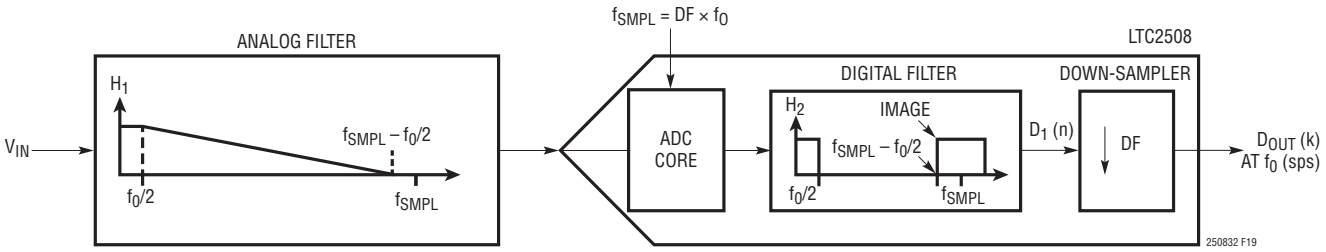

Figure 19. Mixed-Mode Filter Signal Chain

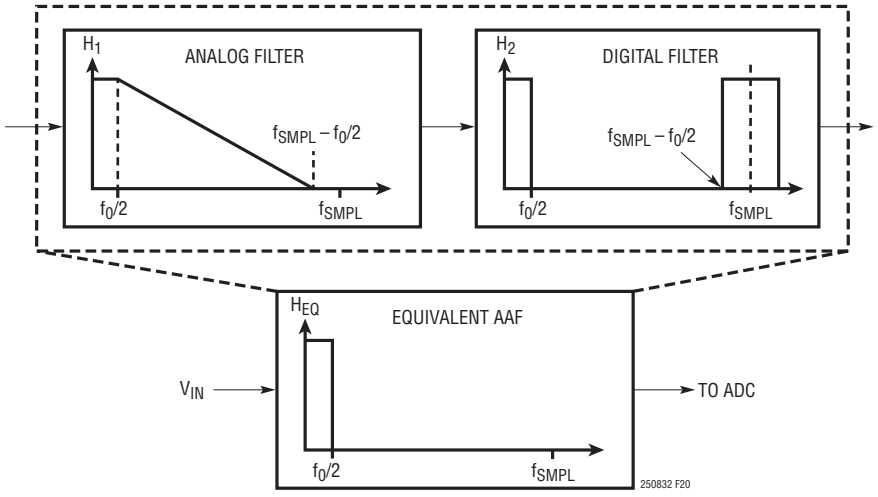

Figure 20. Mixed-Mode Anti-Aliasing Filter (AAF)

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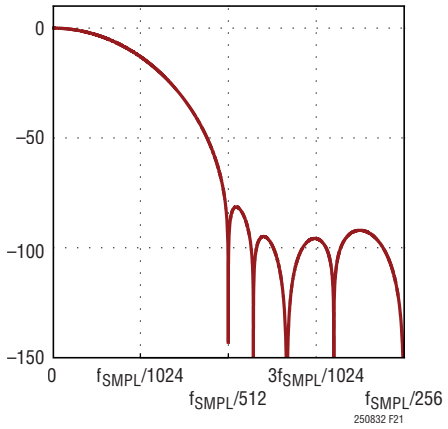

Figure 21. Frequency Response of Digital Filter with DF = 256

Frequency Response of Digital Filters

Figure 21 shows the frequency response of the digital filter when the LTC2508-32 is configured to operate with DF = 256 and sampling at f_{SMPL}.

For each configuration of the LTC2508-32, the digital filter is a lowpass finite impulse response (FIR) filter with linear phase response. The bandwidth is inversely proportional to the selected DF value. Each configuration provides a minimum of 80dB attenuation for frequencies in the range of $f_O/2$ and $f_{SMPL} – f_O/2$. The filter coefficients and detailed version of the frequency response of the 4 digital filter configurations are available at www.linear.com/docs/52896. Table 2 lists the length and group delay of each digital filter's impulse response.

Table 2. Length of Digital Filter

DOWN-SAMPLING FACTOR (DF)	LENGTH OF DIGITAL FILTER IMPULSE RESPONSE	GROUP DELAY (f_{SMPL} = 1Msps)
256	2,304	1.2ms
1,024	9,216	4.6ms
4,096	36,864	18.4ms
16,384	147,456	73.7ms

Settling Time and Group Delay

The length of each digital filter's impulse response determines its settling time. Linear phase filters exhibit constant delay time versus input frequency (that is, constant group delay). Group delay of the digital filter is defined to be the delay to the center of the impulse response.

LTC2508-32 is optimized for low latency, and it provides fast settling. Figure 22 shows the output settling behavior after a step change on the analog inputs of the LTC2508-32. The X axis is given in units of output sample number. The step response is representative for all values of DF. Full settling is achieved in 10 output samples.

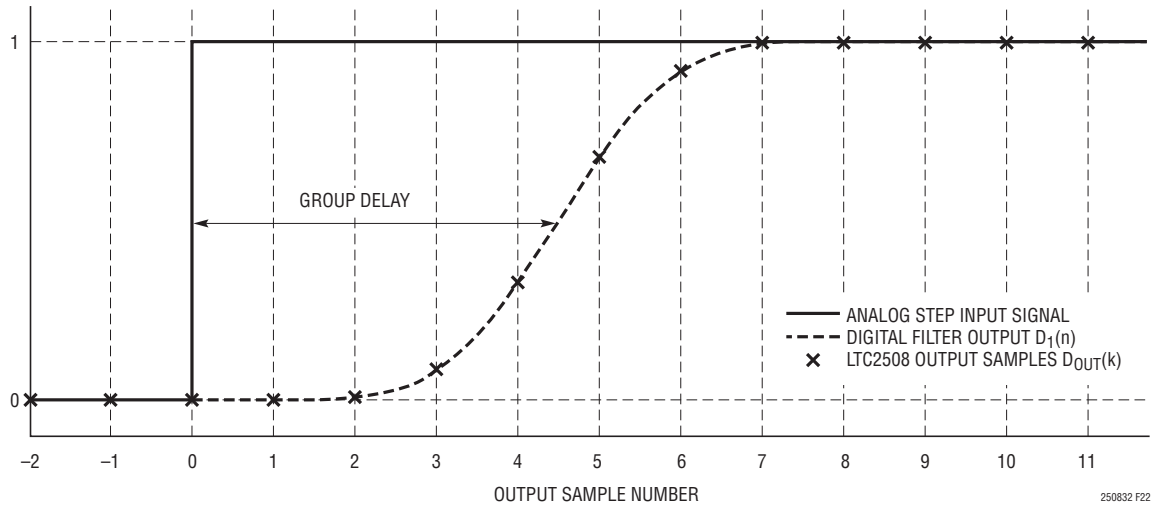

Figure 22. Step Response of LTC2508-32

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DIGITAL INTERFACE

The LTC2508-32 features two digital serial interfaces. Serial interface A is used to read the filtered output data. Serial interface B is used to read the no latency output data. Both interfaces support a flexible OV_{DD} supply, allowing the LTC2508-32 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

Filtered Output Data

Figure 23 shows a typical operation for reading the filtered output data. The I/O register contains filtered output codes $D_{OUT}(k)$ provided by the decimation filter. $D_{OUT}(k)$ is updated once in every DF number of conversion cycles. A timing signal DRL indicates when $D_{OUT}(k)$ is updated. DRL goes high at the beginning of every DF^{th} conversion, and it goes low when the conversion completes. The 32-bits of $D_{OUT}(k)$ can be read out before the beginning of the next A/D conversion.

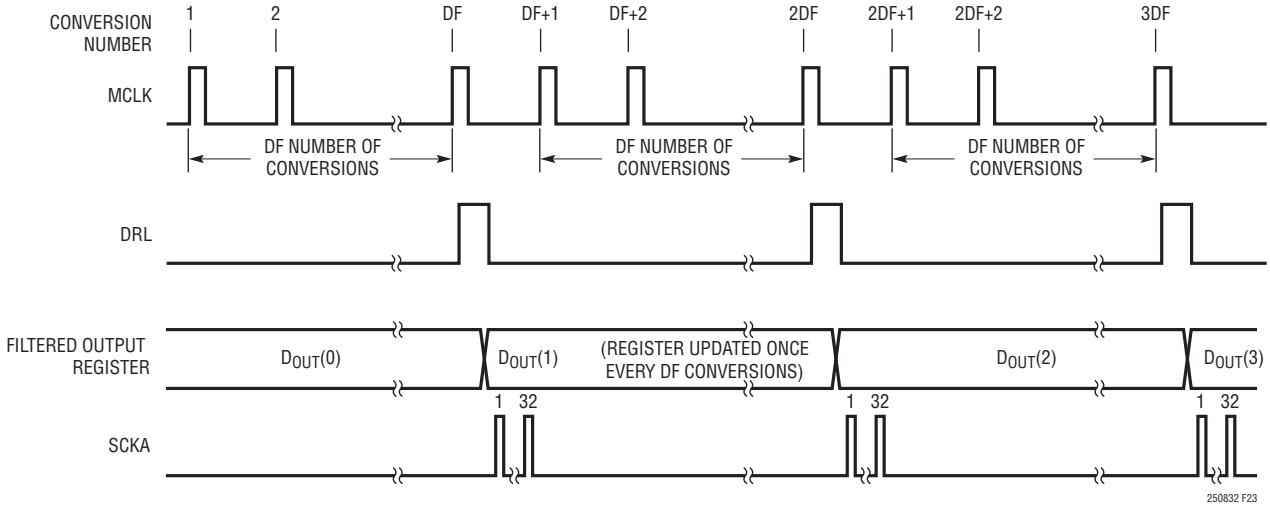

Figure 23. Typical Filtered Output Data Operation Timing

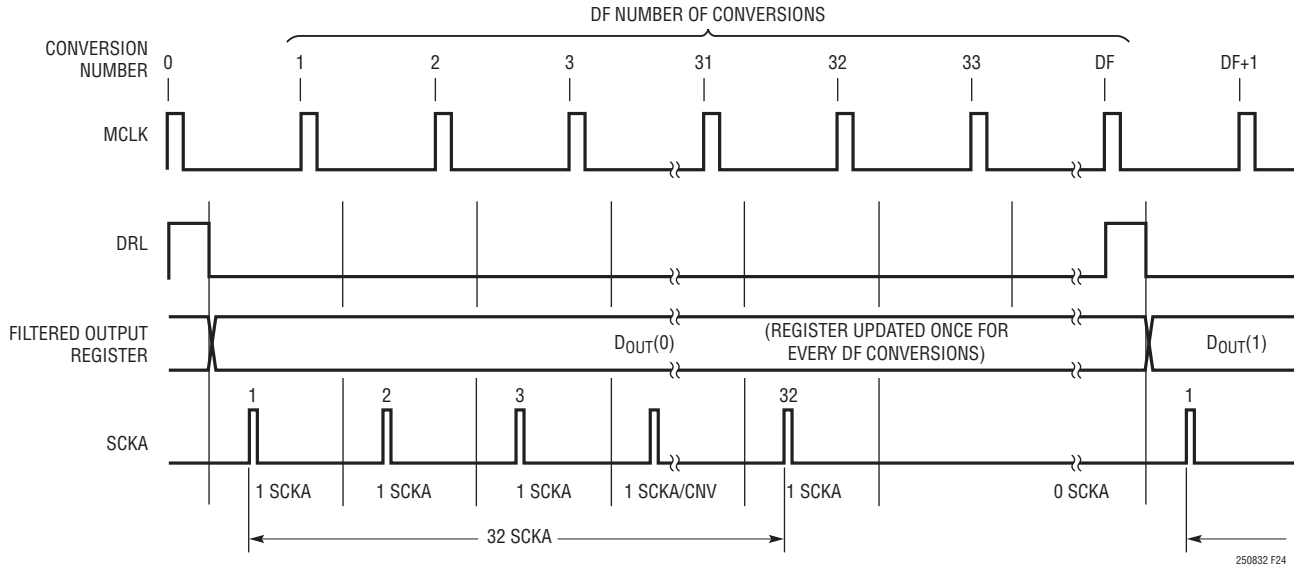

Figure 24. Reading Out Filtered Output Data with Distributed Read

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Distributed Read

LTC2508-32 enables the user to read out the contents of the I/O register over multiple conversions. Figure 24 shows a case where one bit of $D_{OUT}(k)$ is read for each of 32 consecutive A/D conversions, enabling the use of a much slower serial clock (SCKA). Transitions on the digital interface should be avoided during A/D conversion operations (when BUSY is high).

Synchronization

The output of the digital filter $D_1(n)$ is updated every conversion, whereas the down-sampler output $D_{OUT}(k)$ is updated only once every DF number of conversions. Synchronization is the process of selecting when the output $D_{OUT}(k)$ is updated.

This is done by applying a pulse on the SYNC pin of the LTC2508-32. The I/O register for $D_{OUT}(k)$ is updated at each multiple of DF number of conversions after a SYNC pulse is provided, as shown in Figure 25. A timing signal DRL indicates when $D_{OUT}(k)$ is updated.

The SYNC function allows multiple LTC2508 devices, operated from the same master clock that use common SYNC signal, to be synchronized with each other. This allows each LTC2508 device to update its output register at the same time. Note that all devices being synchronized must operate with the same DF.

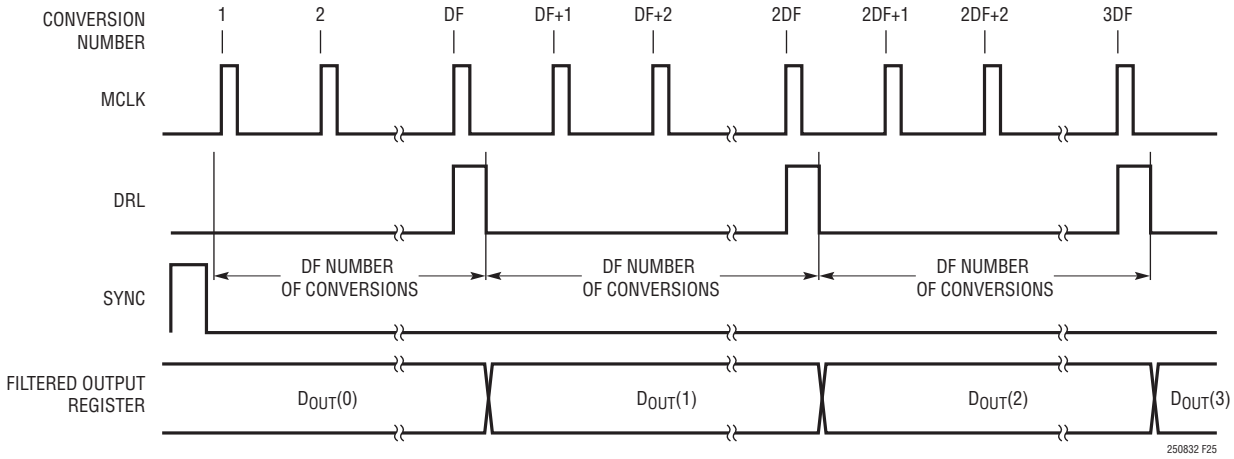

Figure 25. Synchronization Using a Single SYNC Pulse

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Periodic Synchronization

SYNC pulses that reinforce an existing synchronization do not interfere with normal operation. Figure 26 shows a case where a SYNC pulse is applied for each DF number of conversions to continually reinforce a synchronization. Figure 26 indicates synchronization windows when a SYNC pulse may be applied to reinforce the synchronized operation.

Self-Correcting Synchronization

Figure 27 shows a case where an unexpected glitch on MCLK causes an extra A/D conversion to occur. This extra conversion alters the update instants for $D_{OUT}(k)$. The applied periodic SYNC pulse reestablishes the desired synchronization and self corrects within one conversion cycle. Note that the digital filter is reset when the synchronization is changed (reestablished).

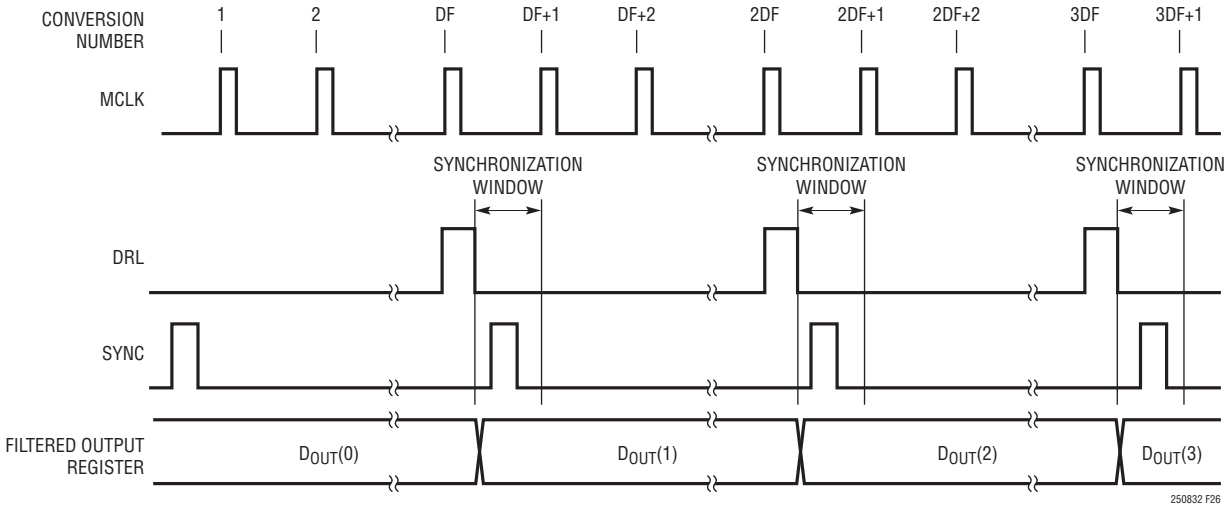

Figure 26. Synchronization Using a Periodic SYNC Pulse

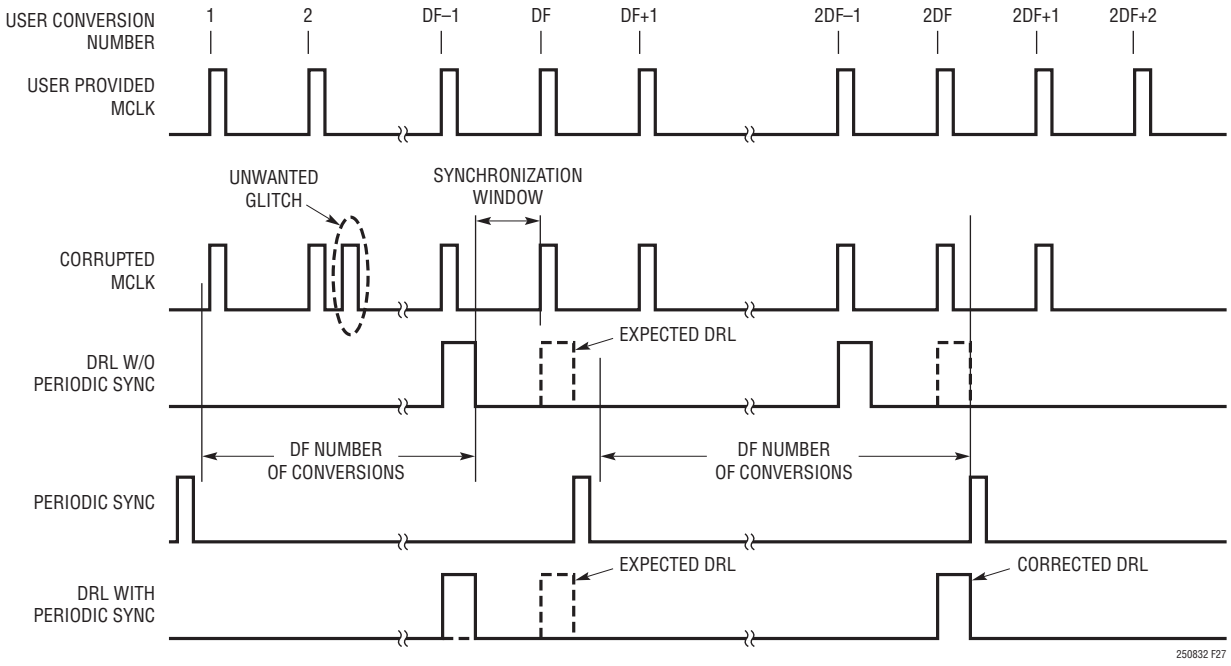

Figure 27. Recovering Synchronization from Unexpected Glitch

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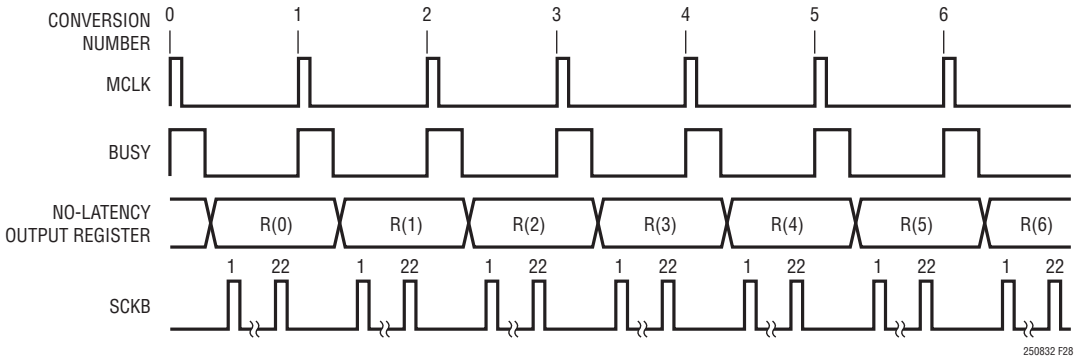

Figure 28. Typical Nyquist Output Data Operation Timing

No Latency Output Data

Figure 28 shows a typical operation for reading the no latency output data. The no latency I/O register holds a 22-bit composite code R(n) from the most recent sample taken of inputs IN^+ and IN^- at the rising edge of MCLK. The first 14 bits of R(n) represent the input voltage difference ($IN^+ – IN^-$), MSB first. The last 8 bits represent the common-mode input voltage ($IN^+ + IN^-$)/2 (in two's complement format), MSB first.

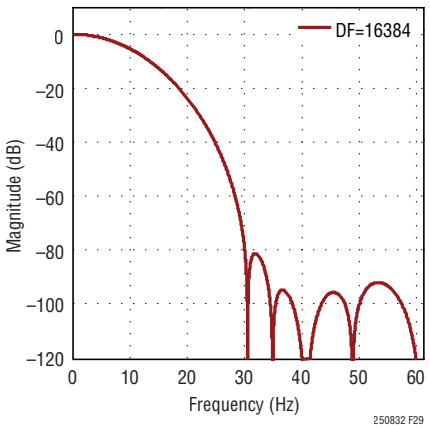

Figure 29. Frequency Response of Digital Filter with DF = 16384

50Hz and 60Hz Rejection

Figure 29 shows the frequency response of the digital filter in the LTC2508-32 configured to operate with DF = 16384, and f_{SMPL} = 1Msps. As shown, at least 100dB simultaneous suppression of 50Hz and 60Hz is obtained. Note that the frequency axis shown in Figure 29 scales with f_{SMPL}.

Configuration Word

An 8-bit configuration word, WA[7:0], is appended to the 32-bit output code on SDOA to produce a total output word of 40 bits as shown in Figure 30. The configuration word designates which downsampling factor (DF) the digital filter is configured to operate with. Clocking out the configuration word is optional. Table 3 lists the configuration words for each DF value.

Table 3. Configuration WORD for Different DF Values

DF	WA[7:0]
256	10000101
1,024	10100101
4,096	11000101
16,384	11100101

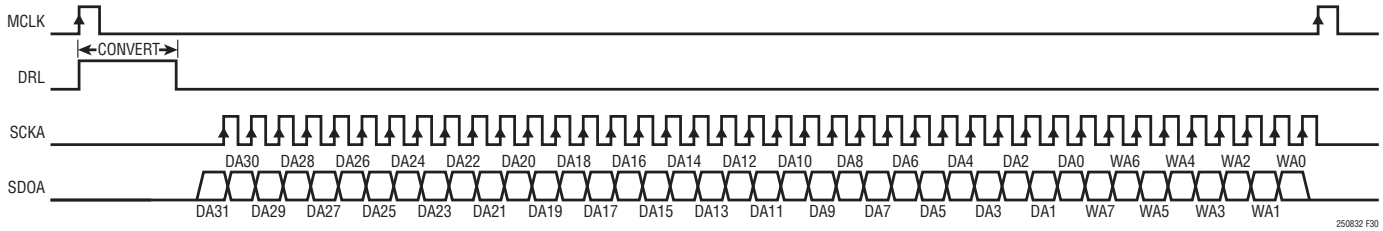

Figure 30. Using LTC2508-3 to Read Filtered Output

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Filtered Output Data, Single Device, DF = 256

Figure 31 shows an LTC2508-32 configured to operate with DF = 256. With RDLA grounded, SDOA is enabled and MSB (DA31) of the output result is available $t_{DSDOADRLL}$ after the falling edge of DRL.

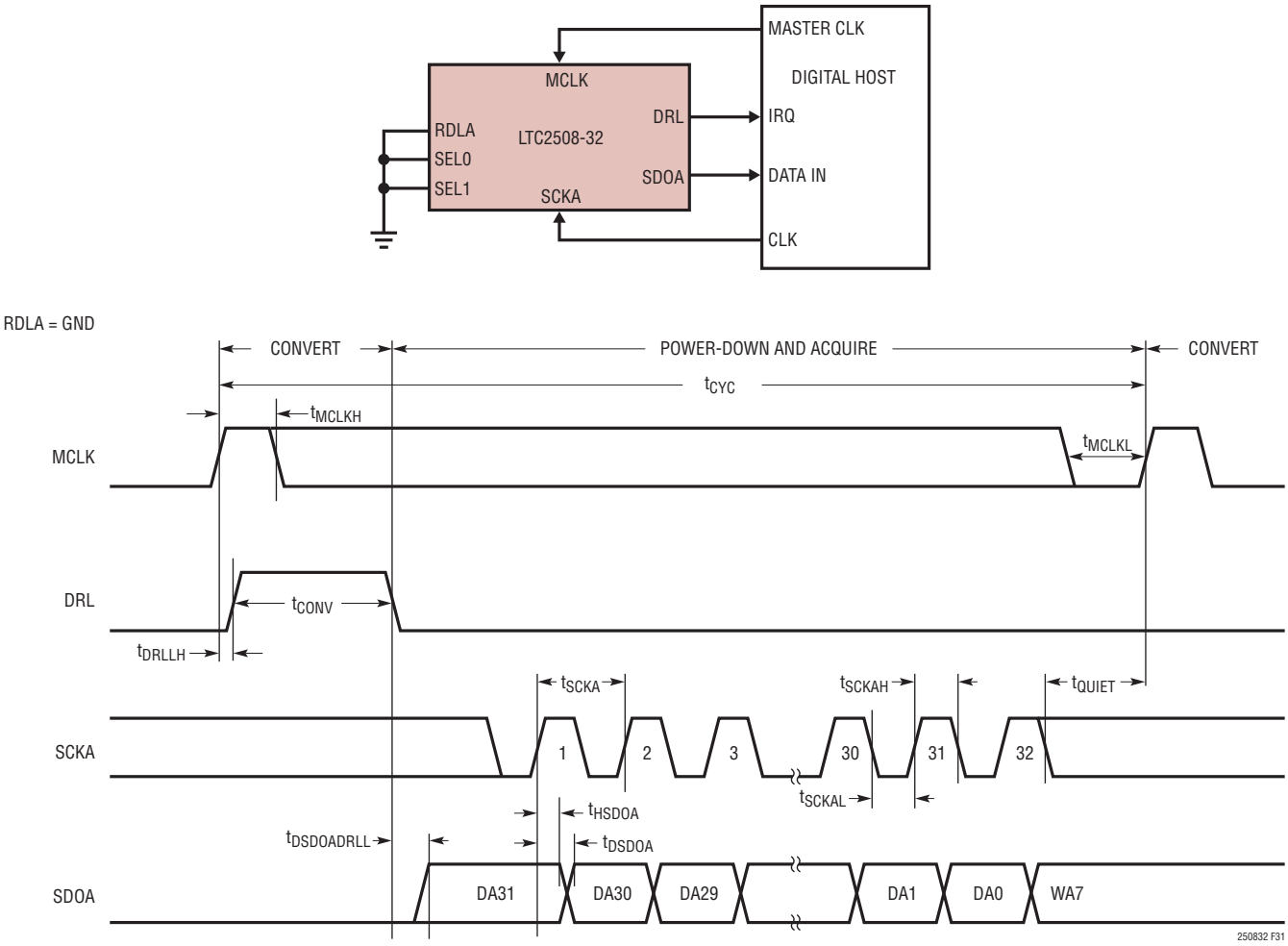

Figure 31. Using a Single LTC2508-32 with DF = 256 to Read Filtered Output

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Filtered Output Data, Multiple Devices, DF = 256

Figure 32 shows two LTC2508-32 devices configured to operate with DF = 256, while sharing MCLK, SYNC, SCKA and SDOA. By sharing MCLK, SYNC, SCKA and SDOA, the number of required signals to operate multiple ADCs in parallel is reduced. Since SDOA is shared, the RDLA input of each ADC must be used to allow only one LTC2508-32 to drive SDOA at a time in order to avoid bus conflicts. As shown in Figure 32, the RDLA inputs idle high and are individually brought low to read data out of each device between conversions. When RDLA is brought low, the MSB of the selected device is output on SDOA.

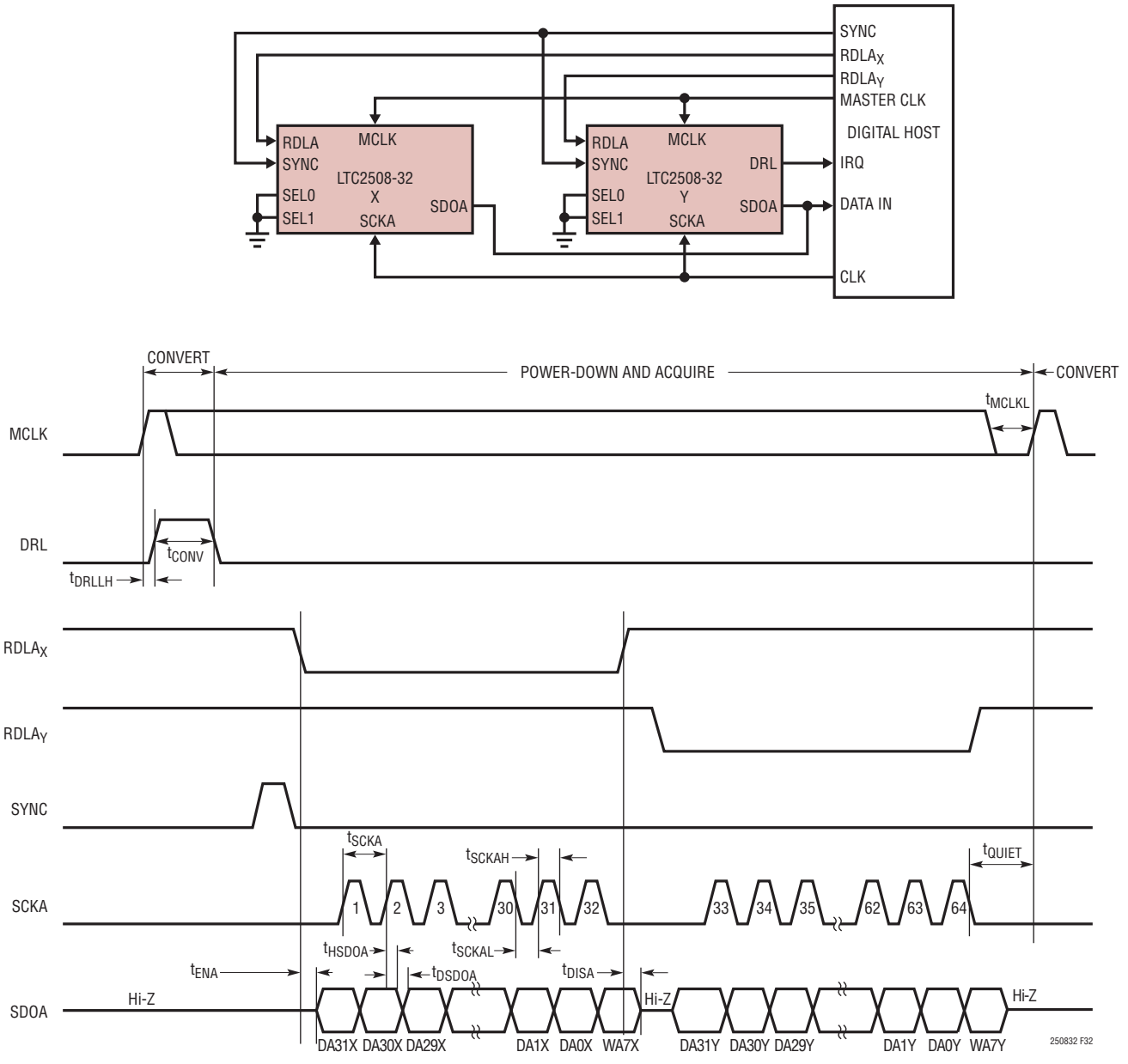

Figure 32. Reading Filtered Output with Multiple Devices Sharing MCLK, SCKA and SDOA

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No Latency Output Data, Single Device

Figure 33 shows a single LTC2508-32 configured to read the no latency data out. With RDLB grounded, SDOB is enabled and MSB (DB13) of the output result is available $t_{DSDOBBUSYL}$ after the falling edge of BUSY.

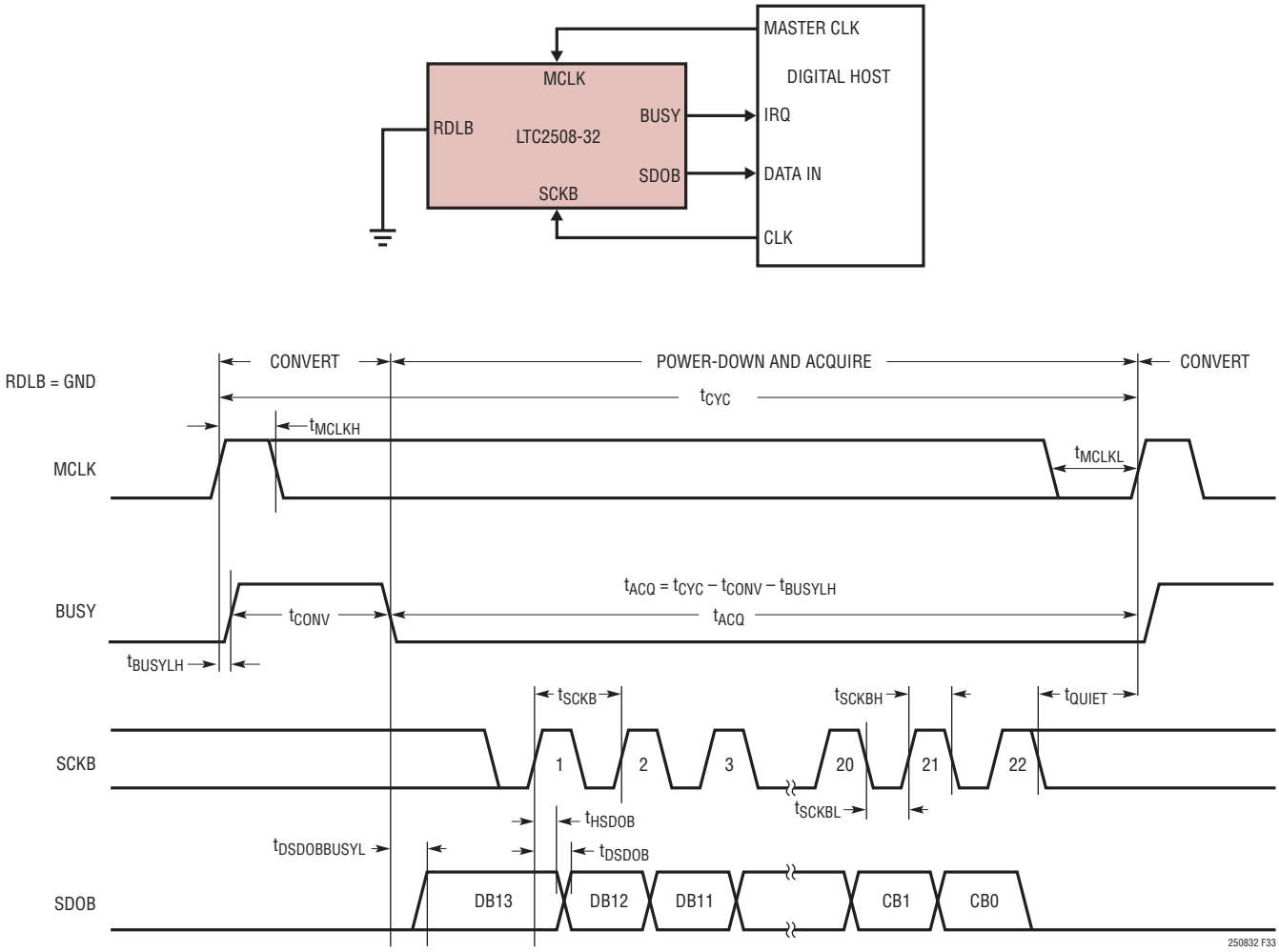

Figure 33. Using a Single LTC2508-32 to Read No Latency Output

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No Latency Output Data, Multiple Devices

Figure 34 shows multiple LTC2508-32 devices configured to read no latency data out, while sharing MCLK, SCKB and SDOB. By sharing MCLK, SCKB and SDOB, the number of required signals to operate multiple ADCs in parallel is reduced. Since SDOB is shared, the RDLB input of each ADC must be used to allow only one LTC2508-32 to drive SDOB at a time in order to avoid bus conflicts. As shown in Figure 34, the RDLB inputs idle high and are individually brought low to read data out of each device between conversions. When RDLB is brought low, the MSB of the selected device is output on SDOB.

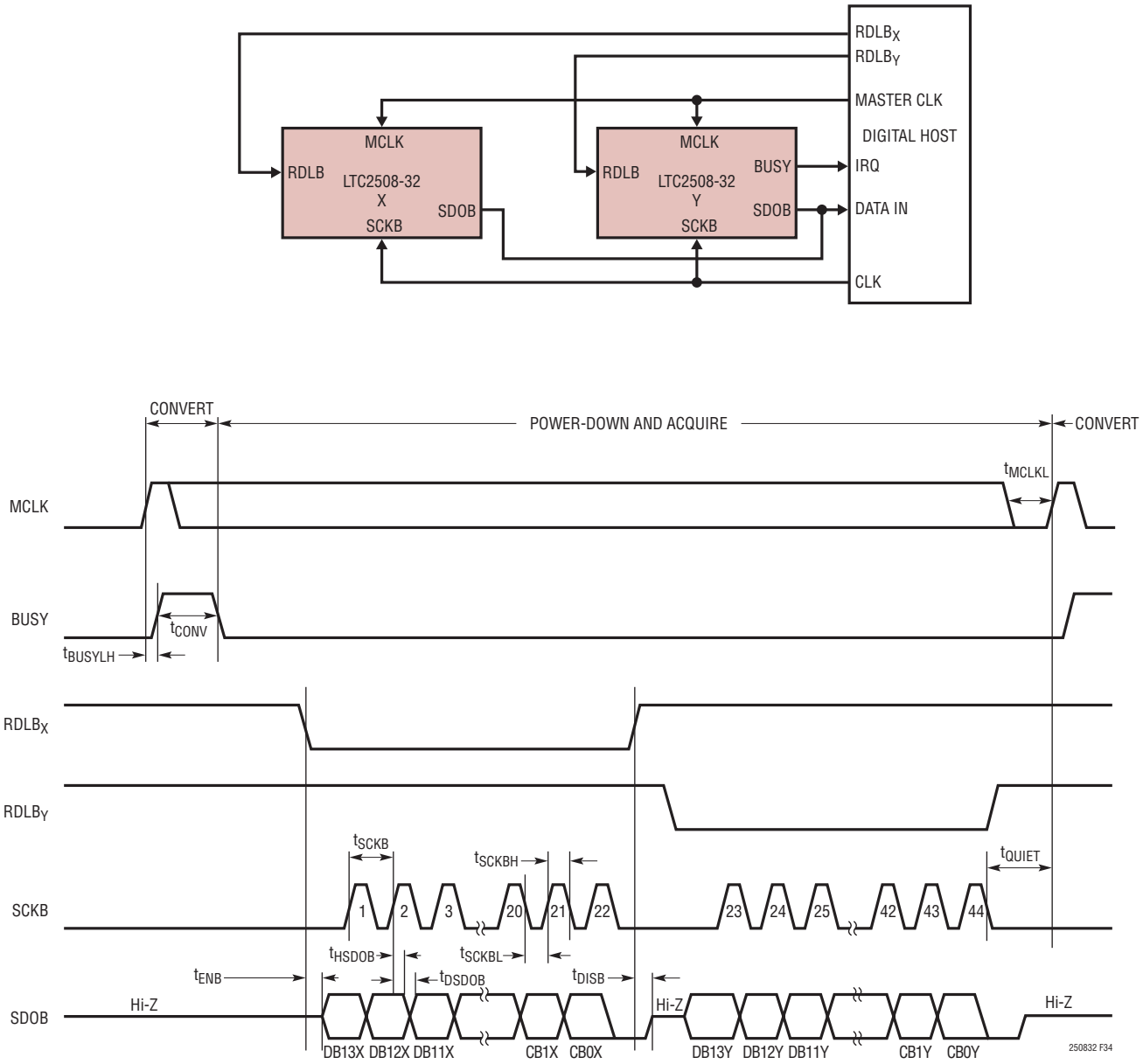


Figure 34. Reading No Latency Output with Multiple Devices Sharing MCLK, SCKB and SDOB

APPLICATIONS INFORMATION

Filtered Output Data, No Latency Data, Single Device

Figure 35 shows a single LTC2508-32 configured to read both filtered and no latency output data, while sharing SDOA with SDOB and SCKA with SCKB. Sharing signals reduces the total number of required signals to read both the filtered and no latency data from the ADC. Since SDOA and SDOB are shared, the RDLA and RDLB inputs of the ADC must be used to allow only one output to drive the shared SDO bus at a time in order to avoid bus conflicts. As shown in Figure 35, the RDLA and RDLB inputs idle high and are individually brought low to read data from each serial output when data is available. When RDLA is brought low, the MSB of the filtered output data from SDOA is output on the shared SDO bus. When RDLB is brought low, the MSB of the no latency data output from SDOB is output on the shared SDO bus.

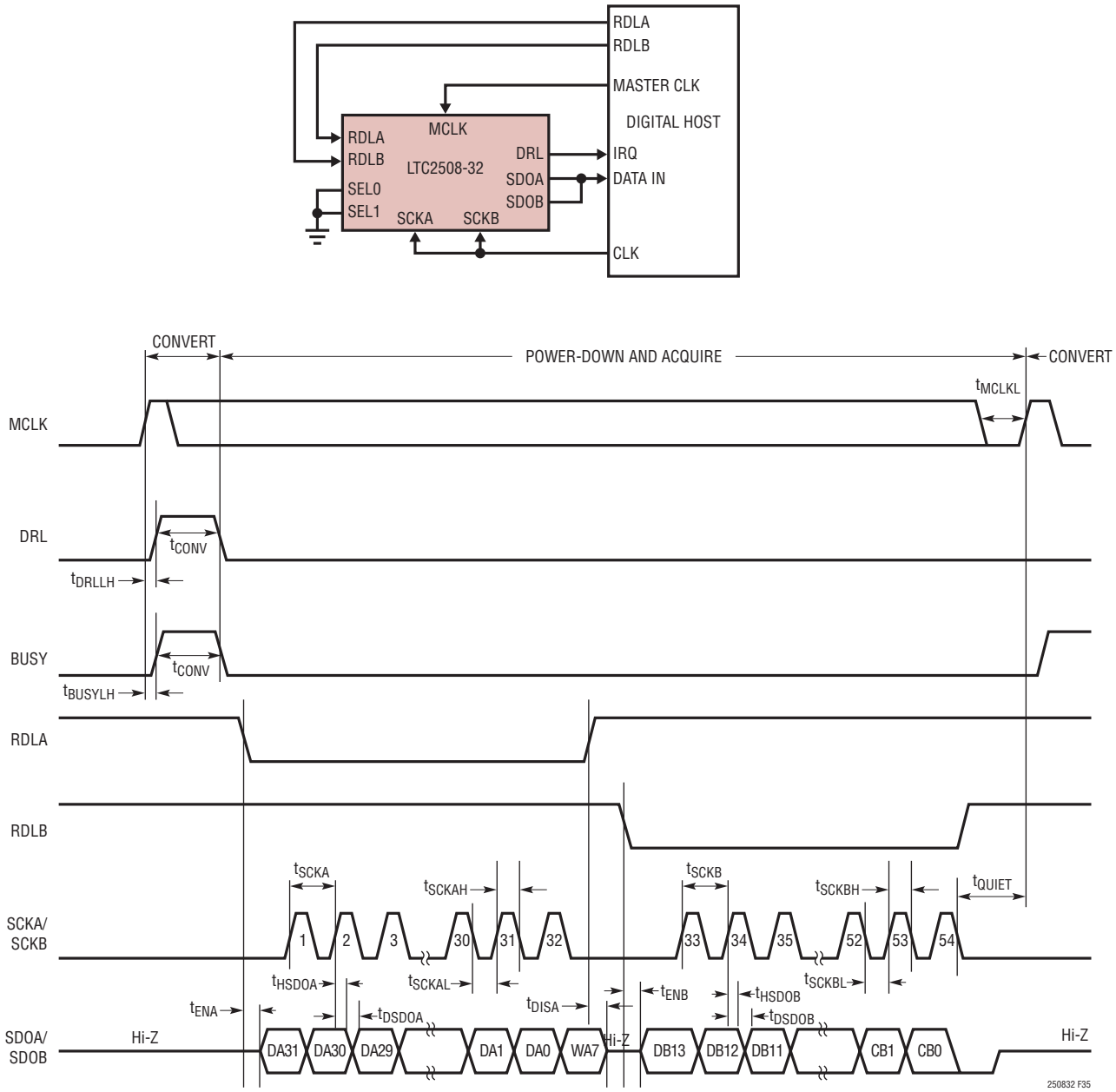


Figure 35. Reading Filtered Output and No Latency Output by Sharing SCK, and SDO

BOARD LAYOUT

To obtain the best performance from the LTC2508-32, a four-layer printed circuit board (PCB) is recommended. Layout for the PCB should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals alongside analog signals or underneath the ADC.

Supply bypass capacitors should be placed as close as possible to the supply pins. Low impedance common returns for these bypass capacitors are essential to the low noise operation of the ADC. A single solid ground plane is recommended for this purpose. When possible, screen the analog input traces using ground.

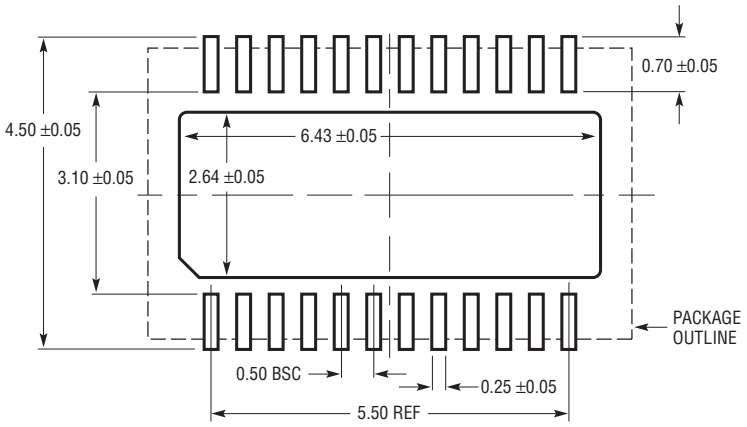
Reference Design

For a detailed look at the reference design for this converter, including schematics and PCB layout, please refer to DC2222, the evaluation kit for the LTC2508-32. DC2222 is designed to achieve the full data sheet performance of the LTC2508-32. Customer board layout should copy DC2222 grounding, and placement of bypass capacitor as closely as possible.

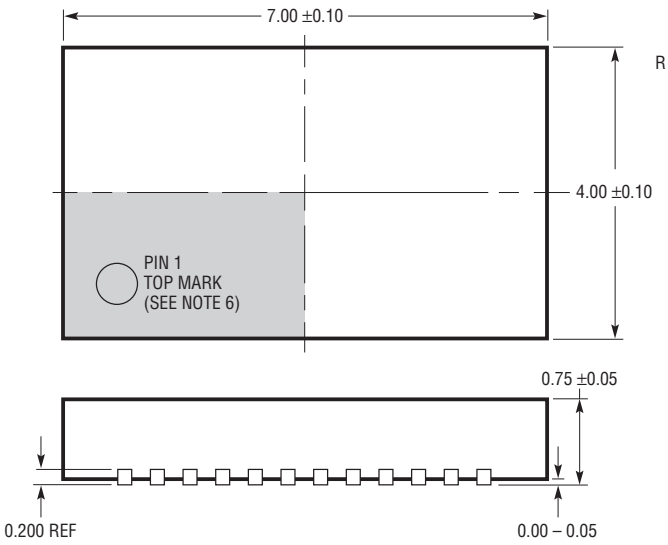
PACKAGE DESCRIPTION

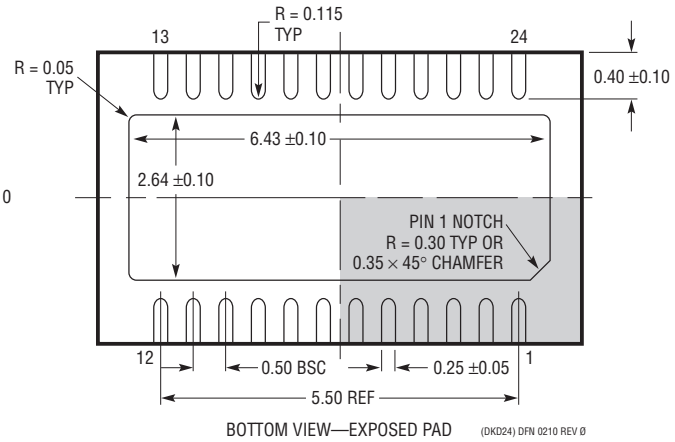
Please refer to http://www.linear.com/product/LTC2508-32#packaging for the most recent package drawings.

DKD Package
24-Lead Plastic DFN (7mm × 4mm)
(Reference LTC DWG # 05-08-1864 Rev Ø)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





BOTTOM VIEW—EXPOSED PAD (DKD24) DFN 0210 REV Ø

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WXXX) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/16	Corrected text in SNR and Digital Filtering sections	19, 20
B	2/17	Corrected output data rate value in Table 1	21
C	4/17	Add operation for 1.024msps sample rate	21