# Dual SEPIC or Inverting µModule DC/DC Converter

## FEATURES

- **Two Complete Switch Mode Power Supplies**
- **SEPIC or Inverting Topology**
- **Wide Input Voltage Range: 2.6V to 20V**
- **2.5V to 24V or –2.5V to –24V Output Voltage**
- **1A at $5V_{OUT}$ from $12V_{IN}$**
- **Selectable Switching Frequency: 200kHz to 2.5MHz**
- **Power Good Outputs for Event Based Sequencing**
- User Configurable Undervoltage Lockout
- (e4) RoHS Compliant Package with Gold Pad Finish
- Low Profile 15mm × 9mm × 2.42mm Surface Mount BGA Package

## APPLICATIONS

- Battery Powered Regulator
- Local Negative Voltage Regulator
- Low Noise Amplifier Power

## DESCRIPTION

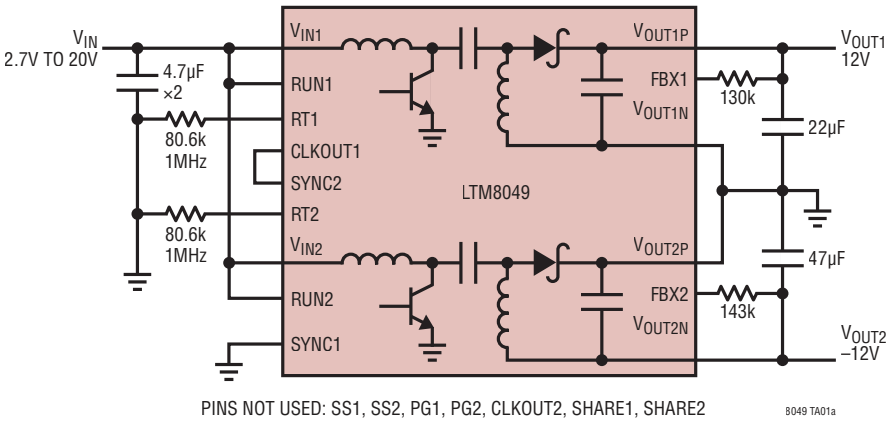
The LTM®8049 is a Dual SEPIC/Inverting µModule® (power module) DC/DC Converter. Each of the two outputs can be easily configured as a SEPIC or Inverting converter by simply grounding the appropriate output rail. The LTM8049 includes power devices, inductors, control circuitry and passive components. All that is needed to complete the design are input and output caps, and small resistors to set the output voltages and switching frequency. Other components may be used to control the soft-start and undervoltage lockout.

The LTM8049 is packaged in a thermally enhanced, compact (15mm × 9mm) over-molded Ball Grid Array (BGA) package suitable for automated assembly by standard surface mount equipment. The LTM8049 is available with SnPb (BGA) or RoHS compliant terminal finish.

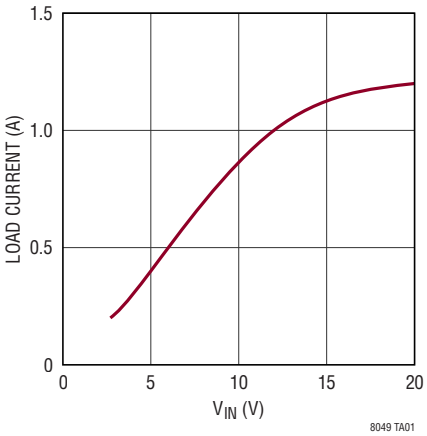


## TYPICAL APPLICATION

**±12$V_{OUT}$ from 2.7$V_{IN}$ to 20$V_{IN}$**




**Maximum Load Current vs $V_{IN}$**

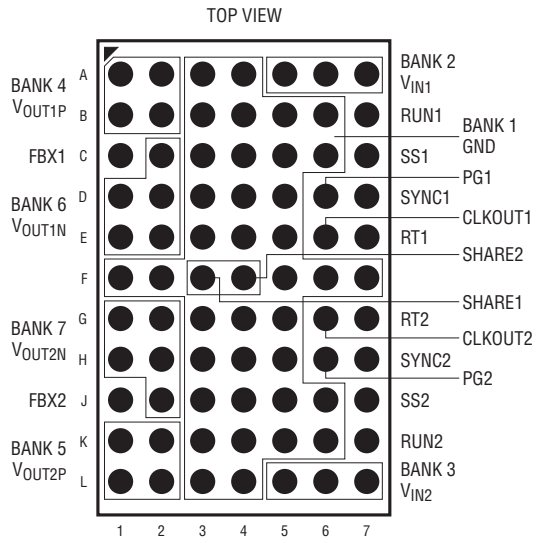


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$V_{INn}$, RUNn, PGn ..... 20V
SYNCn, FBXn ..... 5V
SSn ..... 2.5V
SHAREn ..... 2V
$V_{OUTP}$ ($V_{OUTN}$ = 0V) ..... 25V
$V_{OUTN}$ ($V_{OUTP}$ = 0V) ..... –25V
Maximum Internal Temperature ..... 125°C
Maximum Solder Temperature ..... 260°C
Storage Temperature ..... –55°C to 125°C

## PIN CONFIGURATION




BGA PACKAGE
77-LEAD (15mm × 9mm × 2.42mm)
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 16.2°C/W, $\theta_{JB}$ = 3.8°C/W, $\theta_{JCtop}$ = 8.8°C/W,
$\theta_{JCbottom}$ = 3.8°C/W, $\theta_{JCboard}$ = 4.6°C/W, WEIGHT = 0.8g,
θ VALUES DETERMINED PER JEDEC 51-9, 51-12

## ORDER INFORMATION

| PART NUMBER | PAD OR BALL FINISH | PART MARKING* | | PACKAGE TYPE | MSL RATING | TEMPERATURE RANGE (SEE NOTE 2) |
|---|---|---|---|---|---|---|
| | | DEVICE | FINISH CODE | | | |
| LTM8049EY#PBF | SAC305 (RoHS) | LTM8049Y | e1 | BGA | 3 | –40°C to 125°C |
| LTM8049IY#PBF | | | | | | |
| LTM8049IY | SnPb (63/37) | LTM8049 | e0 | | | |

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- BGA Package and Tray Drawings
- This product is not recommended for second side reflow. This product is moisture sensitive. For more information, go to Recommended BGA PCB Assembly and Manufacturing Procedures.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating temperature range (Notes 2, 3), otherwise specifications are at $T_A$ = 25°C. RUN = 2V unless otherwise specified.**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Minimum Input Operating Voltage | | ● | 2.6 | | | V |
| Positive Output DC Voltage | $I_{OUT}$ = 50mA, $R_{FB}$ = 15.4k, $V_{OUTN}$ Grounded<br>$I_{OUT}$ = 50mA, $R_{FB}$ = 274k, $V_{OUTN}$ Grounded | | | 2.5<br>24 | | V<br>V |
| Negative Output DC Voltage | $I_{OUT}$ = 50mA, $R_{FB}$ = 30.1k, $V_{OUTP}$ Grounded<br>$I_{OUT}$ = 50mA, $R_{FB}$ = 287k, $V_{OUTP}$ Grounded | | | –2.5<br>–24 | | V<br>V |
| Maximum Continuous Output DC Current | $V_{IN}$ = 12V, $V_{OUT}$ = 5V or –5V<br>$V_{IN}$ = 12V, $V_{OUT}$ = 24 or –24V | | 1<br>0.25 | | | A<br>A |
| $V_{IN}$ Quiescent Current | $V_{RUN}$ = 0V<br>$V_{RUN}$ = 2V, No Load | | | 0<br>10 | 2 | µA<br>mA |
| Line Regulation | 4 ≤ $V_{IN}$ ≤ 20V, $I_{OUT}$ = 0.6A | | | 0.1 | | % |
| Load Regulation | 0 ≤ $I_{OUT}$ ≤ 1A | | | 0.3 | | % |
| Switching Frequency | $R_T$ = 31.6k<br>$R_T$ = 412k | ●<br>● | 2100<br>160 | 2500<br>200 | 2900<br>240 | kHz<br>kHz |
| Voltage at FBX Pin | Positive Output<br>Negative Output | ●<br>● | 1.185<br>2 | 1.204<br>7 | 1.22<br>16 | V<br>mV |
| Current into FBX Pin | Positive Output<br>Negative Output | ●<br>● | 81<br>81 | 83.3<br>83.3 | 85.6<br>85.6 | µA<br>µA |
| RUN pin Threshold Voltage | RUN Pin Rising<br>RUN Pin Falling | | <br>1.21 | 1.31<br>1.27 | 1.4<br> | V<br>V |
| RUN Pin Current | $V_{RUN}$ = 3V<br>$V_{RUN}$ = 1.3V<br>$V_{RUN}$ = 0V | | <br>10.1<br> | 45<br>12.1<br>0 | 65<br>14.1<br>0.1 | µA<br>µA<br>µA |
| SS Sourcing Current | SS = 0V | | 5.7 | 8.8 | 11.7 | µA |
| Synchronization Frequency Range | | | 200 | | 2500 | kHz |
| SYNC Input Low Threshold | | | | | 0.4 | V |
| SYNC Input High Threshold | | | 1.3 | | | V |
| CLKOUT1 Duty Cycle | (Note 5) | | | 50 | | % |
| CLKOUT Output Voltage (Low) | 2k Pull-Up to 2V | | | | 0.2 | V |
| CLKOUT Output Voltage (High) | 2k Pull-Down to GND | | 1.9 | | | V |
| PG Threshold for Positive Feedback Voltage | FBX Rising | | 1.09 | | 1.2 | V |
| PG Threshold for Negative Feedback Voltage | FBX Falling | | 20 | | 120 | mV |
| PG Output Voltage Low | 100µA into PG, FBX = 1V | | | | 150 | mV |
| PG Leakage Current | PG = 20V, Run = 0V | | | | 1 | µA |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTM8049E is guaranteed to meet performance specifications from 0°C to 125°C. Specifications over the –40°C to 125°C internal temperature range are assured by design, characterization and correlation with statistical process controls. LTM8049I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

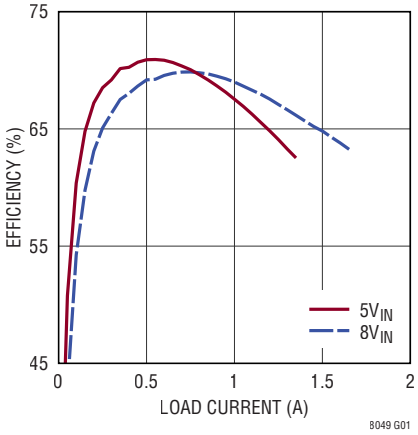
**Note 3:** This µModule regulator includes overtemperature protection that is intended to protect the device during momentary overload conditions. Internal temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum internal operating junction temperature may impair device reliability.

**Note 4:** CLKOUTn is intended to drive other circuitry. Do not apply a positive or negative voltage or current source to CLKOUT, otherwise permanent damage may occur.

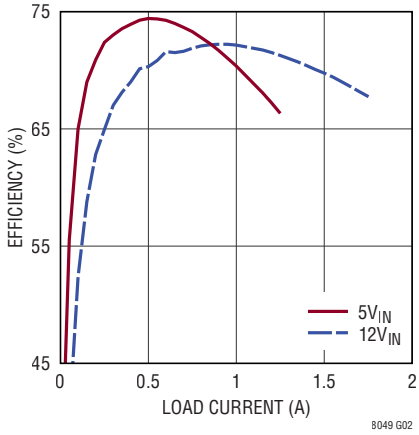
**Note 5:** The duty cycle of CLKOUT2 is dependent upon the internal temperature. See the Applications Information section for more details.

## TYPICAL PERFORMANCE CHARACTERISTICS

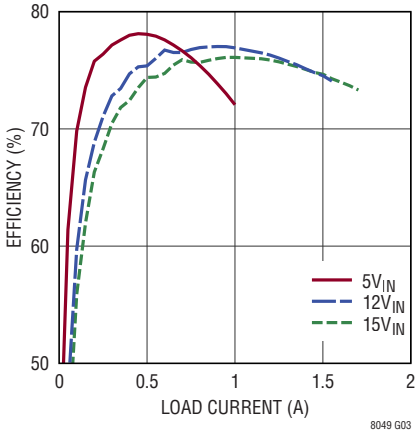
**Efficiency, $V_{OUT}$ ±2.5V**



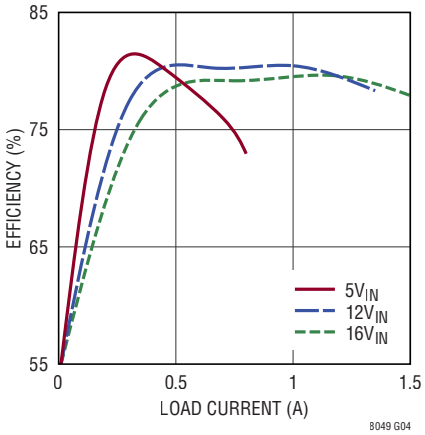

**Efficiency, $V_{OUT}$ ±3.3V**



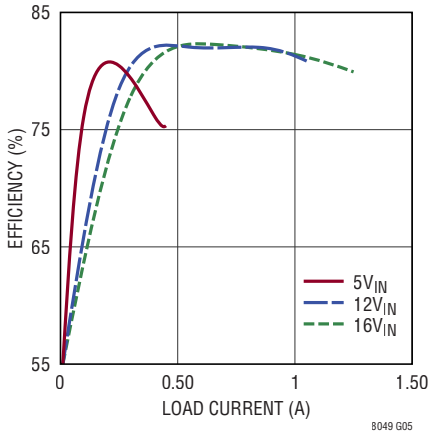

**Efficiency, $V_{OUT}$ ±5V**



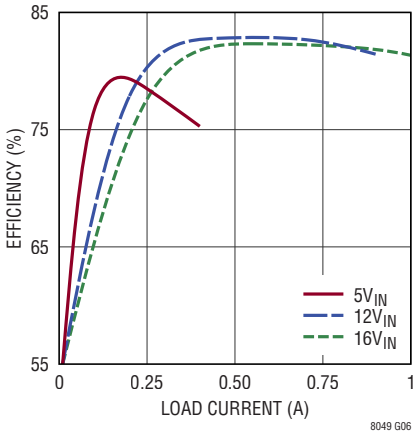

**Efficiency, $V_{OUT}$ ±8V**



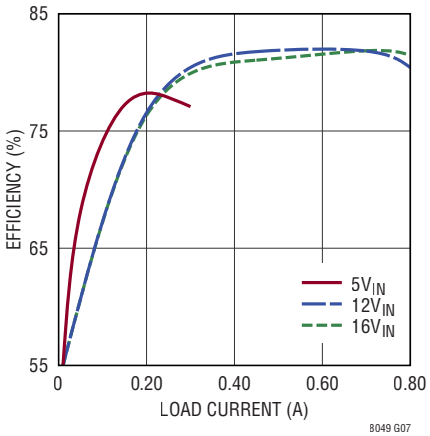

**Efficiency, $V_{OUT}$ ±12V**



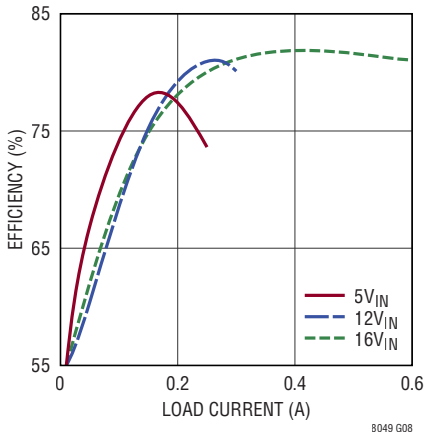

**Efficiency, $V_{OUT}$ ±15V**



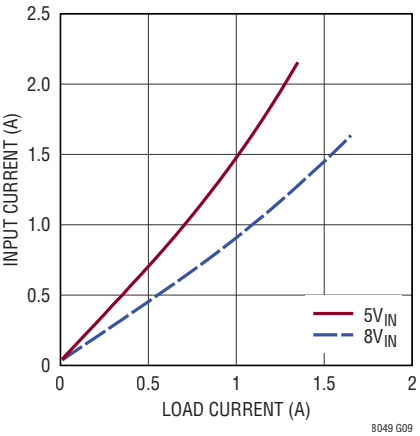

**Efficiency, $V_{OUT}$ ±18V**




**Efficiency, $V_{OUT}$ ±24V**

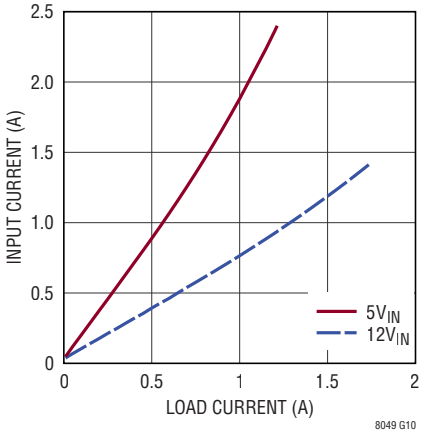



**Input vs Load Current, $V_{OUT}$ ±2.5V**

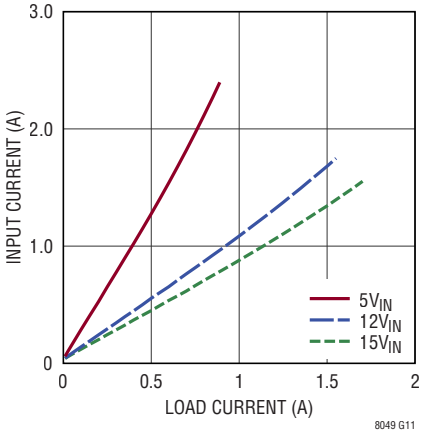


# TYPICAL PERFORMANCE CHARACTERISTICS

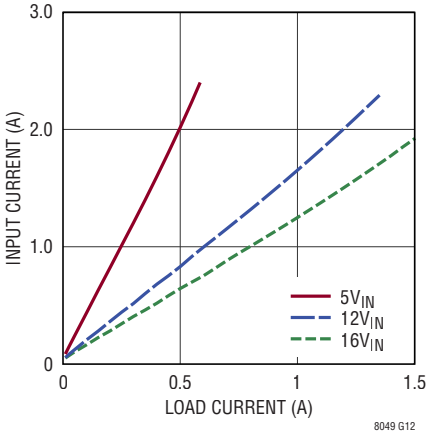
**Input vs Load Current, $V_{OUT}$ ±3.3V**



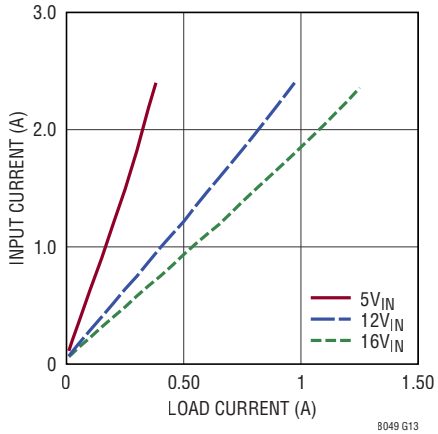

**Input vs Load Current, $V_{OUT}$ ±5V**



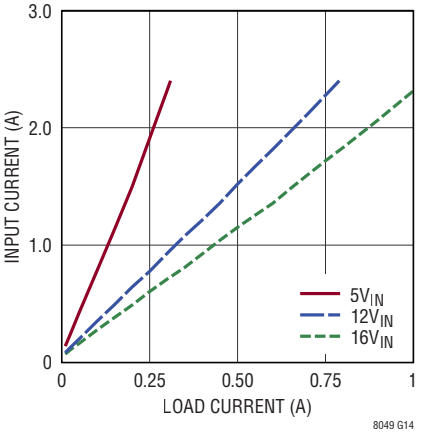

**Input vs Load Current, $V_{OUT}$ ±8V**



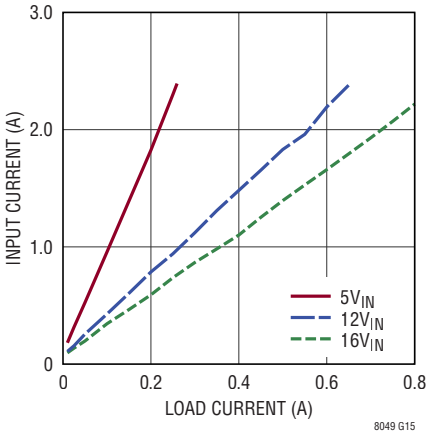

**Input vs Load Current, $V_{OUT}$ ±12V**



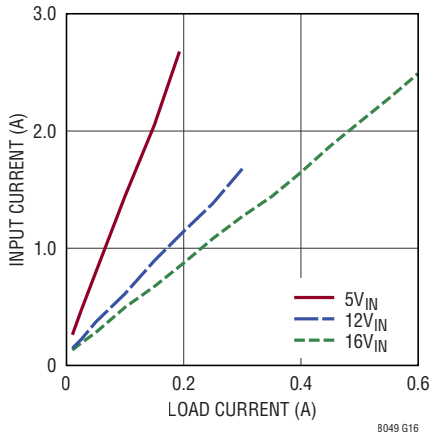

**Input vs Load Current, $V_{OUT}$ ±15V**



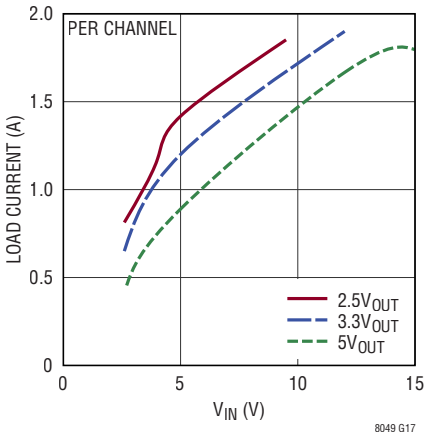

**Input vs Load Current, $V_{OUT}$ ±18V**



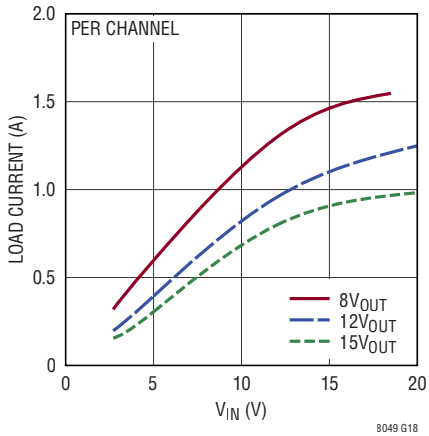

**Input vs Load Current, $V_{OUT}$ ±24V**




**Maximum Load Current vs $V_{IN}$**

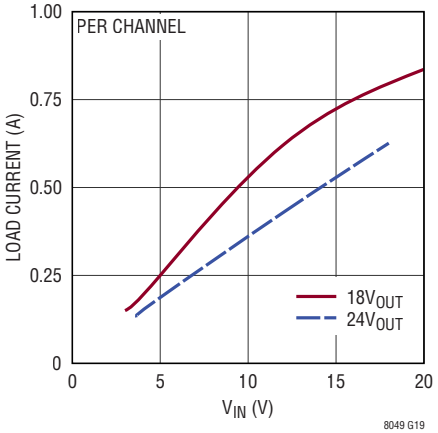



**Maximum Load Current vs $V_{IN}$**

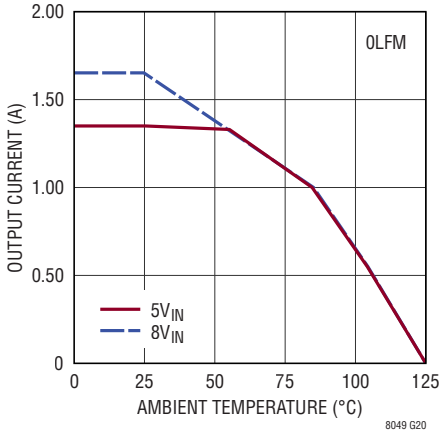


## TYPICAL PERFORMANCE CHARACTERISTICS

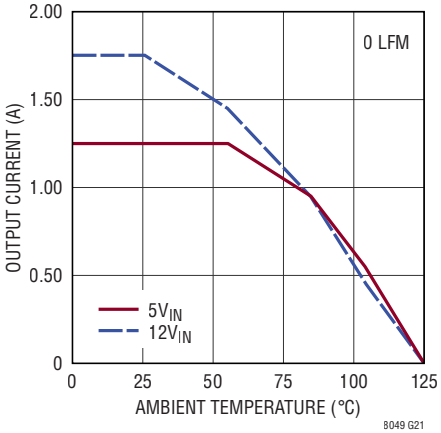
### Maximum Load Current vs $V_{IN}$



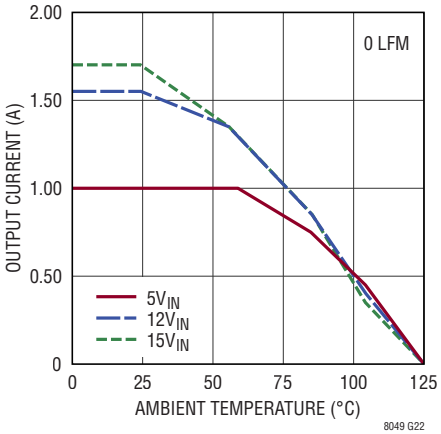

### Derating Curve, $V_{OUT}$ ±2.5$V_{OUT}$



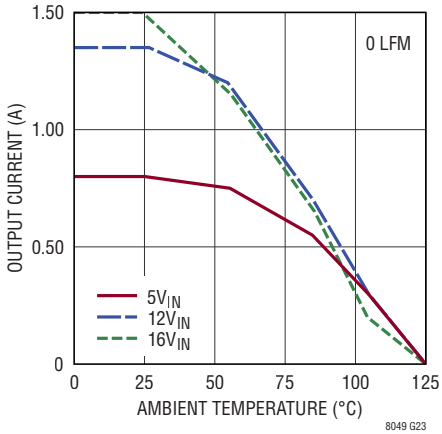

### Derating Curve, $V_{OUT}$ ±3.3$V_{OUT}$



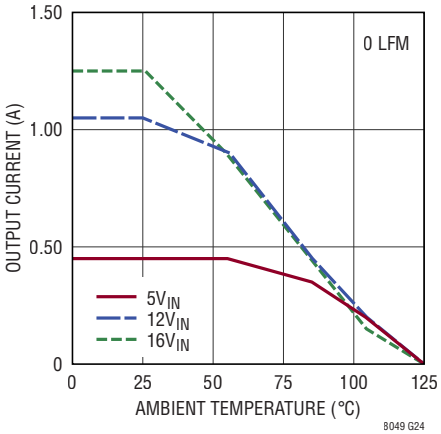

### Derating Curve, $V_{OUT}$ ±5$V_{OUT}$



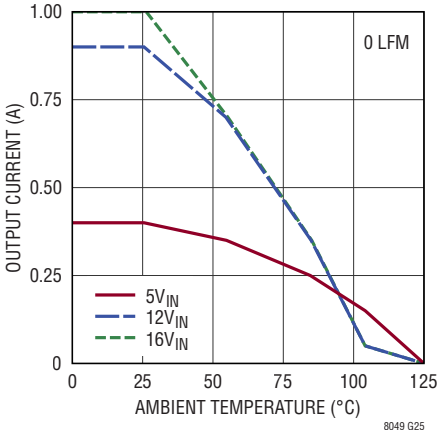

### Derating Curve, $V_{OUT}$ ±8$V_{OUT}$



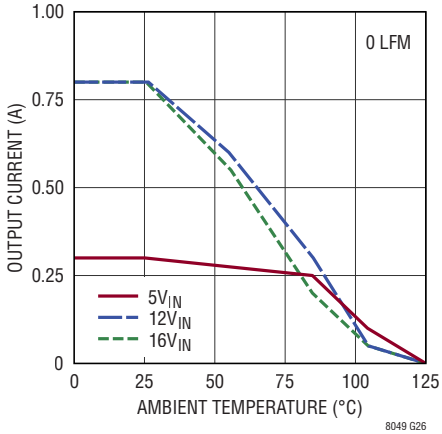

### Derating Curve, $V_{OUT}$ ±12$V_{OUT}$



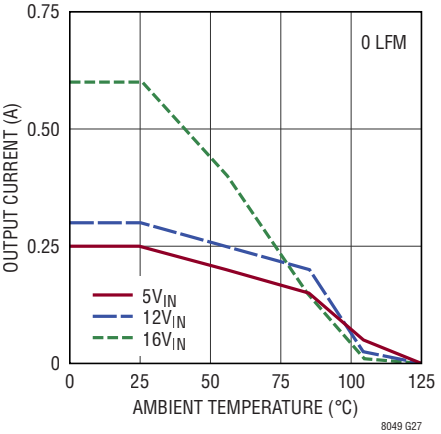

### Derating Curve, $V_{OUT}$ ±15$V_{OUT}$




### Derating Curve, $V_{OUT}$ ±18$V_{OUT}$

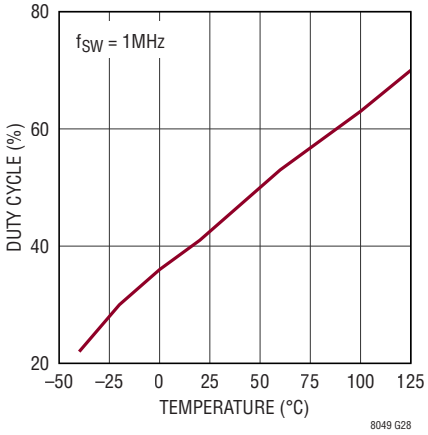



### Derating Curve, $V_{OUT}$ ±24$V_{OUT}$

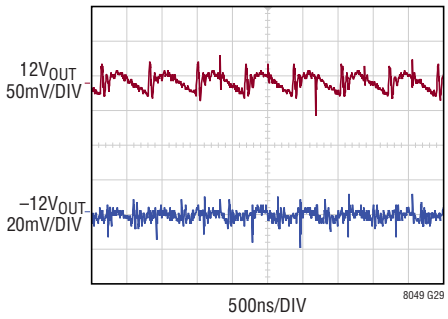


## TYPICAL PERFORMANCE CHARACTERISTICS

**CLKOUT2 Duty Cycle vs Temperature**




**Output Ripple, DC2244A Board 800mA Load, $12V_{IN}$ Measured Across C5, C6**




## PIN FUNCTIONS

**GND (Bank 1):** Tie these GND pins to a local ground plane below the LTM8049 and the circuit components. GND MUST BE CONNECTED EITHER TO $V_{OUTP}$ OR $V_{OUTN}$ FOR PROPER OPERATION. In most applications, the bulk of the heat flow out of the LTM8049 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details. Return the feedback divider (RFB) to this net.

**$V_{IN1}$, $V_{IN2}$ (Banks 2, 3):** The $V_{INn}$ pins supply current to the LTM8049's internal regulator and to the internal power switch. This pin must be locally bypassed with an external, low ESR capacitor.

**$V_{OUT1P}$, $V_{OUT2P}$ (Banks 4, 5):** $V_{OUTnP}$ is the positive output of the LTM8049. Apply an external capacitor between $V_{OUTnP}$ and $V_{OUTnN}$. Tie this net to GND to configure the LMT8049 as a negative output Inverting regulator.

**$V_{OUT1N}$, $V_{OUT2N}$ (Banks 6, 7):** $V_{OUTnN}$ is the negative output of the LTM8049. Apply an external capacitor between $V_{OUTnP}$ and $V_{OUTnN}$. Tie this net to GND to configure the LTM8049 as a positive output SEPIC regulator.

**RUN1, RUN2 (Pins B7, K7):** These pins are used to enable/disable the chip and restart the soft-start sequence. Drive below 1.21V to stop the LTM8049 from switching. Drive above 1.4V to activate the device and restart the soft-start sequence. Do not float this pin.

**RT1, RT2 (Pins E7, G7):** The RTn pins are used to program the switching frequency of the LTM8049 by connecting a resistor from this pin to ground. The switching frequency of the LTM8049 is determined by the equation RTn = (81.6/$f_{OSC}$)-1, where the $f_{OSC}$ is the switching frequency in MHz. This pin must have a resistor to GND. Do not apply a voltage to this pin.

**SS1, SS2 (Pins C7, J7):** Connect a soft-start capacitor from this pin to GND. Upon start-up, the SSn pins will be charged by an internal current source to about 2V.

**SYNC1, SYNC2 (Pins D7, H7):** To synchronize the switching frequency to an outside clock, simply drive this pin with a clock signal. The high voltage level of the clock needs to exceed 1.3V, and the low level must be less than 0.4V. Drive this pin to less than 0.4V to revert to the internal free running clock. Ground these pins if synchronization is not required. See the Applications Information section for more information.

## PIN FUNCTIONS

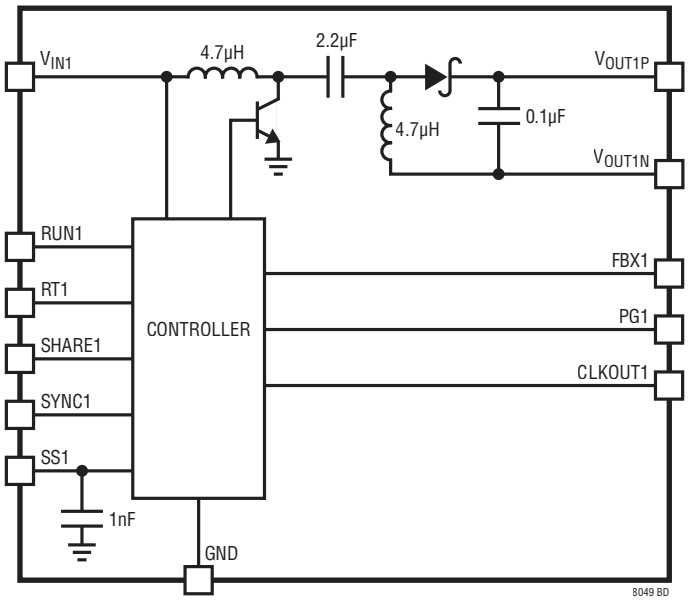
**FBX1, FBX2 (Pins C1, J1):** If configured as a SEPIC, the LTM8049 regulates its FBX pin to 1.204V. Apply a resistor between FBX and $V_{OUTP}$. Its value should be $R_{FB}$ = [($V_{OUTP}$ – 1.204)/0.0833]k. If the LTM8049 is configured as an inverting converter, the LTM8049 regulates the FBX pin to 7mV. Apply a resistor between FBX and $V_{OUTN}$ of value $R_{FB}$ = [(|$V_{OUTN}$| + 0.007)/0.0833]k. The LTM8049 features frequency foldback to protect the power switches during a fault or output current overload. During start-up, frequency foldback also limits the current the LTM8049 delivers to the load. The user must evaluate the start-up behavior of the LTM8049 to ensure that it properly powers up the load.

**PG1, PG2 (Pins D6, H6):** These active high pins indicates that the FBn pin voltage for the corresponding channel is within 4% of its regulation voltage These open drain outputs requires a pull-up resistor to indicate power good. Also, the status of these pins is valid only when RUN > 1.4V and $V_{IN}$ > 2.6V.

**CLKOUT1, CLKOUT2 (Pins E6, G6):** Use these pins to synchronize devices to either channel of the LTM8049. These pins oscillate at the same frequency as the LTM8049 internal oscillator or, if active, the SYNC pin. The CLKOUT1 signal is about 180° out of phase with the oscillator of channel 1 and duty cycle is about 50%. The CLKOUT2 signal is in phase with the internal oscillator of channel 2 and its duty cycle varies linearly with the internal temperature of the LTM8049. Please refer to the Applications Information section for detailed information on using CLKOUT2 as an indication of the LTM8049 internal temperature. Do not apply a voltage to this pin or use this pin to drive capacitive loads greater than 120pF.

**SHARE1, 2 (pins F3, F4):** Connect these pins together if the two outputs of the LTM8049 are paralleled. Otherwise, leave these pins floating.

## BLOCK DIAGRAM




NOTE: CHANNEL 1. CHANNEL 2 IS FUNCTIONAL IDENTICAL, EXCEPT FOR THE CLKOUT2 VS TEMPERATURE BEHAVIOR. PLEASE SEE THE PIN DESCRIPTION AND APPLICATIONS INFORMATION SECTIONS FOR DETAILS.

## OPERATION

The LTM8049 contains two stand-alone switching DC/DC converters; either one may be configured as a SEPIC (single-ended primary inductance converter) or inverting power supply simply by tying $V_{OUTN}$ or $V_{OUTP}$ to GND, respectively. It accepts an input voltage up to 20VDC. The output is adjustable between 2.5V and 24V for the SEPIC, and between –2.5V and –24V for the inverting configuration. The LTM8049 can provide 1.5A at $V_{IN}$ = 12V when $V_{OUT}$ = 5V or –5V at ambient room temperature.

As shown in the Block Diagram, the LTM8049 contains a current mode controller, power switching element, power coupled inductor, power Schottky diode and a modest amount of input and output capacitance. The LTM8049 is a fixed frequency PWM regulator.

The LTM8049 switching can free run by applying a resistor to the RT pin or synchronize to an external source at a frequency between 200kHz and 2.5MHz. To synchronize to an external source, drive a valid signal source into the SYNC pin. See Synchronization in the Applications Section for more details.

The LTM8049 also features RUN and SS pins to control the start-up behavior of the device. The RUN pin may also be used to implement an accurate undervoltage lockout function by applying a resistor network to the RUN pin.

The LTM8049 features frequency foldback to protect the power switches during a fault or output current overload. During start-up, frequency foldback also limits the current the LTM8049 delivers to the load. The user must evaluate the start-up behavior of the LTM8049 to ensure that it properly powers up the load.

The LTM8049 is equipped with a thermal shutdown to protect the device during momentary overload conditions. It is set above the 125°C absolute maximum internal temperature rating to avoid interfering with normal specified operation, so internal device temperatures will exceed the absolute maximum rating when the overtemperature protection is active. Therefore, continuous or repeated activation of the thermal shutdown may impair device reliability.

## APPLICATIONS INFORMATION

For most applications, the design process is straight forward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.
2. Apply the recommended $C_{IN}$, $C_{OUT}$, $R_{ADJ}$ and $R_T$ values.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions. Bear in mind that the maximum output current is limited by junction temperature, the relationship between the input and output voltage magnitude and polarity and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

Table 1 gives the recommended component values and configuration for a single channel. Each channel may be configured independently. The maximum frequency (and attendant $R_T$ value) at which the LTM8049 should be allowed to switch is given in Table 1 in the $f_{MAX}$ column, while the recommended frequency (and $R_T$ value) for optimal efficiency over the given input condition is given in the $f_{OPTIMAL}$ column. Running the LTM8049 faster than the recommended frequency may reduce the usable input voltage range.

### Capacitor Selection Considerations

The $C_{IN}$ and $C_{OUT}$ capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended, and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied

## APPLICATIONS INFORMATION

**Table 1. Recommended Component Values and Configuration ($T_A$ = 25°C)**

| $V_{IN}$ RANGE (V) | $V_{OUT}$ (V) | $C_{IN}$ | $C_{OUT}$ | $R_{FB}$ (Ω) | $f_{OPTIMAL}$ | $R_{TOPTIMAL}$ (Ω) | $f_{MAX}$ | $R_{TMIN}$ (Ω) |
|---|---|---|---|---|---|---|---|---|
| 2.6V to 11.5V | 2.5V | 4.7µF 25V 0603 X5R | 100µF 4V 0805 X5R | 15.4k | 600kHz | 137k | 2MHz | 38.3k |
| 2.6V to 9.5V | –2.5V | 4.7µF 25V 0603 X5R | 100µF 4V 0805 X5R + 47µF 6.3V 0805 X5R | 30.1k | 600kHz | 137k | 2MHz | 38.3k |
| 2.6V to 18V | 3.3V | 4.7µF 25V 0603 X5R | 100µF 4V 0805 X5R | 25.5k | 650kHz | 124k | 2.3MHz | 33.2k |
| 2.6V to 12V | –3.3V | 4.7µF 25V 0603 X5R | 100µF 4V 0805 X5R + 47µF 6.3V 0805 X5R | 39.2k | 650kHz | 124k | 2.3MHz | 33.2k |
| 2.7V to 20V | 5V | 4.7µF 25V 0603 X5R | 47µF 6.3V 0805 X5R | 45.3k | 750k | 107k | 2.5MHz | 31.6k |
| 2.7V to 15V | –5V | 4.7µF 25V 0603 X5R | 100µF 6.3V 1206 X5R + 47µF 10V 1206 X5R | 60.4k | 750k | 107k | 2.5MHz | 31.6k |
| 2.7V to 20V | 8V | 4.7µF 25V 0603 X5R | 22µF 10V 1206 X5R | 82.5k | 1MHz | 80.6k | 2.5MHz | 31.6k |
| 2.7 to 18.5V | –8V | 4.7µF 25V 0603 X5R | 2x 47µF 10V 1206 X5R | 95.3k | 1MHz | 80.6k | 2.5MHz | 31.6k |
| 2.7V to 20V | 12V | 4.7µF 25V 0603 X5R | 22µF 16V 1210 X5R | 130k | 1MHz | 80.6k | 2.5MHz | 31.6k |
| 2.7V to 20V | –12V | 4.7µF 25V 0603 X5R | 47µF 16V 1210 X5R | 143k | 1MHz | 80.6k | 2.5MHz | 31.6k |
| 2.7V to 20V | 15V | 4.7µF 25V 0603 X5R | 22µF 16V 1210 X5R | 165k | 1.1MHz | 73.2k | 1.9MHz | 41.2k |
| 2.7V to 20V | –15V | 4.7µF 25V 0603 X5R | 47µF 16V 1210 X5R | 178k | 1.1MHz | 73.2k | 1.9MHz | 41.2k |
| 3V to 20V | 18V | 4.7µF 25V 0603 X5R | 22µF 16V 1210 X7R | 200k | 1.5MHz | 53.6k | 1.8MHz | 45.3k |
| 3V to 20V | –18V | 4.7µF 25V 0603 X5R | 22µF 16V 1210 X7R | 215k | 1.5MHz | 53.6k | 1.8MHz | 45.3k |
| 3.7V to 18V | 24V | 4.7µF 25V 0603 X5R | 22µF 25V 1206 X5R | 274k | 1.5MHz | 53.6k | 1.8MHz | 45.3k |
| 3.7V to 18V | –24V | 4.7µF 25V 0603 X5R | 22µF 25V 1206 X5R | 287k | 1.5MHz | 53.6k | 1.8MHz | 45.3k |

Note: An input bulk capacitor is required.

voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8049. A ceramic input capacitor combined with trace or cable inductance forms a high Q (underdamped) tank circuit. If the LTM8049 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

### Programming Switching Frequency

The LTM8049 has an operational switching frequency range between 200kHz and 2.5MHz. The free running frequency is programmed with an external resistor from the RT pin to ground. Do not leave this pin open under any condition. When the SYNC pin is driven low (<0.4V), the frequency of operation is set by a resistor from RT to ground. The $R_T$ value is calculated by the following equation:

$$R_T = \frac{81.6}{f_{OSC}} - 1, \text{ where } f_{OSC} \text{ is in MHz and } R_T \text{ is in k}\Omega$$

### Switching Frequency Trade-Offs

It is recommended that the user apply the optimal $R_T$ value given in Table 1 for the corresponding input and output operating condition. System level or other considerations, however, may necessitate another operating frequency. While the LTM8049 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, reduce the usable input voltage range, generate excessive heat or even damage the LTM8049 in some fault conditions. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor. Note that the Maximum Output Current vs Input Voltage curves given in theTypical Performance Characteristics section are for the recommended operating conditions in Table 1. Using a different operating frequency may result in a different maximum output current.

## APPLICATIONS INFORMATION

### Soft-Start

The soft-start circuitry provides for a gradual ramp-up of the switch current in each channel. When the channel is enabled, the external SS capacitor is first discharged. This resets the state of the logic circuits in the channel. Then an integrated resistor pulls the channel's SS pin to about 1.8V. The LTM8049 has a built-in soft-start characteristic, but a slower ramp rate may be implemented by adding capacitance to the SS pin. Typical values are between 0.1µF and 1µF.

### Configurable Undervoltage Lockout

Figure 1 shows how to configure an undervoltage lockout (UVLO) for the LTM8049. Typically, UVLO is used in situations where the input supply is current-limited, has a relatively high source resistance, or ramps up/down slowly. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current-limit or latch low under low source voltage conditions. UVLO prevents the regulator from operating at source voltages where these problems might occur.

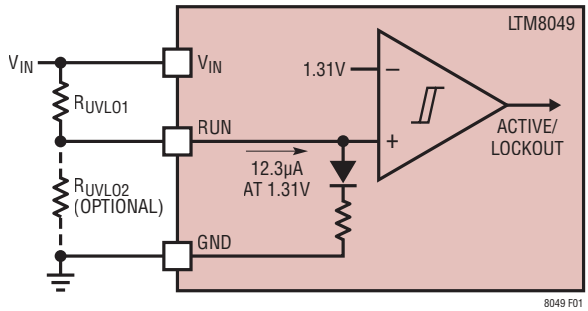



**Figure 1. The RUN Pin May Be Used to Implement an Accurate UVLO**

The RUN pin sinks 12.1µA at the 1.31V rising threshold voltage and about 11.6µA at the 1.27V falling threshold. This makes it easy to set up an input voltage UVLO threshold with just a single resistor. For a desired $V_{IN}$ threshold, choose $R_{UVLO1}$ using the equation:

$$R_{UVLO1} = \frac{V_{IN} - 1.31V}{12.1\mu A}$$

The RUN pin has a voltage hysteresis with typical thresholds of 1.31V (rising) and 1.27V (falling). Resistor $R_{UVLO2}$ is optional. $R_{UVLO2}$ can be included to reduce the overall UVLO voltage variation caused by variations in the RUN pin current (see the Electrical Characteristics). A good choice for $R_{UVLO2}$ is ≤10k + 1%. After choosing a value for $R_{UVLO2}$, $R_{UVLO1}$ can be determined from either of the following:

$$R_{UVLO1} = \frac{V_{IN(RISING)} - 1.31V}{\frac{1.32V}{R_{UVLO2}} + 12.1\mu A}$$

or

$$R_{UVLO1} = \frac{V_{IN(FALLING)} - 1.27V}{\frac{1.29V}{R_{UVLO2}} + 11.6\mu A}$$

where $V_{IN(RISING)}$ and $V_{IN(FALLING)}$ are the $V_{IN}$ threshold voltages when rising or falling respectively.

For example, to disable the LTM8049 for $V_{IN}$ voltages below 3.5V using the single resistor configuration, choose:

$$R_{UVLO1} = \frac{3.5V - 1.27V}{\frac{1.29V}{\infty} + 11.6\mu A} \cong 191k$$

To activate the LTM8049 for $V_{IN}$ greater than 4.5V using the two resistor configuration, choose $R_{UVLO2}$ = 10k and:

$$R_{UVLO1} = \frac{4.5V - 1.31V}{\frac{1.32V}{10k} + 12.1\mu A} \cong 22.1k$$

### Internal Undervoltage Lockout

The LTM8049 monitors the $V_{IN}$ supply voltage in case $V_{IN}$ drops below a minimum operating level (typically about 2.3V). When $V_{IN}$ is detected low, the power switch is deactivated, and while sufficient $V_{IN}$ voltage persists, the soft-start capacitor is discharged. After $V_{IN}$ is sufficiently high, the LTM8049 will reactivate and the soft-start capacitor will begin charging.

## APPLICATIONS INFORMATION

### Frequency Foldback

The frequency foldback function reduces the switching frequency for that channel when the output is about 15% below the target regulation point. This feature lowers the operating frequency, thus controlling the maximum output current during start-up. When the FBX voltage is pulled above the above mentioned range in a positive output voltage application, the switching frequency for that channel runs that the rate set by the $R_T$ resistor value. Note that the maximum output current at start-up is a function of many variables including load profile, output capacitance, target $V_{OUT}$, $V_{IN}$, switching frequency, so the user must evaluate the performance of the LTM8049 to ensure that it properly powers up its load.

### Thermal Shutdown

If the part is too hot, the LTM8049 engages its thermal shutdown and terminates switching and discharges the soft-start capacitor. When the part has cooled, the part automatically restarts. This thermal shutdown is set to engage at temperatures above the 125°C absolute maximum internal operating rating to ensure that it does not interfere with functionality in the specified operating range. This means that internal temperatures will exceed the 125°C absolute maximum rating when the over-temperature protection is active, possibly impairing the device's reliability.

### PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8049. The LTM8049 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 2 for a suggested layout. Ensure that the grounding and heat-sinking are acceptable.

A few rules to keep in mind are:

1. Place the $R_{FBX}$ and $R_T$ resistors as close as possible to their respective pins.
2. Place the $C_{IN}$ capacitor as close as possible to the $V_{IN}$ and GND connection of the LTM8049.
3. Place the $C_{OUT}$ capacitor as close as possible to the $V_{OUT}$ and GND connection of the LTM8049.

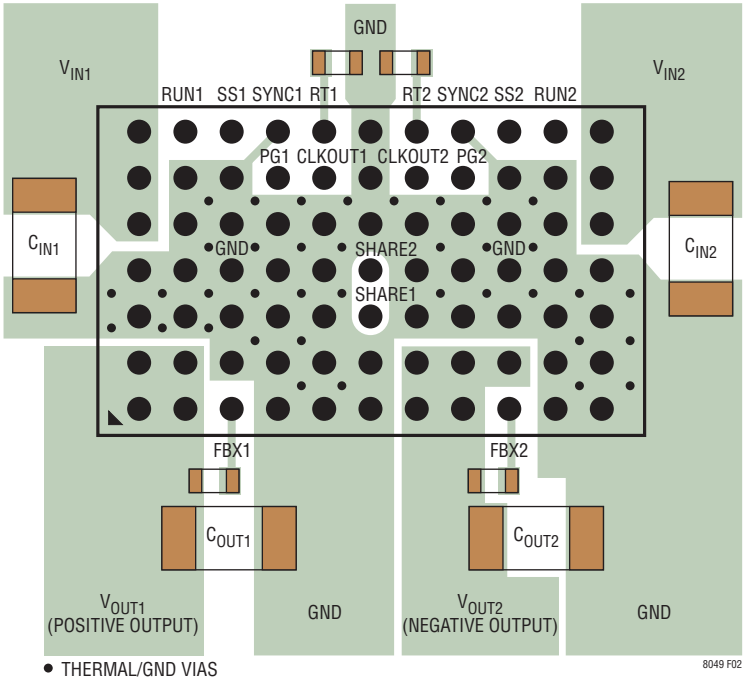



**Figure 2. Layout Showing Suggested External Components, GND Plane and Thermal Vias**

## APPLICATIONS INFORMATION

4. Place the $C_{IN}$ and $C_{OUT}$ capacitors such that their ground current flow directly adjacent or underneath the LTM8049.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8049.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 2. The LTM8049 can benefit from the heat-sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

### Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8049. However, these capacitors can cause problems if the LTM8049 is plugged into a live input supply (see Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the $V_{IN}$ pin of the LTM8049 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8049's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM8049 into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to $V_{IN}$, but the most popular method of controlling input voltage overshoot is to add an electrolytic bulk capacitor to the $V_{IN}$ net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is physically large.

### Thermal Considerations

The LTM8049 output current may need to be derated if it is required to operate in a high ambient temperature or deliver a large amount of continuous power. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by a LTM8049 mounted to a 58cm$^2$ 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

The thermal resistance numbers listed in Page 2 of the data sheet are based on modeling the µModule package mounted on a test board specified per JESD51-9 (Test Boards for Area Array Surface Mount Package Thermal Measurements). The thermal coefficients provided in this page are based on JESD 51-12 (Guidelines for Reporting and Using Electronic Package Thermal Information).

For increased accuracy and fidelity to the actual application, many designers use FEA to predict thermal performance. To that end, Page 2 of the data sheet typically gives four thermal coefficients:

$\theta_{JA}$: Thermal resistance from junction to ambient

$\theta_{JCbottom}$: Thermal resistance from junction to the bottom of the product case

$\theta_{JCtop}$: Thermal resistance from junction to top of the product case

$\theta_{JB}$: Thermal resistance from junction to the printed circuit board.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased below:

$\theta_{JA}$ is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as still

## APPLICATIONS INFORMATION

air although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

$\theta_{JCbottom}$ is the thermal resistance between the junction and bottom of the package with all of the component power dissipation flowing through the bottom of the package. In the typical µModule converter, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

$\theta_{JCtop}$ is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule converter are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

$\theta_{JB}$ is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule converter and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule converter. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs load graphs given in the product's data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

A graphical representation of these thermal resistances is given in Figure 3.

The blue resistances are contained within the µModule converter, and the green are outside.

The die temperature of the LTM8049 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8049. The bulk of the heat flow out of the LTM8049 is through the bottom of the µModule converter and the BGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

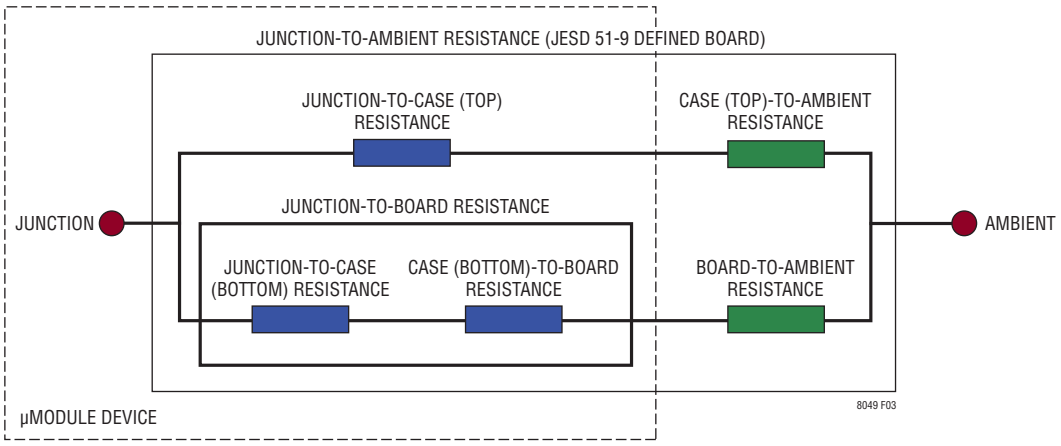
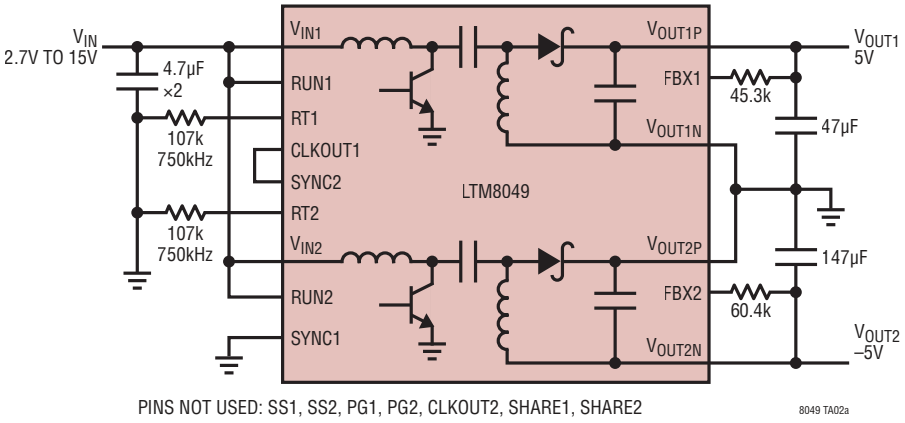


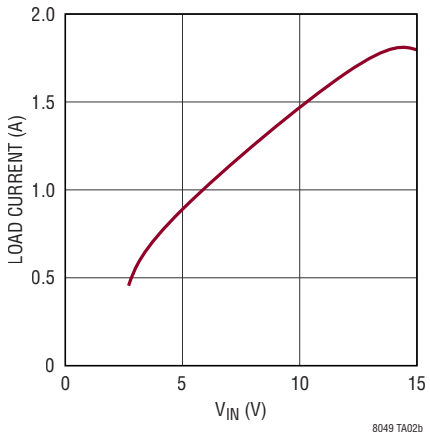

**Figure 3. Graphical Representation of JESD51-12 Thermal Coefficients**

## TYPICAL APPLICATIONS

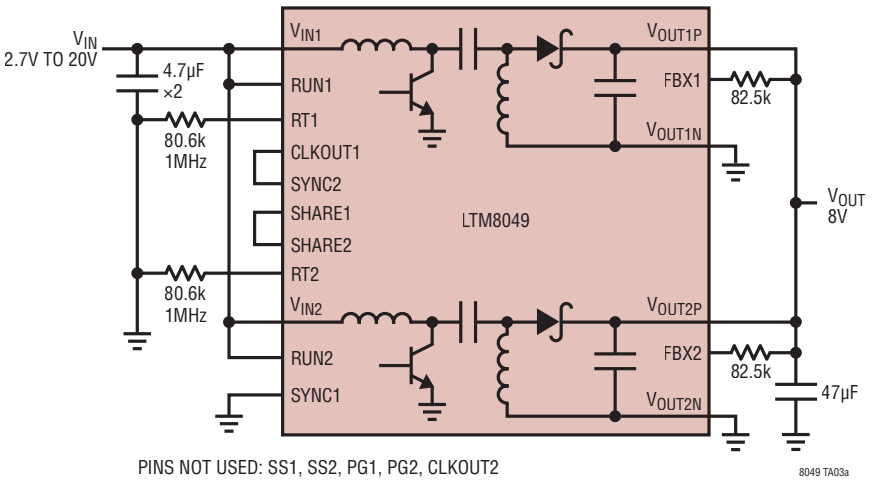
### ±5V Converter



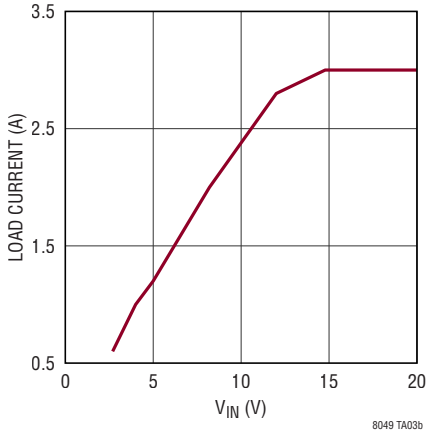

### Maximum Load Current vs $V_{IN}$




### Parallel 8V Outputs for Increased Current




### Maximum Load Current vs $V_{IN}$



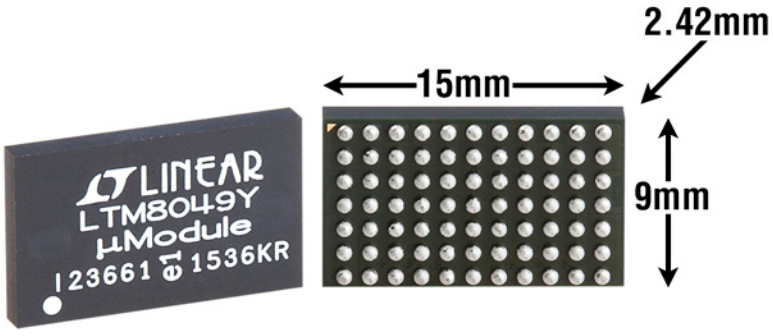
# PACKAGE DESCRIPTION

**Pin Assignment Table**
**(Arranged by Pin Number)**

| PIN NAME | | PIN NAME | | PIN NAME | | PIN NAME | | PIN NAME | | PIN NAME | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | $V_{OUT1P}$ | B1 | $V_{OUT1P}$ | C1 | FBX1 | D1 | $V_{OUT1N}$ | E1 | $V_{OUT1N}$ | F1 | GND |
| A2 | $V_{OUT1P}$ | B2 | $V_{OUT1P}$ | C2 | $V_{OUT1N}$ | D2 | $V_{OUT1N}$ | E2 | $V_{OUT1N}$ | F2 | GND |
| A3 | GND | B3 | GND | C3 | GND | D3 | GND | E3 | GND | F3 | SHARE1 |
| A4 | GND | B4 | GND | C4 | GND | D4 | GND | E4 | GND | F4 | SHARE2 |
| A5 | $V_{IN1}$ | B5 | GND | C5 | GND | D5 | GND | E5 | GND | F5 | GND |
| A6 | $V_{IN1}$ | B6 | GND | C6 | GND | D6 | PG1 | E6 | CLKOUT1 | F6 | GND |
| A7 | $V_{IN1}$ | B7 | RUN1 | C7 | SS1 | D7 | SYNC1 | E7 | RT1 | F7 | GND |

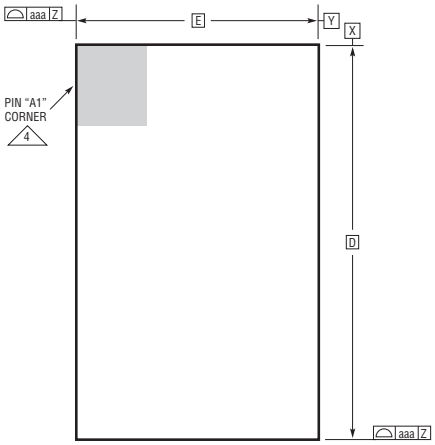
| PIN NAME | | PIN NAME | | PIN NAME | | PIN NAME | | PIN NAME | |
|---|---|---|---|---|---|---|---|---|---|
| G1 | $V_{OUT2N}$ | H1 | $V_{OUT2N}$ | J1 | FBX2 | K1 | $V_{OUT2P}$ | L1 | $V_{OUT2P}$ |
| G2 | $V_{OUT2N}$ | H2 | $V_{OUT2N}$ | J2 | $V_{OUT2N}$ | K2 | $V_{OUT2P}$ | L2 | $V_{OUT2P}$ |
| G3 | GND | H3 | GND | J3 | GND | K3 | GND | L3 | GND |
| G4 | GND | H4 | GND | J4 | GND | K4 | GND | L4 | GND |
| G5 | GND | H5 | GND | J5 | GND | K5 | GND | L5 | $V_{IN2}$ |
| G6 | CLKOUT2 | H6 | PG2 | J6 | GND | K6 | GND | L6 | $V_{IN2}$ |
| G7 | RT2 | H7 | SYNC2 | J7 | SS2 | K7 | RUN2 | L7 | $V_{IN2}$ |

# PACKAGE PHOTO

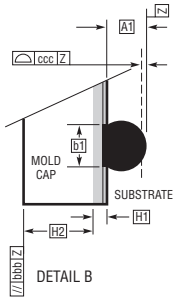


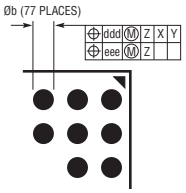
# PACKAGE DESCRIPTION

**BGA Package**
**77-Lead (15.00mm × 9.00mm × 2.42mm)**
(Reference LTC DWG# 05-08-1964 Rev B)

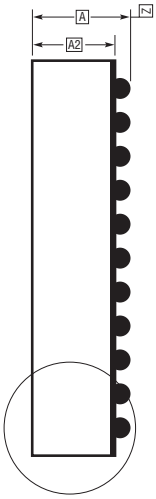



PACKAGE TOP VIEW

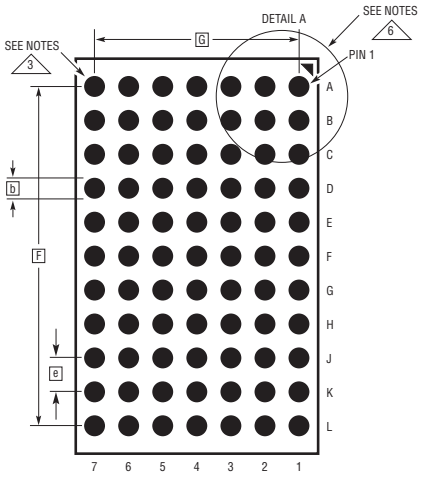


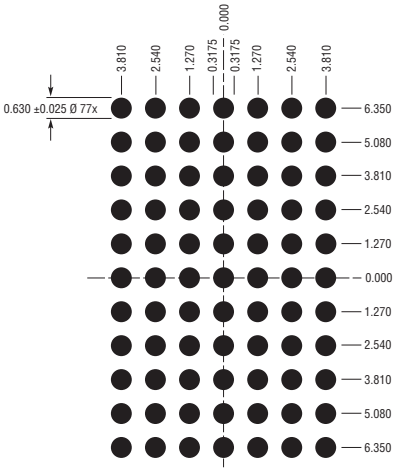

DETAIL A




DETAIL B
PACKAGE SIDE VIEW




PACKAGE BOTTOM VIEW




SUGGESTED PCB LAYOUT
TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

2. ALL DIMENSIONS ARE IN MILLIMETERS

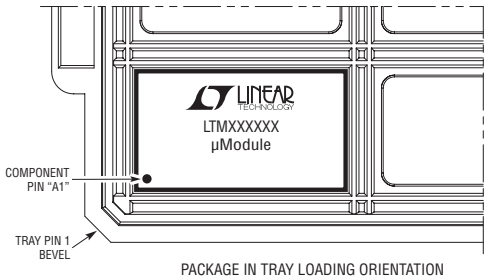
3 BALL DESIGNATION PER JESD MS-028 AND JEP95

4 DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE

5. PRIMARY DATUM -Z- IS SEATING PLANE

6 ⚠ PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

| DIMENSIONS | | | | |
|---|---|---|---|---|
| **SYMBOL** | **MIN** | **NOM** | **MAX** | **NOTES** |
| A | 2.22 | 2.42 | 2.62 | |
| A1 | 0.50 | 0.60 | 0.70 | BALL HT |
| A2 | 1.72 | 1.82 | 1.92 | |
| b | 0.60 | 0.75 | 0.90 | BALL DIMENSION |
| b1 | 0.60 | 0.63 | 0.66 | PAD DIMENSION |
| D | | 15.00 | | |
| E | | 9.00 | | |
| e | | 1.27 | | |
| F | | 12.70 | | |
| G | | 7.62 | | |
| H1 | 0.27 | 0.32 | 0.37 | SUBSTRATE THK |
| H2 | 1.45 | 1.50 | 1.55 | MOLD CAP HT |
| aaa | | | 0.15 | |
| bbb | | | 0.10 | |
| ccc | | | 0.20 | |
| ddd | | | 0.30 | |
| eee | | | 0.15 | |
| TOTAL NUMBER OF BALLS: 77 | | | | |




PACKAGE IN TRAY LOADING ORIENTATION

BGA 77 0517 REV B

## REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 12/17 | Added SnPb BGA Package | 1, 2 |
| B | 07/18 | Added SS1 pin to Block Diagram | 9 |