24-Bit, 1Msps, Pseudo-Differential Unipolar SAR ADC with Integrated Digital Filter

FEATURES

- **Guaranteed 24-Bits No Missing Codes**
- **±0.5ppm INL (Typ)**
- **Integrated Digital Filter with Real-Time Averaging**
- **Low Power: 21mW at 1Msps**
- **98dB SNR (Typ) at 1Msps**
- **140dB Dynamic Range (Typ) at 15.25sps**
- **–116dB THD (Typ) at f_{IN} = 2kHz**
- **50Hz/60Hz Rejection**
- Guaranteed Operation to 85°C
- Single 2.5V Supply
- Pseudo-Differential Unipolar Input Range: 0V to V_{REF}
- 1.8V to 5V SPI-Compatible Serial I/O with Daisy-Chain Mode
- 16-Lead MSOP and 4mm × 3mm DFN Packages

APPLICATIONS

- Seismology
- Energy Exploration
- Medical Imaging
- High Speed Data Acquisition
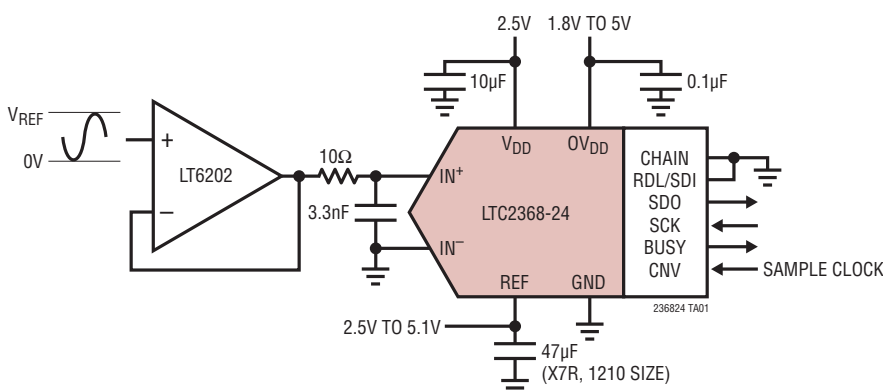- Industrial Process Control
- ATE

DESCRIPTION

The LTC®2368-24 is a low noise, low power, high speed 24-bit successive approximation register (SAR) ADC with an integrated digital averaging filter. Operating from a 2.5V supply, the LTC2368-24 has a 0V to V_{REF} pseudo-differential unipolar input range with V_{REF} ranging from 2.5V to 5.1V. The LTC2368-24 consumes only 21mW (Typ) and achieves ±4.5ppm INL maximum and no missing codes at 24 bits.

The LTC2368-24 has an easy to use integrated digital averaging filter that can average 1 to 65536 conversion results real-time, dramatically improving dynamic range from 98dB at 1Msps to 140dB at 15.25sps. No separate programming interface or configuration register is required.
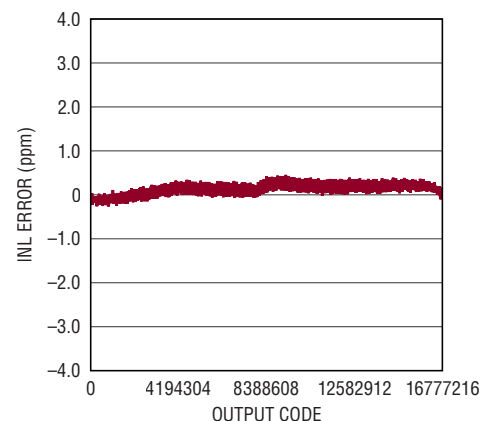
The high speed SPI-compatible serial interface supports 1.8V, 2.5V, 3.3V and 5V logic while also featuring a daisy-chain mode. The LTC2368-24 automatically powers down between conversions, reducing power dissipation at lower sampling rates.

TYPICAL APPLICATION

Integral Nonlinearity vs Output Code

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage (V_{DD}) 2.8V
Supply Voltage (OV_{DD}) 6V
Reference Input (REF)...6V
Analog Input Voltage (Note 3)
IN^+, IN^- ....(GND – 0.3V) to (REF + 0.3V)
Digital Input Voltage
(Note 3)......................... (GND – 0.3V) to (OV_{DD} + 0.3V)

Digital Output Voltage
(Note 3)......................... (GND – 0.3V) to (OV_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
  LTC2368C..0°C to 70°C
  LTC2368I ....−40°C to 85°C
Storage Temperature Range ....−65°C to 150°C

PIN CONFIGURATION

TOP VIEW

```
CHAIN  1          16  GND
VDD    2          15  OVDD
GND    3          14  SDO
IN+    4    17    13  SCK
IN−    5    GND   12  RDL/SDI
GND    6          11  BUSY
REF    7          10  GND
REF    8           9  CNV
```

DE PACKAGE
16-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

TOP VIEW

```
CHAIN  1          16  GND
VDD    2          15  OVDD
GND    3          14  SDO
IN+    4          13  SCK
IN−    5          12  RDL/SDI
GND    6          11  BUSY
REF    7          10  GND
REF    8           9  CNV
```

MS PACKAGE
16-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 110°C/W
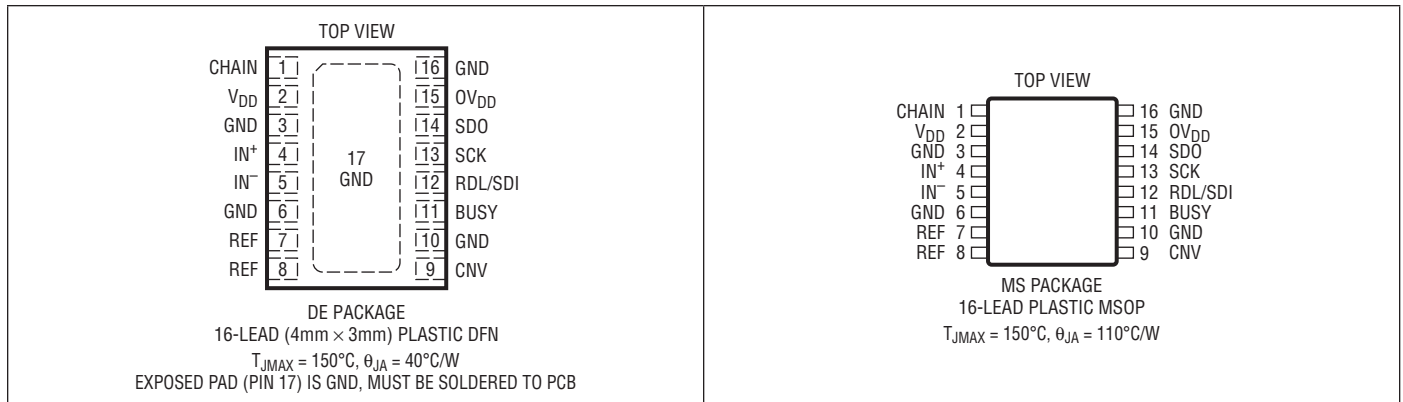
ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2368CMS-24#PBF	LTC2368CMS-24#TRPBF	236824	16-Lead Plastic MSOP	0°C to 70°C
LTC2368IMS-24#PBF	LTC2368IMS-24#TRPBF	236824	16-Lead Plastic MSOP	−40°C to 85°C
LTC2368CDE-24#PBF	LTC2368CDE-24#TRPBF	23684	16-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2368IDE-24#PBF	LTC2368IDE-24#TRPBF	23684	16-Lead (4mm × 3mm) Plastic DFN	−40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

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ELECTRICAL CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}^+	Absolute Input Range (IN⁺)	(Note 5)	●	–0.1		V_{REF} + 0.1	V
V_{IN}^-	Absolute Input Range (IN⁻)	(Note 5)	●	–0.1		0.1	V
$V_{IN}^+ - V_{IN}^-$	Input Differential Voltage Range	$V_{IN} = V_{IN}^+ - V_{IN}^-$	●	0		V_{REF}	V
I_{IN}	Analog Input Leakage Current				0.01		μA
C_{IN}	Analog Input Capacitance	Sample Mode Hold Mode			45 5		pF pF
CMRR	Input Common Mode Rejection Ratio	f_{IN} = 500kHz			83		dB

CONVERTER CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	24			Bits
	No Missing Codes		●	24			Bits
N	Number of Averages		●	1		65536	
	Transition Noise	N = 1 N = 16 N = 1024 N = 16384	● ● ● ●		68.5 16.8 2.24 0.87		LSB_RMS LSB_RMS LSB_RMS LSB_RMS
INL	Integral Linearity Error	(Note 6)	●	–4.5	±0.5	4.5	ppm
DNL	Differential Linearity Error	(Note 7)	●	–0.9	±0.4	0.9	LSB
ZSE	Zero-Scale Error	(Note 8)	●	–20	0	20	ppm
	Zero-Scale Error Drift				±0.7		ppb/°C
FSE	Full-Scale Error	(Note 8)	●	–100	±10	100	ppm
	Full-Scale Error Drift				±0.05		ppm/°C

DYNAMIC ACCURACY
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and A_{IN} = –1dBFS. (Notes 4, 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DR	Dynamic Range	IN⁺ = IN⁻ = GND, V_{REF} = 5V, N = 1 IN⁺ = IN⁻ = GND, V_{REF} = 5V, N = 16 IN⁺ = IN⁻ = GND, V_{REF} = 5V, N = 1024 IN⁺ = IN⁻ = GND, V_{REF} = 5V, N = 16384 IN⁺ = IN⁻ = GND, V_{REF} = 5V, N = 65536			98 110 128 138 140		dB dB dB dB dB
SINAD	Signal-to-(Noise + Distortion) Ratio	f_{IN} = 2kHz, V_{REF} = 5V	●	95.5	98		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 2kHz, V_{REF} = 5V f_{IN} = 2kHz, V_{REF} = 2.5V f_{IN} = 2kHz, V_{REF} = 5V, N = 16, A_{IN} = –20dBFS f_{IN} = 50Hz, V_{REF} = 5V, N = 1024, A_{IN} = –20dBFS	● ●	95.5 90	98 92.3 110 124		dB dB dB dB
THD	Total Harmonic Distortion	f_{IN} = 2kHz, V_{REF} = 5V f_{IN} = 2kHz, V_{REF} = 2.5V f_{IN} = 2kHz, V_{REF} = 5V, N = 16, A_{IN} = –20dBFS f_{IN} = 50Hz, V_{REF} = 5V, N = 1024, A_{IN} = –20dBFS	● ●		–116 –116 –116 –116	–103 –103	dB dB dB dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 2kHz, V_{REF} = 5V	●	103	116		dB
	–3dB Input Linear Bandwidth				34		MHz

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DYNAMIC ACCURACY
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$ and $A_{IN} = −1dBFS$. (Notes 4, 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Aperture Delay				500		ps
	Aperture Jitter				4		ps_{RMS}
	Transient Response	Full–Scale Step			312		ns

REFERENCE INPUT
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	(Note 5)	●	2.5		5.1	V
I_{REF}	Reference Input Current	(Note 10)	●		0.45	0.6	mA

DIGITAL INPUTS AND DIGITAL OUTPUTS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	$0.8 • OV_{DD}$			V
V_{IL}	Low Level Input Voltage		●			$0.2 • OV_{DD}$	V
I_{IN}	Digital Input Current	$V_{IN} = 0V$ to OV_{DD}	●	−10		10	μA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	$I_O = −500μA$	●	$OV_{DD} − 0.2$			V
V_{OL}	Low Level Output Voltage	$I_O = 500μA$	●			0.2	V
I_{OZ}	Hi-Z Output Leakage Current	$V_{OUT} = 0V$ to OV_{DD}	●	−10		10	μA
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$			−10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = OV_{DD}$			10		mA

POWER REQUIREMENTS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		●	2.375	2.5	2.625	V
OV_{DD}	Supply Voltage		●	1.71		5.25	V
I_{VDD}	Supply Current		●		8.4	10	mA
I_{OVDD}	Supply Current	$(C_L = 20pF)$			0.4		mA
I_{PD}	Power Down Mode	Conversion Done $(I_{VDD} + I_{OVDD} + I_{REF})$	●		1	90	μA
P_D	Power Dissipation		●		21	25	mW
	Power Down Mode	Conversion Done $(I_{VDD} + I_{OVDD} + I_{REF})$	●		2.5	225	μW

ADC TIMING CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SMPL}	Maximum Sampling Frequency		●			1	Msps
f_{ODR}	Output Data Rate		●			1	Msps
t_{CONV}	Conversion Time		●	615		675	ns

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ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	$t_{ACQ} = t_{CYC} - t_{CONV} - t_{BUSYLH}$ (Note 7)	●	312			ns
t_{CYC}	Time Between Conversions		●	1			µs
t_{CNVH}	CNV High Time		●	20			ns
t_{CNVL}	Minimum Low Time for CNV	(Note 11)	●	20			ns
t_{BUSYLH}	CNV↑ to BUSY↑ Delay	C_L = 20pF	●			13	ns
t_{QUIET}	SCK Quiet Time from CNV↑	(Note 7)	●	10			ns
t_{SCK}	SCK Period	(Notes 11, 12)	●	10			ns
t_{SCKH}	SCK High Time		●	4			ns
t_{SCKL}	SCK Low Time		●	4			ns
$t_{SSDISCK}$	SDI Setup Time From SCK↑	(Note 11)	●	4			ns
$t_{HSDISCK}$	SDI Hold Time From SCK↑	(Note 11)	●	1			ns
t_{SCKCH}	SCK Period in Chain Mode	$t_{SCKCH} = t_{SSDISCK} + t_{DSDO}$ (Note 11)	●	13.5			ns
t_{DSDO}	SDO Data Valid Delay from SCK↑	C_L = 20pF, OV_{DD} = 5.25V C_L = 20pF, OV_{DD} = 2.5V C_L = 20pF, OV_{DD} = 1.71V	● ● ●			7.5 8 9.5	ns ns ns
t_{HSDO}	SDO Data Remains Valid Delay from SCK↑	C_L = 20pF (Note 7)	●	1			ns
$t_{DSDOBUSYL}$	SDO Data Valid Delay from BUSY↓	C_L = 20pF (Note 7)	●			5	ns
t_{EN}	Bus Enable Time After RDL↓	(Note 11)	●			16	ns
t_{DIS}	Bus Relinquish Time After RDL↑	(Note 11)	●			13	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground.

Note 3: When these pin voltages are taken below ground or above REF or OV_{DD}, they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground or above REF or OV_{DD} without latchup.

Note 4: V_{DD} = 2.5V, OV_{DD} = 2.5V, REF = 5V, f_{SMPL} = 1MHz, N = 1.

Note 5: Recommended operating conditions.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Guaranteed by design, not subject to test.

Note 8: Zero-scale error is the offset voltage measured from 0.5LSB when the output code flickers between 0000 0000 0000 0000 0000 0000 and 0000 0000 0000 0000 0000 0001. Full-scale error is the deviation of the last code transition from ideal and includes the effect of offset error.

Note 9: All specifications in dB are referred to a full-scale 5V input with a 5V reference voltage, unless otherwise specified.

Note 10: f_{SMPL} = 1MHz, I_{REF} varies proportionally with sample rate.

Note 11: Parameter tested and guaranteed at OV_{DD} = 1.71V, OV_{DD} = 2.5V and OV_{DD} = 5.25V.

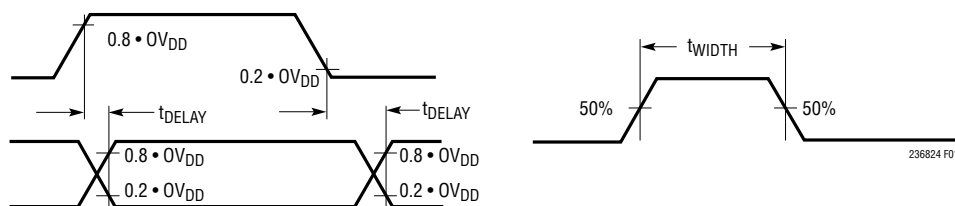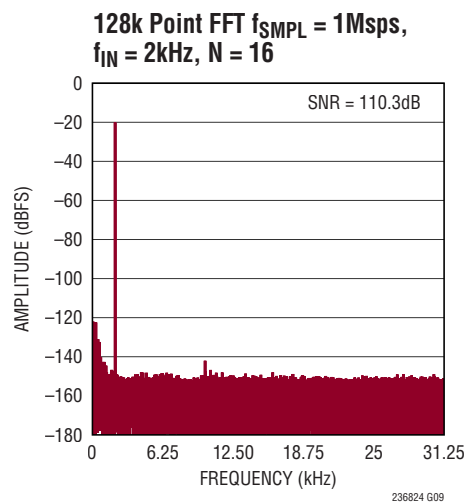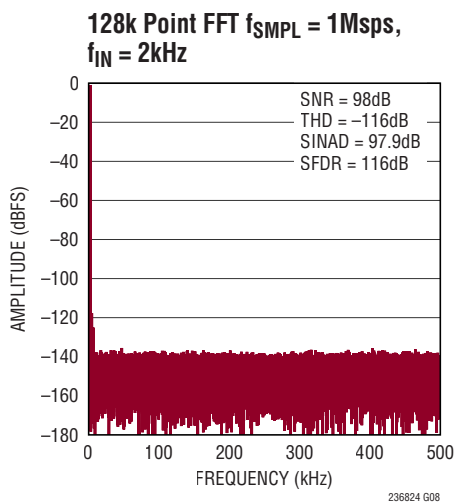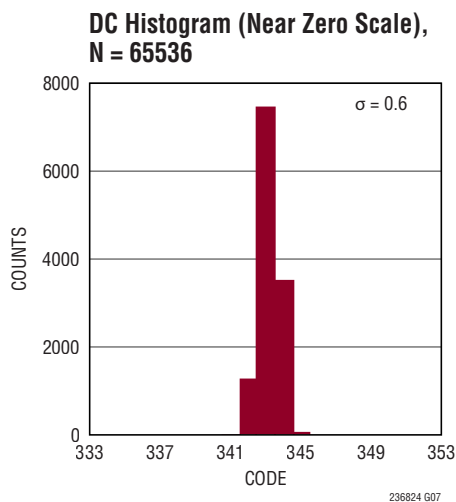**Note 12:** t_{SCK} of 10ns maximum allows a shift clock frequency up to 100MHz for rising edge capture.
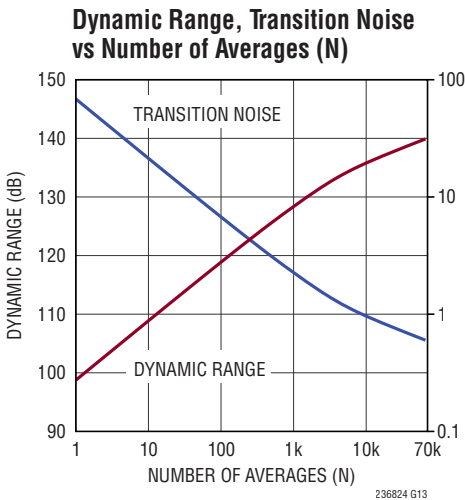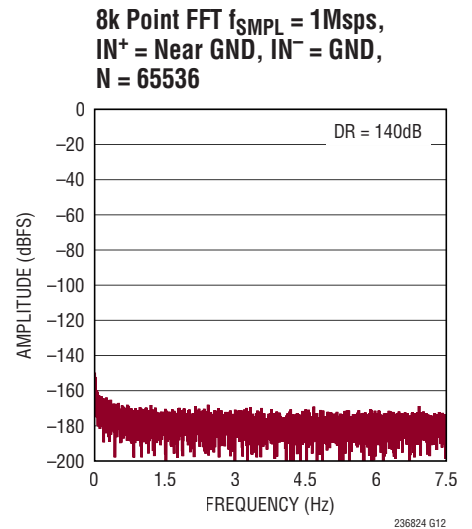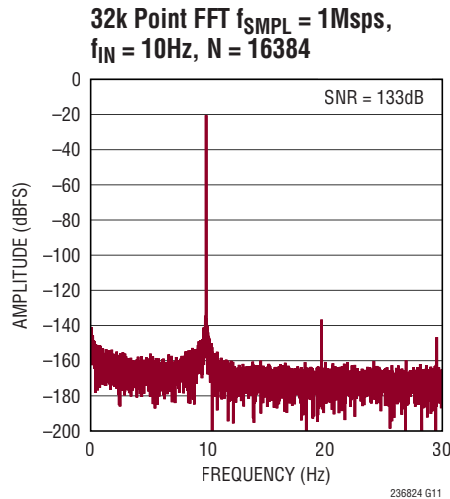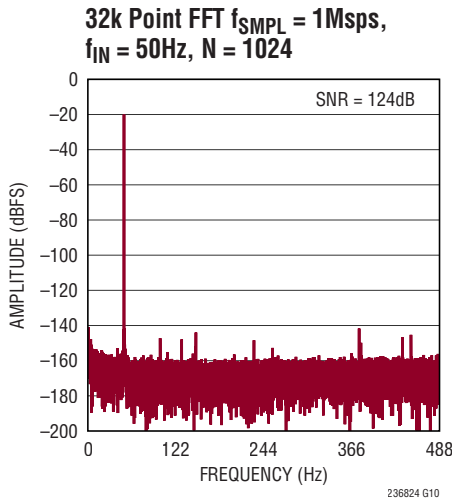

Figure 1. Voltage Levels for Timing Specifications

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, $V_{DD} = 2.5V$, $OV_{DD} = 2.5V$, REF = 5V, $f_{SMPL} = 1Msps$, N = 1, unless otherwise noted.

Integral Nonlinearity vs Output Code

236824 G01

Differential Nonlinearity vs Output Code

236824 G02

DC Histogram (Near Zero Scale), N = 1

$\sigma = 68.5$

236824 G03

DC Histogram (Near Zero Scale), N = 16

$\sigma = 16.8$

236824 G04

DC Histogram (Near Zero Scale), N = 1024

$\sigma = 2.24$

236824 G05

DC Histogram (Near Zero Scale), N = 16384

$\sigma = 0.87$

236824 G06

DC Histogram (Near Zero Scale), N = 65536

$\sigma = 0.6$

236824 G07

128k Point FFT $f_{SMPL} = 1Msps$, $f_{IN} = 2kHz$

SNR = 98dB
THD = −116dB
SINAD = 97.9dB
SFDR = 116dB

236824 G08

128k Point FFT $f_{SMPL} = 1Msps$, $f_{IN} = 2kHz$, N = 16

SNR = 110.3dB

236824 G09

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TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_{DD} = 2.5V$, $OV_{DD} = 2.5V$, REF = 5V, $f_{SMPL} = 1Msps$, N = 1, unless otherwise noted.

32k Point FFT $f_{SMPL} = 1Msps$, $f_{IN} = 50Hz$, N = 1024

SNR = 124dB

236824 G10

32k Point FFT $f_{SMPL} = 1Msps$, $f_{IN} = 10Hz$, N = 16384

SNR = 133dB

236824 G11

8k Point FFT $f_{SMPL} = 1Msps$, IN⁺ = Near GND, IN⁻ = GND, N = 65536

DR = 140dB

236824 G12

Dynamic Range, Transition Noise vs Number of Averages (N)

236824 G13

SNR, SINAD vs Input Frequency

236824 G14

THD, Harmonics vs Input Frequency

236824 G15

SNR, SINAD vs Input level, $f_{IN} = 2kHz$

236824 G16

SNR, SINAD vs Reference Voltage, $f_{IN} = 2kHz$

236824 G17

THD, Harmonics vs Reference Voltage, $f_{IN} = 2kHz$

236824 G18

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TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_{DD} = 2.5V$, $OV_{DD} = 2.5V$, $REF = 5V$, $f_{SMPL} = 1Msps$, $N = 1$, unless otherwise noted.
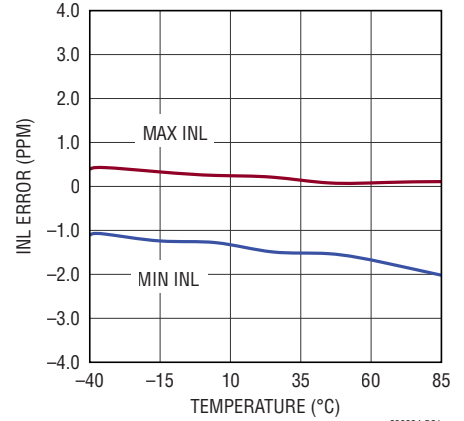
SNR, SINAD vs Temperature, $f_{IN} = 2kHz$
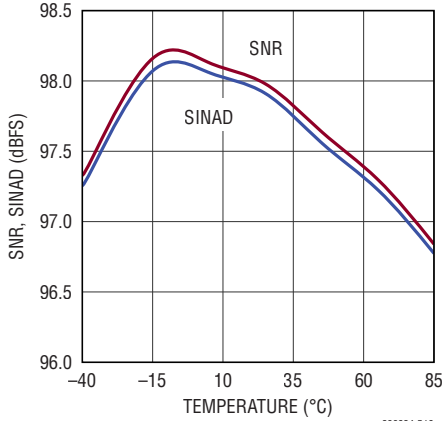
236824 G19

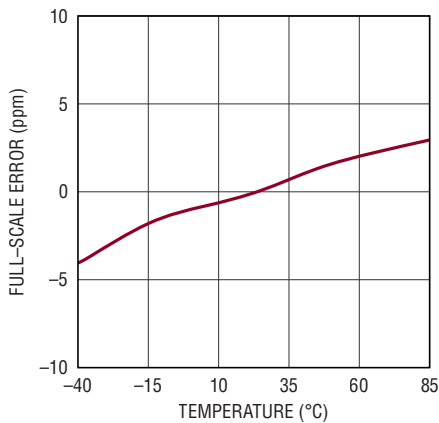**THD, Harmonics vs Temperature, $f_{IN} = 2kHz$**
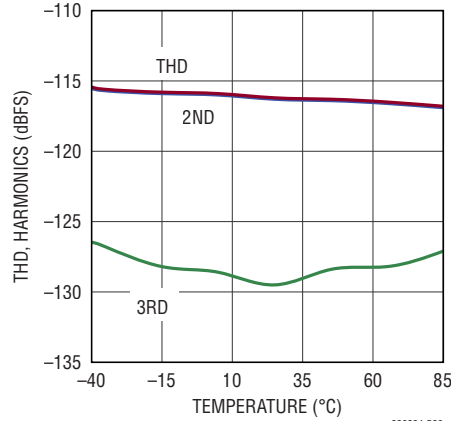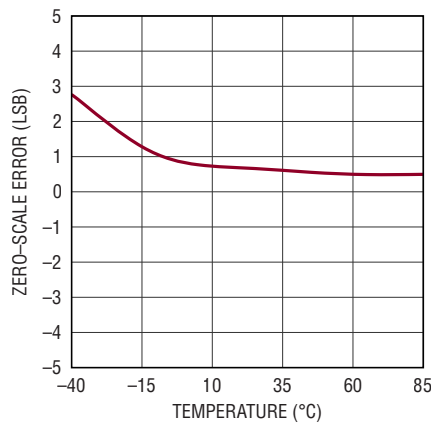
236824 G20

INL vs Temperature

236824 G21

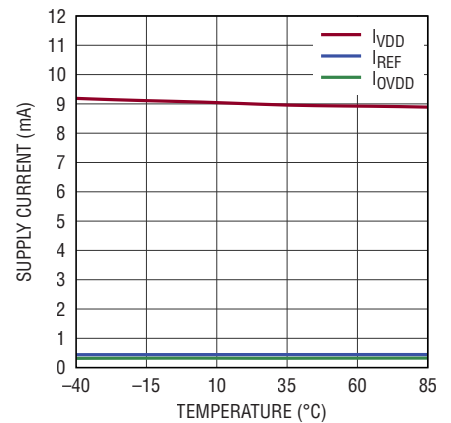**Full-Scale Error vs Temperature**

236824 G22

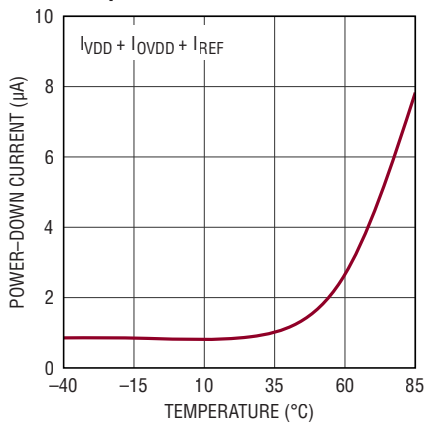**Zero-Scale Error vs Temperature**

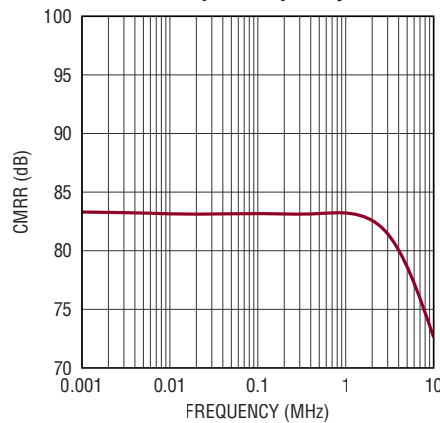236824 G23

Supply Current vs Temperature
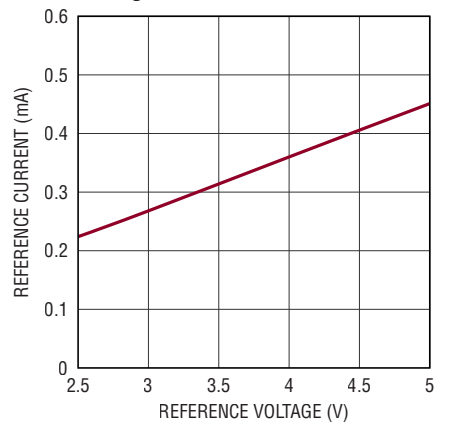
236824 G24

Power-Down Current vs Temperature

236824 G25

CMRR vs Input Frequency

236824 G26

Reference Current vs Reference Voltage

236824 G27

236824f

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PIN FUNCTIONS

CHAIN (Pin 1): Chain Mode Selector Pin. When low, the LTC2368-24 operates in normal mode and the RDL/SDI input pin functions to enable or disable SDO. When high, the LTC2368-24 operates in chain mode and the RDL/SDI pin functions as SDI, the daisy-chain serial data input. Logic levels are determined by OV_{DD}.

V_{DD} (Pin 2): 2.5V Power Supply. The range of V_{DD} is 2.375V to 2.625V. Bypass V_{DD} to GND with a 10µF ceramic capacitor.

GND (Pins 3, 6, 10 and 16): Ground.

IN$^+$ (Pin 4): Analog Input. IN$^+$ operates differential with respect to IN$^-$ with an IN$^+$ to IN$^-$ range of 0V to V_{REF}.

IN$^-$ (Pin 5): Analog Ground Sense. IN$^-$ has an input range of ±100mV with respect to GND and must be tied to the ground plane or a remote ground sense.

REF (Pins 7, 8): Reference Input. The range of REF is 2.5V to 5.1V. This pin is referred to the GND pin and should be decoupled closely to the pin with a 47µF ceramic capacitor (X7R, 1210 size, 10V rating).

CNV (Pin 9): Convert Input. A rising edge on this input powers up the part and initiates a new conversion. Logic levels are determined by OV_{DD}.

BUSY (Pin 11): BUSY Indicator. Goes high at the start of a new conversion and returns low when the conversion has finished. Logic levels are determined by OV_{DD}.

RDL/SDI (Pin 12): Bus Enabling Input/Serial Data Input Pin. This pin serves two functions depending on whether the part is operating in normal mode (CHAIN pin low) or chain mode(CHAIN pin high). In normal mode, RDL/SDI is a bus enabling input for the serial data I/O bus. When RDL/SDI is low in normal mode, data is read out of the ADC on the SDO pin. When RDL/SDI is high in normal mode, SDO becomes Hi-Z and SCK is disabled. In chain mode, RDL/SDI acts as a serial data input pin where data from another ADC in the daisy chain is input. Logic levels are determined by OV_{DD}.

SCK (Pin 13): Serial Data Clock Input. When SDO is enabled, the conversion result or daisy-chain data from another ADC is shifted out on the rising edges of this clock MSB first. Logic levels are determined by OV_{DD}.

SDO (Pin 14): Serial Data Output. The conversion result or daisy-chain data is output on this pin on each rising edge of SCK MSB first. The output data is in straight binary format. Logic levels are determined by OV_{DD}.

OV_{DD} (Pin 15): I/O Interface Digital Power. The range of OV_{DD} is 1.71V to 5.25V. This supply is nominally set to the same supply as the host interface (1.8V, 2.5V, 3.3V, or 5V). Bypass OV_{DD} to GND with a 0.1µF capacitor.
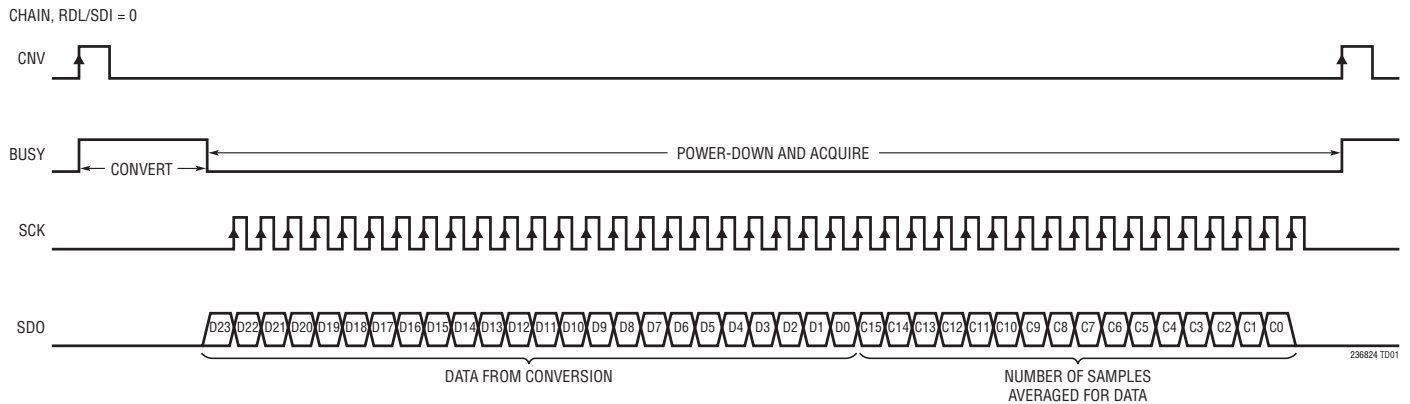
GND (Exposed Pad Pin 17 – DFN Package Only): Ground. Exposed pad must be soldered directly to the ground plane.

FUNCTIONAL BLOCK DIAGRAM
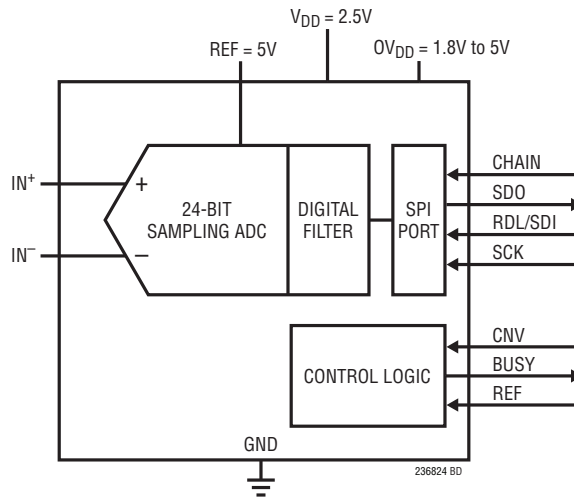
TIMING DIAGRAM

Conversion Timing Using the Serial Interface

CHAIN, RDL/SDI = 0

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OVERVIEW

The LTC2368-24 is a low noise, low power, high speed 24-bit successive approximation register (SAR) ADC with an integrated digital averaging filter. Operating from a 2.5V supply, the LTC2368-24 has a 0V to V_{REF} pseudo-differential unipolar input range with V_{REF} ranging from 2.5V to 5.1V. The LTC2368-24 consumes only 21mW (Typ) and achieves ±4.5ppm INL maximum and no missing codes at 24 bits.

The LTC2368-24 has an easy to use integrated digital averaging filter that can average 1 to 65536 conversion results real-time, dramatically improving dynamic range from 98dB at 1Msps to 140dB at 15.25sps. No separate programming interface or configuration register is required.

The high speed SPI-compatible serial interface supports 1.8V, 2.5V, 3.3V and 5V logic while also featuring a daisy-chain mode. The LTC2368-24 automatically powers down between conversions, reducing power dissipation at lower sampling rates.

CONVERTER OPERATION

The LTC2368-24 operates in two phases. During the acquisition phase, the charge redistribution capacitor D/A converter (CDAC) is connected to the IN$^+$ and IN$^-$ pins to sample the differential analog input voltage. A rising edge on the CNV pin initiates a conversion. During the conversion phase, the 24-bit CDAC is sequenced through a successive approximation algorithm, effectively comparing the sampled input with binary-weighted fractions of the reference voltage (e.g. $V_{REF}/2$, $V_{REF}/4 \ldots V_{REF}/16777216$) using the differential comparator. At the end of conversion, the CDAC output approximates the sampled analog input. The ADC control logic then passes the 24-bit digital output code to the digital filter for further processing.

TRANSFER FUNCTION

The LTC2368-24 digitizes the full-scale voltage of REF into 2^{24} levels, resulting in an LSB size of 0.3µV with REF = 5V. The ideal transfer function is shown in Figure 2. The output data is in straight binary format.
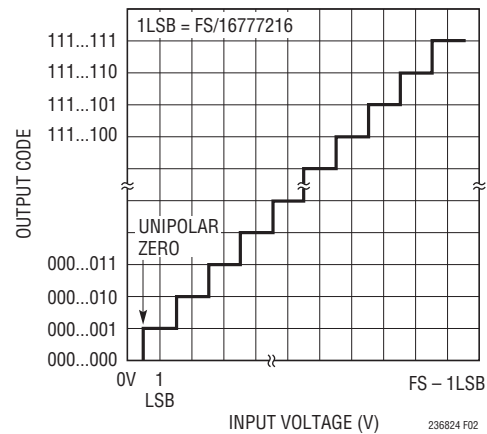

Figure 2. LTC2368-24 Transfer Function

ANALOG INPUT

The analog inputs of the LTC2368-24 are pseudo-differential in order to reduce any unwanted signal that is common to both inputs. The analog inputs can be modeled by the equivalent circuit shown in Figure 3. The diodes at the input provide ESD protection. In the acquisition phase, each input sees approximately 45pF (C_{IN}) from the sampling CDAC in series with 40Ω (R_{ON}) from the on-resistance of the sampling switch. Any unwanted signal that is common to both inputs will be reduced by the common mode rejection of the ADC. The inputs draw a current spike while charging the C_{IN} capacitors during acquisition. During conversion, the analog inputs draw only a small leakage current.
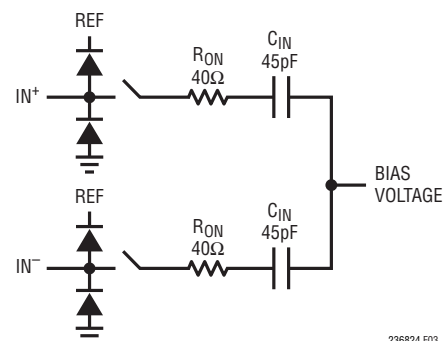

Figure 3. The Equivalent Circuit for the Pseudo-Differential Unipolar Analog Input of the LTC2368-24

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INPUT DRIVE CIRCUITS

A low impedance source can directly drive the high impedance inputs of the LTC2368-24 without gain error. A high impedance source should be buffered to minimize settling time during acquisition and to optimize ADC linearity. For best performance, a buffer amplifier should be used to drive the analog inputs of the LTC2368-24. The amplifier provides low output impedance, which produces fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the ADC input currents.

Noise and Distortion

The noise and distortion of the buffer amplifier and signal source must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the buffer amplifier input with an appropriate filter to minimize noise. The simple 1-pole RC lowpass filter (LPF1) shown in Figure 4 is sufficient for many applications.
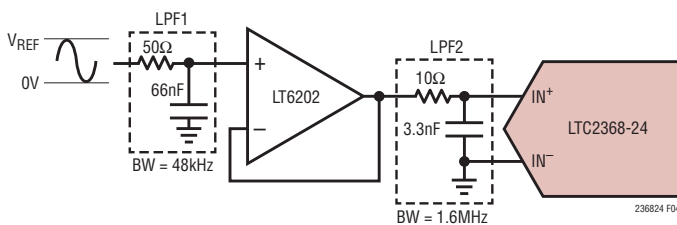

Figure 4. Input Signal Chain

A coupling filter network (LPF2) should be used between the buffer and ADC input to minimize disturbances reflected into the buffer from sampling transients. Long RC time constants at the analog inputs will slow down the settling of the analog inputs. Therefore, LPF2 typically requires a wider bandwidth than LPF1. This filter also helps minimize the noise contribution from the buffer. A buffer amplifier with a low noise density must be selected to minimize degradation of the SNR.

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NP0 and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Input Currents

One of the biggest challenges in coupling an amplifier to the LTC2368-24 is in dealing with current spikes drawn by the ADC inputs at the start of each acquisition phase. The ADC inputs may be modeled as a switched capacitor load of the drive circuit. A drive circuit may rely partially on attenuating switched-capacitor current spikes with small filter capacitors C_{FILT} placed directly at the ADC inputs, and partially on the driver amplifier having sufficient bandwidth to recover from the residual disturbance. Amplifiers optimized for DC performance may not have sufficient bandwidth to fully recover at the ADC's maximum conversion rate, which can produce nonlinearity and other errors. Coupling filter circuits may be classified in three broad categories:

Fully Settled – This case is characterized by filter time constants and an overall settling time that is considerably shorter than the sample period. When acquisition begins, the coupling filter is disturbed. For a typical first order RC filter, the disturbance will look like an initial step with an exponential decay. The amplifier will have its own response to the disturbance, which may include ringing. If the input settles completely (to within the accuracy of the LTC2368-24), the disturbance will not contribute any error.

Partially Settled – In this case, the beginning of acquisition causes a disturbance of the coupling filter, which then begins to settle out towards the nominal input voltage. However, acquisition ends (and the conversion begins) before the input settles to its final value. This generally produces a gain error, but as long as the settling is linear, no distortion is produced. The coupling filter's response is affected by the amplifier's output impedance and other parameters. A linear settling response to fast switched-capacitor current spikes can NOT always be assumed for precision, low bandwidth amplifiers. The coupling filter serves to attenuate the current spikes' high-frequency energy before it reaches the amplifier.

Fully Averaged – If the coupling filter capacitors (C_{FILT}) at the ADC inputs are much larger than the ADC's sample capacitors (45pF), then the sampling glitch is greatly attenuated. The driving amplifier effectively only sees the average sampling current, which is quite small. At 1Msps, the equivalent input resistance is approximately 22k (as

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shown in Figure 5), a benign resistive load for most precision amplifiers. However, resistive voltage division will occur between the coupling filter's DC resistance and the ADC's equivalent (switched-capacitor) input resistance, thus producing a gain error.
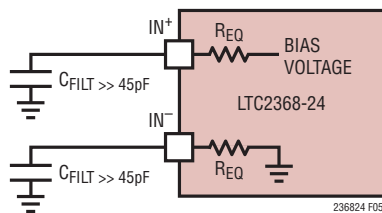
$$R_{EQ} = \frac{1}{f_{SMPL} \cdot 45pF}$$

Figure 5. Equivalent Circuit for the Pseudo-Differential Unipolar Analog Input of the LTC2368-24 at 1Msps

The input leakage currents of the LTC2368-24 should also be considered when designing the input drive circuit, because source impedances will convert input leakage currents to an added input voltage error. The input leakage currents, both common mode and differential, are typically extremely small over the entire operating temperature range. Figure 6 shows input leakage currents over temperature for a typical part.
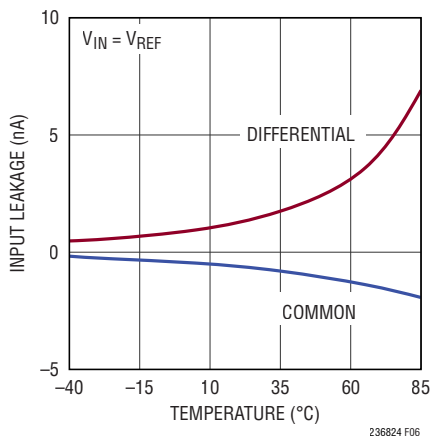

Figure 6. Common Mode and Differential Input Leakage Current over Temperature

Let R_{S1} and R_{S2} be the source impedances of the input drive circuit shown in Figure 7, and let I_{L1} and I_{L2} be the leakage currents flowing out of the ADC's analog inputs. The voltage error, V_E, due to the leakage currents can be expressed as:

$$V_E = \frac{R_{S1}+R_{S2}}{2} \cdot (I_{L1}-I_{L2}) + (R_{S1}-R_{S2}) \cdot \frac{I_{L1}+I_{L2}}{2}$$

The common mode input leakage current, $(I_{L1} + I_{L2})/2$, is typically extremely small (Figure 6) over the entire operating temperature range and common mode input voltage range. Thus, any reasonable mismatch (below 5%) of the source impedances R_{S1} and R_{S2} will cause only a negligible error. The differential input leakage current, $(I_{L1} - I_{L2})$, increases with temperature as shown in Figure 6 and is maximum when $V_{IN} = V_{REF}$. The differential leakage current is also typically very small, and its nonlinear component is even smaller. Only the nonlinear component will impact the ADC's linearity.
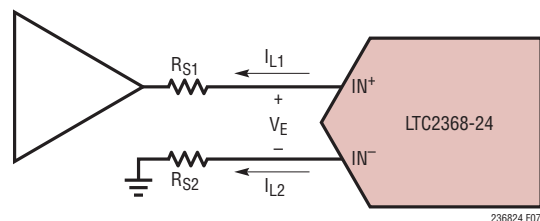
Figure 7. Source Impedances and Input Leakage Currents of the LTC2368-24

For optimal performance, it is recommended that the source impedances, R_{S1} and R_{S2}, be between 5Ω and 50Ω and with 1% tolerance. For source impedances in this range, the voltage and temperature coefficients of R_{S1} and R_{S2} are usually not critical. The guaranteed AC and DC specifications are tested with 10Ω source impedances, and the specifications will gradually degrade with increased source impedances due to incomplete settling of the inputs.

Low Side Current Sensing

Figure 8 shows a typical low side current sense application where a sense resistor, R_{SENSE}, is placed in series with the ground terminal of a circuit block to produce a voltage, V_{SENSE}, that is amplified and buffered before being presented to the ADC input. V_{SENSE} is inherently unipolar with respect to ground, making the pseudo-differential unipolar input range of the LTC2368-24 ideally suited for low side current sense applications.
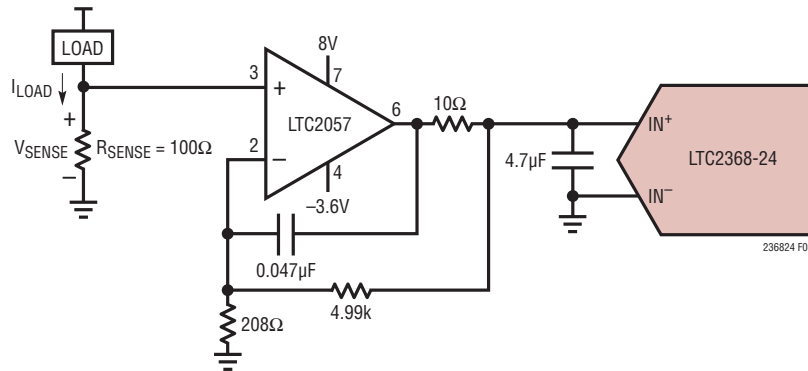
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Figure 8. Low Side Current Sensing

The LTC2057 is a high precision, zero drift amplifier that complements the low offset and offset drift of the LTC2368-24. The LTC2057 is shown in a non-inverting amplifier configuration to provide a gain of 25 to V_{SENSE}. Low noise is achieved using the digital averaging filter provided by the LTC2368-24.

DC Accuracy

The very low level of distortion is a direct consequence of the excellent INL of the LTC2368-24, and this property can be exploited in DC applications. Note that while the driver amplifier in Figure 4 (LT6202) is characterized by excellent AC specifications, its DC specifications do not match those of the LTC2368-24. The offset of this amplifier, for example, is more than 500μV under certain conditions. In contrast, the LTC2368-24 has a guaranteed maximum offset error of 130μV (typical drift ±0.007ppm/°C), and a guaranteed maximum full-scale error of 150ppm (typical drift ±0.05ppm/°C). Low drift is important to maintain accuracy over wide temperature range in a calibrated system. The LTC2057 shown in Figure 8 is an example of an amplifier with low offset and offset drift.

Amplifiers have to be selected very carefully to provide a 24-bit accurate DC signal chain. A large-signal open-loop gain of at least 126dB may be required to ensure 1ppm linearity for amplifiers configured for a gain of negative 1. However, less gain is sufficient if the amplifier's gain characteristic is known to be (mostly) linear. An amplifier's offset versus signal level must be considered for amplifiers configured as unity gain buffers. For example, 1ppm linearity may require that the offset is known to

vary less than 5μV for a 5V swing. However, greater offset variations may be acceptable if the relationship is known to be (mostly) linear. Unity-gain buffer amplifiers typically require substantial headroom to the power supply rails for best performance. Inverting amplifier circuits configured to minimize swing at the amplifier input terminals may perform better with less headroom than unity-gain buffer amplifiers. The linearity and thermal properties of an inverting amplifier's feedback network should be considered carefully to ensure DC accuracy.

ADC REFERENCE

The LTC2368-24 requires an external reference to define its input range. A low noise, low temperature drift reference is critical to achieving the full data sheet performance of the ADC. Linear Technology offers a portfolio of high performance references designed to meet the needs of many applications. With its small size, low power and high accuracy, the LTC6655-5 is particularly well suited for use with the LTC2368-24. The LTC6655-5 offers 0.025% (max) initial accuracy and 2ppm/°C (max) temperature coefficient for high precision applications.

When choosing a bypass capacitor for the LTC6655-5, the capacitor's voltage rating, temperature rating, and package size should be carefully considered. Physically larger capacitors with higher voltage and temperature ratings tend to provide a larger effective capacitance, better filtering the noise of the LTC6655-5, and consequently producing a higher SNR. Therefore, we recommend bypassing the LTC6655-5 with a 47μF ceramic capacitor (X7R, 1210 size, 10V rating) close to the REF pin.

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The REF pin of the LTC2368-24 draws charge (Q_{CONV}) from the 47µF bypass capacitor during each conversion cycle. The reference replenishes this charge with a DC current, $I_{REF} = Q_{CONV}/t_{CYC}$. The DC current draw of the REF pin, I_{REF}, depends on the sampling rate and output code. If the LTC2368-24 is used to continuously sample a signal at a constant rate, the LTC6655-5 will keep the deviation of the reference voltage over the entire code span to less than 0.5ppm.

When idling, the REF pin on the LTC2368-24 draws only a small leakage current (< 1µA). In applications where a burst of samples is taken after idling for long periods as shown in Figure 9, I_{REF} quickly goes from approximately 0µA to a maximum of 1mA at 1Msps. This step in DC current draw triggers a transient response in the reference that must be considered since any deviation in the reference output voltage will affect the accuracy of the output code. In applications where the transient response of the reference is important, the fast settling LTC6655-5 reference is also recommended.

In applications where power management is critical, the external reference may be powered down such that the voltage on the REF pin can go below 2V. In such scenarios, it is recommended that after the voltage on the REF pin recovers to above 2V, the ADC's internal digital I/O registers be cleared before the initiation of the next conversion. This can be achieved by providing at least 20 rising edges on the SCK pin before the first CNV rising edge.

Reference Noise

The dynamic range of the ADC will increase approximately 3dB for every 2× increase in the number of conversion results averaged (N). The SNR should also improve as a function of N in the same manner. For large input signals near full-scale, however, any reference noise will limit the improvement of the SNR as N increases, because any noise on the REF pin will modulate around the fundamental frequency of the input signal. Therefore, it is critical to use a low-noise reference, especially if the input signal amplitude approaches full-scale. For small input signals, the dynamic range will improve as described earlier in this section.

DYNAMIC PERFORMANCE

Fast Fourier Transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2368-24 provides guaranteed tested limits for both AC distortion and noise measurements.

Dynamic Range

The dynamic range is the ratio of the RMS value of a full scale input to the total RMS noise measured with IN⁺ tied to a DC voltage near GND and IN⁻ shorted to GND. The dynamic range of the LTC2368-24 without averaging (N = 1) is 98dB which improves by 3dB for every 2× increase in the number of conversion results averaged (N) per measurement.

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band-limited to frequencies from above DC and below half the sampling frequency. Figure 10 shows that the LTC2368-24 achieves a typical SINAD of 98dB at a 1MHz sampling rate with a 2kHz input.
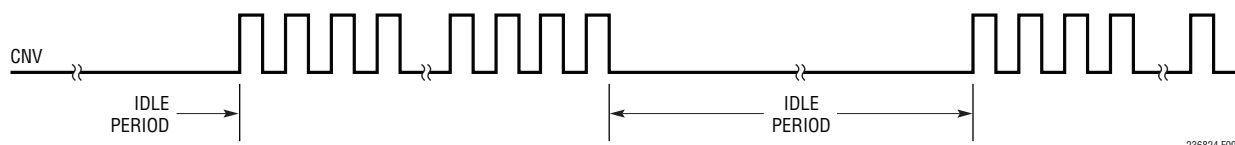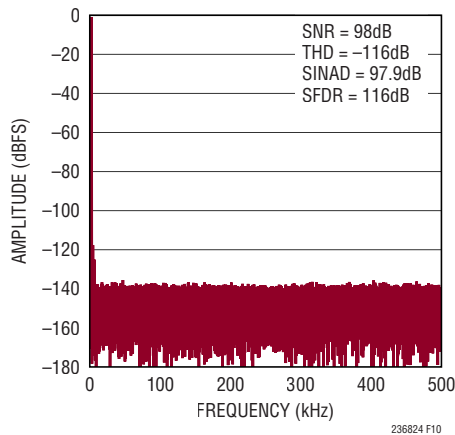

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Figure 9. CNV Waveform Showing Burst Sampling

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Figure 10. 128k Point FFT Plot of the LTC2368-24 with f_{IN} = 2kHz and f_{SMPL} = 1MHz

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 10 shows that the LTC2368-24 achieves a typical SNR of 98dB at a 1MHz sampling rate with a 2kHz input.

Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\frac{\sqrt{V2^2 + V3^2 + V4^2 + \ldots + V_N^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through V_N are the amplitudes of the second through Nth harmonics.

POWER CONSIDERATIONS

The LTC2368-24 provides two power supply pins: the 2.5V power supply (V_{DD}), and the digital input/output interface power supply (OV_{DD}). The flexible OV_{DD} supply allows the LTC2368-24 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

Power Supply Sequencing

The LTC2368-24 does not have any specific power supply sequencing requirements. Care should be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2368-24 has a power-on-reset (POR) circuit that will reset the LTC2368-24 at initial power-up or whenever the power supply voltage drops below 1V. Once the supply voltage re-enters the nominal supply voltage range, the POR will reinitialize the ADC. No conversions should be initiated until 200µs after a POR event to ensure the re-initialization period has ended. Any conversions initiated before this time will produce invalid results. In addition, after a POR event, it is recommended that the ADC's internal digital I/O registers be cleared before the initiation of the next conversion. This can be achieved by providing at least 20 rising edges on the SCK pin before the first CNV rising edge.

TIMING AND CONTROL

CNV Timing

The LTC2368-24 conversion is controlled by CNV. A rising edge on CNV will start a conversion and power up the LTC2368-24. Once a conversion has been initiated, it cannot be restarted until the conversion is complete. For optimum performance, CNV should be driven by a clean low jitter signal. Converter status is indicated by the BUSY output which remains high while the conversion is in progress. To ensure that no errors occur in the digitized results, any additional transitions on CNV should occur within 40ns from the start of the conversion or after the conversion has been completed. Once the conversion has completed, the LTC2368-24 powers down and begins acquiring the input signal.

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Internal Conversion Clock

The LTC2368-24 has an internal clock that is trimmed to achieve a maximum conversion time of 675ns. With a minimum acquisition time of 312ns, a maximum sample rate of 1Msps is guaranteed without any external adjustments.

Auto Power-Down

The LTC2368-24 automatically powers down after a conversion has been completed and powers up once a new conversion is initiated on the rising edge of CNV. During power-down, data from the last conversion can be clocked out. To minimize power dissipation during power-down, disable SDO and turn off SCK. The auto power-down feature will reduce the power dissipation of the LTC2368-24 as the sampling rate is reduced. Since power is consumed only during a conversion, the LTC2368-24 remains powered-down for a larger fraction of the conversion cycle (t_{CYC}) at lower sample rates, thereby reducing the average power dissipation which scales with the sampling rate as shown in Figure 11.
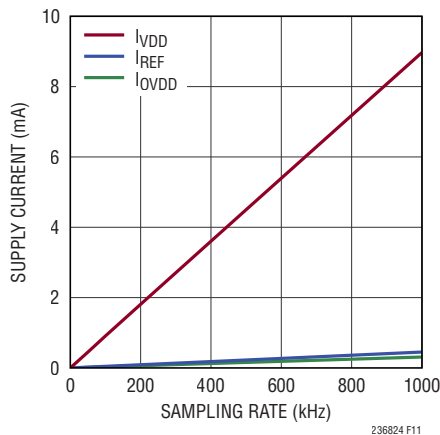
Figure 11. Power Supply Current of the LTC2368-24 Versus Sampling Rate

DIGITAL INTERFACE

The LTC2368-24 features a simple and easy to use serial digital interface that supports output data rates up to 1Msps.

The interface controls a digital averaging filter, which can be used to increase the dynamic range of measurements. The flexible OV_{DD} supply allows the LTC2368-24 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems. The digital interface of the LTC2368-24 is backwards compatible with the LTC2378-20 family.

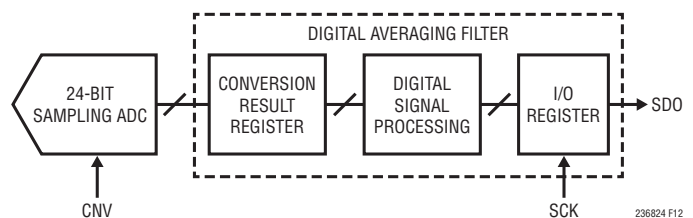**Digital Averaging Filter (SINC[1] Decimation Filter)**

Many SAR ADC applications use digital averaging techniques to reduce the uncertainty of measurements due to noise. An FPGA or DSP is typically needed to compute the average of multiple A/D conversion results. The LTC2368-24 features an integrated digital averaging filter that can provide the function without any additional hardware, thus simplifying the application solution and providing a number of unique advantages. The digital averaging filter can be used to average blocks of as few as N = 1 or as many as N = 65536 conversion results.

The digital averaging filter described in this section is also known as a SINC[1] digital decimation filter. A SINC[1] digital decimation filter is an FIR filter with N equal-valued taps.

Block Diagram

Figure 12 illustrates a block diagram of the digital averaging filter, including a Conversion Result Register, the Digital Signal Processing (DSP) block, and an I/O Register.

The Conversion Result Register holds the 24-bit conversion result from the most recent sample taken at the rising edge of CNV. The DSP block provides an averaging operation,

Figure 12. Block Diagram with Digital Averaging Filter

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loading average values of conversion results into the I/O Register for the user to read through the serial interface.

Conventional SAR Operation

The LTC2368-24 may be operated like a conventional no-latency SAR as shown in Figure 13. Each conversion result is read out via the serial interface before the next conversion is initiated. Note how the contents of the I/O Register track the contents of the Conversion Result Register and that both registers contain a result corresponding to a single conversion. The digital averaging filter is transparent to the user when the LTC2368-24 is operated in this way. No programming is required. Simply read out each conversion result in each cycle. Ri represents the 24-bit conversion result corresponding to conversion number i. As few as 20 SCKs may be given in each conversion cycle (instead of the 24 shown in Figure 13) to obtain a 20-bit accurate result, making the LTC2368-24 backwards compatible with the LTC2378-20.

Reducing Measurement Noise Using the Digital Averaging Filter

Digital averaging techniques are often employed to reduce the uncertainty of measurements due to noise. The LTC2368-24 features a digital averaging filter, making it easy to perform an averaging operation without providing any additional hardware and software.

Averaging 4 Conversion Results

Figure 14 shows a case where an output result is read out once for every 4 conversions initiated. As shown, the output result read out from the I/O Register is the average of the 4 previous conversion results. The digital averaging filter will automatically average conversion results until an output result is read out. When an output result is read out, the digital averaging filter is reset and a new averaging operation starts with the next conversion result.

In this example, output results are read out after conversion numbers 0, 4 and 8. The digital averaging filter is reset after
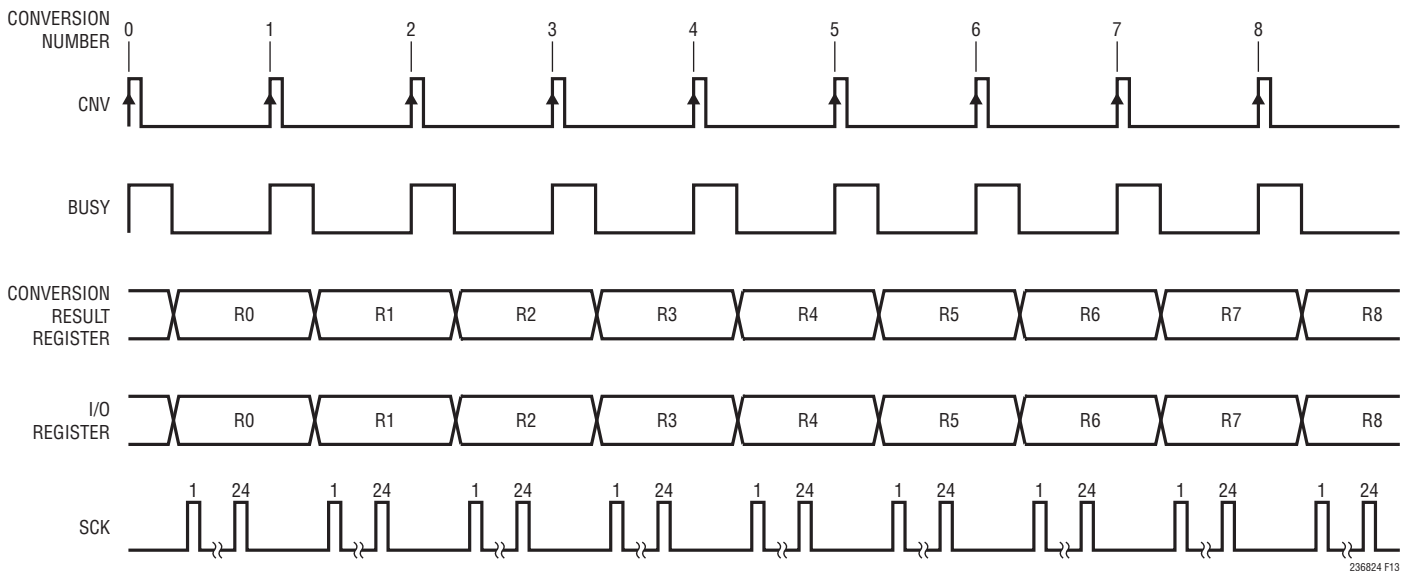

Figure 13. Conventional SAR Operation Timing
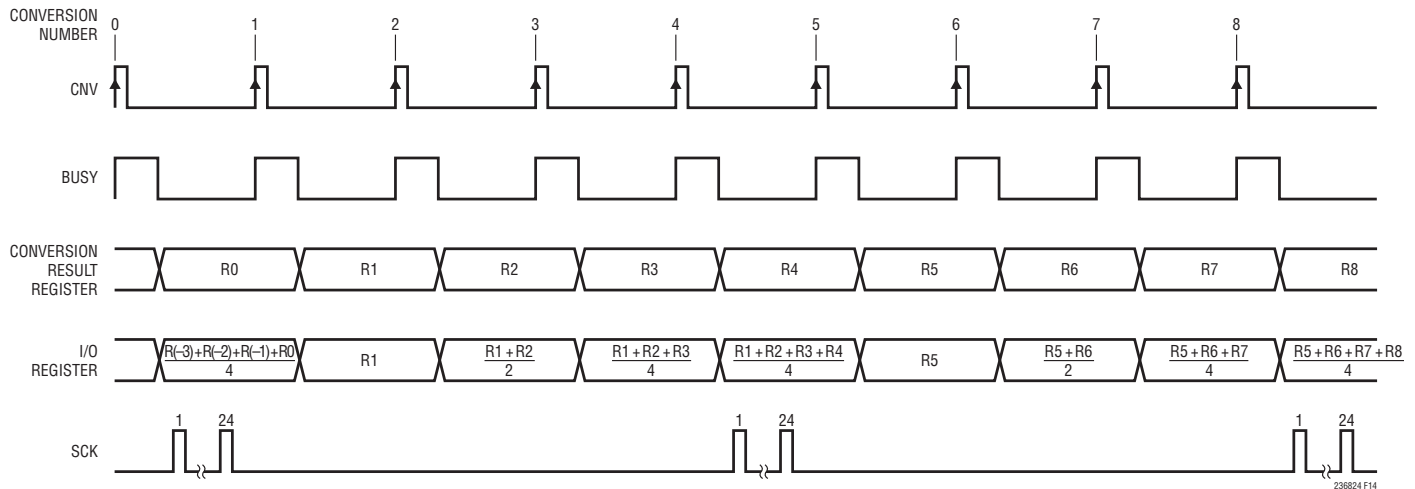
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Figure 14. Averaging 4 Conversion Results

conversion number 0 and starts a new averaging operation beginning with conversion number 1. The output result (R1 + R2 + R3 + R4)/4 is read out after conversion number 4, which resets the digital averaging filter again. Since the digital averaging filter automatically averages conversion results for each new conversion performed, an arbitrary number of conversion results, up to the upper limit of 65536, may be averaged with no programming required.

Averaging 3 Conversion Results

The output result, when averaging N conversion results for values of N that are not a power of 2, will be scaled by N/M, where M is a weighting factor that is the next power of 2 greater than N (described later in the Weighting Factor section). Figure 15 shows an example where only 3 conversion results are averaged. The output result read out is scaled by N/M = ¾.

Using the Digital Averaging Filter with Reduced Data Rate

The examples given in Figures 13, 14 and 15 illustrate some of the most common ways to use the LTC2368-24.

Simply read each individual conversion result, or read an average of N conversion results. In each case, the result is read out between two consecutive A/D conversion (BUSY) periods, requiring a fast serial shift clock.

Distributed Read

A relatively slower serial shift clock may be used when using a distributed read. Distributed reads require that multiple conversion results be averaged.

If at least 1 but less than 20 SCK pulses(0 < SCKs < 20) are given in a conversion cycle between 2 BUSY falling edges (See Figure 16), the I/O Register is not updated with the output of the digital averaging filter, preserving its contents. This allows an output result to be read from the I/O Register over multiple conversion cycles, easing the speed requirements of the serial interface.

A read is initiated by a rising edge of a first SCK pulse and it must be terminated before a next read can be initiated. The digital averaging filter is reset upon the initiation of a read wherein a new averaging operation begins. Conversions completed after the digital averaging filter is reset
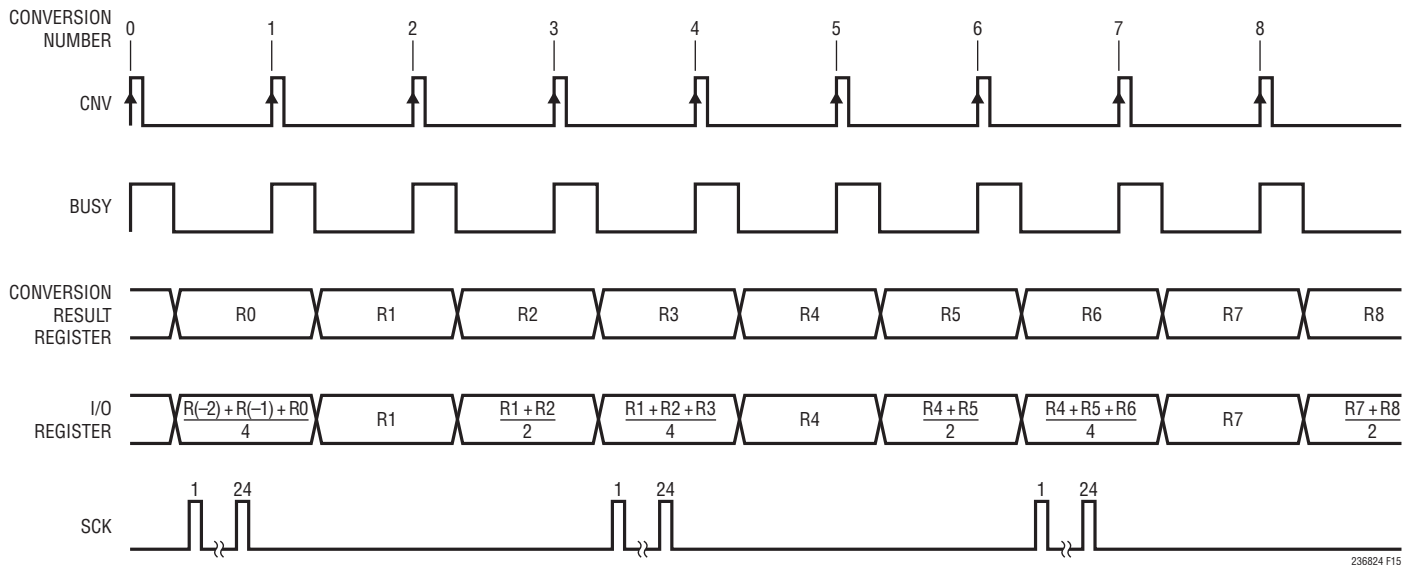
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Figure 15. Averaging 3 Conversion Results

will automatically be averaged until a new read is initiated. Thus, the digital averaging filter will calculate averages of conversion results from conversions completed between a time when one read is initiated to when a next read is initiated.

A read is terminated by providing either 0 or greater than 19 SCK pulses (rising edges) in a conversion cycle between 2 BUSY falling edges, allowing the I/O Register to be updated with new averages from the output of the digital averaging filter.

Averaging 4 Conversions Using a Distributed Read

Figure 16 shows an example where reads are initiated every 4 conversion cycles, and the I/O register is read over 3 conversion cycles. This allows the serial interface to run at 1/3 of the speed that it would otherwise have to run. The first rising SCK edge initiates a 1st read, and 3 groups of 8-bits are read out over 3 conversion cycles. No SCK pulses are provided between the BUSY falling edges of conversion numbers 4 and 5, whereby the read is terminated at the completion of conversion number 5. A second read is initiated after conversion number 5, which results in (R2 + R3 + R4 + R5)/4 being read out from the I/O Register since conversion numbers 2, 3, 4 and 5 completed between the initiation of the two reads shown.

Averaging 25 Conversions Using a Distributed Read

Figure 17 shows an example where a read is initiated every 25 conversion cycles, using a single SCK pulse per conversion cycle to read the output result from the I/O Register. The first rising SCK edge initiates a read where a single bit is then read out over the next 23 conversion cycles. No SCK pulses are provided between the BUSY falling edges of conversion numbers 25 and 26, whereby the read is terminated at the completion of conversion number 26. A 2nd read is initiated after conversion number 26, resulting in (R2 + R3 +…+ R25 + R26)/32 being read out from the I/O Register. Since 0 < SCKs < 20 pulses are given each conversion period during the read, the contents of the I/O Register are not updated, allowing the distributed read to occur without interruption.
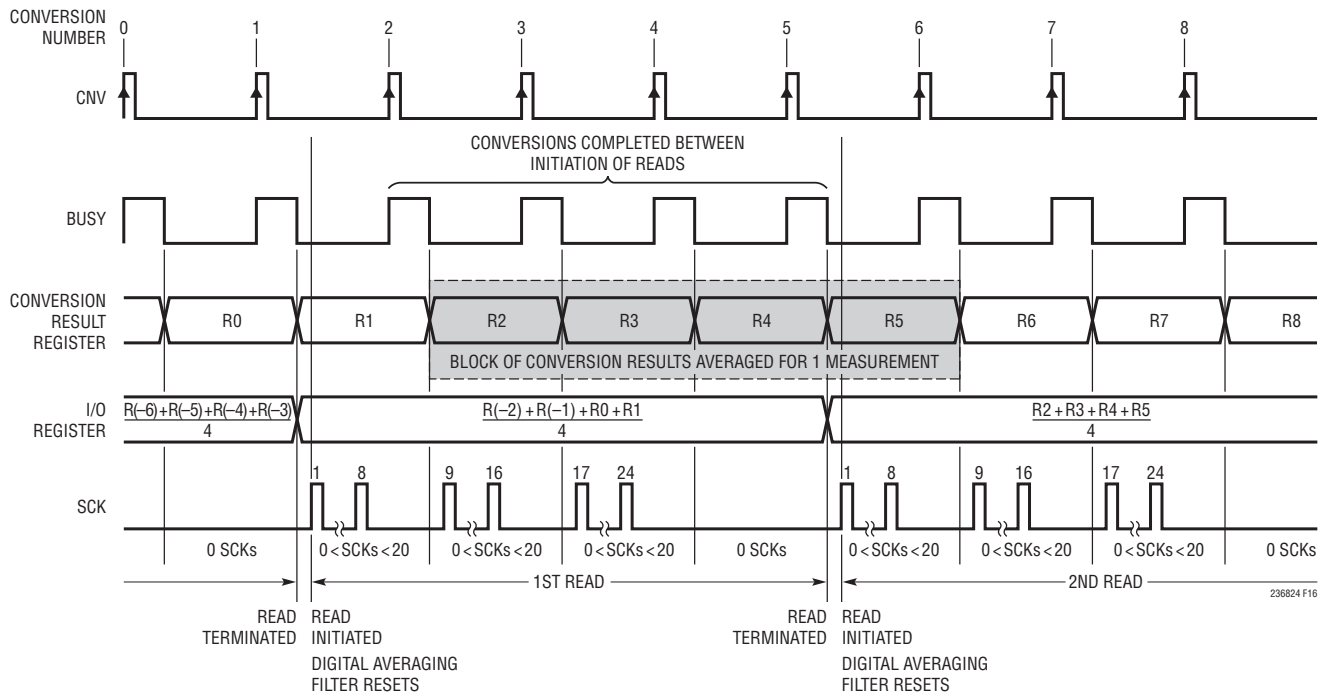
236824f

APPLICATIONS INFORMATION

CONVERSION NUMBER 0 1 2 3 4 5 6 7 8

CNV

CONVERSIONS COMPLETED BETWEEN INITIATION OF READS

BUSY

CONVERSION RESULT REGISTER R0 R1 R2 R3 R4 R5 R6 R7 R8

BLOCK OF CONVERSION RESULTS AVERAGED FOR 1 MEASUREMENT

I/O REGISTER

$$\frac{R(-6)+R(-5)+R(-4)+R(-3)}{4}$$ $$\frac{R(-2)+R(-1)+R0+R1}{4}$$ $$\frac{R2+R3+R4+R5}{4}$$

SCK   1 8   9 16   17 24   1 8   9 16   17 24

0 SCKs   0 < SCKs < 20   0 < SCKs < 20   0 < SCKs < 20   0 SCKs   0 < SCKs < 20   0 < SCKs < 20   0 < SCKs < 20   0 SCKs

1ST READ   2ND READ

READ TERMINATED   READ INITIATED   READ TERMINATED   READ INITIATED

DIGITAL AVERAGING FILTER RESETS   DIGITAL AVERAGING FILTER RESETS

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Figure 16. Averaging 4 Conversion Results and Reading Out Data with a Distributed Read

CONVERSION NUMBER 0 1 2 3 4 23 24 25 26 27

CNV

CONVERSIONS COMPLETED BETWEEN INITIATION OF READS

BUSY

CONVERSION RESULT REGISTER R0 R1 R2 R3 R23 R24 R25 R26

I/O REGISTER

$$\frac{R(-23)+R(-22)+...+R0+R1}{32}$$ (REPEATING READ PATTERN – AVERAGE OF 25 CONVERSION RESULTS FROM 25 CONVERSIONS PRECEDING INITIATION OF READ) $$\frac{R2+R3+...+R25+R26}{32}$$

SCK   1   2   3   4   23   24   1

0 SCKs   0 < SCKs < 20   0 < SCKs < 20   0 < SCKs < 20   1 SCK/CNV   0 < SCKs < 20   0 < SCKs < 20   0 SCKs   0 < SCKs < 20
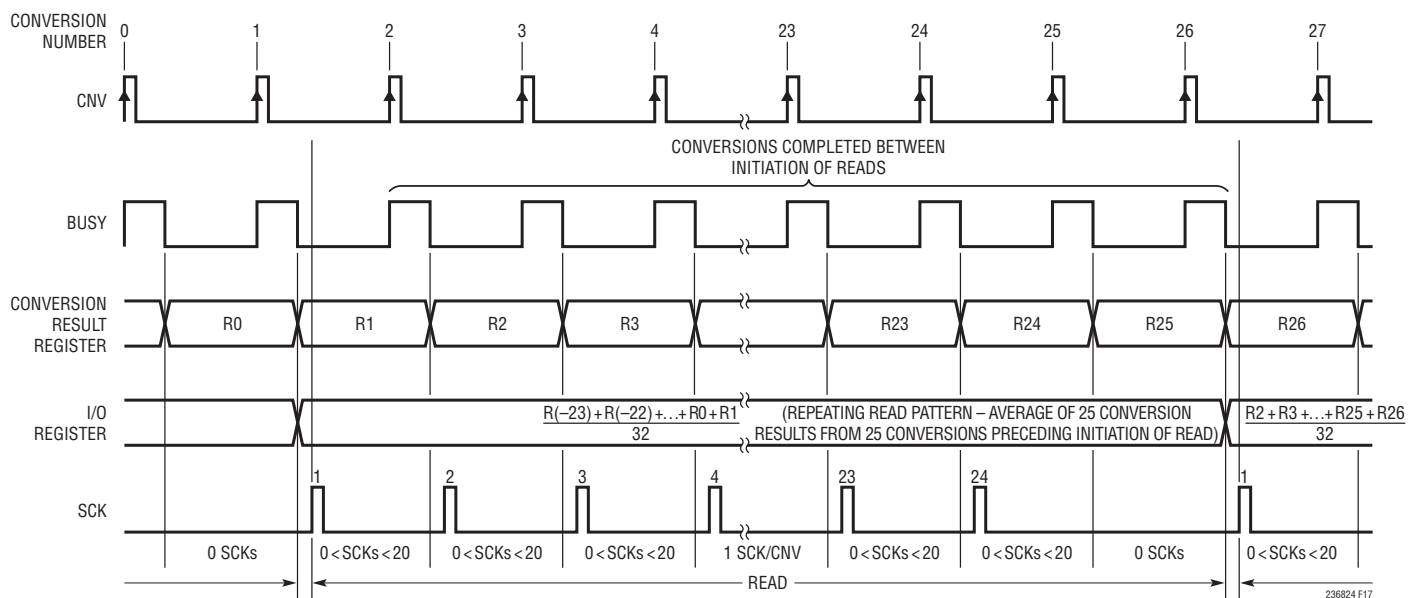
READ

236824 F17

Figure 17. Averaging 25 Conversion Results and Reading Out Data with a Distributed Read

APPLICATIONS INFORMATION

Minimum Shift Clock Frequency

Requiring at least 1 SCK pulse per conversion cycle while performing a read sets a lower limit on the SCK frequency that can be used which is: $f_{SCK} = f_{SMPL}$.

Noise vs Averaging

The noise of the ADC is un-correlated from one sample to the next. As a result, the ADC noise for a measurement will decrease by $\sqrt{N}$ where N is the number of A/D conversion results averaged for a given measurement. Other noise sources, such as noise from the input buffer amplifier and reference noise may be correlated from sample-to-sample and may be reduced by averaging, but to a lesser extent.

Weighting Factor

When conversion results are averaged, the resulting output code represents an equally weighted average of the previous N samples if N is a power of 2. If N is not a power of 2, a weighting factor, M, is chosen according to Table 1. Specifically, if Ri represents the 24-bit conversion result of the ith analog sample, then the output code, D, representing N averaged conversion results is defined as:

$$D = \sum_{i=1}^{N} \frac{R_i}{M}$$

Table 1 illustrates weighting factors for any number of averages, N, between 1 and 65536 and the resulting data throughputs. Note that M reaches a maximum value of 65536 when N = 65536. For N > 65536, the digital averaging filter will continue to accumulate conversion results such that N/M > 1. In such a case, if the ADC core produces conversion results that have a non-zero mean, the output result will eventually saturate at positive or negative full-scale.

Table 1. Weighting Factors and Throughput for Various Values of N

N	M	DATA THROUGHPUT
1	1	1Msps
2	2	500ksps
3 - 4	4	333.3ksps - 250ksps
5 - 8	8	200ksps - 125ksps
9 - 16	16	111.1ksps - 62.5ksps
17 - 32	32	58.8ksps - 31.3ksps
33 - 64	64	30.3ksps - 15.6ksps
65 - 128	128	15.4ksps - 7.8ksps
129 - 256	256	7.8ksps - 3.9ksps
257 - 512	512	3.9ksps - 2ksps
513 - 1024	1024	2ksps - 1ksps
1025 - 2048	2048	1ksps - 500sps
2049 - 4096	4096	488sps - 244sps
4097 - 8192	8192	244sps - 122sps
8193 - 16384	16384	122sps - 61sps
16385 - 32768	32768	61sps - 30.5sps
32769 - 65536	65536	30.5sps - 15.3sps

In cases where N/M < 1, achieving a full-scale output result would require driving the analog inputs beyond the specified guaranteed input differential voltage range. Doing so is strongly discouraged since operation of the LTC2368-24 beyond guaranteed specifications could result in undesired behavior, possibly corrupting results. For proper operation, it is recommended that the analog input voltage not exceed the 0V to V_{REF} specification. Note that the output results do not saturate at N/M when N/M < 1.

50Hz and 60Hz Rejection

Particular input frequencies may be rejected by selecting the appropriate number of averages, N, based on the sampling rate, f_{SMPL}, and the desired frequency to be rejected, f_{REJECT}. If,

$$T_{AVG} = \frac{1}{f_{SMPL}} \bullet N = \frac{1}{f_{REJECT}}$$

APPLICATIONS INFORMATION

then, D is an average value for a full sine wave cycle of f_{REJECT}, resulting in zero gain for that particular frequency and integer multiples thereof up to $f_{SMPL} - f_{REJECT}$ (See Figure 18). Solving for N gives:

$$N = \frac{f_{SMPL}}{f_{REJECT}}$$

Using this expression, we can find N for rejecting 50Hz and 60Hz as well as other frequencies. Note that N and f_{SMPL} may be traded off to achieve rejection of particular frequencies as shown below.

To reject 50Hz with f_{SMPL} = 1Msps:

$$N = \frac{1,000,000sps}{50Hz}$$
$$= 20,000$$

To reject both 50Hz and 60Hz (each being a multiple of 10Hz), with N = 1024:

$$f_{SMPL} = 1024 \cdot 10Hz$$
$$= 10.24ksps$$

Figure 18 shows an example of a SINC[1] filter where f_{SMPL} = 1Msps and N = 8, resulting in f_{REJECT} = 125kHz. Note that input frequencies above DC other than f_{REJECT} or multiples thereof are also attenuated to varying degrees due to the averaging operation.
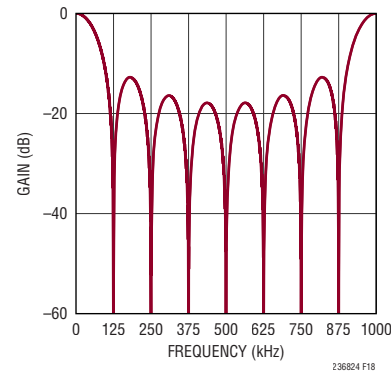

Figure 18. SINC[1] Filter with f_{SMPL} = 1Msps and N = 8

Count

In addition to the 24-bit output code, a 16-bit WORD, C[15:0], is appended to produce a total output WORD of 40 bits, as shown in Figure 19. C[15:0] is the straight binary representation (MSB first) of the number of samples averaged to produce the output result minus one. For instance, if N samples are averaged to produce the output result, C[15:0] will equal N – 1. Thus, if N is 1 which is the case with no averaging, C[15:0] will always be 0. If N is 16384, then C[15:0] will equal 16383, and so on. If more than 65536 samples are averaged, then C[15:0] saturates at 65535.
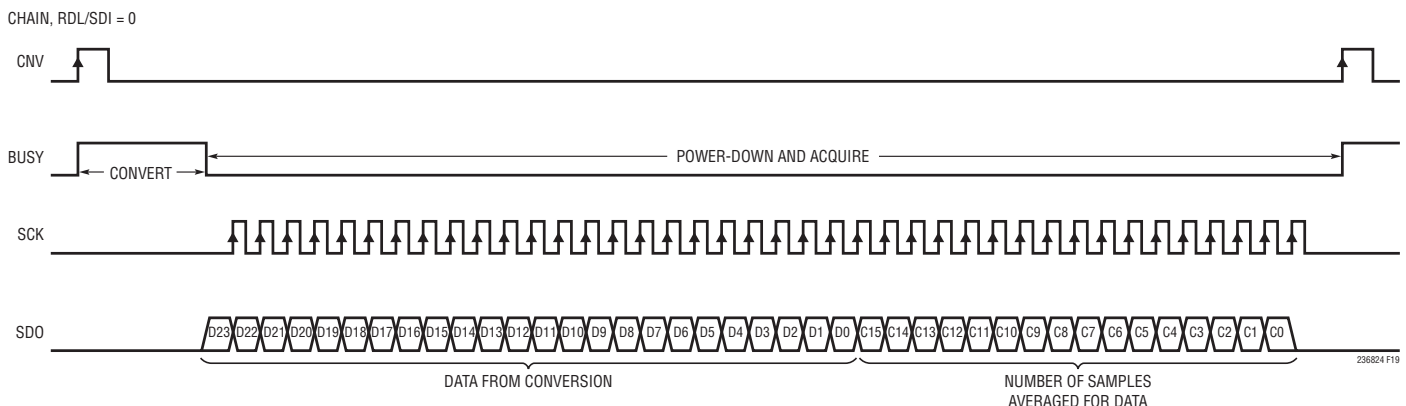
CHAIN, RDL/SDI = 0

Figure 19. Serial Output Code Parsing

TIMING DIAGRAMS

Normal Mode, Single Device

When CHAIN = 0, the LTC2368-24 operates in normal mode. In normal mode, RDL/SDI enables or disables the serial data output pin SDO. If RDL/SDI is high, SDO is in high impedance and SCK is ignored. If RDL/SDI is low,

SDO is driven. Figure 20 shows a single LTC2368-24 operated in normal mode with CHAIN and RDL/SDI tied to ground. With RDL/SDI grounded, SDO is enabled and the MSB(D23) of the output result is available $t_{DSDOBUSYL}$ after the falling edge of BUSY. The count information is shifted out after the output result.
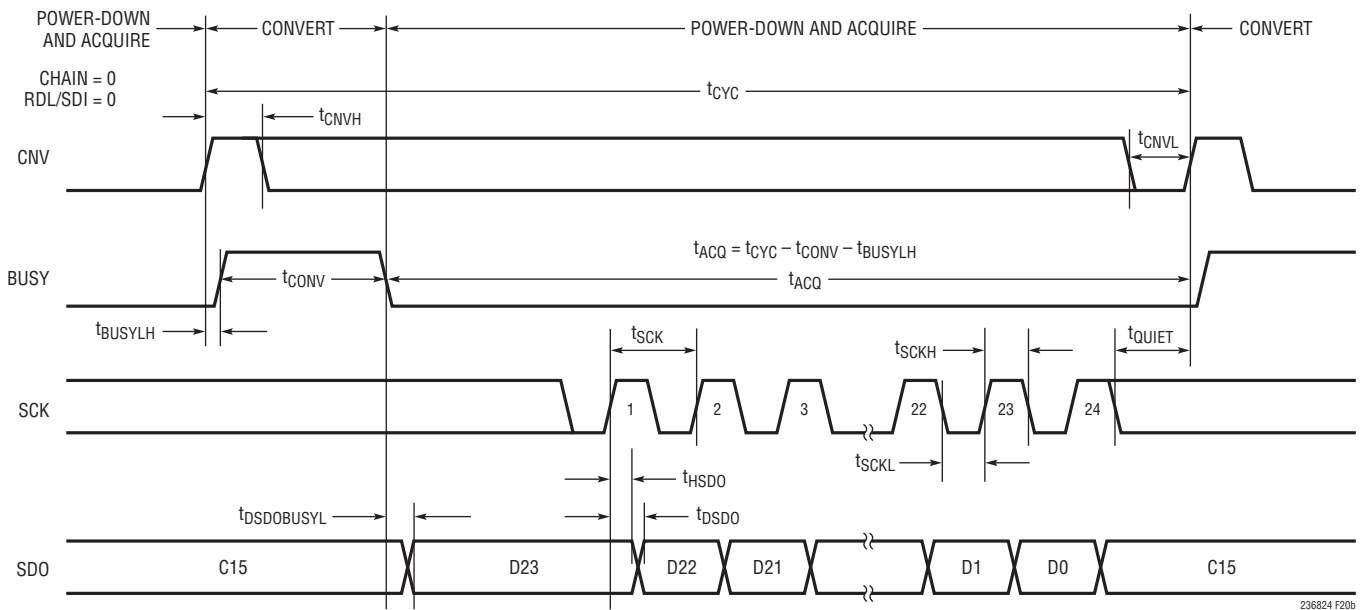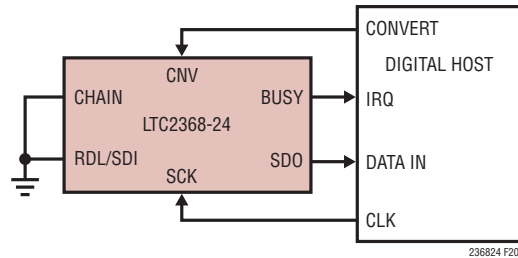

Figure 20. Using a Single LTC2368-24 in Normal Mode

For more information www.linear.com/LTC2368-24

TIMING DIAGRAMS

Normal Mode, Multiple Devices

Figure 21 shows multiple LTC2368-24 devices operating in normal mode (CHAIN = 0) sharing CNV, SCK and SDO. By sharing CNV, SCK and SDO, the number of required signals to operate multiple ADCs in parallel is reduced.

Since SDO is shared, the RDL/SDI input of each ADC must be used to allow only one LTC2368-24 to drive SDO at a time in order to avoid bus conflicts. As shown in Figure 21, the RDL/SDI inputs idle high and are individually brought low to read data out of each device between conversions. When RDL/SDI is brought low, the MSB of the selected device is output onto SDO. The count information is shifted out after the output result.
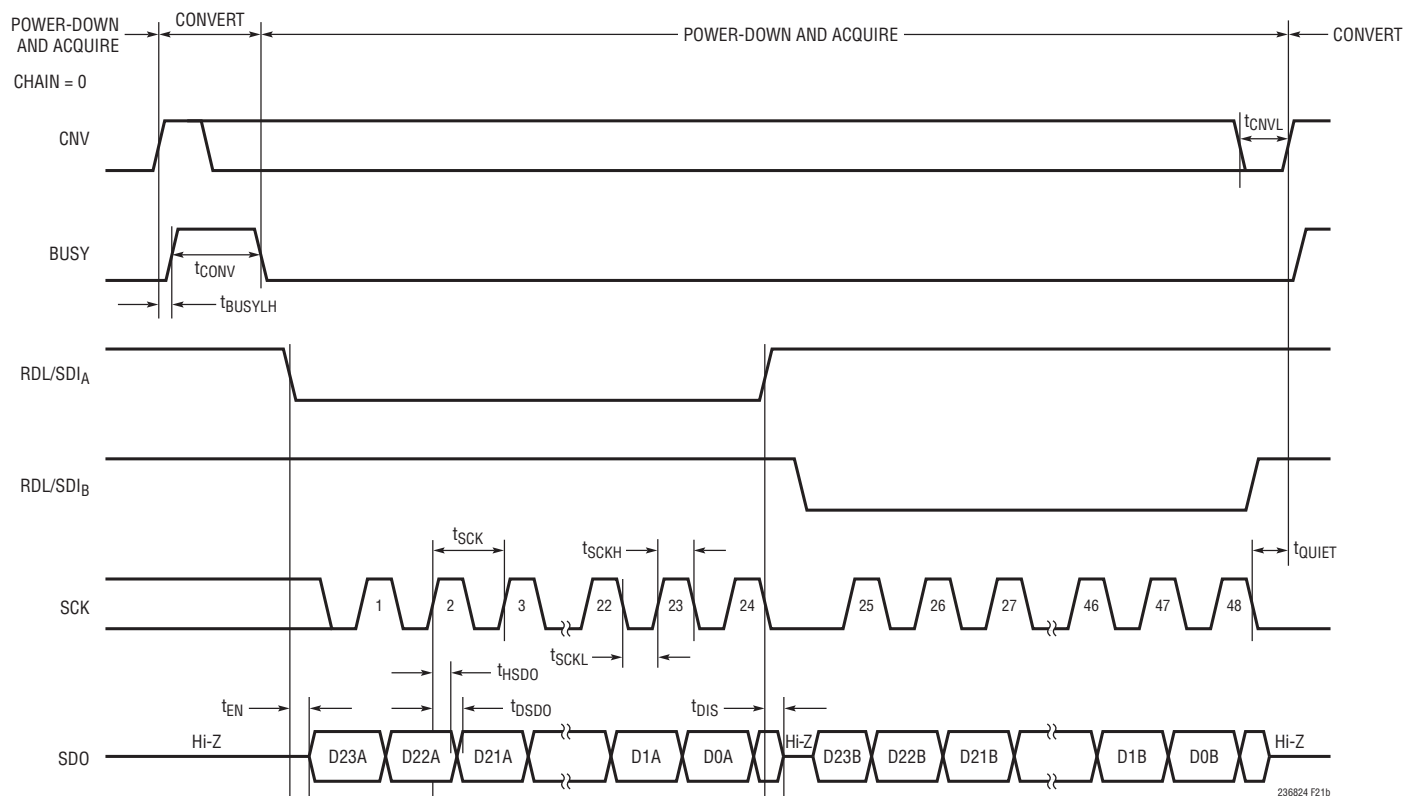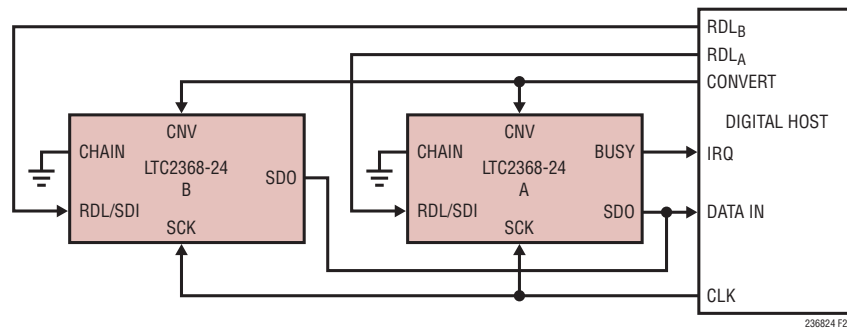

Figure 21. Normal Mode with Multiple Devices Sharing CNV, SCK and SDO

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TIMING DIAGRAMS

Chain Mode, Multiple Devices

When CHAIN = OV_{DD}, the LTC2368-24 operates in chain mode. In chain mode, SDO is always enabled and RDL/SDI serves as the serial data pin (SDI) where daisy-chain data output from another ADC can be input.

This is useful for applications where hardware constraints may limit the number of lines needed to interface to a large number of converters. Figure 22 shows an example with two daisy-chained devices. The MSB of converter A will appear at SDO of converter B after 40 SCK cycles. The MSB of converter A is clocked in at the RDL/SDI pin of converter B on the rising edge of the first SCK pulse. The functionality of the digital averaging filter is preserved when in chain mode.
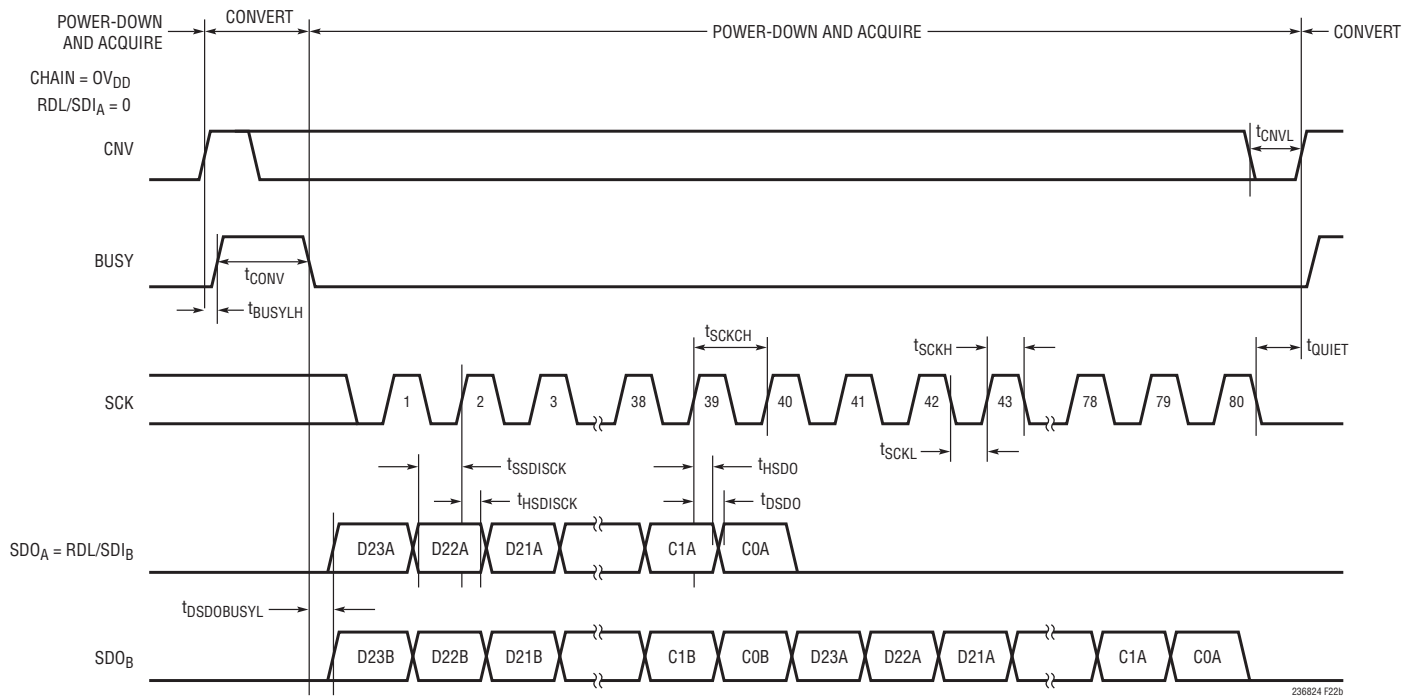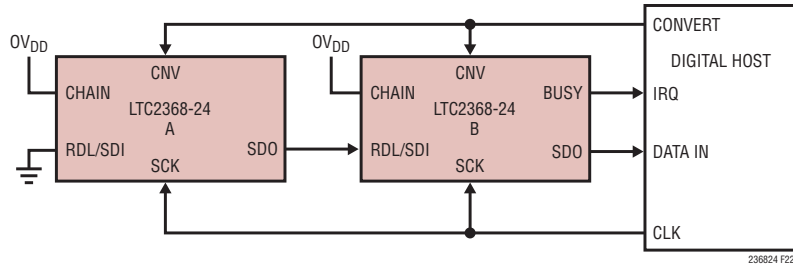

Figure 22. Chain Mode Timing Diagram

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BOARD LAYOUT

To obtain the best performance from the LTC2368-24 a printed circuit board is recommended. Layout for the printed circuit board (PCB) should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals alongside analog signals or underneath the ADC.

Supply bypass capacitors should be placed as close as possible to the supply pins. Low impedance common re-turns for these bypass capacitors are essential to the low noise operation of the ADC. A single solid ground plane is recommended for this purpose. When possible, screen the analog input traces using ground.

Reference Design

For a detailed look at the reference design for this converter, including schematics and PCB layout, please refer to DC2289, the evaluation kit for the LTC2368-24.
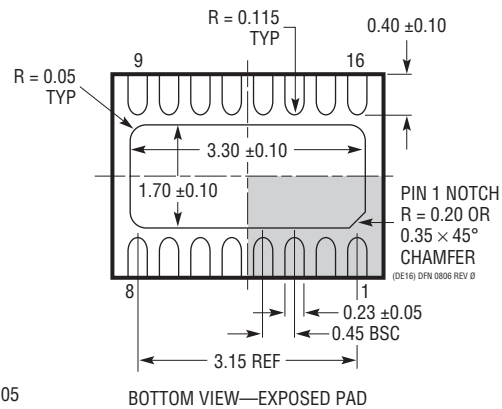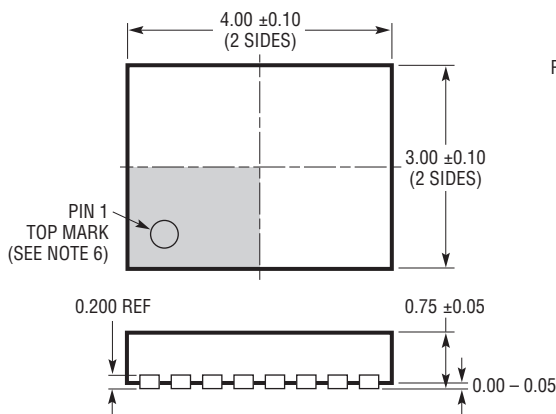
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2368-24#packaging for the most recent package drawings.

DE Package
16-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1732 Rev Ø)
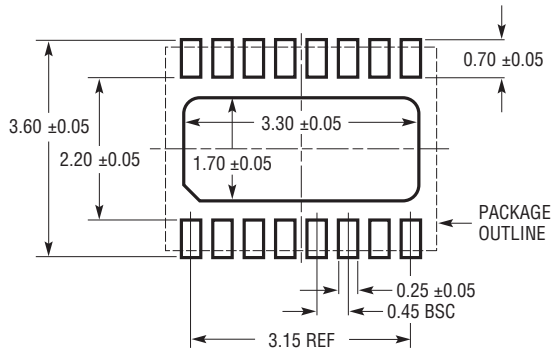
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC
   PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

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PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2368-24#packaging for the most recent package drawings.

MS Package
16-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1669 Rev A)

$\frac{0.889 \pm 0.127}{(.035 \pm .005)}$

$\frac{5.10}{(.201)}$ MIN

$\frac{3.20 - 3.45}{(.126 - .136)}$

$\frac{0.305 \pm 0.038}{(.0120 \pm .0015)}$ TYP

$\frac{0.50}{(.0197)}$ BSC

RECOMMENDED SOLDER PAD LAYOUT

DETAIL "A"

$\frac{0.254}{(.010)}$

GAUGE PLANE

0° – 6° TYP

$\frac{0.53 \pm 0.152}{(.021 \pm .006)}$

DETAIL "A"

$\frac{0.18}{(.007)}$

$\frac{4.039 \pm 0.102}{(.159 \pm .004)}$
(NOTE 3)

16 15 14 13 12 11 10 9

$\frac{0.280 \pm 0.076}{(.011 \pm .003)}$ REF

$\frac{4.90 \pm 0.152}{(.193 \pm .006)}$

$\frac{3.00 \pm 0.102}{(.118 \pm .004)}$
(NOTE 4)

1 2 3 4 5 6 7 8

$\frac{1.10}{(.043)}$ MAX

$\frac{0.86}{(.034)}$ REF

SEATING PLANE

$\frac{0.17 - 0.27}{(.007 - .011)}$ TYP

$\frac{0.50}{(.0197)}$ BSC

$\frac{0.1016 \pm 0.0508}{(.004 \pm .002)}$

MSOP (MS16) 0213 REV A

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

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