# LTC2385-16
## 16-Bit, 5Msps SAR ADC

## FEATURES

- **5Msps Throughput Rate**
- **No Pipeline Delay, No Cycle Latency**
- **93.8dB SNR (Typ) at $f_{IN}$ = 1MHz**
- **101dB SFDR (Typ) at $f_{IN}$ = 1MHz**
- **Nyquist Sampling Up to 2.5MHz Input**
- Guaranteed 16-Bit, No Missing Codes
- ±0.5LSB INL (Max)
- 8.192$V_{P-P}$ Differential Inputs
- 5V and 2.5V Supplies
- Internal 20ppm/°C (Max) Reference
- Serial LVDS Interface
- 78mW Power Dissipation
- 32-Pin (5mm × 5mm) QFN Package

## APPLICATIONS

- High Speed Data Acquisition
- Imaging
- Communications
- Control Loops
- Instrumentation
- ATE

## DESCRIPTION

The LTC®2385-16 is a low noise, high speed, 16-bit 5Msps successive approximation register (SAR) ADC ideally suited for a wide range of applications. The combination of excellent linearity and wide dynamic range makes the LTC2385-16 ideal for high speed imaging and instrumentation applications. No-latency operation provides a unique solution for high speed control loop applications. The very low distortion at high input frequencies enables communications applications requiring wide dynamic range and significant signal bandwidth.

To support high speed operation while minimizing the number of data lines, the LTC2385-16 features a serial LVDS digital interface. The LVDS interface has one-lane and two-lane output modes, allowing the user to optimize the interface data rate for each application.

## TYPICAL APPLICATION



FFT, $f_{SMPL}$ = 5Msps, $f_{IN}$ = 2kHz

SNR = 94.0dB
THD = −117dB
SINAD = 93.9dB
SFDR = 119dB
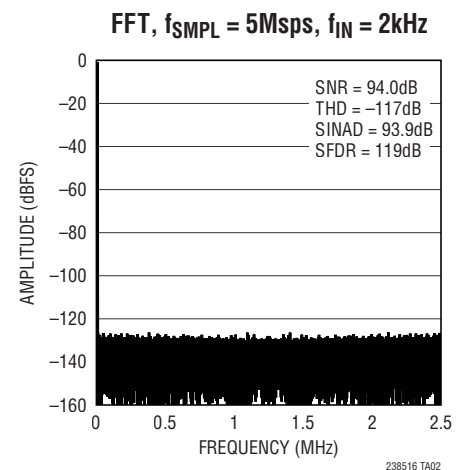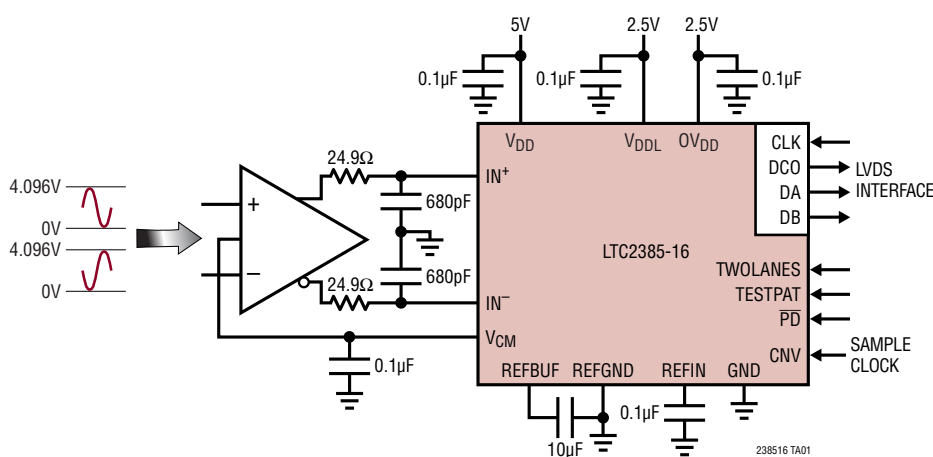
# ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage ($V_{DD}$) ...................................................6V
Supply Voltage ($V_{DDL}$, $OV_{DD}$) ...................................2.8V
Analog Input Voltage (Note 3)
  $IN^+$, $IN^-$ ........................(GND – 0.3V) to ($V_{DD}$ + 0.3V)
  REFBUF.........................(GND – 0.3V) to ($V_{DD}$ + 0.3V)
  REFIN (Note 4)...........................(GND – 0.3V) to 2.8V
Digital Input Voltage (Note 3)
  $\overline{PD}$, TESTPAT ............. (GND – 0.3V) to ($OV_{DD}$ + 0.3V)
  $CLK^+$, $CLK^-$ ................ (GND – 0.3V) to ($OV_{DD}$ + 0.3V)
  TWOLANES, $CNV^+$,
  $CNV^-$ ..........................(GND – 0.3V) to ($V_{DDL}$ + 0.3V)
Power Dissipation ............................................ 500mW
Operating Temperature Range
  LTC2385C ............................................. 0°C to 70°C
  LTC2385I ..........................................–40°C to 85°C
Storage Temperature Range .................–65°C to 150°C

# PIN CONFIGURATION

TOP VIEW

$V_{CM}$ $V_{DDL}$ $V_{DDL}$ GND $CNV^+$ $CNV^-$ GND TWOLANES

| 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 |

GND 1
$IN^+$ 2
$IN^-$ 3
GND 4
REFGND 5
REFGND 6
REFBUF 7
REFBUF 8

33
GND

24 $CLK^+$
23 $CLK^-$
22 $OV_{DD}$
21 GND
20 $DCO^+$
19 $DCO^-$
18 $DA^+$
17 $DA^-$

| 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |

REFIN GND $V_{DD}$ $V_{DD}$ $\overline{PD}$ TESTPAT $DB^-$ $DB^+$

UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 34°C/W
EXPOSED PAD (PIN 33) IS GND, MUST BE SOLDERED TO PCB
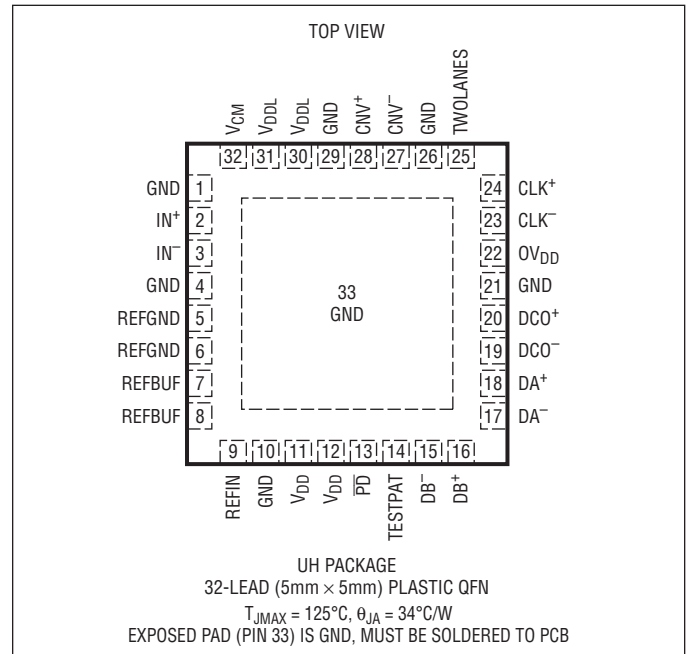
# ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC2385CUH-16#PBF | LTC2385CUH-16#TRPBF | 238516 | 32-Lead (5mm × 5mm) Plastic QFN | 0°C to 70°C |
| LTC2385IUH-16#PBF | LTC2385IUH-16#TRPBF | 238516 | 32-Lead (5mm × 5mm) Plastic QFN | –40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

# ELECTRICAL CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 5)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IN}^+$ | Absolute Input Range ($IN^+$) | (Note 6) | ● | –0.1 | | $V_{REFBUF}$ + 0.1 | V |
| $V_{IN}^-$ | Absolute Input Range ($IN^-$) | (Note 6) | ● | –0.1 | | $V_{REFBUF}$ + 0.1 | V |
| $V_{IN}^+ - V_{IN}^-$ | Input Differential Voltage Range | $V_{IN}^+ - V_{IN}^-$ | ● | $-V_{REFBUF}$ | | $V_{REFBUF}$ | V |
| $V_{INCM}$ | Common Mode Input Range | $(V_{IN}^+ + V_{IN}^-)/2$ | ● | $V_{REFBUF}/2 - 0.1$ | $V_{REFBUF}/2$ | $V_{REFBUF}/2 + 0.1$ | V |
| $I_{IN}$ | Analog Input DC Leakage Current | | ● | –1 | | 1 | µA |
| $C_{IN}$ | Analog Input Capacitance | Sample Mode<br>Hold Mode | | | 20<br>2 | | pF<br>pF |
| CMRR | Input Common Mode Rejection Ratio | $f_{IN}$ = 1MHz | | | 75 | | dB |

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# CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 5)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| | Resolution | | ● | 16 | | | Bits |
| | No Missing Codes | | ● | 16 | | | Bits |
| | Transition Noise | | | | 0.35 | | $LSB_{RMS}$ |
| INL | Integral Linearity Error | REFBUF = 4.096V (Notes 7, 9) | ● | −0.5 | ±0.15 | 0.5 | LSB |
| DNL | Differential Linearity Error | | ● | −0.6 | ±0.06 | 0.6 | LSB |
| ZSE | Zero-Scale Error | (Note 8) | ● | −2.5 | ±0.4 | 2.5 | LSB |
| | Zero-Scale Error Drift | | | | 0.005 | | LSB/°C |
| FSE | Full-Scale Error | REFBUF = 4.096V (REFBUF Overdriven) (Notes 8, 9)<br>REFIN = 2.048V (REFIN Overdriven) (Note 8) | ●<br>● | −5<br>−40 | ±1.3<br>±7 | 5<br>40 | LSB<br>LSB |
| | Full-Scale Error Drift | REFBUF = 4.096V (REFBUF Overdriven) (Note 9)<br>REFIN = 2.048V (REFIN Overdriven) | | | ±0.1<br>±1.5 | | ppm/°C<br>ppm/°C |

# DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C and $A_{IN}$ = −1dBFS. (Notes 5, 10)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| SINAD | Signal-to-(Noise + Distortion) Ratio | $f_{IN}$ = 2kHz<br>$f_{IN}$ = 1MHz | ●<br>● | 91.5<br>91.2 | 93.9<br>93.2 | | dB<br>dB |
| SNR | Signal-to-Noise Ratio | $f_{IN}$ = 2kHz<br>$f_{IN}$ = 1MHz | ●<br>● | 91.6<br>91.4 | 94<br>93.8 | | dB<br>dB |
| THD | Total Harmonic Distortion (First Five Harmonics) | $f_{IN}$ = 2kHz<br>$f_{IN}$ = 1MHz | ●<br>● | | −117<br>−100 | −108<br>−97 | dB<br>dB |
| SFDR | Spurious Free Dynamic Range | $f_{IN}$ = 2kHz<br>$f_{IN}$ = 1MHz | ●<br>● | 107<br>97 | 119<br>101 | | dB<br>dB |
| | −3dB Input Bandwidth | | | | 200 | | MHz |

# INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 5)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{REFIN}$ | Internal Reference Output Voltage | $I_{OUT}$ = 0µA | | 2.043 | 2.048 | 2.053 | V |
| | $V_{REFIN}$ Temperature Coefficient | (Note 11) | ● | | ±5 | ±20 | ppm/°C |
| | REFIN Output Impedance | | | | 15 | | kΩ |
| | $V_{REFIN}$ Line Regulation | $V_{DD}$ = 4.75V to 5.25V | | | 0.3 | | mV/V |
| | REFIN Input Voltage Range | (REFIN Overdriven) (Note 6) | ● | 2.008 | 2.048 | 2.088 | V |

# REFERENCE BUFFER CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 5)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{REFBUF}$ | Reference Buffer Output Voltage | $V_{REFIN}$ = 2.048V | ● | 4.090 | 4.096 | 4.102 | V |
| | REFBUF Input Voltage Range | (REFBUF Overdriven) (Notes 6, 9) | ● | 4.016 | 4.096 | 4.176 | V |
| $I_{REFBUF}$ | REFBUF Load Current | $V_{REFBUF}$ = 4.096V (REFBUF Overdriven) (Notes 9, 12) | ● | | 0.9 | 1.1 | mA |
| | | $V_{REFBUF}$ = 4.096V, Sleep Mode (REFBUF Overdriven) (Note 9) | | | 0.5 | | mA |
| $V_{CM}$ | Common Mode Output | $V_{REFBUF}$ = 4.096V, $I_{OUT}$ = 0µA | | 2.028 | 2.048 | 2.068 | V |
| | $V_{CM}$ Output Impedance | −1mA < $I_{OUT}$ < 1mA | ● | | 15 | | Ω |

# DIGITAL INPUTS AND DIGITAL OUTPUTS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 5)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **$\overline{PD}$, TESTPAT, TWOLANES** | | | | | | | |
| $V_{IH}$ | High Level Input Voltage | $V_{DDL}$ = 0$V_{DD}$ = 2.5V | ● | 1.7 | | | V |
| $V_{IL}$ | Low Level Input Voltage | $V_{DDL}$ = 0$V_{DD}$ = 2.5V | ● | | | 0.6 | V |
| $I_{IN}$ | Digital Input Current | $V_{IN}$ = 0V to 2.5V | ● | −10 | | 10 | µA |
| $C_{IN}$ | Digital Input Capacitance | | | | 3 | | pF |
| **$CNV^+$, Single-Ended Convert Start Mode ($CNV^-$ Tied to GND)** | | | | | | | |
| $V_{IH}$ | High Level Input Voltage | $V_{DDL}$ = 2.5V | ● | 1.7 | | | V |
| $V_{IL}$ | Low Level Input Voltage | $V_{DDL}$ = 2.5V | ● | | | 0.6 | V |
| $C_{IN}$ | Digital Input Capacitance | | | | 2 | | pF |
| **$CNV^+/CNV^-$, Differential Convert Start Mode** | | | | | | | |
| $V_{ID}$ | Differential Input Voltage | (Note 13) | ● | 175 | 350 | 650 | mV |
| $V_{ICM}$ | Common Mode Input Voltage | | ● | 0.8 | 1.25 | 1.7 | V |
| **$CLK^+/CLK^-$ (LVDS Clock Input)** | | | | | | | |
| $V_{ID}$ | Differential Input Voltage | (Note 13) | ● | 175 | 350 | 650 | mV |
| $V_{ICM}$ | Common Mode Input Voltage | | ● | 0.8 | 1.25 | 1.7 | V |
| **$DCO^+/DCO^-$, $DA^+/DA^-$, $DB^+/DB^-$ (LVDS Outputs)** | | | | | | | |
| $V_{OD}$ | Differential Output Voltage | 100Ω Differential Load | ● | 247 | 350 | 454 | mV |
| $V_{OS}$ | Common Mode Output Voltage | 100Ω Differential Load | ● | 1.125 | 1.25 | 1.375 | V |

# POWER REQUIREMENTS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 5)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | (Note 6) | ● | 4.75 | 5 | 5.25 | V |
| $V_{DDL}$ | Supply Voltage | (Note 6) | ● | 2.375 | 2.5 | 2.625 | V |
| $0V_{DD}$ | Supply Voltage | (Note 6) | ● | 2.375 | 2.5 | 2.625 | V |
| $I_{VDD}$ | Supply Current | 5Msps Sample Rate | ● | | 3 | 3.8 | mA |
| $I_{VDDL}$ | Supply Current | 5Msps Sample Rate | ● | | 17.1 | 19.6 | mA |
| $I_{OVDD}$ | Supply Current | 5Msps Sample Rate | ● | | 8.1 | 9.6 | mA |
| $I_{POWERDOWN}$ | Power-Down Mode Current | Power-Down Mode ($I_{VDD}$) | ● | | 1 | 20 | µA |
| $I_{POWERDOWN}$ | Power-Down Mode Current | Power-Down Mode ($I_{VDDL}$ + $I_{OVDD}$) | ● | | 2 | 250 | µA |
| $P_D$ | Power Dissipation | 5Msps Sample Rate | ● | | 78 | 92 | mW |
| | Power-Down Mode | Power-Down Mode ($I_{VDD}$ + $I_{VDDL}$ + $I_{OVDD}$) | ● | | 10 | 725 | µW |
| $I_{DIFFCNV}$ | Increase in $I_{VDDL}$ with Differential CNV Mode Enabled (No Increase During Power-Down) | | | | 2.1 | | mA |
| $I_{TWOLANE}$ | Increase in $I_{OVDD}$ with Two-Lane Mode Enabled (No Increase During Power-Down) | | | | 3.6 | | mA |

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# ADC TIMING CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 5)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $f_{SMPL}$ | Sampling Frequency | | ● | 0.02 | | 5 | Msps |
| $t_{CONV}$ | CNV↑ to Output Data Ready | | ● | 88 | 94 | 101 | ns |
| $t_{ACQ}$ | Acquisition Time | | | | $t_{CYC}$ – 67 | | ns |
| $t_{CYC}$ | Time Between Conversions | | ● | 200 | | 50,000 | ns |
| $t_{CNVH}$ | CNV High Time | (Note 13) | ● | 5 | | | ns |
| $t_{CNVL}$ | CNV Low Time | (Note 13) | ● | 8 | | | ns |
| $t_{FIRSTCLK}$ | CNV↑ to First CLK↑ from the Same Conversion | (Note 13) | ● | 104 | | | ns |
| $t_{LASTCLK}$ | CNV↑ to Last CLK↓ from the Previous Conversion | (Note 13) | ● | | | 83 | ns |
| $t_{CLKH}$ | CLK High Time | | ● | 1.25 | | | ns |
| $t_{CLKL}$ | CLK Low Time | | ● | 1.25 | | | ns |
| $t_{CLKDCO}$ | CLK to DCO Delay | (Note 13) | ● | 0.7 | 1.3 | 2.3 | ns |
| $t_{CLKD}$ | CLK to DA/DB Delay | (Note 13) | ● | 0.7 | 1.3 | 2.3 | ns |
| $t_{SKEW}$ | DCO to DA/DB skew | $t_{CLKD}$ – $t_{CLKDCO}$ (Note 13) | ● | –200 | 0 | 200 | ps |
| $t_{AP}$ | Sampling Delay Time | (Note 13) | | | 0 | | ns |
| $t_{JITTER}$ | Sampling Delay Jitter | (Note 13) | | | 0.25 | | $ps_{RMS}$ |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltage values are with respect to ground.

**Note 3:** When these pin voltages are taken below ground or above $V_{DD}$, $V_{DDL}$ or $OV_{DD}$, they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground or above $V_{DD}$, $V_{DDL}$ or $OV_{DD}$ without latchup.

**Note 4:** When this pin voltage is taken below ground, it will be clamped by an internal diode. When this pin voltage is taken above $V_{DDL}$, it is clamped by a diode in series with a 2k resistor. This product can handle input currents up to 100mA below ground without latchup.

**Note 5:** $V_{DD}$ = 5V, $V_{DDL}$ = 2.5V, $OV_{DD}$ = 2.5V, $f_{SMPL}$ = 5MHz, REFIN = 2.048V, single-ended CNV, one-lane output mode unless otherwise noted.

**Note 6:** Recommended operating conditions.

**Note 7:** Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

**Note 8:** Zero-scale error is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111. Full-scale error is the worst-case deviation of the first and last code transitions from ideal and includes the effect of offset error.

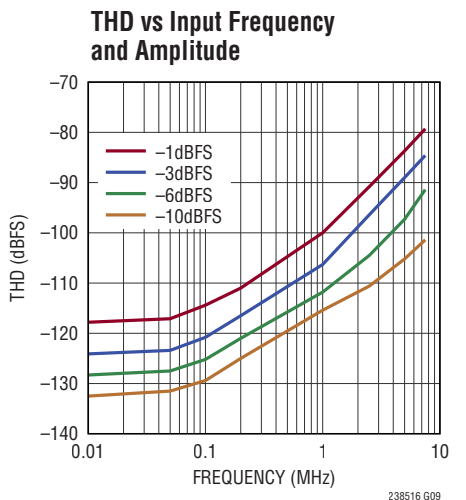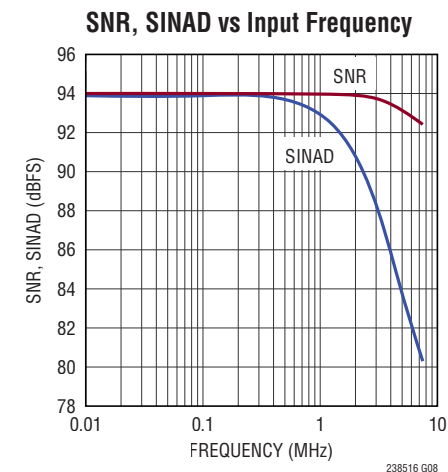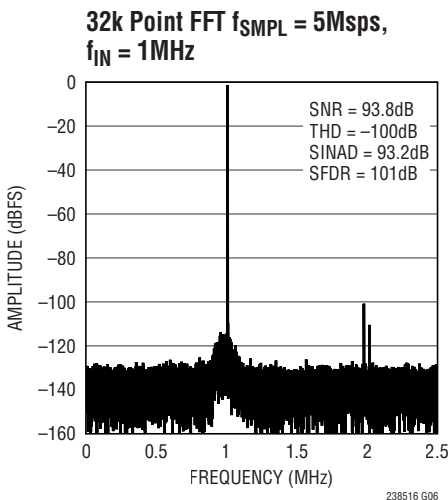**Note 9:** When REFBUF is overdriven, the internal reference buffer must be turned off by setting REFIN = 0V.

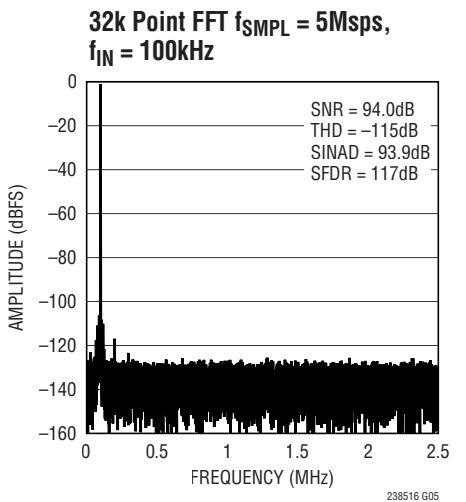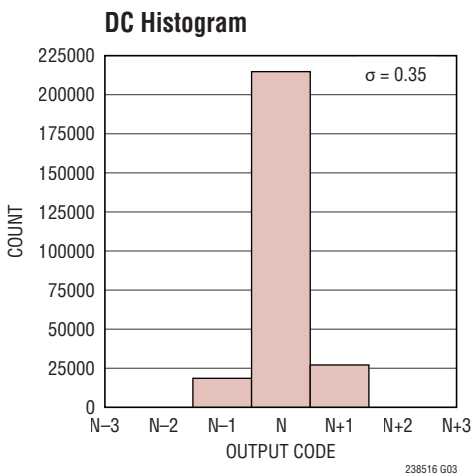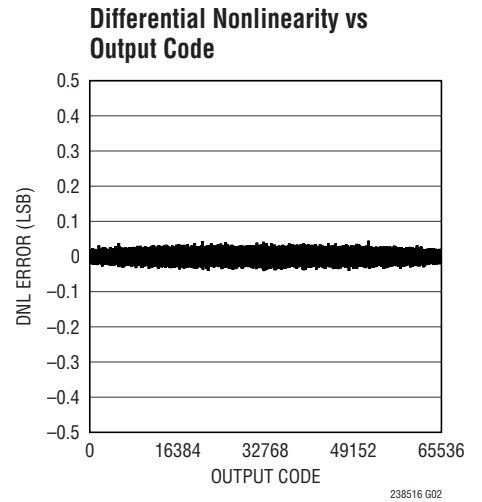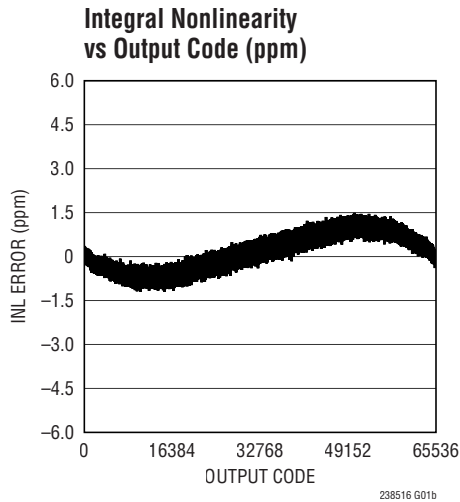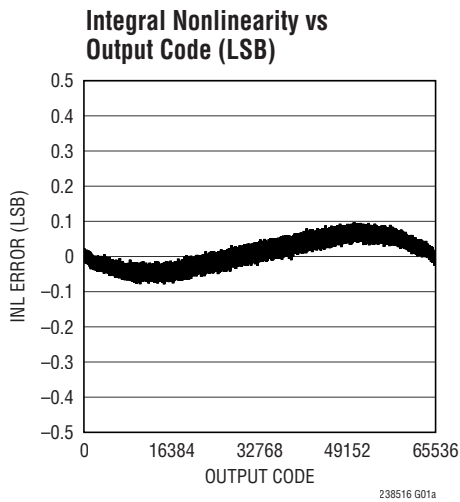**Note 10:** All specifications in dB are referred to a full-scale $\pm V_{REFBUF}$ differential input.

**Note 11:** Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.
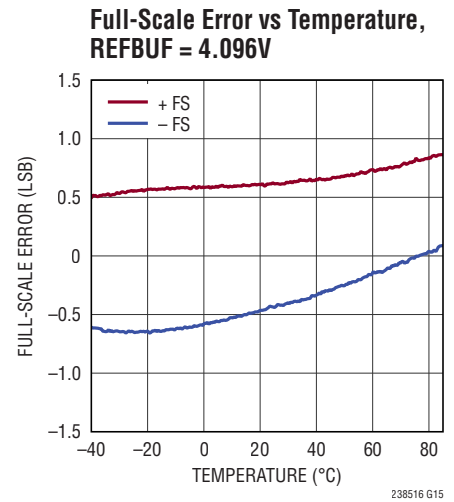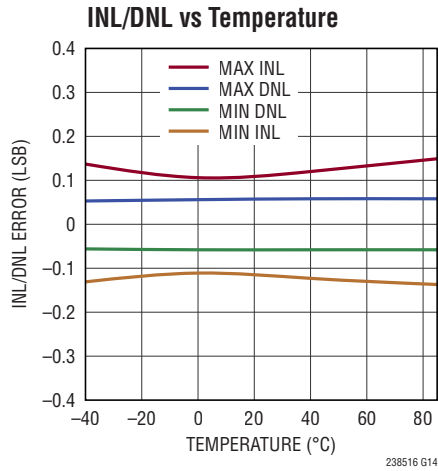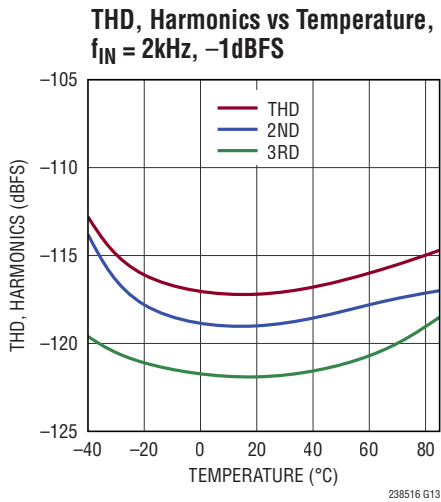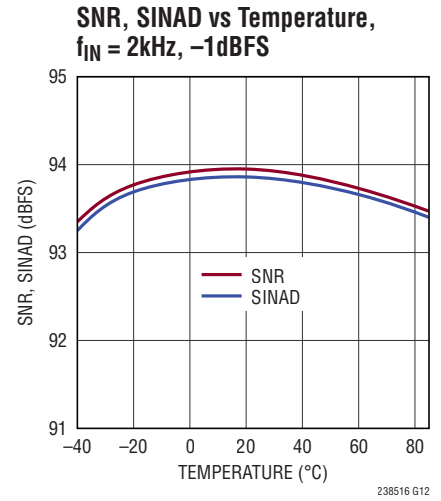
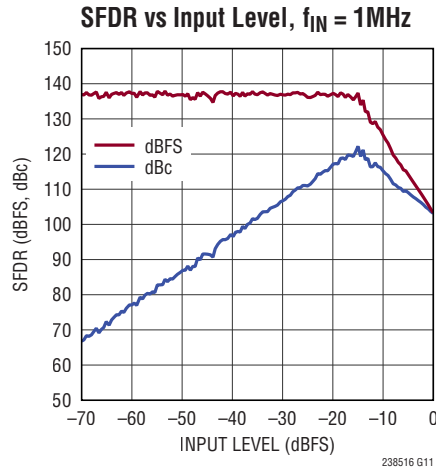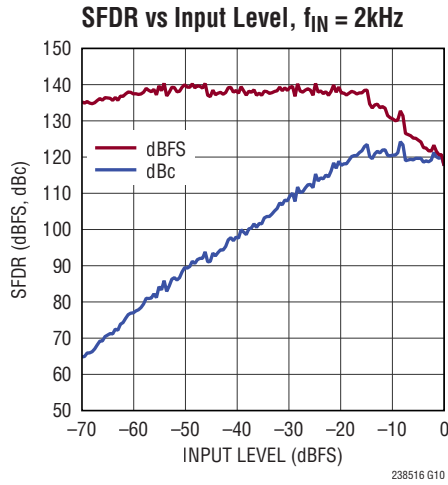**Note 12:** $f_{SMPL}$ = 5MHz, $I_{REFBUF}$ varies linearly with sample rate.

**Note 13:** Guaranteed by design, not subject to test.

# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_{DD} = 5V$, $V_{DDL} = 2.5V$, $OV_{DD} = 2.5V$, REFIN = 2.048V, $f_{SMPL}$ = 5Msps, unless otherwise noted.

### Integral Nonlinearity vs Output Code (LSB)



238516 G01a

### Integral Nonlinearity vs Output Code (ppm)



238516 G01b

### Differential Nonlinearity vs Output Code



238516 G02

### DC Histogram



σ = 0.35

238516 G03

### 32k Point FFT $f_{SMPL}$ = 5Msps, $f_{IN}$ = 2kHz



SNR = 94.0dB
THD = −117dB
SINAD = 93.9dB
SFDR = 119dB

238516 G04

### 32k Point FFT $f_{SMPL}$ = 5Msps, $f_{IN}$ = 100kHz



SNR = 94.0dB
THD = −115dB
SINAD = 93.9dB
SFDR = 117dB

238516 G05

### 32k Point FFT $f_{SMPL}$ = 5Msps, $f_{IN}$ = 1MHz



SNR = 93.8dB
THD = −100dB
SINAD = 93.2dB
SFDR = 101dB

238516 G06

### SNR, SINAD vs Input Frequency



238516 G08

### THD vs Input Frequency and Amplitude



−1dBFS
−3dBFS
−6dBFS
−10dBFS

238516 G09

238516f

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# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_{DD} = 5V$, $V_{DDL} = 2.5V$, $OV_{DD} = 2.5V$, REFIN = 2.048V, $f_{SMPL}$ = 5Msps, unless otherwise noted.

**SFDR vs Input Level, $f_{IN}$ = 2kHz**



**SFDR vs Input Level, $f_{IN}$ = 1MHz**



**SNR, SINAD vs Temperature, $f_{IN}$ = 2kHz, −1dBFS**



**THD, Harmonics vs Temperature, $f_{IN}$ = 2kHz, −1dBFS**



**INL/DNL vs Temperature**



**Full-Scale Error vs Temperature, REFBUF = 4.096V**

# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, $V_{DD}$ = 5V, $V_{DDL}$ = 2.5V, $OV_{DD}$ = 2.5V, REFIN = 2.048V, $f_{SMPL}$ = 5Msps, unless otherwise noted.

**Zero-Scale Error vs Temperature**



238516 G16

**Supply Current vs Temperature**



238516 G17

**Supply Current vs Sample Rate**



238516 G18

**Analog Input Current vs Differential Input Voltage**



238516 G19

**Internal Reference Output vs Temperature**



238516 G20

# PIN FUNCTIONS

**GND (Pins 1, 4, 10, 21, 26, 29 ):** Ground. Connect to a solid ground plane in the PCB underneath the ADC.

**IN⁺, IN⁻ (Pins 2, 3):** Positive and Negative Differential Analog Inputs. The inputs must be driven differentially and 180° out of phase, with a common mode voltage of 2.048V. The differential input range is ±4.096V (each input pin swings from 0V to 4.096V.)

**REFGND (Pins 5, 6):** Reference Ground. The two pins should be shorted together and connected to the reference bypass capacitor with a short, wide trace. In addition, connect the pins to the exposed pad (Pin 33). A suggested layout is shown in the ADC Reference section of the data sheet.

**REFBUF (Pins 7, 8):** Internal Reference Buffer Output. The output voltage of the internal 2× gain reference buffer, nominally 4.096V, is provided on this pin. The two pins should be shorted together and bypassed to REFGND with a 10µF (X7R, 0805 size) ceramic capacitor. If the internal buffer is not required, tie REFIN to GND to power down the buffer and connect an external 4.096V reference to REFBUF.

**REFIN (Pin 9):** Internal Reference Output/Reference Buffer Input. The output voltage of the internal reference, nominally 2.048V, is output on this pin. An external reference can be applied to REFIN if a more accurate reference is required. For increased filtering of reference noise, bypass this pin to GND using a 0.1µF or larger ceramic capacitor. If the internal reference buffer is not used, tie REFIN to GND to power down the buffer and connect an external buffered reference to REFBUF.

**V$_{DD}$ (Pins 11, 12):** 5V Analog Power Supply. The range of V$_{DD}$ is 4.75V to 5.25V. The two pins should be shorted together and bypassed to GND with 0.1µF and 10µF ceramic capacitors.

**$\overline{PD}$ (Pin 13):** Digital input that enables power-down mode. When $\overline{PD}$ is low, the LTC2385 enters power-down mode, and all circuitry (including the LVDS interface) is shut down. When $\overline{PD}$ is high, the part operates normally. Logic levels are determined by OV$_{DD}$.

**TESTPAT (Pin 14):** Digital input that forces the LVDS data outputs to be a test pattern. When TESTPAT is high, the digital outputs are a test pattern. When TESTPAT is low, the digital outputs are the ADC conversion result. Logic levels are determined by OV$_{DD}$.

**DB⁻/DB⁺, DA⁻/DA⁺ (Pins 15/16, 17/18):** Serial LVDS Data Outputs. In one-lane output mode, DB⁻/DB⁺ are not used and their LVDS driver is disabled to reduce power consumption.

**DCO⁻/DCO⁺ (Pins 19/20):** LVDS Data Clock Output. This is an echoed version of CLK⁻/CLK⁺ that can be used to latch the data outputs.

**OV$_{DD}$ (Pin 22):** 2.5V Output Power Supply. The range of OV$_{DD}$ is 2.375V to 2.625V. Bypass to GND with a 0.1µF ceramic capacitor.

**CLK⁻/CLK⁺ (Pins 23/24):** LVDS Clock Input. This is an externally applied clock that serially shifts out the conversion result.

**TWOLANES (Pin 25):** Digital input that enables two-lane output mode. When TWOLANES is high (two-lane output mode), the ADC outputs two bits at a time on DA⁻/DA⁺ and DB⁻/DB⁺. When TWOLANES is low (one-lane output mode), the ADC outputs one bit at a time on DA⁻/DA⁺, and DB⁻/DB⁺ are disabled. Logic levels are determined by V$_{DDL}$.

**CNV⁻/CNV⁺ (Pins 27/28):** Conversion Start LVDS Input. A rising edge on CNV⁺ puts the internal sample-and-hold into the hold mode and starts a conversion cycle. CNV⁺ can also be driven with a 2.5V CMOS signal if CNV⁻ is tied to GND.

# PIN FUNCTIONS

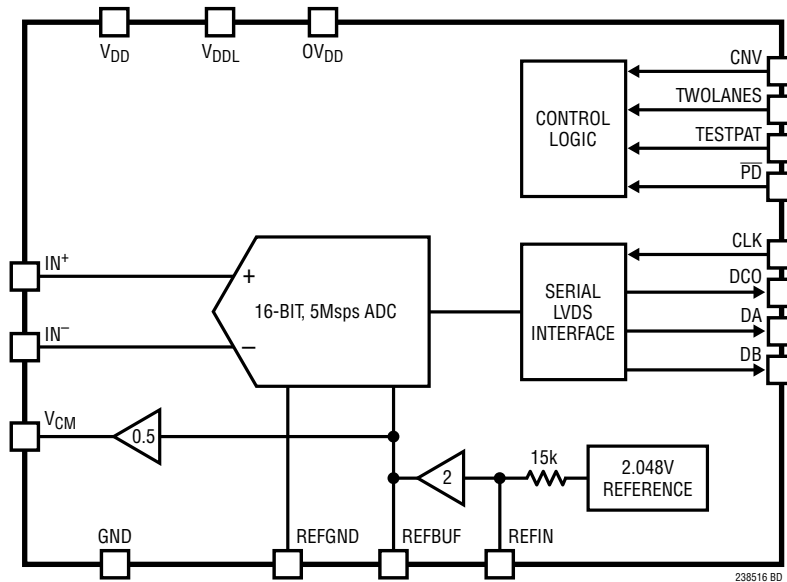$V_{DDL}$ **(Pins 30, 31):** 2.5V Analog Power Supply. The range of $V_{DDL}$ is 2.375V to 2.625V. The two pins should be shorted together and bypassed to GND with 0.1µF and 10µF ceramic capacitors.

$V_{CM}$ **(Pin 32):** Common Mode Output. $V_{CM}$, nominally 2.048V, can be used to set the common mode of the analog inputs. Bypass to GND with a 0.1µF ceramic capacitor close to the pin. If $V_{CM}$ is not used, the bypass capacitor is not necessary as long as the parasitic capacitance on the $V_{CM}$ pin is under 10pF.

**Exposed Pad (Pin 33):** The exposed pad on the bottom of the package. Connect to the ground plane of the PCB using multiple vias.
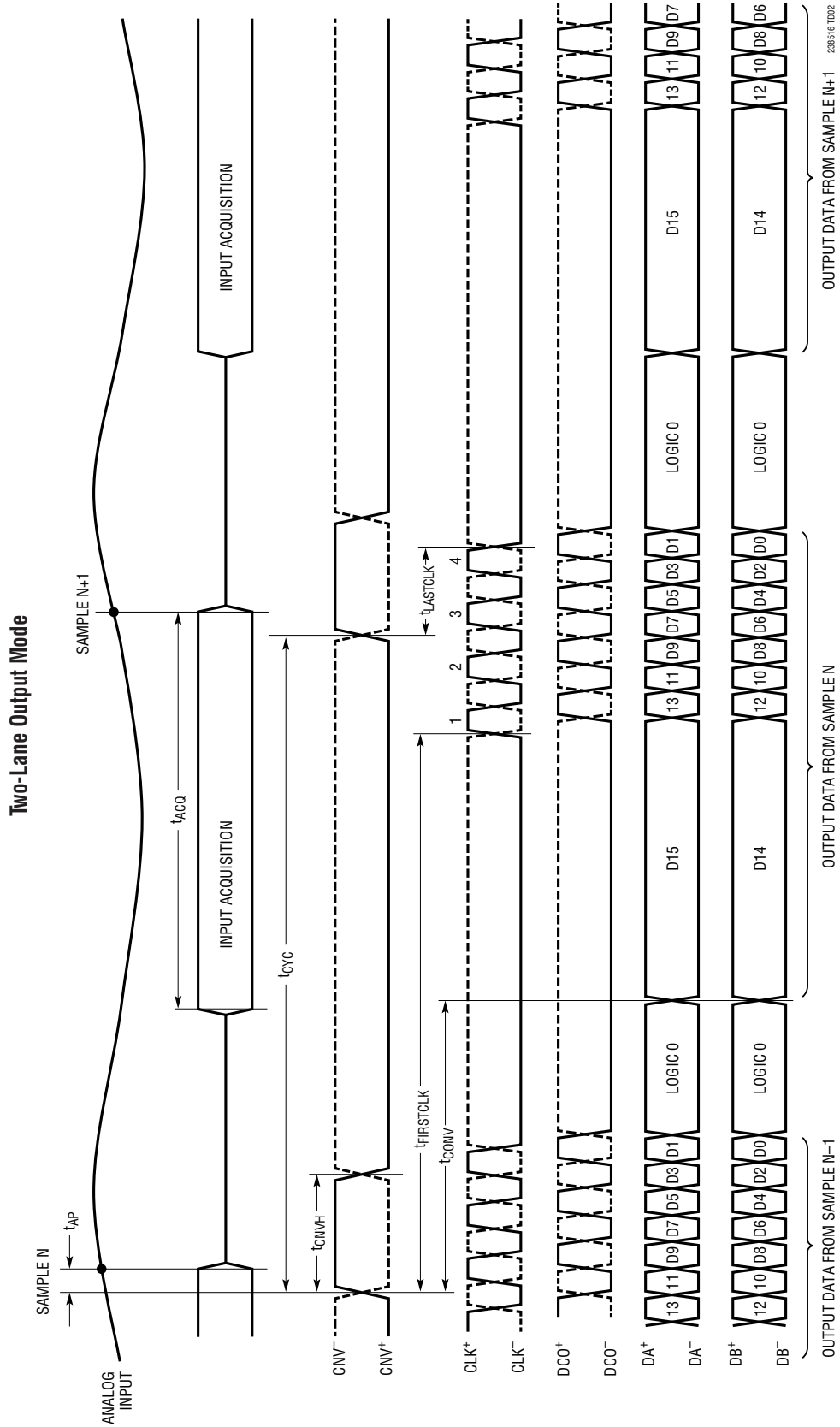
# FUNCTIONAL BLOCK DIAGRAM



238516 BD

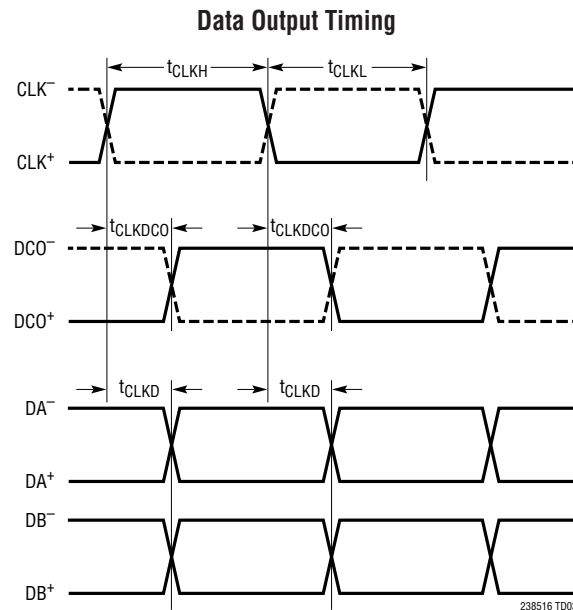# TIMING DIAGRAM



One-Lane Output Mode
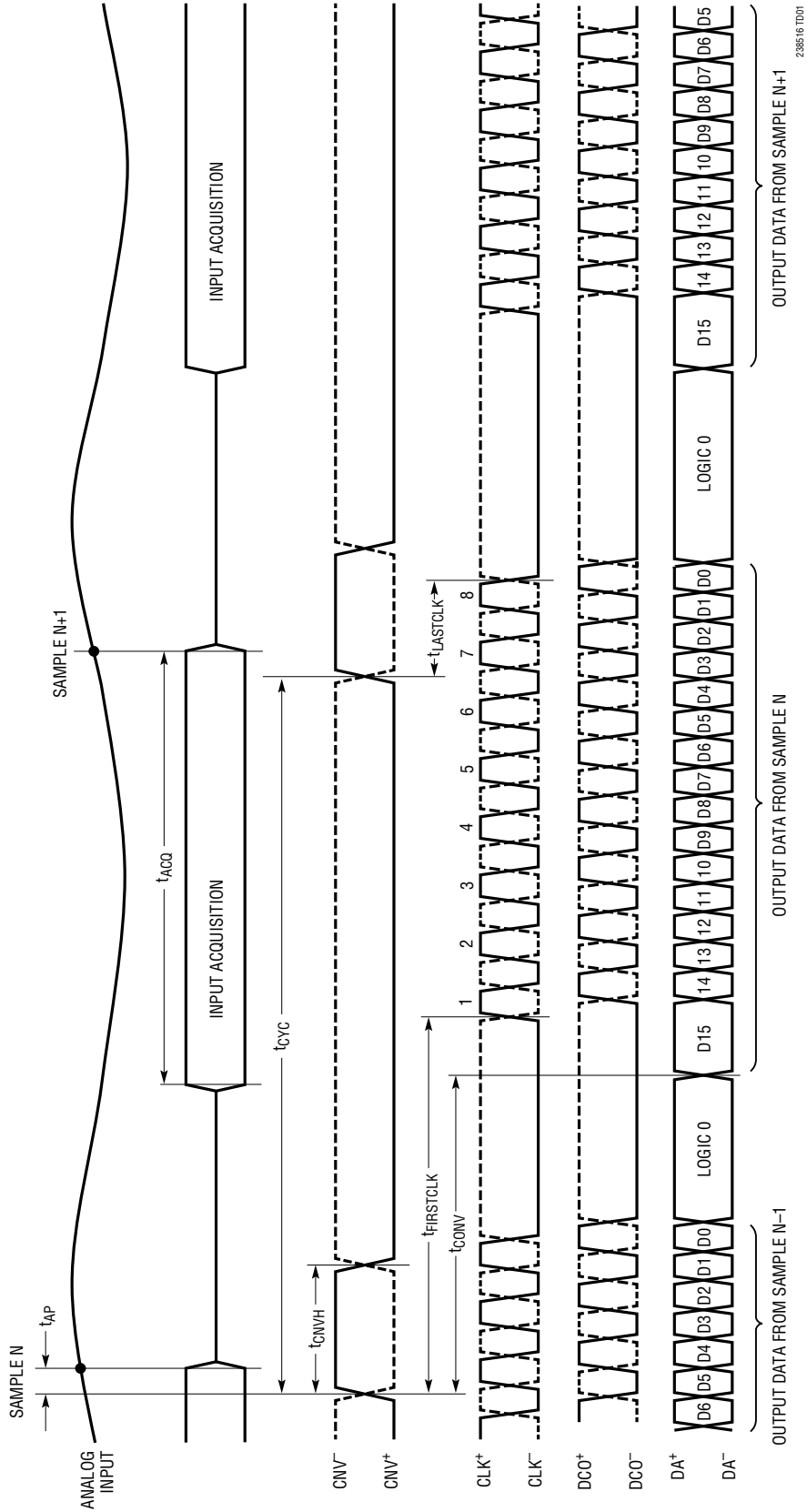
# TIMING DIAGRAM

**Two-Lane Output Mode**

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# TIMING DIAGRAM

**Data Output Timing**



238516 TD03

# APPLICATIONS INFORMATION

## OVERVIEW

The LTC2385-16 is a low noise, high speed, 16-bit successive approximation register (SAR) ADC. Operating from 5V and 2.5V supplies, the LTC2385-16 has a fully differential ±4.096V input range, making it ideal for applications that require a wide dynamic range. The LTC2385-16 achieves ±0.5 LSB INL (maximum), no missing codes at 16-bits and 94dB SNR (typical).

The LTC2385-16 includes a precision internal 2.048V reference, with a guaranteed 0.25% initial accuracy and a ±20ppm/°C (maximum) temperature coefficient, as well as an internal reference buffer. The LTC2385-16 also has a high speed serial LVDS interface that can output one or two bits at a time. The fast 5Msps throughput with no pipeline latency makes the LTC2385-16 ideally suited for a wide variety of high speed applications. The LTC2385-16 dissipates only 78mW at 5Msps and has a power-down mode to reduce the power consumption to 10µW during inactive periods.

## CONVERTER OPERATION

The LTC2385-16 operates in two phases. During the acquisition phase, the sample capacitors are connected to the analog input pins IN$^+$ and IN$^-$ to sample the differential analog input voltage. A rising edge on the CNV pin initiates a conversion. During the conversion phase, the ADC is sequenced through a successive approximation algorithm, comparing the sampled input with binary-weighted fractions of the reference voltage (e.g. $V_{REFBUF}$/2, $V_{REFBUF}$/4 … $V_{REFBUF}$/65536) using a differential comparator. At the end of conversion, control logic prepares the 16-bit digital output code for serial transfer.

## TRANSFER FUNCTION

The LTC2385-16 digitizes the full-scale voltage of 2× REFBUF into $2^{16}$ levels, resulting in an LSB size of 125µV with REFBUF = 4.096V. The output data is in two's complement format. The ideal transfer function is shown in Figure 1. The ideal offset binary transfer function can be obtained from the two's complement transfer function by inverting the most significant bit (MSB) of each output code.
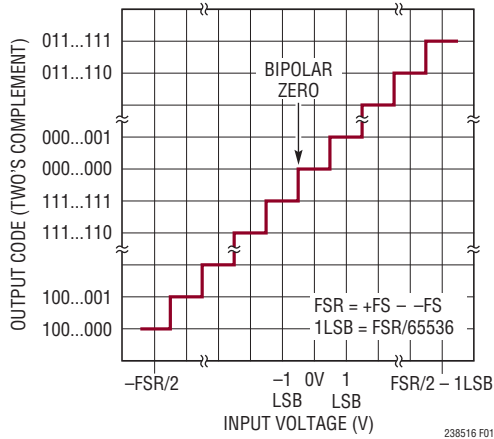
# APPLICATIONS INFORMATION



Figure 1. LTC2385-16 Transfer Function

## ANALOG INPUTS

The LTC2385-16 has a fully differential ±4.096V input range. The IN⁺ and IN⁻ pins should be driven 180 degrees out-of-phase with respect to each other, centered around a common mode voltage (IN⁺ + IN⁻)/2 that is restricted to ($V_{REFBUF}$/2 ± 0.1V). The ADC samples and digitizes the voltage difference between the two analog input pins (IN⁺ – IN⁻), and any unwanted signal that is common to both inputs is reduced by the common mode rejection ratio (CMRR) of the ADC. The analog inputs can be modeled by the equivalent circuit shown in Figure 2. The diodes and 10Ω resistors at the input provide ESD and overdrive protection. In the acquisition phase, each input sees approximately 18pF ($C_{SAMPLE}$) from the sampling capacitor in series with 28Ω ($R_{ON}$) from the on-resistance of the sampling switch. $C_{PAR}$ is a lumped capacitance on the order of 2pF formed primarily of diode junctions.
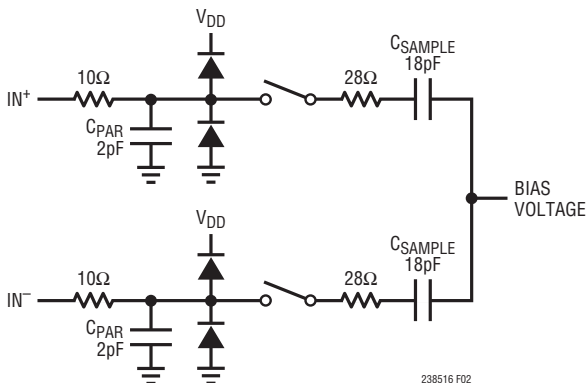


Figure 2. Equivalent Circuit for the Differential Analog Inputs of the LTC2385-16

The inputs draw a small current spike while charging the $C_{SAMPLE}$ capacitors during acquisition. This current spike is consistent and does not depend on the previously sampled input voltage. During conversion and power-down, the analog inputs draw only a small leakage current.

### Input Drive Circuits

A low impedance source can directly drive the high impedance inputs of the LTC2385-16 without gain error. A high impedance source should be buffered to minimize settling time during acquisition and to optimize the distortion performance of the ADC. Minimizing settling time is important even for DC signals because the ADC inputs draw a current spike when entering acquisition.

For best performance, a buffer amplifier should be used to drive the analog inputs of the LTC2385-16. The amplifier provides low output impedance enabling fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the current spike drawn by the ADC inputs when entering acquisition.

The LTC2385-16 is optimized for pulsed inputs that are fully settled when sampled, or dynamic signals up to 7.5MHz. Input signals that change faster than 300mV/ns when they are sampled are not recommended. This is equivalent to an 8V$_{P-P}$ sine wave at 12MHz.

### Input Filtering

The noise and distortion of the buffer amplifier and other supporting circuitry must be considered since they add to the ADC noise and distortion. A buffer amplifier with low noise density must be selected to minimize SNR degradation. A filter network should be placed between the buffer output and ADC input to both minimize the noise contribution of the buffer and reduce disturbances reflected into the buffer from ADC sampling transients. A simple one-pole lowpass RC filter is sufficient for many applications. It is important that the RC time constant of this filter be small enough to allow the analog inputs to settle within the ADC acquisition time ($t_{ACQ}$), as insufficient settling can limit INL and THD performance.

High quality capacitors and resistors should be used in the RC filters since these components can add distortion.

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NPO type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self-heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Figure 3 shows a typical input drive circuit with an RC filter. The optimal values for R and C are application specific and may require experimentation. Setting R = 24.9Ω gives good performance over a wide range of conditions.
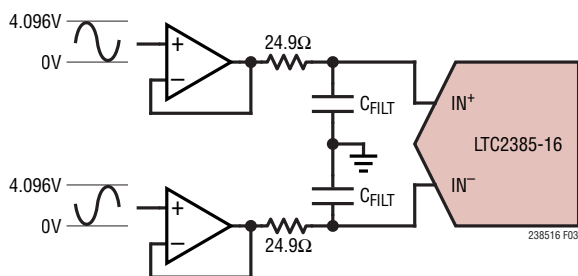


**Figure 3. Typical Input Drive Circuit**

The value for C$_{FILT}$ involves a trade-off: larger values give better noise, and smaller values give better full-scale error. Figure 4 shows a range of capacitor values to consider as a starting point based on the sample rate.
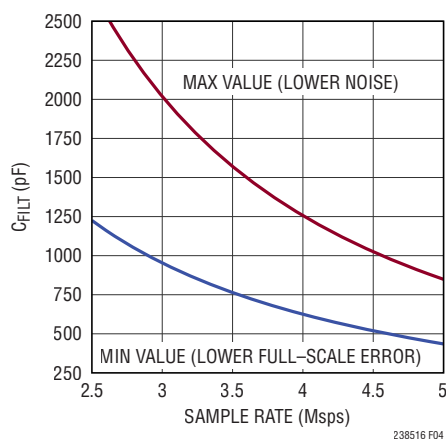


**Figure 4. Suggested Range of C$_{FILT}$ Values vs Sample Rate**

### Input Currents

One of the biggest challenges in coupling an amplifier to the LTC2385-16 is in dealing with current spikes drawn by analog inputs at the start of each acquisition phase.

The analog inputs may be modeled as a switched capacitor load on the drive circuit. A drive circuit may rely partially on attenuating switched-capacitor current spikes with small filter capacitors placed directly at the ADC inputs and partially on the driver amplifier having sufficient bandwidth to recover from the residual disturbance. Amplifiers optimized for DC performance may not have sufficient bandwidth to fully recover at the ADC's maximum conversion rate, which can produce nonlinearity and other errors. Coupling filter circuits may be classified in two broad categories:

*Fully Settled* – This case is characterized by filter time constants and an overall settling time that are considerably shorter than the sample period. When acquisition begins, the coupling filter is disturbed. For a typical first order RC filter, the disturbance will look like an initial step with an exponential decay. The amplifier will have its own response to the disturbance, which may include ringing. If the input settles completely (to within the accuracy of the LTC2385-16), the disturbance will not contribute any error.

*Partially Settled* – In this case, the beginning of acquisition causes a disturbance of the coupling filter, which then begins to settle out towards the nominal input voltage. However, acquisition ends (and the conversion begins) before the input settles to its final value. This generally produces a gain error, but as long as the settling is linear, no distortion is produced. The coupling filter's response is affected by the amplifier's output impedance and other parameters. A linear settling response to fast switched-capacitor current spikes can NOT always be assumed for precision, low bandwidth amplifiers. The coupling filter serves to attenuate the current spikes' high-frequency energy before it reaches the amplifier.

### ADC REFERENCE

The internal reference circuitry of the LTC2385-16 is shown in Figure 5. There is a low noise, low drift (20ppm/°C), bandgap reference connected to REFIN (Pin 9). An internal reference buffer gains the REFIN voltage by 2× to 4.096V at REFBUF (Pins 7, 8). The voltage difference between REFBUF and REFGND determines the full-scale input range of the ADC. The reference and reference buffer can also be externally driven if desired.
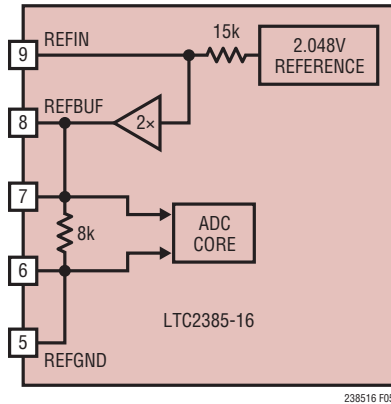
# APPLICATIONS INFORMATION



**Figure 5. LTC2385-16 Internal Reference Circuitry**

## Internal Reference with Internal Reference Buffer

To use the internal reference and internal reference buffer, bypass REFIN to GND with a 0.1µF ceramic capacitor (Figure 6). Bypass REFBUF to REFGND with a single 10µF (X7R, 0805 size) ceramic capacitor. The REFBUF capacitor should be as close as possible to the LTC2385-16 package to minimize wiring inductance. Do not place this capacitor on the opposite side of the board. Adding a second, smaller capacitor in parallel with the 10µF may degrade performance and is not recommended.
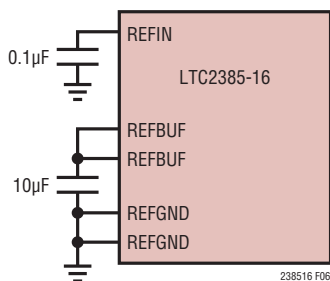


**Figure 6. Configuration for Using the Internal Reference**

Figure 7 shows a suggested layout for the REFBUF capacitor. The capacitor should be connected to REFBUF and REFGND through short, wide traces. REFGND should also be connected with a wide trace to the grounded exposed pad (Pin 33).

## External Reference with Internal Reference Buffer

If more accuracy and/or lower drift is desired, REFIN can be directly overdriven by an external 2.048V reference as
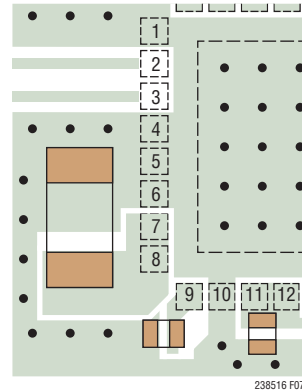


**Figure 7. Suggested REFBUF Bypass Capacitor Layout**

shown in Figure 8. Linear Technology offers a portfolio of high performance references designed to meet the needs of many applications. With its small size, low power, and high accuracy, the LTC6655-2.048 is well suited for use with the LTC2385-16 when overdriving the internal reference. The LTC6655-2.048 offers 0.025% (max) initial accuracy and 2ppm/°C (max) temperature coefficient for high precision applications. Bypassing the LTC6655-2.048 with a 2.7µF to 10µF ceramic capacitor close to the REFIN pin is recommended.
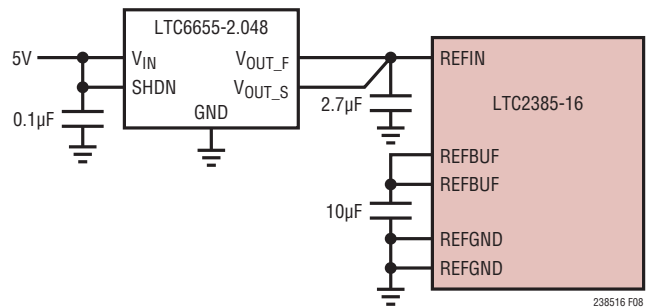


**Figure 8. Using the LTC6655-2.048 as an External Reference**

## External Reference Buffer

The internal reference buffer can also be overdriven with an external 4.096V reference at REFBUF as shown in Figure 9. To do so, REFIN must be grounded to disable the reference buffer. The external reference must have a fast transient response and be able to drive the 0.5mA to 0.9mA load at the REFBUF pin. The LTC6655-4.096 is recommended when overdriving REFBUF.
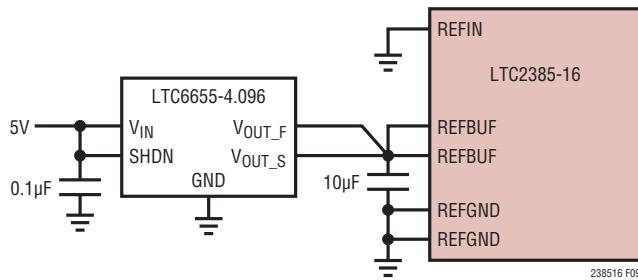
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**Figure 9. Overdriving REFBUF Using the LTC6655-4.096**



**Figure 10. 32k Point FFT of the LTC2385-16, $f_{SMPL}$ = 5Msps, $f_{IN}$ = 2kHz**

## Common Mode Output

The $V_{CM}$ pin is an output that provides one-half the voltage present on the REFBUF pin. This voltage can be used to set the common mode of a differential amplifier driving the analog inputs. Bypass $V_{CM}$ to GND with a 0.1µF ceramic capacitor. If $V_{CM}$ is not used it can be left floating, but the parasitic capacitance on the pin needs to be under 10pF.

The $V_{CM}$ output has 1/f noise which for most driver circuits will be removed by the ADC common mode rejection ratio. $V_{CM}$ is not recommended for single-ended to differential circuits that pass the $V_{CM}$ noise to only one ADC input.

## DYNAMIC PERFORMANCE

Fast Fourier Transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2385-16 provides guaranteed tested limits for both AC distortion and noise measurements.

## Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the A/D output. The output is band-limited to frequencies from above DC and below half the sampling frequency. Figure 10 shows that the LTC2385-16 achieves a typical SINAD of 93.9dB at a 5MHz sampling rate with a 2kHz input.
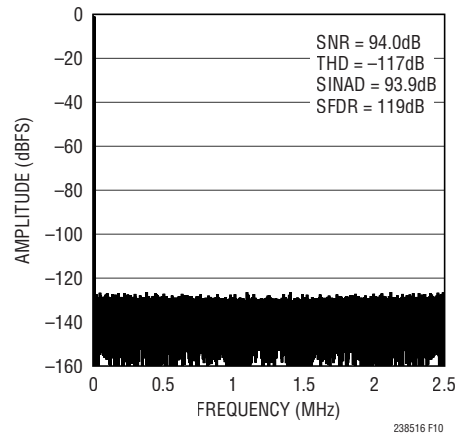
## Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 10 shows that the LTC2385-16 achieves a typical SNR of 94dB at a 5MHz sampling rate with a 2kHz input.

## Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\frac{\sqrt{V2^2 + V3^2 + V4^2 + \ldots + V_n^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through nth harmonics. Figure 10 shows that the LTC2385-16 achieves a typical THD of –117dB at a 5MHz sampling rate with a 2kHz input.

## POWER CONSIDERATIONS

The LTC2385-16 requires three power supplies: $V_{DD}$ (5V), $V_{DDL}$ (2.5V), and $OV_{DD}$ (2.5V). Bypass $V_{DD}$ to GND with a 0.1µF ceramic capacitor close to the pair of pins and a

# APPLICATIONS INFORMATION

10µF ceramic capacitor in parallel. Bypass $V_{DDL}$ to GND with a 0.1µF ceramic capacitor close to the pair of pins and a 10µF ceramic capacitor in parallel. $OV_{DD}$ can come from the same source as $V_{DDL}$ but it should be isolated by a ferrite bead and have its own 0.1µF bypass capacitor.

## Power Supply Sequencing

The LTC2385-16 does not have any specific power supply sequencing requirements. Care should be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2385-16 has a power-on-reset (POR) circuit that will reset the LTC2385-16 at initial power-up or whenever $V_{DD}$ or $V_{DDL}$ drops well below their minimum values. Once the supply voltage re-enters the nominal supply voltage range, the POR will reinitialize the ADC.

## Power-Down Mode

When $\overline{PD}$ is pulled low, LTC2385-16 enters power-down mode. In this state, all internal functions, including the reference and LVDS outputs, are turned off and subsequent conversion requests are ignored. The power consumption drops to a typical value of 10µW. This mode can be used if the LTC2385-16 is inactive for a long period of time and the user wants to minimize power dissipation.

The amount of time required to recover from power-down mode depends on how REFBUF is configured. When using the internal reference buffer with a 10µF bypass capacitor, the ADC will stabilize after 20ms. If REFBUF is externally driven, the recovery time can be significantly less.

## TIMING AND CONTROL

### CNV Timing

The LTC2385-16 conversion is controlled by the CNV+ and CNV− inputs. CNV+/CNV− can be driven directly with an LVDS signal. Alternatively, CNV+ can be driven with a 0V to 2.5V CMOS signal when CNV− is tied to GND. A rising edge on CNV+ will sample the analog inputs and start a conversion. The pulse width of CNV+ should meet the $t_{CNVH}$ and $t_{CNVL}$ specifications in the timing table.

After the LTC2385-16 is powered on, or exits power-down mode, conversion data is invalid for the first two conversion cycles. Subsequent results are accurate as long as the time between conversions meets the $t_{CYC}$ specification.

If the analog input signal has not completely settled when it is sampled, the ADC noise performance will be affected by jitter on the rising edge of CNV+. In this case the rising edge of CNV+ should be driven by a clean low jitter signal. Note that the ADC is less sensitive to jitter on the falling edge of CNV+.

In applications that are insensitive to jitter, CNV can be driven directly from an FPGA.

## Internal Conversion Clock

The LTC2385-16 has an internal clock that is trimmed to achieve a maximum conversion time of 101ns. With a typical acquisition time of 133ns, throughput performance of 5Msps is guaranteed.

## DIGITAL INTERFACE

The LTC2385-16 has a serial LVDS digital interface that is easy to connect to an FPGA. Three LVDS pairs are required: CLK±, DCO±, and DA±. A fourth LVDS pair, DB±, is optional (Figure 11).



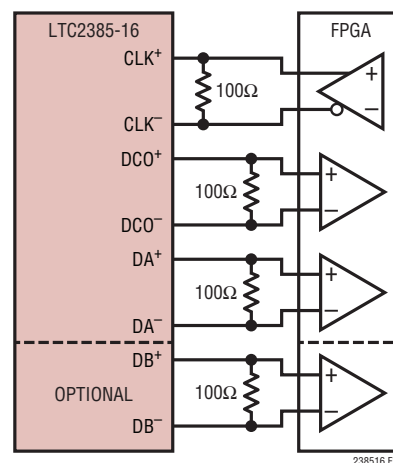**Figure 11. Digital Output Interface to an FPGA**

For more information www.linear.com/LTC2385-16

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The LVDS signals should be routed on the PC board as 100Ω differential transmission lines and terminated at the receiver with 100Ω resistors.

A conversion is started by the rising edge of CNV$^+$. When the conversion is complete, the most-significant data bit is output on DA$^\pm$. Data is then ready to be shifted out by applying a burst of eight clock pulses to the CLK$^\pm$ input. The data on DA$^\pm$ is updated by every edge of CLK$^\pm$. An echoed version of CLK$^\pm$ is output on DCO$^\pm$. The edges of DA$^\pm$ and DCO$^\pm$ are aligned, so DCO$^\pm$ can be used to latch DA$^\pm$ in the FPGA. The timing of a single conversion is shown in Figure 12.

Data must be clocked out after the current conversion is complete, and before the next conversion finishes. The valid time window for clocking out data is shown in Figure 13. Note that it is allowed to be still clocking out data when the next conversion begins.

### Two-Lane Output Mode

At high sample rates the required LVDS interface data rate can reach >200Mbps. Most FPGAs can support this, but if a lower data rate is desired, the two-lane output mode can be used. When the TWOLANES input pin is tied high,

the optional LVDS output DB$^\pm$ is enabled, and data is output two bits at a time on DA$^\pm$ and DB$^\pm$. Enabling the DB$^\pm$ output increases the supply current from OV$_{DD}$ by about 3.6mA. In two-lane mode, four clock pulses are required for CLK$^\pm$ (see Timing Diagrams).

### Output Test Patterns

To allow in-circuit testing of the digital interface to the ADC, there is a test mode that forces the ADC data outputs to known values:

One-Lane Mode:    1010 0000 0111 1111

Two-Lane Mode:    1100 1100 0011 1111

The test pattern is enabled when the TESTPAT pin is brought high.

### BOARD LAYOUT

The LTC2385-16 requires a printed circuit board with a clean unbroken ground plane. A multilayer board with an internal ground plane in the first layer beneath the ADC is recommended. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not
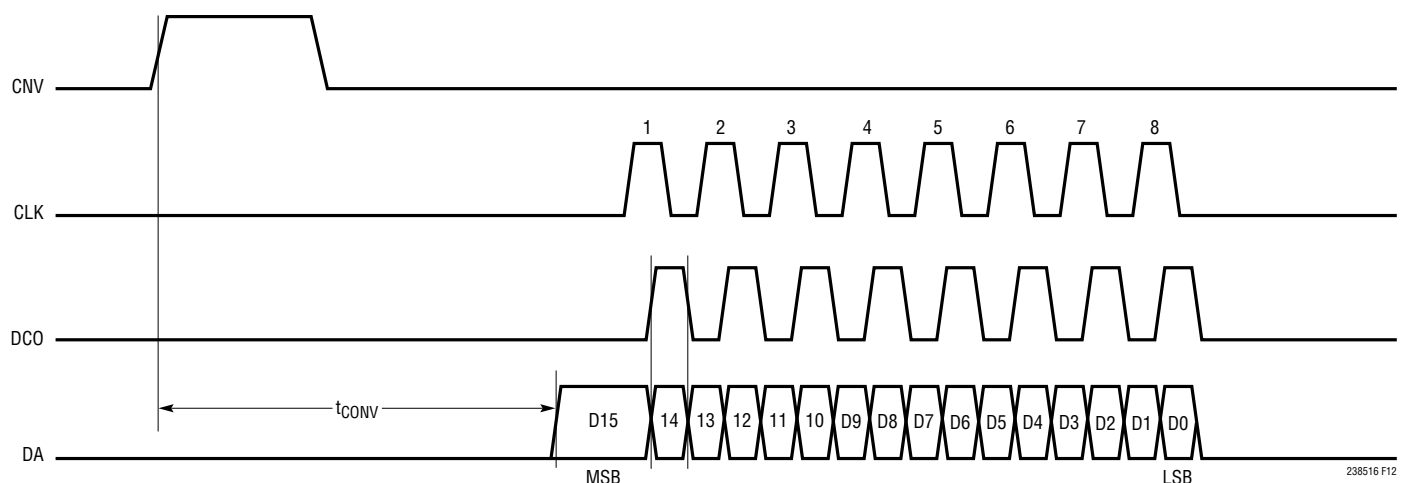


**Figure 12. Timing Diagram for a Single Conversion in One-Lane Mode**
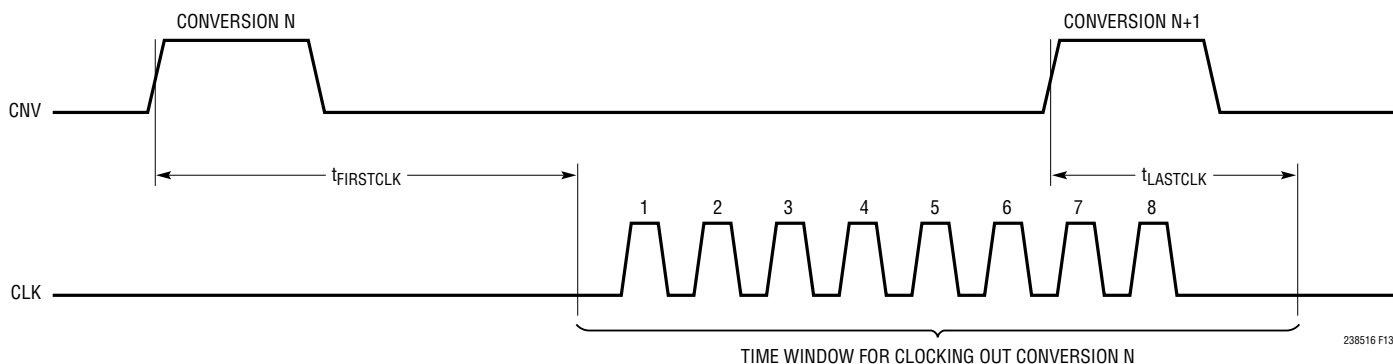
# APPLICATIONS INFORMATION



Figure 13. Valid Time Window for Clocking Out Data

to run any digital track alongside an analog signal track or underneath the ADC.

High quality ceramic bypass capacitors should be used at the $V_{DD}$, $V_{DDL}$, $OV_{DD}$, $V_{CM}$, REFIN, and REFBUF pins. Bypass capacitors must be located as close to the pins as possible. Size 0402 ceramic capacitors are recommended (except for REFBUF). The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

Of particular importance is the capacitor between REFBUF and REFGND, which should be a 10µF (X7R, 0805 size) ceramic capacitor. This capacitor should be on the same side of the circuit board as the ADC, and as close to the device as possible. Adding a second, smaller capacitor in parallel with the 10µF may degrade performance and is not recommended.

The analog inputs, convert start, and digital outputs should not be routed next to each other. Ground fill and grounded vias should be used as barriers to isolate these signals from each other.

**Exposed Package Pad**

For good electrical and thermal performance, the exposed pad on the bottom of the package must be soldered to a large grounded pad on the PC board. This pad should be connected to the internal ground planes by an array of vias.

**Mechanical Stress Shift**

The mechanical stress of mounting a part to a board can cause subtle changes to the SNR and internal voltage reference. The best soldering method is to use IR reflow or convection soldering with a controlled temperature profile. Hand soldering with a heat gun or a soldering iron is not recommended.
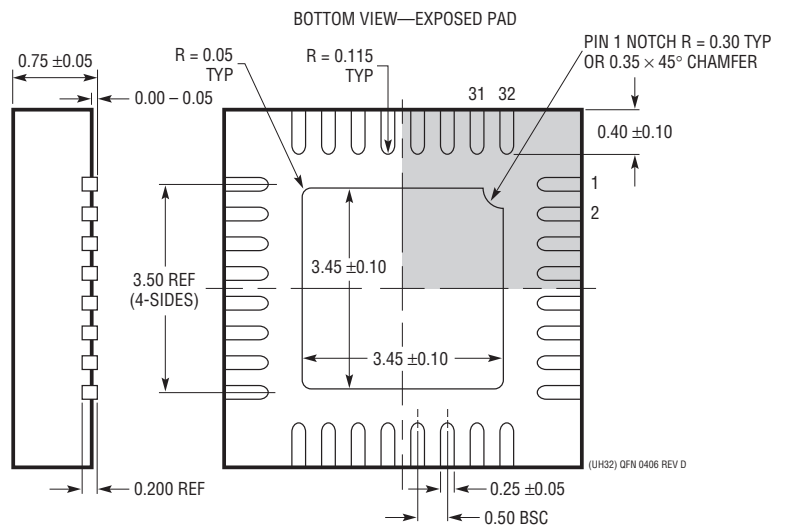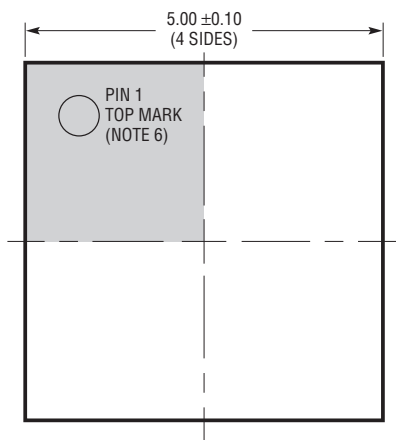
# PACKAGE DESCRIPTION

**Please refer to** http://www.linear.com/product/LTC2385-16#packaging **for the most recent package drawings.**

**UH Package**
**32-Lead Plastic QFN (5mm × 5mm)**
(Reference LTC DWG # 05-08-1693 Rev D)
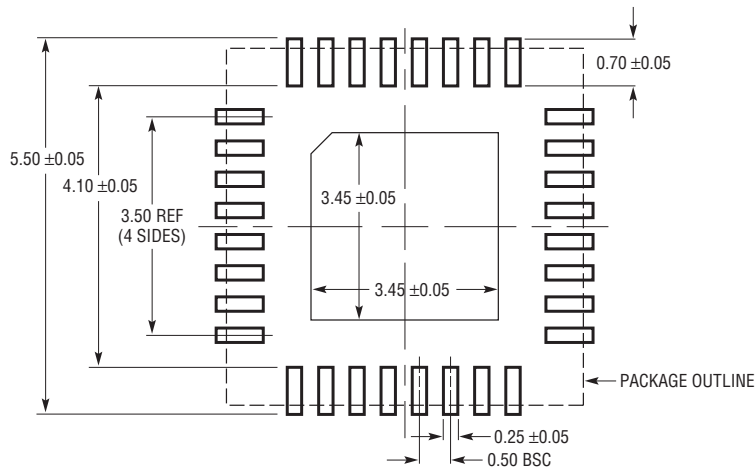


RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE