



# LTC4236

## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

### Supply Voltages

IN1, IN2	-0.3V to 24V
INTV <sub>CC</sub>	-0.3V to 7V
REG	SENSE <sup>+</sup> - 5V to SENSE <sup>+</sup> + 0.3V

### Input Voltages

ON, D2OFF, $\overline{\text{EN}}$	-0.3V to 24V
FTMR, DTMR	-0.3V to INTV <sub>CC</sub> + 0.3V
FB	-0.3V to 7V
SENSE <sup>+</sup> , SENSE <sup>-</sup> , CS <sup>+</sup> , D2SRC	-0.3V to 24V

### Output Voltages

IMON	-0.3V to 7V
FAULT, PWRGD, DSTAT1, DSTAT2	-0.3V to 24V
CPO1, CPO2 (Notes 3, 4)	-0.3V to 35V
DGATE1, DGATE2 (Notes 3, 4)	-0.3V to 35V
HGATE (Note 5)	-0.3V to 35V
OUT	-0.3V to 24V

### Average Currents

FAULT, PWRGD, DSTAT1, DSTAT2	5mA
INTV <sub>CC</sub>	10mA

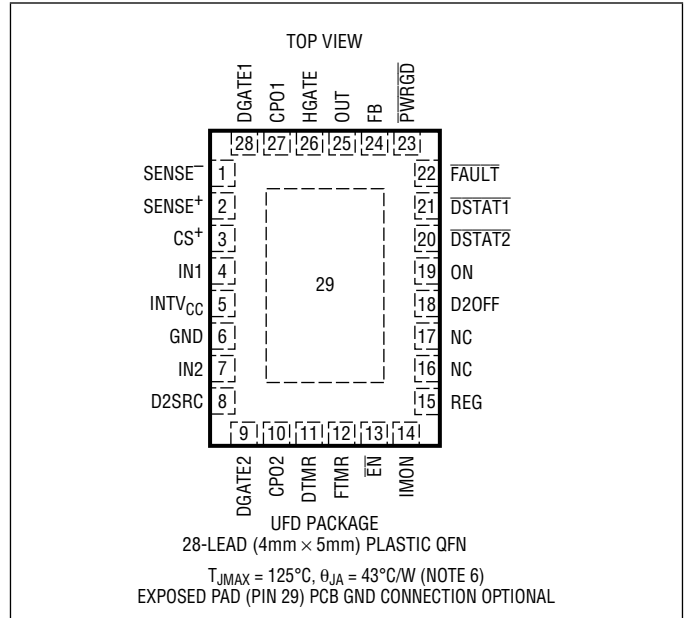
### Operating Ambient Temperature Range

LTC4236C	0°C to 70°C
LTC4236I	-40°C to 85°C

### Storage Temperature Range

	-65°C to 150°C
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## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4236CUFD-1#PBF	LTC4236CUFD-1#TRPBF	42361	28-Lead (4mm x 5mm) Plastic QFN	0°C to 70°C
LTC4236CUFD-2#PBF	LTC4236CUFD-2#TRPBF	42362	28-Lead (4mm x 5mm) Plastic QFN	0°C to 70°C
LTC4236IUFD-1#PBF	LTC4236IUFD-1#TRPBF	42361	28-Lead (4mm x 5mm) Plastic QFN	-40°C to 85°C
LTC4236IUFD-2#PBF	LTC4236IUFD-2#TRPBF	42362	28-Lead (4mm x 5mm) Plastic QFN	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 12\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Supplies</b>							
$V_{IN}$	Input Supply Range	●	2.9		18	V	
$I_{IN}$	Input Supply Current	●		2.7	4	mA	
$V_{INTVCC}$	Internal Regulator Voltage	$I = 0, -500\mu\text{A}$	●	4.5	5	5.5	V
$V_{INTVCC(UVL)}$	Internal $V_{CC}$ Undervoltage Lockout	INTVCC Rising	●	2.1	2.2	2.3	V
$\Delta V_{INTVCC(HYST)}$	Internal $V_{CC}$ Undervoltage Lockout Hysteresis	●	30	60	90	mV	
<b>Ideal Diode Control</b>							
$\Delta V_{FWD(REG)}$	Forward Regulation Voltage ( $V_{INn} - V_{SENSE+}$ )	●	2	15	28	mV	
$\Delta V_{DGATE}$	External N-Channel Gate Drive ( $V_{DGATE1} - V_{IN1}$ ) and ( $V_{DGATE2} - V_{D2SRC}$ )	IN < 7V, $\Delta V_{FWD} = 0.15\text{V}$ ; $I = 0, -1\mu\text{A}$ IN = 7V to 18V, $\Delta V_{FWD} = 0.15\text{V}$ ; $I = 0, -1\mu\text{A}$	● ●	5 10	7 12	14 14	V V
$\Delta V_{DGATE(ST)}$	Diode MOSFET On Detect Threshold ( $V_{DGATE1} - V_{IN1}$ ) and ( $V_{DGATE2} - V_{D2SRC}$ )	DSTAT Pulls Low, $\Delta V_{FWD} = 50\text{mV}$	●	0.3	0.7	1.1	V
$I_{D2SRC}$	D2SRC Pin Current	D2SRC = 0V	●		-90	-130	$\mu\text{A}$
$I_{CPO(UP)}$	CPOn Pull-Up Current	CPO = IN = D2SRC = 2.9V CPO = IN = D2SRC = 18V	● ●	-60 -50	-100 -90	-130 -120	$\mu\text{A}$ $\mu\text{A}$
$I_{DGATE(FPU)}$	DGATEn Fast Pull-Up Current	$\Delta V_{FWD} = 0.2\text{V}$ , $\Delta V_{DGATE} = 0\text{V}$ , CPO = 17V			-1.5		A
$I_{DGATE(FPD)}$	DGATEn Fast Pull-Down Current	$\Delta V_{FWD} = -0.2\text{V}$ , $\Delta V_{DGATE} = 5\text{V}$			1.5		A
$I_{DGATE2(DN)}$	DGATE2 Off Pull-Down Current	D2OFF = 2V, $\Delta V_{DGATE2} = 2.5\text{V}$	●	50	100	200	$\mu\text{A}$
$t_{ON(DGATE)}$	DGATEn Turn-On Delay	$\Delta V_{FWD} = 0.2\text{V}$ , $C_{DGATE} = 10\text{nF}$	●		0.25	0.5	$\mu\text{s}$
$t_{OFF(DGATE)}$	DGATEn Turn-Off Delay	$\Delta V_{FWD} = -0.2\text{V}$ , $C_{DGATE} = 10\text{nF}$	●		0.2	0.5	$\mu\text{s}$
$t_{PLH(DGATE2)}$	D2OFF Low to DGATE2 High	●			50	100	$\mu\text{s}$
<b>Hot Swap Control</b>							
$\Delta V_{SENSE(TH)}$	Current Limit Sense Voltage Threshold ( $V_{SENSE+} - V_{SENSE-}$ )	FB = 1.3V FB = 0V	● ●	22.5 5.8	25 8.3	27.5 10.8	mV mV
$V_{SENSE+(UVL)}$	SENSE+ Undervoltage Lockout	SENSE+ Rising	●	1.8	1.9	2	V
$\Delta V_{SENSE+(HYST)}$	SENSE+ Undervoltage Lockout Hysteresis	●	10	50	90	mV	
$I_{SENSE+}$	SENSE+ Pin Current	SENSE+ = 12V	●	0.3	0.8	1.3	mA
$I_{SENSE-}$	SENSE- Pin Current	SENSE- = 12V	●	10	40	100	$\mu\text{A}$
$I_{CS+}$	CS+ Pin Current	CS+ = 12V, $\Delta V_{SENSE} = 0\text{V}$	●			$\pm 1$	$\mu\text{A}$
$\Delta V_{HGATE}$	External N-Channel Gate Drive ( $V_{HGATE} - V_{OUT}$ )	IN < 7V, $I = 0, -1\mu\text{A}$ IN = 7V to 18V, $I = 0, -1\mu\text{A}$	● ●	5 10	7 12	14 14	V V
$\Delta V_{HGATE(H)}$	Gate High Threshold ( $V_{HGATE} - V_{OUT}$ )	●	3.6	4.2	4.8	V	
$I_{HGATE(UP)}$	External N-Channel Gate Pull-Up Current	Gate Drive On, HGATE = 0V	●	-7	-10	-13	$\mu\text{A}$
$I_{HGATE(DN)}$	External N-Channel Gate Pull-Down Current	Gate Drive Off, OUT = 12V, HGATE = OUT + 5V	●	1	2	4	mA
$I_{HGATE(FPD)}$	External N-Channel Gate Fast Pull-Down Current	Fast Turn-Off, OUT = 12V, HGATE = OUT + 5V	●	100	200	350	mA
$t_{PHL(SENSE)}$	Sense Voltage ( $SENSE+ - SENSE-$ ) High to HGATE Low	$\Delta V_{SENSE} = 200\text{mV}$ , $C_{HGATE} = 10\text{nF}$	●		0.5	1	$\mu\text{s}$
$t_{OFF(HGATE)}$	ON Low to HGATE Low $\overline{EN}$ High to HGATE Low SENSE+ Low to HGATE Low	SENSE+ UVLO	● ● ●		10 20 10	20 40 20	$\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$
$t_D(HGATE)$	ON High, $\overline{EN}$ Low to HGATE Turn-On Delay	DTMR = INTVCC	●	50	100	150	ms
$t_P(HGATE)$	ON to HGATE Propagation Delay	ON = Step 0.8V to 2V	●		10	20	$\mu\text{s}$

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 12\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>Inputs</b>							
$V_{D2OFF(H,TH)}$	D2OFF Pin High Threshold	D2OFF Rising	●	1.21	1.235	1.26	V
$V_{D2OFF(L,TH)}$	D2OFF Pin Low Threshold	D2OFF Falling	●	1.19	1.215	1.24	V
$\Delta V_{D2OFF(HYST)}$	D2OFF Pin Hysteresis		●	10	20	30	mV
$V_{IN(TH)}$	ON, FB Pin Threshold Voltage	Voltage Rising	●	1.21	1.235	1.26	V
$\Delta V_{ON(HYST)}$	ON Pin Hysteresis		●	40	80	120	mV
$\Delta V_{FB(HYST)}$	FB Pin Hysteresis		●	10	20	30	mV
$V_{ON(RESET)}$	ON Pin Fault Reset Threshold Voltage	ON Falling	●	0.57	0.6	0.63	V
$I_{IN(LEAK)}$	Input Leakage Current (ON, FB, D2OFF)	$V = 5\text{V}$	●		0	$\pm 1$	$\mu\text{A}$
$V_{\overline{EN}(TH)}$	$\overline{EN}$ Pin Threshold Voltage	$\overline{EN}$ Rising	●	1.185	1.235	1.284	V
$\Delta V_{\overline{EN}(HYST)}$	$\overline{EN}$ Pin Hysteresis		●	60	110	200	mV
$I_{\overline{EN}(UP)}$	$\overline{EN}$ Pull-Up Current	$\overline{EN} = 1\text{V}$	●	-7	-10	-13	$\mu\text{A}$
$V_{TMR(H)}$	FTMR, DTMR Pin High Threshold		●	1.198	1.235	1.272	V
$V_{TMR(L)}$	FTMR, DTMR Pin Low Threshold		●	0.15	0.2	0.25	V
$I_{FTMR(UP)}$	FTMR Pull-Up Current	FTMR = 1V, In Fault Mode	●	-80	-100	-120	$\mu\text{A}$
$I_{FTMR(DN)}$	FTMR Pull-Down Current	FTMR = 2V, No Faults	●	1.3	2	2.7	$\mu\text{A}$
$D_{RETRY}$	Auto-Retry Duty Cycle		●	0.07	0.15	0.23	%
$I_{DTMR(UP)}$	DTMR Pull-Up Current	DTMR = 0.6V	●	-8	-10	-12	$\mu\text{A}$
$I_{DTMR(DN)}$	DTMR Pull-Down Current	DTMR = 1.5V	●	1	5	10	mA
$\Delta V_{DTMR(TH)}$	DTMR Pin Threshold Voltage ( $V_{DTMR} - V_{INTVCC}$ )	$t_{D(HGATE)}$ Start-Up Delay	●	-0.1	-0.3	-0.5	V
$t_{RST(ON)}$	ON Low to FAULT High		●		20	40	$\mu\text{s}$
$t_{PG(FB)}$	FB Low to PWRGD High		●		20	40	$\mu\text{s}$
<b>Outputs</b>							
$I_{OUT}$	OUT Pin Current	OUT = 11V, IN = 12V, ON = 2V OUT = 13V, IN = 12V, ON = 2V	● ●		40 2.5	100 4	$\mu\text{A}$ mA
$V_{OL}$	Output Low Voltage (FAULT, PWRGD, DSTAT1, DSTAT2)	$I = 1\text{mA}$ $I = 3\text{mA}$	● ●		0.15 0.4	0.4 1.2	V V
$V_{OH}$	Output High Voltage (FAULT, PWRGD)	$I = -1\mu\text{A}$	●	$INTV_{CC} - 1$	$INTV_{CC} - 0.5$		V
$I_{OH}$	Input Leakage Current (FAULT, PWRGD, DSTAT1, DSTAT2)	$V = 18\text{V}$	●		0	$\pm 1$	$\mu\text{A}$
$I_{PU}$	Output Pull-Up Current (FAULT, PWRGD)	$V = 1.5\text{V}$	●	-7	-10	-13	$\mu\text{A}$
<b>Current Monitor</b>							
$\Delta V_{REG}$	Floating Regulator Voltage ( $V_{SENSE+} - V_{REG}$ )	$I_{REG} = \pm 1\mu\text{A}$	●	3.6	4.1	4.6	V
$\Delta V_{SENSE(FS)}$	Input Sense Voltage Full Scale ( $V_{SENSE+} - V_{SENSE-}$ )	$SENSE+ = 12\text{V}$	●	25			mV
$V_{IMON(OS)}$	IMON Input Offset Voltage	$\Delta V_{SENSE} = 0\text{V}$	●			$\pm 150$	$\mu\text{V}$
$G_{IMON}$	IMON Voltage Gain	$\Delta V_{SENSE} = 20\text{mV}$ and $5\text{mV}$	●	99	100	101	V/V
$V_{IMON(MAX)}$	IMON Maximum Output Voltage	$\Delta V_{SENSE} = 70\text{mV}$ , $5\text{V} \leq SENSE+ \leq 18\text{V}$ $\Delta V_{SENSE} = 35\text{mV}$ , $SENSE+ = 2.9\text{V}$	● ●	3.5 2.7		5.5 2.9	V V
$V_{IMON(MIN)}$	IMON Minimum Output Voltage	$\Delta V_{SENSE} = 200\mu\text{V}$	●			40	mV
$R_{IMON(OUT)}$	IMON Output Resistance	$\Delta V_{SENSE} = 200\mu\text{V}$	●	15	20	27	k $\Omega$

## ELECTRICAL CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

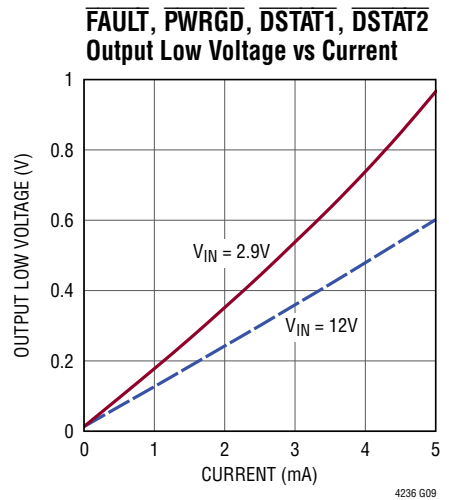
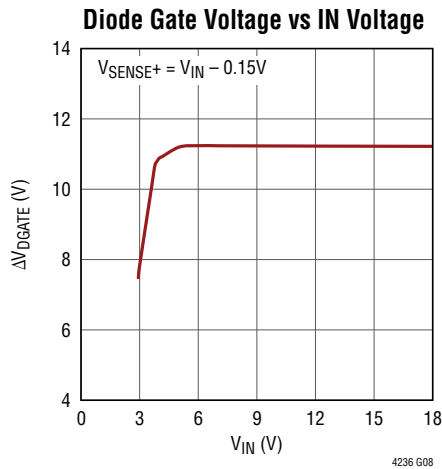
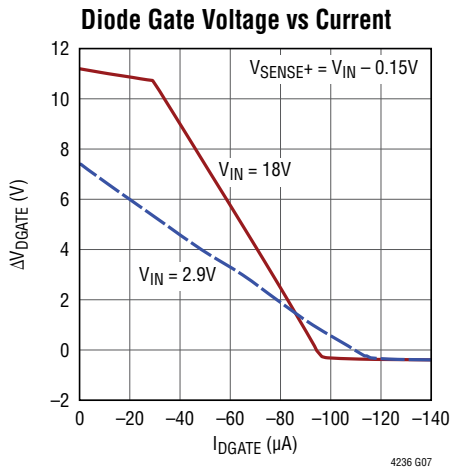
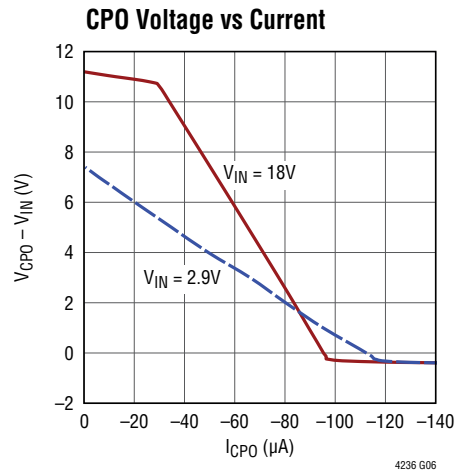
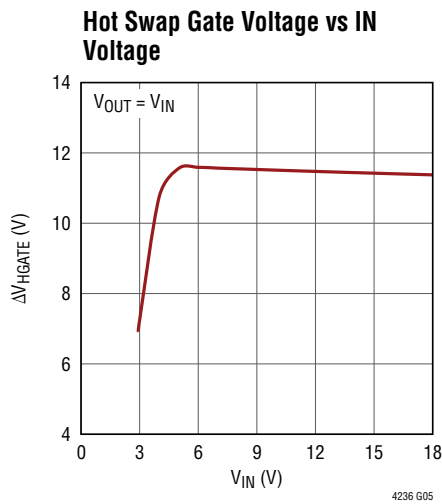
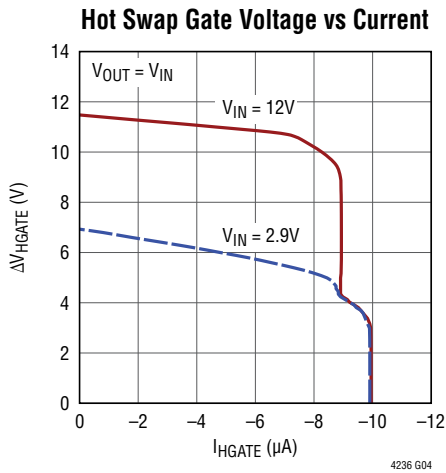
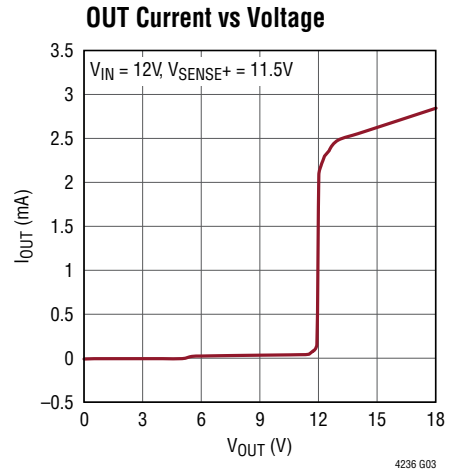
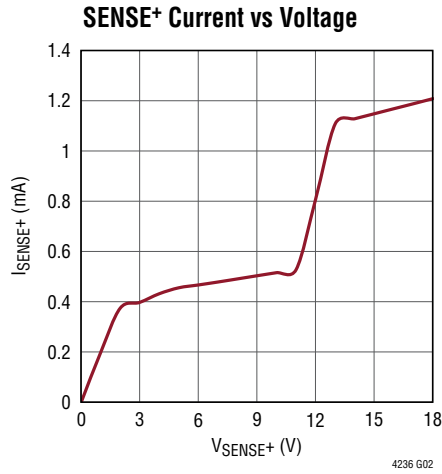
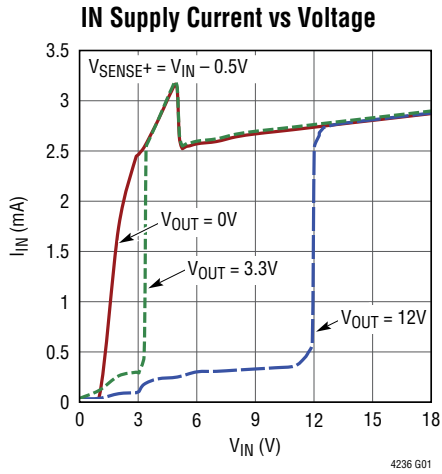
**Note 3:** An internal clamp limits the DGATE1 and CPO1 pins to a minimum of 10V above and a diode below IN1. Driving these pins to voltages beyond the clamp may damage the device.

**Note 4:** An internal clamp limits the DGATE2 and CPO2 pins to a minimum of 10V above and a diode below D2SRC. Driving these pins to voltages beyond the clamp may damage the device.

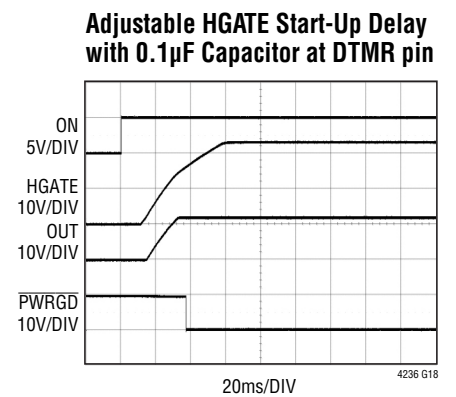
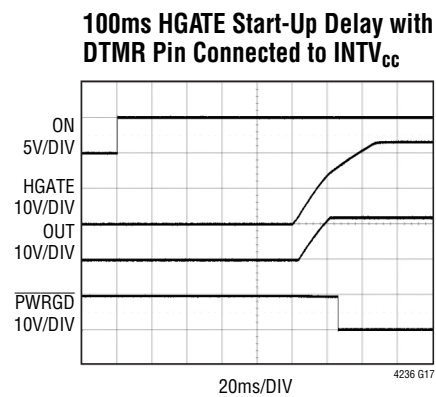
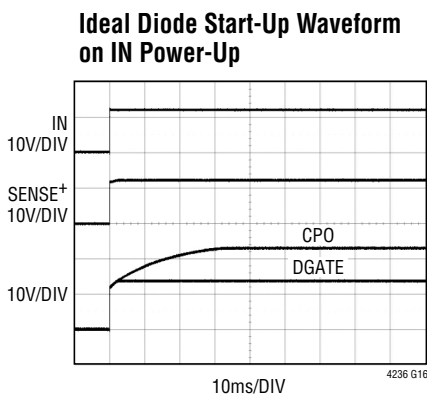
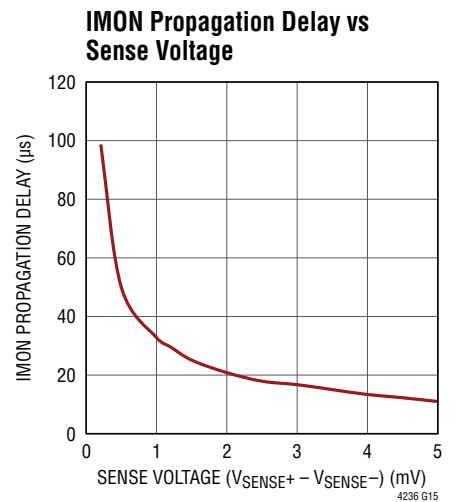
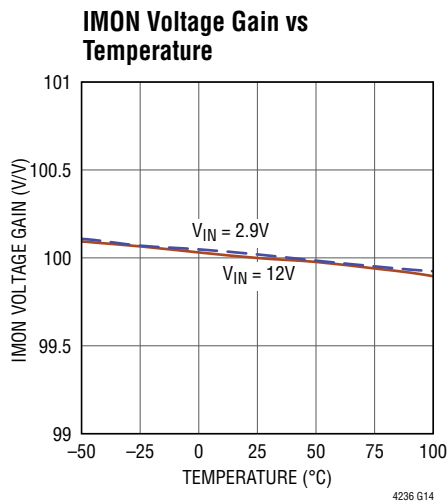
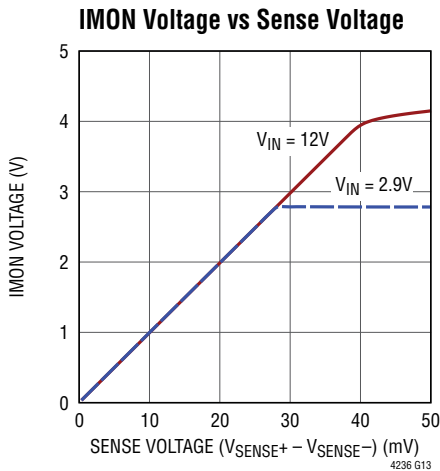
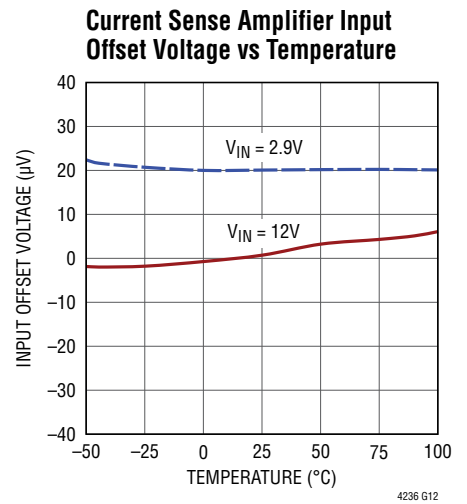
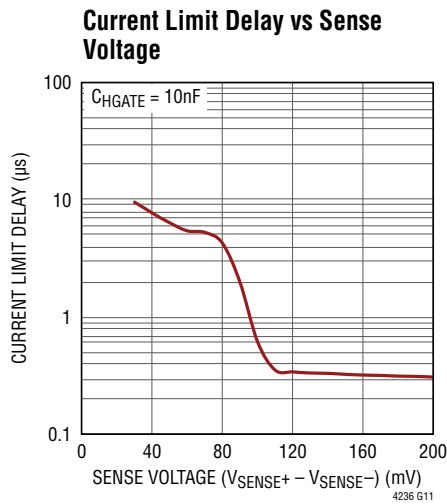
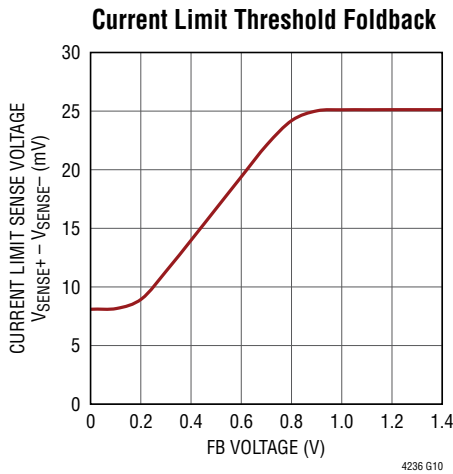
**Note 5:** An internal clamp limits the HGATE pin to a minimum of 10V above and a diode below OUT. Driving this pin to voltages beyond the clamp may damage the device.

**Note 6:** Thermal resistance is specified when the exposed pad is soldered to a 3" x 5", four layer, FR4 board.

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_{IN} = 12\text{V}$ , unless otherwise noted.



**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{V}$ , unless otherwise noted.



## PIN FUNCTIONS

**CPO1, CPO2:** Charge Pump Output. Connect a capacitor from CPO1 or CPO2 to the corresponding IN1 or D2SRC pin. The value of this capacitor is approximately  $10\times$  the gate capacitance ( $C_{ISS}$ ) of the external MOSFET for ideal diode control. The charge stored on this capacitor is used to pull up the ideal diode MOSFET gate during a fast turn-on. Leave this pin open if fast ideal diode turn-on is not needed.

**CS<sup>+</sup>:** Positive Current Sense Input for Current Sense Amplifier. Connect this pin to the input of the current sense resistor. The voltage between CS<sup>+</sup> and SENSE<sup>-</sup> is translated to a ground referenced signal at IMON pin.

**DGATE1, DGATE2:** Ideal Diode MOSFET Gate Drive Output. Connect this pin to the gate of an external N-channel MOSFET for ideal diode control. An internal clamp limits the gate voltage to 12V above and a diode voltage below IN1 or D2SRC. During fast turn-on, a 1.5A pull-up charges DGATE from CPO. During fast turn-off, a 1.5A pull-down discharges DGATE1 to IN1 and DGATE2 to D2SRC.

**D2OFF:** Control Input. A rising edge above 1.235V turns off the external ideal diode MOSFET in the IN2 supply path and a falling edge below 1.215V allows the MOSFET to be turned on. Connect this pin to an external resistive divider from IN1 to make IN1 the higher priority input supply when IN1 and IN2 are equal.

**D2SRC:** Ideal Diode MOSFET Gate Drive Return. Connect this pin to the source of the external N-channel MOSFET switch in the IN2 power path. The gate fast pull-down current returns through this pin when DGATE2 is discharged.

**DSTAT1:** Diode MOSFET Status Output. Open drain output that pulls low when the MOSFET gate drive voltage between DGATE1 and IN1 exceeds 0.7V indicating that the MOSFET diode path is on. Otherwise it goes high impedance. It requires an external pull-up resistor to a positive supply. Leave open if unused.

**DSTAT2:** Diode MOSFET Status Output. Open drain output that pulls low when the MOSFET gate drive voltage between DGATE2 and D2SRC exceeds 0.7V indicating that the MOSFET diode path is on. Otherwise it goes high impedance. It requires an external pull-up resistor to a positive supply. Leave open if unused.

**DTMR:** Debounce Timer Capacitor Terminal. Connect this pin to either INTV<sub>CC</sub> for fixed 100ms delay or an external capacitor to ground for adjustable start-up delay (123ms/ $\mu$ F) when  $\overline{EN}$  toggles low.

**$\overline{EN}$ :** Enable Input. Ground this pin to enable Hot Swap control. If this pin is pulled high, the Hot Swap MOSFET is not allowed to turn on. A 10 $\mu$ A current source pulls this pin up to a diode below INTV<sub>CC</sub>. Upon  $\overline{EN}$  going low when ON is high, there is a start-up delay for debounce as configured at the DTMR pin, after which the fault is cleared.

**FAULT:** Overcurrent Fault Status Output. Output that pulls low when the fault timer expires during an overcurrent fault. Otherwise it is pulled high by a 10 $\mu$ A current source to a diode below INTV<sub>CC</sub>. It may be pulled above INTV<sub>CC</sub> using an external pull-up. Leave open if unused.

**FB:** Foldback and Power Good Comparator Input. Connect this pin to an external resistive divider from OUT. If the voltage falls below 1.215V, the  $\overline{PWRGD}$  pin pulls high to indicate the power is bad. If the voltage falls below 0.9V, the output power is considered bad and the current limit is reduced. Tie to INTV<sub>CC</sub> to disable foldback.

**FTMR:** Fault Timer Capacitor Terminal. Connect a capacitor between this pin and ground to set a 12ms/ $\mu$ F duration for current limit before the external Hot Swap MOSFET is turned off. The duration of the off time is 8s/ $\mu$ F, resulting in a 0.15% duty cycle.

**GND:** Device Ground.



## PIN FUNCTIONS

**HGATE:** Hot Swap MOSFET Gate Drive Output. Connect this pin to the gate of the external N-channel MOSFET for Hot Swap control. An internal 10 $\mu$ A current source charges the MOSFET gate. An internal clamp limits the gate voltage to 12V above and a diode voltage below OUT. During an undervoltage generated turn-off, a 2mA pull-down discharges HGATE to ground. During an output short or INTV<sub>CC</sub> undervoltage lockout, a fast 200mA pull-down discharges HGATE to OUT.

**IN1, IN2:** Positive Supply Input and Ideal Diode MOSFET Gate Drive Return. Connect this pin to the power input side of the external ideal diode MOSFET. The 5V INTV<sub>CC</sub> supply is generated from IN1, IN2 and OUT via an internal diode-OR. The voltage sensed at this pin is used to control DGATE. The gate fast pull-down current returns through IN1 pin when DGATE1 is discharged.

**INTV<sub>CC</sub>:** Internal 5V Supply Decoupling Output. This pin must have a 0.1 $\mu$ F or larger capacitor to GND. An external load of less than 500 $\mu$ A can be connected at this pin. An undervoltage lockout threshold of 2.2V will turn off both MOSFETs.

**IMON:** Current Sense Monitoring Output. This pin voltage is proportional to the sense voltage across the current sense resistor with a voltage gain of 100. An internal 20k resistor is connected from this pin to ground.

**ON:** ON Control Input. A rising edge above 1.235V turns on the external Hot Swap MOSFET and a falling edge below 1.155V turns it off. Connect this pin to an external resistive divider from SENSE<sup>+</sup> to monitor the supply undervoltage condition. Pulling the ON pin below 0.6V resets the fault latch after an overcurrent fault. Tie to INTV<sub>CC</sub> if unused.

**OUT:** Hot Swap MOSFET Gate Drive Return. Connect this pin to the output side of the external MOSFET. The gate fast pull-down current returns through this pin when HGATE is discharged.

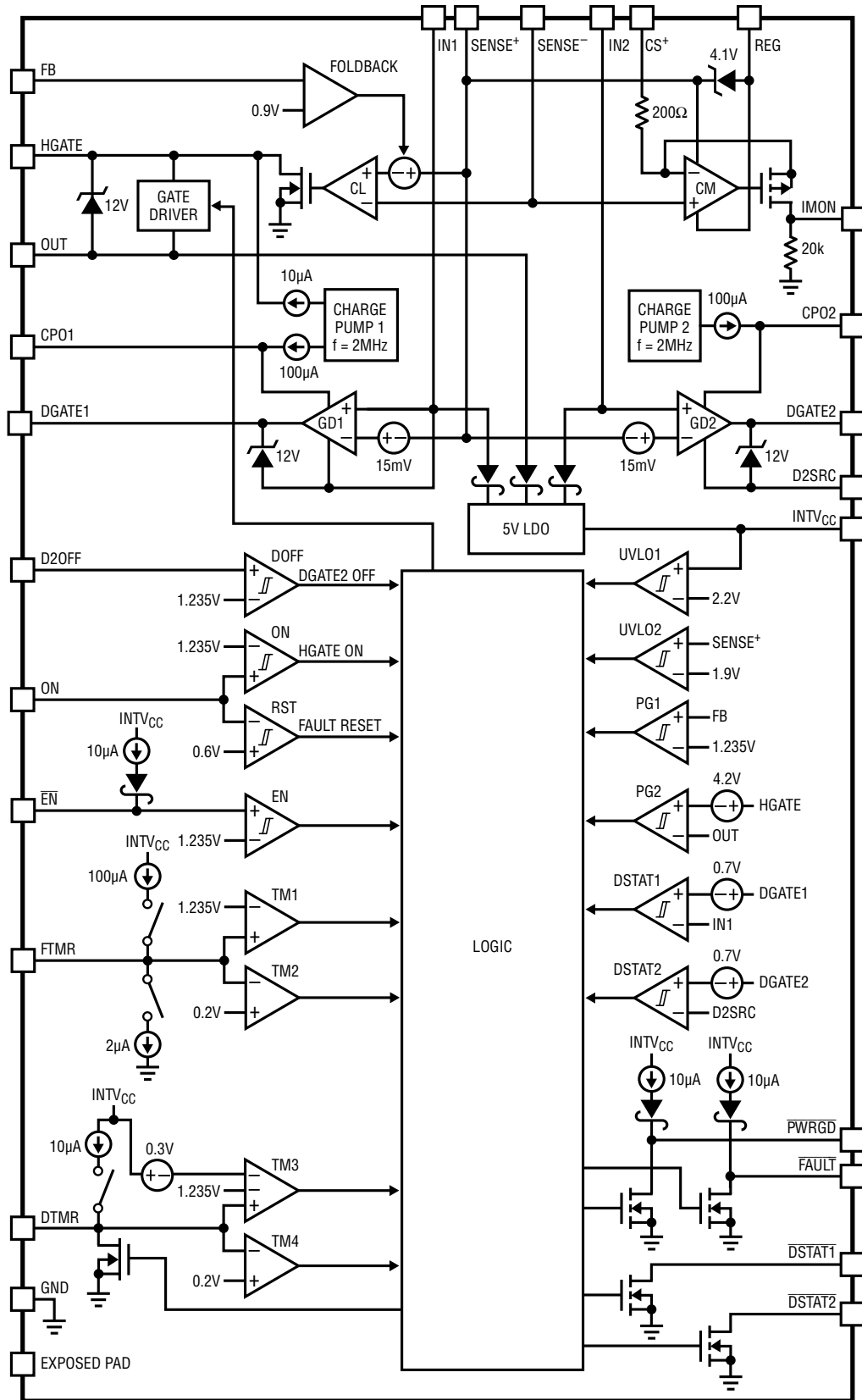
**PWRGD:** Power Status Output. Output that pulls low when the FB pin rises above 1.235V and the MOSFET gate drive between HGATE and OUT exceeds 4.2V. Otherwise it is pulled high by a 10 $\mu$ A current source to a diode below INTV<sub>CC</sub>. It may be pulled above INTV<sub>CC</sub> using an external pull-up. Leave open if unused.

**REG:** Internal Regulated Supply for Current Sense Amplifier. A 0.1 $\mu$ F or larger capacitor should be tied from REG to SENSE<sup>+</sup>. This pin is not designed to drive external circuits.

**SENSE<sup>+</sup>:** Positive Current Sense Input. Connect this pin to the diode-OR output of the external ideal diode MOSFETs and input of the current sense resistor. The voltage sensed at this pin is used for monitoring the current limit and also to control DGATE for forward voltage regulation and reverse turn-off. This pin has an undervoltage lockout threshold of 1.9V that will turn off the Hot Swap MOSFET.

**SENSE<sup>-</sup>:** Negative Current Sense Input. Connect this pin to the output of the current sense resistor. The current limit circuit controls HGATE to limit the voltage between SENSE<sup>+</sup> and SENSE<sup>-</sup> to 25mV or less depending on the voltage at the FB pin.

**BLOCK DIAGRAM**



4236 BD

4236f

## OPERATION

The LTC4236 functions as an input supply diode-OR with inrush current limiting and overcurrent protection by controlling the external N-channel MOSFETs ( $M_{D1}$ ,  $M_{D2}$  and  $M_H$ ) on a supply path. This allows boards to be safely inserted and removed in systems with a backplane powered by redundant supplies. The LTC4236 has a single Hot Swap controller and two separate ideal diode controllers, each providing independent control for the two input supplies.

When the LTC4236 is first powered up, the gates of the external MOSFETs are held low, keeping them off. As the DGATE2 pull-up can be disabled by the D2OFF pin, DGATE2 will pull high only when the D2OFF pin is pulled low. The gate drive amplifier (GD1, GD2) monitors the voltage between the IN and SENSE+ pins and drives the respective DGATE pin. The amplifier quickly pulls up the DGATE pin, turning on the MOSFET for ideal diode control, when it senses a large forward voltage drop. With the ideal diode MOSFETs acting as input supply diode-OR, the SENSE+ pin voltage rises to the highest of the supplies at the IN1 and IN2 pins. An external capacitor connected at the CPO pin provides the charge needed to quickly turn on the ideal diode MOSFET. An internal charge pump charges up this capacitor at device power-up. The DGATE pin sources current from the CPO pin and sinks current into the IN1, D2SRC and GND pins. When the DGATE1 to IN1 or DGATE2 to D2SRC voltage exceeds 0.7V, the respective  $\overline{\text{DSTAT}}$  pin pulls low to indicate that the ideal diode MOSFET is turned on.

Pulling the ON pin high and  $\overline{\text{EN}}$  pin low initiates a debounce timing cycle that can be a fixed 100ms or adjustable delay as configured at the DTMR pin. After this timing cycle, a 10 $\mu$ A current source from the charge pump ramps up the HGATE pin. When the Hot Swap MOSFET turns on, the inrush current is limited at a level set by an external sense resistor ( $R_S$ ) connected between the SENSE+ and SENSE- pins. An active current limit amplifier (CL) servos the gate of the MOSFET to 25mV or less across the current sense resistor depending on the voltage at the FB pin. Inrush current can be further reduced, if desired, by adding a capacitor from HGATE to GND. When FB voltage

rises above 1.235V and the MOSFET's gate drive (HGATE to OUT voltage) exceeds 4.2V, the  $\overline{\text{PWRGD}}$  pin pulls low.

The high side current sense amplifier (CM) provides accurate monitoring of current through the current sense resistor. The sense voltage is amplified by 100 times and level shifted from the positive rail to a ground-referred output at the IMON pin. The output signal is analog and may be used as is or measured with an ADC.

When the ideal diode MOSFET is turned on, the gate drive amplifier controls DGATE to servo the forward voltage drop ( $V_{\text{IN}} - V_{\text{SENSE+}}$ ) across the MOSFET to 15mV. If the load current causes more than 15mV of voltage drop, the gate voltage rises to enhance the MOSFET. For large output currents, the MOSFET's gate is driven fully on and the voltage drop is equal to  $I_{\text{LOAD}} \cdot R_{\text{DS(ON)}}$  of the MOSFET.

In the case of an input supply short-circuit when the MOSFETs are conducting, a large reverse current starts flowing from the load towards the input. The gate drive amplifier detects this failure condition and turns off the ideal diode MOSFET by pulling down the DGATE pin.

In the case where an overcurrent fault occurs on the supply output, the current is limited with foldback. After a delay set by 100 $\mu$ A charging the FTMR pin capacitor, the fault timer expires and pulls the HGATE pin low, turning off the Hot Swap MOSFET. The  $\overline{\text{FAULT}}$  pin is also latched low. At this point, the DGATE pin continues to pull high and keeps the ideal diode MOSFET on.

Internal clamps limit both the DGATE1 and CPO1 to IN1, and DGATE2 and CPO2 to D2SRC voltages to 12V. The same clamps also limit the DGATE and CPO pins to a diode voltage below the IN1 or D2SRC pins. Another internal clamp limits the HGATE to OUT voltage to 12V and also clamps the HGATE pin to a diode voltage below the OUT pin.

Power to the LTC4236 is supplied from either the IN or OUT pins, through an internal diode-OR circuit to a low dropout regulator (LDO). That LDO generates a 5V supply at the INTV<sub>CC</sub> pin and powers the LTC4236's internal low voltage circuitry.

## APPLICATIONS INFORMATION

High availability systems often employ parallel-connected power supplies or battery feeds to achieve redundancy and enhance system reliability. Power ORing diodes are commonly used to connect these supplies at the point of load at the expense of power loss due to significant diode forward voltage drop. The LTC4236 minimizes this power loss by using external N-channel MOSFETs as the pass elements, allowing for a low voltage drop from the supply to the load when the MOSFETs are turned on. When an input source voltage drops below the output common supply voltage, the appropriate MOSFET is turned off, thereby matching the function and performance of an ideal diode. By adding a current sense resistor and a Hot Swap MOSFET after the parallel-connected ideal diode MOSFETs, the LTC4236 enhances the ideal diode performance with inrush current limiting and overcurrent protection (see Figure 1). This allows the board to be safely inserted and removed from a live backplane without damaging the connector.

### Internal V<sub>CC</sub> Supply

The LTC4236 operates with an input supply from 2.9V to 18V. The power supply to the device is internally regulated at 5V by a low dropout regulator (LDO) with an output at the INTV<sub>CC</sub> pin. An internal diode-OR circuit selects the highest of the supplies at the IN and OUT pins to power the device through the LDO. The diode-OR scheme permits the device's power to be kept alive by the OUT voltage when the IN supplies have collapsed or shut off.

An undervoltage lockout circuit prevents all of the MOSFETs from turning on until the INTV<sub>CC</sub> voltage exceeds 2.2V. A 0.1μF capacitor is recommended between the INTV<sub>CC</sub> and GND pins, close to the device for bypassing. No external supply should be connected at the INTV<sub>CC</sub> pin so as not to affect the LDO's operation. A small external load of less than 500μA can be connected at the INTV<sub>CC</sub> pin.

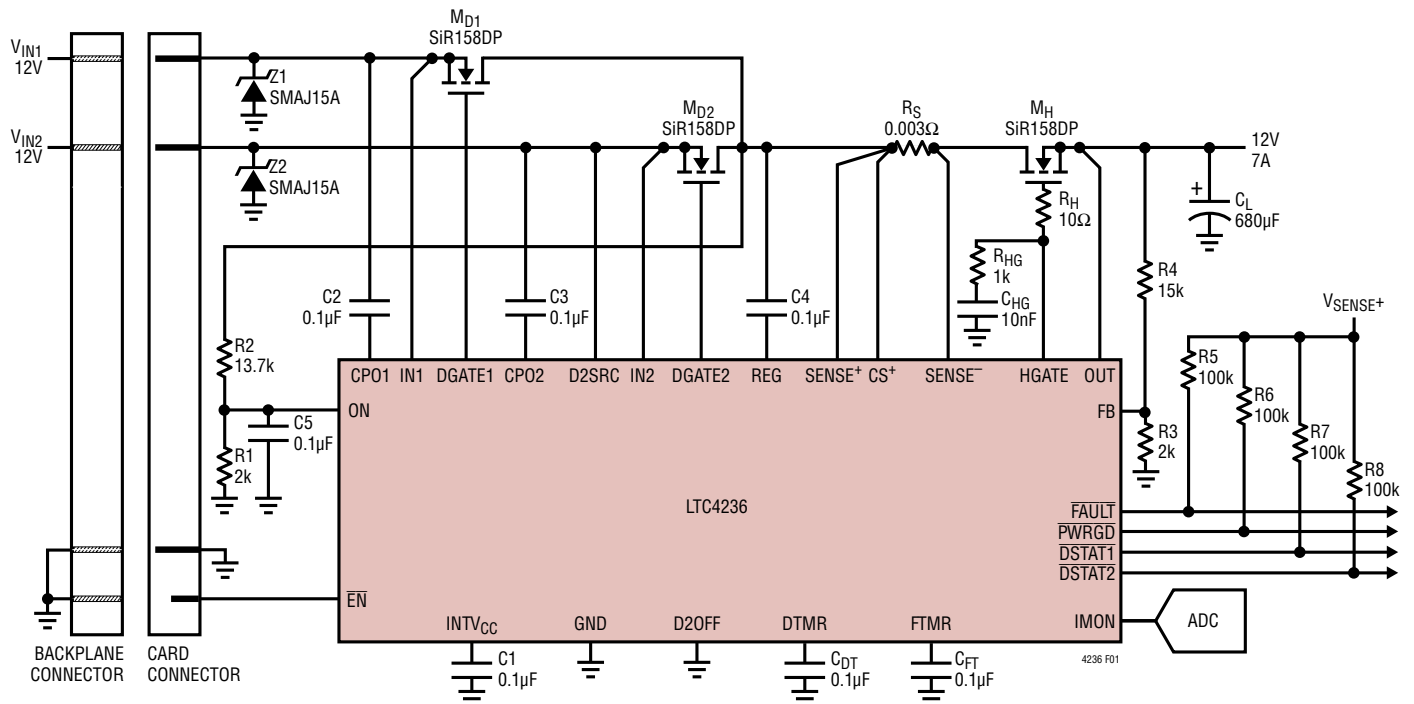


Figure 1. Card Resident Diode-OR with Hot Swap Application

## APPLICATIONS INFORMATION

### Turn-On Sequence

The board power supply at the OUT pin is controlled with external N-channel MOSFETs ( $M_{D1}$ ,  $M_{D2}$  and  $M_H$ ) in Figure 1. The ideal diode MOSFETs connected in parallel on the supply side function as a diode-OR, while  $M_H$  on the load side acts as a Hot Swap MOSFET controlling the power supplied to the output load. The sense resistor  $R_S$  monitors the load current for overcurrent detection. The HGATE capacitor  $C_{HG}$  controls the gate slew rate to limit the inrush current. Resistor  $R_{HG}$  with  $C_{HG}$  compensates the current control loop, while  $R_H$  prevents high frequency oscillations in the Hot Swap MOSFET.

During a normal power-up, the ideal diode MOSFETs turn on first. As soon as the internally generated supply,  $INTV_{CC}$ , rises above its 2.2V undervoltage lockout threshold, the internal charge pump is allowed to charge up the CPO pins. Because the ideal diode MOSFETs are connected in parallel as a diode-OR, the SENSE<sup>+</sup> pin voltage approaches the highest of the supplies at the IN1 and IN2 pins. The MOSFET associated with the lower input supply voltage will be turned off by the corresponding gate drive amplifier.

Before the Hot Swap MOSFET can be turned on,  $\overline{EN}$  must remain low and ON must remain high for a debounce cycle as configured at the DTMR pin, to ensure that any contact bounces during the insertion have ceased. At the end of the debounce cycle, the internal fault latch is cleared. The Hot Swap MOSFET is then allowed to turn on by charging up HGATE with a 10 $\mu$ A current source from the charge pump. The voltage at the HGATE pin rises with a slope equal to 10 $\mu$ A/ $C_{HG}$  and the supply inrush current flowing into the load capacitor  $C_L$  is limited to:

$$I_{INRUSH} = \frac{C_L}{C_{HG}} \cdot 10\mu A$$

The OUT voltage follows the HGATE voltage when the Hot Swap MOSFET turns on. If the voltage across the current sense resistor  $R_S$  becomes too high based on the FB pin voltage, the inrush current will be limited by the internal current limiting circuitry. Once the MOSFET gate overdrive exceeds 4.2V and the FB pin voltage is above 1.235V, the  $\overline{PWRGD}$  pin pulls low to indicate that the power is good.

Once OUT reaches the input supply voltage, HGATE continues to ramp up. An internal 12V clamp limits the HGATE voltage above OUT.

When the ideal diode MOSFET is turned on, the gate drive amplifier controls the gate of the MOSFET to servo the forward voltage drop across the MOSFET to 15mV. If the load current causes more than 15mV of drop, the MOSFET gate is driven fully on and the voltage drop is equal to  $I_{LOAD} \cdot R_{DS(ON)}$ .

### Turn-Off Sequence

The external MOSFETs can be turned off by a variety of conditions. A normal turn-off for the Hot Swap MOSFET is initiated by pulling the ON pin below its 1.155V threshold (80mV ON pin hysteresis), or pulling the  $\overline{EN}$  pin above its 1.235V threshold. Additionally, an overcurrent fault that exceeds the fault timer period also turns off the Hot Swap MOSFET. Normally, the LTC4236 turns off the MOSFET by pulling the HGATE pin to ground with a 2mA current sink.

All of the MOSFETs turn off when  $INTV_{CC}$  falls below its undervoltage lockout threshold (2.2V). The DGATE pin is pulled down with a 100 $\mu$ A current to one diode voltage below the IN1 or D2SRC pins, while the HGATE pin is pulled down to the OUT pin by a 200mA current. When D2OFF is pulled high above 1.235V, the ideal diode MOSFET in the IN2 power path is turned off with DGATE2 pulled low by a 100 $\mu$ A current.

The gate drive amplifier controls the ideal diode MOSFET to prevent reverse current when the input supply falls below SENSE<sup>+</sup>. If the input supply collapses quickly, the gate drive amplifier turns off the ideal diode MOSFET with a fast pull-down circuit. If the input supply falls at a more modest rate, the gate drive amplifier controls the MOSFET to maintain SENSE<sup>+</sup> at 15mV below IN.

### Board Presence Detect with $\overline{EN}$

If ON is high when the  $\overline{EN}$  pin goes low, indicating a board presence, the LTC4236 initiates a timing cycle as configured at the DTMR pin for contact debounce. It defaults to internal 100ms delay if DTMR is tied to  $INTV_{CC}$ . If an external capacitor  $C_{DT}$  is connected from the DTMR pin to GND, the delay is given by charging the capacitor to 1.235V with



## APPLICATIONS INFORMATION

a  $10\mu\text{A}$  current. Thereafter, the capacitor is discharged to ground by a  $5\text{mA}$  current. For a given debounce delay, the equation for setting the external capacitor  $C_{DT}$  value is:

$$C_{DT} = t_{DB} \bullet 0.0081 \text{ } [\mu\text{F}/\text{ms}]$$

Upon board insertion, any bounces on the  $\overline{\text{EN}}$  pin restart the timing cycle. When the debounce timing cycle is done, the internal fault latch is cleared. If the  $\overline{\text{EN}}$  pin remains low at the end of the timing cycle, HGATE is charged up with a  $10\mu\text{A}$  current source to turn on the Hot Swap MOSFET.

If the  $\overline{\text{EN}}$  pin goes high, indicating a board removal, the HGATE pin is pulled low with a  $2\text{mA}$  current sink after a  $20\mu\text{s}$  delay, turning off the Hot Swap MOSFET without clearing any latched fault.

### Overcurrent Fault

The LTC4236 features an adjustable current limit with foldback that protects the external MOSFET against short circuits or excessive load current. The voltage across the external sense resistor  $R_S$  is monitored by an active current limit amplifier. The amplifier controls the gate of the Hot Swap MOSFET to reduce the load current as a function of the output voltage sensed by the FB pin during active current limit. A graph in the Typical Performance Characteristics shows the current limit sense voltage versus FB voltage.

An overcurrent fault occurs when the output has been in current limit for longer than the fault timer period configured at the FTMR pin. Current limiting begins when the sense voltage between the SENSE<sup>+</sup> and SENSE<sup>-</sup> pins reaches  $8.3\text{mV}$  to  $25\text{mV}$  depending on the FB pin voltage. The gate of the Hot Swap MOSFET is brought under control by the current limit amplifier and the output current is regulated to limit the sense voltage to less than  $25\text{mV}$ . At this point, the fault timer starts with a  $100\mu\text{A}$  current charging the FTMR pin capacitor. If the FTMR pin voltage exceeds its  $1.235\text{V}$  threshold, the external MOSFET turns off with HGATE pulled to ground by  $2\text{mA}$  and  $\overline{\text{FAULT}}$  pulls low.

After the Hot Swap MOSFET turns off, the FTMR pin capacitor is discharged with a  $2\mu\text{A}$  pull-down current until its threshold reaches  $0.2\text{V}$ . This is followed by a cool-off period of 14 timing cycles as described in the FTMR Pin Functions. Figure 2 shows an overcurrent fault on the 12V output.

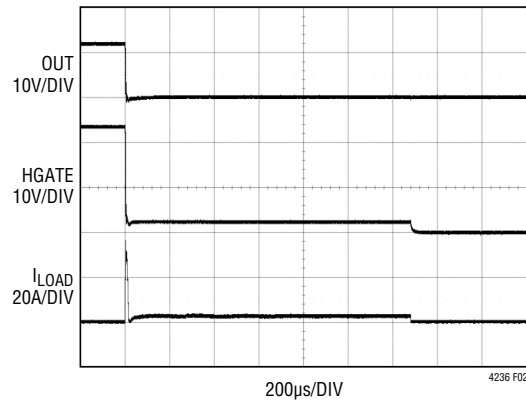


Figure 2. Overcurrent Fault on 12V Output

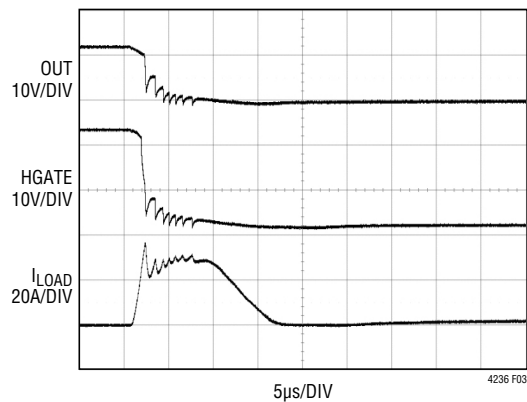


Figure 3. Severe Short-Circuit on 12V Output

In the event of a severe short-circuit fault on the 12V output as shown in Figure 3, the output current can surge to tens of amperes. The LTC4236 responds within  $1\mu\text{s}$  to bring the current under control by pulling the HGATE to OUT voltage down to zero volts. Almost immediately, the gate of the Hot Swap MOSFET recovers rapidly due to the charge stored in the  $R_{HG}$  and  $C_{HG}$  network and current is actively limited until the fault timer expires. Due to parasitic supply lead inductance, an input supply without any bypass capacitor may collapse during the high current surge and then spike upwards when the current is interrupted. Figure 9 shows the input supply transient suppressors comprising of  $Z1$ ,  $R_{SNUB1}$ ,  $C_{SNUB1}$  and  $Z2$ ,  $R_{SNUB2}$ ,  $C_{SNUB2}$  for the two supplies if there is no input capacitance.

### FTMR Pin Functions

An external capacitor  $C_{FT}$  connected from the FTMR pin to GND serves as fault timing when the supply output is

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## APPLICATIONS INFORMATION

in active current limit. When the voltage across the sense resistor exceeds the foldback current limit threshold (from 25mV to 8.3mV), FTMR pulls up with 100 $\mu$ A. Otherwise, it pulls down with 2 $\mu$ A. The fault timer expires when the 1.235V FTMR threshold is exceeded, causing the  $\overline{\text{FAULT}}$  pin to pull low. For a given fault timer period, the equation for setting the external capacitor  $C_{\text{FT}}$  value is:

$$C_{\text{FT}} = t_{\text{FT}} \cdot 0.083 \text{ } [\mu\text{F/ms}]$$

After the fault timer expires, the FTMR pin capacitor pulls down with 2 $\mu$ A from the 1.235V FTMR threshold until it reaches 0.2V. Then, it completes 14 cooling cycles consisting of the FTMR pin capacitor charging to 1.235V with a 100 $\mu$ A current and discharging to 0.2V with a 2 $\mu$ A current. At that point, the HGATE pin voltage is allowed to start up if the fault has been cleared as described in the Resetting Fault section. When the latched fault is cleared during the cool-off period, the  $\overline{\text{FAULT}}$  pin pulls high. The total cool-off time for the MOSFET after an overcurrent fault is:

$$t_{\text{COOL}} = C_{\text{FT}} \cdot 8 \text{ } [\text{s}/\mu\text{F}]$$

After the cool-off period, the HGATE pin is only allowed to pull up if the fault has been cleared for the latching part. For the auto-retry part, the latched fault is cleared automatically following the cool-off period and the HGATE pin voltage is allowed to restart.

### Resetting Fault (LTC4236-1)

For the latching part, an overcurrent fault is latched after the fault timer expires and the  $\overline{\text{FAULT}}$  pin is asserted low. Only the Hot Swap MOSFET is turned off and the ideal diode MOSFETs are not affected.

To reset a latched fault and restart the output, pull the ON pin below 0.6V for more than 100 $\mu$ s and then high above 1.235V. The fault latch resets and the  $\overline{\text{FAULT}}$  pin de-asserts on the falling edge of the ON pin. When ON goes high again and the cool-off cycle has completed, a debounce timing cycle is initiated before the HGATE pin voltage restarts. Toggling the  $\overline{\text{EN}}$  pin high and then low again also resets a fault, but the  $\overline{\text{FAULT}}$  pin pulls high at the end of the debounce cycle before the HGATE pin voltage starts up. Bringing all the supplies below the  $\text{INTV}_{\text{CC}}$  undervoltage lockout threshold (2.2V) shuts off all the MOSFETs and resets the fault latch. A debounce cycle is

initiated before a normal start-up when any of the supplies is restored above the  $\text{INTV}_{\text{CC}}$  UVLO threshold.

### Auto-Retry after a Fault (LTC4236-2)

For the auto-retry part, the latched fault is reset automatically at the end of the cool-off period as described in the FTMR Pin Functions section. At the end of the cool-off period, the fault latch is cleared and  $\overline{\text{FAULT}}$  pulls high. The HGATE pin voltage is allowed to start up and turn on the Hot Swap MOSFET. If the output short persists, the supply powers up into a short with active current limiting until the fault timer expires and  $\overline{\text{FAULT}}$  again pulls low. A new cool-off cycle begins with FTMR ramping down with a 2 $\mu$ A current. The whole process repeats itself until the output short is removed. Since  $t_{\text{FT}}$  and  $t_{\text{COOL}}$  are a function of FTMR capacitance  $C_{\text{FT}}$ , the auto-retry cycle is equal to 0.15%, irrespective of  $C_{\text{FT}}$ .

Figure 4 shows an auto-retry sequence after an overcurrent fault.

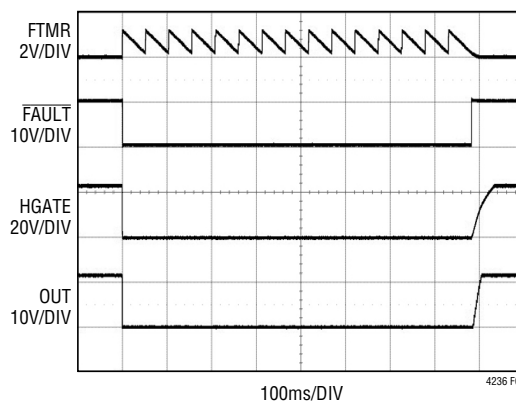


Figure 4. Auto-Retry Sequence After a Fault

### Monitor Undervoltage Fault

The ON pin functions as a turn-on control and an input supply monitor. A resistive divider connected between the supply diode-OR output (SENSE+) and GND at the ON pin monitors the supply for undervoltage condition. The undervoltage threshold is set by proper selection of the resistors at the ON rising threshold voltage (1.235V).

For Figure 1, if  $R_1 = 2\text{k}$ ,  $R_2 = 13.7\text{k}$ , the input supply undervoltage threshold is set to 9.7V.

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An undervoltage fault occurs if the diode-OR output supply falls below its undervoltage threshold. If the ON pin voltage falls below 1.155V but remains above 0.6V, the Hot Swap MOSFET is turned off by a 2mA pull-down from HGATE to ground. The Hot Swap MOSFET turns back on instantly without the debounce cycle when the diode-OR output supply rises above its undervoltage threshold. However, if the ON pin voltage drops below 0.6V, it turns off the Hot Swap MOSFET and clears the fault latch. The Hot Swap MOSFET turns back on only after a debounce cycle when the diode-OR output supply is restored above its undervoltage threshold.

During the undervoltage fault condition,  $\overline{\text{FAULT}}$  will not be pulled low but  $\overline{\text{PWRGD}}$  will be pulled high as HGATE is pulled low. The ideal diode function controlled by the ideal diode MOSFET is not affected by the undervoltage (UV) fault condition.

### Power Good Monitor

Internal circuitry monitors the MOSFET gate overdrive between the HGATE and OUT pins. Also, the FB pin that connects to OUT through a resistive divider is used to determine a power good condition. The power good comparator drives high when the FB pin rises above 1.235V, and drives low when FB falls below 1.215V. The power good status for the input supply is reported via an open-drain output,  $\overline{\text{PWRGD}}$ . It is normally pulled high by an external pull-up resistor or the internal 10 $\mu$ A pull-up.

The  $\overline{\text{PWRGD}}$  pin pulls low when the FB power good comparator is high and the HGATE drive exceeds 4.2V. The  $\overline{\text{PWRGD}}$  pin goes high when the HGATE is turned off by the ON or  $\overline{\text{EN}}$  pins, or when the FB power good comparator drives low, or when  $\text{INTV}_{\text{CC}}$  enters undervoltage lockout.

### Current Sense Monitor

The current through the external sense resistor is monitored by LTC4236's current sense amplifier at the  $\text{CS}^+$  and  $\text{SENSE}^-$  pins (see Figure 5). The amplifier uses auto-zeroing circuitry to achieve an offset below 150 $\mu$ V over temperature, sense voltage and input supply voltage. The frequency of the auto-zero clock is 10kHz. An internal resistor  $R_{\text{IN}}$  is connected between the amplifier's negative input terminal and  $\text{CS}^+$  pin. The sense amplifier loop forces the negative input terminal to have the same potential as  $\text{SENSE}^-$  and that develops a potential across  $R_{\text{IN}}$  to be the same as the sense voltage  $V_{\text{SENSE}}$ . A corresponding current,  $V_{\text{SENSE}}/R_{\text{IN}}$ , will flow through  $R_{\text{IN}}$ . The high impedance inputs of the sense amplifier will not conduct this input current, allowing it to flow through an internal MOSFET to a resistor  $R_{\text{OUT}}$  connected between the IMON and GND pins. The IMON output voltage is equal to  $(R_{\text{OUT}}/R_{\text{IN}}) \cdot V_{\text{SENSE}}$ . The resistor ratio  $R_{\text{OUT}}/R_{\text{IN}}$  defines the voltage gain of the sense amplifier and is set to 100 with  $R_{\text{IN}} = 200\Omega$  and  $R_{\text{OUT}} = 20\text{k}$ . Full scale input sense voltage to the sense amplifier is 25mV, corresponding to an output of 2.5V. For input supply voltages greater than

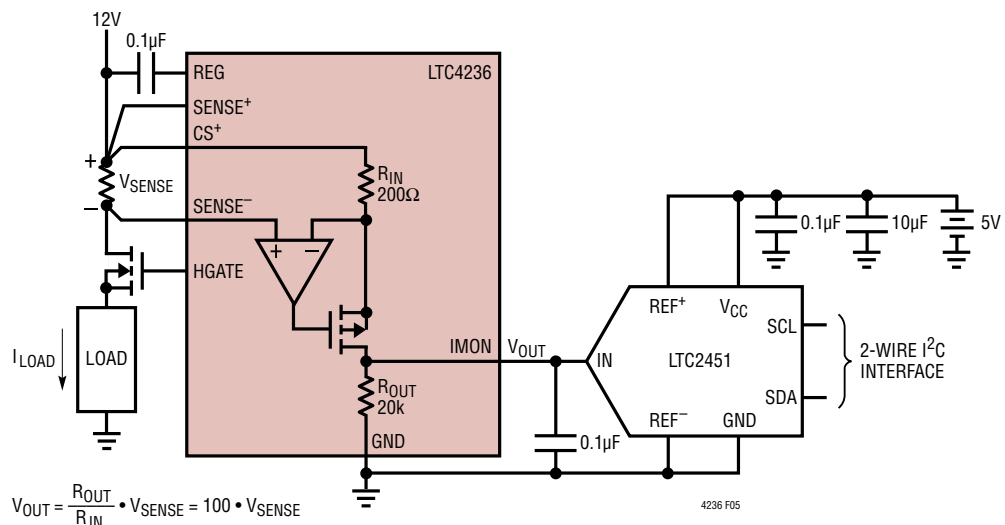


Figure 5. High Side Current Monitor with LTC2451 ADC



## APPLICATIONS INFORMATION

5V, the output clamps at 3.5V if the allowable input sense voltage range is exceeded.

### IMON Output Filtering

A capacitor connected in parallel with  $R_{OUT}$  will give a low pass response. This will reduce unwanted noise at the output, and may also be useful as a charge reservoir to keep the output steady while driving a switching circuit such as an ADC (see Figure 5). This output capacitor  $C_{OUT}$  in parallel with  $R_{OUT}$  will create a pole in the output response at:

$$f_c = \frac{1}{2 \cdot \pi \cdot R_{OUT} \cdot C_{OUT}}$$

### REG Pin Bypassing

The LTC4236 has an internally regulated supply near  $SENSE^+$  for internal bias of the current sense amplifier. It is not intended for use as a supply or bias pin for external circuitry. A 0.1 $\mu$ F capacitor should be connected between the REG and  $SENSE^+$  pins. This capacitor should be located very near to the device and close to the REG pin for the best performance.

### REG and IMON Start-Up

The start-up current of the current sense amplifier when the LTC4236 is powered on consists of two parts: the first is the current necessary to charge the REG bypass capacitor, which is nominally 0.1 $\mu$ F. Since the REG voltage charges to approximately 4.1V below the  $SENSE^+$  voltage, this can require a significant amount of start-up current. The second source is the output current that flows into  $R_{OUT}$ , which upon start-up may temporarily drive the IMON output high for less than 2ms. This is a temporary condition which will cease when the sense amplifier settles into normal closed-loop operation.

### CPO and DGATE Start-Up

The CPO pin voltage is initially pulled up to a diode below the IN1 or D2SRC pin when first powered up (see Figure 1). However, for application with back-to-back MOSFETs in IN2 power path, CPO2 starts off at 0V since D2SRC is

near ground (see Figure 8). CPO starts ramping up 7 $\mu$ s after  $INTV_{CC}$  clears its undervoltage lockout level. Another 40 $\mu$ s later, DGATE also starts ramping up with CPO. The CPO ramp rate is determined by the CPO pull-up current into the combined CPO and DGATE pin capacitances. An internal clamp limits the CPO pin voltage to 12V above the IN1 or D2SRC pin, while the final DGATE pin voltage is determined by the gate drive amplifier. An internal 12V clamp limits the DGATE1 and DGATE2 pin voltages above IN1 and D2SRC respectively.

### CPO Capacitor Selection

The recommended value of the capacitor between the CPO1 and IN1, and CPO2 and D2SRC pins is approximately 10 $\times$  the input capacitance  $C_{ISS}$  of the ideal diode MOSFET. A larger capacitor takes a correspondingly longer time to charge up by the internal charge pump. A smaller capacitor suffers more voltage drop during a fast gate turn-on event as it shares charge with the MOSFET gate capacitance.

### MOSFET Selection

The LTC4236 drives N-channel MOSFETs to conduct the load current. The important features of the MOSFETs are on-resistance  $R_{DS(ON)}$ , the maximum drain-source voltage  $BV_{DSS}$  and the threshold voltage.

The gate drive for the ideal diode and Hot Swap MOSFET is guaranteed to be greater than 5V when the supply voltages at IN1 and IN2 are between 2.9V and 7V. When the supply voltages at IN1 and IN2 are greater than 7V, the gate drive is guaranteed to be greater than 10V. The gate drive is limited to 14V. An external Zener diode can be used to clamp the potential from the MOSFET's gate to source if the rated breakdown voltage is less than 14V.

The maximum allowable drain-source voltage  $BV_{DSS}$  must be higher than the supply voltage including supply transients as the full supply voltage can appear across the MOSFET. If an input or output is connected to ground, the full supply voltage will appear across the MOSFET. The  $R_{DS(ON)}$  should be small enough to conduct the maximum load current, and also stay within the MOSFET's power rating.

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### Supply Transient Protection

When the capacitances at the input and output are very small, rapid changes in current during input or output short-circuit events can cause transients that exceed the 24V absolute maximum ratings of the IN and OUT pins. To minimize such spikes, use wider traces or heavier trace plating to reduce the power trace inductance. Also, bypass locally with a 10 $\mu$ F electrolytic and 0.1 $\mu$ F ceramic, or alternatively clamp the input with a transient voltage suppressor (Z1, Z2). A 100 $\Omega$ , 0.1 $\mu$ F snubber damps the response and eliminates ringing (See Figure 9).

### Design Example

As a design example for selecting components, consider a 12V system with a 7A maximum load current for the two supplies (see Figure 1).

First, select the appropriate value of the current sense resistor  $R_S$  for the 12V supply. Calculate the sense resistor value based on the maximum load current  $I_{LOAD(MAX)}$  and the lower limit for the current limit sense voltage threshold  $\Delta V_{SENSE(TH)(MIN)}$ .

$$R_S = \frac{\Delta V_{SENSE(TH)(MIN)}}{I_{LOAD(MAX)}} = \frac{22.5mV}{7A} = 3.2m\Omega$$

Choose a 3m $\Omega$  sense resistor with a 1% tolerance.

Next, calculate the  $R_{DS(ON)}$  of the ideal diode MOSFET to achieve the desired forward drop at maximum load. Assuming a forward drop,  $\Delta V_{FWD}$  of 30mV across the MOSFET:

$$R_{DS(ON)} \leq \frac{\Delta V_{FWD}}{I_{LOAD(MAX)}} = \frac{30mV}{7A} = 4.2m\Omega$$

The SiR158DP offers a good choice with a maximum  $R_{DS(ON)}$  of 1.8m $\Omega$  at  $V_{GS} = 10V$ . The input capacitance  $C_{ISS}$  of the SiR158DP is about 4980pF. Slightly exceeding the 10 $\times$  recommendation, a 0.1 $\mu$ F capacitor is selected for C2 and C3 at the CPO pins.

Next, verify that the thermal ratings of the selected Hot Swap MOSFET are not exceeded during power-up or an overcurrent fault.

Assuming the MOSFET dissipates power due to inrush current charging the load capacitor  $C_L$  at power-up, the energy dissipated in the MOSFET is the same as the energy stored in the load capacitor, and is given by:

$$E_{CL} = \frac{1}{2} \cdot C_L \cdot V_{IN}^2$$

For  $C_L = 680\mu F$ , the time it takes to charge up  $C_L$  is calculated as:

$$t_{CHARGE} = \frac{C_L \cdot V_{IN}}{I_{INRUSH}} = \frac{680\mu F \cdot 12V}{1A} = 8ms$$

The inrush current is set to 1A by adding capacitance  $C_{HG}$  at the gate of the Hot Swap MOSFET.

$$C_{HG} = \frac{C_L \cdot I_{HGATE(UP)}}{I_{INRUSH}} = \frac{680\mu F \cdot 10\mu A}{1A} = 6.8nF$$

Choose a practical value of 10nF for  $C_{HG}$ .

The average power dissipated in the MOSFET is calculated as:

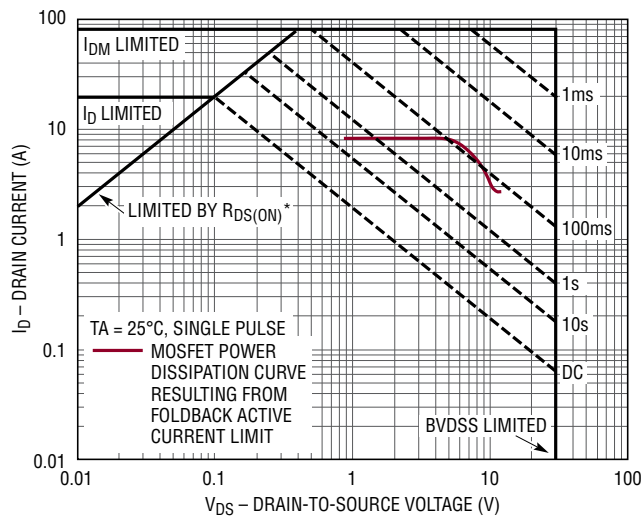
$$P_{AVG} = \frac{E_{CL}}{t_{CHARGE}} = \frac{1}{2} \cdot \frac{680\mu F \cdot (12V)^2}{8ms} = 6W$$

The MOSFET selected must be able to tolerate 6W for 8ms during power-up. The SOA curves of the SiR158DP provide 45W (1.5A at 30V) for 100ms. This is sufficient to satisfy the requirement. The increase in junction temperature due to the power dissipated in the MOSFET is  $\Delta T = P_{AVG} \cdot Z_{thJC}$  where  $Z_{thJC}$  is the junction-to-case thermal impedance. Under this condition, the SiR158DP data sheet indicates that the junction temperature will increase by 3 $^{\circ}C$  using  $Z_{thJC} = 0.5^{\circ}C/W$  (single pulse).

Next, the power dissipated in the MOSFET during an overcurrent fault must be safely limited. The fault timer capacitor ( $C_{FT}$ ) is used to prevent power dissipation in the MOSFET from exceeding the SOA rating during active current limit. A good way to determine a suitable value for  $C_{FT}$  is to superimpose the foldback current limit profile shown in the Typical Performance Characteristics on the MOSFET data sheet's SOA curves.

## APPLICATIONS INFORMATION

For the SiR158DP MOSFET, this exercise yields the plot in Figure 6.



\*  $V_{GS} >$  MINIMUM  $V_{GS}$  AT WHICH  $R_{DS(ON)}$  IS SPECIFIED

**Figure 6. SiR158DP SOA with Design Example MOSFET Power Dissipation Superimposed**

As can be seen, the LTC4236's foldback current limit profile roughly coincides with the 100ms SOA contour. Since this SOA plot is for an ambient temperature of 25°C only, a maximum fault timer period of much less than 100ms should be considered, such as 10ms or less. Selecting a 0.1μF ±10% value for  $C_{FT}$  yields a maximum fault timer period of 1.75ms which should be small enough to protect the MOSFET during any overcurrent fault scenario.

Next, select the values for the resistive divider at the ON pin that defines the undervoltage threshold of 9.7V for the 12V supply at SENSE<sup>+</sup>. Since the leakage current for the ON pin can be as high as ±1μA, the total resistance in the divider should be low enough to minimize the resulting offset error. Calculate the bottom resistor R1 based on the following equation to obtain less than ±0.2% error due to leakage current.

$$R1 = \left( \frac{V_{ON(TH)}}{I_{IN(LEAK)}} \right) \cdot 0.2\% = \left( \frac{1.235V}{1\mu A} \right) \cdot 0.2\% = 2.4k$$

Choose R1 to be 2k to achieve less than ±0.2% error and calculating R2 yields:

$$R2 = \left( \frac{V_{IN(UV)}}{V_{ON(TH)}} - 1 \right) \cdot R1$$

$$R2 = \left( \frac{9.7V}{1.235V} - 1 \right) \cdot 2k = 13.7k$$

It remains to select the values for the FB pin resistive divider in order to set a power good threshold of 10.5V. Keeping in mind the FB pin's ±1μA leakage current, choose a value of 2k for the bottom resistor R3. Calculating the top resistor R4 value yields:

$$R4 = \left( \frac{V_{OUT(PG)}}{V_{FB(TH)}} - 1 \right) \cdot R3$$

$$R4 = \left( \frac{10.5V}{1.235V} - 1 \right) \cdot 2k = 15k$$

The subsequent offset error due to the FB pin leakage current will be less than ±0.2%.

The final components to consider are a 0.1μF bypass (C1) at the INTV<sub>CC</sub> pin and a 0.1μF capacitor (C4) connected between the REG and SENSE<sup>+</sup> pins.

### PCB Layout Considerations

To achieve accurate current sensing, a Kelvin connection for the sense resistor is recommended. The PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistor and the power MOSFET should include good thermal management techniques for optimal device power dissipation. A recommended PCB layout is illustrated in Figure 7.

Connect the IN and OUT pin traces as close as possible to the MOSFETs' terminals. Keep the traces to the MOSFETs wide and short to minimize resistive losses. The PCB traces associated with the power path through the MOSFETs should have low resistance. The suggested trace width for 1oz copper foil is 0.03" for each ampere of DC current to keep PCB trace resistance, voltage drop and temperature rise to a minimum. Note that the sheet resistance of 1oz copper foil is approximately 0.5mΩ/square, and voltage drops due to trace resistance add up quickly in high current applications.

## APPLICATIONS INFORMATION

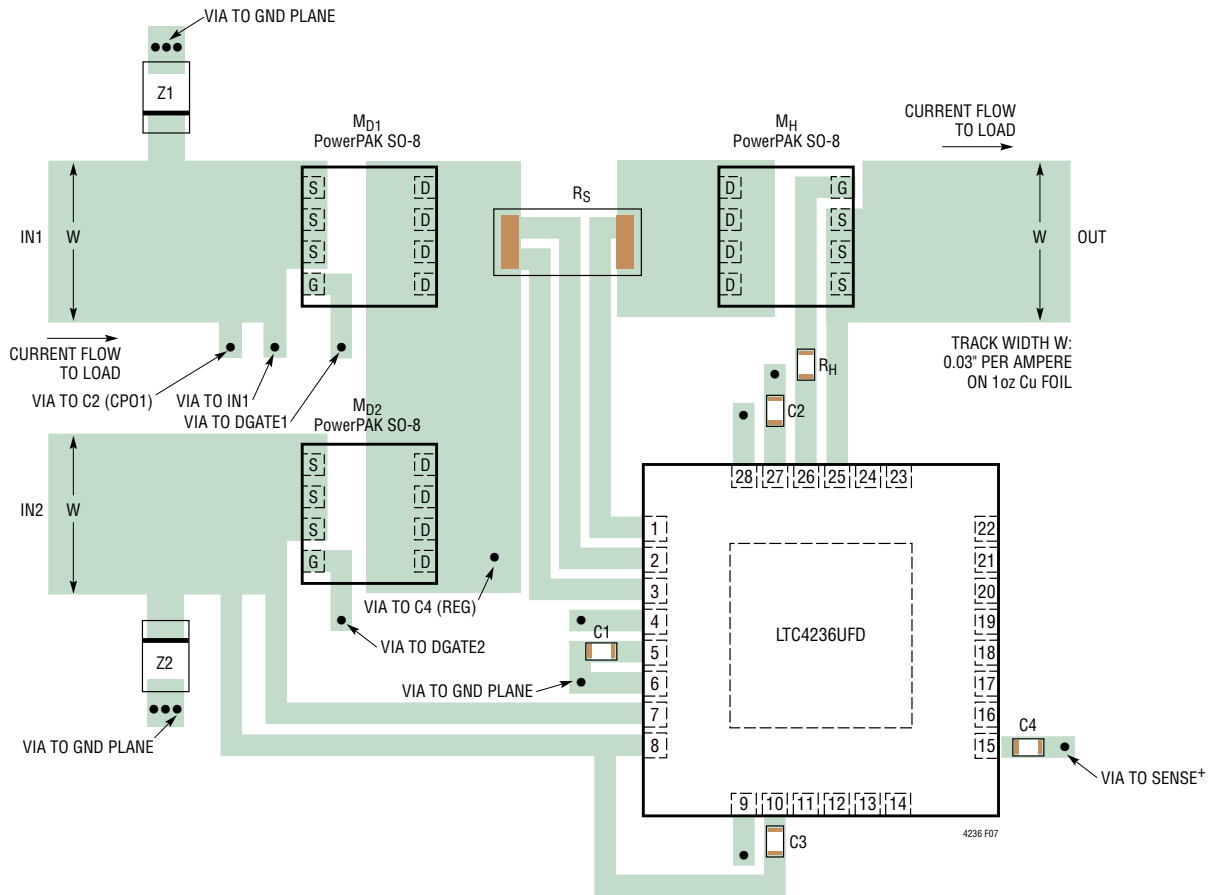


Figure 7. Recommended PCB Layout for Power MOSFETs and Sense Resistor

It is also important to place the bypass capacitor C1 for the  $INTV_{CC}$  pin, as close as possible between  $INTV_{CC}$  and GND. Also place C2 near the CPO1 and IN1 pins, C3 near the CPO2 and D2SRC pins, and C4 near the REG and SENSE<sup>+</sup> pins. The transient voltage suppressors Z1 and Z2, when used, should be mounted close to the LTC4236 using short lead lengths.

### Power Prioritizer

Figure 8 shows an application where the IN1 supply is passed to the output on the basis of priority, rather than simply allowing the highest voltage to prevail. This is achieved by connecting a resistive divider from IN1 at the D2OFF pin to suppress the turn-on of the back-to-back ideal diode MOSFETs,  $M_{D2}$  and  $M_{D3}$  in the IN2 power path. In this application, the 5V primary supply ( $V_{IN1}$ ) is passed to the output whenever it is available; power is drawn

from the 12V backup supply ( $V_{IN2}$ ) only when the primary supply is unavailable. As long as  $V_{IN1}$  is above the 4.7V threshold set by the R6-R7 divider at the D2OFF pin,  $M_{D2}$  and  $M_{D3}$  are turned off, allowing  $V_{IN1}$  to be connected to the output through  $M_{D1}$ . The common source terminals of  $M_{D2}$  and  $M_{D3}$  are connected to D2SRC pin, which allows the body-diode of  $M_{D2}$  to reverse block the current flow from the higher backup supply ( $V_{IN2}$ ) to the output. If the primary supply fails and  $V_{IN1}$  drops below 4.3V, D2OFF is allowed to turn on  $M_{D2}$  and  $M_{D3}$ , and connect the  $V_{IN2}$  to the output. When  $V_{IN1}$  returns to a viable voltage,  $M_{D2}$  and  $M_{D3}$  turn off, and the output is connected to  $V_{IN1}$ . Adding R5 in the R6-R7 divider and bypassing it with DSTAT2 pin control allows the D2OFF pin hysteresis to be increased from 20mV to 100mV. The resistive divider at the ON pin sets the SENSE<sup>+</sup> undervoltage threshold to 4.1V.

# APPLICATIONS INFORMATION

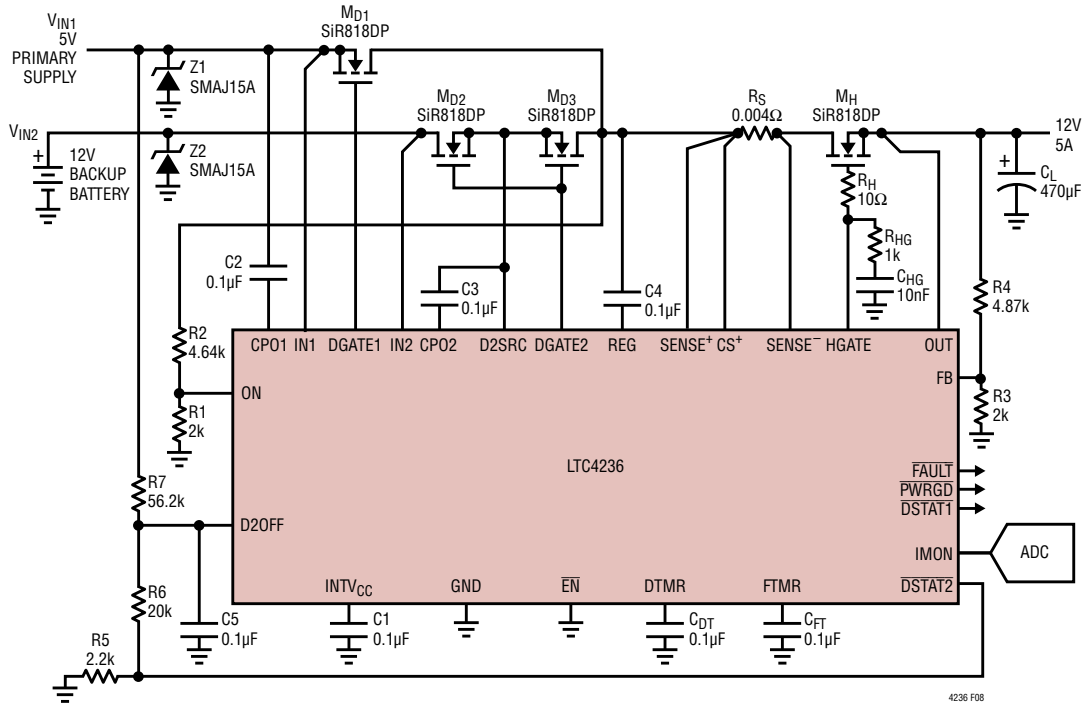


Figure 8. 2-Channel Power Prioritizer

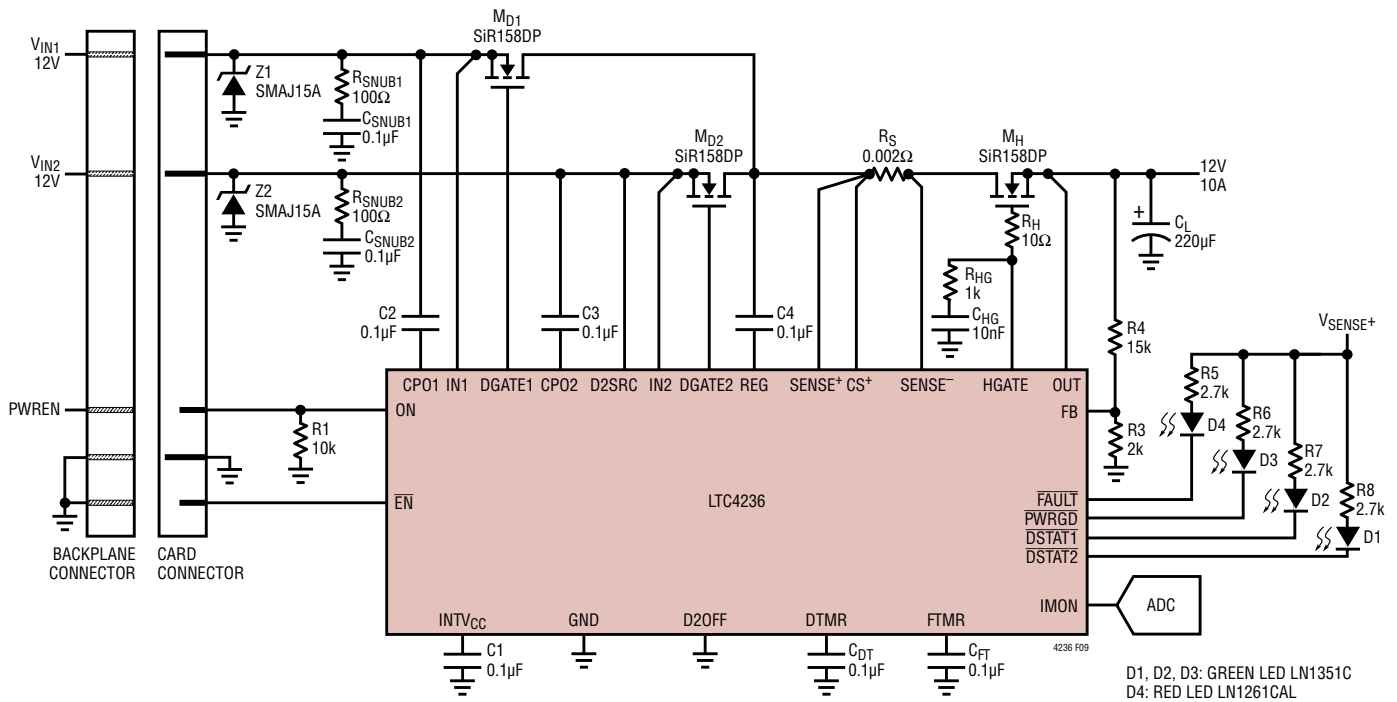
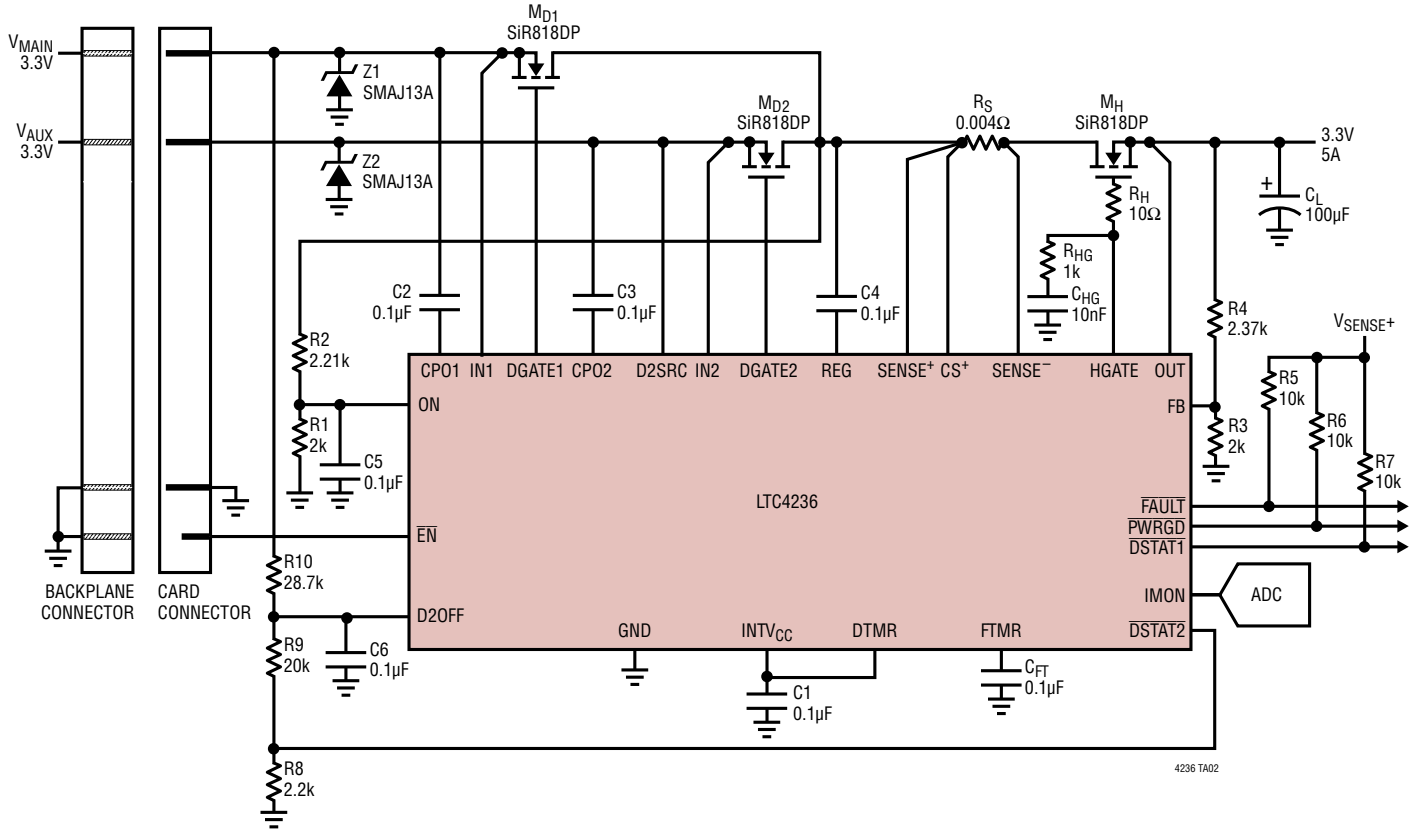


Figure 9. 12V, 10A Card Resident Application

## TYPICAL APPLICATION

### Plug-In Card 3.3V Prioritized Power Supply at IN1

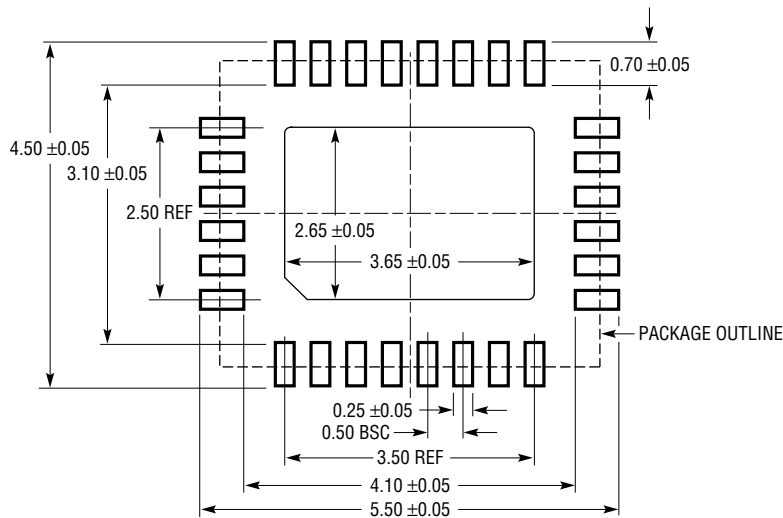


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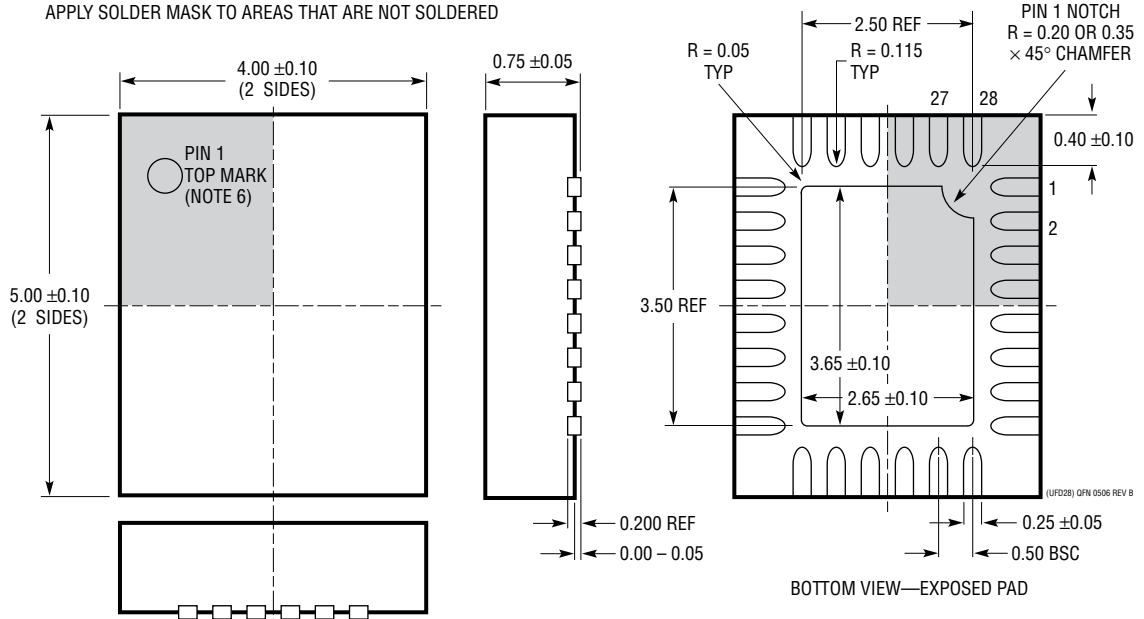
# PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC4236#packaging> for the most recent package drawings.

**UFD Package**  
**28-Lead Plastic QFN (4mm × 5mm)**  
 (Reference LTC DWG # 05-08-1712 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS  
 APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



- NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
  2. DRAWING NOT TO SCALE
  3. ALL DIMENSIONS ARE IN MILLIMETERS
  4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
  5. EXPOSED PAD SHALL BE SOLDER PLATED
  6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE