Active Clamp Synchronous Forward Controller

FEATURES

- **Input Voltage Range: 8.5V to 100V**
- **Programmable Volt-Second Clamp**
- **High Efficiency Control: Active Clamp, Synchronous Rectification, Programmable Delays**
- Short-Circuit (Hiccup Mode) Overcurrent Protection
- Programmable Soft-Start/Stop
- Programmable OVLO and UVLO with Hysteresis
- Programmable Frequency (100kHz to 500kHz)
- Synchronizable to an External Clock

APPLICATIONS

- Industrial, Automotive and Military Systems
- 48V Telecommunication Isolated Power Supplies

DESCRIPTION

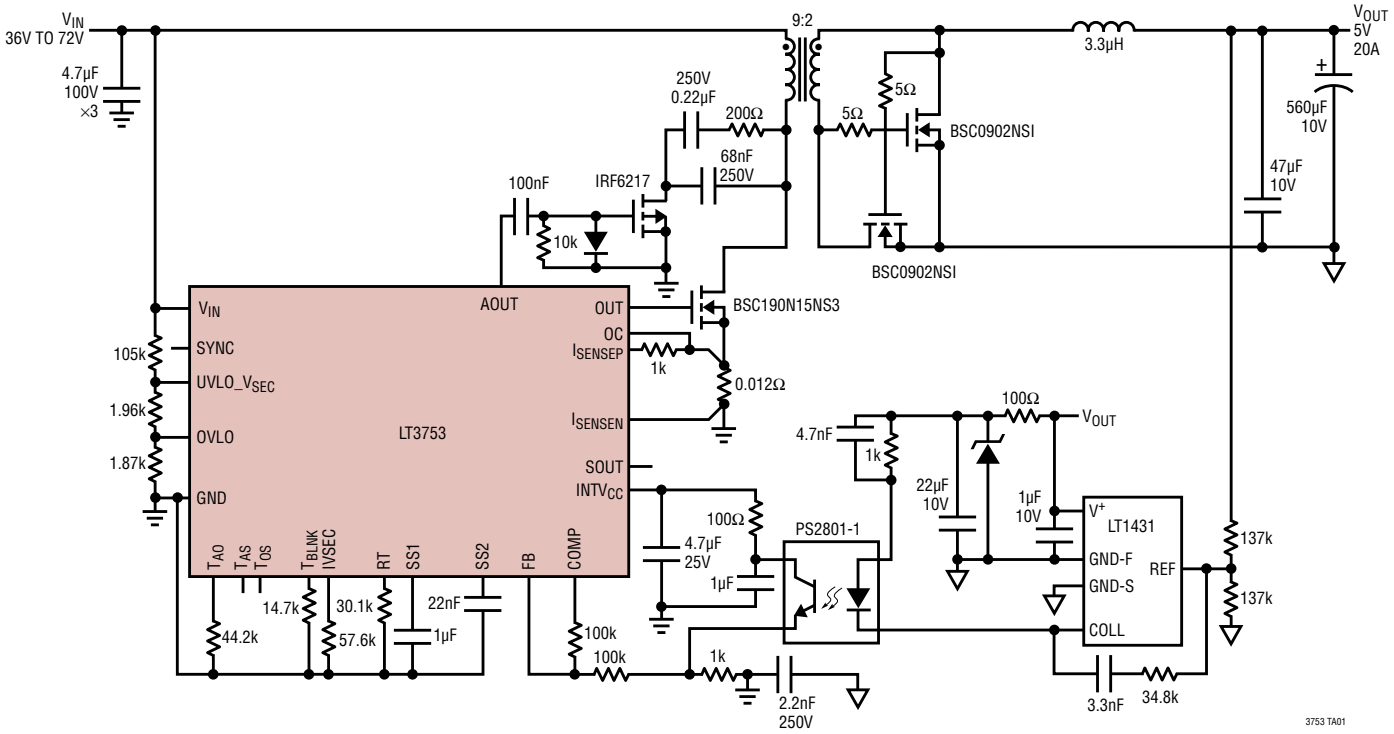
The LT®3753 is a current mode PWM controller optimized for an active clamp forward converter topology, allowing up to 100V input operation.

A programmable volt-second clamp allows primary switch duty cycles above 50% for high switch, transformer and rectifier utilization. Active clamp control reduces switch voltage stress and increases efficiency. A synchronous output is available for controlling secondary side synchronous rectification.

The LT3753 is available in a 38-lead plastic TSSOP package with missing pins for high voltage spacings.

TYPICAL APPLICATION

36V to 72V, 5V/20A Active Clamp Isolated Forward Converter



Rev. C

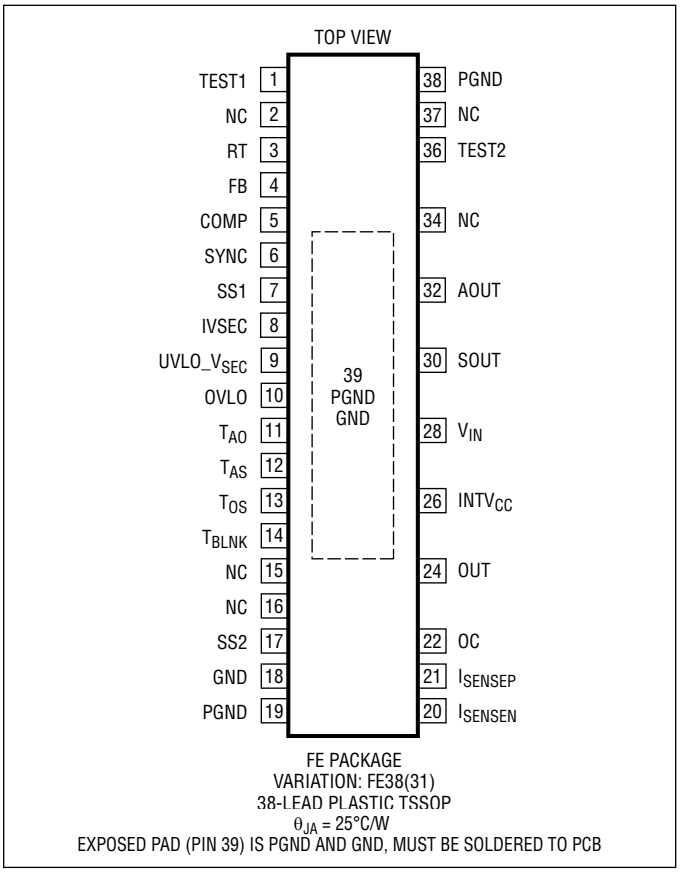
TABLE OF CONTENTS

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} 100V
UVLO_V_{SEC}, OVLO 20V
$INTV_{CC}$, SS2.....16V
FB, SYNC 6V
SS1, COMP, TEST1, RT 3V
I_{SENSEP}, I_{SENSEN}, OC, TEST2 .....0.35V
IVSEC.....–250µA
Operating Junction Temperature Range (Notes 2, 3)
LT3753EFE.....–40°C to 125°C
LT3753IFE.....–40°C to 125°C
LT3753HFE .....–40°C to 150°C
LT3753MPFE .....–55°C to 150°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering, 10 Sec) .....300°C

PIN CONFIGURATION



FE PACKAGE
VARIATION: FE38(31)
38-LEAD PLASTIC TSSOP
θ_{JA} = 25°C/W
EXPOSED PAD (PIN 39) IS PGND AND GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3753EFE#PBF	LT3753EFE#TRPBF	LT3753FE	38-Lead Plastic TSSOP	–40°C to 125°C
LT3753IFE#PBF	LT3753IFE#TRPBF	LT3753FE	38-Lead Plastic TSSOP	–40°C to 125°C
LT3753HFE#PBF	LT3753HFE#TRPBF	LT3753FE	38-Lead Plastic TSSOP	–40°C to 150°C
LT3753MPFE#PBF	LT3753MPFE#TRPBF	LT3753FE	38-Lead Plastic TSSOP	–55°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, UVLO_V_{SEC} = 2.5V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operational Input Voltage		●	8.5		100	V
$V_{IN(ON)}$		●		7.75	8.4	V
$V_{IN(OFF)}$				7.42		V
$V_{IN(ON/OFF)}$ Hysteresis		●	0.11	0.33	0.55	V
V_{IN} Quiescent Current	FB = 1.5V (Not Switching)			5.9	7.5	mA
UVLO_V_{SEC} Micropower Threshold (V_{SD})	I_{VIN} < 20µA	●	0.2	0.4	0.6	V
V_{IN} Shutdown Current (Micropower)	UVLO_V_{SEC} = 0.2V			20	40	µA
UVLO_V_{SEC} Threshold (V_{SYS_UV})		●	1.180	1.250	1.320	V
V_{IN} Shutdown Current (After Soft-Stop)	UVLO_V_{SEC} = 1V			165	220	µA
UVLO_V_{SEC} (ON) Current	UVLO_V_{SEC} = V_{SYS_UV} + 50mV			0		µA
UVLO_V_{SEC} (OFF) Current Hysteresis Current With One-Shot Communication Current	UVLO_V_{SEC} = V_{SYS_UV} – 50mV (Note 13)	●	4.0	5 25	6.0	µA µA
OVLO (Rising) (No Switching, Reset SS1)		●	1.220	1.250	1.280	V
OVLO (Falling) (Restart SS1)				1.215		V
OVLO Hysteresis		●	23	35	47	mV
OVLO Pin Current (Note 8)	OVLO = 0V OVLO = 1.5V (SS1 = 2.7V) OVLO = 1.5V (SS1 = 1.0V)			5 0.9 5	100 100	nA mA nA
Oscillator						
Frequency: f_{OSC} = 100kHz	R_T = 82.5k		94	100	106	kHz
Frequency: f_{OSC} = 300kHz	R_T = 24.9k	●	279	300	321	kHz
Frequency: f_{OSC} = 500kHz	R_T = 14k		470	500	530	kHz
f_{OSC} Line Regulation	R_T = 24.9k, 8.5V < V_{IN} < 100V			0.05	0.1	%/V
Frequency and D_{VSEC} Foldback Ratio (Fold)	SS1 = V_{SSACT} + 25mV, SS2 = 2.7V			4		
SYNC Input High Threshold	(Note 4)	●		1.2	1.8	V
SYNC Input Low Threshold	(Note 4)	●	0.6	1.025		V
SYNC Pin Current	SYNC = 6V			75		µA
SYNC Frequency/Programmed f_{OSC}			1.0		1.25	kHz/kHz
Linear Regulator ($INTV_{CC}$)						
$INTV_{CC}$ Regulation Voltage			9.4	10	10.4	V
Dropout (V_{IN}-$INTV_{CC}$)	V_{IN} = 8.75V, I_{INTVCC} = 10mA			0.6		V
$INTV_{CC}$ UVLO(+)	(Start Switching)			7	7.4	V
$INTV_{CC}$ UVLO(–)	(Stop Switching)			6.8	7.2	V
$INTV_{CC}$ UVLO Hysteresis			0.1	0.2	0.3	V
$INTV_{CC}$ OVLO(+)	(Stop Switching)		15.9	16.5	17.2	V
$INTV_{CC}$ OVLO(–)	(Start Switching)		15.4	16	16.7	V
$INTV_{CC}$ OVLO Hysteresis			0.38	0.5	0.67	V
$INTV_{CC}$ Current Limit	$INTV_{CC}$ = 0V $INTV_{CC}$ = 8.75V	●	9.5 19	13 27	17 32	mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, UVLO_V_{SEC} = 2.5V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Error Amplifier						
FB Reference Voltage		●	1.220	1.250	1.275	V
FB Line Reg	8.5V < V_{IN} < 100V			0.1	0.3	mV/V
FB Load Reg	COMP_SW – 0.1V < COMP < COMP_V_{OH} – 0.1V			0.1	0.3	mV/V
FB Input Bias Current	(Note 8)			50	200	nA
Open-Loop Voltage Gain				85		dB
Unity-Gain Bandwidth	(Note 6)			2.5		MHz
COMP Source Current	FB = 1V, COMP = 1.75V (Note 8)		6	11		mA
COMP Sink Current	FB = 1.5V, COMP = 1.75V		6.5	11.5		mA
COMP Output High Clamp	FB = 1V			2.6		V
COMP Switching Threshold				1.25		V
Current Sense						
I_{SENSEP} Maximum Threshold	FB = 1V, OC = 0V		180	220	260	mV
COMP Current Mode Gain	$\Delta V_{COMP}/\Delta V_{ISENSEP}$			6.1		V/V
I_{SENSEP} Input Current (D = 0%)	(Note 8)			2		µA
I_{SENSEP} Input Current (D = 80%)	(Note 8)			33		µA
I_{SENSEN} Input Current	FB = 1.5V (COMP Open) (Note 8) FB = 1V (COMP Open) (Note 8)			20 90	30 135	µA µA
OC Overcurrent Threshold		●	82.5	96	107.5	mV
OC Input Current				200	500	nA
AOUT Driver (Active Clamp Switch Control)						
AOUT Rise Time	C_L = 1nF (Note 5), $INTV_{CC}$ = 12V			23		ns
AOUT Fall Time	C_L = 1nF (Note 5), $INTV_{CC}$ = 12V			19		ns
AOUT Low Level				0.1		V
AOUT High Level	$INTV_{CC}$ = 12V		11.9			V
AOUT High Level in Shutdown	UVLO_V_{SEC} = 0V, $INTV_{CC}$ = 8V, I_{AOUT} = 1mA Out of the Pin		7.8			V
AOUT Edge to OUT (Rise): (t_{AO})	C_{SOUT} = 1nF, C_{OUT} = 3.3nF, $INTV_{CC}$ = 12V R_{TAO} = 44.2k R_{TAO} = 73.2k (Note 9)		 168 253	 218 328	 268 403	 ns ns
OUT (Fall) to AOUT Edge: (t_{OA})	C_{SOUT} = 1nF, C_{OUT} = 3.3nF, $INTV_{CC}$ = 12V R_{TAO} = 44.2k R_{TAO} = 73.2k (Note 10)		 150 214	 196 295	 250 376	 ns ns
SOUT Driver (Synchronous Rectification Control)						
SOUT Rise Time	C_{OUT} = 1nF, $INTV_{CC}$ = 12V (Note 5)			21		ns
SOUT Fall Time	C_{OUT} = 1nF, $INTV_{CC}$ = 12V (Note 5)			19		ns
SOUT Low Level				0.1		V
SOUT High Level	$INTV_{CC}$ = 12V		11.9			V
SOUT High Level in Shutdown	UVLO_V_{SEC} = 0V, $INTV_{CC}$ = 8V, I_{SOUT} = 1mA Out of the Pin		7.8			V
AOUT Edge to SOUT (Fall): (t_{AS})	C_{AOUT} = C_{SOUT} = 1nF, $INTV_{CC}$ = 12V R_{TAS} = 44.2k (Note 11) R_{TAS} = 73.2k		 168 253	 218 328	 268 403	 ns ns
SOUT (Fall) to OUT (Rise): (t_{SO} = t_{AO} – t_{AS})	C_{SOUT} = 1nF, C_{OUT} = 3.3nF, $INTV_{CC}$ = 12V R_{TAO} = 73.2k, R_{TAS} = 44.2k (Notes 9, 11) R_{TAO} = 44.2k, R_{TAS} = 73.2k		 70 –70	 110 –110	 132 –132	 ns ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, UVLO_V_{SEC} = 2.5V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OUT (Fall) to SOUT (Rise): (t_{OS})	C_{SOUT} = 1nF, C_{OUT} = 3.3nF, $INTV_{CC}$ = 12V					
	R_{TOS} = 14.7k		52	68	84	ns
	R_{TOS} = 44.2k (Note 12)		102	133	164	ns
OUT Driver (Main Power Switch Control)						
OUT Rise Time	C_{OUT} = 3.3nF, $INTV_{CC}$ = 12V (Note 5)			19		ns
OUT Fall Time	C_{OUT} = 3.3nF, $INTV_{CC}$ = 12V (Note 5)			20		ns
OUT Low Level				0.1		V
OUT High Level	$INTV_{CC}$ = 12V		11.9			V
OUT Low Level in Shutdown	UVLO_V_{SEC} = 0V, $INTV_{CC}$ = 8V, I_{OUT} = 1mA Into the Pin			0.25		V
OUT (Volt-Sec) Max Duty Cycle Clamp	R_T = 22.6k, R_{IVSEC} = 51.1k, FB = 1V, SS1 = 2.7V					
D_{VSEC} (1 • System Input (Min)) × 100	UVLO_V_{SEC} = 1.25V		68.5	72.5	76.2	%
D_{VSEC} (2 • System Input (Min)) × 100	UVLO_V_{SEC} = 2.50V		34.3	36.5	38.7	%
D_{VSEC} (4 • System Input (Min)) × 100	UVLO_V_{SEC} = 5.00V		17.5	18.6	19.7	%
OUT Minimum ON Time	C_{OUT} = 3.3nF, $INTV_{CC}$ = 12V (Note 7)					
	R_{TBLNK} = 14.7k			325		ns
	R_{TBLNK} = 73.2k (Note 14)			454		ns
SS1 Pin (Soft-Start: Frequency and D_{VSEC}) (Soft-Stop: COMP Pin, Frequency and D_{VSEC})						
SS1 Reset Threshold ($V_{SS1(RTH)}$)				150		mV
SS1 Active Threshold ($V_{SS1(ACT)}$)	(Allow Switching)			1.25		V
SS1 Charge Current (Soft-Start)	SS1 = 1.5V (Note 8)		7	11.5	16	µA
SS1 Discharge Current (Soft-Stop)	SS1 = 1V, UVLO_V_{SEC} = V_{SYS_UV} – 50mV		6.4	10.5	14.6	µA
SS1 Discharge Current (Hard Stop)	SS1 = 1V					
OC > OC Threshold				0.9		mA
$INTV_{CC}$ < $INTV_{CC}$ UVLO(–)				0.9		mA
OVLO > OVLO(+)				0.9		mA
SS2 Pin (Soft-Start: Comp Pin)						
SS2 Discharge Current	SS1 < $V_{SS(ACT)}$, SS2 = 2.5V			2.8		mA
SS2 Charge Current	SS1 > $V_{SS(ACT)}$, SS2 = 1.5V		11	21	28	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3753EFE is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3753IFE is guaranteed to meet performance specifications from –40°C to 125°C junction temperature. The LT3753HFE is guaranteed to meet performance specifications from –40°C to 150°C junction temperature. The LT3753MPFE is tested and guaranteed to meet performance specifications from –55°C to 150°C junction temperature.

Note 3: For maximum operating ambient temperature, see the Thermal Calculations section in the Applications Information section.

Note 4: SYNC minimum and maximum thresholds are guaranteed by SYNC frequency range test using a clock input with guard banded SYNC levels of 0.7V low level and 1.7V high level.

Note 5: Rise and fall times are measured between 10% and 90% of gate driver supply voltage.

Note 6: Guaranteed by design.

Note 7: ON times are measured between rising and falling edges at 50% of gate driver supply voltage.

Note 8: Current flows out of pin.

Note 9: Guaranteed by correlation to R_{TAS} = 73.2k test.

Note 10: t_{OA} timing guaranteed by design based on correlation to measured t_{AO} timing.

Note 11: Guaranteed by correlation to R_{TAO} = 44.2k test.

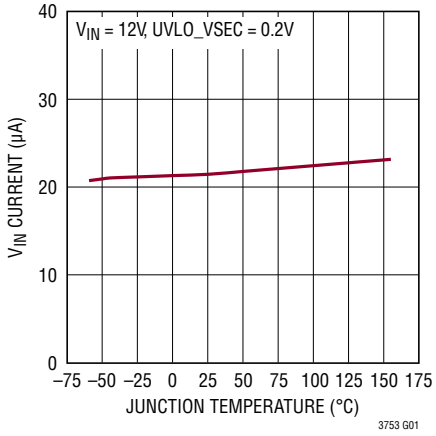
Note 12: Guaranteed by correlation to R_{TOS} = 14.7k test.

Note 13: A 2µs one-shot of 20µA from the UVLO_V_{SEC} pin allows communication between ICs to begin shutdown (useful when stacking supplies for more power (= inputs in parallel/outputs in series)). The current is tested in a static test mode. The 2µs one-shot is guaranteed by design.

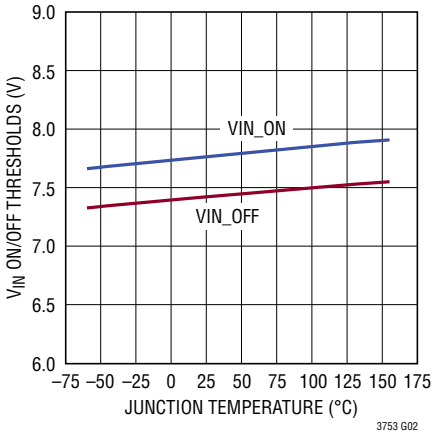
Note 14: Guaranteed by correlation to R_{TBLNK} = 14.7k test.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

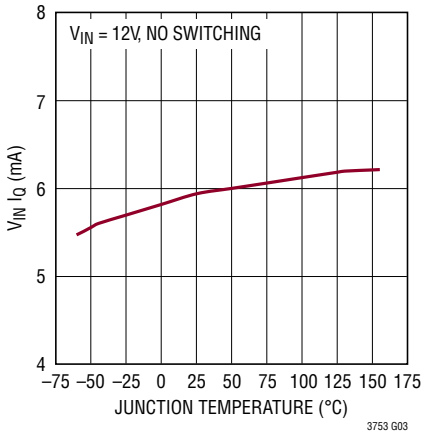
V_{IN} Shutdown Current vs Junction Temperature



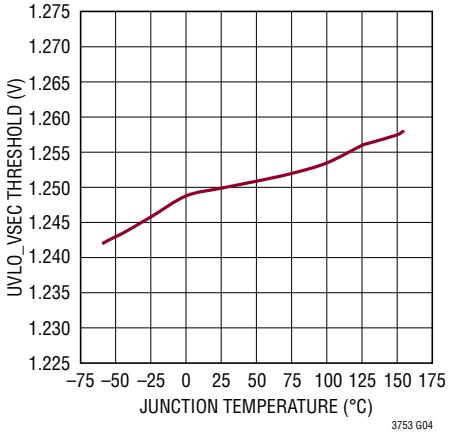
$V_{IN(ON)}$, $V_{IN(OFF)}$ Thresholds vs Junction Temperature



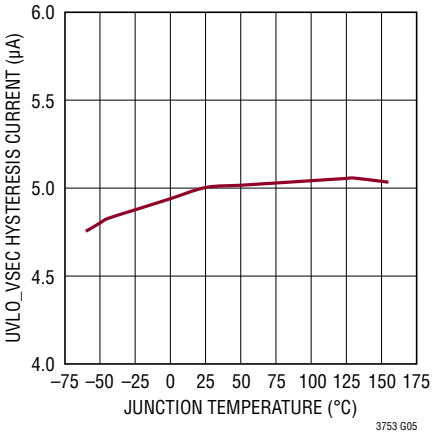
V_{IN} Quiescent Current vs Junction Temperature



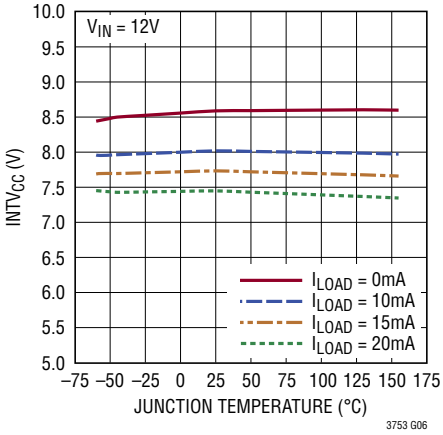
UVLO_VSEC Turn-On Threshold vs Junction Temperature



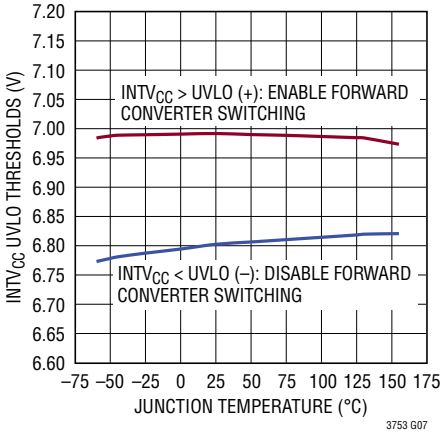
UVLO_V_{SEC} Hysteresis Current vs Junction Temperature



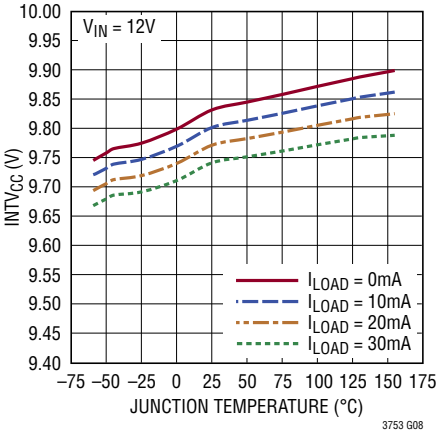
$INTV_{CC}$ in Dropout at V_{IN} = 8.75V vs Current, Junction Temperature



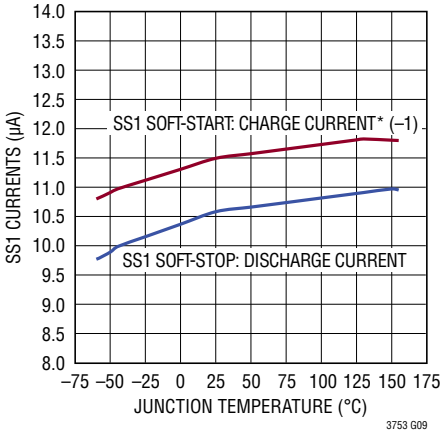
$INTV_{CC}$ UVLO Thresholds vs Junction Temperature



$INTV_{CC}$ Regulation Voltage vs Current, Junction Temperature



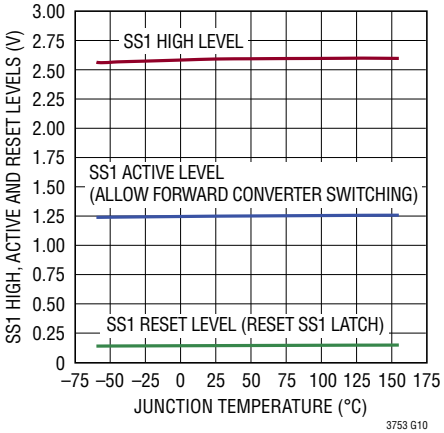
SS1 Soft-Start/Soft-Stop Pin Currents vs Junction Temperature



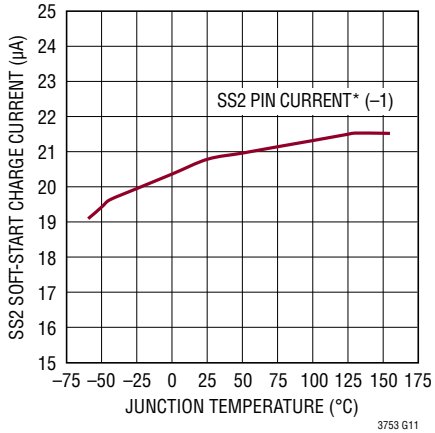
Rev. C

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

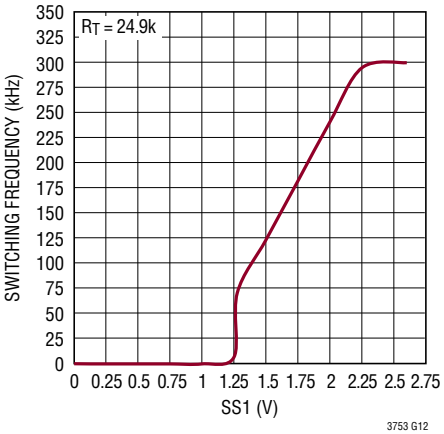
SS1 High, Active and Reset Levels vs Junction Temperature



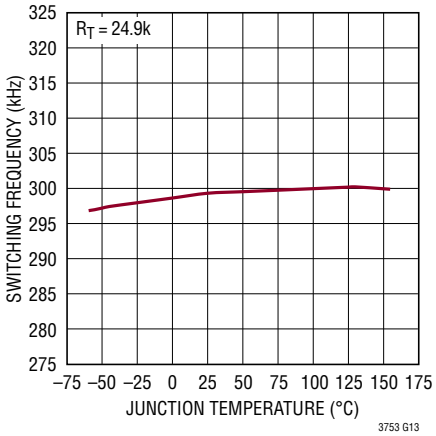
SS2 Soft-Start Charge Current vs Junction Temperature



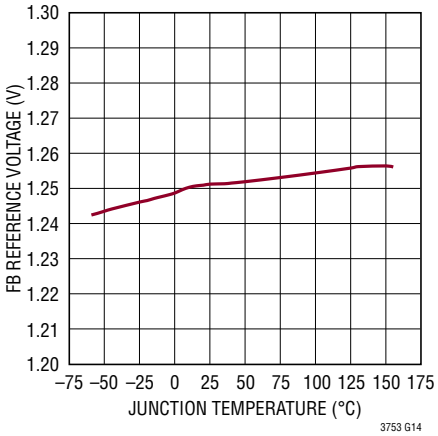
Switching Frequency vs SS1 Pin Voltage



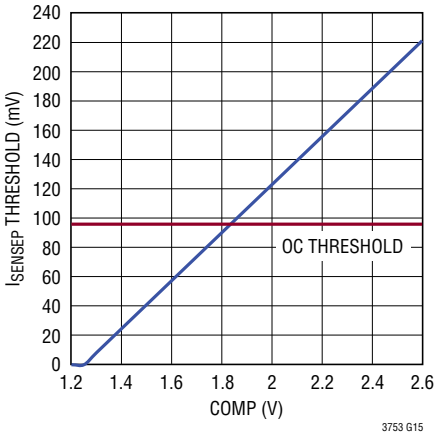
Switching Frequency vs Junction Temperature



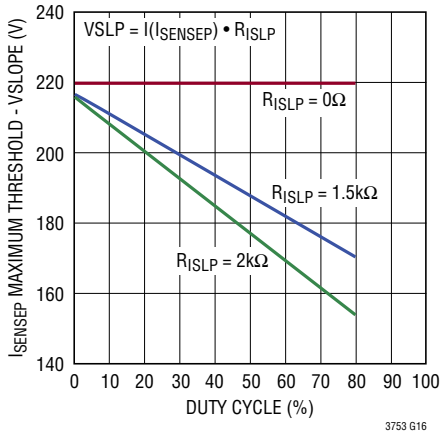
FB Reference Voltage vs Junction Temperature



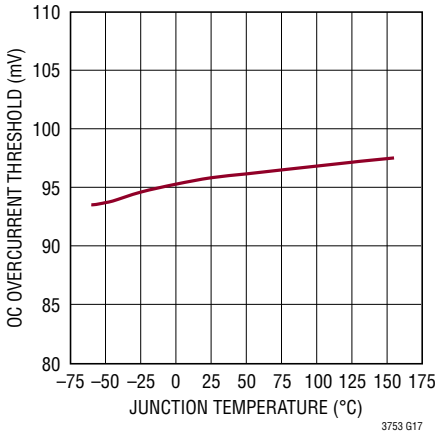
I_{SENSEP} Maximum Threshold vs COMP



I_{SENSEP} Maximum Threshold – VSLP vs Duty Cycle (Programming Slope Compensation)

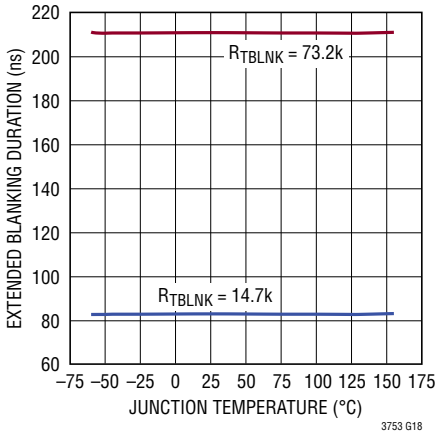


OC Overcurrent (Hiccup Mode) Threshold vs Junction Temperature

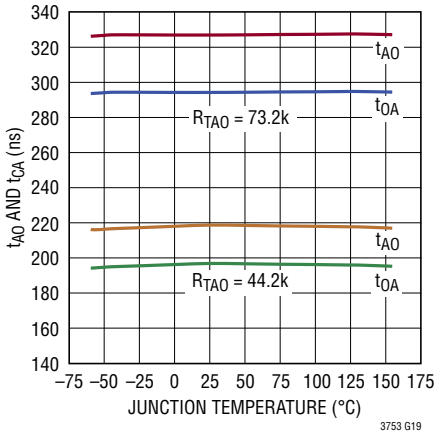


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

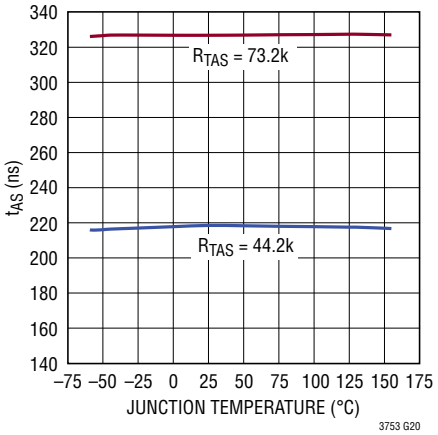
Extended Blanking Duration vs Junction Temperature



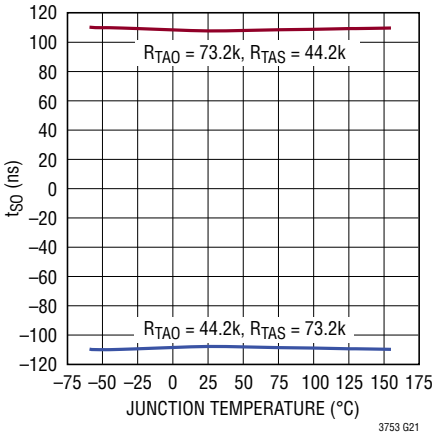
AOUT to OUT Delay (t_{AO}) and OUT to AOUT Delay (t_{OA}) vs Junction Temperature



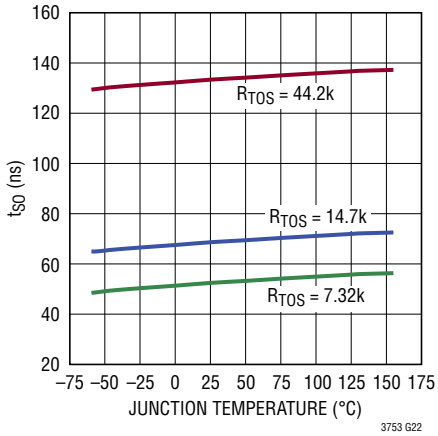
AOUT to SOUT Delay (t_{AS}) vs Junction Temperature



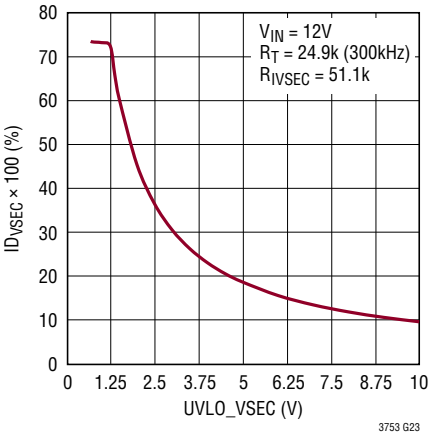
SOUT (Fall) to OUT (Rise) Delay ($t_{SO} = t_{AO} - t_{AS}$) vs Junction Temperature



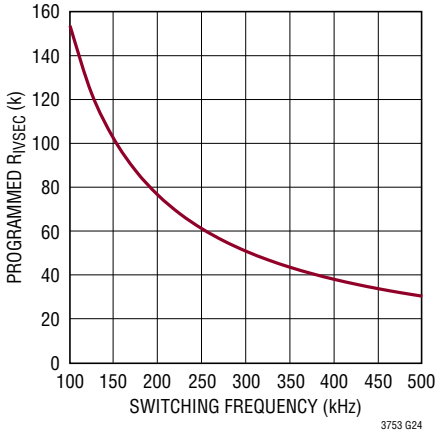
OUT (Fall) to SOUT (Rise) Delay (t_{OS}) vs Junction Temperature



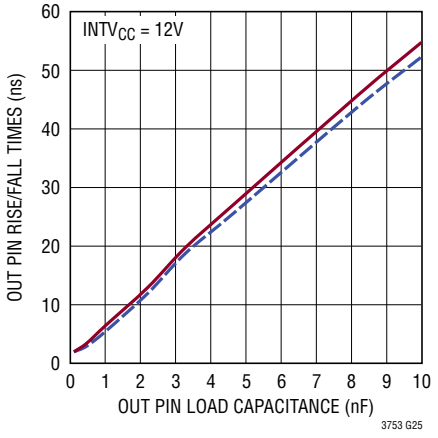
OUT Maximum Duty Cycle Clamp (D_{VSEC}) vs UVLO_V_{SEC}



Required R_{IVSEC} vs Switching Frequency (for D_{VSEC} × 100 = 72.5%, UVLO_VSEC = 1.25V)



OUT Pin Rise/Fall Times vs OUT Pin Load Capacitance



PIN FUNCTIONS

TEST1 (Pin 1): Connect to GND.

NC (Pins 2, 15, 16, 34, 37): No Connect Pins. These pins are not connected inside the IC. These pins should be left open.

RT (Pin 3): A resistor to ground programs switching frequency.

FB (Pin 4): Error Amplifier Inverting Input.

COMP (Pin 5): Error Amplifier Output. Allows various compensation networks for nonisolated applications.

SYNC (Pin 6): Allows synchronization of internal oscillator to an external clock. f_{SYNC} equal to f_{OSC} allowed.

SS1 (Pin 7): Capacitor controls soft-start/stop of switching frequency and volt-second clamp. During soft-stop it also controls the COMP pin.

IVSEC (Pin 8): Resistor Programs OUT Pin Maximum Duty Cycle Clamp (D_{VSEC}). This clamp moves inversely proportional to system input voltage to provide a volt-second clamp.

UVLO_V_{SEC} (Pin 9): A resistor divider from system input allows switch maximum duty cycle to vary inversely proportional with system input. This volt-second clamp prevents transformer saturation for duty cycles above 50%. Resistor divider ratio programs undervoltage lockout (UVLO) threshold. A 5µA pin current hysteresis allows programming of UVLO hysteresis. Pin below 0.4V reduces V_{IN} currents to microamps.

OVLO (Pin 10): A resistor divider from system input programs overvoltage lockout (OVLO) threshold. Fixed hysteresis included.

T_{AO} (Pin 11): A resistor programs nonoverlap timing between AOUT rise and OUT rise control signals.

T_{AS} (Pin 12): Resistors at T_{AO} and T_{AS} define delay between SOUT fall and OUT rise (= $t_{AO} - t_{AS}$).

T_{OS} (Pin 13): Resistor programs delay between OUT fall and SOUT rise.

T_{BLNK} (Pin 14): Resistor programs extended blanking of I_{SENSEP} and OC signals during MOSFET turn-on.

SS2 (Pin 17): Capacitor controls soft-start of COMP pin. Alternatively can connect to OPTO to communicate start of switching to secondary side. If unused, leave the pin open.

GND (Pin 18): Analog Signal Ground. Electrical connection exists inside the IC to the exposed pad (Pin 39).

PGND (Pins 19, 38, 39): The Power Grounds for the IC. The package has an exposed pad (Pin 39) underneath the IC which is the best path for heat out of the package. Pin 39 should be soldered to a continuous copper ground plane under the device to reduce die temperature and increase the power capability of the LT3753.

I_{SENSEN} (Pin 20): Negative input for the current sense comparator. Kelvin connect to the sense resistor in the source of the power MOSFET.

I_{SENSEP} (Pin 21): Positive input for the current sense comparator. Kelvin connect to the sense resistor in the source of the power MOSFET. A resistor in series with I_{SENSEP} programs slope compensation.

OC (Pin 22): An accurate 96mV threshold, independent of duty cycle, for detection of primary side MOSFET overcurrent and trigger of hiccup mode. Connect directly to sense resistor in the source of the primary side MOSFET.

Missing Pins 23, 25, 27, 29, 31, 33, 35: Pins removed for high voltage spacings and improved reliability.

OUT (Pin 24): Drives the gate of an N-channel MOSFET between 0V and $INTV_{CC}$. Active pull-off exists in shutdown.

$INTV_{CC}$ (Pin 26): A linear regulator supply generated from V_{IN}. Supplies 10V for AOUT, SOUT and OUT gate drivers. $INTV_{CC}$ must be bypassed with a 4.7µF capacitor to power ground. Can be externally driven by the housekeeping supply to remove power from within the IC.

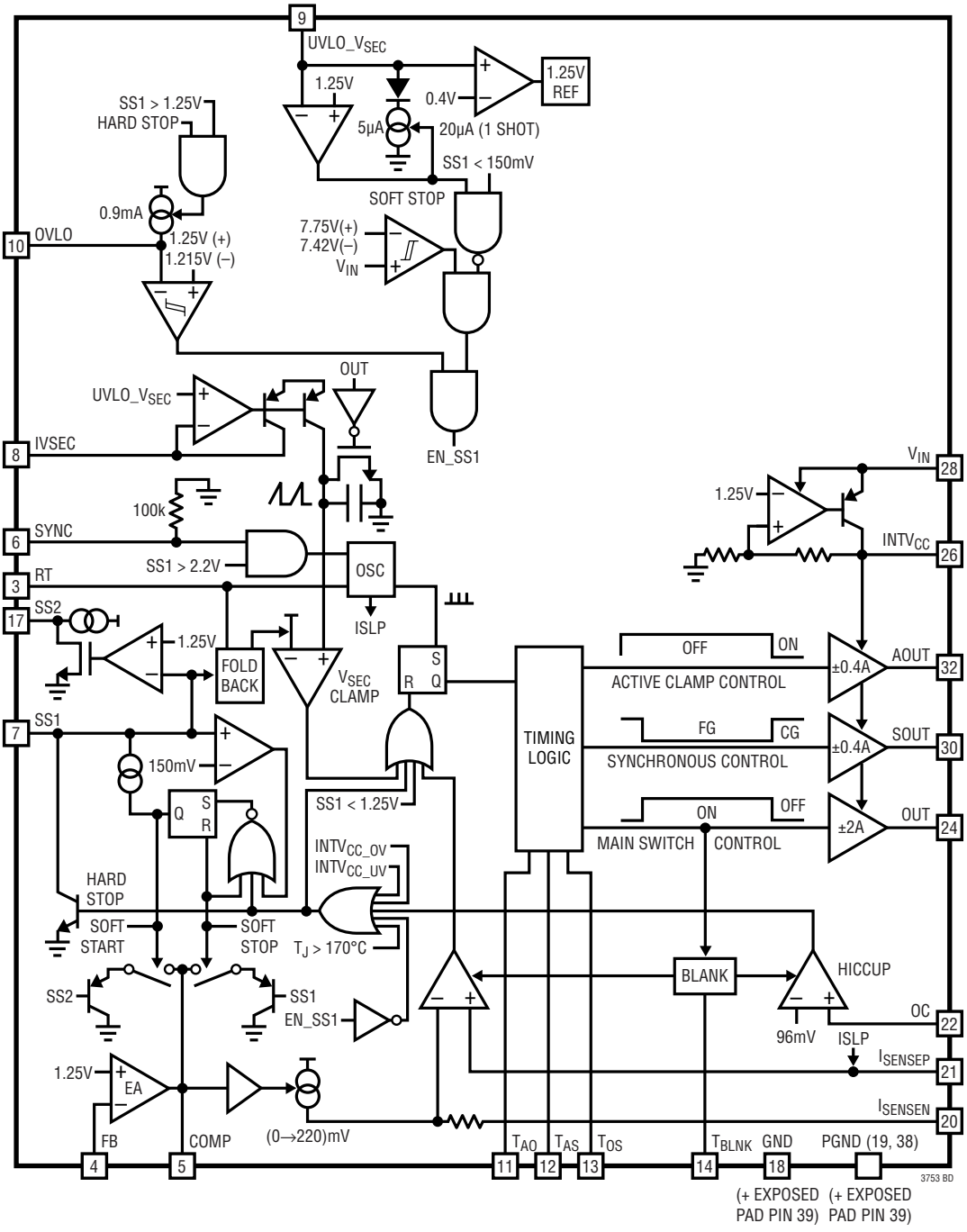
V_{IN} (Pin 28): Input Supply Pin. Bypass with 1µF to ground.

SOUT (Pin 30): Sync signal for secondary side synchronous rectifier controller.

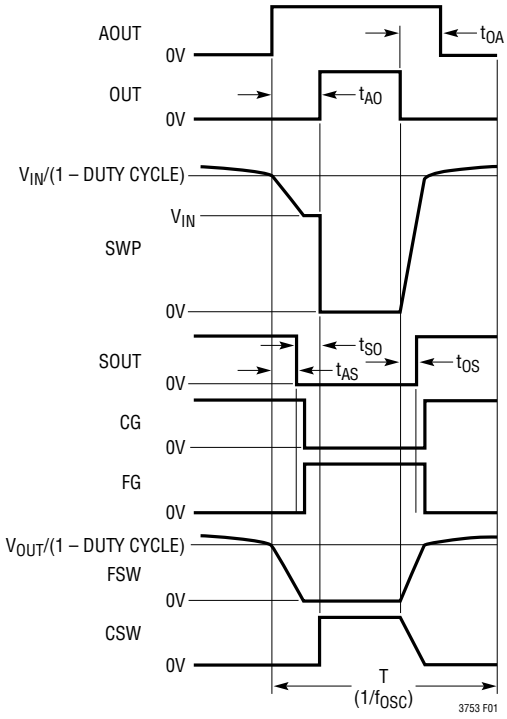
AOUT (Pin 32): Control signal for external active clamp switch.

TEST2 (Pin 36): Connect to GND.

BLOCK DIAGRAM



TIMING DIAGRAMS



t_{AO} PROGRAMMED BY R_{TAO}, t_{AS} PROGRAMMED BY R_{TAS}
t_{OS} PROGRAMMED BY R_{TOS}, $t_{OA} = 0.9 \bullet t_{AO}$, $t_{SO} = t_{AO} – t_{AS}$

Figure 1. Timing Diagram

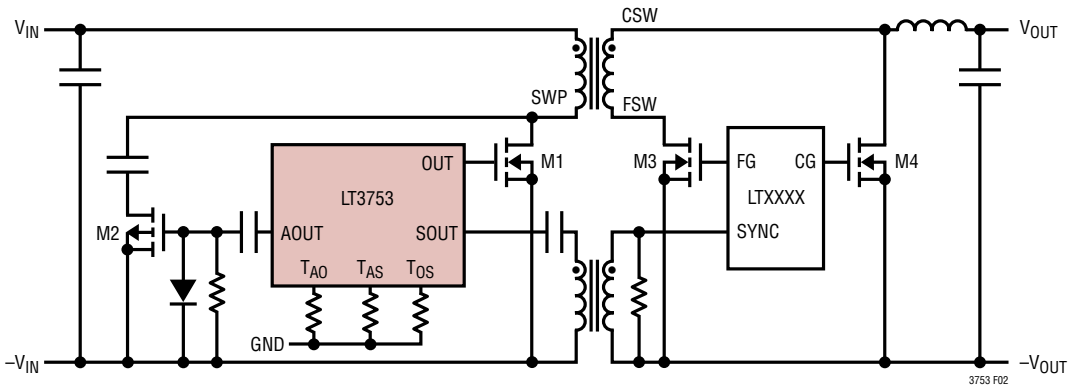


Figure 2. Timing Reference Circuit

TIMING DIAGRAMS

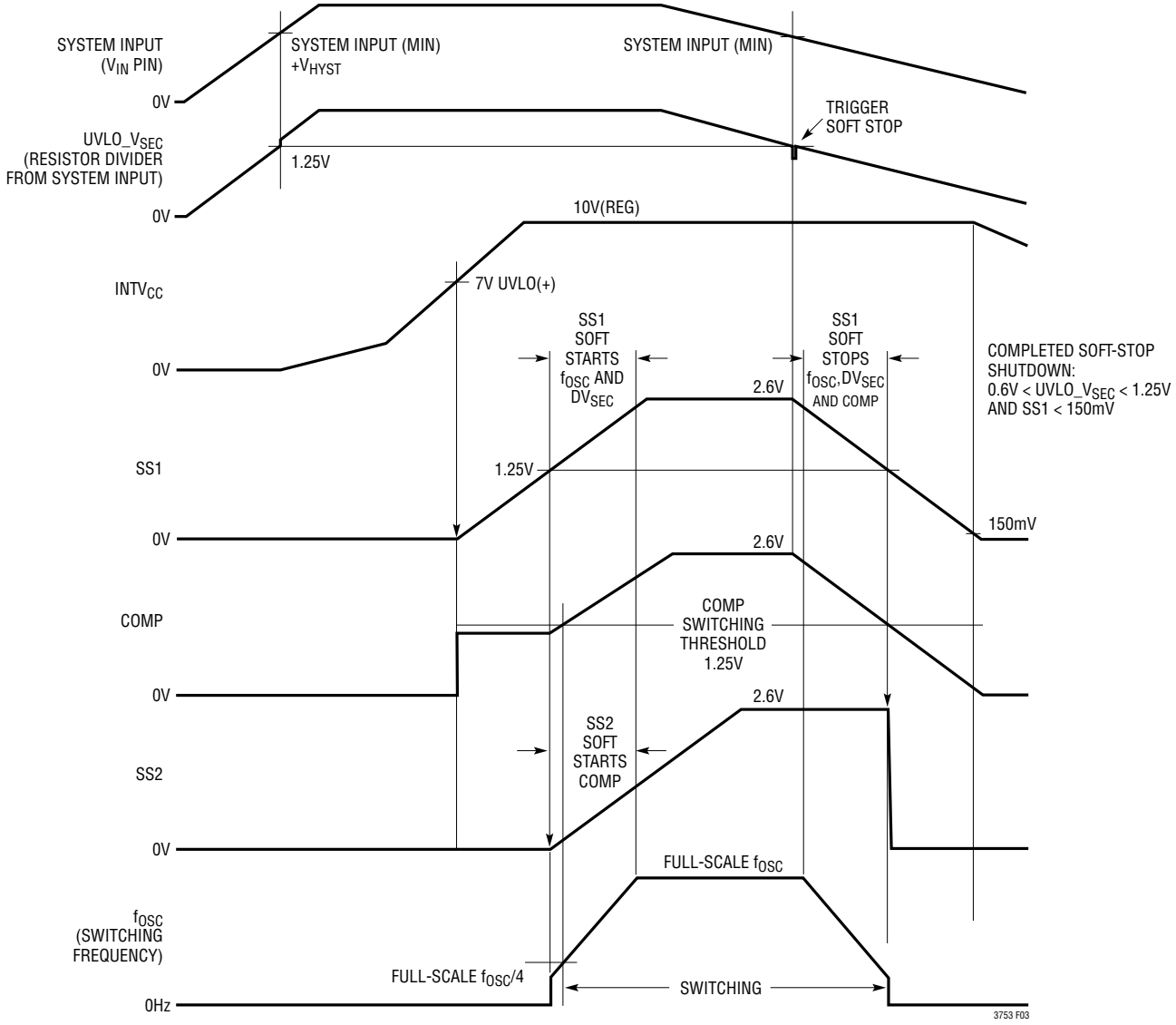


Figure 3. Start-Up and Shutdown Timing Diagram

OPERATION

Introduction

The LT3753 is a primary side, current mode, PWM controller optimized for use in a synchronous forward converter with active clamp reset. The LT3753 allows V_{IN} pin operation between 8.5V and 100V. The LT3753 based forward converter is targeted for power levels up to 400W and is not intended for battery charger applications. For higher power levels the converter outputs can be stacked in series. Connecting UVLO_V_{SEC} pins, OVLO pins, SS1 pins and SS2 pins together allows blocks to react simultaneously to all fault modes and conditions.

The IC contains an accurate programmable volt-second clamp. When set above the natural duty cycle of the converter, it provides a duty cycle guardrail to limit primary switch reset voltage and prevent transformer saturation during load transients. The accuracy and excellent line regulation of the volt-second clamp provides V_{OUT} regulation for open-loop conditions such as no opto-coupler, reference or error amplifier on the secondary side.

For applications not requiring isolation but requiring high step-down ratios, each IC contains a voltage error amplifier to allow a very simple nonisolated, fully regulated synchronous forward converter.

A range of protection features include programmable overcurrent (OC) hiccup mode, programmable system input undervoltage lockout (UVLO), programmable system input overvoltage lockout (OVLO) and built-in thermal shutdown. Programmable slope compensation and switching frequency allow the use of a wide range of output inductor values and transformer sizes.

Part Start-Up

LT3753 start-up is best described by referring to the Block Diagram and to the start-up waveforms in Figure 3. For part start-up, system input voltage must be high enough to drive the UVLO_V_{SEC} pin above 1.25V and the V_{IN} pin must be greater than 8.5V. An internal linear regulator is activated and provides a 10V $INTV_{CC}$ supply for all gate drivers. The SS1 pin of the forward controller is allowed to start charging when $INTV_{CC}$ reaches its 7V UVLO(+) threshold. When SS1 reaches 1.25V, the SS2 pin begins to charge, controlling COMP pin rise and the soft-start of output inductor peak current. The SS1 pin independently soft starts switching frequency and a volt-second clamp from 22% of their full-scale programmed values.

If secondary side control already exists for soft starting the converter output voltage then the SS2 pin can still be used to control initial inductor peak current rise. Simply programming the primary side SS2 soft-start faster than the secondary side allows the secondary side to take over. If SS2 is not needed for soft-start control, its pull-down strength and voltage rating also allow it to drive the input of an opto-coupler connected to $INTV_{CC}$. This allows the option of communicating to the secondary side that switching has begun.

APPLICATIONS INFORMATION

Programming System Input Undervoltage Lockout (UVLO) Threshold and Hysteresis

The LT3753 has an accurate 1.25V shutdown threshold at the UVLO_V_{SEC} pin. This threshold can be used in conjunction with an external resistor divider to define the falling undervoltage lockout threshold (UVLO(–)) for the converter's system input voltage (V_S) (Figure 4). A pin hysteresis current of 5µA allows programming of the UVLO(+) threshold.

V_S (UVLO(–)) [begin SOFT-STOP then shut down]

$$= 1.25\left[1+\left(\frac{R1}{R2+R3}\right)\right]$$

V_S (UVLO(+)) [begin SOFT-START]
= V_S (UVLO(–)) + (5µA • R1)

It is important to note that the part enters soft-stop when the UVLO_V_{SEC} pin falls back below 1.25V. During soft-stop the converter continues to switch as it folds back switching frequency, volt-second clamp and COMP pin voltage. See Soft-Stop in the Applications Information section. When the SS2 pin is finally discharged below its 150mV reset threshold the forward converter is shut down.

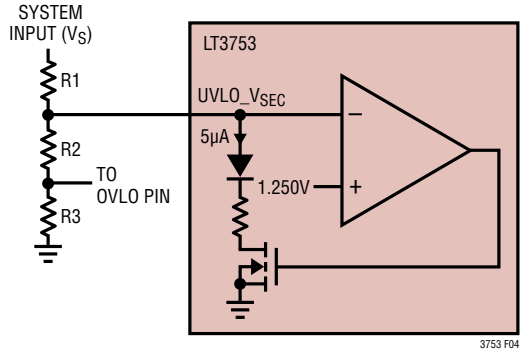


Figure 4. Programming Undervoltage Lockout (UVLO)

Soft-Stop Shutdown

Soft-stop shutdown (similar to system undervoltage) can be commanded by an external control signal. A MOSFET with a diode (or diodes) in series with the drain should be used to pull down the UVLO_V_{SEC} pin below 1.25V but not below the micropower shutdown threshold of 0.6V(max). Typical V_{IN} quiescent current after soft-stop is 165µA.

Micropower Shutdown

If a micropower shutdown is required using an external control signal, an open-drain transistor can be directly connected to the UVLO_V_{SEC} pin. The LT3753 has a micropower shutdown threshold of typically 0.4V at the UVLO_V_{SEC} pin. V_{IN} quiescent current in micropower shutdown is 20µA.

Programming System Input Overvoltage Lockout (OVLO) Threshold

The LT3753 has an accurate 1.25V overvoltage shutdown threshold at the OVLO pin. This threshold can be used in conjunction with an external resistor divider to define the rising overvoltage lockout threshold (OVLO(+)) for the converter's system input voltage (V_S) (Figure 5). When OVLO(+) is reached, the part stops switching immediately and a hard stop discharges the SS1 and SS2 pins. The falling threshold OVLO(–) is fixed internally at 1.215V and allows the part to restart in soft-start mode. A single resistor divider can be used from system input supply (V_S) to define both the undervoltage and overvoltage thresholds for the system. Minimum value for R3 is 1k. If OVLO is unused, place a 10k resistor from OVLO pin to ground.

V_S OVLO(+) [stop switching; HARD STOP]

$$= 1.25\left[1+\left(\frac{R1+R2}{R3}\right)\right]$$

V_S OVLO(–) [begin SOFT-START]

$$= V_S\ \mathrm{OVLO}(+)\bullet\frac{1.215}{1.25}$$

APPLICATIONS INFORMATION

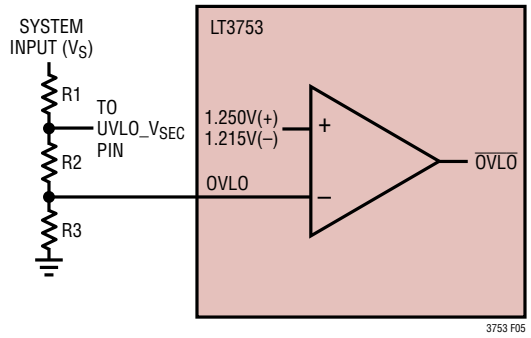


Figure 5. Programming Overvoltage Lockout (OVLO)

Programming Switching Frequency

The switching frequency for the LT3753 is programmed using a resistor, R_T, connected from analog ground (Pin 18) to the RT pin. Table 1 shows typical f_{OSC} vs R_T resistor values. The value for R_T is given by:

$$R_T = 8.39 \bullet X \bullet (1 + Y)$$

where,

$$X = (10^9/f_{OSC}) – 365$$
$$Y = (300kHz – f_{OSC})/10^7 \quad (f_{OSC} < 300kHz)$$
$$Y = (f_{OSC} – 300kHz)/10^7 \quad (f_{OSC} > 300kHz)$$

Example: For f_{OSC} = 200kHz,

$$R_T = 8.39 \bullet 4635 \bullet (1 + 0.01) = 39.28k \text{ (choose 39.2k)}$$

The LT3753 includes frequency foldback at start-up (see Figure 3). In order to make sure that a SYNC input does not override frequency foldback during start-up, the SYNC function is ignored until SS1 pin reaches 2.2V.

Table 1. R_T vs Switching Frequency (f_{OSC})

SWITCHING FREQUENCY (kHz)	R_T (kΩ)
100	82.5
150	53.6
200	39.2
250	30.9
300	24.9
350	21
400	18.2
450	15.8
500	14

Synchronizing to an External Clock

The LT3753 internal oscillator can be synchronized to an external clock at the SYNC pin. SYNC pin high level should exceed 1.8V for at least 100ns and SYNC pin low level should fall below 0.6V for at least 100ns. The SYNC pin frequency should be set equal to or higher than the typical frequency programmed by the RT pin. An f_{SYNC}/f_{OSC} ratio of x (1.0 < x < 1.25) will reduce the externally programmed slope compensation by a factor of 1.2x. If required, the external resistor R_{ISLP} can be reprogrammed higher by a factor of 1.2x. (see Current Sensing and Programmable Slope Compensation).

The part injection locks the internal oscillator to every rising edge of the SYNC pin. If the SYNC input is removed at any time during normal operation the part will simply change switching frequency back to the oscillator frequency programmed by the R_T resistor. This injection lock method avoids the possible issues from a PLL method which can potentially cause a large drop in frequency if SYNC input is removed.

During soft-start the SYNC input is ignored until SS1 exceeds 2.2V. During soft-stop the SYNC input is completely ignored. If the SYNC input is to be used, recall that the programmable duty cycle clamp D_{VSEC} is dependent on the switching frequency of the part (see section Programming Duty Cycle Clamp). R_{IVSEC} should be reprogrammed by 1/x for an f_{SYNC}/f_{OSC} ratio of x.

$INTV_{CC}$ Regulator Bypassing and Operation

The $INTV_{CC}$ pin is the output of an internal linear regulator driven from V_{IN} and provides a 10V supply for onboard gate drivers AOUT, SOUT and OUT. $INTV_{CC}$ should be bypassed with a 4.7µF low ESR, X7R or X5R ceramic capacitor to power ground to ensure stability and to provide enough charge for the gate drivers.

The $INTV_{CC}$ regulator has a minimum 19mA output current limit. This current limit should be considered when choosing the switching frequency and capacitance loading on each gate driver. Average current load on the $INTV_{CC}$ pin for a single gate driver driving an external MOSFET is given as :

$$I_{INTVCC} = f_{OSC} \bullet Q_G$$

APPLICATIONS INFORMATION

where:

f_{OSC} = controller switching frequency

Q_G = gate charge (V_{GS} = $INTV_{CC}$)

While the $INTV_{CC}$ 19mA output current limit is sufficient for LT3753 applications, efficiency and internal power dissipation should also be considered. $INTV_{CC}$ can be externally overdriven by an auxiliary supply (see Generating Auxiliary Supplies in the Applications Information section) to improve efficiency, remove power dissipation from within the IC and provide more than 19mA output current capability. Any overdrive level should exceed the regulated $INTV_{CC}$ level but not exceed 16V.

In the case of a short-circuit fault from $INTV_{CC}$ to ground, the IC reduces the $INTV_{CC}$ output current limit to typically 13mA. The $INTV_{CC}$ regulator has an undervoltage lockout rising threshold, UVLO(+), which prevents gate driver switching until $INTV_{CC}$ reaches 7V and maintains switching until $INTV_{CC}$ falls below a UVLO(–) threshold of 6.8V.

For V_{IN} levels close to or below the $INTV_{CC}$ regulated level, the $INTV_{CC}$ linear regulator may enter dropout. The resulting lower $INTV_{CC}$ level will still allow gate driver switching as long as $INTV_{CC}$ remains above $INTV_{CC}$ UVLO(–) levels. See the Typical Performance Characteristics section for $INTV_{CC}$ performance vs V_{IN} and load current.

Adaptive Leading Edge Blanking Plus Programmable Extended Blanking

The LT3753 provides a ±2A gate driver at the OUT pin to control an external N-channel MOSFET for main power delivery in the forward converter (Figure 7). During gate rise time and sometime thereafter, noise can be generated in the current sensing resistor connected to the source of the MOSFET. This noise can potentially cause a false trip of sensing comparators resulting in early switch turn off and in some cases re-soft-start of the system. To prevent this, LT3753 provides adaptive leading edge blanking of both OC and I_{SENSEP} signals to allow a wide range of MOSFET Q_G ratings. In addition, a resistor R_{TBLNK} connected from T_{BLNK} pin to analog ground (Pin 18) programs an extended blanking duration (Figure 6).

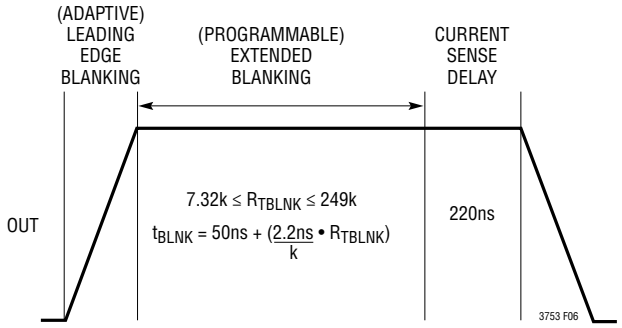


Figure 6. Adaptive Leading Edge Blanking Plus Programmable Extended Blanking

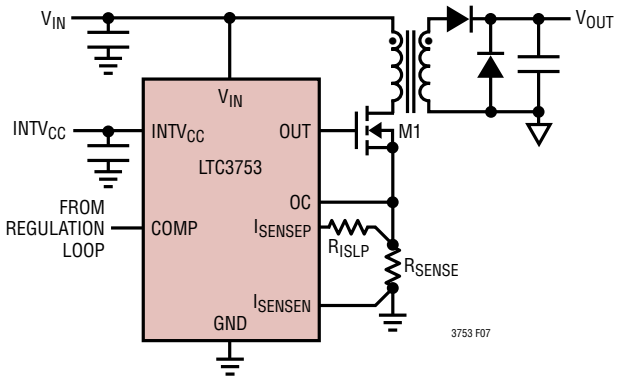


Figure 7. Current Sensing and Programmable Slope Compensation

Adaptive leading edge blanking occurs from the start of OUT rise and completes when OUT reaches within 1V of its maximum level. An extended blanking then occurs which is programmable using the R_{TBLNK} resistor given by:

$$t_{BLNK} = 50ns + \left(\frac{2.2ns}{k} \bullet R_{TBLNK}\right),$$

$$7.32k < R_{TBLNK} < 249k$$

Adaptive leading edge blanking minimizes the value required for R_{TBLNK}. Increasing R_{TBLNK} further than required increases M1 minimum on time (Figure 7).

In addition, the critical volt-second clamp (D_{VSEC}) is not blanked. Therefore, if D_{VSEC} decreases far enough (in soft start foldback and at maximum input voltage) M1 may turn off before blanking has completed. Since OC and I_{SENSEP} signals are only seen when M1 is on (and after blanking has completed), R_{TBLNK} value should be limited by:

$$(2.2ns/k)R_{TBLNK} < T_{VSEC(MIN)} - t_{ADAPTIVE} - 50ns$$

APPLICATIONS INFORMATION

where,

$T_{VSEC(MIN)} = 10^9(D_{VSEC\ (MAX)} /(fold.fosc)) \bullet (Input_{(MIN)}/Input_{(MAX)})$

fold = f_{OSC} and D_{VSEC} foldback ratio (for OUT pin)

$t_{ADAPTIVE}$ = OUT pin rise time to $INTV_{CC}$ – 1V

Example: For Figure 22 circuit, $D_{VSEC(MAX)}$ = 0.77, $Input_{(MIN)/(MAX)}$ = 17.4V/74V, fold = 4, $t_{ADAPTIVE}$ = 23ns and f_{OSC} = 240kHz,

$T_{VSEC(MIN)} = 10^9(0.77/(4 \bullet 2.4 \bullet 10^5)) \bullet 17.4/74 = 188ns$

$(2.2ns/1k)R_{TBLNK} < 188 – 23 – 50$

$R_{TBLNK} < 52.5k$ (Actual Circuit Uses 34k)

Current Sensing and Programmable Slope Compensation

The LT3753 commands cycle-by-cycle peak current in the external switch and primary winding of the forward transformer by sensing voltage across a resistor connected in the source of the external n-channel MOSFET (Figure 7).

The sense voltage across R_{SENSE} is compared to a sense threshold at the I_{SENSEP} pin, controlled by COMP pin level. Two sense inputs, I_{SENSEP} and I_{SENSEN}, are provided to allow a Kelvin connection to R_{SENSE}. For operation in continuous mode and above 50% duty cycle, required slope compensation can be programmed by adding a resistor, R_{ISLP}, in series with the I_{SENSEP} pin. A ramped current always flows out of the I_{SENSE} pin. The current starts from 2µA at 0% duty cycle and linearly ramps to 33µA at 80% duty cycle. A good starting value for R_{ISLP} is 1.5kΩ which gives a 41mV total drop in current comparator threshold at 65% duty cycle.

The COMP pin commands an I_{SENSEP} threshold between 0mV and 220mV. The 220mV allows a large slope compensation voltage drop to exist in R_{ISLP} without effecting the programming of R_{SENSE} to set maximum operational currents in M1. An f_{SYNC}/f_{OSC} ratio of x (1.0 < x < 1.25) will reduce the externally programmed slope compensation by a factor of 1.2x. If required, the external resistor R_{ISLP} can be reprogrammed higher by a factor of 1.2x.

Overcurrent: Hiccup Mode

The LT3753 uses a precise 96mV sense threshold at the OC pin to detect excessive peak switch current (Figure 7). During an overload condition switching stops immediately and the SS1/SS2 pins are rapidly discharged. The absence of switching reduces the sense voltage at the OC pin, allowing SS1/SS2 pins to recharge and eventually attempt switching again. The part exists in this hiccup mode as long as the overcurrent condition exists. This protects the converter and reduces power dissipation in the components (see Hard Stop in the Applications Information section). The 96mV peak switch current threshold is independent of the voltage drop in R_{ISLP} used for slope compensation.

Output DC load current to trigger hiccup mode:

$$= I_{LOAD(OVERCURRENT)}$$

$$= \left(\frac{N_P}{N_S} \bullet \frac{96mV}{R_{ISENSE}}\right) - \left(1/2\ I_{RIPPLE(P-P)}\right)$$

where:

N_P = forward transformer primary turns

N_S = forward transformer secondary turns

$I_{RIPPLE(P-P)}$ = Output inductor peak-to-peak ripple current

R_{ISENSE} should be programmed to allow maximum DC load current for the application plus enough margin during load transients to avoid overcurrent hiccup mode.

Programming Maximum Duty Cycle Clamp: D_{VSEC} (Volt-Second Clamp)

Unlike other converters which only provide a fixed maximum duty cycle clamp, the LT3753 provides an accurate programmable maximum duty cycle clamp (D_{VSEC}) on the OUT pin which moves inversely with system input. D_{VSEC} provides a duty cycle guardrail to limit the volt-seconds-on product over the entire

APPLICATIONS INFORMATION

natural duty cycle range (Figures 8 and 9). This limits the drain voltage required for complete transformer reset. A resistor R_{IVSEC} from the IVSEC pin to analog ground (Pin 18) programs D_{VSEC}.

D_{VSEC} (OUT pin duty cycle clamp)

$$= 0.725 \bullet \frac{R_{IVSEC}}{51.1k} \bullet \frac{f_{OSC}}{300} \bullet \frac{1.25}{UVLO\_V_{SEC}}$$

where:

R_{IVSEC} = programming resistor at IVSEC pin

f_{OSC} = switching frequency (kHz)

$UVLO\_V_{SEC}$ = resistor divided system input voltage

R_{IVSEC} can program any D_{VSEC} required at minimum system input. D_{VSEC} will then follow natural duty cycle as V_{IN} varies. Maximum programmable D_{VSEC} is typically 0.75 but may be further limited by the transformer design and voltage ratings of components connected to the drain of the primary side power MOSFET (SWP). See voltage calculations in the LO side and HI side active clamp topologies sections.

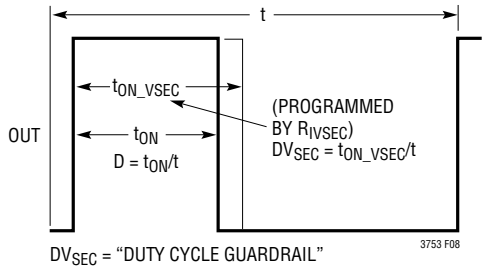


Figure 8. Volt-Second (D_{VSEC}) Clamp

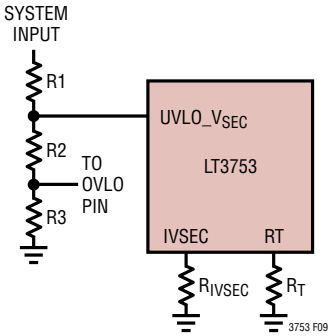


Figure 9. Programming D_{VSEC}

If system input voltage falls below it's UVLO threshold the part will enter soft-stop with continued switching. The LT3753 includes an intelligent circuit which prevents D_{VSEC} from continuing to rise as system input voltage falls (see Soft-Stop). Without this, too large a D_{VSEC} would require extremely high reset voltages on the SWP node to properly reset the transformer. The $UVLO\_V_{SEC}$ pin maximum operational level is the lesser of V_{IN} – 2V or 12.5V.

The LT3753 volt-second clamp architecture is superior to an external RC network connected from system input to trip an internal comparator threshold. The RC method suffers from external capacitor error, part-to-part mismatch between the RC time constant and the IC's switching period, the error of the internal comparator threshold and the nonlinearity of charging at low input voltages. The LT3753 uses the R_{IVSEC} resistor to define the charge current for an internal timer capacitor to set an OUT pin maximum on-time, $t_{ON(VSEC)}$. The voltage across R_{IVSEC} follows $UVLO\_V_{SEC}$ pin voltage (divided down from system input voltage). Hence, R_{IVSEC} current varies linearly with input supply. The LT3753 also trims out internal timing capacitor and comparator threshold errors to optimize part-to-part matching between $t_{ON(VSEC)}$ and T.

D_{VSEC} Open Loop Control: No Opto-Coupler, Error Amplifier or Reference

The accuracy of the programmable volt-second clamp (D_{VSEC}) safely controls V_{OUT} if open loop conditions exist such as no opto-coupler, error amplifier or reference on the secondary side. D_{VSEC} controls the output of the converter by controlling duty cycle inversely proportional to system input. If D_{VSEC} duty cycle guardrail is programmed X% above natural duty cycle, V_{OUT} will only increase by X% if a closed loop system breaks open. This volt-second clamp is operational over a 10:1 system input voltage range. See D_{VSEC} versus $UVLO\_V_{SEC}$ pin voltage in the Typical Performance Characteristics section.

R_{IVSEC}: Open Pin Detection Provides Safety

The LT3753 provides an open-detection safety feature for the R_{IVSEC} pin. If the R_{IVSEC} resistor goes open circuit the part immediately stops switching. This prevents the part from running without the volt-second clamp in place.

APPLICATIONS INFORMATION

Transformer Reset: Active Clamp Technique

The LT3753 includes a ±0.4A gate driver at the AOUT pin to allow the use of an active clamp transformer reset technique (Figures 10, 14). The active clamp method improves efficiency and reduces voltage stress on the main power switch, M1. By switching in the active clamp capacitor only when needed, the capacitor does not lose its charge during M1 on-time. By allowing the active clamp capacitor, C_{CL}, to store the average voltage required to reset the transformer, the main power switch sees lower drain voltage.

In addition, the active clamp drain waveform on M1 (Figure 11) allows a self-driven architecture, whereby the drains of M3 and M4 drive the gates of M4 and M3 respectively, removing the need for a secondary-side synchronous MOSFET driver (Figure 21). In a self-driven architecture, the reset voltage level on M1, V_{OUT} level and duty cycle range (governed by system input range) must be considered to ensure the maximum V_{GS} rating of synchronous MOSFETs M3, M4 are not exceeded.

An imbalance of volt-seconds will cause magnetizing current to walk upwards or downwards until the active clamp capacitor is charged to the optimal voltage for proper transformer reset. The voltage rating of the capacitor will depend on whether the active clamp capacitor is actively switched to ground (Figure 10) or actively switched to system input (Figure 14). In an active clamp reset topology, volt-second balance requires:

$$V_{IN} \bullet D = (SWP - V_{IN}) \bullet (1 - D)$$

where:

V_{IN} = Transformer input supply

$D = (V_{OUT}/V_{IN}) \bullet N$ = switch M1 duty cycle

V_{OUT} = Output voltage (including the voltage drop contribution of M4 catch diode during M1 off)

N = Transformer turns ratio = N_P/N_S

SWP = M1 drain voltage

LO Side Active Clamp Topology (LT3753)

The steady-state active clamp capacitor voltage, V_{CCL}, required to reset the transformer in a LO side active clamp topology (Figure 10) can be approximated as the drain-to-source voltage (V_{DS}) of switch M1, given by:

V_{CCL} (LO side):

(a) Steady state: $V_{CCL} = SWP = V_{DS}$

$$= \left(\frac{1}{1-D}\right) \bullet V_{IN} = \frac{V_{IN}^2}{\left(V_{IN} - \left(V_{OUT} \bullet N\right)\right)}$$

(b) Transient:

During load transients, duty cycle and hence V_{CCL} may increase. Replace D with D_{VSEC} in the equation above to calculate transient V_{CCL} values. See the previous section Programming Duty Cycle Clamp–D_{VSEC}. The D_{VSEC} guardrail can be programmed as close as 5% higher than D but may require a larger margin to improve transient response.

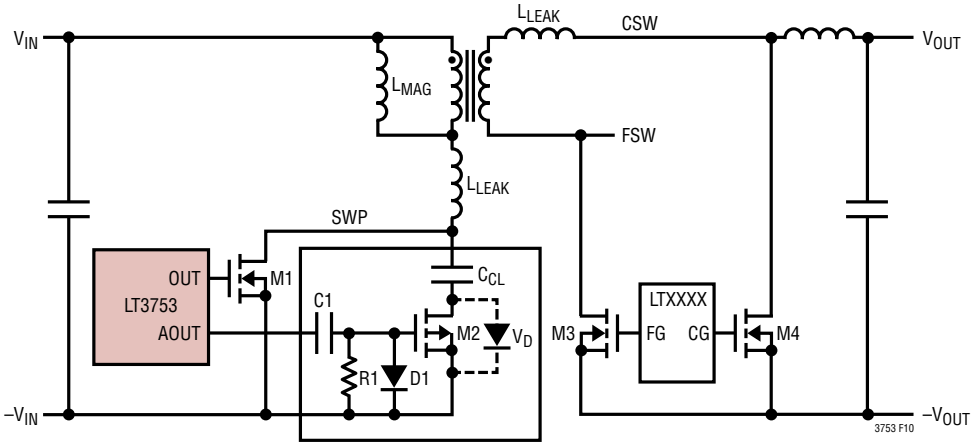


Figure 10. LO Side Active Clamp Topology

APPLICATIONS INFORMATION

As shown in Figure 12, the maximum steady-state value for V_{CCL} may occur at minimum or maximum input voltage. Hence V_{CCL} should be calculated at both input voltage levels and the largest of the two calculations used. M1 drain should be rated for a voltage greater than the above steady-state V_{DS} calculation due to tolerances in duty cycle, load transients, voltage ripple on C_{CL} and leakage inductance spikes. C_{CL} should be rated higher due to the effect of voltage coefficient on capacitance value. A typical choice for C_{CL} is a good quality X7R capacitor. M2 should have a V_{DS} rating greater than V_{CCL} since the bottom plate of C_{CL} is $-V_{CCL}$ during M1 on and M2 off. For high input voltage applications, the limited V_{DS} rating of available P-channel MOSFETs might require changing from a LO side to HI side active clamp topology.

For the lo side active clamp topology in steady state, during M1 on time, magnetizing current (I_{MAG}) increases from a negative value to a positive value (Figure 11). When M1 turns off, magnetizing current charges SWP until it reaches V_{CCL} plus the voltage drop of the M2 body diode. At this

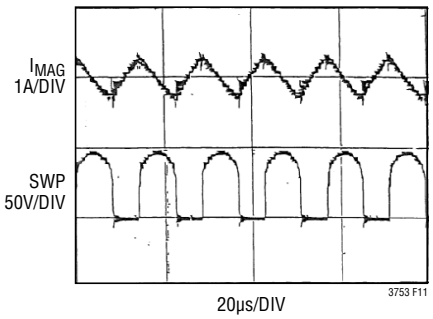


Figure 11. Active Clamp Reset: Magnetizing Current and M1 Drain Voltage

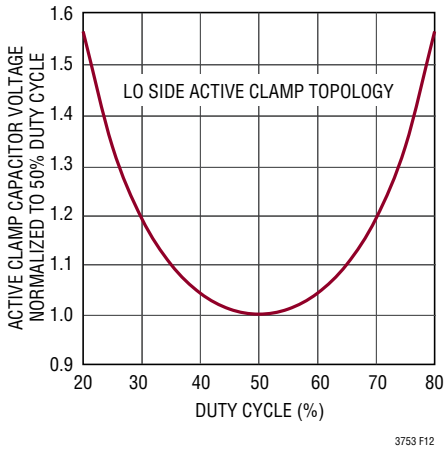


Figure 12. LO Side V_{CCL} vs Duty Cycle (Normalized to 50% Duty Cycle)

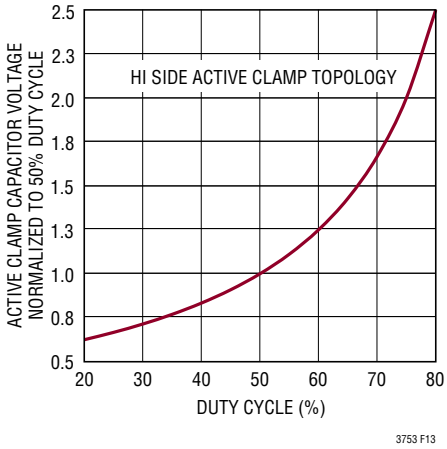


Figure 13. HI Side V_{CCL} vs Duty Cycle (Normalized to 50% Duty Cycle)

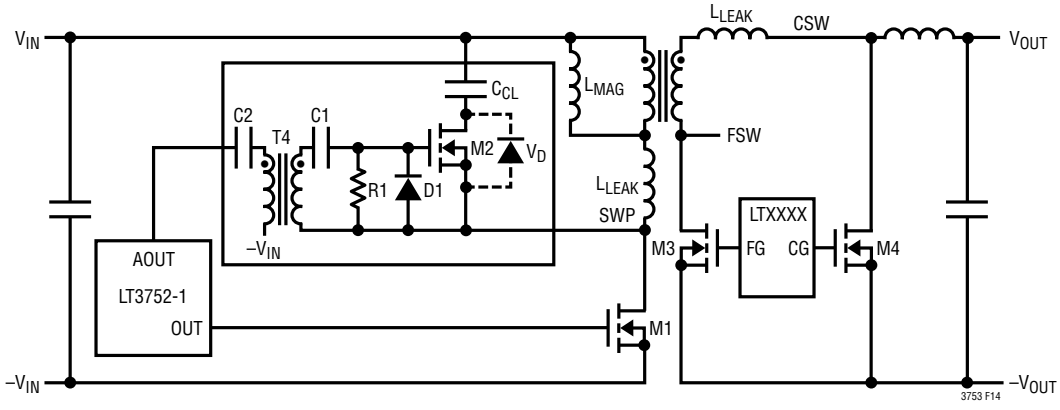


Figure 14. HI Side Active Clamp Topology (Using LT3752-1)

APPLICATIONS INFORMATION

moment the active clamp capacitor is passively switched in to ground (due to the forward conduction of M2 body diode) and the drain voltage increases at a slower rate due to the loading of C_{CL}. SWP above V_{IN} causes I_{MAG} to reduce from a positive value towards zero ($dV_{SWP}/dT = 0$). As I_{MAG} becomes negative it begins to discharge the SWP node. Switching in M2 before I_{MAG} reverses, actively connects the bottom plate of C_{CL} to ground and allows SWP to be discharged slowly. The resulting SWP waveform during M1 off-time appears as a square wave with a superimposed sinusoidal peak representing ripple voltage on C_{CL}.

The switch M2 experiences near zero voltage switching (ZVS) since only the body diode voltage drop appears across it at switch turn on.

HI Side Active Clamp Topology (LT3752-1)

For high input voltage applications the V_{DS} rating of available P-channel MOSFETs might not be high enough to be used as the active clamp switch in the LO side active clamp topology (Figure 10). An N-channel approach using the HI side active clamp topology (Figure 14) should be used. (The LT3752-1 is ideal for the HI side active clamp topology). This topology requires a gate drive transformer or a simple gate drive opto-coupler to drive the N-channel MOSFET (M2) for switching in the active clamp capacitor from SWP to V_{IN}. The M1 drain voltage calculation is the same as in the LO side active clamp case and M1 should be rated in a similar manner. The voltage across the clamp capacitor in the HI side architecture, however, is lower by V_{IN} since it is referenced to V_{IN}.

The steady-state active clamp capacitor voltage V_{CCL} to reset the transformer in a HI side active clamp topology can be approximated by:

V_{CCL} (HI side):

(a) Steady state: $V_{CCL} = V_{RESET} = V_{DS} - V_{IN}$

$$= \left(\frac{D}{1-D}\right) \bullet V_{IN} = V_{IN} \bullet V_{OUT} \bullet \frac{N}{V_{IN} - \left(V_{OUT} \bullet N\right)}$$

(b) Transient:

During load transients, duty cycle and hence V_{CCL} may increase. Replace D with D_{VSEC} in the equation above to calculate transient V_{CCL} values. D_{VSEC} guardrail can be programmed as close as 6% higher than D but may require a larger margin to improve transient response. See the previous section Programming Duty Cycle Clamp–D_{VSEC}.

C_{CL} should be rated for a voltage higher than the above steady-state calculation due to tolerances in duty cycle, load transients, voltage ripple on C_{CL} and the effect of voltage coefficient on capacitance value. A typical choice for C_{CL} is a good quality (X7R) capacitor. When using a gate drive transformer to provide control of the active clamp switch (M2), the external components C1, C2, R1, D1 and T4 are required. T4 size will increase for lower programmed switching frequencies due to a minimum volt-second requirement. Alternatively, a simple gate driver opto-coupler can be used as a switch to control M2, for a smaller solution size.

Active Clamp Capacitor Value and Voltage Ripple

The active clamp capacitor value should be chosen based on the amount of voltage ripple which can be tolerated by components attached to SWP. Lower C_{CL} values will create larger voltage ripple (increased drain voltage for the primary side power MOSFET) but will require less swing in magnetizing current to move the active clamp capacitor during duty cycle changes. Choosing too high a value for the active clamp capacitor (beyond what is needed to keep ripple voltage to an acceptable level) will require unnecessary additional flux swing during transient conditions. For systems with flux swing detection, too high a value for the active clamp capacitor will trigger the detection system early and degrade transient response.

Another factor to consider is the resonance between C_{CL} and the magnetizing inductance (L_{MAG}) of the main transformer. An RC snubber (R_S, C_S) in parallel with C_{CL} will dampen

APPLICATIONS INFORMATION

the sinusoidal ringing and limit the peak voltages at the primary side MOSFET drain during input/load transients. Check circuit performance to determine if the snubber is required. Component values can be approximated as:

$$C_{CL}\ (\text{active clamp capacitance}) = \frac{10}{L_{MAG}} \bullet \left(\frac{(1-D_{MIN})}{2 \bullet \pi \bullet f_{OSC}}\right)^2$$

where,

$D_{MIN} = (V_{OUT}/V_{IN(MAX)}) \bullet N_P/N_S$

and (if needed),

C_S (snubber capacitance) = $6 \bullet C_{CL}$

R_S (snubber resistance) = $(1/(1\text{-}D_{MAX})) \bullet \sqrt{(L_{MAG}/C_{CL})}$

where,

$D_{MAX} = (V_{OUT}/V_{IN(MIN)}) \bullet N_P/N_S$

Check the voltage ripple on SWP during steady-state operation.

C_{CL} voltage ripple can be estimated as:

$V_{CCL(RIPPLE)} = V_{CCL} \bullet (1\text{-}D)^2/(8 \bullet C_{CL} \bullet L_{MAG} \bullet f_{OSC}^2)$

where,

$D = (V_{OUT}/V_{IN}) \bullet (N_P/N_S)$

$V_{CCL} = V_{IN}/(1\text{-}D)$ (Lo side active clamp topology)

$V_{CCL} = D \bullet V_{IN}/(1\text{-}D)$ (Hi side active clamp topology)

Example : For V_{IN} = 36V, V_{OUT} = 12V, N_P/N_S = 2, V_{CCL} = 108V (Lo side active clamp topology), C_{CL} = 22nF, L_{MAG} = 100µH, f_{OSC} = 250kHz, $V_{CCL(RIPPLE)} = 108(0.33)^2/(8(22 \bullet 10^{-9})(10^{-4})(2.5 \bullet 10^5)^2)$ = 10.7V

The transformer is typically chosen to operate at a maximum flux density that is low enough to avoid excessive core losses. This also allows enough headroom during input and load transients to move the active clamp capacitor at a fast enough rate to keep up with duty cycle changes.

Active Clamp MOSFET Selection

The selection of active clamp MOSFET is determined by the maximum levels expected for the drain voltage and drain current. The active clamp switch (M2) in a either a lo side or hi side active clamp topology has the same BVdss requirements as the main N-channel power MOSFET. The current requirements are divided into two categories :

(A) Drain Current

This is typically less than the main N-channel power MOSFET because the active clamp MOSFET sees only magnetizing current, estimated as :

Peak I_{MAG} (steady state) = $(1/2) \bullet (N_P/N_S) \bullet (V_{OUT}/L_{MAG}) \bullet (1/f_{OSC})$

where,

L_{MAG} = main transformer's magnetizing inductance

Example (LT3752) : For V_{OUT} =12V, N_P/N_S = 2, f_{OSC} = 250kHz and L_{MAG} = 100µH, Peak I_{MAG} = 0.48A.

This value should be doubled for safety margin due to variations in L_{MAG}, f_{OSC} and transient conditions.

(B) Body Diode Current

The body diode will see reflected output current as a pulse every time the main N-channel power MOSFET turns off. This is due to residual energy stored in the transformer's leakage inductance. The body diode of the active clamp MOSFET should be rated to withstand a forward pulsed current of:

$I_{D(MAX)} = (N_S/N_P)\ (I_{OUT(MAX)} + (I_{L(RIPPLE)(P\text{-}P)}/2))$

where,

$I_{L(RIPPLE)(P\text{-}P)}$ = output inductor ripple current = $(V_{OUT}/(L_{OUT} \bullet f_{OSC})) \bullet (1-(V_{OUT}/V_{IN})(N_P/N_S))$

$I_{OUT(MAX)}$ = maximum output load current

APPLICATIONS INFORMATION

Programming Active Clamp Switch Timing: AOUT to OUT (t_{AO}) and OUT to AOUT (t_{OA}) Delays

The timings t_{AO} and t_{OA} represent the delays between AOUT and OUT edges (Figures 1 and 2) and are programmed by a single resistor, R_{TAO}, connected from analog ground (Pin 18) to the T_{AO} pin. Once t_{AO} is programmed for the reasons given below, t_{OA} will be automatically generated.

Front-end timing t_{AO} (M2 off, M1 on)

= AOUT(edge)-to-OUT(rising)

$$= 50ns + 3.8ns \bullet \left(\frac{R_{TAO}}{1k}\right), 14.7 < R_{TAO} < 125k$$

In order to minimize turn-on transition loss in M1 the drain of M1 should be as low as possible before M1 turns on. To achieve this, AOUT should turn M2 off a delay of t_{AO} before OUT turns M1 on. This allows the main transformer's magnetizing current to discharge M1 drain voltage quickly towards V_{IN} before M1 turns on.

As SWP falls below V_{IN}, however, the rectifying diodes on the secondary side are typically active and clamp the SWP node close to V_{IN}. If enough leakage inductance exists, however, the clamping action on SWP by the secondary side will be delayed—potentially allowing the drain of M1 to be fully discharged to ground just before M1 turns on. Even with this delay due to the leakage inductance, L_{MAG} needs to be low enough to allow I_{MAG} to be negative enough to slew SWP down to ground before M1 turns on. If achievable, M1 will experience zero voltage switching (ZVS) for highest efficiency. As will be seen in a later section entitled Primary-Side Power MOSFET Selection, M1 transition loss is a significant contributor to M1 losses.

Back-end timing t_{OA} (M1 off, M2 on) is automatically generated

= OUT(falling)-to-AOUT(edge) = $0.9 \bullet t_{AO}$

t_{OA} should be checked to ensure M2 is not turned on until M1 and M3 are turned off.

Programming Synchronous Rectifier Timing: SOUT to OUT (t_{SO}) and OUT to SOUT (t_{OS}) Delays

The LT3753 includes a ±0.4A gate driver at the SOUT pin to send a control signal via a pulse transformer to the secondary side of the forward converter for synchronous rectification (see Figures 1 and 2). For the highest efficiency, M4 should be turned on whenever M1 is turned off. This suggests that SOUT should be a non-overlapping signal with OUT with very small non-overlap times. Inherent timing delays, however, which can vary from application to application, can exist between OUT to CSW and between SOUT to CG. Possible shoot-through can occur if both M1 and M4 are on at the same time, resulting in transformer and/or switch damage.

Front-end timing: t_{SO} (M4 off, M1 on)

= SOUT(falling)-to-OUT(rising) delay

$= t_{SO} = t_{AO} - t_{AS}$

$= 3.8ns \bullet (R_{TAS} - R_{TAO})$

where:

$t_{AS} = 50ns + (3.8ns \bullet R_{TAS}/1k)$, $14.7k < R_{TAS} < 125k$,

$t_{AO} = 50ns + (3.8ns \bullet R_{TAO}/1k)$, $14.7k < R_{TAO} < 125k$,

t_{SO} is defined by resistors R_{TAS} and R_{TAO} connected from analog ground (Pin 18) to their respective pins T_{AS} and T_{AO}. Each of these resistor defines a delay referenced to the AOUT edge at the start of each cycle. R_{TAO} was already programmed based on requirements defined in the previous section Programming AOUT to OUT Delay. R_{TAS} is then programmed as a delay from AOUT to SOUT to fulfill the equation above for t_{SO}. By choosing R_{TAS} less than or greater than R_{TAO}, the delay between SOUT falling and OUT rising can be programmed as positive or negative. While a positive delay can always be programmed for t_{SO}, the ability to program a negative delay allows for improved efficiency if OUT(rising)-to-CSW(rising) delay is larger than SOUT(falling)-to-CG(rising) delay.

Back-end timing: t_{OS} (M1 off, M4 on)

= OUT (falling)-to-SOUT (rising) delay

$= t_{OS} = 35ns + (2.2ns \bullet R_{TOS}/1k)$, $7.32k < R_{TOS} < 249k$

APPLICATIONS INFORMATION

The timing resistor, R_{TOS}, defines the OUT (falling)-to-SOUT (rising) delay. This pin allows programming of a positive delay, for applications which might have a large inherent delay from OUT fall to SW2 fall.

Soft-Start (SS1, SS2)

The LT3753 uses SS1 and SS2 pins for soft starting various parameters (Figures 3 and 15). SS1 soft starts internal oscillator frequency and D_{VSEC} (maximum duty cycle clamp). SS2 soft starts COMP pin voltage to control output inductor peak current. Using separate SS1 and SS2 pins allows the soft-start ramp of oscillator frequency and D_{VSEC} to be independent of COMP pin soft-start. Typically SS1 capacitor (C_{SS1}) is chosen as 0.47µF and SS2 capacitor (C_{SS2}) is chosen as 0.1µF. Soft-start charge currents are 11.5µA for SS1 and 21µA for SS2.

SS1 is allowed to start charging (soft-start) if all of the following conditions exist (typical values) :

(1) UVLO_V_{SEC} > 1.25V: System input not in UVLO

(2) OVLO < 1.215V: System input not in OVLO

(3) OC < 96mV: No over current condition

(4) 7V < $INTV_{CC}$ < 16V: $INTV_{CC}$ valid

(5) T_J < 165°C: Junction temperature valid

(6) V_{IN} > 7.75V: V_{IN} pin valid

SS1 = 0V to 1.25V (no switching). This is the SS1 range for no switching for the forward converter. SS2 = 0V.

SS1 > 1.25V allows SS2 to begin charging from 0V.

SS1 = 1.25V to 2.45V (soft-start f_{OSC}, D_{VSEC}). This is the SS1 range for soft-starting f_{OSC} and D_{VSEC} folded back from 22% to 100% of their programmed levels. Fold back of f_{OSC} and D_{VSEC} reduces effective minimum duty cycle for the primary side MOSFET. This allows inductor current to be controlled at low output voltages during start-up.

SS1 ramp rate is chosen slow enough to ensure f_{OSC} and D_{VSEC} foldback lasts long enough for the converter to take control of inductor current at low output voltages. In addition, slower SS1 ramp rate increases the non-switching period during an output short to ground fault (over current hiccup mode) to reduce average power dissipation (see Hard-Stop).

SS2 = 0V to 1.6V (soft-start COMP pin). This is the SS2 range for soft-starting COMP pin from approximately 1V to 2.6V.

SS2 ramp rate is chosen fast enough to allow a (slower) soft-start control of COMP pin from a secondary side opto-coupler controller.

SS1 soft-start non-switching period (0V to 1.25V) = 1.25V • C_{SS1}/11.5µA

SS1 soft-start f_{OSC}, D_{VSEC} period (1.25V to 2.45V) = 1.2V • C_{SS1}/11.5µA

SS2 soft-start COMP period (0V to 1.6V) = 1.6V • C_{SS2}/21µA

Soft-Stop (SS1)

The LT3753 gradually discharges the SS1 pin (soft-stop) when a system input UVLO occurs or when an external soft-stop shutdown command occurs (0.4V < UVLO_V_{SEC} < 1.25V). During SS1 soft-stop the converter continues to switch, folding back f_{OSC}, D_{VSEC} and COMP pin voltage (Figures 3 and 15). Soft-stop discharge current is 10.5µA for SS1. Soft-stop provides:

(1) Active control of the secondary winding during output discharge for clean shutdown in self-driven applications.

(2) Controlled discharge of the active clamp capacitor to minimize magnetizing current swing during restart.

SS1: 2.45V to 1.25V (soft-stop f_{OSC}, D_{VSEC}, COMP). This is the SS1 range for soft-stop folding back of:

(1) f_{OSC} and D_{VSEC} from 100% to 22% of their programmed levels.

(2) COMP pin (100% to 0% of commanded peak current).

SS1 soft-stop f_{OSC} , D_{VSEC}, COMP period (2.45V to 1.25V) = 1.2V • C_{SS1}/10.5µA

APPLICATIONS INFORMATION

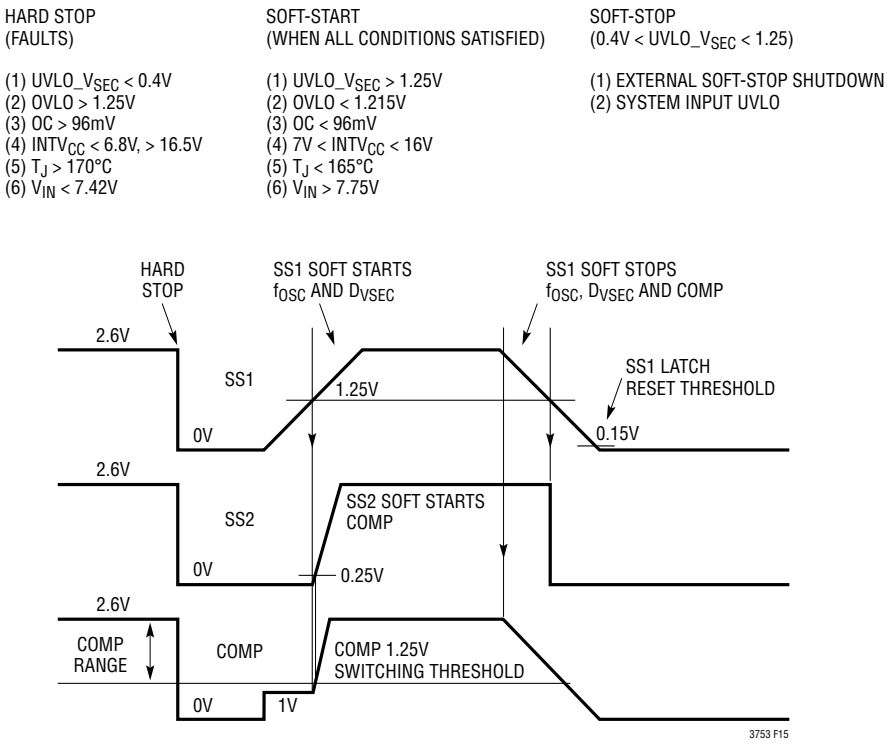


Figure 15. SS1, SS2 and COMP Pin Voltages During Faults, Soft-Start and Soft-Stop

SS1 < 1.25V. Forward converter stops switching and SS2 pin is discharged to 0V using 2.8mA.

SS1 = 1.25V to 0V: When SS1 falls below 0.15V the internal SS1 latch is reset. If all faults are removed, SS1 begins charging again. If faults still remain, SS1 discharges to 0V.

SS1 soft-stop non-switching period (1.25V to 0V) = 1.25V • C_{SS1}/10.5µA

D_{VSEC} rises as system input voltage falls in order to provide a maximum duty cycle guardrail (volt-second clamp). When system input falls below it's UVLO threshold, however, this triggers a soft-stop with the converter continuing to switch. It is important that D_{VSEC} no longer increases even though system input voltage may still be falling. The LT3753 achieves an upper clamp on D_{VSEC} by clamping the minimum level for the I_{VSEC} pin to 1.25V. As SS1 pin discharges during soft-stop it folds back D_{VSEC}. As D_{VSEC} falls below the natural duty cycle of the converter, the converter loop follows D_{VSEC}. If the system input voltage rises (I_{VSEC} pin rises) during soft-stop the volt-second clamp circuit further reduces D_{VSEC}. The I.C. chooses the lowest D_{VSEC} commanded by either the I_{VSEC} pin or the SS1 soft-stop function.

Hard-Stop (SS1, SS2)

Switching immediately stops and both SS1 and SS2 pins are rapidly discharged (Figure 15. Hard-Stop) if any of the following faults occur (typical values):

(1) UVLO_V_{SEC} < 0.4V: Micropower shutdown

(2) OVLO > 1.250V: System input OVLO

(3) OC > 96mV: Over current condition

(4) $INTV_{CC}$ < 6.8V(UVLO), > 16.5V (OVLO)

(5) T_J > 170°C: Thermal shutdown

(6) V_{IN} < 7.42: V_{IN} pin UVLO

APPLICATIONS INFORMATION

Switching stops immediately for any of the faults listed above. When SS1 discharges below 0.15V it begins charging again if all faults have been removed. For an over current fault triggered by OC > 96mV, the disable of switching will cause the OC pin voltage to fall back below 96mV. This will allow SS1 and SS2 to recharge and eventually attempt switching again. If the over current condition still exists, OC pin will exceed 96mV again and the discharge/charge cycle of SS1 and SS2 will repeat in a hiccup mode. The non-switching dead time period during hiccup mode reduces the average power seen by the converter in an over current fault condition. The dead time is dominated by SS1 recharging from 0.15V to 1.25V.

Non-switching period in over current (hiccup mode): $= 1.1V \bullet C_{SS1}/11.5\mu A$

OUT, AOUT, SOUT Pulse-Skipping Mode

During load steps, initial soft-start, end of soft-stop or light load operation (if the forward converter is designed to operate in DCM), the loop may require pulse skipping on the OUT pin. This occurs when the COMP pin falls below its switching threshold. If the COMP pin falls below it's switching threshold while OUT is turned on, the LT3753 will immediately turn OUT off ; both AOUT and SOUT will complete their normal signal timings referenced from the OUT falling edge. If the COMP pin remains below it's switching threshold at the start of the next switching cycle, the LT3753 will skip the next OUT pulse and therefore also skip AOUT and SOUT pulses. For AOUT control, this prevents the active clamp capacitor from being accidentally discharged during missing OUT pulses and/or causing reverse saturation of the transformer. For SOUT control, this prevents the secondary side synchronous rectifier controller from incorrectly switching between forward FET and synchronous FET conduction. The LT3753 correctly re-establishes the required AOUT, SOUT control signals if the OUT signal is required for the next cycle.

AOUT Timeout

During converter start-up in soft-start, the switching frequency and maximum duty cycle clamp D_{VSEC} are both folded back. While this correctly reduces the effective minimum on time of the OUT pin (to allow control of inductor current for very low output voltages during start-up), this means the AOUT pin on time duration can be large. In order to ensure the active clamp switch controlled by AOUT does not stay on too long, the LT3753 has an internal 15µs timeout to turn off the AOUT signal. This prevents the active clamp capacitor from being connected across the transformer primary winding long enough to create reverse saturation.

Main Transformer Selection

The selection of the main transformer will depend on the applications requirements : isolation voltage, power level, maximum volt-seconds, turns ratio, component size, power losses and switching frequency.

Transformer construction using the planar winding technology is typically chosen for minimizing leakage inductance and reducing component height. Transformer core type is usually a ferrite material for high frequency applications.

Find a family of transformers that meet both the isolation and power level requirements of the application. The next step is to find a transformer within that family which is suitable for the application. The subsequent thought process for the transformer design will include :

(1) Secondary turns (N_S), core losses, temperature rise, flux density, switching frequency

(2) Primary turns (N_P), maximum duty cycle and reset voltages

(3) Copper losses

The expression for secondary turns (N_S) is given by,

$$N_S = 10^8 V_{OUT}/(f_{OSC} \bullet A_C \bullet B_M)$$

APPLICATIONS INFORMATION

where,

A_C = cross-sectional area of the core in cm^2

B_M = maximum AC flux density desired

For flux density, choose a level which achieves an acceptable level of core loss/temperature rise at a given switching frequency. The transformer data sheet will provide curves of core loss versus flux density at various switching frequencies. The data sheet will also provide temperature rise versus core loss. While choosing a value for BM to avoid excessive core losses will usually allow enough headroom for flux swing during input / load transients, still make sure to stay well below the saturation flux density of the transformer core. If needed, increasing N_S will reduce flux density. After calculating N_S, the number of primary turns (N_P) can be calculated from,

$$N_P = N_S \bullet D_{MAX}\ V_{IN(MIN)}/V_{OUT}$$

where,

$V_{IN(MIN)}$ = minimum system input voltage

D_{MAX} = maximum switch duty cycle at $V_{IN(MIN)}$ (typically chosen between 0.6 and 0.7)

At minimum input voltage the converter will run at a maximum duty cycle D_{MAX}. A higher transformer turns ratio (N_P/N_S) will create a higher D_{MAX} but it will also require higher voltages at the drain of the primary side switch to reset the transformer (see previous sections Lo side Active Clamp Topology and Hi side Active Clamp Topology). D_{MAX} values are typically chosen between 0.6 and 0.7. Even for a given D_{MAX} value, the loop must also provide protection against duty cycles that may excessively exceed D_{MAX} during transients or faults. While most converters only provide a fixed duty cycle clamp, the LT3753 provides a programmable maximum duty cycle clamp D_{VSEC} that also moves inversely with input voltage.

The resulting function is that of a programmable volt-second clamp. This allows the user to choose a transformer turns ratio for D_{MAX} and then customize a maximum duty cycle clamp D_{VSEC} above D_{MAX} for safety. D_{VSEC} then follows the natural duty cycle of the converter as a safety guardrail (see previous section Programming Duty Cycle Clamp).

After deciding on the particular transformer and turns ratio, the copper losses can then be approximated by,

$$P_{CU} = D \bullet I(Load)_{(MAX)}^2\ (R_{SEC} + (N_S/N_P)^2\ R_{PRI})$$

where,

D = switch duty cycle (choose nominal 0.5)

$I(Load)_{(MAX)}$ = maximum load current

R_{PRI} = primary winding resistance

R_{SEC} = secondary winding resistance

If there is a large difference between the core losses and the copper losses then the number of secondary turns can be adjusted to achieve a more suitable balance. The number of primary turns should then be recalculated to maintain the desired turns ratio.

Generating Auxiliary Supplies

In many isolated forward converter applications, an auxiliary bias may be required for the primary-side circuitry and/or the secondary-side circuitry. This bias is required for various reasons: to limit voltages seen by an IC, to improve efficiency, to remove power dissipation from inside an IC and/or to power an IC before target output voltage regulation is achieved ((eg) during V_{OUT} start-up).

The best method for generating an auxiliary supply, that is available even for V_{OUT} = 0V, is to have a housekeeping controller integrated into the primary-side IC (Figure 16). This gives the highest efficiency, most cost effective

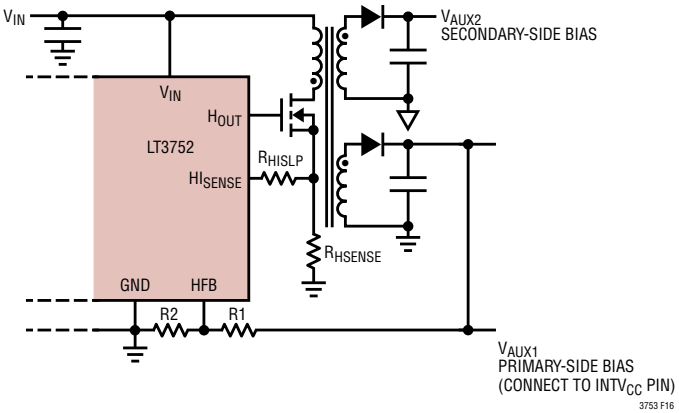


Figure 16. LT3752 Forward Controller with Additional Integrated Housekeeping Controller for Primary-Side and Secondary-Side Bias

APPLICATIONS INFORMATION

solution without the need for custom magnetics (limiting selection) or the need for an additional flyback controller IC. The LT3752 is a primary-side forward controller IC with an integrated housekeeping controller and can be easily substituted for the LT3753.

For isolated solutions without a housekeeping controller, there are alternative methods for generating an auxiliary supply for primary-side and secondary-side circuitry. Each method, however, will have trade-offs from the recommended housekeeping controller solution.

Primary-Side Auxiliary Supply

The LT3753 can operate without a primary-side auxiliary supply since the V_{IN} pin has a wide operational range. The current required for all of the gate drivers (OUT, AOUT and SOUT) is supplied by an internal linear regulator connected between V_{IN} and $INTV_{CC}$. If the efficiency loss and/or power dissipation and/or current drive capability of that internal linear regulator is a limiting factor in the forward converter design, then a primary-side bias (V_{AUX1}) can be generated to overdrive the $INTV_{CC}$ pin (Figure 17). V_{AUX1} is generated using an extra winding (N_{AUX}) from the main power transformer in combination with an inductor (L1) and two Schottky diodes (D1, D2) to generate a buck-derived supply. A 1mH inductor will usually suffice and should be chosen to handle the maximum supply current required by $INTV_{CC}$. See also the section $INTV_{CC}$ Regulator Bypassing and Operation in the Applications Information Section.

Secondary-Side Auxiliary Supply

There are various methods for generating an auxiliary supply to power secondary-side circuitry. The LT8311 synchronous rectifier controller and opto coupler driver IC can be powered in several ways including connection directly to V_{OUT}. While this is the easiest method, there are various guidelines described in the LT8311 data sheet for

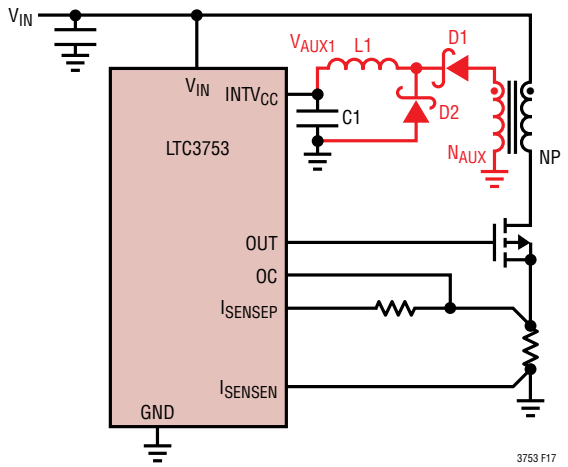


Figure 17. Primary-Side Bias V_{AUX1} (N_{AUX}, L1, D1, D2)

APPLICATIONS INFORMATION

powering it's V_{IN} pin. In most cases a an auxiliary supply is the best approach. The following methods can be used to generate a bias (V_{AUX2}) to power secondary-side circuitry :

(1) Use a primary-side forward controller with integrated housekeeping controller to generate a secondary-side bias (Figure 16).

(2) Use a buck-derived bias using an extra winding from the main power transformer (similar method as Figure 17, applied to secondary-side circuitry)

(3) Use a custom output inductor with overwinding (Figure 18).

(4) Use a peak-charge circuit (Figures 19 (a), (b), (c)).

Whichever method is used to create the auxiliary supply for secondary-side circuitry, the forward converter should be tested to ensure the auxiliary supply is acceptable for voltage range, supply current requirements and behavior during converter power-up/down.

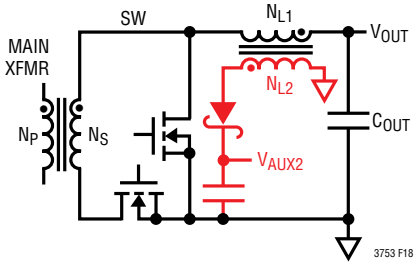


Figure 18. Output Inductor with Overwinding Supply

Primary-Side Power MOSFET Selection

The selection of the primary-side N-channel power MOSFET M1 is determined by the maximum levels expected for the drain voltage and drain current. In addition, the power losses due to conduction losses, gate driver losses and transition losses will lead to a fine tuning of the MOSFET selection. If power losses are high enough to cause an unacceptable temperature rise in the MOSFET then several MOSFETs may be required to be connected in parallel.

The maximum drain voltage expected for the MOSFET M1 follows from the equations previously stated in the active clamp topology sections:

$$V_{DS}\ (M1) = V_{IN}^2/(V_{IN} - (V_{OUT} \bullet N))$$

The MOSFET should be selected with a BV_{DSS} rating approximately 20% greater than the above steady state V_{DS} calculation due to tolerances in duty cycle, load transients, voltage ripple on C_{CL} and leakage inductance spikes. A MOSFET with the lowest possible voltage rating for the application should be selected to minimize switch on resistance for improved efficiency. In addition, the MOSFET should be selected with the lowest gate charge to further minimize losses.

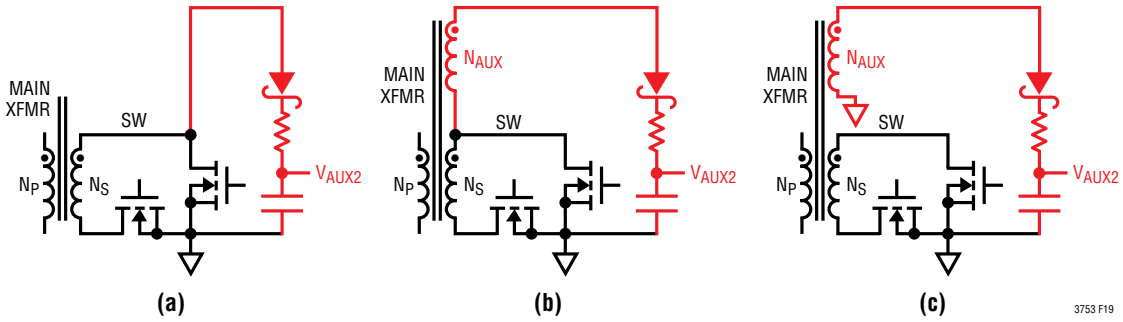


Figure 19. Peak Charge Supply: (a) Directly from SW, (b) For Low V_{OUT} Applications, (c) For High V_{OUT} Applications

APPLICATIONS INFORMATION

MOSFET M1 losses at maximum output current can be approximated as :

$P_{M1} = P_{CONDUCTION} + P_{GATEDRIVER} + P_{TRANSITION}$

(i) $P_{CONDUCTION} = (N_P/N_S) \bullet (V_{OUT}/V_{IN}) \bullet (N_S/N_P \bullet I_{OUT(MAX)})^2 \bullet R_{DS(ON)}$

Note: The on resistance of the MOSFET, $R_{DS(ON)}$, increases with the MOSFET's junction temperature. $R_{DS(ON)}$ should therefore be recalculated once junction temperature is known. A final value for $R_{DS(ON)}$ and therefore $P_{CONDUCTION}$ can be achieved from a few iterations.

(ii) $P_{GATEDRIVER} = (Q_G \bullet INTV_{CC} \bullet f_{OSC})$

where,

Q_G = gate charge ($V_{GS} = INTV_{CC}$)

(iii) $P_{TRANSITION} = P_{TURN\_OFF} + P_{TURN\_ON}$ (≈ 0 if ZVS)

(a) $P_{TURN\_OFF} = (1/2)I_{OUT(MAX)}(N_S/N_P)(V_{IN}/1\text{-}D)(Q_{GD}/I_{GATE}) \bullet f_{OSC}$

where,

Q_{GD} = gate to drain charge

I_{GATE} = 2A source/sink for OUT pin gate driver

(b) $P_{TURN\_ON} = (1/2)I_{OUT(MAX)}(N_S/N_P)(V_{DS})(Q_{GD}/I_{GATE}) \bullet f_{OSC}$

where,

V_{DS} = M1 drain voltage at the beginning of M1 turn on

V_{DS} typically sits between V_{IN} and 0V (ZVS)

During programmable timing t_{AO}, negative I_{MAG} discharges M1 drain SWP towards V_{IN} (Figure 1). ZVS is achieved if enough leakage inductance exists—to delay the secondary side from clamping M1 drain to V_{IN}—and if enough energy is stored in L_{MAG} to discharge SWP to 0V during that delay. (see Programming Active Clamp Switch Timing: AOUT to OUT (t_{AO})).

Synchronous Control (SOUT)

The LT3753 uses the SOUT pin to communicate synchronous control information to the secondary side synchronous rectifier controller (Figure 20). The isolating transformer (T_{SYNC}), coupling capacitor (C_{SYNC}) and resistive load (R_{SYNC}) allow the ground referenced SOUT signal to generate positive and negative signals required at the SYNC input of the secondary side synchronous rectifier controller. For the typical LT3753 applications operating with an LT8311, C_{SYNC} is 220pF, R_{SYNC} is 560Ω and T_{SYNC} is typically a PULSE PE-68386NL.

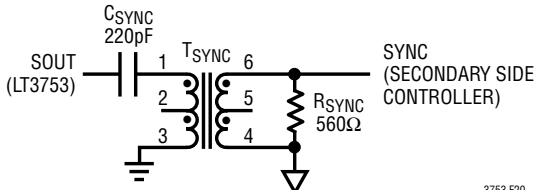


Figure 20. SOUT Pulse Transformer

Typically choose C_{SYNC} between 220pF and 1nF. R_{SYNC} should then be chosen to obey :

(1) $SOUT_{MAX}/100mA \le R_{SYNC} \le \sqrt{(L_{MAG}/C_{SYNC})}$

where,

$SOUT_{MAX} = INTV_{CC}$

L_{MAG} = $T_{SYNC'S}$ magnetizing inductance

100mA = SOUT gate driver minimum source current

and

(2) $R_{SYNC} \bullet C_{SYNC} \ge (-1) \bullet Y/(\ln (Z/SOUT_{MAX}))$

APPLICATIONS INFORMATION

where,

Y = SYNC minimum pulse duration (50ns; LT8311)

Z = |SYNC level to achieve Y| (±2V: LT8311)

Even though the LT3753 $INTV_{CC}$ pin is allowed to be over driven by as much as 15.4V, $SOUT_{MAX}$ level should be designed to not cause T_{SYNC} output to exceed the maximum ratings of the LT8311's SYNC pin.

Cost/Space reduction : If discontinuous conduction mode (DCM) operation is acceptable at light load, the LT8311 has a preactive mode which controls the synchronous MOSFETs without T_{SYNC}, C_{SYNC}, R_{SYNC} or the LT3753 timing resistors R_{TAS}, R_{TOS} (leave open).

Output Inductor Value

The choice of output inductor value L_{OUT} will depend on the amount of allowable ripple current. The inductor ripple current is given by:

$I_{L(RIPPLE)(P-P)}$

$= \Delta I_L = (V_{OUT}/(L_{OUT} \bullet f_{OSC})) \bullet (1 - (V_{OUT}/V_{IN})(N_P/N_S))$

The LT3753 allows very large ΔI_L values (low L_{OUT} values) without the worry of insufficient slope compensation—by allowing slope compensation to be programmed with an external resistor in series with the I_{SENSEP} pin (see Current Sensing and Programmable Slope Compensation).

Larger ΔI_L will allow lower L_{OUT}, reducing component size, but will also cause higher output voltage ripple and core losses. For LT3753 applications, ΔI_L is typically chosen to be 40% of $I_{OUT(MAX)}$.

Output Capacitor Selection

The choice of output capacitor value is dependent on output voltage ripple requirements given by :

$\Delta V_{OUT} \approx \Delta I_L(ESR + (1/(8 \bullet f_{OSC} \bullet C_{OUT}))$

where,

ΔI_L = output inductor ripple current $I_{L(RIPPLE)(P-P)}$

ESR = effective series resistance (of C_{OUT})

f_{OSC} = switching frequency

C_{OUT} = output capacitance

This gives:

$C_{OUT} = \Delta I_L/(8 \bullet f_{OSC} \bullet (\Delta V_{OUT} - \Delta I_L \bullet ESR))$

Typically C_{OUT} is made up of a low ESR ceramic capacitor(s) to minimize ΔV_{OUT}. Additional bulk capacitance is added in the form of electrolytic capacitors to minimize output voltage excursions during load steps.

Input Capacitor Selection

The active clamp forward converter demands pulses of current from the input due to primary winding current and magnetizing current. The input capacitor is required to provide high frequency filtering to achieve an input voltage as close as possible to a pure DC source with low ripple voltage. For low impedance input sources and medium to low voltage input levels, a simple ceramic capacitor with low ESR should suffice. It should be rated to operate at a worst case RMS input current of :

$I_{CIN(RMS)} = (N_S/N_P)\ I_{OUT(MAX)}/2$

A small 1µF bypass capacitor should also be placed close to the IC between V_{IN} and GND.

As input voltage levels increase, any use of bulk capacitance to minimize input ripple can impact on solution size and cost. In addition, inputs with higher source impedance will cause an increase in voltage ripple. In these applications it is recommended to include an LC input filter. The output impedance of the input filter should remain below the negative input impedance of the DC/DC forward converter.

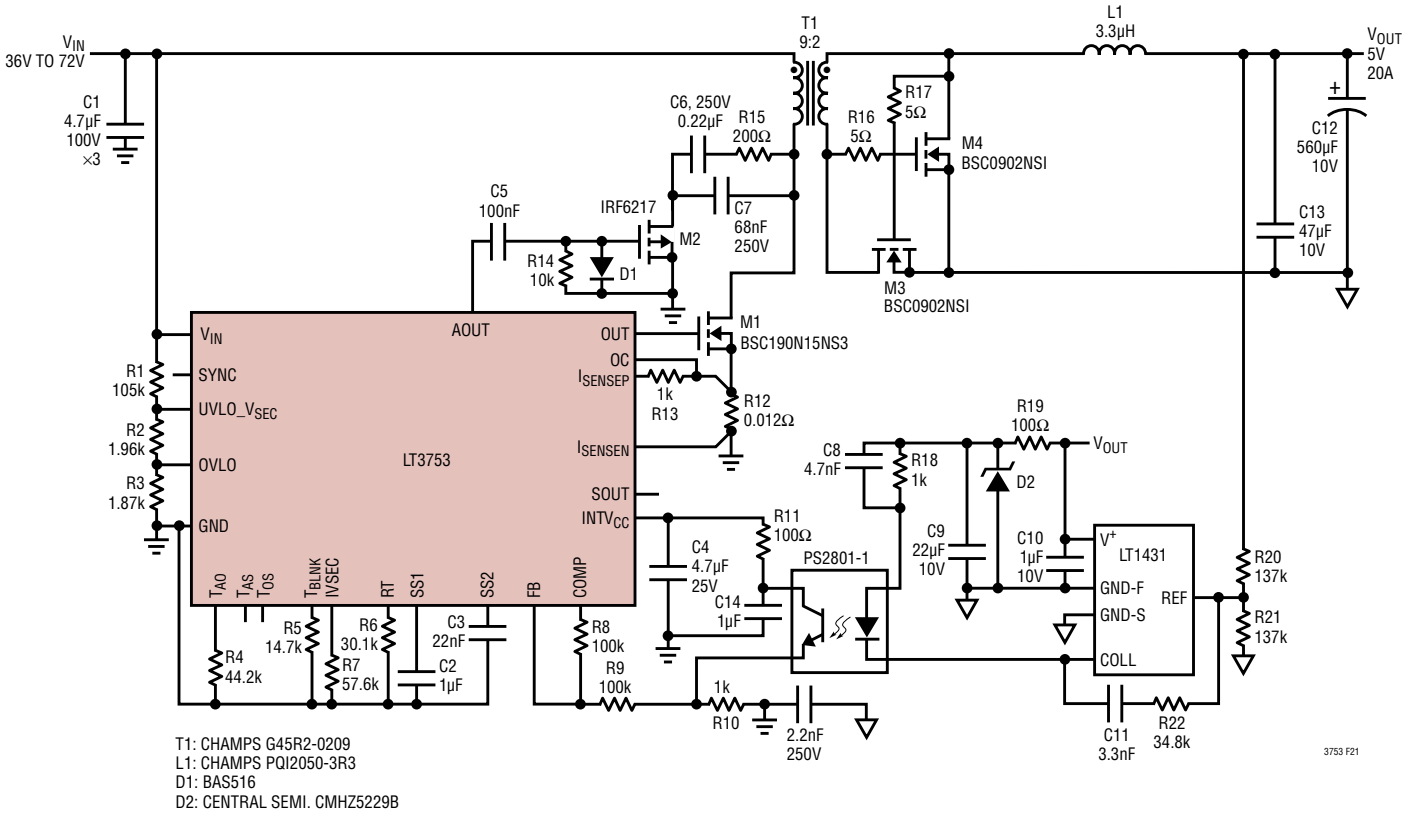
APPLICATIONS INFORMATION

PCB Layout/Thermal Guidelines

For proper operation, PCB layout must be given special attention. Critical programming signals must be able to coexist with high dv/dt signals. Compact layout can be achieved but not at the cost of poor thermal management. The following guidelines should be followed to approach optimal performance.

1. Ensure that a local bypass capacitor is used (and placed as close as possible) between V_{IN} and GND for the controller IC(s).
2. The critical programming resistors for timing (pins T_{AO}, T_{AS}, T_{OS}, T_{BLNK}, IVSEC and RT) must use short traces to each pin. Each resistor should also use a short trace to connect to a single ground bus specifically connected to pin 18 of the IC (GND).
3. The current sense resistor for the forward converter must use short Kelvin connections to the I_{SENSEP} and I_{SENSEN} pins.
4. High dv/dt lines should be kept away from all timing resistors, current sense inputs, COMP pin, UVLO_VSEC/OVLO pins and the FB trace.
5. Gate driver traces (AOUT, SOUT, OUT) should be kept as short as possible.
6. When working with high power components, multiple parallel components are the best method for spreading out power dissipation and minimizing temperature rise. In particular, multiple copper layers connected by vias should be used to sink heat away from each power MOSFET.
7. Keep high switching current PGND paths away from signal ground. Also minimize trace lengths for those high current switching paths to minimize parasitic inductance.

APPLICATIONS INFORMATION



Efficiency vs Load Current

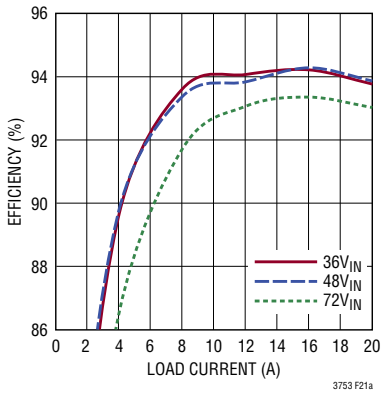
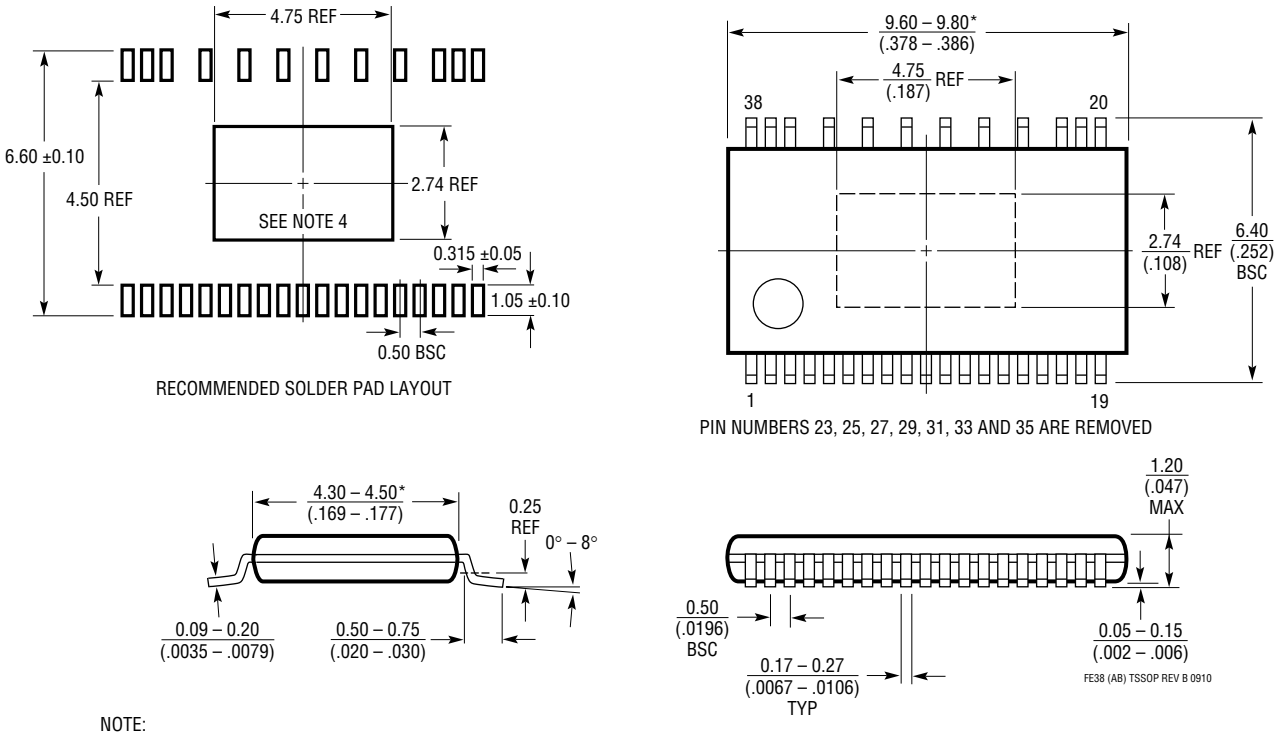


Figure 21. 36V to 72V, 5V/20A 100W Active Clamp Isolated Forward Converter

PACKAGE DESCRIPTION

FE Package
Package Variation: FE38 (31)
38-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1865 Rev B)
Exposed Pad Variation AB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/15	Changed SS1 and SS2 ABS MAX ratings	3
		Changed AOUT and SOUT driver times	5
		Clarified SS2 pin (Soft-Start: Comp Pin) conditions	6
B	08/19	Corrected Active Clamp Capacitor Equation	23
C	06/20	Corrected UVLO Typo	3