20V 20A Monolithic Buck Converter with Ultralow DCR Sensing

FEATURES

- **Wide V_{IN} Range: 4.5V to 20V**
- **Optimized for Low Duty Cycle Applications**
- **High Efficiency: Up to 95%**
- **LTC Proprietary Current Mode Architecture**
- **High Current Parallel Operation**
- **Ultralow DCR Current Sensing with Temperature Compensation**
- **Programmable Output Current Limit**
- High Speed Differential Remote Sense Amplifier
- ±0.5% Output Voltage Regulation Accuracy
- Output Short-Circuit Protection with Soft Recovery
- Programmable Soft-Start, Tracking
- Programmable Fixed Frequency: 250kHz to 770kHz
- $EXTV_{CC}$ for Reduced Power Dissipation
- Fault Indicator for Output UV/OV Conditions
- 6.25mm × 7.5mm × 2.22mm BGA Package

APPLICATIONS

- DSP, FPGA, ASIC Reference Designs
- Telecom/Datacom Systems
- Distributed High Power Density Systems

DESCRIPTION

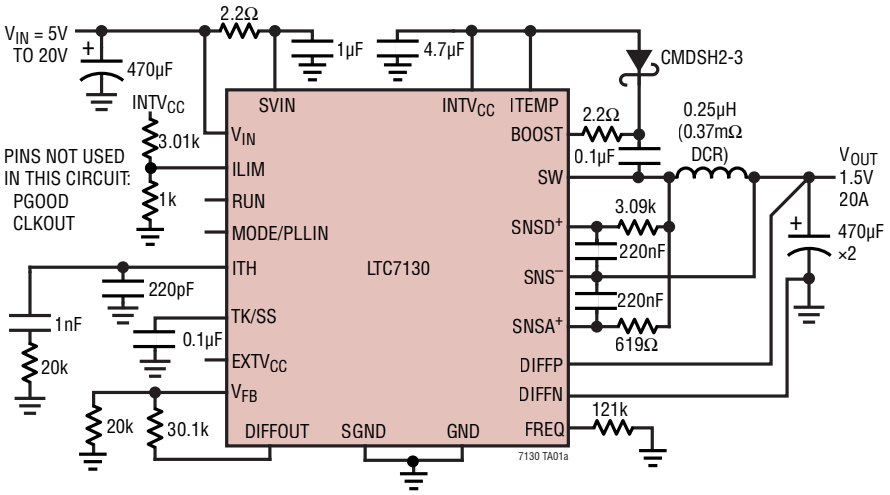
The LTC®7130 is a current mode synchronous step-down monolithic converter that can deliver up to 20A continuous load current. It employs a unique architecture which enhances the signal-to-noise ratio of the current sense signal, allowing the use of a very low DC resistance power inductor to maximize efficiency in high current applications. This feature also reduces the switching jitter commonly found in low DCR applications. The LTC7130 also includes a high speed differential remote sense amplifier and a programmable current sense limit that can be selected from 10mV to 30mV to set the output current limit up to 20A. In addition, the DCR temperature compensation feature limits the maximum output current precisely over temperature.

The LTC7130 also features a precise 0.6V reference with a guaranteed limit of ±0.5% that provides an accurate output voltage. A 5V to 20V input voltage range supports a wide variety of bus voltages and various types of batteries.

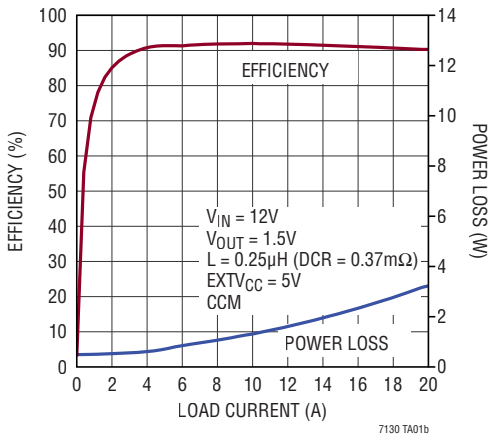
The LTC7130 is offered in a compact and low profile BGA package available with SnPb/RoHS compliant terminal finishes.

TYPICAL APPLICATION

High Efficiency, 1.5V/20A Step-Down Converter with Very Low DCR Sensing



Efficiency vs Load Current

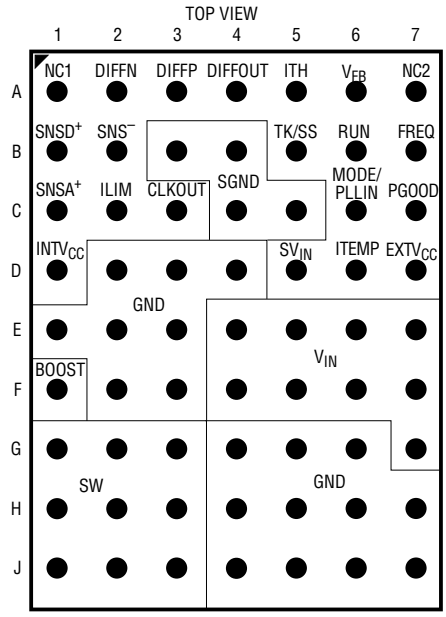


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage ..... –0.3V to 20V
$EXTV_{CC}$, RUN, PGOOD ..... –0.3V to 6V
$SNSD^+$, $SNSA^+$, SNS^- Voltages ..... –0.3V to $INTV_{CC}$
MODE/PLLIN, ILIM, TK/SS, FREQ ..... –0.3V to $INTV_{CC}$
DIFFP, DIFFN ..... –0.3V to $INTV_{CC}$
ITEMP, ITH, V_{FB} Voltages ..... –0.3V to $INTV_{CC}$
Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Peak Solder Reflow Body Temperature ..... 260°C

PIN CONFIGURATION



BGA PACKAGE
63-PIN (6.25mm × 7.5mm × 2.22mm)

T_{JMAX} = 125°C, θ_{JA} = 21°C/W, θ_{JC} = 10°C/W
θ_{JA} DERIVED FROM LTC7130 DEMO BOARD, Weight = 0.24g

ORDER INFORMATION

(http://www.linear.com/product/LTC7130#orderinfo)

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTC7130EY#PBF	SAC305 (RoHS)	LTC7130	e1	BGA	3	–40°C to 125°C
LTC7130IY#PBF	SAC305 (RoHS)	LTC7130	e1	BGA	3	–40°C to 125°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Terminal Finish Part Marking: www.linear.com/leadfree
- This product is not recommended for second side reflow. For more information, go to www.linear.com/BGA-assy
- Recommended BGA PCB Assembly and Manufacturing Procedures: www.linear.com/BGA-assy
- BGA Package and Tray Drawings: www.linear.com/packaging
- This product is moisture sensitive. For more information, go to: www.linear.com/BGA-assy

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, V_{RUN} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops							
V_{IN}	Input Voltage Range	(Note 3)		4.5		20	V
V_{OUT}	Output Voltage Range	with Diffamp Low DCR Sensing without Diffamp and No Low DCR Sensing		0.6 0.6		3.5 5.5	V V
V_{FB}	Regulated Feedback Voltage	Current ITH Voltage = 1.2V (Note 4) –40°C to 85°C –40°C to 125°C	 ● ●	 0.597 0.5955	 0.6 0.6	 0.603 0.6045	 V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, V_{RUN} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{FB}	Feedback Current	(Note 4)			–15	–50	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{IN} = 4.5V to 20V (Note 4)			0.002	0.02	%
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop; ΔITH Voltage = 1.2V to 0.7V Measured in Servo Loop; ΔITH Voltage = 1.2V to 1.6V	 ● ●		 0.01 0.01	 0.1 0.1	 % %
g_m	Error Amplifier (EA) Transconductance	ITH =1.2V, Sink/Source 5µA (Note 4)			2		mmho
I_Q	Input DC Supply Current Normal Mode Shutdown	(Note 5) V_{RUN} = 0V			 3.8 30	 50	 mA µA
UVLO	Undervoltage Lockout	V_{INTVCC} Ramping Down		3.4	3.75	4.1	V
$UVLO_{HYS}$	UVLO Hysteresis Voltage				0.5		V
V_{FBOVL}	Feedback Overvoltage Lockout	Measured at V_{FB}	●	0.64	0.66	0.68	V
I_{SNSD+}	$SNSD^+$ Pin Bias Current	V_{SNSD+} = 3.3V			30	100	nA
I_{SNSA+}	$SNSA^+$ Pin Bias Current	V_{SNSA+} = 3.3V			1	2	µA
A_{VT_SNS}	Total Sense Signal Gain to Current Comparator				5		V/V
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	–40°C to 125°C $V_{SNS–}$ = 1.8V, I_{LIM} = 0V I_{LIM} = 1/4V_{INTVCC} I_{LIM} = 1/2V_{INTVCC} or Float I_{LIM} = 3/4V_{INTVCC} I_{LIM} = V_{INTVCC}	 ● ● ● ● ●	 8.8 14 19 23.5 28.3	 10 15 20 25 30	 11.2 16 21 26.5 31.7	 mV mV mV mV mV
I_{TEMP}	DCR Temperature Compensation Current	V_{ITEMP} = 0.3V	●	9	10	11	µA
$I_{TK/SS}$	Soft-Start Charge Current	$V_{TK/SS}$ = 0V	●	1.0	1.25	1.5	µA
V_{RUN}	RUN Pin on Threshold Voltage	V_{RUN} Rising	●	1.1	1.22	1.35	V
$V_{RUN(HYS)}$	RUN Pin on Hysteresis Voltage				80		mV
$t_{ON(MIN)}$	Minimum On-Time	(Note 6)			90		ns
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 20V		5.25	5.5	5.75	V
	Load Regulation	I_{INTVCC} = 0mA to 20mA			0.5	2	%
V_{EXTVCC}	External V_{CC} Switchover Voltage	$EXTV_{CC}$ Ramping Positive		4.5	4.7		V
	$EXTV_{CC}$ Voltage Drop	I_{EXTVCC} = 20mA, V_{EXTVCC} = 5.5V			40	100	mV
	$EXTV_{CC}$ Hysteresis				250		mV
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	V_{FREQ} = 1.2V		450	500	550	kHz
f_{LOW}	Lowest Frequency	V_{FREQ} = 0.4V		225	250	275	kHz
f_{HIGH}	Highest Frequency	V_{FREQ} > 2.4V		700	770	850	kHz
$R_{MODE/PLLIN}$	MODE/PLLIN Input Resistance				250		kΩ
I_{FREQ}	Frequency Setting Current			9	10	11	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, V_{RUN} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CLKOUT	Phase Relative to the Oscillator Clock				180		Deg
$CLKOUT_{HI}$	Clock Output High Voltage	V_{INTVCC} = 5.5V		4.5	5.5		V
$CLKOUT_{LO}$	Clock Output Low Voltage				0	0.2	V
PGOOD Output							
V_{PGDLO}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGD}	PGOOD Leakage Current	V_{PGOOD} = 5.5V				2	µA
V_{PGD}	PGOOD Trip	V_{FB} with Respect to Set Output Voltage V_{FB} Going Negative V_{FB} Going Positive			 –10 10		 % %
Differential Amplifier							
A_V	Gain	–40°C to 125°C	●	0.997	1	1.003	V/V
R_{IN}	Input Resistance	Measured at DIFFP Input			80		kΩ
V_{OS}	Input Offset Voltage	V_{DIFFP} = 1.5V, $V_{DIFFOUT}$ = 100µA				2	mV
PSRR	Power Supply Rejection Ratio	5V < V_{IN} < 20V (Note 7)			90		dB
I_{OUT}	Maximum Sourcing Output Current			1.5	2		mA
V_{OUT}	Maximum Output Voltage	V_{INTVCC} = 5.5V, $I_{DIFFOUT}$ = 300µA		V_{INTVCC} – 1.4	V_{INTVCC} – 1.1		V
GBW	Gain-Bandwidth Product	(Note 7)			3		MHz
SR	Slew Rate	(Note 7)			2		V/µs
$R_{DS(ON)}$							
R_{TOP}	Top Power NMOS On-Resistance				7.3		mΩ
R_{BOTTOM}	Bottom Power NMOS On-Resistance				2.1		mΩ

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7130 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7130E is guaranteed to meet performance specifications from 0°C to 85°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7130I is guaranteed to meet performance specifications over the full –40°C to 125°C operating junction temperature range. The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the package thermal impedance and other environmental factors. The thermal derating curves are based on the LTC7130 demo board.

Note 3: When 4.5V ≤ V_{IN} ≤ 5.5V, $INTV_{CC}$ must be tied to V_{IN}. Guaranteed by design.

Note 4: The LTC7130 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}.

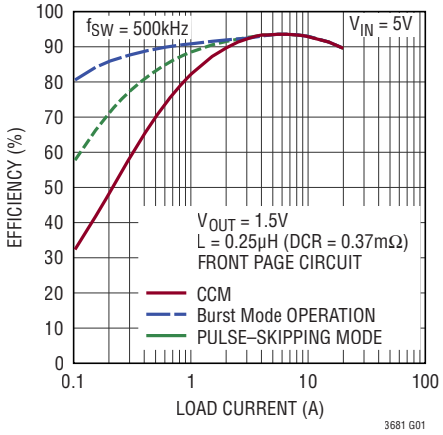
Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 6: The minimum on-time condition corresponds to the on inductor peak-to-peak ripple current ≥40% of I_{MAX} (see Minimum On-Time Considerations in the Applications Information section).

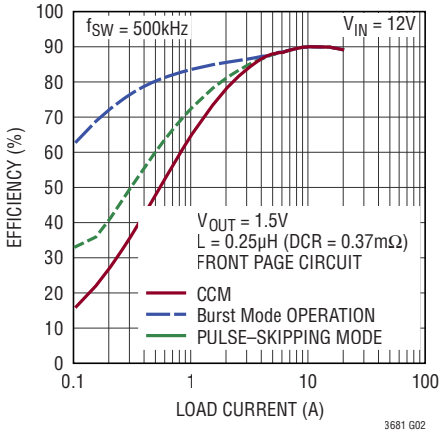
Note 7: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

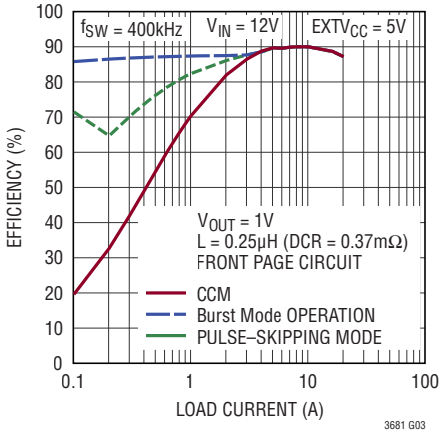
Efficiency vs Load Current and Mode



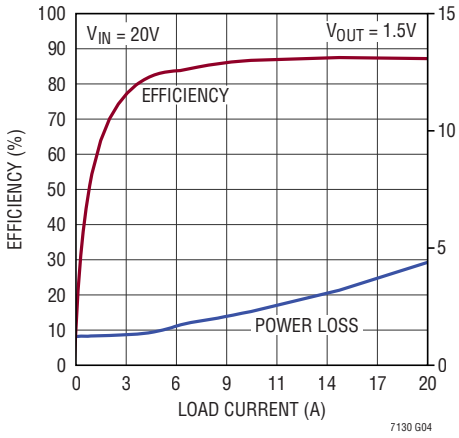
Efficiency vs Load Current and Mode



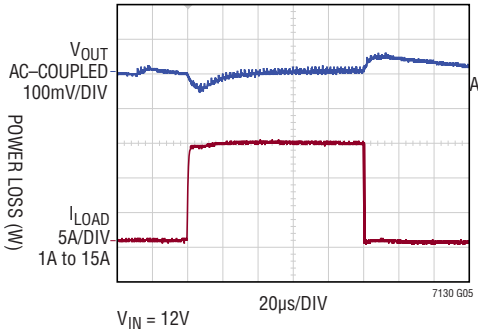
Efficiency vs Load Current and Mode



Efficiency and Power Loss vs Load Current

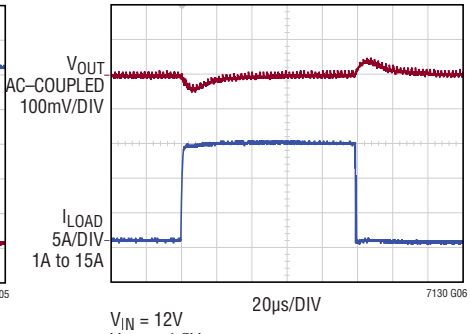


Load Step (Burst Mode® Operation)



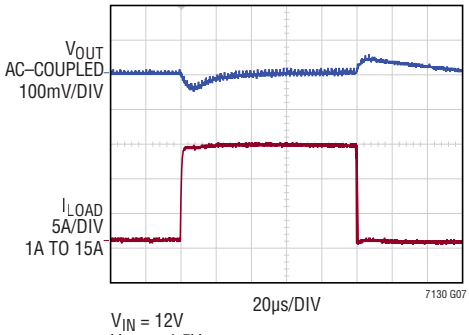
VIN = 12V
VOUT = 1.5V
FRONT PAGE CIRCUIT

Load Step (Continuous Conduction Mode)



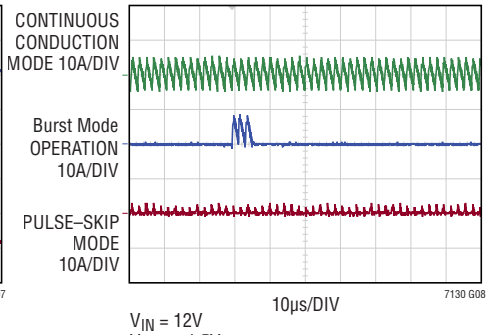
VIN = 12V
VOUT = 1.5V
FRONT PAGE CIRCUIT

Load Step (Pulse-Skipping Mode)



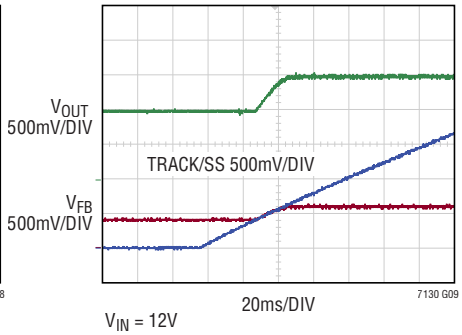
VIN = 12V
VOUT = 1.5V
FRONT PAGE CIRCUIT

Inductor Current at Light Load



VIN = 12V
VOUT = 1.5V
LOAD = 300mA

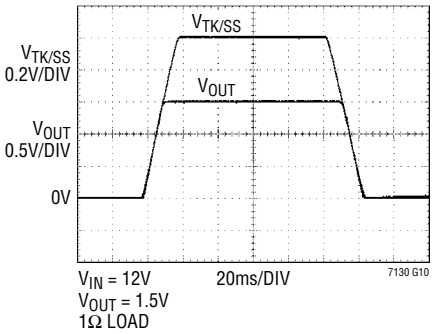
Prebiased Output at 1V



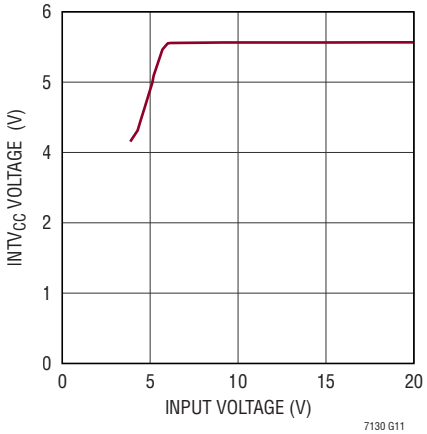
VIN = 12V
VOUT = 1.5V

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

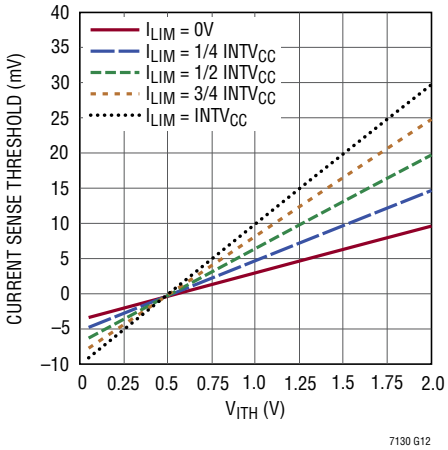
Tracking Up and Down with TK/SS External Ramp



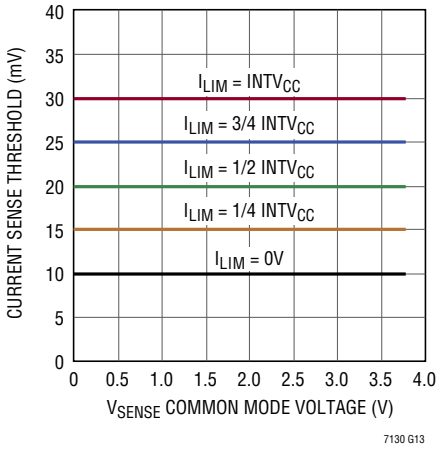
INTVCC Line Regulation



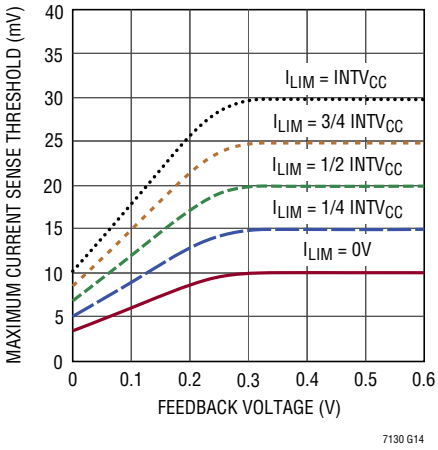
Current Sense Threshold vs ITH Voltage



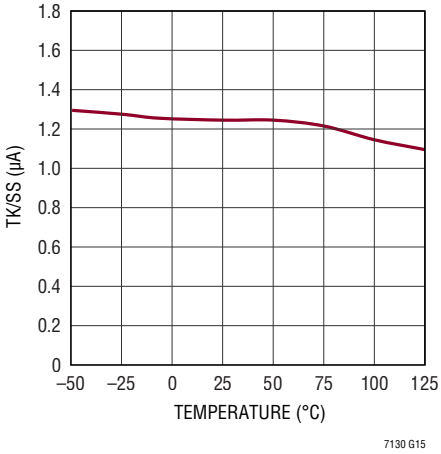
Maximum Current Sense Threshold vs Common Mode Voltage



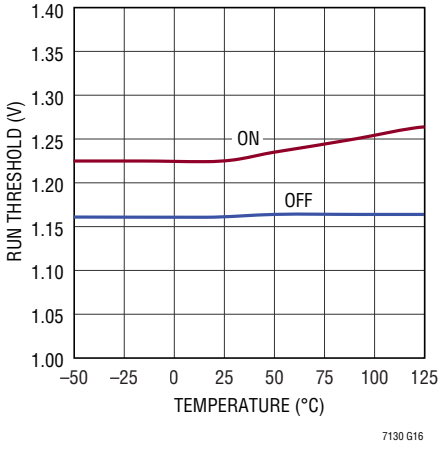
Maximum Current Sense Threshold Voltage vs Feedback Voltage (Current Foldback)



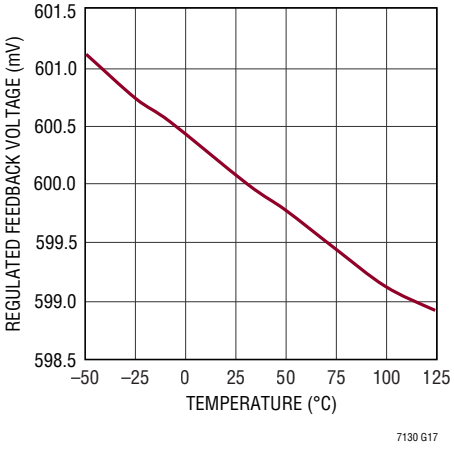
TK/SS Pull-Up Current vs Temperature



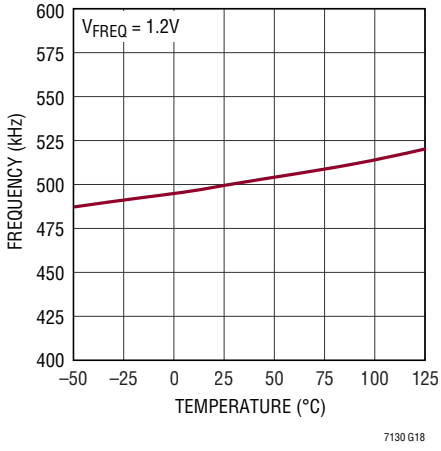
Shutdown (RUN) Threshold vs Temperature



Regulated Feedback Voltage vs Temperature

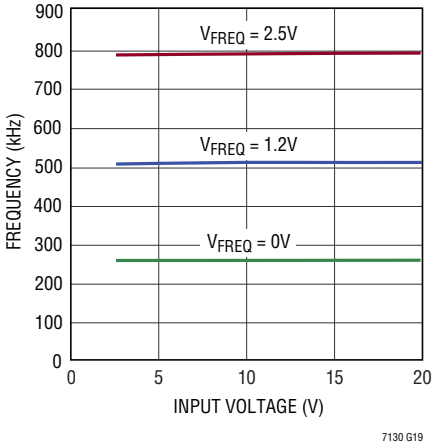


Oscillator Frequency vs Temperature

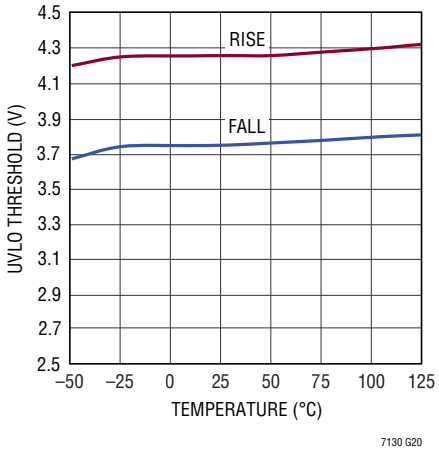


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

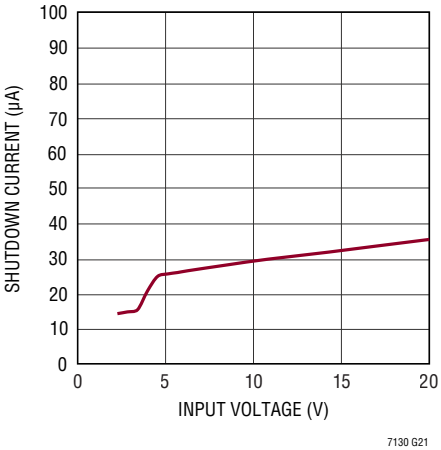
Oscillator Frequency vs Input Voltage



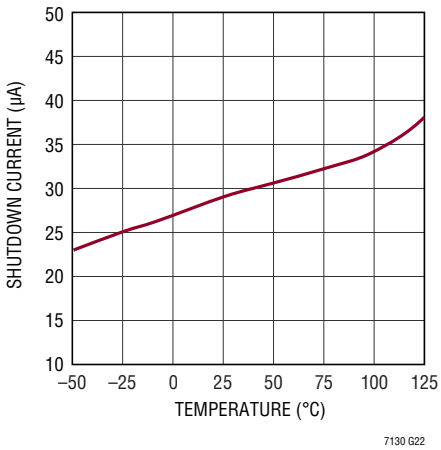
Undervoltage Lockout Threshold ($INTV_{CC}$) vs Temperature



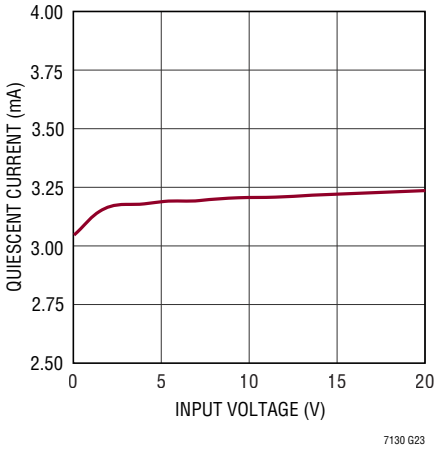
Shutdown Current vs Input Voltage



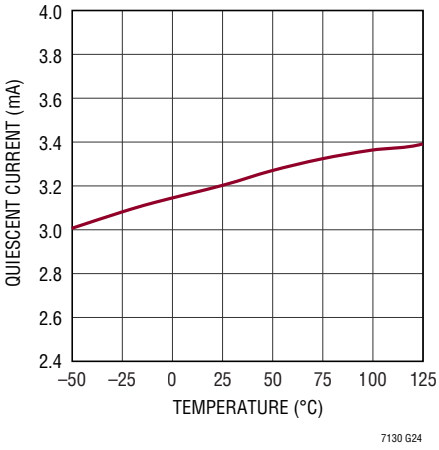
Shutdown Current vs Temperature



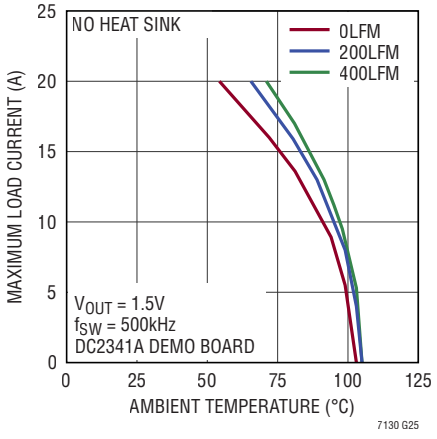
Input Quiescent Current vs Input Voltage without $EXTV_{CC}$



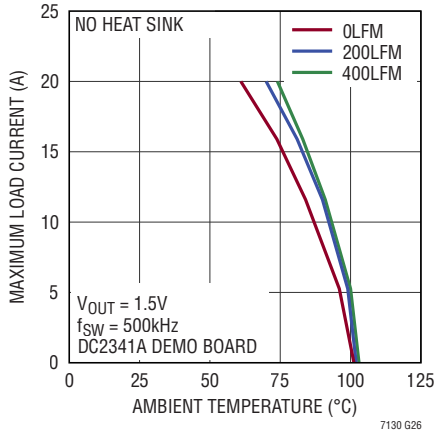
Quiescent Current vs Temperature without $EXTV_{CC}$



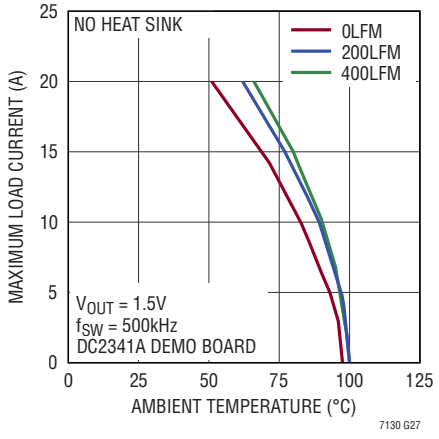
Thermal Derating V_{IN} = 5V



Thermal Derating V_{IN} = 12V



Thermal Derating V_{IN} = 20V



PIN FUNCTIONS

FREQ (B7): Oscillator Frequency Control Input. A 10µA current source flows out of this pin. Connecting a resistor between this pin and ground sets a DC voltage which in turn programs the oscillator frequency. Alternatively, this pin can be driven with a DC voltage to vary the frequency of the internal oscillator.

RUN (B6): Run Control Input. A voltage above 1.22V turns on the IC. Pulling this pin below 1.1V causes the IC to shut down. There is a 1µA pull-up current for the pin. Once the RUN pin rises above 1.22V, an additional 4.5µA pull-up current is added to the pin.

TK/SS (B5): Output Voltage Tracking and Soft-Start Input. An internal soft-start current of 1.25µA charges the external soft-start capacitor connected to this pin.

ITH (A5): Current Control Threshold and Error Amplifier Compensation Pin. The current comparator tripping threshold is proportional with this voltage.

V_{FB} (A6): Error Amplifier Feedback Input. This pin receives the remotely sensed feedback voltage to set the output voltage through an external resistive divider connected to the DIFFOUT pin or the output.

DIFFOUT (A4): Output of Remote Sensing Differential Amplifier. Connect this pin to V_{FB} through a resistive divider to set the desired output voltage.

DIFFN (A2): Negative Input of Remote Sensing Differential Amplifier. Connect this pin close to the ground of the output load.

DIFFP (A3): Positive Input of Remote Sensing Differential Amplifier. Connect this pin close to the output load.

$SNSD^+$ (B1): DC Current Sense Comparator Input. The (+) output to the DC current. Comparator is normally connected to a DC current sensing network with a time constant that matches the bandwidth, L/DCR, of the inductor.

SNS^- (B2): Negative Current Sense Input. This negative input of the current comparator is to be connected to the output.

$SNSA^+$ (C1): AC Current Sense Comparator Input. The (+) output to the AC current comparator is normally connected to a DCR sensing network. When combined with the $SNSD^+$ pin, the DCR sensing network can be skewed to increase the AC ripple voltage by a factor of 5.

ILIM (C2): Current Comparator Sense Voltage Limit. Apply a DC voltage to set the maximum current sense threshold for the current comparator.

CLKOUT (C3): Clock Output Pin. The CLKOUT signal is 180° out of phase to the rising edge of the IC internal clock.

GND (D2, D3, D4, E1, E2, E3, F2, F3, G4, G5, G6, H4, H5, H6, H7, J4, J5, J6, J7): Power Ground. Connect this pin closely to the (–) terminal of CV_{CC} and the (–) terminal of C_{IN}.

SW (G1, G2, G3, H1, H2, H3, J1, J2, J3): Switch Node Connection. Connect this pin to the output filter inductor, bottom N-channel MOSFET drain and top N-channel MOSFET source. Voltage swing at these pins is from a Schottky diode (external) voltage drop below ground to V_{IN}.

BOOST (F1): Boosted Top Gate Driver Supply. The (+) terminal of the bootstrap capacitor connects to this pin. This pin swings from a diode voltage drop below $INTV_{CC}$ up to V_{IN} + $INTV_{CC}$.

$INTV_{CC}$ (D1): Internal 5.5V Regulator Output. The internal control circuits are powered from this voltage. Decouple this pin to PGND with a 4.7µF low ESR tantalum or ceramic capacitor.

PIN FUNCTIONS

SV_{IN} (D5): Main Input Supply. Decouple this pin to PGND with a capacitor (0.1µF to 1µF). For applications where the main input power is 5V, tie the SV_{IN} and $INTV_{CC}$ pins together.

V_{IN} (E4, E5, E6, E7, F4, F5, F6, F7, G7): Main Input Supply. These pins connect to the drain of the internal power MOSFETs. Decouple this pin to GND with the input capacitance C_{IN}.

$EXTV_{CC}$ (D7): External Supply Voltage Input. Whenever an external voltage supply greater than 4.7V is connected to this pin, an internal switch will close and bypass the internal low dropout regulator, and the external supply will power the IC. Do not exceed 6V on this pin and ensure $V_{IN} > V_{EXTVCC}$ at all times.

ITEMP (D6): Temperature DCR Compensation Input. Connect to a NTC (negative tempco) resistor placed near the output inductor to compensate for its DCR change over temperature. Floating this pin or tying it to $INTV_{CC}$ disables the DCR temperature compensation function.

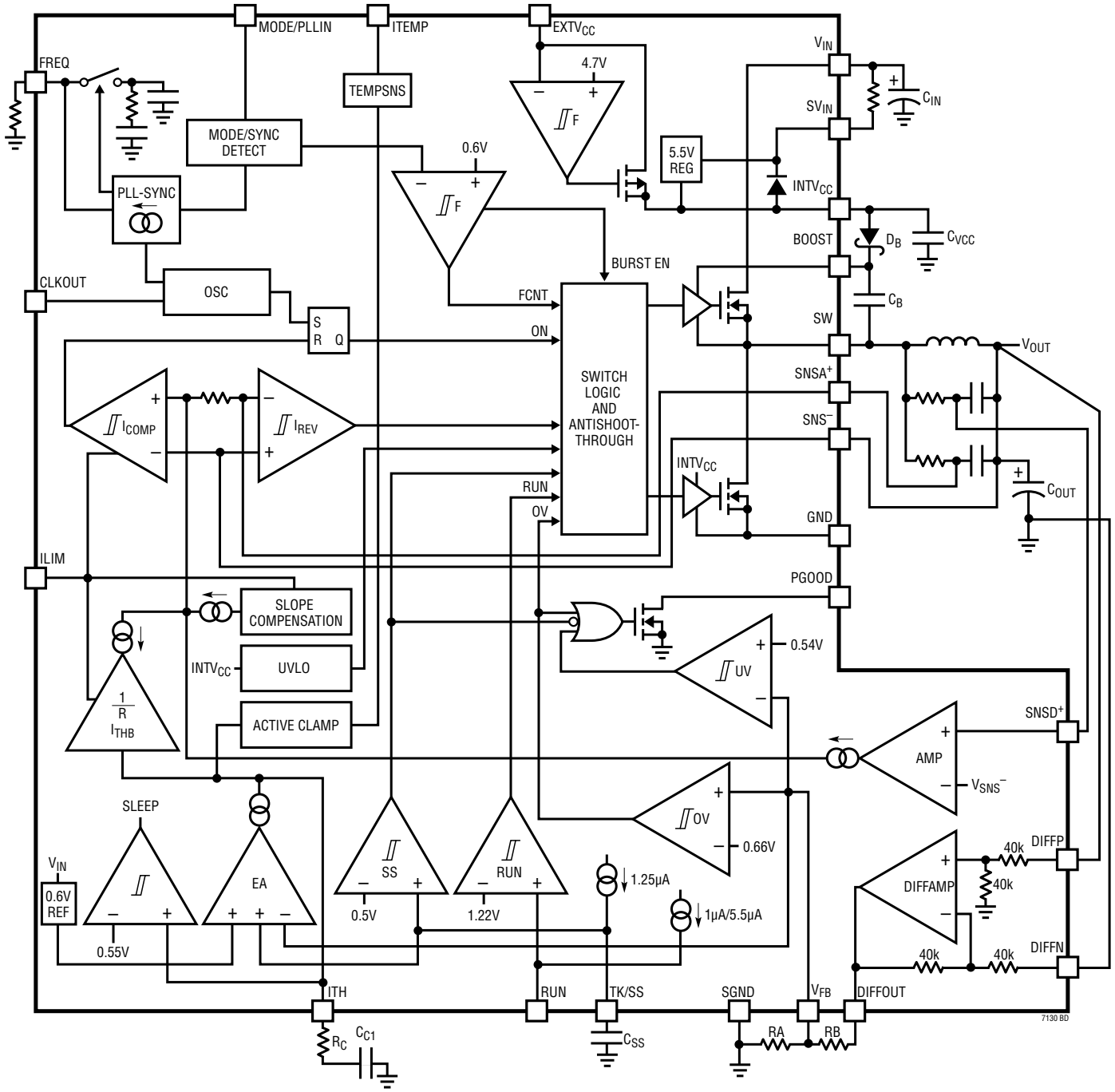
PGOOD (C7): Power Good Indicator Output. Open-drain logic out that is pulled to ground when the output exceeds the 10% regulation window, after the internal 20µs power bad mask timer expires.

MODE/PLLIN (C6): Mode Operation or External Clock Synchronization. Connect this pin to SGND to set the continuous mode of operation. Connect to $INTV_{CC}$ to enable pulse-skipping mode of operation. Leaving the pin floating will enable Burst Mode operation. A clock signal applied to the pin will force the controller into continuous mode of operation and synchronizes the internal oscillator.

SGND (B3, B4, C4, C5): Signal Ground. This is the ground of the controller. Connect compensation components and output setting resistors to this ground.

NC (A1, A7): Do not connect. These pins are not connected to anything internally.

FUNCTIONAL BLOCK DIAGRAM



OPERATION

Main Control Loop

The LTC7130 uses a LTC proprietary current sensing, current mode step-down architecture. During normal operation, the top MOSFET is turned on every cycle when the oscillator sets the RS latch, and turned off when the main current comparator, I_{CMP}, resets the RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier, EA. The remote sense amplifier (diffamp) produces a signal equal to the differential voltage sensed across the output capacitor divided down by the feedback divider and re-references it to the local IC ground reference. The V_{FB} pin receives this feedback signal and compares it to the internal 0.6V reference. When the load current increases, it causes a slight decrease in the V_{FB} pin voltage relative to the 0.6V reference, which in turn causes the ITH voltage to increase until the inductor's average current equals the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the reverse current comparator, I_{REV}, or the beginning of the next cycle.

The main control loop is shut down by pulling the RUN pin low. Releasing RUN allows an internal 1.0µA current source to pull up the RUN pin. When the RUN pin reaches 1.22V, the main control loop is enabled and the IC is powered up. When the RUN pin is low, all functions are kept in a controlled state.

Sensing Signal of Very Low DCR

The LTC7130 employs a unique architecture to enhance the signal-to-noise ratio that enables it to operate with a small sense signal of a very low value inductor DCR, 1mΩ or less, to improve power efficiency, and reduce jitter due to the switching noise which could corrupt the signal. The LTC7130 comprises two positive sense pins, $SNSD^+$ and $SNSA^+$, to acquire signals and processes them internally to provide the response as with a DCR sense signal that has a 14dB signal-to-noise ratio improvement. In the meantime, the current limit threshold is still a function of the inductor peak current and its DCR value, and can be accurately set from 10mV to 30mV in a 5mV steps with the ILIM pin. The filter time constant, R1 • C1, of the $SNSD^+$ should match the L/DCR of the output inductor, while the filter at $SNSA^+$ should have a bandwidth of five times larger than $SNSD^+$, R2 • C2 equals R1 • C1/5 (see Figure 3).

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is tied to a voltage less than 4.7V, an internal 5.5V linear regulator supplies $INTV_{CC}$ power from V_{IN}. Ground $EXTV_{CC}$ if it is not used. If $EXTV_{CC}$ is taken above 4.7V, the 5.5V regulator is turned off and an internal switch is turned on connecting $EXTV_{CC}$ to $INTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as a switching regulator output. The top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during the off cycle through an external diode when the top MOSFET turns off. If the input voltage, V_{IN}, decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one-twelfth of the clock period plus 100ns every third cycle to allow C_B to recharge (note 7). However, it is recommended that a load be present or the IC operates at low frequency during the dropout transition to ensure C_B is recharged.

Internal Soft-Start

By default, the start-up of the output voltage is normally controlled by an internal soft-start ramp. The internal soft-start ramp connects to the noninverting input of the error amplifier. The V_{FB} pin is regulated to the lower of the error amplifier's three noninverting inputs (the internal soft-start ramp, the TK/SS pin or the internal 600mV reference). As the ramp voltage rises from 0V to 0.6V over approximately 600µs, the output voltage rises smoothly from its prebiased value to its final set value.

Certain applications can result in the start-up of the converter into a non-zero load voltage, where residual charge is stored on the output capacitor at the onset of converter switching. In order to prevent the output from discharging under these conditions, the bottom MOSFET is disabled until soft-start is greater than V_{FB}.

OPERATION

Shutdown and Start-Up (RUN and TK/SS Pins)

The LTC7130 can be shut down using the RUN pin. Pulling the RUN pin below 1.1V shuts down the main control loop for the controller and most internal circuits, including the $INTV_{CC}$ regulator. Releasing the RUN pin allows an internal 1.0µA current to pull up the pin and enable the controller. Alternatively, the RUN pin may be externally pulled up or driven directly by logic. Be careful not to exceed the absolute maximum rating of 6V on this pin. The start-up of the controller's output voltage, V_{OUT}, is controlled by the voltage on the TK/SS pin, if the internal soft-start has expired. When the voltage on the TK/SS pin is less than the 0.6V internal reference, the LTC7130 regulates the V_{FB} voltage to the TK/SS pin voltage instead of the 0.6V reference. This allows the TK/SS pin to be used to program a soft-start by connecting an external capacitor from the TK/SS pin to SGND. An internal 1.25µA pull-up current charges this capacitor, creating a voltage ramp on the TK/SS pin. As the TK/SS voltage rises linearly from 0V to 0.6V (and beyond), the output voltage, V_{OUT}, rises smoothly from zero to its final value. Alternatively, the TK/SS pin can be used to cause the start-up of V_{OUT} to *track* that of another supply. Typically, this requires connecting to the TK/SS pin an external resistor divider from the other supply to ground (see the Applications Information section). When the RUN pin is pulled low to disable the controller, or when $INTV_{CC}$ drops below its undervoltage lockout threshold of 3.75V, the TK/SS pin is pulled low by an internal MOSFET. When in undervoltage lockout, the controller is disabled and the MOSFETs are held off.

Light Load Current Operation (Burst Mode Operation, Pulse-Skipping or Continuous Conduction)

The LTC7130 can be enabled to enter high efficiency Burst Mode operation, constant-frequency pulse-skipping mode or forced continuous conduction mode. To select forced continuous operation, tie the MODE/PLLIN pin to SGND. To select pulse-skipping mode of operation, tie the MODE/PLLIN pin to $INTV_{CC}$. To select Burst Mode operation, float the MODE/PLLIN pin. When the controller is enabled for Burst Mode operation, the peak current in the inductor is set to approximately one-third of the maximum sense voltage even though the voltage on the ITH pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier, EA, will decrease the voltage on the ITH pin. When the ITH voltage drops below 0.5V, the internal sleep signal goes high (enabling "sleep" mode) and both MOSFETs are turned off.

In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the sleep signal goes low, and the controller resumes normal operation by turning on the top MOSFET on the next cycle of the internal oscillator. When the controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (I_{REV}) turns off the bottom MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous mode has the advantages of lower output ripple and less interference with audio circuitry.

When the MODE/PLLIN pin is connected to $INTV_{CC}$, the LTC7130 operates in PWM pulse skipping mode at light loads. At very light loads, the current comparator, I_{CMP}, may remain tripped for several cycles and force the top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

OPERATION

Frequency Selection and Phase-Locked Loop (FREQ and MODE/PLLIN Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

If the MODE/PLLIN pin is not being driven by an external clock source, the FREQ pin can be used to program the controller's operating frequency from 250kHz to 770kHz. There is a precision 10µA current flowing out of the FREQ pin so that the user can program the controller's switching frequency with a single resistor to SGND. A curve is provided later in the Applications Information section showing the relationship between the voltage on the FREQ pin and switching frequency.

A phase-locked loop (PLL) is available on the LTC7130 to synchronize the internal oscillator to an external clock source that is connected to the MODE/PLLIN pin. The PLL loop filter network is integrated inside the LTC7130. The phase-locked loop is capable of locking any frequency within the range of 250kHz to 770kHz. The frequency setting resistor should always be present to set the controller's initial switching frequency before locking to the external clock. The controller operates in forced continuous mode when it is synchronized.

Sensing the Output Voltage with a Differential Amplifier

The LTC7130 includes a low offset, high input impedance, unity-gain, high bandwidth differential amplifier for applications that require true remote sensing. Sensing the load across the load capacitors directly greatly benefits regulation in high current, low voltage applications, where board interconnection losses can be a significant portion of the total error budget. Connect DIFFP to the output load, and DIFFN to the load ground. See Figure 1.

The LTC7130 differential amplifier has a typical output slew rate of 2V/µs. The amplifier is configured for unity gain, meaning that the difference between DIFFP and DIFFN is translated to DIFFOUT, relative to SGND.

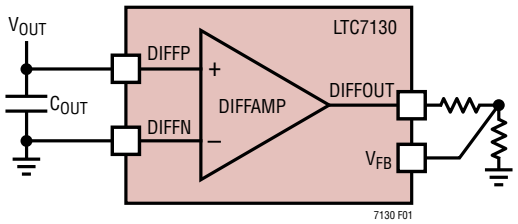


Figure 1. Differential Amplifier Connection

Care should be taken to route the DIFFP and DIFFN PCB traces parallel to each other all the way to the remote sensing points on the board. In addition, avoid routing these sensitive traces near any high speed switching nodes in the circuit. Ideally, the DIFFP and DIFFN traces should be shielded by a low impedance ground plane to maintain signal integrity. The maximum output voltage is limited to 3.5V when using the differential amplifier. If the differential amplifier is not used, tie the feedback divider directly across the output with its center point connected to V_{FB} and ground the SNSD+ pin. In this case the maximum supported V_{OUT} is 5V.

Power Good (PGOOD Pin)

The PGOOD pin is connected to the open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the V_{FB} pin voltage is not within ±10% of the 0.6V reference voltage. The PGOOD pin is also pulled low when the RUN pin is below 1.1V or when the LTC7130 is in the soft-start or tracking up phase. When the V_{FB} pin voltage is within the ±10% regulation window, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source of up to 6V. The PGOOD pin will flag power good immediately when the V_{FB} pin is within the regulation window. However, there is an internal 20µs power-bad mask when the V_{FB} goes out of the window.

Inductor DCR Sensing Temperature Compensation (ITEMP Pin)

Inductor DCR current sensing provides a lossless method of sensing the instantaneous current. Therefore, it can provide higher efficiency for applications with high output currents. However, the DCR of a copper inductor typically

OPERATION

has a positive temperature coefficient. As the temperature of the inductor rises, its DCR value increases. The current limit of the controller is therefore reduced.

The LTC7130 offers a method to counter this inaccuracy by allowing the user to place an NTC temperature sensing resistor near the inductor. A constant and precise 10µA current flows out of the ITEMP pin. By connecting a linearized NTC resistor network from the ITEMP pin to SGND, the maximum current sense threshold can be varied over temperature according to the following equation:

$$V_{SENSEMAX(ADJ)} = V_{SENSE(MAX)} \bullet \frac{2.2 - V_{ITEMP}}{1.5}$$

Where:

$V_{SENSEMAX(ADJ)}$ is the maximum adjusted current sense threshold.

$V_{SENSE(MAX)}$ is the maximum current sense threshold specified in the Electrical Characteristics table. It is typically 10mV, 15mV, 20mV, 25mV or 30mV, depending on the I_{LIM} pin's voltage.

V_{ITEMP} is the voltage of the ITEMP pin.

The valid voltage range for DCR temperature compensation on the ITEMP pin is between 0.7V to SGND with 0.7V or above being no DCR temperature correction.

An NTC resistor has a negative temperature coefficient, meaning that its resistance decreases as its temperature rises. The V_{ITEMP} voltage, therefore, decreases as the inductor's temperature increases, and in turn the $V_{SENSEMAX(ADJ)}$ will increase to compensate for the inductor's DCR temperature coefficient. The NTC resistor, however, is non-linear and the user can linearize its value by building a resistor network with regular resistors.

Output Overvoltage Protection

An overvoltage comparator, OV, guards against transient overshoots (>10%) as well as other more serious conditions that may overvoltage the output. In such cases, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Undervoltage Lockout

The LTC7130 has two functions that help protect the controller in case of undervoltage conditions. A precision UVLO comparator constantly monitors the $INTV_{CC}$ voltage to ensure that an adequate gate-drive voltage is present. It locks out the switching action when $INTV_{CC}$ is below 3.75V. To prevent oscillation when there is a disturbance on the $INTV_{CC}$, the UVLO comparator has 500mV of precision hysteresis.

Another way to detect an undervoltage condition is to monitor the V_{IN} supply. Because the RUN pin has a precision turn-on reference of 1.22V, one can use a resistor divider to V_{IN} to turn on the IC when V_{IN} is high enough. An extra 4.5µA of current flows out of the RUN pin once the RUN pin voltage passes 1.22V. The RUN comparator itself has about 80mV of hysteresis. One can program additional hysteresis for the RUN comparator by adjusting the values of the resistive divider. For accurate V_{IN} undervoltage detection, V_{IN} needs to be higher than 4.75V.

APPLICATIONS INFORMATION

The Typical Application on the first page of this data sheet is a basic LTC7130 application circuit. The LTC7130 is designed and optimized for use with a very low DCR value by utilizing a novel approach to reduce the noise sensitivity of the sensing signal by a factor of 14dB. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, as the DCR value drops below 1mΩ, the signal-to-noise ratio is low and current sensing is difficult. LTC7130 uses an LTC proprietary technique to solve this issue. In general, external component selection is driven by the load requirement, and begins with the DCR and inductor value. Next, input and output capacitors are selected.

Current Limit Programming

The ILIM pin is a 5-level logic input which sets the maximum current limit of the controller. When ILIM is either grounded, floated or tied to $INTV_{CC}$, the typical value for the maximum current sense threshold will be 10mV, 20mV or 30mV, respectively. Setting ILIM to one-fourth $INTV_{CC}$ and three-fourths $INTV_{CC}$ for maximum current sense thresholds of 15mV and 25mV.

Which setting should be used? For the best current limit accuracy, use the highest setting that is applicable to the output requirements.

SNSD+, SNSA+ and SNS– Pins

Compared to the conventional DCR sensing where there are only 2 sense pins, SENSE+ and SENSE– to sense across the DCR value of an inductor, the LTC7130 is designed to sense very low DCR value inductors in the sub milliohms range by adding an extra current sensing loop with SNSD+ pin. The SNSA+ and SNS– pins are the inputs to the current comparators, while the SNSD+ pin is the input of an internal amplifier.

All the positive sense pins that are connected to the current comparator or the amplifier are high impedance with input bias currents of less than 1µA, but there is also a resistance of about 300k from the SNS– pin to ground. The SNS– should be connected directly to VOUT. The SNSD+ pin connects to the filter that has a R1 • C1 time constant matched to L/DCR of the inductor. The SNSA+ pin is connected to the second filter with the time constant one-fifth that of R1 • C1. Care must be taken not to float these pins during normal operation. Filter components, especially capacitors, must be placed close to the LTC7130, and the sense lines should run close together to a Kelvin connection underneath the current sense element (Figure 2). Because the LTC7130 is designed to be used with a very low DCR value to sense inductor current, without proper care, the parasitic resistance, capacitance and inductance will degrade the current sense signal integrity, making the programmed current limit unpredictable. As shown in Figure 3, resistors R1 and R2 are placed close to the inductor and capacitors C1 and C2 are close to the IC pins to prevent noise coupling to the sense signal.

When the SNSD+ pin is in use for low DCR sensing, the maximum output voltage allowed is 3.5V due to the limitation of the internal amplifiers' inputs operating range. If low DCR sensing is not needed, the LTC7130 could also be used like any typical current mode controller by disabling the SNSD+ pin, shorting it to ground. RC filter can be used to sense the output inductor signal and connects to the SNSA+ pin. Its time constant, R • C, is equaled to L/DCR of the output inductor. In these applications, the current limit, $V_{SENSE(MAX)}$, will be five times larger for the specified I_{LIM}, and the operating voltage range of SNSA+ and SNS– is from 0V to 5V. Without using the internal differential amplifier, the output voltage of 5V can be generated as shown in the Typical Application section.

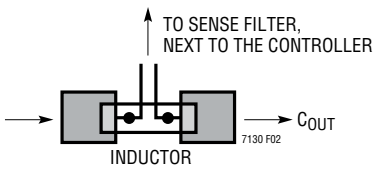


Figure 2. Sense Lines Placement with Inductor DCR

APPLICATIONS INFORMATION

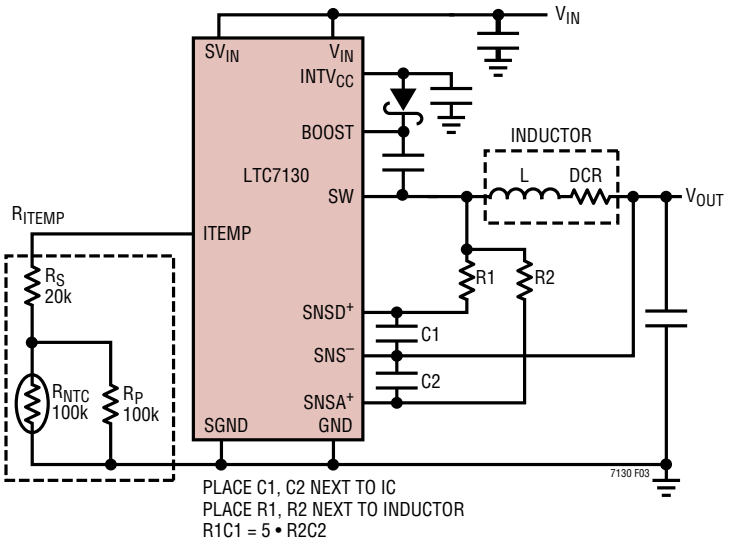


Figure 3. Inductor DCR Current Sensing

Inductor DCR Sensing

The LTC7130 is specifically designed for high load current applications requiring the highest possible efficiency; it is capable of sensing the signal of an inductor DCR in the sub milliohm range (Figure 3). The DCR is the DC winding resistance of the inductor's copper, which is often less than 1mΩ for high current inductors. In high current and low output voltage applications, a conduction loss of a high DCR or a sense resistor will cause a significant reduction in power efficiency. For a specific output requirement, chose the inductor with the DCR that satisfies the maximum desirable sense voltage, and uses the relationship of the sense pin filters to output inductor characteristics as depicted below.

$$DCR = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

$$L/DCR = R_1 \bullet C_1 = 5 \bullet R_2 \bullet C_2$$

where:

$V_{SENSE(MAX)}$: Maximum sense voltage for a given I_{LIM} threshold

I_{MAX}: Maximum load current

ΔI_L: Inductor ripple current

L, DCR: Output inductor characteristics

R1, C1: Filter time constant of the SNSD+ pin

R2, C2: Filter time constant of the SNSA+ pin

To ensure that the load current will be delivered over the full operating temperature range, the temperature coefficient of DCR resistance, approximately 0.4%/°C, should be taken into account. The LTC7130 features a DCR temperature compensation circuit that uses an NTC temperature sensing resistor for this purpose. See the Inductor DCR Sensing Temperature Compensation section for details.

Typically, C1 and C2 are selected in the range of 0.047µF to 0.47µF. If C1 and C2 are chosen to be 220nF, and an inductor of 0.25µH with 0.37mΩ DCR is selected, R1 and R2 will be 3.09k and 619Ω respectively. The bias current at SNSD+ and SNSA+ is about 30nA and 500nA respectively, and it causes some small error to the sense signal.

There will be some power loss in R1 and R2 that relates to the duty cycle, and will be the most in continuous mode at the maximum input voltage:

$$P_{LOSS}(R) = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \bullet V_{OUT}}{R}$$

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Ensure that R1 and R2 have a power rating higher than this value. However, DCR sensing eliminates the conduction loss of a sense resistor; it will provide a better efficiency at heavy loads. The actual ripple voltage will be determined by the following equation:

$$\Delta V_{SENSE} = \frac{V_{OUT}}{V_{IN}} \bullet \frac{V_{IN} - V_{OUT}}{R1 \bullet C1 \bullet f_{OSC}}$$

Inductor DCR Sensing Temperature Compensation with NTC Thermistor

For DCR sensing applications, the temperature coefficient of the inductor winding resistance should be taken into account when the accuracy of the current limit is critical over a wide range of temperature. The main element used in inductors is Copper; that has a positive tempco of approximately 4000ppm/°C. The LTC7130 provides a feature to correct for this variation through the use of the ITEMP pin. There is a 10µA precision current source flowing out of the ITEMP pin. A thermistor with a NTC (negative temperature coefficient) resistance can be used in a network, R_{ITEMP} (Figure 3) connected to maintain the current limit threshold constant over a wide operating temperature. The ITEMP voltage range that activates the correction is from 0.7V or less. If floating this pin, its voltage will be at $INTV_{CC}$ potential, about 5.5V. When the ITEMP voltage is higher than 0.7V, the temperature compensation is inactive.

The following guidelines will help to choose components for temperature correction. The initial compensation is for 25°C ambient temperature:

1. Set the ITEMP pin resistance to 70k at 25°C. With 10µA flowing out of the ITEMP pin, the voltage on the ITEMP pin will be 0.7V at room temperature. Current limit correction will occur for inductor temperatures greater than 25°C.
2. Calculate the ITEMP pin resistance at the maximum inductor temperature, which is typically 100°C.

Use the following equations:

$$V_{ITEMP100C} = 0.7 - 1.5\left(\frac{I_{MAX} \bullet DCR\,(Max) \bullet \frac{(100°C - 25°C) \bullet 0.4}{100}}{V_{SENSE(MAX)}}\right) = 0.25V$$

Since $V_{SENSE(MAX)} = I_{MAX} \bullet DCR\,(Max)$:

$$R_{ITEMP100C} = \frac{V_{ITEMP100C}}{10\mu A} = 25k$$

where:

$R_{ITEMP100C}$ = ITEMP pin resistance at 100°C;

$V_{ITEMP100C}$ = ITEMP pin voltage at 100°C;

$V_{SENSE(MAX)}$ = Maximum current sense threshold at room temperature;

I_{MAX} = Maximum load current; and

DCR (Max) = Maximum DCR value.

Calculate the values for the NTC network's parallel and series resistors, R_P and R_S. A simple method is to graph the following R_S versus R_P equations with R_S on the y-axis and R_P on the x-axis.

$$R_S = R_{ITEMP25C} - R_{NTC25C} || R_P$$

$$R_S = R_{ITEMP100C} - R_{NTC100C} || R_P$$

Next, find the value of R_P that satisfies both equations, which will be the point where the curves intersect. Once R_P is known, solve for R_S. The resistance of the NTC thermistor can be obtained from the vendor's data sheet in the form of graphs, tabulated data, or formulas. The approximate value for the NTC thermistor for a given temperature can be calculated from the following equation:

$$R = R_0 \bullet \exp\left(B \bullet \left(\frac{1}{T + 273} - \frac{1}{T_0 + 273}\right)\right)$$

APPLICATIONS INFORMATION

where:

R = Resistance at temperature T, which is in degrees C.

R_0 = Resistance at temperature T_0, typically 25°C.

B = B-constant of the thermistor.

Figure 4 shows a typical resistance curve for a 100k thermistor and the ITEMP pin network over temperature.

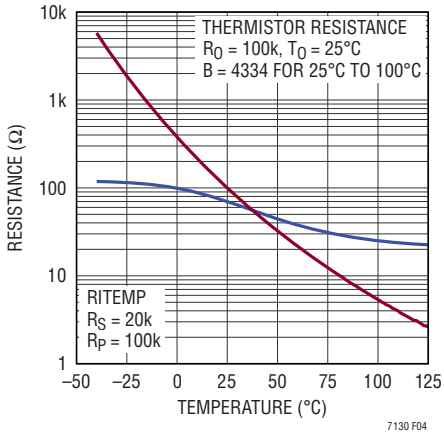

Figure 4. Resistance Versus Temperature for the ITEMP Pin Network and the 100k NTC

Starting values for the NTC compensation network are:

- NTC R_0 = 100k
- R_S = 20k
- R_P =100k

But, the final values should be calculated using the above equations and checked at 25°C and 100°C. After determining the components for the temperature compensation network, check the results by plotting I_{MAX} versus inductor temperature using the following equations:

$$I_{DC(MAX)} = \frac{V_{SENSEMAX(ADJ)} - \frac{\Delta V_{SENSE}}{2}}{DCR(MAX)\ \text{at}\ 25°C \bullet \left(1 + \left(T_{L(MAX)} - 25°C\right) \bullet \frac{0.4}{100}\right)}$$

where:

$$V_{SENSEMAX(ADJ)} = V_{SENSE(MAX)} \bullet \frac{2.2 - V_{ITEMP}}{1.5};$$

V_{ITEMP} = 10µA • (R_S + R_P||R_{NTC});

$I_{DC(MAX)}$ = Maximum average inductor current; and

T_L is the inductor temperature.

The resulting current limit should be greater than or equal to I_{MAX} for inductor temperatures between 25°C and 100°C.

With the front page circuit where the current limit setting is 15mV, and inductor DCR is 0.37mΩ, the LTC7130 can deliver 20A of load current from 25°C to 125°C without the need for temperature compensation, however, if another inductor with a higher DCR is chosen, say 0.53mΩ, the current limit can be compensated by using the temperature compensation network. (Figure 5).

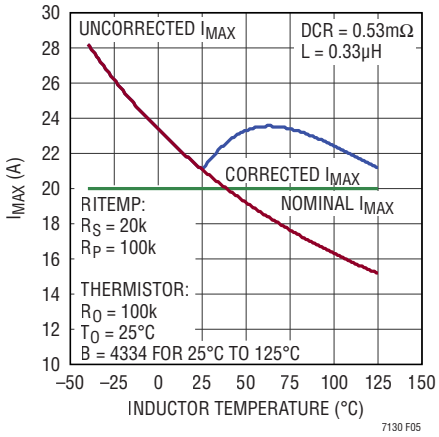

Figure 5. Worst-Case I_{MAX} Versus Inductor Temperature Curve with and without NTC Temperature Compensation

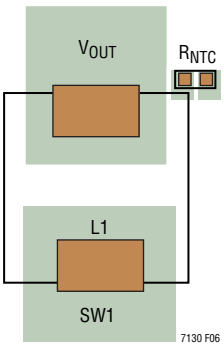

Figure 6. Thermistor Location. Place the Thermistor Next to the Inductor for Accurate Sensing of the Inductor Temperature, But Keep the ITEMP Pin Away from the Switch Nodes and Gate Drive Traces

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For the most accurate temperature detection, place the thermistor next to the output inductor as shown in Figure 6. Care should be taken to keep the ITEMP sense line away from switch nodes.

Pre-Biased Output Start-Up

There may be situations that require the power supply to start up with a pre-bias on the output capacitors. In this case, it is desirable to start up without discharging that output pre-bias. The LTC7130 can safely power up into a pre-biased output without discharging it.

The LTC7130 accomplishes this by turning off both top and bottom MOSFETs until the TK/SS pin voltage and the internal soft-start voltage are above the V_{FB} pin voltage. When V_{FB} is higher than TK/SS or the internal soft-start voltage, the error amp output is railed low. The control loop would like to turn bottom MOSFET on, which would discharge the output. Disabling both MOSFETs will prevent the pre-biased output voltage from being discharged. When TK/SS and the internal soft-start both cross 500mV or V_{FB}, whichever is lower, both MOSFETs are enabled. If the pre-bias is higher than the OV threshold, the bottom MOSFET is turned on immediately to pull the output back into the regulation window.

Overcurrent Fault Recovery

When the output of the power supply is loaded beyond its preset current limit, the regulated output voltage will collapse depending on the load. The output may be shorted to ground through a very low impedance path or it may be a resistive short, in which case the output will collapse partially, until the load current equals the preset current limit. The controller will continue to source current into the short. The amount of current sourced depends on the ILIM pin setting and the V_{FB} voltage as shown in the Current Foldback graph in the Typical Performance Characteristics section.

Upon removal of the short, the output soft starts using the internal soft-start, thus reducing output overshoot. In the absence of this feature, the output capacitors would have been charged at current limit, and in applications with minimal output capacitance this may have resulted in output overshoot. Current limit foldback is not disabled during an overcurrent recovery. The load must step below the folded back current limit threshold in order to restart from a hard short.

Thermal Considerations

In some applications where the LTC7130 is operated at high ambient temperature, high V_{IN}, high switching frequency and maximum output current load, the heat dissipated may exceed the maximum junction temperature of the part.

To avoid the LTC7130 from exceeding the maximum junction temperature, current rating shall be derated in accordance to Ambient Temperature vs Maximum Load Current in the Typical Performance Characteristics.

The junction to ambient thermal resistance will vary depending on the size amount of heat sinking copper on the PCB board where the part is mounted, as well as the amount of air flow on the device. Figure 7, 8 and 9 show temperature derating with both heatsink and airflow.

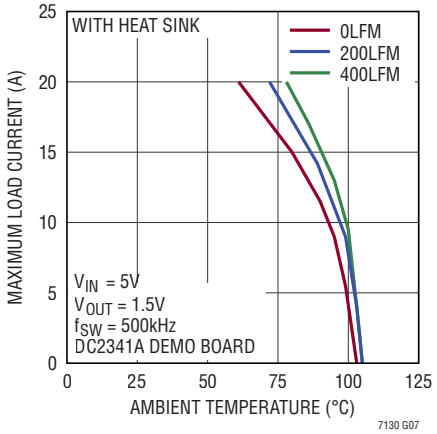

Figure 7. Temperature Derating Curve Based on the DC2341A Demo Board

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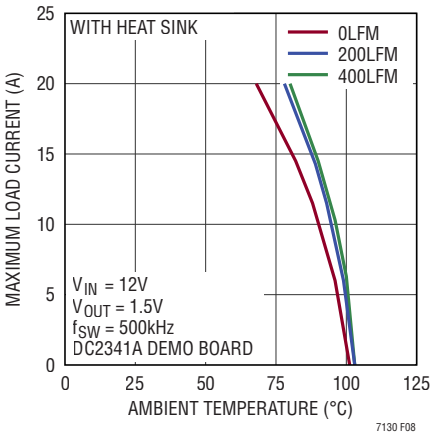

Figure 8. Temperature Derating Curve Based on the DC2341A Demo Board

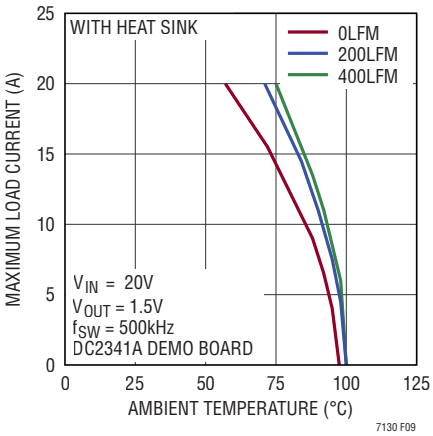

Figure 9. Temperature Derating Curve Based on the DC2341A Demo Board

Tables 1 and 2 provide heat sink and thermal conductive adhesive tape information.

Table 1. Heat Sink Manufacturer (Thermally Conductive Adhesive Tape Pre-Attached)

HEAT SINK MANUFACTURER	PART NUMBER	WEBSITE
Cool Innovations	3-040404U	www.coolinnovations.com

Table 2. Thermally Conductive Adhesive Tape Vendor

THERMALLY CONDUCTIVE ADHESIVE TAPE MANUFACTURER	PART NUMBER	WEBSITE
Chomerics	T411	www.chomerics.com

Inductor Value Calculation

Given the desired input and output voltages, the inductor value and operating frequency, f_{OSC}, directly determine the inductor's peak-to-peak ripple current:

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN}}\left(\frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet L}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor.

It is recommended to choose a ripple current that is about 50% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \approx \frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet I_{RIPPLE}} \bullet \frac{V_{OUT}}{V_{IN}}$$

Inductor Core Selection

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the

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maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[(V_{OUT})(V_{IN}-V_{OUT})\right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC7130, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

Ceramic capacitors are becoming very popular for small designs but several cautions should be observed. X7R, X5R and Y5V are examples of a few of the ceramic materials used as the dielectric layer, and these different dielectrics have very different effect on the capacitance value due to the voltage and temperature conditions applied. Physically, if the capacitance value changes due to applied voltage change, there is a concomitant piezo effect which results in radiating sound! A load that draws varying current at an audible rate may cause an attendant varying input voltage on a ceramic capacitor, resulting in an audible signal. A secondary issue relates to the energy flowing back into a ceramic capacitor whose capacitance value is being reduced by the increasing charge. The voltage can increase at a considerably higher rate than the constant current being supplied because the capacitance value is decreasing as the voltage is increasing! Nevertheless, ceramic capacitors, when properly selected and used, can provide the lowest overall loss due to their extremely low ESR.

A small (0.1µF to 1µF) bypass capacitor, C_{IN}, between the chip V_{IN} pin and ground, placed close to the LTC7130, is also suggested. A 2.2Ω to 10Ω resistor placed between C_{IN} and V_{IN} pin provides further isolation.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically once the ESR requirement is satisfied the capacitance is adequate for filtering.

The steady-state output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_{RIPPLE}\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_{RIPPLE} = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_{RIPPLE} increases with input voltage. The output ripple will be less than 50mV at maximum V_{IN} with $\Delta I_{RIPPLE} = 0.4I_{OUT(MAX)}$ assuming:

$$C_{OUT}\ \text{required ESR} < N \bullet R_{SENSE}$$

and

$$C_{OUT} > \frac{1}{(8f)(R_{SENSE})}$$

The emergence of very low ESR capacitors in small, surface mount packages makes very small physical implementations possible. The ability to externally compensate the switching regulator loop using the ITH pin allows a much wider selection of output capacitor types. The impedance characteristic of each capacitor type is significantly different than an ideal capacitor and therefore requires accurate modeling or bench evaluation during design. Manufacturers such as Nichicon, Nippon Chemi-Con and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitors available from Sanyo and the Panasonic SP surface mount types have a good (ESR)(size) product.

Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. Ceramic capacitors from AVX, Taiyo Yuden, Murata and TDK offer high capacitance value and very low ESR, especially applicable for low output voltage applications.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer surface mount capacitors offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several

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excellent choices are the AVX TPS, AVX TPSV, the KEMET T510 series of surface mount tantalums or the Panasonic SP series of surface mount special polymer capacitors available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo POSCAP, Sanyo OS-CON, Nichicon PL series and Sprague 595D series. Consult the manufacturers for other specific recommendations.

Differential Amplifier

The LTC7130 has true remote voltage sense capability. The sense connections should be returned from the load, back to the differential amplifier's inputs through a common, tightly coupled pair of PC traces. The differential amplifier rejects common mode signals capacitively or inductively radiated into the feedback PC traces as well as ground loop disturbances. The LTC7130 diffamp has 80kΩ input impedance on DIFFP. It is designed to be connected directly to the output. The output of the diffamp connects to the V_{FB} pin through a voltage divider, setting the output voltage.

External Soft-Start and Tracking

The LTC7130 has the ability to either soft-start by itself or track the output of another channel or external supply. When the controller is configured to soft-start by itself, a capacitor may be connected to its TK/SS pin or the internal soft-start may be used. The controller is in the shutdown state if its RUN pin voltage is below 1.1V and its TK/SS pin is actively pulled to ground in this shutdown state. If the RUN pin voltage is above 1.22V, the controller powers up. A soft-start current of 1.25µA then starts to charge the TK/SS soft-start capacitor. Note that soft-start or tracking is achieved not by limiting the maximum output current of the controller but by controlling the output ramp voltage according to the ramp rate on the TK/SS pin. Current foldback is disabled during this phase to ensure smooth soft-start or tracking. The soft-start or tracking range is defined to be the voltage range from 0V to 0.6V on the TK/SS pin. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = 0.6 \bullet \frac{C_{SS}}{1.25\mu A}$$

Regardless of the mode selected by the MODE/PLLIN pin, the controller always starts in discontinuous mode up to TK/SS = 0.5V. Between TK/SS = 0.5V and 0.54V, it will operate in forced continuous mode and revert to the selected mode once TK/SS > 0.54V. The output ripple is minimized during the 40mV forced continuous mode window, ensuring a clean PGOOD signal. When the channel is configured to track another supply, the feedback voltage of the other supply is duplicated by a resistor divider and applied to the TK/SS pin. Therefore, the voltage ramp rate on this pin is determined by the ramp rate of the other supply's voltage. It is only possible to track another supply that is slower than the internal soft-start ramp. Note that the small soft-start capacitor charging current is always flowing, producing a small offset error. To minimize this error, select the tracking resistive divider value to be small enough to make this error negligible. In order to track down another channel or supply after the soft-start phase expires, the LTC7130 is forced into continuous mode of operation as soon as V_{FB} is below the undervoltage threshold of 0.54V regardless of the setting on the MODE/PLLIN pin. However, the LTC7130 should always be set in forced continuous mode tracking down when there is no load. After TK/SS drops below 0.1V, the controller operates in discontinuous mode.

The LTC7130 allows the user to program how its output ramps up and down by means of the TK/SS pin. Through these pins, the output can be set up to either coincidentally or ratiometrically track another supply's output, as shown in Figure 10. In the following discussions, V_{OUT2} refers to the LTC7130's output as a slave and V_{OUT1} refers to another supply output as a master. To implement the coincident tracking in Figure 10a, connect an additional resistive divider to V_{OUT1} and connect its mid-point to the TK/SS pin of the slave controller. The ratio of this divider should be the same as that of the slave controller's feedback divider shown in Figure 11a. In this tracking mode, V_{OUT1} must be set higher than V_{OUT2}. To implement the ratiometric tracking in Figure 10b, the ratio of the V_{OUT2} divider should be exactly the same as the master controller's feedback divider shown in Figure 11b . By selecting different resistors, the LTC7130 can achieve different modes of tracking including the two in Figure 10.

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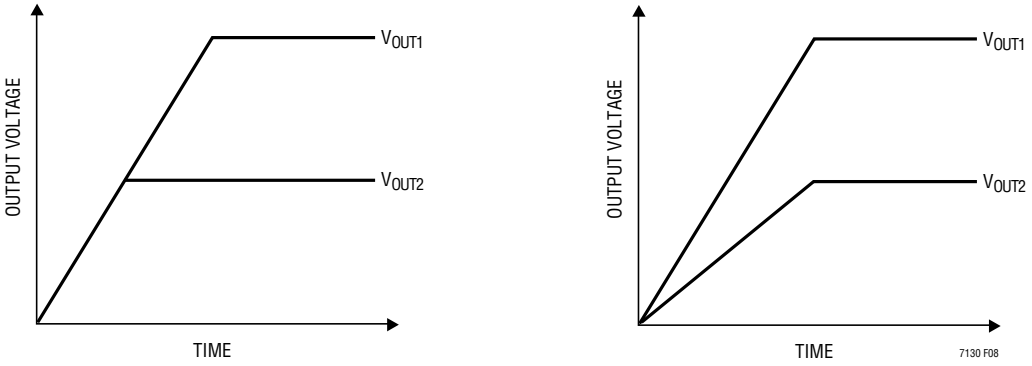
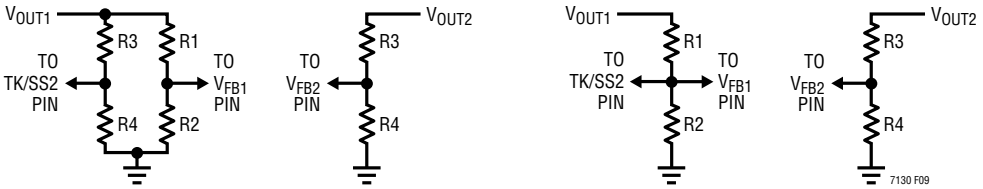


(10a) Coincident Tracking **(10b) Ratiometric Tracking**

Figure 10. Two Different Modes of Output Voltage Tracking



(11a) Coincident Tracking Setup **(11b) Ratiometric Tracking Setup**

Figure 11. Setup and Coincident and Ratiometric Tracking

So which mode should be programmed? While either mode in Figure 10 satisfies most practical applications, some trade-offs exist. The ratiometric mode saves a pair of resistors, but the coincident mode offers better output regulation. Under ratiometric tracking, when the master controller's output experiences dynamic excursion (under load transient, for example), the slave controller output will be affected as well. For better output regulation, use the coincident tracking mode instead of ratiometric.

$INTV_{CC}$ (LDO) and $EXTV_{CC}$

The LTC7130 features a true PMOS LDO that supplies power to $INTV_{CC}$ from the V_{IN} supply. $INTV_{CC}$ powers the gate drivers and much of the LTC7130's internal circuitry. The LDO regulates the voltage at the $INTV_{CC}$ pin to 5.5V when V_{IN} is greater than 6V. $EXTV_{CC}$ connects to $INTV_{CC}$ through a P-channel MOSFET and can supply the needed power when its voltage is higher than 4.7V. Either of these can supply a peak current of 100mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and PGND pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers. High input voltage applications in which the internal MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC7130 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, also known as the driver current, may be supplied by either the 5.5V LDO or $EXTV_{CC}$. When the voltage on the $EXTV_{CC}$ pin is less than 4.5V, the LDO is enabled. The gate charge current is dependent on operating frequency as discussed on Efficiency Considerations section. The power dissipation for the IC in this case is equal to $V_{IN} \bullet INTV_{CC}$. For example, the LTC7130 $INTV_{CC}$ current is about 27.5mA from a 20V supply in the BGA package not using the $EXTV_{CC}$:

$$P_D = 20V \bullet 27.5mA = 0.55W$$

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To reduce the total power loss and prevent the maximum junction temperature from being exceeded due to the IC, the $EXTV_{CC}$ pin can be used to provide MOSFET gate drive and control power. When the voltage applied to $EXTV_{CC}$ rises above 4.7V, the $INTV_{CC}$ LDO is turned off and the $EXTV_{CC}$ is connected to the $INTV_{CC}$. The $EXTV_{CC}$ remains on as long as the voltage applied to $EXTV_{CC}$ remains above 4.5V. Using the $EXTV_{CC}$ allows the MOSFET driver and control power to be derived from an efficient switching regulator output during normal operation. If more current is required through the $EXTV_{CC}$ than is specified, an external Schottky diode can be added between the $EXTV_{CC}$ and $INTV_{CC}$ pins. Do not apply more than 6V to the $EXTV_{CC}$ pin and make sure that $EXTV_{CC} < V_{IN}$.

Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from $EXTV_{CC}$, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (duty cycle)/(switcher efficiency). Tying the $EXTV_{CC}$ pin to a 5V supply reduces power loss of the IC to:

$$P_D = 5V \bullet 24.5mA = 0.14W$$

However, for low voltage outputs, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the three possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. This will cause $INTV_{CC}$ to be powered from the internal LDO resulting in an efficiency penalty of up to 10% at high input voltages.
2. $EXTV_{CC}$ connected to an external supply. If a 5V external supply is available, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements.
3. $EXTV_{CC}$ connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 4.7V.

For applications where the main input power is 5V, tie the V_{IN} and $INTV_{CC}$ pins together and tie the combined pins to the 5V input with a 1Ω or 2.2Ω resistor as shown in Figure 12 to minimize the voltage drop caused by the gate charge current. This will override the $INTV_{CC}$ linear regulator and will prevent $INTV_{CC}$ from dropping too low due to the dropout voltage. Make sure the $INTV_{CC}$ voltage is at or exceeds the $R_{DS(ON)}$ test voltage for the MOSFET which is typically 4.5V for logic-level devices.

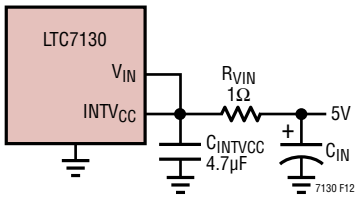

Figure 12. Setup for a 5V Input

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitor, C_B, connected to the BOOST pin supplies the gate drive voltages for the topside MOSFET. Capacitor C_B in the Functional Diagram is charged through external diode D_B from $INTV_{CC}$ when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate source of the MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply:

$$V_{BOOST} = V_{IN} + V_{INTVCC} – V_{DB}$$

The value of the boost capacitor, C_B, needs to store approximately 100 times the gate charge required by the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

For applications that require high V_{IN} and high output current, in order to minimize SW node ringing and EMI, connect a 2Ω to 10Ω resistor R_{BOOST} in series with the BOOST pin. Make the C_B and D_B connections on the other side of the resistor. This series resistor helps to

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slow down the SW node rise time, limiting the high d_I/d_t current through the top MOSFET that causes SW node ringing (see Figure 13).

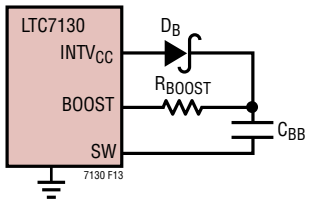

Figure 13. Using Boost Resistor

Setting Output Voltage

The LTC7130 output voltage is set by an external feedback resistive divider carefully placed across the DIFFOUT pin, as shown in Figure 14. The regulated output voltage is determined by:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R_B}{R_A}\right)$$

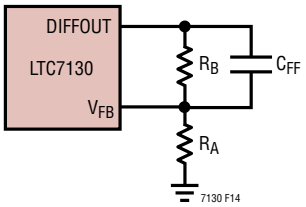

Figure 14. Setting Output Voltage

To improve the frequency response, a feedforward capacitor, C_{FF}, may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

To minimize the effect of the voltage drop caused by high current flowing through board conductance; connect DIFFN and DIFFP sense lines close to the ground and the load output respectively.

Fault Conditions: Current Limit and Current Foldback

The LTC7130 includes current foldback to help limit load current when the output is shorted to ground. If the output falls below 50% of its nominal output level, then the maximum sense voltage is progressively lowered from its maximum programmed value to one-third of the maximum value. Foldback current limiting is disabled during the soft-start or tracking up using the TK/SS pin. It is not disabled for internal soft-start. Under short-circuit conditions with very low duty cycles, the LTC7130 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short circuit ripple current is determined by the minimum on-time $t_{ON(MIN)}$ of the LTC7130 (≈90ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \bullet \frac{V_{IN}}{L}$$

The resulting short-circuit current is:

$$I_{SC} = \left(\frac{1/3\, V_{SENSE(MAX)}}{R_{SENSE}} - \frac{1}{2}\Delta I_{L(SC)}\right)$$

After a short, or while starting with internal soft-start, make sure that the load current takes the folded-back current limit into account.

Phase-Locked Loop and Frequency Synchronization

The LTC7130 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the turn-on of the top MOSFET to be locked to the rising edge of an external clock signal applied to the MODE/PLLIN pin. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. There is a precision 10µA current flowing out of the FREQ pin. This allows the user to use a single resistor to SGND to set the switching frequency when no external clock is applied to the MODE/PLLIN pin. The internal switch between the FREQ pin and the integrated PLL filter network is on, allowing the filter network to be pre-charged to the same voltage as the FREQ pin. The

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relationship between the voltage on the FREQ pin and operating frequency is shown in Figure 15 and specified in the Electrical Characteristics table. If an external clock is detected on the MODE/PLLIN pin, the internal switch mentioned above turns off and isolates the influence of the FREQ pin. Note that the LTC7130 can only be synchronized to an external clock whose frequency is within range of the LTC7130's internal VCO. This is guaranteed to be between 250kHz and 770kHz. A simplified block diagram is shown in Figure 16.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the filter network. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the filter network. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the filter network is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor C_{LP} holds the voltage.

Typically, the external clock (on the MODE/PLLIN pin) input high threshold is 1.6V, while the input low threshold is 1V.

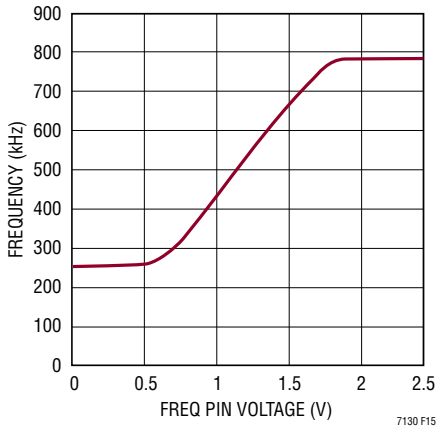

Figure 15. Relationship Between Oscillator Frequency and Voltage at the FREQ Pin

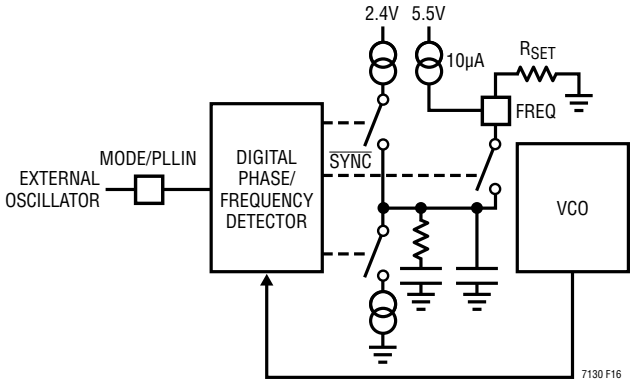

Figure 16. Phase-Locked Loop Block Diagram

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC7130 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the voltage ripple and current ripple will increase. The minimum on-time for the LTC7130 is approximately 90ns, with good PCB layout, minimum 50% inductor current ripple and at least 2mV ripple on the current sense signal. The minimum on-time can be affected by PCB switching noise in the voltage and current loop. As the peak sense voltage decreases the minimum on-time gradually increases to about 110ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine

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what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

% Efficiency = 100%–(L1 + L2 + L3 +…)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LTC7130 circuits: 1) I^2R losses, 2) switching and biasing losses, 3) other losses.

1. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L but is "chopped" between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $R_{SW} = (R_{DS(ON)}TOP)(DC) + (R_{DS(ON)}BOT)(1\text{-}DC)$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I^2R losses:

   $I^2R \text{ losses} = I_{OUT}^2(R_{SW} + R_L)$

2. The $INTV_{CC}$ current is the sum of the power MOSFET driver and control currents. The power MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f is the switching frequency. Since $INTV_{CC}$ is a low dropout regulator output powered by V_{IN}, its power loss equals:

   $P_{LDO} = V_{IN} \bullet I_{INTVCC}$

3. Other "hidden" losses such as transition loss and copper trace and internal load resistances can account for additional efficiency degradations in the overall power system. It is very important to include these "system" level losses in the design of a system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. Other losses including diode conduction losses during dead-time and inductor core losses which generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the ITH pin not only allows optimization of control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in the Typical Application circuit will provide an adequate starting point for most applications. The ITH series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a

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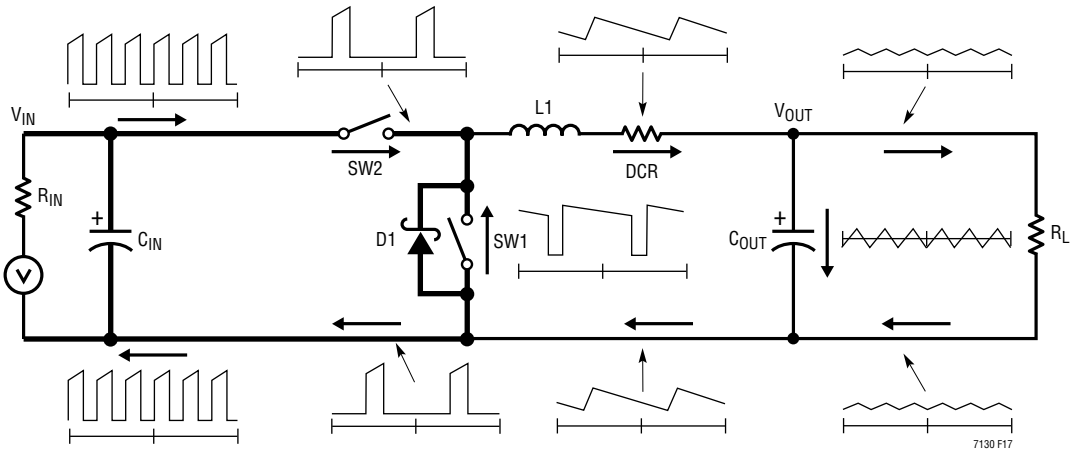
rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 17. Check the following in the PC layout:

1. The $INTV_{CC}$ decoupling capacitor should be placed immediately adjacent to the IC between the $INTV_{CC}$ pin and PGND plane. A 1µF ceramic capacitor of the X7R or X5R type is small enough to fit very close to the IC to minimize the ill effects of the large current pulses drawn to drive the bottom MOSFETs. An additional 4.7µF to 10µF of ceramic, tantalum or other very low ESR capacitance is recommended in order to keep the internal IC supply quiet.
2. Place the feedback divider between the + and – terminals of C_{OUT}. Route DIFFP and DIFFN with minimum PC trace spacing from the IC to the feedback divider.
3. Are the $SNSD^+$, $SNSA^+$ and SNS^- printed circuit traces routed together with minimum PC trace spacing? The filter capacitors between $SNSD^+$, $SNSA^+$ and SNS^- should be as close as possible to the pins of the IC. Connect the $SNSD^+$ and $SNSA^+$ pins to the filter resistors as illustrated in Figure 3.



BOLD LINES INDICATE HIGH, SWITCHING CURRENTS. KEEP LINES TO A MINIMUM LENGTH

Figure 17. Branch Current Waveforms

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4. Do the (+) plates of C_{IN} connect to the drain of the topside MOSFET as closely as possible? This capacitor provides the pulsed current to the MOSFET.

5. Keep the switching nodes, SW, BOOST away from sensitive small-signal nodes ($SNSD^+$, $SNSA^+$, SNS^-, DIFFP, DIFFN, V_{FB}). Ideally the SW, and BOOST printed circuit traces should be routed away and separated from the IC and especially the *quiet* side of the IC. Separate the high d_V/d_t traces from sensitive small-signal nodes with ground traces or ground planes.

6. Use a low impedance source such as a logic gate to drive the MODE/PLLIN pin and keep the lead as short as possible.

7. The 47pF to 330pF ceramic capacitor between the I_{TH} pin and signal ground should be placed as close as possible to the IC. Figure 17 illustrates all branch currents in a switching regulator. It becomes very clear after studying the current waveforms why it is critical to keep the high switching current paths to a small physical size. High electric and magnetic fields will radiate from these *loops* just as radio stations transmit signals. The output capacitor ground should return to the negative terminal of the input capacitor and not share a common ground path with any switched current paths. The left half of the circuit gives rise to the *noise* generated by a switching regulator. The GND terminations and Schottky diode should return to the bottom plate(s) of the input capacitor(s) with a short isolated PC trace since very high switched currents are present. External OPTI-LOOP® compensation allows overcompensation for PC layouts which are not optimized but this is not the recommended design procedure.

8. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The V_{FB} and ITH traces should be as short as possible. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.

9. Use a modified "star ground" technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the SGND pin of the IC.

Design Example

As a design example of the front page circuit for a single channel high current regulator, assume V_{IN} = 12V(nominal), V_{IN} = 20V(maximum), V_{OUT} = 1.5V, I_{MAX} = 20A, and f = 500kHz (see front page schematic).

The regulated output voltage is determined by:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R_B}{R_A}\right)$$

Using a 20k 1% resistor from the V_{FB} node to ground, the top feedback resistor is (to the nearest 1% standard value) 30.1k.

The frequency is set by biasing the FREQ pin to 1.2V (see Figure 15).

The inductance value is based on a 50% maximum ripple current assumption (10A). The highest value of ripple current occurs at the maximum input voltage:

$$L = \frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

This design will require 0.25µH. The Würth 744308025, 0.25µH inductor is chosen. At the nominal input voltage (12V), the ripple current will be:

$$\Delta I_{L(NOM)} = \frac{V_{OUT}}{f \bullet L}\left(1 - \frac{V_{OUT}}{V_{IN(NOM)}}\right)$$

It will have 10.5A (52.5%) ripple. The peak inductor current will be the maximum DC value plus one-half the ripple current, or around 25A.

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The minimum on-time occurs at the maximum V_{IN}, and should not be less than 90ns:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}f} = \frac{1.5V}{20V(500kHz)} = 150ns$$

DCR sensing is used in this circuit. If C1 and C2 are chosen to be 220nF, based on the chosen 0.25µH inductor with 0.37mΩ DCR, R1 and R2 can be calculated as:

$$R1 = \frac{L}{DCR \bullet C1} = 3.07k$$

$$R2 = \frac{L}{DCR \bullet C2 \bullet 5} = 614\Omega$$

Choose R1 = 3.09k and R2 = 619Ω.

The maximum DCR of the inductor is 0.4mΩ. The $V_{SENSE(MAX)}$ is calculated as:

$$V_{SENSE(MAX)} = 25A \bullet DCR_{MAX} = 10mV$$

The current limit is chosen to be 15mV. If temperature variation is considered, please refer to Inductor DCR Sensing Temperature Compensation with NTC Thermistor.

For a 0.37mΩ DCR, a short-circuit to ground will result in a folded back current of:

$$I_{SC} = \frac{(1/3)15mV}{0.37m\Omega} - \frac{1}{2}\left(\frac{90ns(20V)}{0.25\mu H}\right) \approx 10A$$

C_{OUT} is chosen with an equivalent ESR of 4.5mΩ for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$$V_{ORIPPLE} = R_{ESR}\,(\Delta I_L) \approx 0.0045\Omega \bullet 10A = 45mV_{P-P}$$

Further reductions in output voltage ripple can be made by placing a 100µF ceramic capacitor across C_{OUT}.

Very Low Output Ripple Converter

Although the LTC7130 recommends 50% inductor ripple for most it's applications, for applications that need very small output ripple, the inductance can be increased to achieve smaller output ripple.

The schematic as shown Figure 18 is similar to that of the front page circuit, except that three times the inductance and double the output capacitance are used. The compensation components are changed to maintain the same crossover frequency and phase margin. Figure 19 shows the transient response of 10A load step, and Figure 20 demonstrates that the output voltage ripple is a factor of six smaller than that of typical current mode converters.

TYPICAL APPLICATIONS

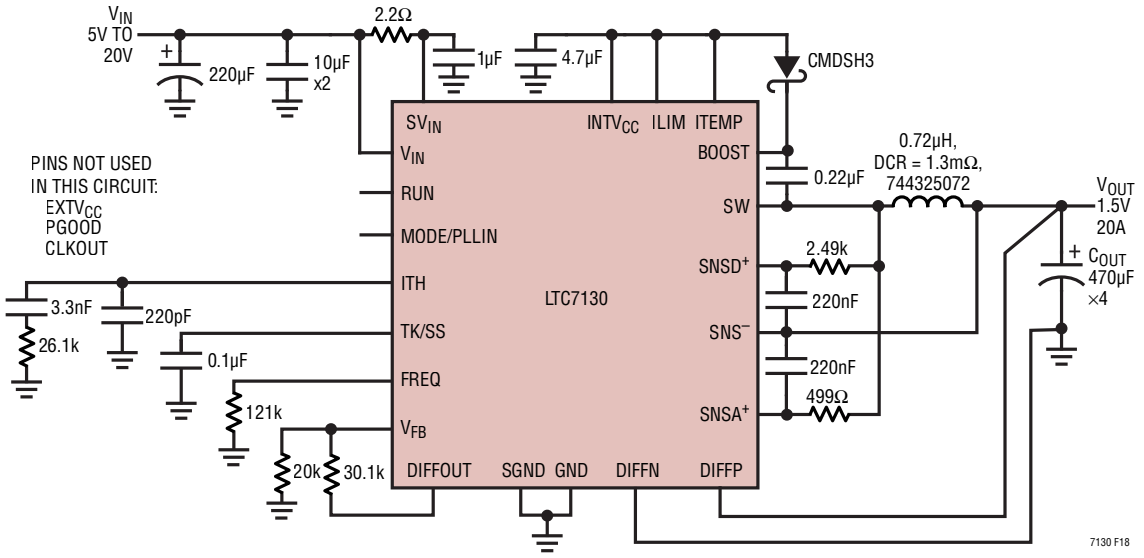


Figure 18. High Efficiency, 1.5V/15A Step-Down Converter with Very Low Output Ripple

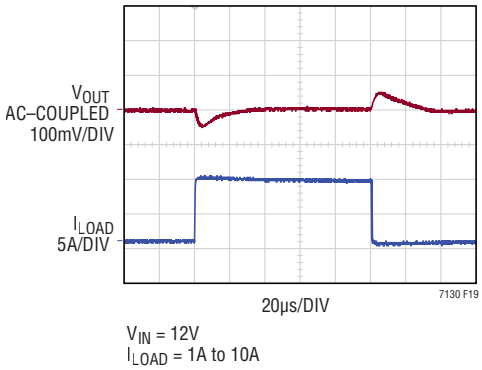


Figure 19. Load Step Transient Response

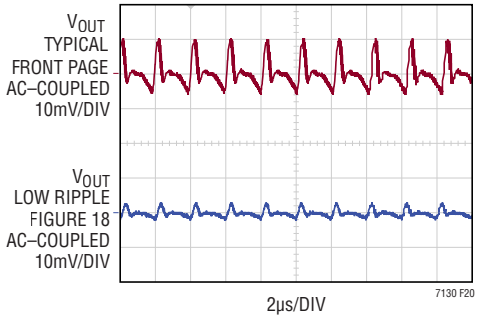
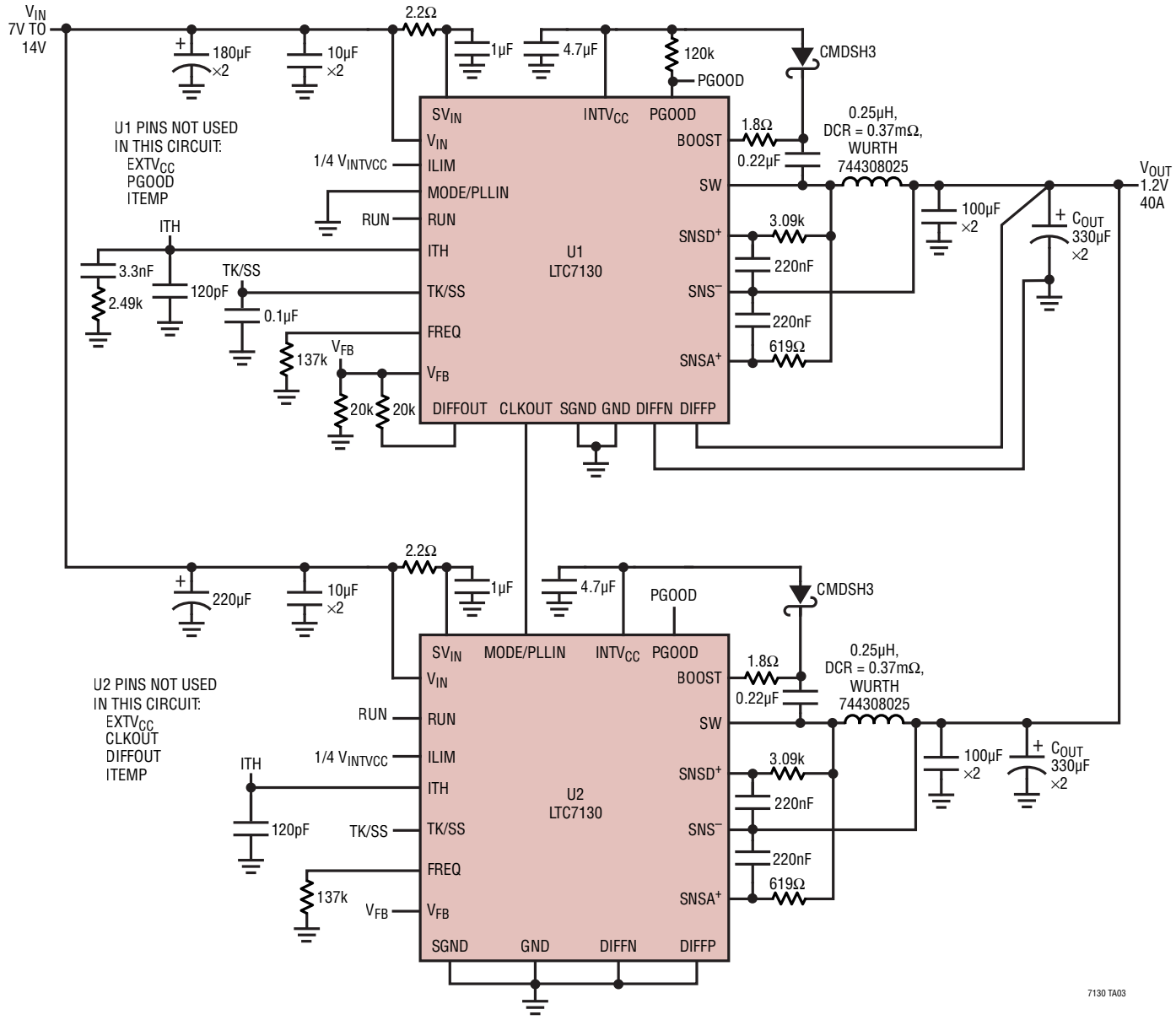


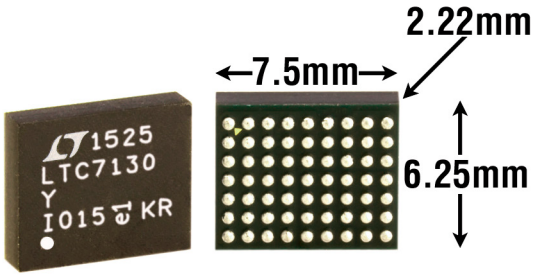
Figure 20. Very Low Output Voltage Ripple

TYPICAL APPLICATIONS

High Efficiency, Dual Phase Very Low DCR Sensing 1.2V/40A Step-Down Supply



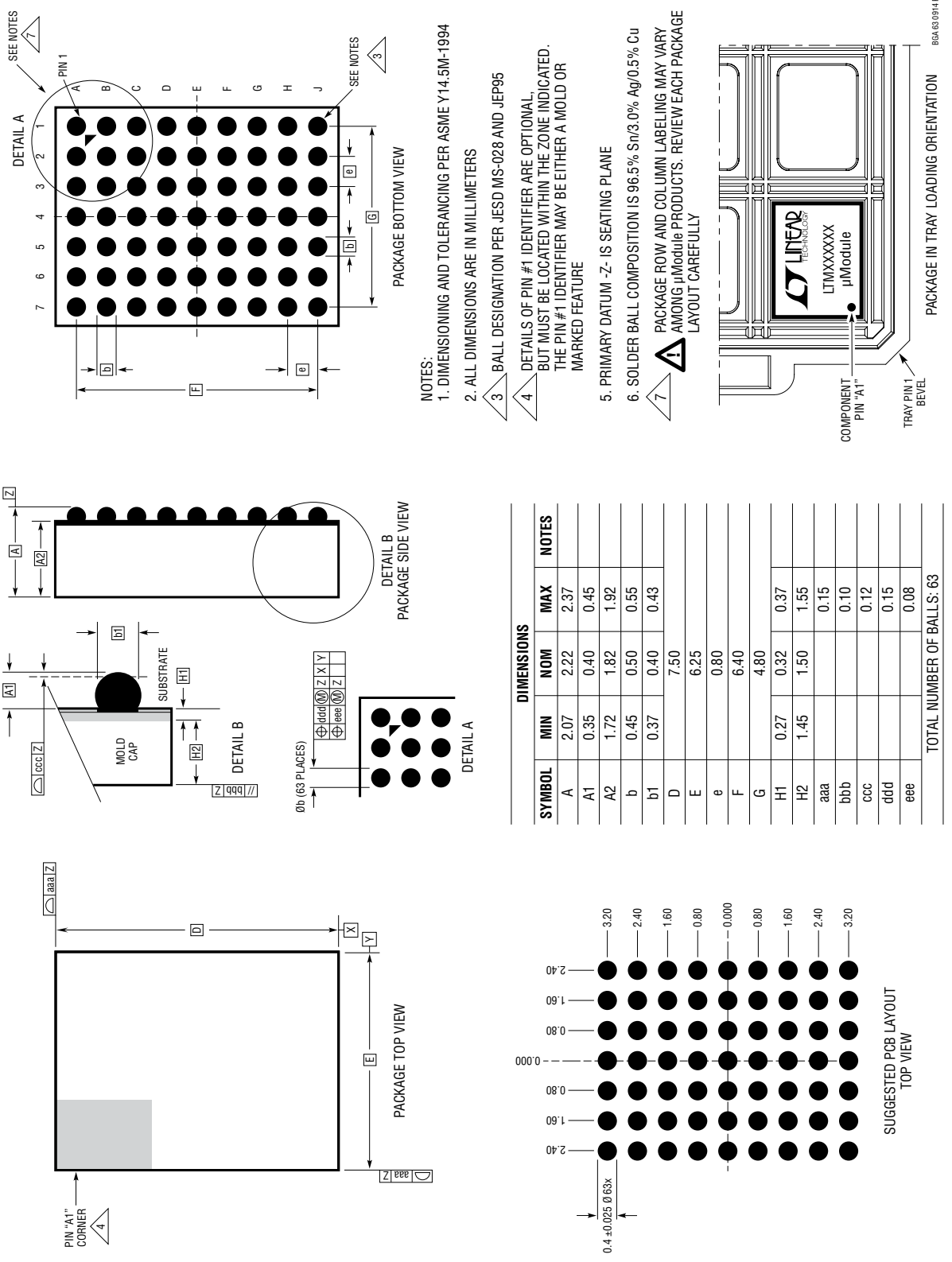
PACKAGE PHOTOGRAPHS



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC7130#packaging for the most recent package drawings.

BGA Package
63-Lead (7.5mm × 6.25mm × 2.22mm)
(Reference LTC DWG # 05-08-1988 Rev Ø)



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	2.07	2.22	2.37	
A1	0.35	0.40	0.45	
A2	1.72	1.82	1.92	
b	0.45	0.50	0.55	
b1	0.37	0.40	0.43	
D		7.50		
E		6.25		
e		0.80		
F		6.40		
G		4.80		
H1	0.27	0.32	0.37	
H2	1.45	1.50	1.55	
aaa			0.15	
bbb			0.10	
ccc			0.12	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 63				

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/16	Modified I_Q conditions	3
		Changed RUN threshold value	8, 12, 13, 22
		Modified $INTV_{CC}/EXTV_{CC}$ section, added Note 7	11
B	05/17	Corrected pin number of Boost pin	8