Nanopower Buck-Boost DC/DC with Integrated Coulomb Counter

FEATURES

- **680nA Input Quiescent Current (Output in Regulation at No Load)**
- **1.8V to 5.5V Input Operating Range**
- **Selectable Output Voltages of 1.8V, 2.5V, 2.8V, 3V, 3.3V, 3.6V, 4.5V, 5V**
- **Integrated Coulomb Counter Measures Accumulated Battery Discharge**
- **±5% Battery Discharge Measurement Accuracy**
- Programmable Peak Input Current of 5mA, 10mA, 15mA, 25mA, 50mA, 100mA, 150mA, 250mA
- Up to 50mA of Output Current
- Up to 90% Efficiency
- Programmable Coulomb Counter Prescaler for Wide Range of Battery Sizes
- Programmable Discharge Alarm Threshold
- I^2C Interface
- Low Profile (0.75mm) 20-Lead (3mm × 4mm) QFN Package

APPLICATIONS

- Long Lifetime Primary Cell Battery Applications
- Wireless Sensors
- Remote Monitors
- Dust Networks® SmartMesh® Applications

DESCRIPTION

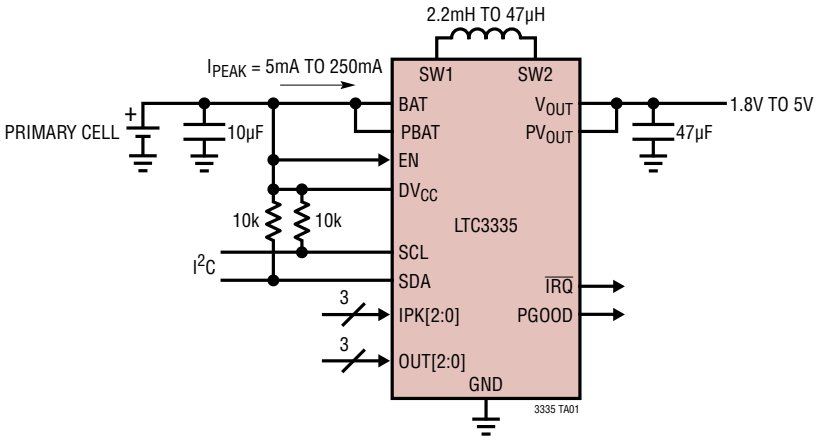
The LTC®3335 is a high efficiency, low quiescent current (680nA) buck-boost DC/DC converter with an integrated precision coulomb counter which monitors accumulated battery discharge in long life battery powered applications. The buck-boost can operate down to 1.8V on its input and provides eight pin-selectable output voltages with up to 50mA of output current.

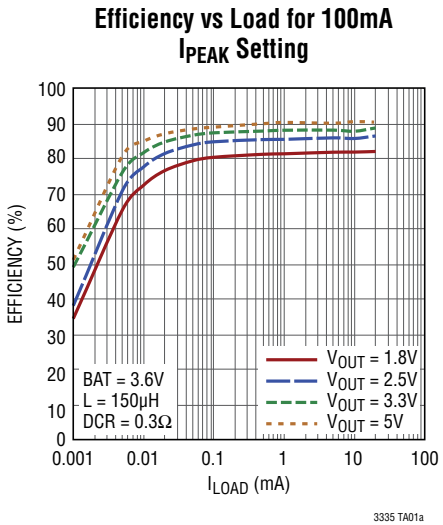
The coulomb counter stores the accumulated battery discharge in an internal register accessible via an I^2C interface. The LTC3335 features a programmable discharge alarm threshold. When the threshold is reached, an interrupt is generated at the $\overline{IRQ}$ pin.

To accommodate a wide range of battery types and sizes, the peak input current can be selected from as low as 5mA to as high as 250mA and the full-scale coulomb counter has a programmable range of 32,768:1.

The LTC3335 is available in a 3mm × 4mm QFN-20 package.

TYPICAL APPLICATION



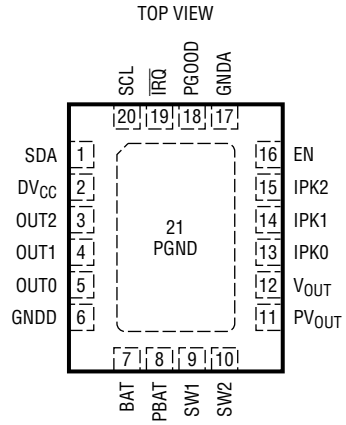


ABSOLUTE MAXIMUM RATINGS

(Note 1)

BAT, PBAT, V_{OUT}, PV_{OUT} Voltage ..... –0.3V to 6V
EN, OUT[2:0],
IPK[2:0] Voltage .....–0.3V to [Lesser of (BAT + 0.3V) or 6V]
DV_{CC}, SDA, SCL Voltage ..... –0.3V to 6V
PGOOD,
$\overline{IRQ}$ Voltage.....–0.3V to [Lesser of (DV_{CC} + 0.3V) or 6V]
SW1, SW2 Current..... 350mA
Operating Junction Temperature Range
(Notes 2, 3)..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UDC PACKAGE
20-LEAD (3mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 52°C/W
EXPOSED PAD (PIN 21) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3335EUDC#PBF	LTC3335EUDC#TRPBF	LGTR	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3335IUDC#PBF	LTC3335IUDC#TRPBF	LGTR	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). BAT = PBAT = DV_{CC} = 3.6V, GNDA = GNDD = PGND = 0V, V_{OUT} = PV_{OUT}.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Buck-Boost DC/DC						
Input Voltage Range		●	1.8		5.5	V
Input Quiescent Current	BAT and PBAT Combined					
Shutdown	EN = 0			440	700	nA
Sleeping (In Regulation)	EN = 1			680	1000	nA
Not Sleeping	EN = 1, I_{SW1} = I_{SW2} = 0 (Note 4)			360	540	µA
Regulated Output Voltage	1.8V Output Setting					
	Sleep Threshold	●		1.806	1.863	V
	Wake-Up Threshold	●	1.737	1.794		V
	2.5V Output Setting					
	Sleep Threshold	●		2.508	2.575	V
	Wake-Up Threshold	●	2.425	2.492		V
	2.8V Output Setting					
	Sleep Threshold	●		2.809	2.884	V
	Wake-Up Threshold	●	2.716	2.791		V
	3V Output Setting					
	Sleep Threshold	●		3.010	3.090	V
	Wake-Up Threshold	●	2.910	2.990		V
	3.3V Output Setting					
	Sleep Threshold	●		3.311	3.400	V
	Wake-Up Threshold	●	3.200	3.289		V
	3.6V Output Setting					
	Sleep Threshold	●		3.612	3.708	V
	Wake-Up Threshold	●	3.492	3.588		V
	4.5V Output Setting					
	Sleep Threshold	●		4.515	4.635	V
	Wake-Up Threshold	●	4.365	4.485		V
	5V Output Setting					
	Sleep Threshold	●		5.017	5.150	V
	Wake-Up Threshold	●	4.850	4.983		V
PGOOD Falling Threshold	(Note 5)	●	89	92	95	%
V_{OUT} Leakage Current	All Output Settings, V_{OUT} in Regulation			100	150	nA
Input Peak Switch Current	250mA I_{PEAK} Setting (Note 6)		225	250	275	mA
		●	200	250	275	mA
	150mA I_{PEAK} Setting (Note 6)		135	150	165	mA
		●	125	150	165	mA
	100mA I_{PEAK} Setting (Note 6)		90	100	110	mA
		●	85	100	110	mA
	50mA I_{PEAK} Setting (Note 6)		45	50	55	mA
		●	42.5	50	55	mA
	25mA I_{PEAK} Setting (Note 6)		21.5	25	27.5	mA
		●	20	25	27.5	mA
	15mA I_{PEAK} Setting (Note 6)		12.5	15	16.5	mA
		●	12	15	16.5	mA
	10mA I_{PEAK} Setting (Note 6)		8.25	10	11	mA
		●	8	10	11	mA
	5mA I_{PEAK} Setting (Note 6)		4	5	5.5	mA
		●	3.75	5	5.5	mA
I_{ZERO} Current Threshold (Note 7)	All I_{PEAK} Settings			0		mA
Available Output Current	100mA I_{PEAK} Setting, V_{OUT} = 3.3V		20			mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). BAT = PBAT = DV_{CC} = 3.6V, GNDA = GNDD = PGND = 0V, V_{OUT} = PV_{OUT}.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PMOS Switch A On-Resistance (From PBAT to SW1)	250mA I_{PEAK} Setting			0.38		Ω
	150mA I_{PEAK} Setting			0.55		Ω
	100mA I_{PEAK} Setting			0.76		Ω
	50mA I_{PEAK} Setting			1.40		Ω
	25mA I_{PEAK} Setting			2.67		Ω
	15mA I_{PEAK} Setting			4.36		Ω
	10mA I_{PEAK} Setting			6.48		Ω
	5mA I_{PEAK} Setting			12.82		Ω
NMOS Switch B On-Resistance (From SW1 to PGND)	250mA I_{PEAK} Setting			0.57		Ω
	150mA I_{PEAK} Setting			0.85		Ω
	100mA I_{PEAK} Setting			1.20		Ω
	50mA I_{PEAK} Setting			2.26		Ω
	25mA I_{PEAK} Setting			4.37		Ω
	15mA I_{PEAK} Setting			7.18		Ω
	10mA I_{PEAK} Setting			10.69		Ω
	5mA I_{PEAK} Setting			21.20		Ω
NMOS Switch C On-Resistance (From SW2 to PGND)	IPK[2:0] = 1xx			0.37		Ω
	IPK[2:0] = 0xx			2.05		Ω
PMOS Switch D On-Resistance (From PV_{OUT} to SW2) PV_{OUT} = V_{OUT} = 3.3V	250mA I_{PEAK} Setting			0.60		Ω
	150mA I_{PEAK} Setting			0.86		Ω
	100mA I_{PEAK} Setting			1.18		Ω
	50mA I_{PEAK} Setting			2.14		Ω
	25mA I_{PEAK} Setting			4.06		Ω
	15mA I_{PEAK} Setting			6.61		Ω
	10mA I_{PEAK} Setting			9.81		Ω
	5mA I_{PEAK} Setting			19.40		Ω
PMOS Switch Leakage	Switches A, D SW1 = SW2 = 0V, BAT = 5.5V, V_{OUT} = 5.5V			0	10	nA
NMOS Switch Leakage	Switches B, C SW1 = BAT = 5.5V, SW2 = V_{OUT} = 5.5V			0	10	nA
Coulomb Counter						
q_{LSB} (for Prescaler setting M=0) (Notes 8,9)	250mA I_{PEAK} Setting			7.031		A • hr
	150mA I_{PEAK} Setting			4.218		A • hr
	100mA I_{PEAK} Setting (Note 10)	●	2.728	2.812	2.896	A • hr
	50mA I_{PEAK} Setting			1.406		A • hr
	25mA I_{PEAK} Setting			703.1		mA • hr
	15mA I_{PEAK} Setting			421.8		mA • hr
	10mA I_{PEAK} Setting			281.2		mA • hr
	5mA I_{PEAK} Setting			140.6		mA • hr
Full-Scale Coulomb Count (Battery Capacity)	5mA I_{PEAK} Setting, M=15, L = 2.2mH; (Smallest Battery)			1.094		mA • hr
	100mA I_{PEAK} Setting, M = 8, L = 100µH	●	2.717	2.801	2.885	A • hr
	250mA I_{PEAK} Setting, M = 0, L = 47µH; (Largest Battery)			1793		A • hr
Total Unadjusted Coulomb Counter Error (Note 10)	Buck-Boost Switching, 100mA I_{PEAK} Setting, V_{OUT} = 3.3V, BAT = 3.6V	●	–5		5	%
Digital Inputs and Output						
DV_{CC} Voltage		●	1.8		5.5	V
Digital Input High Voltage	For Pins EN, IPK[2:0], OUT[2:0] For Pins SDA, SCL	●	BAT – 0.5 70			V %DV_{CC}

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). BAT = PBAT = DV_{CC} = 3.6V, GNDA = GNDD = PGND = 0V, V_{OUT} = PV_{OUT}.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Input Low Voltage	For Pins EN, IPK[2:0], OUT[2:0] For Pins SDA, SCL	●			0.5 30	V %DV_{CC}
Digital Output High Voltage	For Pins PGOOD, $\overline{IRQ}$; 1µA Out of Pin	●	DV_{CC} – 0.5			V
Digital Output Low Voltage	For Pins PGOOD, $\overline{IRQ}$; 1µA Into Pin For Pin SDA; 3mA Into Pin	●			0.5 0.4	V V
Input High Current	For Pins EN, IPK[2:0], OUT[2:0], SDA, SCL			0	10	nA
Input Low Current	For Pins EN, IPK[2:0], OUT[2:0], SDA, SCL			0	10	nA
I^2C Timing Characteristics (See Figure 1)						
I^2C Read Address I^2C Write Address				11001001 11001000		
Clock Operating Frequency	f_{SCL}				400	kHz
Bus Free Time Between STOP/START	t_{BUF}		1.3			µs
Repeated START Set-Up Time	$t_{SU,STA}$		600			ns
Hold Time (Repeated) START Condition	$t_{HD,STA}$		600			ns
Set-Up Time for STOP Condition	$t_{SU,STO}$		600			ns
Data Set-Up Time (Input)	$t_{SU,DAT}$		100			ns
Data Hold Time (Input)	$t_{HD,DATI}$		0			µs
Data Hold Time (Output)	$t_{HD,DATO}$		0		0.9	µs
Clock/Data Fall Time	t_f		20		300	ns
Clock/Data Rise Time	t_r		20		300	ns
Clock LOW Period	t_{LOW}		1.3			µs
Clock HIGH Period	t_{HIGH}		0.6			µs
Spike Suppression Time	t_{SP}				50	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3335 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3335E is guaranteed to meet specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LTC3335I is guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors.

Note 3: T_J is calculated from the ambient T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D \bullet \theta_{JA})$.

Note 4: Dynamic supply current is higher due to gate charge being delivered at the switching frequency.

Note 5: The PGOOD Falling Threshold is specified as a percentage of the average of the measured sleep and wake-up thresholds for each selected output. The PGOOD rising threshold is equal to the sleep threshold. See Regulated Output Voltage specification.

Note 6: For the 100mA I_{PEAK} setting, the value given in the table is measured in a closed-loop set-up with a 100µH inductor, a 3.6V BAT voltage, and the LTC3335 switching. For the other seven I_{PEAK} settings, the values given in the table are calculated from an open-loop DC measurement of I_{PEAK} (LTC3335 not switching), the propagation delay of the I_{PEAK} comparator, and the recommended inductor value for each I_{PEAK} setting.

Note 7: I_{ZERO} measurements are performed when the LTC3335 is not switching. The values seen in operation will be slightly lower due to the propagation delay of the comparators

Note 8: The equivalent charge of an LSB in the accumulated charge register depends on the I_{PEAK} setting and the internal pre-scaling factor M. See Choosing Coulomb Counter Prescaler M section for more information. 1mA • hr = 3.6A • s = 3.6C.

Note 9: The values given in the table are for applications using the recommended inductor value for each I_{PEAK} setting.

Note 10: The specified accuracy of q_{LSB} in percent is better than that of the corresponding I_{PEAK} because the full-scale ON time of the AC(ON) time measurement is internally adjusted to compensate for errors in the actual I_{PEAK} value. The Total Unadjusted Coulomb Counter Error specified includes any inaccuracy in q_{LSB}.

TIMING DIAGRAM

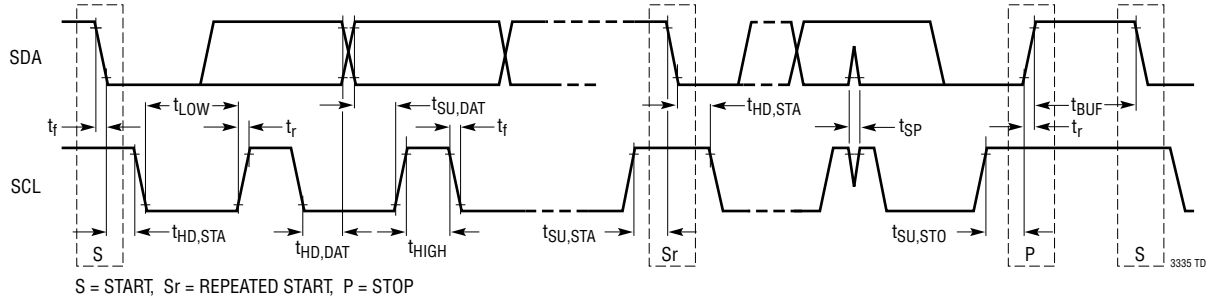
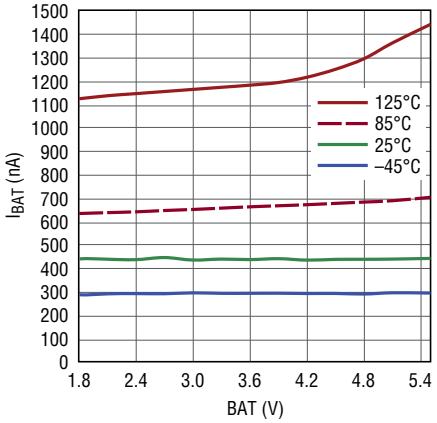


Figure 1. Definition of Timing on I²C Bus

TYPICAL PERFORMANCE CHARACTERISTICS

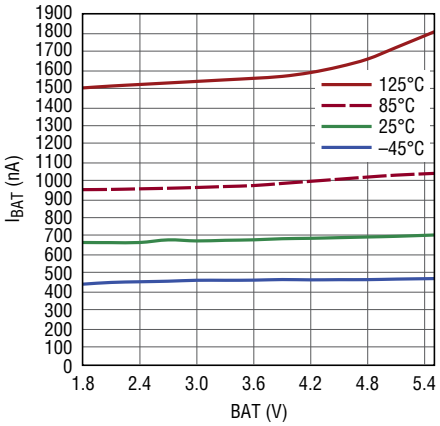
T_A = 25°C, BAT = PBAT = 3.6V, GNDA = GNDD = PGND = 0V, V_{OUT} = PV_{OUT} = 3.3V, 100mA I_{PEAK} setting, unless otherwise noted.

Input Quiescent Current in Shutdown vs BAT



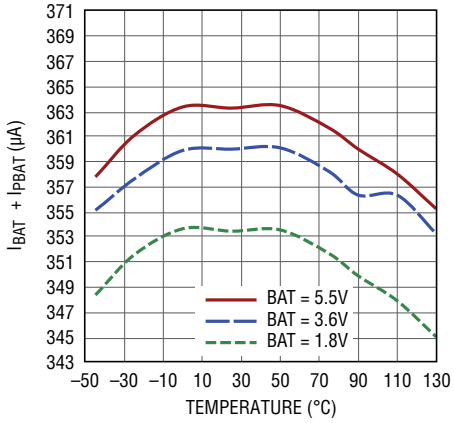
3335 G01

Input Quiescent Current in Sleep vs BAT



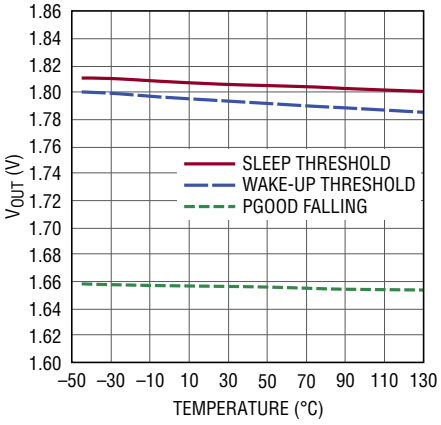
3335 G02

Input Quiescent Current (Active) vs Temperature



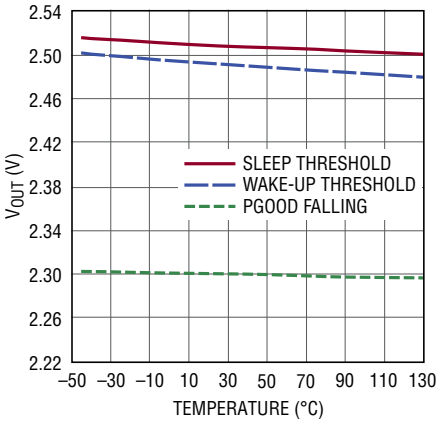
3335 G03

1.8V Output vs Temperature



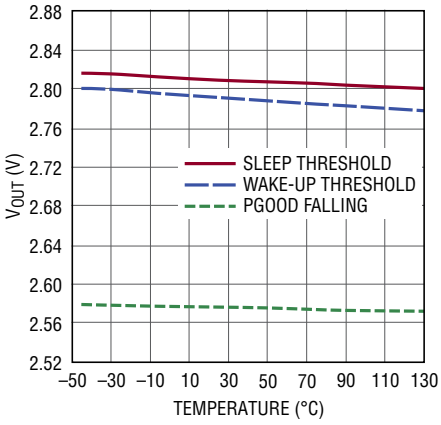
3335 G04

2.5V Output vs Temperature



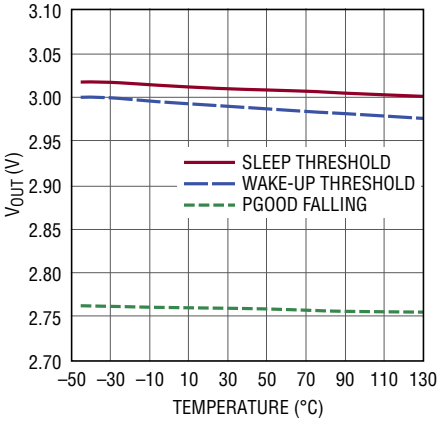
3335 G05

2.8V Output vs Temperature



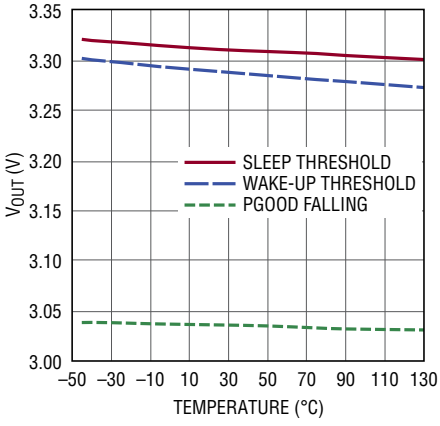
3335 G06

3V Output vs Temperature



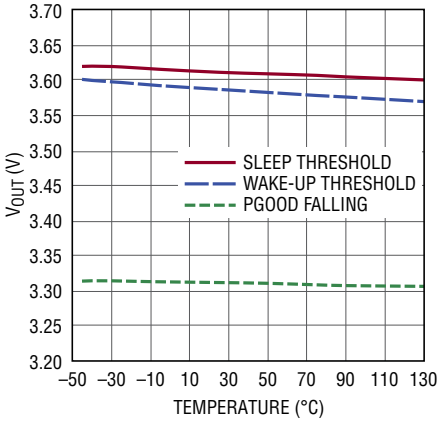
3335 G07

3.3V Output vs Temperature



3335 G08

3.6V Output vs Temperature

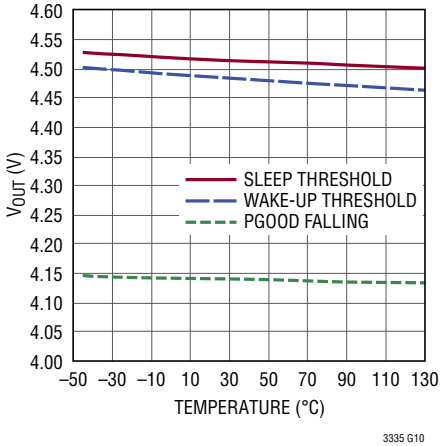


3335 G09

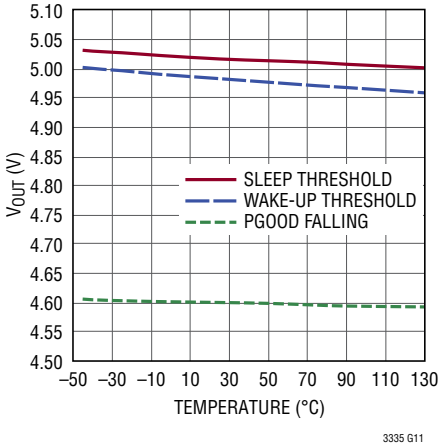
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, BAT = PBAT = 3.6V, GNDA = GNDD = PGND = 0V, V_{OUT} = PV_{OUT} = 3.3V, 100mA I_{PEAK} setting, unless otherwise noted.

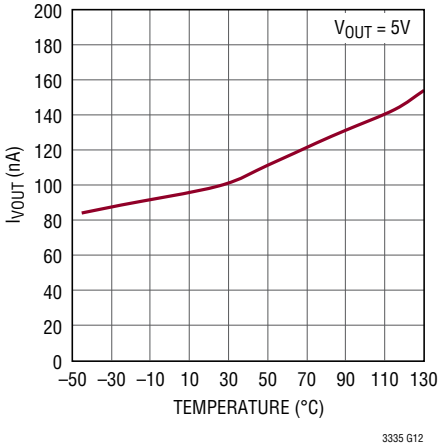
4.5V Output vs Temperature



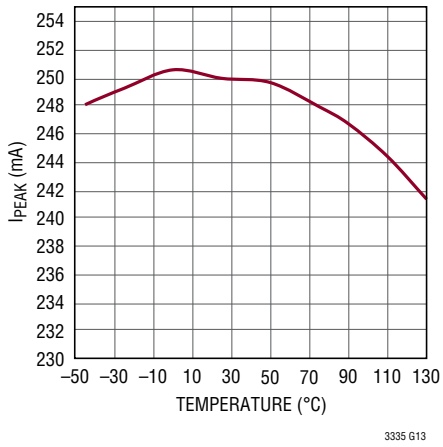
5V Output vs Temperature



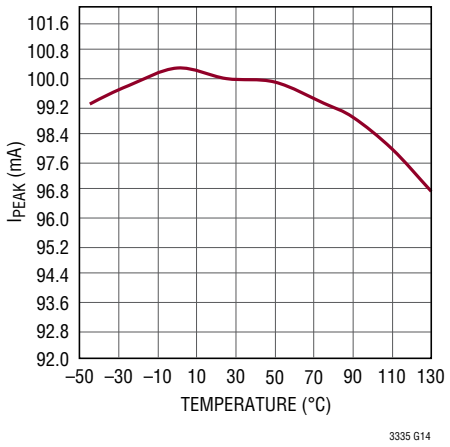
I_{VOUT} vs Temperature



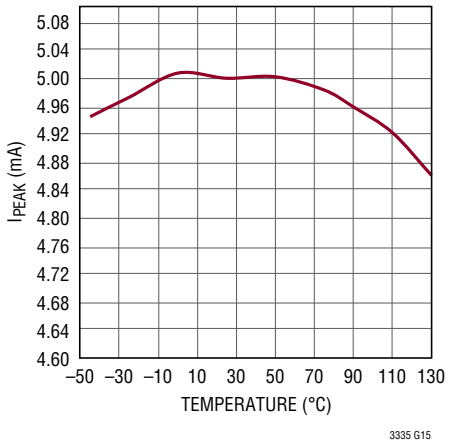
I_{PEAK} vs Temperature, 250mA Setting



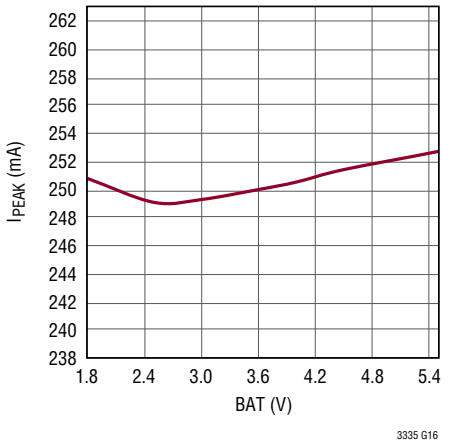
I_{PEAK} vs Temperature, 100mA Setting



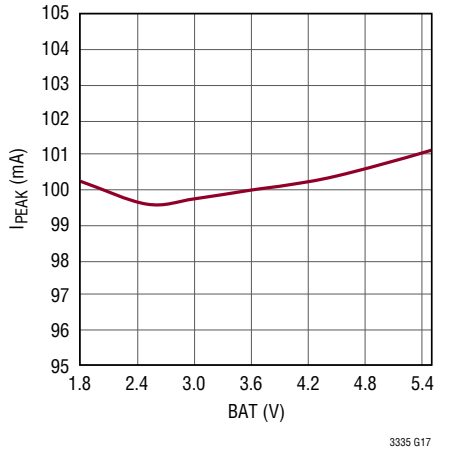
I_{PEAK} vs Temperature, 5mA Setting



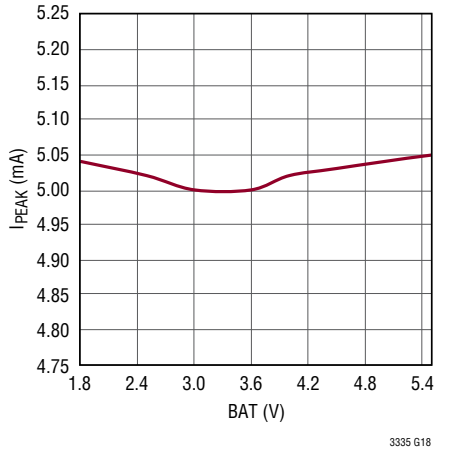
I_{PEAK} vs BAT, 250mA Setting



I_{PEAK} vs BAT, 100mA Setting



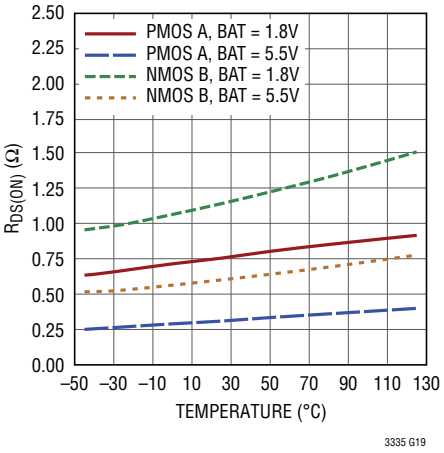
I_{PEAK} vs BAT, 5mA Setting



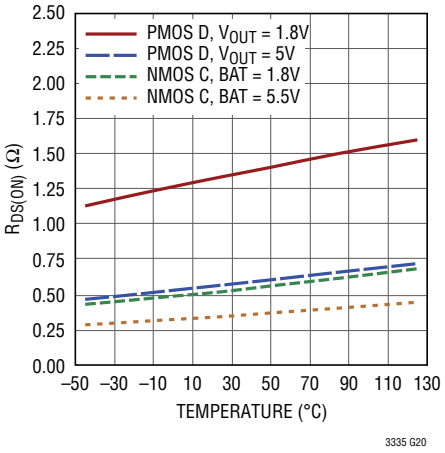
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, BAT = PBAT = 3.6V, GNDA = GNDD = PGND = 0V, V_{OUT} = PV_{OUT} = 3.3V, 100mA I_{PEAK} setting, unless otherwise noted.

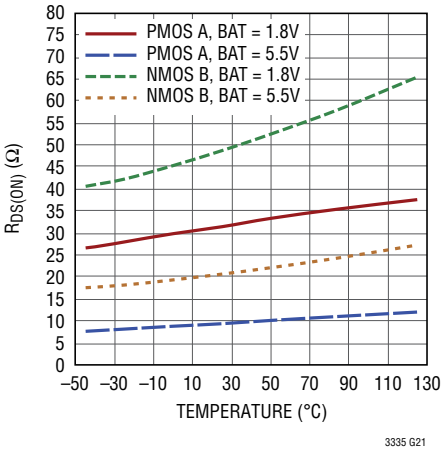
$R_{DS(ON)}$ vs Temperature, 250mA Setting



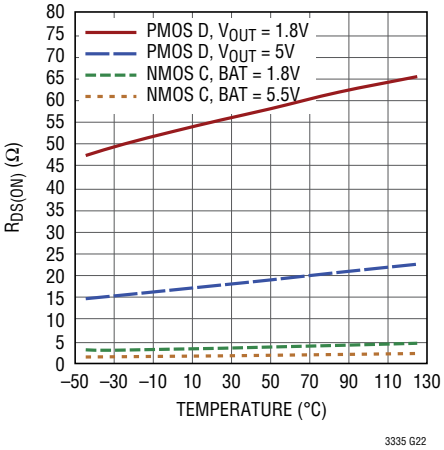
$R_{DS(ON)}$ vs Temperature, 250mA Setting



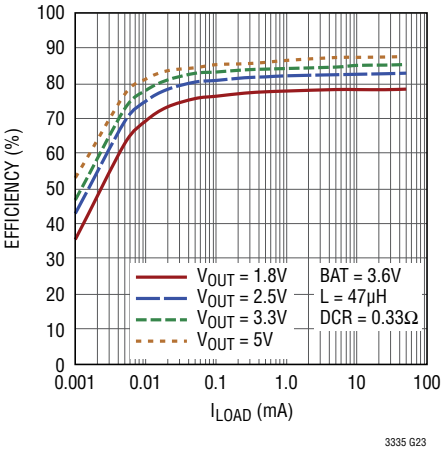
$R_{DS(ON)}$ vs Temperature, 5mA Setting



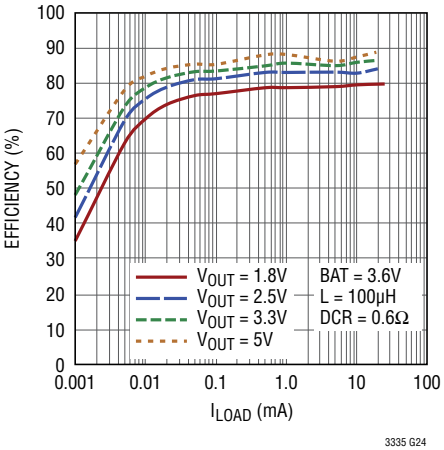
$R_{DS(ON)}$ vs Temperature, 5mA Setting



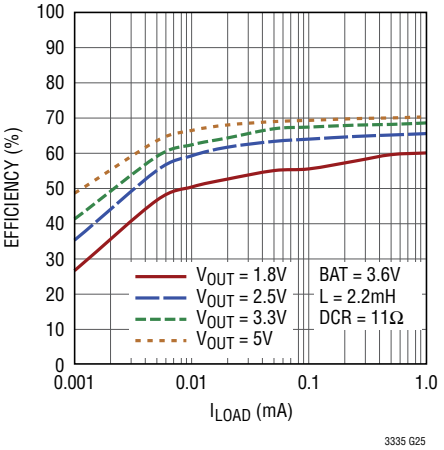
Efficiency vs Load Current for 250mA I_{PEAK} Setting



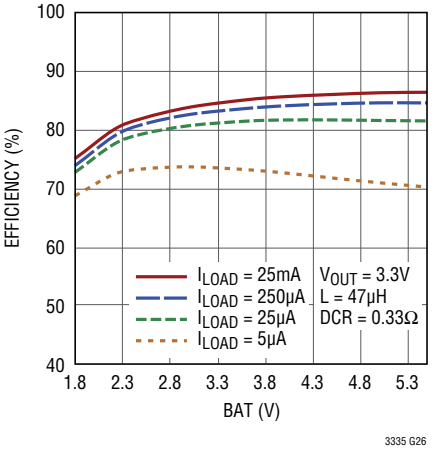
Efficiency vs Load Current for 100mA I_{PEAK} Setting



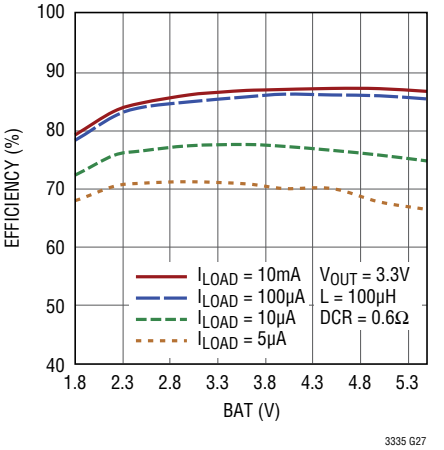
Efficiency vs Load Current for 5mA I_{PEAK} Setting



Efficiency vs BAT for 250mA I_{PEAK} Setting



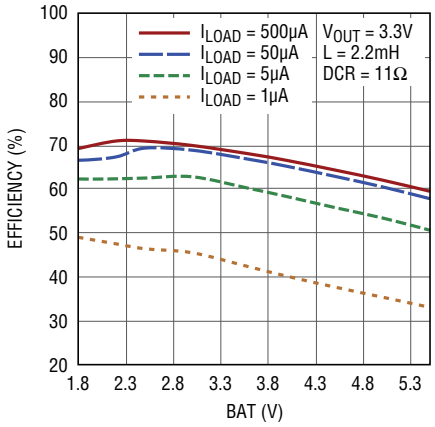
Efficiency vs BAT for 100mA I_{PEAK} Setting



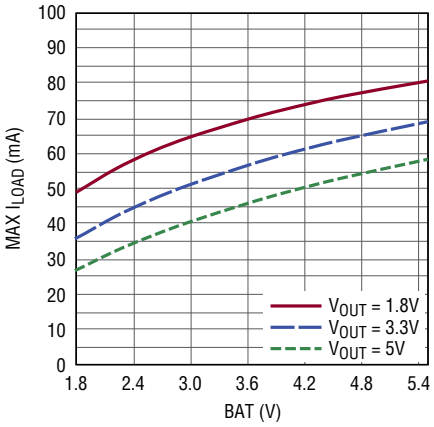
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, BAT = PBAT = 3.6V, GNDA = GNDD = PGND = 0V, V_{OUT} = PV_{OUT} = 3.3V, 100mA I_{PEAK} setting, unless otherwise noted.

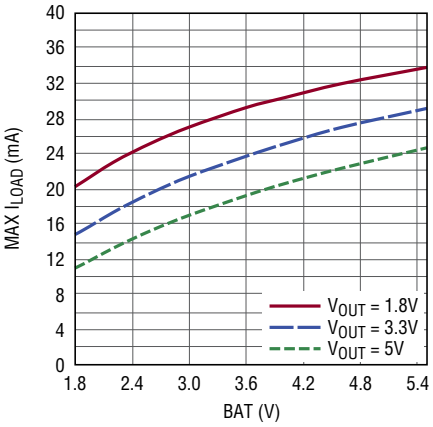
Efficiency vs BAT for 5mA I_{PEAK} Setting



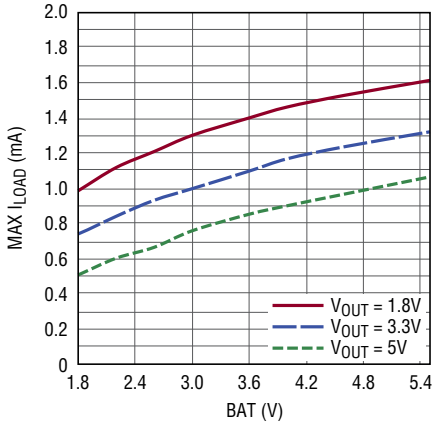
Buck-Boost Maximum Load vs BAT for 250mA I_{PEAK} Setting



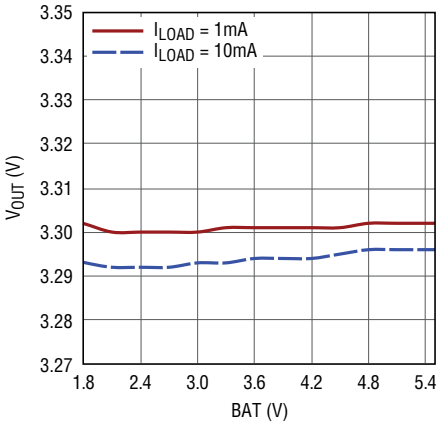
Buck-Boost Maximum Load vs BAT for 100mA I_{PEAK} Setting



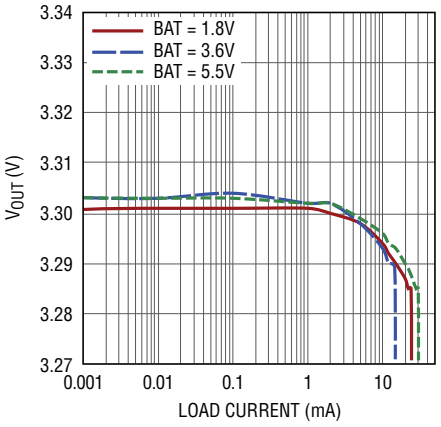
Buck-Boost Maximum Load vs BAT for 5mA I_{PEAK} Setting



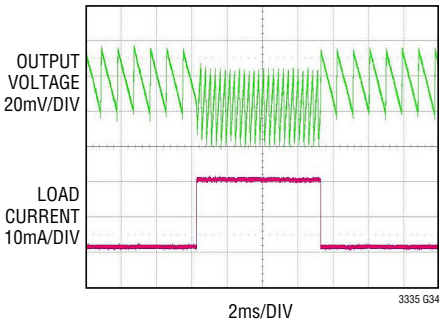
Buck-Boost Line Regulation, V_{OUT} = 3.3V, 100mA I_{PEAK} Setting



Buck-Boost Load Regulation, V_{OUT} = 3.3V, 100mA I_{PEAK} Setting

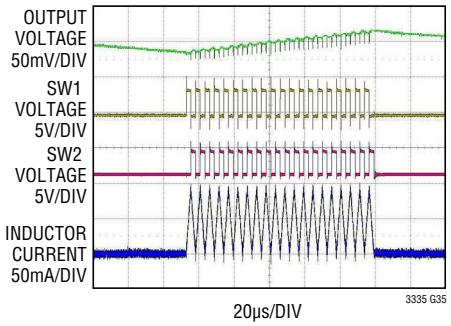


Buck-Boost Load Step Transient



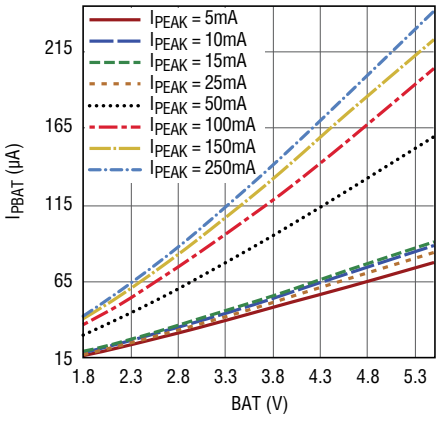
BAT = 3.6V, V_{OUT} = 3.3V
C_{OUT} = 47µF, L = 100µH
100mA I_{PEAK} SETTING
LOAD STEP FROM 1mA TO 20mA

Buck-Boost Switching Waveforms



BAT = 3.6V, V_{OUT} = 3.3V
C_{OUT} = 100µF, L = 100µH
100mA I_{PEAK} SETTING
I_{LOAD} = 10mA

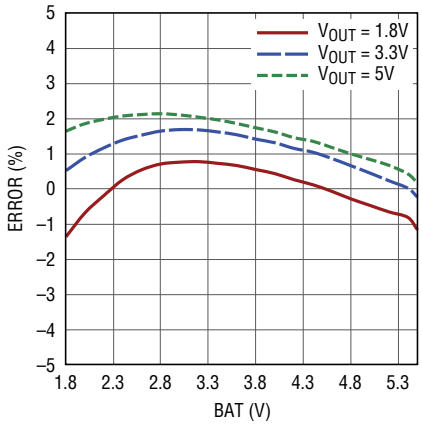
Input Quiescent Current Into PBAT Due to Gate Charge, V_{OUT} = 3.3V, Running Continuous



TYPICAL PERFORMANCE CHARACTERISTICS

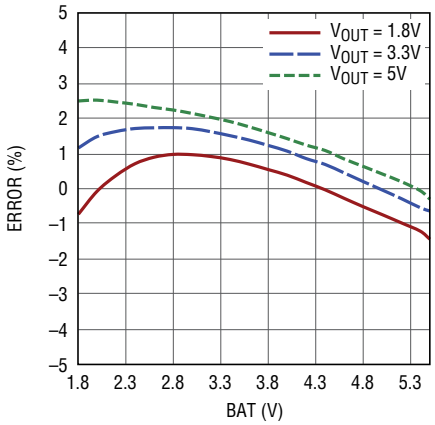
T_A = 25°C, BAT = PBAT = 3.6V, GNDA = GNDD = PGND = 0V, V_{OUT} = PV_{OUT} = 3.3V, 100mA I_{PEAK} setting, unless otherwise noted.

Total Unadjusted Coulomb Counter Error During Continuous Switching (250mA I_{PEAK} Setting)



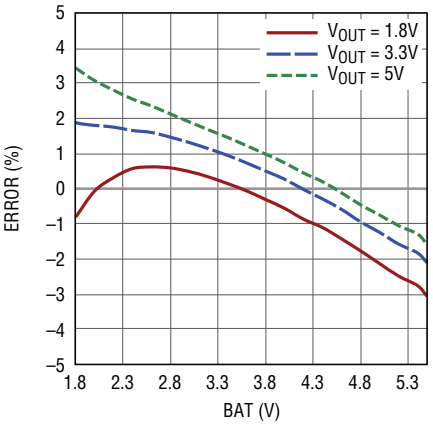
3335 G37

Total Unadjusted Coulomb Counter Error During Continuous Switching (150mA I_{PEAK} Setting)



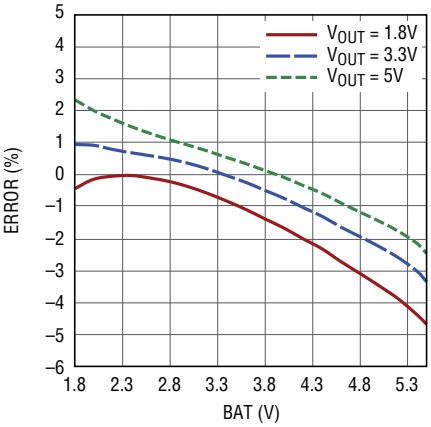
3335 G38

Total Unadjusted Coulomb Counter Error During Continuous Switching (100mA I_{PEAK} Setting)



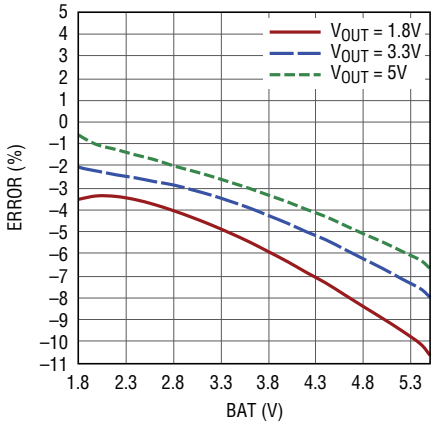
3335 G39

Total Unadjusted Coulomb Counter Error During Continuous Switching (50mA I_{PEAK} Setting)



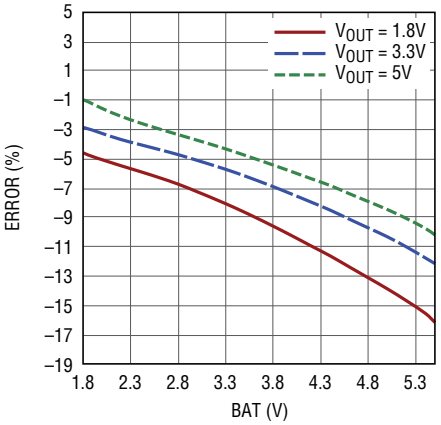
3335 G40

Total Unadjusted Coulomb Counter Error During Continuous Switching (25mA I_{PEAK} Setting)



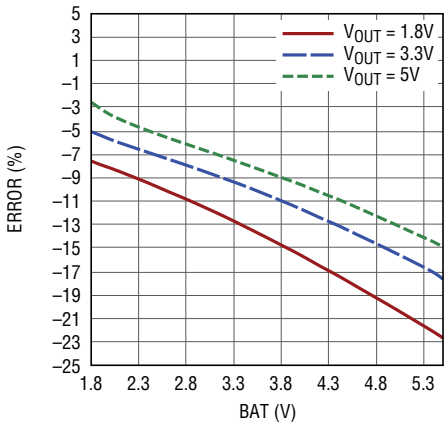
3335 G41

Total Unadjusted Coulomb Counter Error During Continuous Switching (15mA I_{PEAK} Setting)



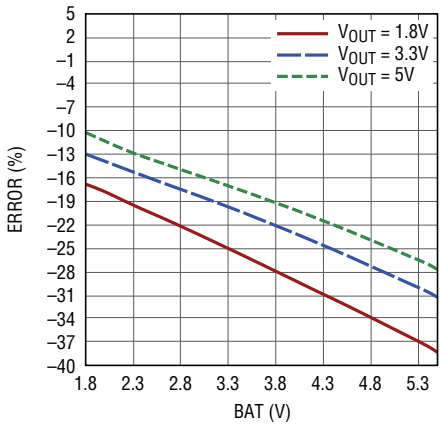
3335 G42

Total Unadjusted Coulomb Counter Error During Continuous Switching (10mA I_{PEAK} Setting)



3335 G43

Total Unadjusted Coulomb Counter Error During Continuous Switching(5mA I_{PEAK} Setting)



3335 G44

PIN FUNCTIONS

SDA (Pin 1): Serial Data Input/Output for the I^2C Serial Port. The I^2C input levels are scaled with respect to DV_{CC} for I^2C compliance. Do not float.

DV_{CC} (Pin 2): Supply Rail for the I^2C Serial Bus. DV_{CC} sets the reference level of the SDA and SCL pins for I^2C compliance. The external I^2C pull-up resistors on SDA and SCL should connect to DV_{CC}. Depending on the particular application, DV_{CC} can be connected to BAT, to V_{OUT}, or to a separate external supply between 1.8V and 5.5V. In most applications DV_{CC} will be connected to the I/O rail of the microprocessor reading the I^2C registers.

OUT[2:0] (Pin 3, 4, 5): V_{OUT} Voltage Select Bits. Tie high to BAT or low to GNDA to select the desired V_{OUT} (see Table 2). Do not float.

GNDD (Pin 6): Signal ground for internal digital circuits. Connect to GNDA and PGND.

BAT (Pin 7): Buck-Boost Input Voltage Sense Pin. Connect to PBAT.

PBAT (Pin 8): Buck-Boost Input Voltage. This pin is the power input of the regulator. Connect to BAT.

SW1 (Pin 9): Buck-Boost Switch Pin. Connected to internal power switches A and B. Connect an inductor (value in Table 8) between this node and SW2.

SW2 (Pin 10): Buck-Boost Switch Pin. Connected to internal power switches C and D. Connect an inductor (value in Table 8) between this node and SW1.

PV_{OUT} (Pin 11): Buck-Boost Output Voltage. This pin is the power output of the regulator. Connect to V_{OUT}.

V_{OUT} (Pin 12): Buck-Boost Output Voltage Sense Pin. Connect to PV_{OUT}.

IPK[2:0] (Pin 15, 14, 13): Peak Input Current Select Bits. Tie high to BAT or low to GNDA to select desired I_{PEAK} (see Table 1). Do not float.

EN (Pin 16): Buck-Boost Enable Input. Tie high to BAT or low to GNDA to enable/disable the buck-boost. If EN is pulled low, the buck-boost is disabled but internal register contents are saved. Do not float.

GNDA (Pin 17): Signal ground for internal analog circuits. Connect to GNDD and PGND.

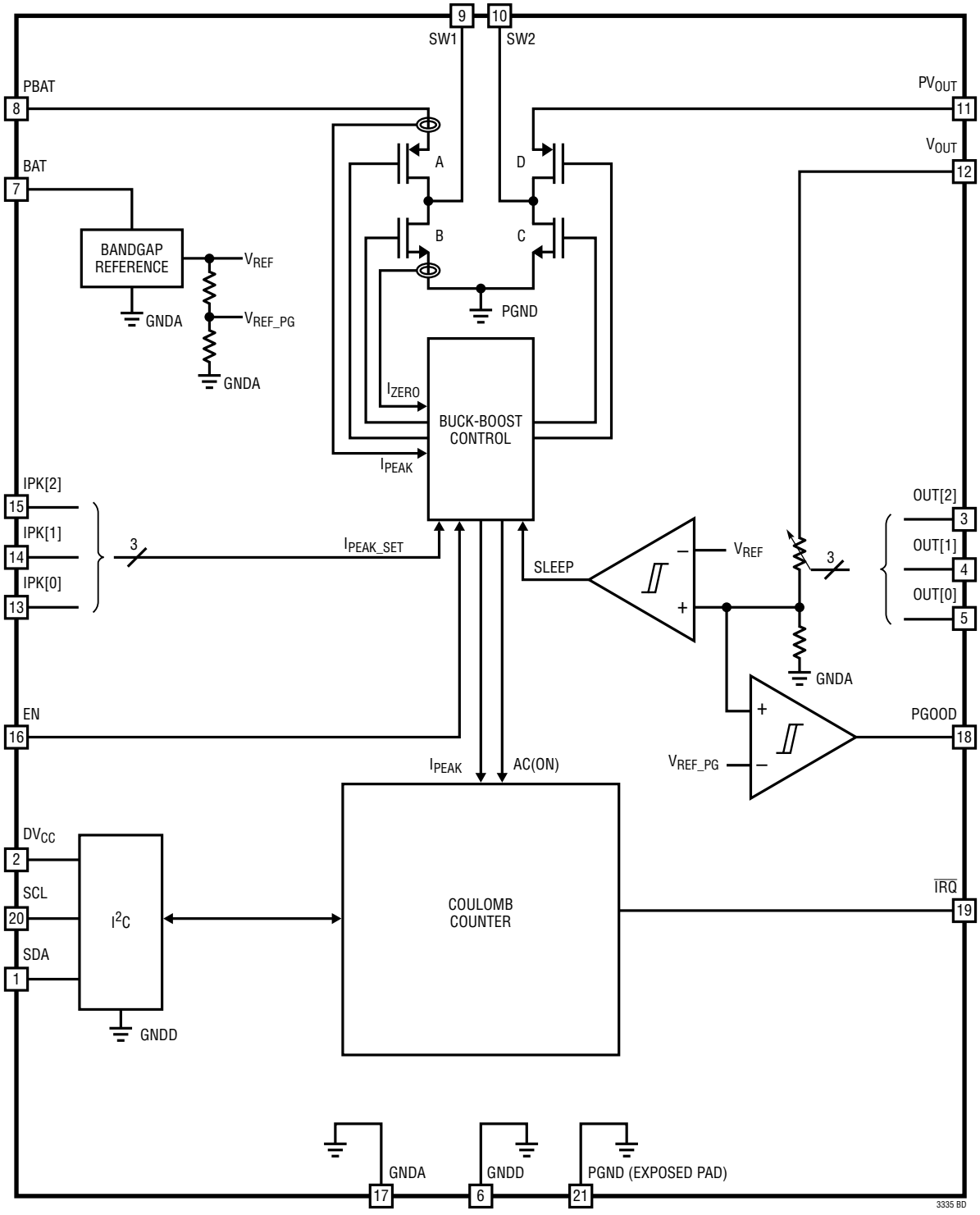
PGOOD (Pin 18): Power Good Output. Logic level output referenced to DV_{CC}. This output is pulled low after the buck-boost is enabled and remains low until V_{OUT} reaches regulation.

$\overline{IRQ}$ (Pin 19): Interrupt Output. Logic level output referenced to DV_{CC}. Active low. This pin is normally logic high but will transition low when the preset alarm level is reached or if there is an overflow in either the coulomb counter or the AC(ON) time measurement.

SCL (Pin 20): Serial Clock Input for the I^2C Serial Port. The I^2C input levels are scaled with respect to DV_{CC} for I^2C compliance. Do not float.

PGND (Exposed Pad Pin 21): Power Ground. The Exposed Pad connects to the sources of the internal N-channel power MOSFETs. It should be soldered to the PCB and electrically connected to system ground through the shortest and lowest impedance connection possible. Connect to GNDA and GNDD.

BLOCK DIAGRAM



OPERATION

Buck-Boost Regulator

The buck-boost regulator consists of four internal switches, labeled A, B, C, and D, as shown in Figure 2, and control circuitry which together connect the input and output voltages to the power inductor.

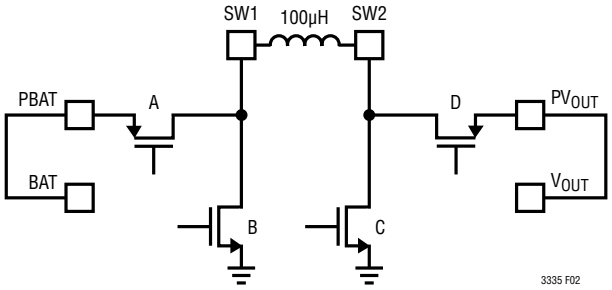


Figure 2. Power FETs

The buck-boost operates as an H-Bridge for all BAT and V_{OUT} conditions when not in sleep. This means that switches A and C are always on together, followed by switches B and D always on together. A hysteretic voltage algorithm is used to control the output through internal feedback from the V_{OUT} sense pin.

The buck-boost regulator charges the output capacitor through the inductor. Current is delivered first by ramping the inductor current up to I_{PEAK} through switches A and C, and then ramping it down to 0mA through switches B and D. The I_{PEAK} level is programmable via the IPK[2:0] pins and ranges from 5mA to 250mA (see Table 1).

Table 1. I_{PEAK} Selection

IPK2	IPK1	IPK0	I_{PEAK}
0	0	0	5mA
0	0	1	10mA
0	1	0	15mA
0	1	1	25mA
1	0	0	50mA
1	0	1	100mA
1	1	0	150mA
1	1	1	250mA

This cycle repeats until the output voltage rises to a value slightly higher than the regulation point (sleep threshold) after which the converter enters a low quiescent current sleep state that monitors the output voltage with a sleep comparator. During sleep, load current is provided by the output capacitor.

When the output voltage falls to a value slightly lower than the regulation point (wake-up threshold) the buck-boost regulator wakes up and then the inductor current starts ramping up again within 3µs (typical).

This hysteretic method of providing a regulated output voltage reduces losses associated with FET switching while regulating at light loads.

V_{OUT} can be set via the voltage select pins OUT[2:0] from 1.8V to 5V (see Table 2).

Table 2. Output Voltage Selection via Pins

OUT2	OUT1	OUT0	V_{OUT}
0	0	0	1.8V
0	0	1	2.5V
0	1	0	2.8V
0	1	1	3.0V
1	0	0	3.3V
1	0	1	3.6V
1	1	0	4.5V
1	1	1	5.0V

When the sleep comparator senses that the output voltage has reached the sleep threshold, the buck-boost converter may be in the middle of a cycle with current still flowing through the inductor. The converter enters the low quiescent current sleep state only at the end of a full AC-BD cycle after the inductor current reaches 0mA. This behavior is necessary for counting coulombs accurately.

During start-up and until V_{OUT} rises to approximately 1.2V, switch D is held off and its body diode conducts. This ensures proper I_{PEAK}/I_{ZERO} operation for coulomb counter accuracy.

OPERATION

V_{OUT} Power Good

A power good comparator is provided for the V_{OUT} output. The PGOOD pin transitions high when the LTC3335 first goes to sleep, indicating that V_{OUT} has reached regulation. It transitions low when V_{OUT} falls to 92% (typical) of its average value at regulation.

Coulomb Counter

The LTC3335 integrates a precision coulomb counter to monitor the accumulated charge that is transferred from the battery whenever the buck-boost converter is delivering current to V_{OUT}. The buck-boost converter operates as an H-Bridge for all BAT/V_{OUT} conditions when not in sleep (see Figure 3). Switches A and C turn ON at the beginning of each burst cycle. Inductor current ramps to I_{PEAK} and then switches A and C turn OFF. Switches B and D then turn ON until the inductor current ramps to zero (I_{ZERO}). This cycle repeats until V_{OUT} reaches the sleep threshold.

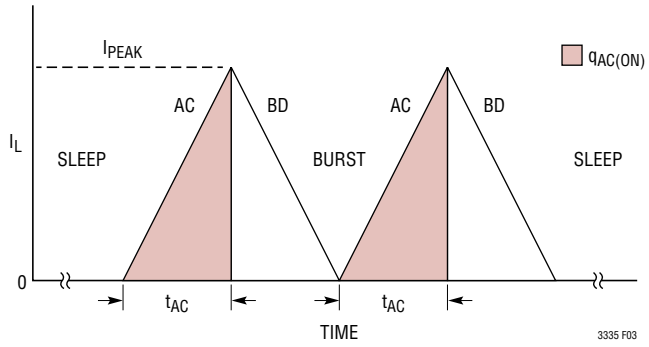


Figure 3

If I_{PEAK} and the switch AC(ON) time (t_{AC}) are both known, then the BAT discharge coulombs (shaded area in Figure 3) can be calculated by counting the number of AC(ON) cycles and multiplying by the charge per AC(ON) cycle given in Formula (1) below:

$$q_{AC(ON)} = \frac{I_{PEAK} \bullet t_{AC}}{2} \quad (1)$$

When the buck-boost is operating, the LTC3335 measures the actual AC(ON) time relative to a full scale ON time (t_{FS}, approximately 11.74µs) which is internally adjusted to compensate for differences between the actual I_{PEAK} value and the ideal I_{PEAK} value due to supply, temperature, and process variations. This results in a very accurate "measurement" of the charge transferred from the battery during each AC(ON) cycle which is represented as an 8-bit number and then added to the previous accumulated total coulomb count each time switches A and C turn on. The adder carry bit is the clock for the remaining 42-bit ripple counter. When the buck-boost is in sleep, the coulomb counter holds its state and draws no current.

There are a total of 50 bits in the coulomb counter chain, but only the 8 MSBs may be read back over I²C. These bits are contained in register C, the accumulated charge register. The amount of charge represented by the least significant bit (q_{LSB}) of the accumulated charge register (Register C) is given in the Electrical Characteristics section for all 8 I_{PEAK} settings for the case of the default prescaler setting (M = 0, which uses the full length of the internal counter). See Choosing Coulomb Counter Prescaler M section for instructions on calculating q_{LSB} with a nonzero prescaler setting.

I²C Interface

The 7-bit hard-wired I²C address of the LTC3335 is 1100100[R/$\overline{W}$]. The LTC3335 is a slave-only device meaning that the serial clock line (SCL) is only an input while the serial data line (SDA) is bidirectional.

Internal Registers

The LTC3335 has 5 internal subaddressed I²C registers, as shown in Table 3. Registers A, B, and E are write only, Register C is read/write, and Register D is read only, as shown in Tables 4, 5, and 6, respectively.

Table 3. Register Map

SUB ADDRESS	REGISTER NAME	REGISTER DESCRIPTION	R/W	DEFAULT
01h	A	V_{OUT} selection and prescaler selection	W	00h
02h	B	Alarm threshold	W	FFh
03h	C	Accumulated charge	R/W	00h
04h	D	Alarms	R	00h
05h	E	Interrupt register	W	00h

R = read, W = write

OPERATION

Table 4. Write Registers A, B, and E

BIT	NAME	OPERATION	DEFAULT
A[3:0]	Prescaler Bits	Set coulomb counter prescaling factor M from 0 to 15	0000
A[7:4]	V_{OUT} Selection	Selection of output voltage	0000
B[7:0]	Alarm Level	Coulomb count alarm level threshold calculated by the user based on battery capacity and I_{PEAK} current	11111111
E[0]	Clear_Int	Clear interrupt (Alarm reset)	0
E[1]	Counter Test	Counter check using $\overline{IRQ}$ pin	0
E[7:2]	Not Used		

Table 5. Read/Write Register C

BIT	NAME	OPERATION	DEFAULT
C[7:0]	Accumulated Charge	Read back 8 MSBs of counter data	00000000

Table 6. Read Register D

BIT	NAME	OPERATION	DEFAULT
D[0]	AC(ON) Time Overflow	AC(ON) time operating fault ($t_{AC} > t_{FS}$) due to improperly chosen inductor value timing out the AC(ON) measurement	0
D[1]	Coulomb Counter Overflow	Coulomb counter operating fault due to an improperly chosen prescaler causing the ripple counter to overflow	0
D[2]	Alarm Trip	Accumulator Register C value has met or exceeded the Alarm threshold set in Register B	0
D[7:3]	Not Used		00000

Output Voltage Setting Via I²C

Selection of the output voltage can be done not only via pins OUT[2:0], but also via I²C (see Table 7). The user can change the V_{OUT} settings dynamically by writing to register A. Note that bit A[7] must be set to 1 for bits A[6:4] to take effect.

Table 7. V_{OUT} Selection Bits

BIT	SET	DESCRIPTION
A[4]	0/1	Overwrite OUT0 Pin
A[5]	0/1	Overwrite OUT1 Pin
A[6]	0/1	Overwrite OUT2 Pin
A[7]	1	Must be 1 to set output voltage via I²C

Choosing Coulomb Counter Prescaler M

To preserve digital resolution for a wide range of battery capacities and peak current values, the LTC3335 includes a programmable prescaler. The user can set the prescaler value from 0 to 15 by writing bits A[3:0]. The default value for the prescaler is 0.

To use the majority of the range of Accumulated Charge Register C, the prescaler factor (M) should be chosen for a given battery capacity Q_{BAT} based on Formula (2):

$$M = \log_2\left(\frac{q_{LSB} \bullet 255}{Q_{BAT}}\right) \quad (2)$$

where Q_{BAT} is the battery size in A • hr and q_{LSB} is the typical value (for M=0) from the Electrical Characteristics table for the selected I_{PEAK}. M must be an integer, so the result of Formula (2) must be rounded down to the next integer value. M has a maximum value of 15.

A smaller capacity battery will require a higher prescaler factor M than a larger capacity battery for the same I_{PEAK}. Likewise, a lower I_{PEAK} will require a higher prescaler factor M than a higher I_{PEAK} for the same capacity battery.

The amount of charge represented by the least significant bit (q_{LSB_M}) of the accumulated charge register is given by:

$$q_{LSB\_M} = \frac{q_{LSB}}{2^M} \quad (3)$$

where q_{LSB} is the typical value in Electrical Characteristics table for the selected I_{PEAK}.

Counter Check Test

Setting the bit E[1] = 1 allows the user to verify that the coulomb counter is operating correctly without having to wait for the accumulated charge register to increment from 00000000. In this mode the input clock of the ripple counter is output to the $\overline{IRQ}$ pin, and the frequency of switching seen at the $\overline{IRQ}$ pin will increase with output load.

OPERATION

Alarm

An alarm causes the $\overline{IRQ}$ pin to be pulled low. The user can read register D to determine what caused the alarm. The alarm can then be cleared by writing 1 to bit E[0]. The clear interrupt bit is self-clearing after taking action on the $\overline{IRQ}$ pin.

When clearing an alarm, if another alarm trips, the $\overline{IRQ}$ pin will go high for 1µs (typical) before returning low again. During this time, the clear interrupt bit E[0] is also reset to zero.

There are 3 different fault/alarm conditions:

1) An AC(ON) time overflow (D[0] is high) due to an improperly chosen inductor value timing out the AC(ON) time measurement. After the alarm is cleared the $\overline{IRQ}$ pin goes high and stays high at least until the next AC(ON) pulse is measured. A different inductor or I_{PEAK} setting needs to be chosen to keep the alarm from continuously tripping.

2) A coulomb counter overflow (D[1] is high) due to an improperly chosen prescaler value causing the ripple counter to overflow. After the alarm is cleared the $\overline{IRQ}$ pin is released for 1µs and later pulled low again unless register C is overwritten with a lower value and the prescaler is changed.

3) The preset alarm level is reached (D[2] is high) when the 8 MSBs of the ripple counter are equal to or higher than the 8 bits in register B. The user should increase the alarm threshold in register B and then write bit E[0] to 1 to clear the alarm.

   The alarm threshold is only checked after each AC(ON) pulse or when a write to register C is done via I^2C. Therefore, if bit E[0] is set to 1 to clear an alarm interrupt without also changing the contents of register B and/or C, and this occurs during a long sleep time, the $\overline{IRQ}$ pin is cleared and doesn't go back low again until the next AC(ON) pulse.

Power Up Sequence

When the battery is first inserted and the internal circuits are powering up, the LTC3335 resets all registers to their default states, including the adder and the ripple counter. The buck-boost requires a finite start up time until V_{OUT} charges up to the target value. When V_{OUT} reaches the PGOOD threshold, the PGOOD pin goes high. During the entire start-up sequence, the coulomb counter counts correctly.

If the EN pin is pulled low, the buck-boost is disabled. However, the digital register contents of the coulomb counter remain saved in memory. When re-enabled, the coulomb counter continues counting from where it left off. The digital registers are reset only if the BAT voltage is lost.

DV_{CC} I^2C Power Supply

The DV_{CC} pin can be connected to BAT, to V_{OUT}, or to a separate external supply between 1.8V and 5.5V. A power-on-reset circuit monitors the DV_{CC} supply. For DV_{CC} voltages below 1.3V (typical), the I^2C interface is disabled. The user can't read or write, but the coulomb counter is still fully functional.

If the BAT voltage is lost, the coulomb counter and the buck-boost are switched off and the contents of all digital registers are lost. The full functionality of the coulomb counter is guaranteed for BAT voltages equal to or greater than 1.8V.

If DV_{CC} is connected to V_{OUT} or to a separate external supply, the coulomb counter is still fully functional, even if V_{OUT} = 0V such as during startup.

For the external pull-up resistors on the SDA and SCL pins, 10kΩ is recommended.

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Input/Output Capacitor Selection

The input capacitor for the buck-boost on the BAT pin should be bypassed with at least 4.7µF to GND. In cases where the series resistance of the battery is high, a larger capacitor may be desired to handle transients.

A larger capacitor may also be necessary when operating close to 1.8V at higher I_{PEAK} settings to prevent the battery voltage from falling below 1.8V when the buck-boost is switching.

The duration for which the buck-boost regulator sleeps depends on the load current and the size of the V_{OUT} capacitor. The sleep time decreases as the load current increases and/or as the output capacitor decreases. The DC sleep hysteresis window is ±6mV for the 1.8V output setting and scales linearly with the output voltage setting (±12mV for the 3.6V setting, etc.). Ideally this means that the sleep time is determined by the following equation:

$$t_{SLEEP} = C_{OUT} \bullet \frac{V_{DC\_HYS}}{I_{LOAD}} \quad (4)$$

This is true for output capacitance on the order of 100µF or larger, but as the output capacitance decreases towards 10µF, delays in the internal sleep comparator along with the load current itself may result in the V_{OUT} voltage slewing past the DC thresholds. This will lengthen the sleep time and increase V_{OUT} ripple. An output capacitance less than 22µF is not recommended as V_{OUT} ripple could increase to an undesirable level.

If transient load currents higher than the maximum deliverable are required, then a larger capacitor should be used at the output. This capacitor will be continuously discharged during a load condition and the capacitor can be sized for an acceptable drop in V_{OUT}:

$$C_{OUT} = t_{LOAD} \bullet \frac{I_{LOAD} - I_{DC/DC}}{V_{OUT}^{+} - V_{OUT}^{-}} \quad (5)$$

Here V_{OUT}^{+} is the value of V_{OUT} when PGOOD goes high and V_{OUT}^{-} is the desired lower limit of V_{OUT}. $I_{DC/DC}$ is the average current being delivered from the buck-boost converter, and t_{LOAD} is the duration of the transient load.

The LTC3335 always operates as an H-bridge, even at start-up. The start-up duration is dependent on the load current and the output capacitor; a larger output capacitor makes the start-up time longer.

A standard surface mount ceramic capacitor can be used for C_{OUT}. Some applications, however, may benefit from a low leakage aluminum electrolytic capacitor or a supercapacitor. These capacitors can be obtained from manufacturers such as Vishay, Illinois Capacitor, AVX, or CAP-XX.

Inductor Selection

The AC(ON) and BD(ON) times are determined to first order by BAT, V_{OUT}, the inductor value, and the I_{PEAK} current setting.

$$AC(ON) = \frac{I_{PEAK} \bullet L}{BAT} \quad (6)$$

$$BD(ON) = \frac{I_{PEAK} \bullet L}{V_{OUT}} \quad (7)$$

The buck-boost is designed to work with a 100µH inductor for typical applications using the 100mA peak current setting.

For the other seven I_{PEAK} settings the inductor value should scale so as to keep the I_{PEAK} • L product approximately constant. This maintains on-times required for accurate coulomb counter operation. The nominal recommended inductor value (L_{REC}) for each I_{PEAK} setting is given in Table 8.

Table 8. Recommended Inductor Value L_{REC} vs I_{PEAK}

I_{PEAK} SETTING (mA)	L_{REC} (µH)
5	2200
10	1000
15	680
25	470
50	220
100	100
150	68
250	47

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Higher value inductors provide the benefit of lower switching losses by increasing both AC(ON) and BD(ON). However, care must be taken so that AC(ON) never exceeds the max full-scale time t_{FS} (11.74µs).

Recommended inductor values from Table 8 assure that for BAT from 1.8V to 5.5V, V_{OUT} from 1.8V to 5V, and ±20% inductor variation, the AC(ON) time is always below 11.74µs.

If in the application the minimum BAT voltage is higher than 1.8V, the inductor value can be increased using the formula below:

$$L_{MAX} = \frac{BAT_{MIN} \bullet L_{REC}}{1.8} \quad (8)$$

where L_{MAX} is the maximum inductor value (including production tolerance), L_{REC} is the inductor value from Table 8 and BAT_{MIN} is the minimum BAT voltage used in the application. Inductors typically have production tolerances of ±20%.

The DCR of the inductor can have an impact on efficiency as it is a source of loss. In addition it is a source of error for the coulomb counter because it increases the nonlinearity of the inductor current during the AC(ON) time.

Choose an inductor with an I_{SAT} rating at least 50% greater than the selected I_{PEAK} value. Table 9 lists several inductors that work well. Trade-offs between price, size, and DCR should be evaluated.

Load Current Capability

The maximum load current the buck-boost can support depends on the I_{PEAK} setting, the BAT voltage, and the V_{OUT} voltage and is ideally given by:

$$I_{LOAD(MAX)} = \frac{I_{PEAK}}{2} \bullet \frac{BAT}{BAT + V_{OUT}} \quad (9)$$

However, due to finite $R_{DS(ON)}$ of power FETs A, B, C, and D, as well as inductor DCR, the maximum deliverable current is actually lower. Refer to the curves given in the Typical Performance Characteristics section for actual load current capability under various conditions.

Coulomb Counter Errors

The battery discharge coulombs is calculated by counting the number of AC(ON) cycles and multiplying by the number of coulombs per AC(ON) time given by the following formula:

$$q_{AC(ON)} = \frac{I_{PEAK} \bullet t_{AC}}{2} \quad (10)$$

This formula assumes that the LTC3335 input quiescent current, gate charge current, $R_{DS(ON)}$ of the power switches, and the inductor DCR have negligible effect. It also assumes that every pulse starts from an inductor current equal to 0 and ends at I_{PEAK}. The contribution of each of these errors will be discussed in the following sections.

Input Quiescent Current Error

The control circuit of the buck-boost consumes DC quiescent current when not in sleep. This current is dependent on BAT voltage and temperature as shown in the Typical Performance Characteristics section. This current, (typically 360µA) generates a small error at the 250mA peak current setting, but can be significant for lower peak current settings as shown in Figures 4 and 5.

When the buck-boost is sleeping, the DC quiescent current is typically 680nA. This equates to an error of 5.96mA • hr per year of cumulative sleep time. For a battery capacity of 18.3A • hr, the error is only 0.033% per year.

As shown in Figure 6, for load currents smaller than approximately 100µA, the sleep current can result in a significant error.

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Table 9. Recommended Inductors for the LTC3335

MANUFACTURER	PART FAMILY	L (µH)	$I_{SAT(MAX)}$ (A)	DCR MAX (Ω)	WIDTH (mm)	LENGTH (mm)	HEIGHT (mm)
For 250mA I_{PEAK} Setting							
Coilcraft	LPS5030	47	0.55	0.33	5.51	5.51	2.9
Vishay	IDCS-2512	47	0.5	0.23	6.6	4.45	2.92
Sumida	CDRH4D29	47	0.36	0.239	5.1	5.1	3
Wurth	WE-TPC SMD 4828	47	0.5	0.28	4.8	4.8	2.8
For 150mA I_{PEAK} Setting							
Coilcraft	LPS5030	68	0.44	0.44	5.51	5.51	2.9
Vishay	IDCS-2512	68	0.4	0.29	6.6	4.45	2.92
Sumida	CDRH4D29	68	0.3	0.355	5.1	5.1	3
Wurth	WE-TPC SMD 4828	68	0.4	0.4	4.8	4.8	2.8
For 100mA I_{PEAK} Setting							
Coilcraft	LPS5030	100	0.32	0.6	5.51	5.51	2.9
Vishay	IDCS-2512	100	0.3	0.48	6.6	4.45	2.92
Sumida	CDRH4D29	100	0.24	0.523	5.1	5.1	3
Wurth	WE-TPC SMD 4828	100	0.29	0.6	4.8	4.8	2.8
For 50mA I_{PEAK} Setting							
Coilcraft	LPS5030	220	0.245	1.35	5.51	5.51	2.9
Vishay	IDCS-2512	220	0.22	0.77	6.6	4.45	2.92
Sumida	CDRH60D45	220	0.39	1.02	6.4	6.1	4.8
Wurth	WE-TPC SMD 4828	220	0.2	1.25	4.8	4.8	2.8
For 25mA I_{PEAK} Setting							
Coilcraft	LPS5030	470	0.146	2.8	5.51	5.51	2.9
Vishay	IDCS-2512	470	0.19	1.8	6.6	4.45	2.92
Sumida	CDMPIH58D28	470	0.14	3	6	6	3.2
Wurth	WE-TPC SMD 4828	470	0.125	2.6	4.8	4.8	2.8
For 15mA I_{PEAK} Setting							
Coilcraft	LPS5030	680	0.126	3.8	5.51	5.51	2.9
Vishay	IDCS-2512	680	0.18	2.2	6.6	4.45	2.92
Sumida	CDMPIH58D28	680	0.12	4.4	6	6	3.2
Wurth	WE-PD SMD 7332	680	0.22	5.73	7.3	7.3	3.2
For 10mA I_{PEAK} Setting							
Coilcraft	LPS5030	1000	0.11	5.1	5.51	5.51	2.9
Vishay	IDCS-2512	1000	0.15	3.4	6.6	4.45	2.92
Sumida	CDMPIH58D28	1000	0.09	6.6	6	6	3.2
Wurth	WE-TPC SMD 4828	1000	0.08	7	4.8	4.8	2.8
For 5mA I_{PEAK} Setting							
Coilcraft	LPS5030	2200	0.08	11	5.51	5.51	2.9
Vishay	IDCS-2512	2200	0.1	8.5	6.6	4.45	2.92
Sumida	CDMPIH58D28	2200	0.065	16.5	6	6	3.2
Wurth	WE-PD2 SMD 1054	2200	0.26	5.3	10	9	5.4

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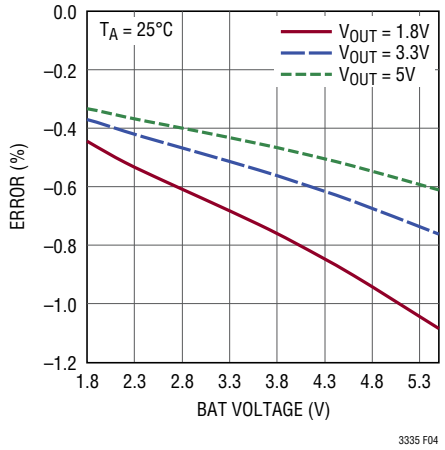

Figure 4. Typical Error Due to Input Quiescent Current for 250mA I_{PEAK} Setting

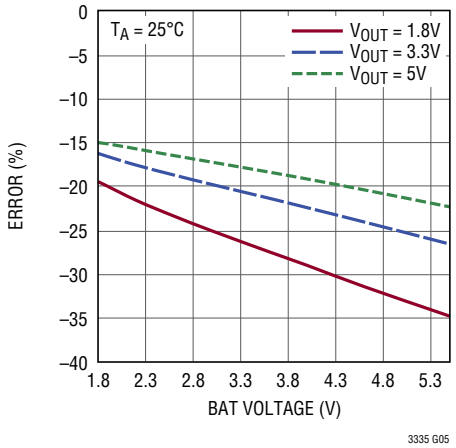

Figure 5. Typical Error Due to Input Quiescent Current for 5mA I_{PEAK} Setting

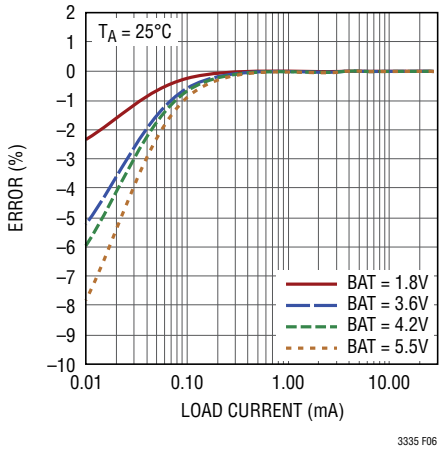

Figure 6. Typical Error Due to Sleep Current (250mA I_{PEAK} Setting, V_{OUT} = 3.3V)

Gate Charge Current Error

The gate charge current needed to turn on and off switches A, B, and C is also a source of error for the coulomb counter. This error increases at higher BAT voltages and is generally higher at low I_{PEAK} settings as shown in Figures 7, 8, and 9. Gate charge current for switch D is provided from the output and does not create an error.

Power Switches $R_{DS(ON)}$ Error

The battery discharge coulombs are calculated assuming that the inductor current rises to the I_{PEAK} setting value linearly. However, finite $R_{DS(ON)}$ of switches A and C cause the actual inductor current to bow slightly which creates an undercount in the coulomb counter (see Figure 10). This error increases at lower BAT voltages and at higher temperature.

Inductor DCR Error

An inductor with high DCR generates the same type of error as the power switches $R_{DS(ON)}$ error due to a similar nonlinear bowing of the inductor current waveform. Using the recommended inductors from Table 9 assures that the coulomb counter error due to the DCR is small.

Other Errors

Each of the individual coulomb counter error terms discussed above results in an undercount of the battery discharge coulombs (negative percent error). There are, however, other error terms which can contribute to an overcount of the battery discharge coulombs (positive percent error). For example, I_{ZERO} can be slightly negative under some conditions, and this results in a slight overcount. This particular error is more likely to occur at low BAT voltages, high I_{PEAK} settings, and/or high V_{OUT} voltages.

Total Coulomb Counter Error

The total unadjusted coulomb counter error curves in the Typical Performance Characteristics section show actual data taken from an actual circuit and include the effects of all of the above mentioned error sources with the exception of the sleep current error, as these curves were taken with continuous switching. The errors present

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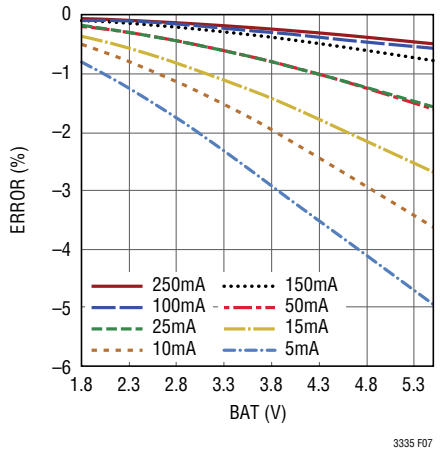

Figure 7. Typical Error Due to Gate Charge Current V_{OUT} = 1.8V, Ambient Temperature

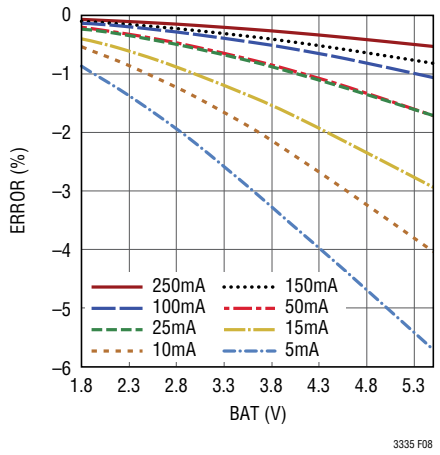

Figure 8. Typical Error Due to Gate Charge Current V_{OUT} = 3.3V, Ambient Temperature

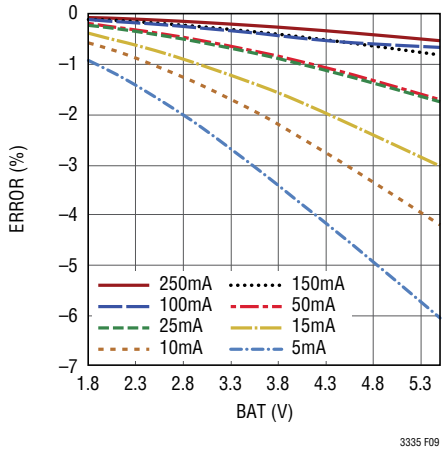

Figure 9. Typical Error Due to Gate Charge Current V_{OUT} = 5V, Ambient Temperature

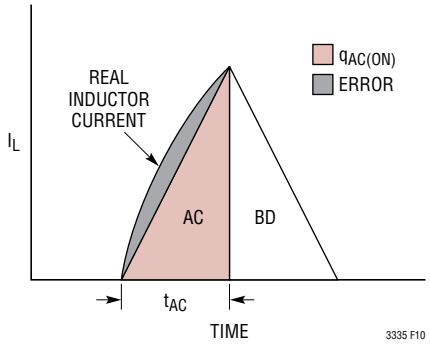

Figure 10.

during continuous switching are well-characterized for a given set of operating conditions and can to first order be compensated for by applying a multiplicative scale factor to the raw coulomb count reported by the LTC3335. The error due to the sleep current can then be compensated for by adding an offset term equal to the sleep current multiplied by the cumulative sleep time (or if not known, the battery service time). The error adjustment is given by the following formula:

Adjusted Coulomb Count = (Raw Coulomb Count) • [1/(1+Error)] + (5.96mA • hr) • Years/q_{LSB_M}

where Error is the error in % from Figures G37-G44 in the Typical Performance Characteristics, q_{LSB_M} is the least significant bit of the accumulated charge register for the chosen Prescaler M in A • hr, and Years is the number of years of cumulative battery service.

The following two examples further illustrate how to compensate for the raw coulomb count error.

Example 1: A Tadiran TL4903 primary cell (3.6V nominal, 2.4A • hr) is powering a 3.3V output and the I_{PEAK} setting is 100mA. The appropriate prescaler is M=8. From curve G39 in the Typical Performance Characteristics, the nominal error for continuous switching under these conditions is only +0.5%. The raw coulomb count C[7:0] read from the LTC3335 can be adjusted by multiplying by 1/(1+ 0.005). To this result, the error due to the sleep current (5.96mA • hr for each year of use) can be added, but this additional term corresponds to less than 0.25% of the battery's capacity per year of service. In this example, the difference between the raw and adjusted coulomb count is minimal.

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Example 2: A Panasonic CR2032 primary cell (3.0V nominal, 225mA • hr) is powering a 5V output and the I_{PEAK} setting is 5mA. The appropriate prescaler is M=7. From curve G44 in the Typical Performance Characteristics, the nominal error for continuous switching under these conditions is –16%. In this case the raw coulomb count error is significant if left unadjusted. Suppose after 6 months of battery service, the accumulated charge register C[7:0] reads 28h(hex) or 40(decimal). The adjusted coulomb count is given by:

Adjusted Coulomb Count = 40 • (1/(1 – 0.16) + (5.96mA • hr) • 0.5/(140.6mA • hr/2^7) = 51

The adjusted coulomb count will more accurately represent the actual coulombs and the preset alarm level (if used) can be appropriately adjusted to compensate for this:

Adjusted Alarm Set Count = [(Desired Alarm Level/100) • Q_{BAT}) - (5.96mA • hr • Years)] • (1 + Error/100) • 1/q_{LSB_M}

where Desired Alarm Level is the percentage of the battery capacity at which to trip the alarm.

I²C Interface

The LTC3335 communicates with a bus master using the standard I²C 2-wire serial interface. The Timing Diagram (Figure 1) shows the relationship of the signals on the bus. The two bus lines, SDA and SCL, must be HIGH when the bus is not in use. External pull-up resistors are required on these lines. The I²C control signals, SDA and SCL, are scaled internally to the DV_{CC} supply. DV_{CC} should be connected to the same power supply as the bus pull-up resistors.

The I²C port has an undervoltage lockout on the DV_{CC} pin. When DV_{CC} is below approximately 1.3V, the I²C serial port is disabled.

Bus Speed

The I²C port is designed to operate at speeds of up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I²C compliant master device. It also contains input filters designed to suppress glitches.

START and STOP Conditions

A bus master signals the beginning of communications by transmitting a START condition. A START condition is generated by transitioning SDA from HIGH to LOW while SCL is HIGH. The master may transmit either the slave write address or the slave read address. Once data is written to the LTC3335, the master may transmit a STOP condition which commands the LTC3335 to act upon its new command set. A STOP condition is sent by the master by transitioning SDA from LOW to HIGH while SCL is HIGH.

Byte Format

Each frame sent to or received from the LTC3335 must be eight bits long, followed by an extra clock cycle for the acknowledge bit. The data must be sent to the LTC3335 most significant bit (MSB) first.

Master and Slave Transmitters and Receivers

Devices connected to an I²C bus may be classified as either master or slave. A typical bus is composed of one or more master devices and a number of slave devices.

Some devices are capable of acting as either a master or a slave, but they may not change roles while a transaction is in progress.

The transmitter/receiver relationship is distinct from that of master and slave. The transmitter is responsible for control of the SDA line during the eight bit data portion of each frame. The receiver is responsible for control of SDA during the ninth and final acknowledge clock cycle of each frame.

All transactions are initiated by the master with a START or repeat START condition. The master controls the active (falling) edge of each clock pulse on SCL, regardless of its status as transmitter or receiver. The slave device never brings SCL LOW.

The LTC3335 does not clock stretch and will never hold SCL LOW under any circumstance.

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The master device begins each I²C transaction as the transmitter and the slave device begins each transaction as the receiver. For bus write operations, the master acts as the transmitter and the slave acts as receiver for the duration of the transaction. For bus read operations, the master and slave exchange transmit/receive roles following the address frame for the remainder of the transaction.

Acknowledge

The acknowledge signal (ACK) is used for handshaking between the transmitter and receiver. When the LTC3335 is written to, it acknowledges its write address as well as the subsequent data bytes as a slave receiver. When it is read from, the LTC3335 acknowledges its read address as a slave receiver. The LTC3335 then changes to a slave transmitter and the master receiver may optionally acknowledge receipt of the following data byte from the LTC3335.

The acknowledge related clock pulse is always generated by the bus master. The transmitter (master or slave) releases the SDA line (HIGH) during the acknowledge clock cycle.

The receiver (slave or master) pulls down the SDA line during the acknowledge clock pulse so that it is a stable LOW during the HIGH period of this clock pulse.

When the LTC3335 is read from, it releases the SDA line after the eighth data bit so that the master may acknowledge receipt of the data. The I²C specification calls for a not acknowledge (NACK) by the master receiver following the last data byte during a read transaction. Upon receipt of the NACK, the slave transmitter is instructed to release control of the bus. Because the LTC3335 only transmits one byte of data under any circumstance, a master acknowledging or not acknowledging the data sent by the LTC3335 has no consequence. The LTC3335 will release the bus in either case.

Slave Address

The LTC3335 responds to a 7-bit address which has been factory programmed to 1100100[R/$\overline{W}$]. The LSB of the address byte, known as the read/write bit, should be 0 when writing data to the LTC3335, and 1 when reading data from it. Considering the address an 8-bit word, then the write address is 0xC8, and the read address is 0xC9.

The LTC3335 will acknowledge both its read and write addresses.

Subaddressed Access

The LTC3335 has three write registers for control input, one read register for alarm reporting and one read/write register for the accumulated battery discharge. They are accessed by the I²C port via a subaddressed pointer system where each subaddress value points to one of the five control or status registers within the LTC3335. See Table 3 for subaddress information.

The subaddress pointer is always the first byte written immediately following the LTC3335 write address during bus write operations. The subaddress pointer value persists after the bus write operation and will determine which data byte is returned by the LTC3335 during any subsequent bus read operations.

Bus Write Operation

The bus master initiates communication with the LTC3335 with a START condition and the LTC3335's write address.

If the address matches that of the LTC3335, the LTC3335 returns an acknowledge. The bus master should then deliver the subaddress. The subaddress value is transferred to a special pointer register within the LTC3335 upon the return of the subaddress acknowledge bit by the LTC3335. If the master wishes to continue the write transaction, it may then deliver the data byte. The data byte is transferred to an internal pending data register at the location of the subaddress pointer when the LTC3335 acknowledges the data byte. The LTC3335 is then ready to receive a new subaddress, optionally repeating the [SUBADDRESS] [DATA] cycle indefinitely. After the write address, the odd position bytes always represent a subaddress pointer assignment and the even position bytes always represent data to be stored at the location referenced by the subaddress pointer. The master may terminate communication with the LTC3335 after any even or odd number of bytes with

APPLICATIONS INFORMATION

either a repeat START or a STOP condition. If a repeat START condition is initiated by the master, the LTC3335, or any other chip on the I^2C bus, can then be addressed. The LTC3335 will remember, but not act on, the last input of valid data that it received at each subaddress location. This cycle can also continue indefinitely. Once all chips on the bus have been addressed and sent valid data, a global STOP can be sent and the LTC3335 will immediately update all of its command registers with the most recent pending data that it had previously received.

Bus Read Operation

The LTC3335 contains 2 readable registers. One is read only and contains alarm information (Register D). The other contains accumulated battery discharge information (Register C) which may be both written and read back by the bus master.

Only one subaddressed data register is accessible during each bus read operation. The data returned by the LTC3335 is from the data register pointed to by the contents of the subaddress pointer register. The pointer register contents are determined by the previous bus write operation.

In preparation for a bus read operation, it may be advantageous for a bus master to prematurely terminate a write transaction with a STOP or repeat START condition after transmitting only an odd number of bytes. The last transmitted byte then represents a pointer to the register of interest for the subsequent bus read operation.

The bus master reads status data from the LTC3335 with a START or repeat START condition followed by the LTC3335 read address. If the read address matches that of the LTC3335, the LTC3335 returns an acknowledge. Following the acknowledgement of its read address, the LTC3335 returns one bit of status information for each of the next eight clock cycles from the register selected by the subaddress pointer. Additional clock cycles from the master after the single data byte has been read will leave the SDA line high (0xFF transmitted). The LTC3335 will never acknowledge any bytes during a bus read operation with the exception of its read address.

To read the same register again, the transaction may be repeated starting with a START followed by the LTC3335 read address. It is not necessary to rewrite the subaddress pointer register if the subaddress has not changed. To read a different register, a write transaction must be initiated with a START or repeat START followed by the LTC3335 write address and subaddress pointer byte before the read transaction may be repeated.

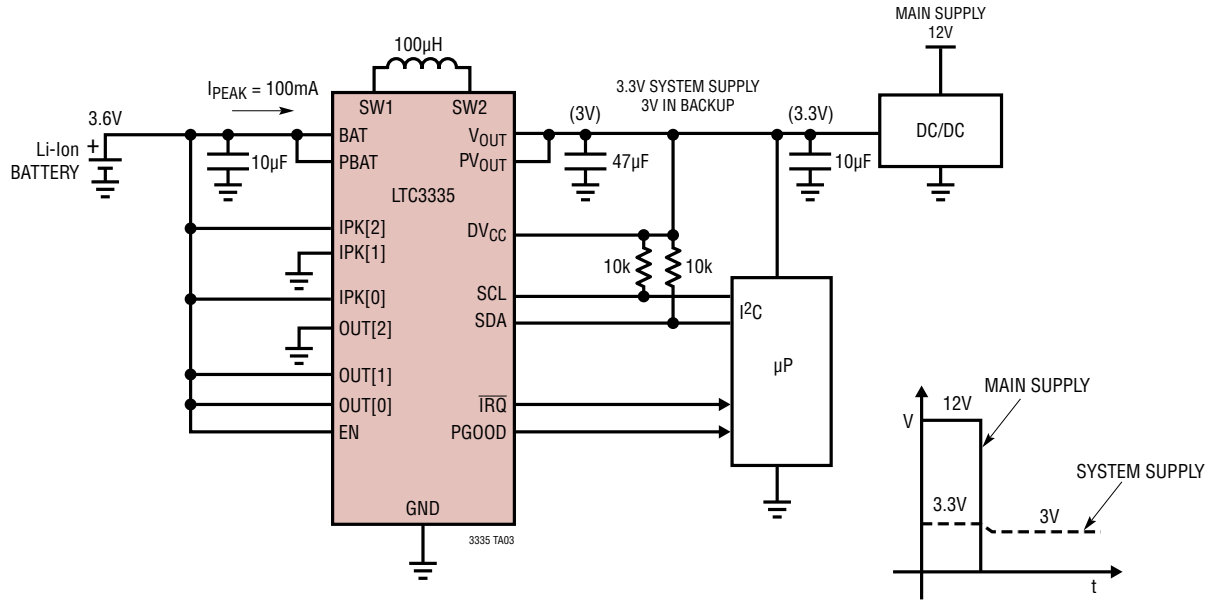
When the contents of the subaddress pointer register point to write-only command register (A, B, E), the data returned in a bus read operation is the pending command data at that location if it had been modified since the last STOP condition. After a STOP condition, all pending data is copied to the command registers for immediate effect.

When the contents of the subaddress pointer register point to the writable and readable command register C, the data returned in a bus read operation is data at that location, not the pending command data from previous write operation. After a STOP condition, all pending data is copied to the command registers for immediate effect and a following read operation can read the effect.

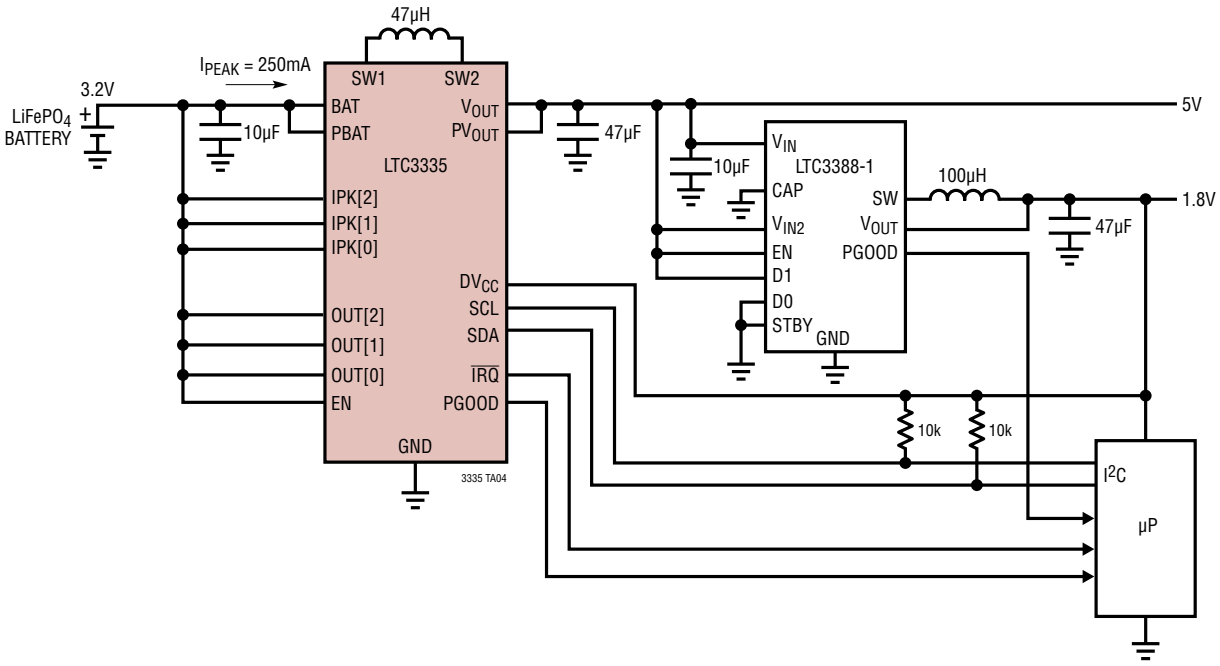
When the contents of the subaddress pointer register point to the read-only alarm register D, the data returned is a snapshot of the state of the LTC3335 at a particular instant in time. If no interrupt requests are pending, the status data is sampled when the LTC3335 acknowledges its read address, just before the LTC3335 begins data transmission during a bus read operation. When an alarm/fault occurs, the $\overline{IRQ}$ pin is driven low and data is latched in the alarm register D at that moment. Any subsequent read operation from register D will return this frozen data to facilitate determination of the cause of the interrupt request. After the bus master clears the LTC3335 interrupt request (E[0] =1), the status latches are cleared. Bus read operations will then again return either a snapshot of the data at the read address acknowledge, or at the time of the next interrupt assertion, whichever comes first.

TYPICAL APPLICATION

Backup Power Supply



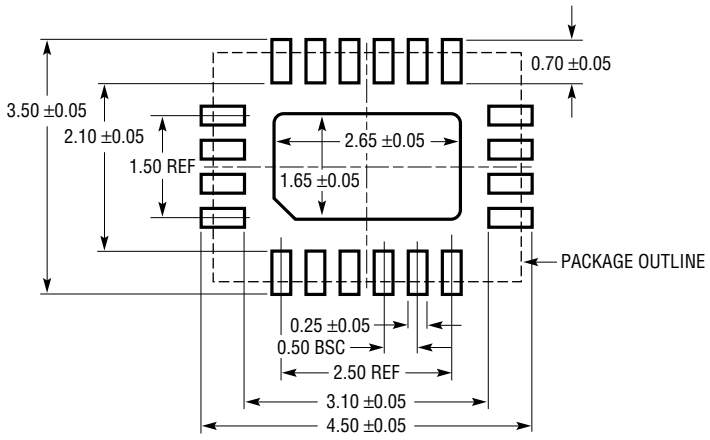
Dual 5V/1.8V Regulator Where LTC3335 Counts Coulombs for Both Output Rails



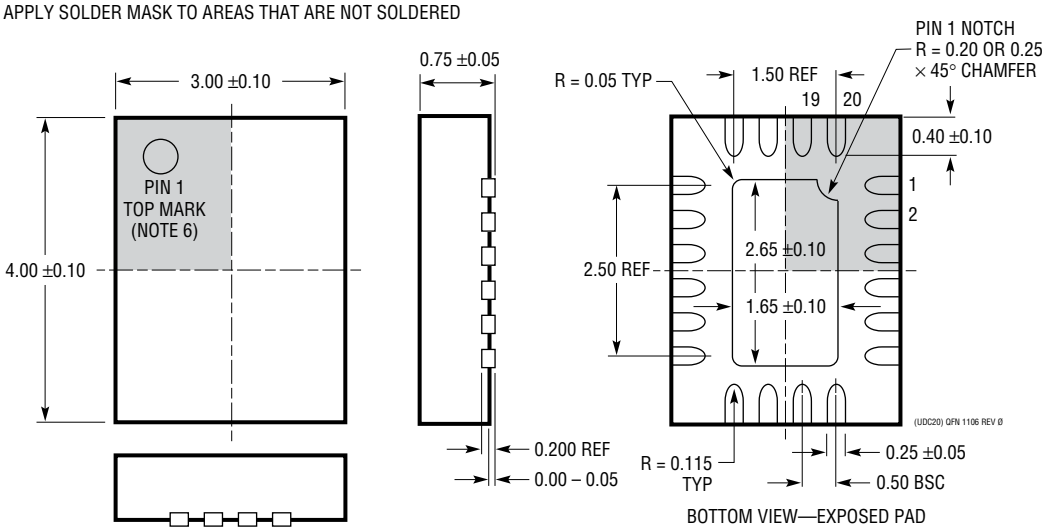
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UDC Package
20-Lead Plastic QFN (3mm × 4mm)
(Reference LTC DWG # 05-08-1742 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE