500MHz Ultra-Low Bias Current FET Input Op Amp

FEATURES

- **Gain Bandwidth Product: 500MHz**
- **–3dB Bandwidth (A = 1): 350MHz**
- **Low Input Bias Current:**
  - **±3fA Typ. Room Temperature**
  - **4pA Max at 125°C**
- **Current Noise (100kHz): 5.5fA/√Hz**
- **Voltage Noise (1MHz): 4.3nV/√Hz**
- **Extremely Low C_{IN} 450fF**
- **Rail-to-Rail Output**
- Slew Rate: 400V/µs
- Supply Range: 3.1V to 5.25V
- Quiescent Current: 16.5mA
- Harmonic Distortion ($2V_{P-P}$):
  - –100dB at 1MHz
  - –80dB at 10MHz
- Operating Temp Range: –40°C to 125°C
- Single in 8-Lead SO-8, 6-Lead TSOT-23 Packages
- Dual in 8-Lead MS8, 3mm × 3mm 10-Lead DFN 10 Packages

APPLICATIONS

- Trans-Impedance Amplifiers
- ADC Drivers
- CCD Output Buffer
- Photomultiplier Tube Post-Amplifier
- Low I_{BIAS} Circuits

DESCRIPTION

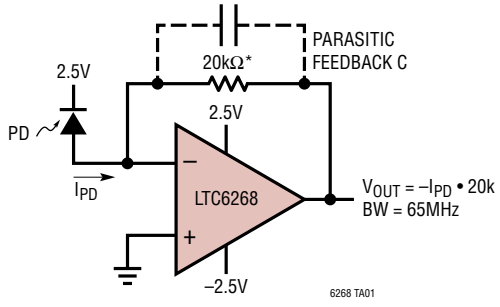
The LTC®6268/LTC6269 is a single/dual 500MHz FET-input operational amplifier with extremely low input bias current and low input capacitance. It also features low input-referred current noise and voltage noise making it an ideal choice for high speed transimpedance amplifiers, CCD output buffers, and high-impedance sensor amplifiers. Its low distortion makes the LTC6268/LTC6269 an ideal amplifier for driving SAR ADCs.

It operates on 3.1V to 5.25V supply and consumes 16.5mA per amplifier. A shutdown feature can be used to lower power consumption when the amplifier is not in use.

The LTC6268 single op amp is available in 8-lead SOIC and 6-lead SOT-23 packages. The SOIC package includes two unconnected pins which can be used to create an input pin guard ring to protect against board leakage currents. The LTC6269 dual op amp is available in 8-lead MSOP with exposed pad and 3mm × 3mm 10-lead DFN packages. They are fully specified over the –40°C to 85°C and the –40°C to 125°C temperature ranges.

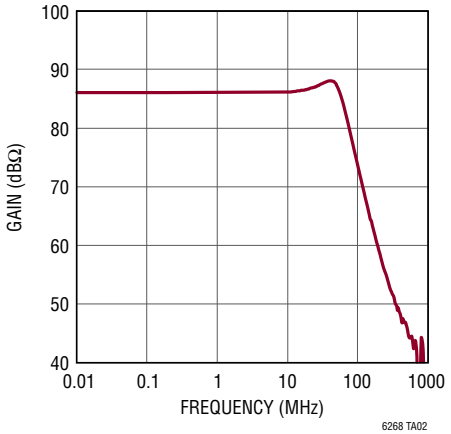
TYPICAL APPLICATION

20kΩ Gain 65MHz Trans-Impedance Amplifier



PD = OSI OPTOELECTRONICS, FCI-125G-006
*TWO 40.2kΩ 0603 PACKAGE RESISTORS IN PARALLEL

20kΩ TIA Frequency Response

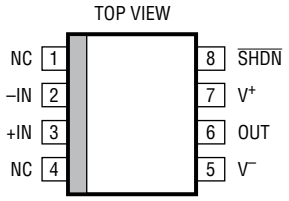


ABSOLUTE MAXIMUM RATINGS

(Note 1)

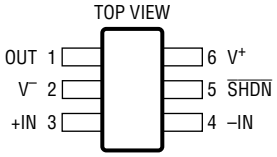
Supply Voltage V^+ to V^- 5.5V
Input Voltage ..... V^- – 0.2V to V^+ + 0.2V
Input Current (+IN, –IN)(Note 2) ..... ±1mA
Input Current ($\overline{SHDN}$) ..... ±1mA
Output Current (I_{OUT}) (Note 8, 9) 135mA
Output Short-Circuit Duration (Note 3) ... Thermally Limited
Operating Temperature Range
LTC6268I/LTC6269I ..... –40°C to 85°C
LTC6268H/LTC6269H ..... –40°C to 125°C
Specified Temperature Range (Note 4)
LTC6268I/LTC6269I ..... –40°C to 85°C
LTC6268H/LTC6269H ..... –40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



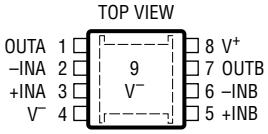
S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 120°C/W (NOTE 5)



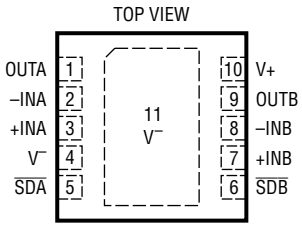
S6 PACKAGE
6-LEAD PLASTIC TSOT-23

T_{JMAX} = 150°C, θ_{JA} = 192°C/W (NOTE 5)



MS8E PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 40°C/W (NOTE 5)
EXPOSED PAD (PIN 9) IS V^-, IT IS RECOMMENDED TO SOLDER TO PCB



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W (NOTE 5)
EXPOSED PAD (PIN 11) IS V^-, IT IS RECOMMENDED TO SOLDER TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6268IS6#TRMPBF	LTC6268IS6#TRPBF	LTGFS	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6268HS6#TRMPBF	LTC6268HS6#TRPBF	LTGFS	6-Lead Plastic TSOT-23	–40°C to 125°C
LTC6268IS8#PBF	LTC6268IS8#TRPBF	6268	8-Lead Plastic SOIC	–40°C to 85°C
LTC6268HS8#PBF	LTC6268HS8#TRPBF	6268	8-Lead Plastic SOIC	–40°C to 125°C
LTC6269IMS8E#PBF	LTC6269IMS8E#TRPBF	LTGFP	8-Lead Plastic MSOP	–40°C to 85°C
LTC6269HMS8E#PBF	LTC6269HMS8E#TRPBF	LTGFP	8-Lead Plastic MSOP	–40°C to 125°C
LTC6269IDD#PBF	LTC6269IDD#TRPBF	LGFN	10-Lead Plastic DD	–40°C to 85°C
LTC6269HDD#PBF	LTC6269HDD#TRPBF	LGFN	10-Lead Plastic DD	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

5.0V ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{SUPPLY} = 5.0V (V^+ = 5V, V^- = 0V, V_{CM} = mid-supply), R_L = 1kΩ, C_L = 10pF, $V_{\overline{SHDN}}$ is unconnected.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = 2.75V	 ●	–0.7 –2.5	0.2	0.7 2.5	mV mV
		V_{CM} = 4.0V	 ●	–1.0 –4.5	0.2	1.0 4.5	mV mV
TC V_{OS}	Input Offset Voltage Drift	V_{CM} = 2.75V			4		µV/°C
I_B	Input Bias Current (Notes 6, 8)	V_{CM} = 2.75V LTC6268I/LTC6269I LTC6268H/LTC6269H	 ● ●	–20 –900 –4	±3	20 900 4	fA fA pA
		V_{CM} = 4.0V LTC6268I/LTC6269I LTC6268H/LTC6269H	 ● ●	–20 –900 –4	±3	20 900 4	fA fA pA
I_{OS}	Input Offset Current (Notes 6, 8)	V_{CM} = 2.75V LTC6268I/LTC6269I LTC6268H/LTC6269H	 ● ●	–40 –450 –2	±6	40 450 2	fA fA pA
e_n	Input Voltage Noise Density, V_{CM} = 2.75V	f = 1MHz			4.3		nV/√Hz
	Input Voltage Noise Density, V_{CM} = 4.0V	f = 1MHz			4.9		nV/√Hz
	Input Referred Noise Voltage	f = 0.1Hz to 10Hz			13		$µV_{P-P}$
i_n	Input Current Noise Density, V_{CM} = 2.75V	f = 100kHz			5.5		fA/√Hz
	Input Current Noise Density, V_{CM} = 4.0V	f = 100kHz			5.3		fA/√Hz
R_{IN}	Input Resistance	Differential			>1000		GΩ
		Common Mode			>1000		GΩ
C_{IN}	Input Capacitance	Differential (DC to 200MHz)			100		fF
		Common Mode (DC to 100MHz)			450		fF
CMRR	Common Mode Rejection Ratio	V_{CM} = 0.5V to 3.2V (PNP Side)	 ●	72 70	90		dB dB
		V_{CM} = 0V to 4.5V	 ●	64 52	82		dB dB
IVR	Input Voltage Range	Guaranteed by CMRR	●	0		4.5	V

5.0V ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{SUPPLY} = 5.0V (V^+ = 5V, V^- = 0V, V_{CM} = mid-supply), R_L = 1kΩ, C_L = 10pF, $V_{\overline{SHDN}}$ is unconnected.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection Ratio	V_{CM} = 1.0V, V_{SUPPLY} Ranges from 3.1V to 5.25V		 ●	78 75	95		dB dB
	Supply Voltage Range			●	3.1		5.25	
A_V	Open Loop Voltage Gain	V_{OUT} = 0.5V to 4.5V	R_{LOAD} = 10k	 ●	125 40	250		V/mV V/mV
			R_{LOAD} = 100	 ●	10 2	21		V/mV V/mV
V_{OL}	Output Swing Low (Input Overdrive 30mV) Measured from V^-	I_{SINK} = 10mA		 ●		80	140 200	mV mV
		I_{SINK} = 25mA		 ●		130	200 260	mV mV
V_{OH}	Output Swing High (Input Overdrive 30mV) Measured from V^+	I_{SOURCE} = 10mA		 ●		70	140 200	mV mV
		I_{SOURCE} = 25mA		 ●		160	270 370	mV mV
I_{SC}	Output Short Circuit Current	(Note 9)		 ●	60 40	90		mA mA
I_S	Supply Current Per Amplifier			 ●	15 9	16.5	18 23	mA mA
	Supply Current in Shutdown (Per Amplifier)			 ●		0.39	0.85 1.2	mA mA
$I_{\overline{SHDN}}$	Shutdown Pin Current	$V_{\overline{SHDN}}$ = 0.75V $V_{\overline{SHDN}}$ =1.50V		● ●	–12 –12	2 2	12 12	µA µA
V_{IL}	$\overline{SHDN}$ Input Low Voltage	Disable		●			0.75	V
V_{IH}	$\overline{SHDN}$ Input High Voltage	Enable. If $\overline{SHDN}$ is Unconnected, Amp is Enabled		●	1.5			V
t_{ON}	Turn On Time, Delay from $\overline{SHDN}$ Toggle to Output Reaching 90% of Target	$\overline{SHDN}$ Toggle from 0V to 2V, A_V = 1				580		ns
t_{OFF}	Turn Off Time, Delay from $\overline{SHDN}$ Toggle to Output High Z	$\overline{SHDN}$ Toggle from 2V to 0V, A_V = 1				480		ns
BW	–3dB Closed Loop Bandwidth	A_V = 1				350		MHz
GBW	Gain-Bandwidth Product	f = 10MHz			400	500		MHz
t_S	Settling Time, 1V to 4V, Unity Gain	0.1%				17		ns
SR+	Slew Rate+	A_V = 6 (R_F = 499, R_G = 100) V_{OUT} = 0.5V to 4.5V, Measured 20% to 80%, C_{LOAD} = 10pF		 ●	300 200	400		V/µs V/µs
SR–	Slew Rate–	A_V = 6 (R_F = 499, R_G = 100) V_{OUT} = 4.5V to 0.5V, Measured 80% to 20%, C_{LOAD} = 10pF		 ●	180 130	260		V/µs V/µs
FPBW	Full Power Bandwidth (Note 7)	$4V_{P-P}$				21		MHz
HD	Harmonic Distortion(HD2/HD3)	A = 1, 10MHz. $2V_{P-P}$, V_{CM} = 1.75V, R_L = 1k				–81/–90		dB
THD+N	Total Harmonic Distortion and Noise	A = 1, 10MHz. $2V_{P-P}$, V_{CM} = 1.75V, R_L = 1k				0.01 –79.6		% dB
I_{LEAK}	Output Leakage Current in Shutdown	$V_{\overline{SHDN}}$ = 0V, V_{OUT} = 0V $V_{\overline{SHDN}}$ = 0V, V_{OUT} = 5V					400 400	nA nA

3.3V ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{SUPPLY} = 3.3V (V^+ = 3.3V, V^- = 0V, V_{CM} = mid-supply), R_L = 1kΩ, C_L = 10pF, $V_{\overline{SHDN}}$ is unconnected.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = 1.0V	 ●	–0.7 –2.5	0.2	0.7 2.5	mV mV
		V_{CM} = 2.3V	 ●	–1.0 –4.5	0.2	1.0 4.5	mV mV
TC V_{OS}	Input Offset Voltage Drift	V_{CM} = 1.0V			4		µV/C
I_B	Input Bias Current (Notes 6, 8)	V_{CM} = 1.0V LTC6268I/LTC6269I LTC6268H/LTC6269H	 ● ●	–20 –900 –4	±3	20 900 4	fA fA pA
		V_{CM} = 2.3V LTC6268I/LTC6269I LTC6268H/LTC6269H	 ● ●	–20 –900 –4	±3	20 900 4	fA fA pA
I_{OS}	Input Offset Current (Notes 6, 8)	V_{CM} = 1.0V LTC6268I/LTC6269I LTC6268H/LTC6269H	 ● ●	–40 –450 –2	±6	40 450 2	fA fA pA
e_n	Input Voltage Noise Density, V_{CM} =1.0V	f = 1MHz			4.3		nV/√Hz
	Input Voltage Noise Density, V_{CM} = 2.3V	f = 1MHz			4.9		nV/√Hz
	Input Referred Noise Voltage	f = 0.1Hz to 10Hz			13		μV_{P-P}
i_n	Input Current Noise Density, V_{CM} = 1.0V	f = 100kHz			5.6		fA/√Hz
	Input Current Noise Density, V_{CM} = 2.3V	f = 100kHz			5.3		fA/√Hz
R_{IN}	Input Resistance	Differential Common Mode			>1000 >1000		GΩ GΩ
C_{IN}	Input Capacitance	Differential (DC to 200MHz) Common Mode (DC to 100MHz)			100 450		fF fF
CMRR	Common Mode Rejection Ratio	V_{CM} = 0.5V to 1.2V (PNP Side)	 ●	63 60	100		dB dB
		V_{CM} = 0V to 2.8V (Full Range)	 ●	60 50	77		dB dB
IVR	Input Voltage Range	Guaranteed by CMRR	●	0		2.8	V
A_V	Open Loop Voltage Gain	V_{OUT} = 0.5V to 2.8V, R_{LOAD} = 10k	 ●	80 40	200		V/mV V/mV
		R_{LOAD} = 100	 ●	10 2	18		V/mV V/mV
V_{OL}	Output Swing Low (Input Overdrive 30mV). Measured from V^-	I_{SINK} = 10mA	 ●		80	140 200	mV mV
		I_{SINK} = 25mA	 ●		140	200 260	mV mV
V_{OH}	Output Swing High (Input Overdrive 30mV). Measured from V^+	I_{SOURCE} = 10mA	 ●		80	140 200	mV mV
		I_{SOURCE} = 25mA	 ●		170	270 370	mV mV
I_{SC}	Output Short Circuit Current	(Note 9)	 ●	50 35	80		mA mA
I_S	Supply Current per Amplifier		 ●	14.5 9	16	17.5 23	mA mA

3.3V ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{SUPPLY} = 3.3V (V^+ = 3.3V, V^- = 0V, V_{CM} = mid-supply) R_L = 1kΩ, C_L = 10pF, $V_{\overline{SHDN}}$ is unconnected.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Supply Current in Shutdown (Per Amplifier)		 ●		0.23	0.6 0.8	mA mA
$I_{\overline{SHDN}}$	Shutdown Pin Current	$V_{\overline{SHDN}}$ = 0.75V $V_{\overline{SHDN}}$ = 1.5V	● ●	–12 –12	2 2	12 12	µA µA
V_{IL}	$\overline{SHDN}$ Input Low Voltage	Disable	●			0.75	V
V_{IH}	$\overline{SHDN}$ Input High Voltage	Enable. If $\overline{SHDN}$ is Unconnected, Amp Is Enabled	●	1.5			V
t_{ON}	Turn On Time, Delay from $\overline{SHDN}$ Toggle to Output Reaching 90% of Target	$\overline{SHDN}$ Toggle from 0V to 2V			710		ns
t_{OFF}	Turn Off Time, Delay from $\overline{SHDN}$ Toggle to Output High Z	$\overline{SHDN}$ Toggle from 2V to 0V			620		ns
BW	–3dB Closed Loop Bandwidth	A_V = 1			350		MHz
GBW	Gain-Bandwidth Product	f = 10MHz		370	420		MHz
SR+	Slew Rate+	A_V = 6 (R_F = 499, R_G = 100), V_{OUT} = 0.5V to 2.8V, Measured 20% to 80%, C_{LOAD} = 10pF	 ●	 300 200	 400		 V/µs V/µs
SR–	Slew Rate–	A_V = 6 (R_F = 499, R_G = 100), V_{OUT} = 2.8V to 0.5V, Measured 80% to 20%, C_{LOAD} = 10pF	 ●	 180 130	 260		 V/µs V/µs
FPBW	Full Power Bandwidth (Note 7)	$2V_{P-P}$			40		MHz
HD	Harmonic Distortion(HD2/HD3)	A = 1, 10MHz. $1V_{P-P}$, V_{CM} = 1.65V, R_L = 1k			–81/–90		dB
THD+N	Total Harmonic Distortion and Noise	A = 1, 10MHz. $1V_{P-P}$, V_{CM} = 1.65V, R_L = 1k			0.01 –78		% dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by two series connected ESD protection diodes to each power supply. The input current should be limited to less than 1mA. The input voltage should not exceed 200mV beyond the power supply.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LTC6268I/LTC6269I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6268H/LTC6269H is guaranteed to meet specified performance from –40°C to 125°C.

Note 5: Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

Note 6: The input bias current is the average of the currents into the positive and negative input pins. Typical measurement is for S8 package.

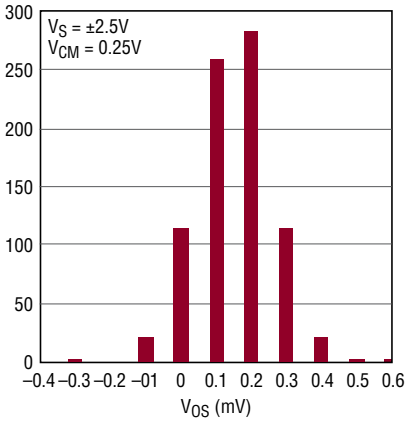
Note 7: Full Power Bandwidth is calculated from slew rate using the following equation: FPBW = SR/(2π • V_{PEAK})

Note 8: This parameter is specified by design and/or characterization and is not tested in production.

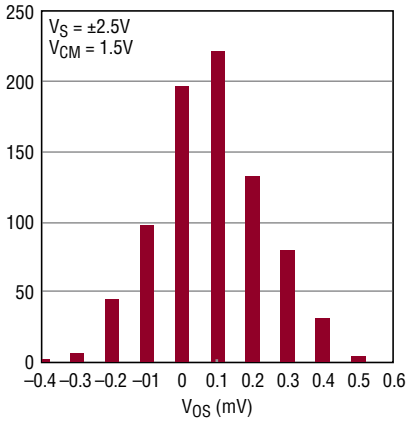
Note 9: The LTC6268/LTC6269 is capable of producing peak output currents in excess of 135mA. Current density limitations within the IC require the continuous current supplied by the output (sourcing or sinking) over the operating lifetime of the part be limited to under 135mA (Absolute Maximum).

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

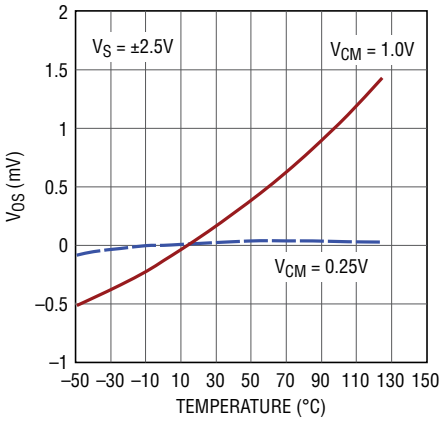
Input Offset Voltage Distribution



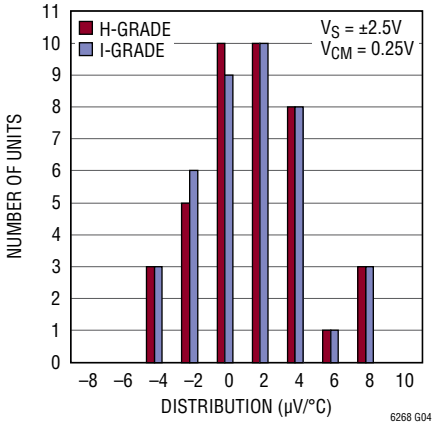
Input Offset Voltage Distribution



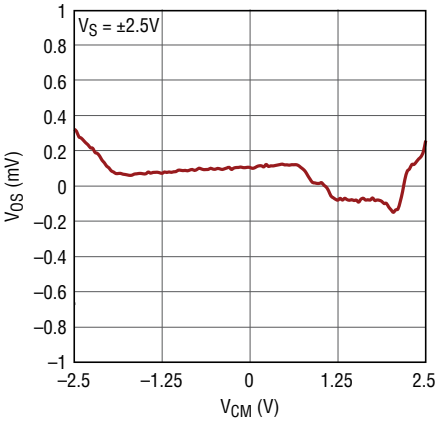
Input Offset Voltage vs Temperature



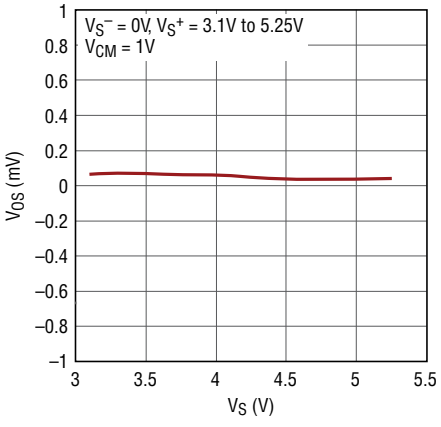
Input Offset Drift Distribution



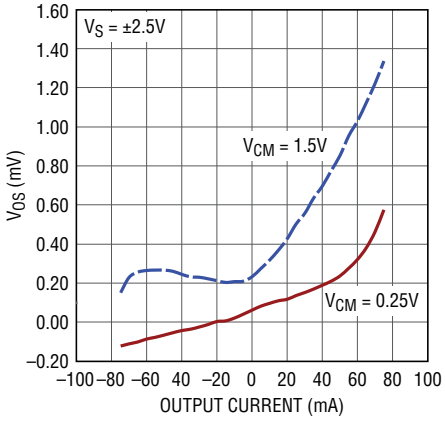
Input Offset Voltage vs Common Mode Voltage



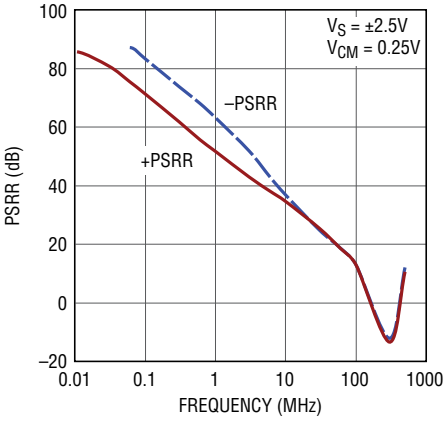
Input Offset Voltage vs Supply Voltage



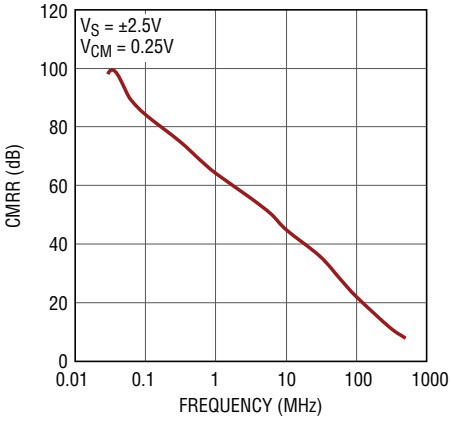
Input Offset Voltage vs Output Current



PSRR vs Frequency

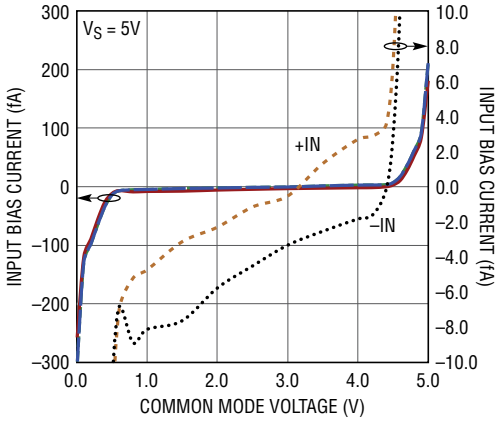


CMRR vs Frequency

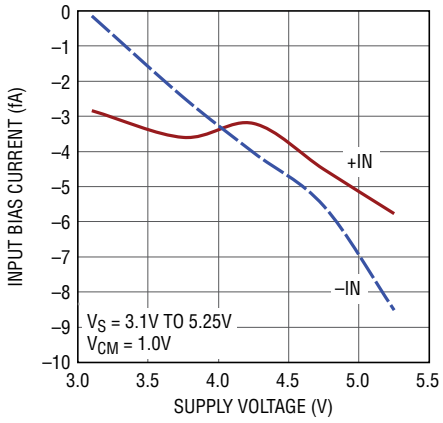


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

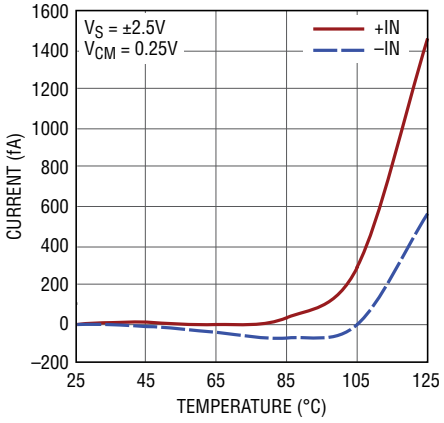
Input Bias Current vs Common Mode Voltage



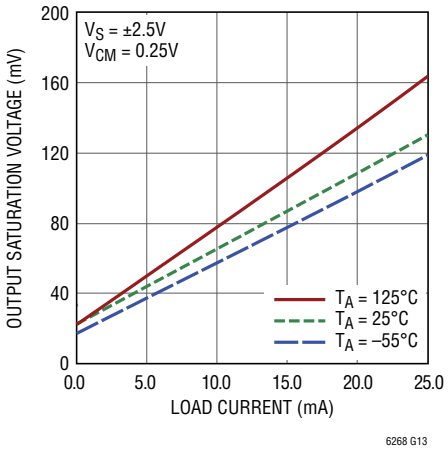
Input Bias Current vs Supply Voltage



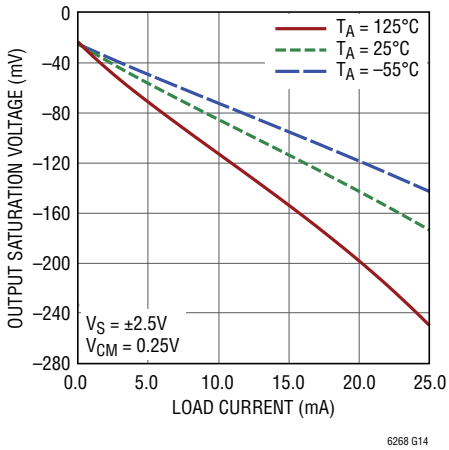
Input Bias Current vs Temperature



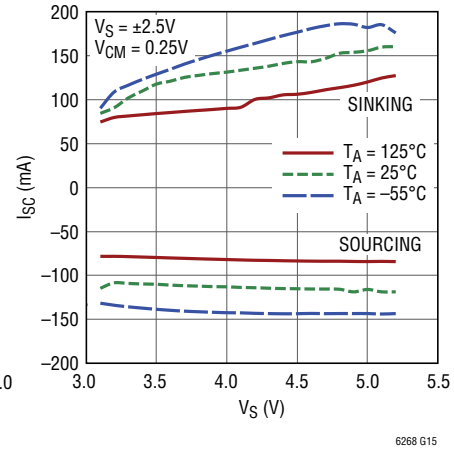
Output Saturation Voltage vs Load Current (Output Low)



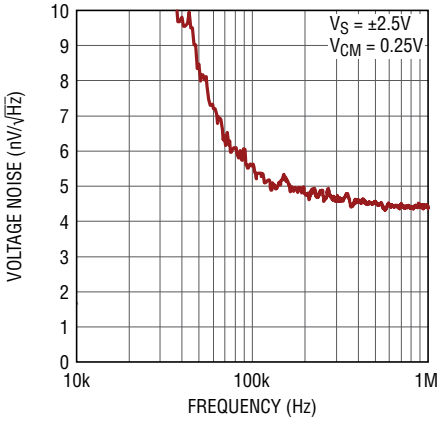
Output Saturation Voltage vs Load Current (Output High)



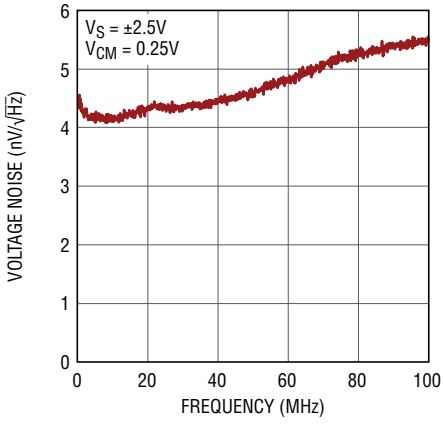
Output Short Circuit Current vs Supply Voltage



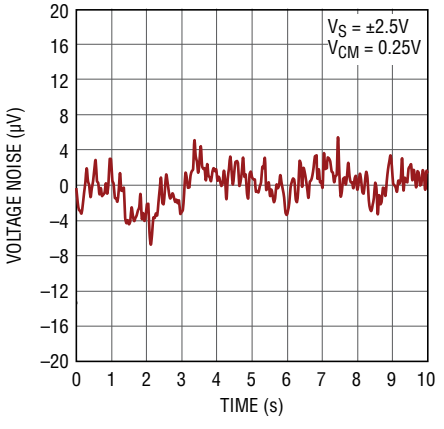
Input Referred Voltage Noise



Wide Band Input Referred Voltage Noise

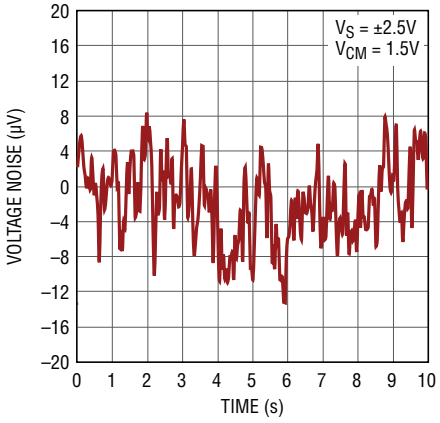


0.1Hz to 10Hz Output Voltage Noise

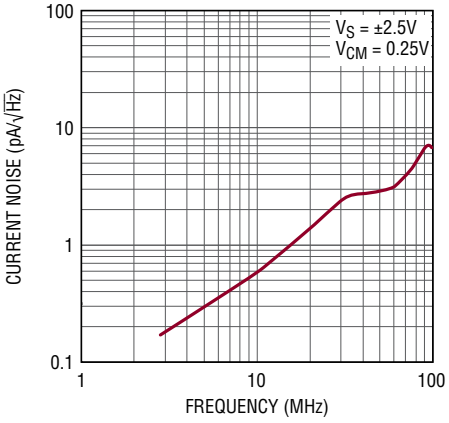


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

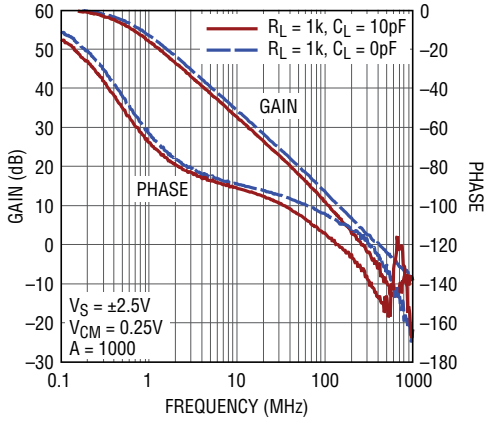
0.1Hz to 10Hz Output Voltage Noise



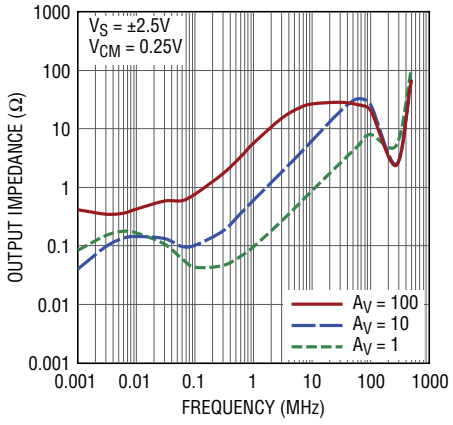
Input Referred Current Noise



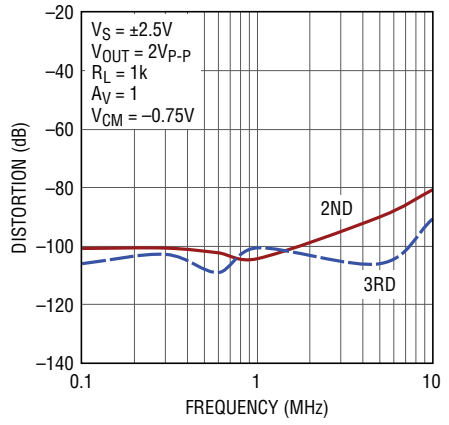
Gain and Phase vs Frequency



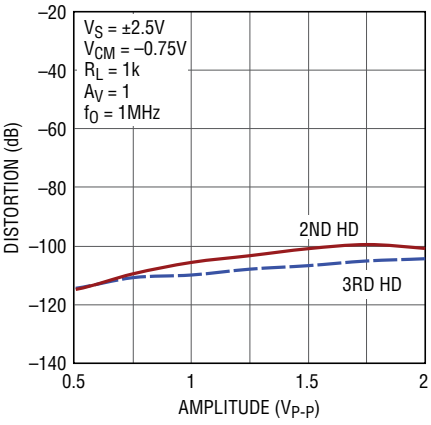
Output Impedance vs Frequency



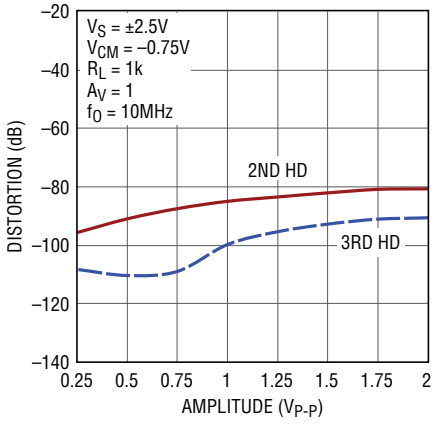
Harmonic Distortion vs Frequency



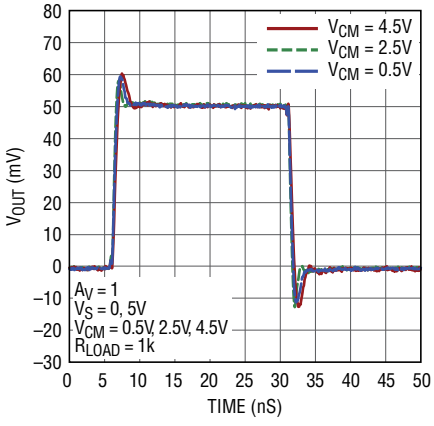
Harmonic Distortion vs Amplitude



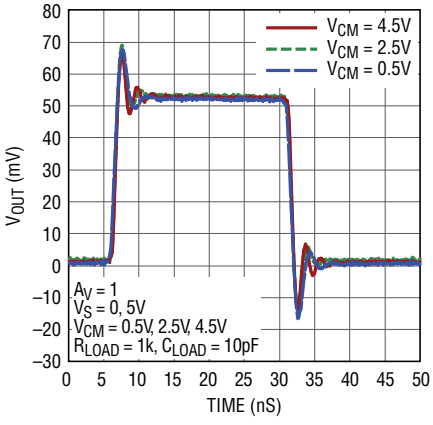
Harmonic Distortion vs Amplitude



50mV Step Response

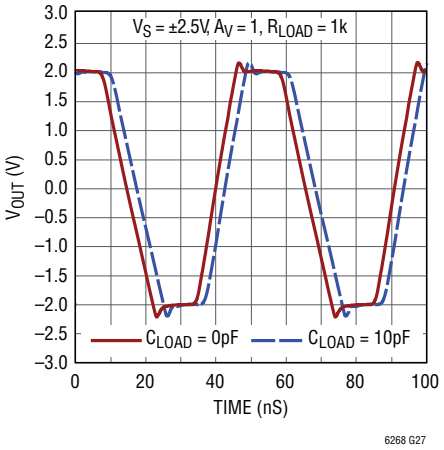


50mV Step Response

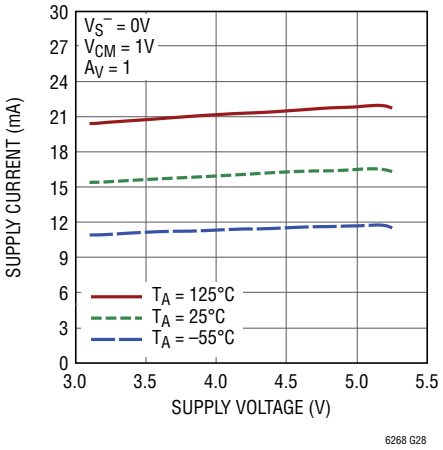


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

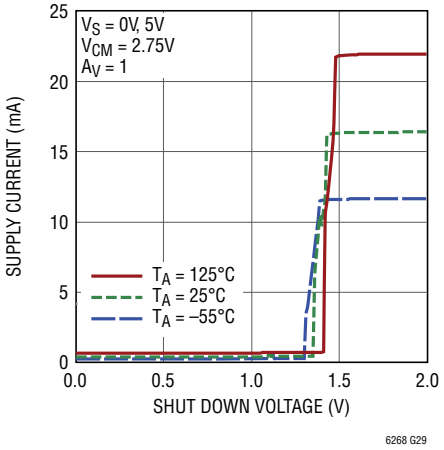
Large Signal Response



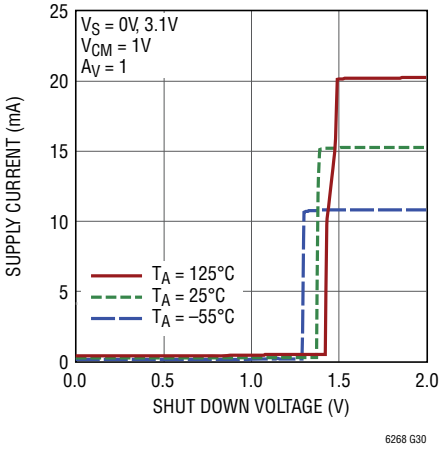
Supply Current vs Supply Voltage



Supply Current vs Shutdown Voltage



Supply Current vs Shutdown Voltage



PIN FUNCTIONS

–IN: Inverting Input of the Amplifier. The voltage range of this pin is from V^- to V^+ –0.5V.

+IN: Non-Inverting Input. The voltage range of this pin is from V^- to V^+ –0.5V.

V^+: Positive Power Supply. Total supply ($V^+ – V^-$) voltage is from 3.1V to 5.25V. Split supplies are possible as long as the total voltage between V^+ and V^- is between 3.1V and 5.25. A bypass capacitor of 0.1µF should be used between V^+ to ground as close to the pin as possible.

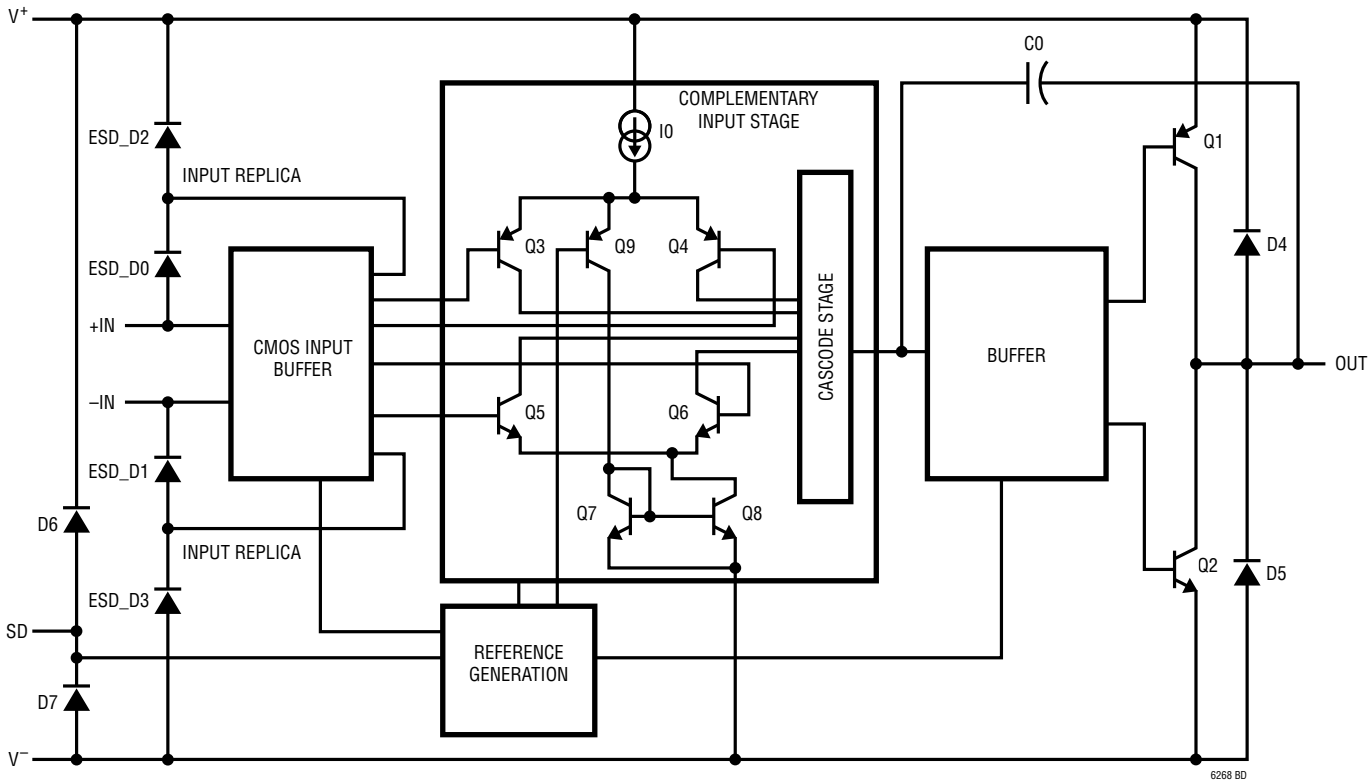
V^-: Negative Power Supply. Normally tied to ground, it can also be tied to a voltage other than ground as long as the voltage difference between V^+ and V^- is between 3.1V and 5.25V. If it is not connected to ground, bypass it to ground with a capacitor of 0.1µF as close to the pin as possible.

$\overline{SHDN}$, $\overline{SDA}$, $\overline{SDB}$: Active Low op amp shutdown, threshold is 0.75V above the negative supply, V^-. If left unconnected, the amplifier is enabled.

OUT: Amplifier Output.

NC: Not connected. May be used to create a guard ring around the input to guard against board leakage currents. See Applications Information section for more details.

SIMPLIFIED SCHEMATIC



LTC6268 Simplified Schematic Diagram

OPERATION

The LTC6268 input signal range is specified from the negative supply to 0.5V below the positive power supply, while the output can swing from rail-to-rail. The schematic above depicts a simplified schematic of the amplifier.

The input pins drive a CMOS buffer stage. The CMOS buffer stage creates replicas of the input voltages to boot strap the protection diodes. In turn, the buffer stage drives a complementary input stage consisting of two differential amplifiers, active over different ranges of input common mode voltage. The main differential amplifier is active with input common mode voltages from the negative power supply to approximately 1.55V below the positive supply, with the second amplifier active over the remaining range to 0.5V below the positive supply rail. The buffer and output bias stage uses a special compensation technique ensuring stability of the op amp. The common emitter topology of output transistors Q1/Q2 enables the output to swing from rail-to-rail.

APPLICATIONS INFORMATION

Noise

To minimize the LTC6268's noise over a broad range of applications, careful consideration has been placed on input referred voltage noise (e_N), input referred current noise (i_N) and input capacitance C_{IN}.

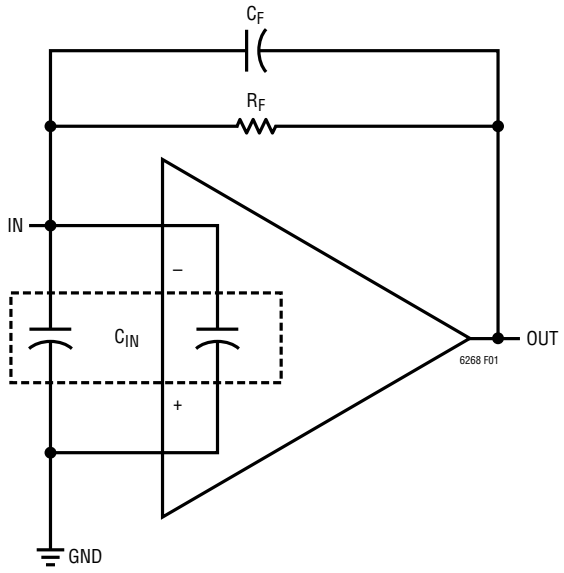


Figure 1. Simplified TIA Schematic

For a trans-impedance amplifier (TIA) application such as shown in Figure 1, all three of these op amp parameters, plus the value of feedback resistance R_F, contribute to noise behavior in different ways, and external components and traces will add to C_{IN}. It is important to understand the impact of each parameter independently. Input referred voltage noise (e_N) consists of flicker noise (or 1/f noise), which dominates at lower frequencies, and thermal noise which dominates at higher frequencies. For LTC6268, the 1/f corner, or transition between 1/f and thermal noise, is at 80kHz. The i_N and R_F contributions to input referred noise current at the minus input are relatively straight forward, while the e_N contribution is amplified by the noise gain. Because there is no gain resistor, the noise gain is calculated using feedback resistor(R_F) in conjunction with impedance of C_{IN} as $(1 + 2\pi R_F \bullet C_{IN} \bullet Freq)$, which increases with frequency. All of the contributions will be limited by the closed loop bandwidth. The equivalent input current noise is shown in Figures 2-5, where e_N represents contribution from input referred voltage noise (e_N), i_N represents contribution from input referred current noise (i_N), and R_F represents contribution from feedback resistor (R_F). TIA gain (R_F) and capacitance at input (C_{IN}) are also shown on each figure. Comparing Figures 2 & 3, and 4 & 5 for higher frequencies, e_N dominates when C_{IN} is high (5pF) due to the amplification mentioned above while i_N dominates when C_{IN} is low (1pF). At lower frequencies, the

APPLICATIONS INFORMATION

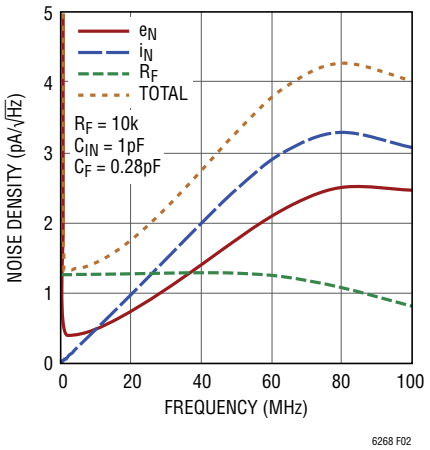


Figure 2

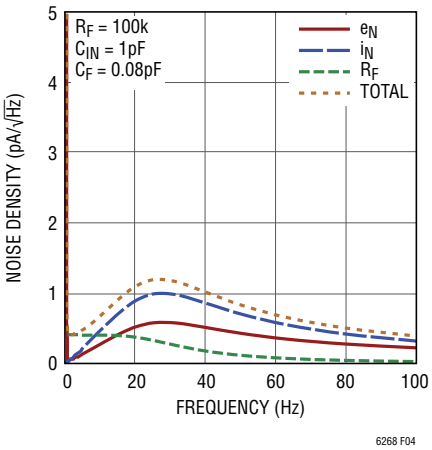


Figure 4

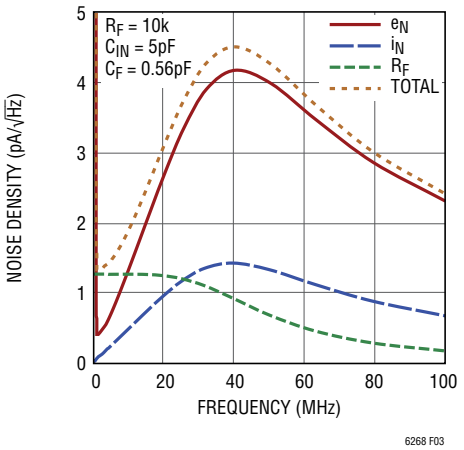


Figure 3

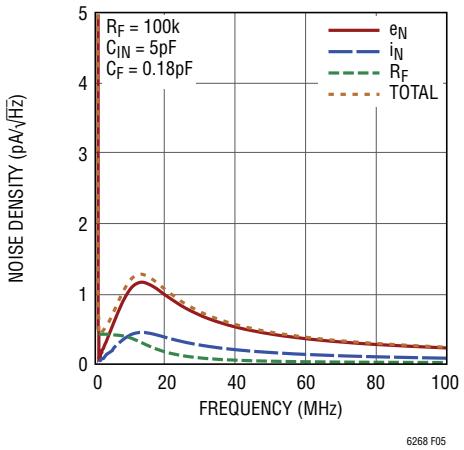


Figure 5

R_F contribution dominates for 10k and 100k. Since wide band e_N is 4.3nV/√Hz (see typical performance characteristics), R_F contribution will become a lesser factor at lower frequencies if R_F is less than 1.16kΩ as indicated by the following equation:

$$\frac{eN/R_F}{\sqrt{4kT/R_F}} \geq 1$$

Optimizing the Bandwidth for TIA Application

The capacitance at the inverting input node can cause amplifier stability problems if left unchecked. When the feedback around the op amp is resistive (R_F), a pole will be created with $R_F||C_{IN}$. This pole can create excessive phase shift and possibly oscillation. Referring to Figure 1, the response at the output is:

$$\frac{R_F}{1+\frac{2\zeta s}{\omega}+\frac{S^2}{\omega^2}}$$

APPLICATIONS INFORMATION

Where R_F is the DC gain of the TIA, ω is the natural frequency of the closed loop, which can be expressed as:

$$\omega = \sqrt{\frac{2\pi GBW}{R_F(C_{IN}+C_F)}}$$

ζ is the damping factor of the loop, which can be expressed as

$$\zeta = \frac{1}{2}\left(\sqrt{\frac{1}{2\pi GBW \bullet R_F(C_{IN}+C_F)}} + R_F\left(C_F + \frac{C_{IN}+C_F}{1+A_O}\right)\sqrt{\frac{2\pi GBW}{R_F(C_{IN}+C_F)}}\right)$$

Where C_{IN} is the total capacitance at the inverting input node of the op amp, and GBW is the gain bandwidth of the op amp. There are two regions that the system will be stable regardless of C_F. The first region is when R_F is less than $1/(4\pi \cdot C_{IN} \cdot GBW)$. In this region, the pole produced by the feedback resistor and C_{IN} is at a high frequency which does not cause stability problems. The second region is where:

$$R_F > \frac{A_O{}^2}{\pi GBW \bullet C_{IN}}$$

Where A_O is the DC open loop gain of the op amp, and the pole formed by $R_F C_{IN}$ is the dominant pole.

For R_F between these two regions, the small capacitor C_F in parallel with R_F can introduce enough damping to stabilize the loop. By assuming $C_{IN} >> C_F$, the following condition needs to be met for C_F,

$$C_F > \sqrt{\frac{C_{IN}}{\pi \bullet GBW \bullet R_F}}$$

The above condition implies that higher GBW will require lower feedback capacitance C_F, which will have higher loop bandwidth. Table 1 shows the optimal C_F for R_F of 10kΩ and 100kΩ and C_{IN} of 1pF and 5pF.

Table 1. Min C_F

R_F	C_{IN} = 1pF	C_{IN} = 5pF
10kΩ	0.25pF	0.56pF
100kΩ	0.08pF	0.18pF

Achieving Higher Bandwidth with Higher Gain TIAs

Good layout practices are essential to achieving best results from a TIA circuit. The following two examples show drastically different results from an LTC6268 in a 499kΩ TIA. (See Figure 6.) The first example is with an 0603 resistor in a basic circuit layout. In a simple layout, without expending a lot of effort to reduce feedback capacitance, the bandwidth achieved is about 2.5MHz. In this case, the bandwidth of the TIA is limited not by the GBW of the LTC6268, but rather by the fact that the feedback capacitance is reducing the actual feedback impedance (the TIA gain itself) of the TIA. Basically, it's a resistor bandwidth limitation. The impedance of the 499kΩ is being reduced by its own parasitic capacitance at high frequency. From the 2.5MHz bandwidth and the 499kΩ low frequency gain, we can estimate the total feedback capacitance as C = 1/(2π • 2.5MHz • 499kΩ) = 0.13pF. That's fairly low, but it can be reduced further.

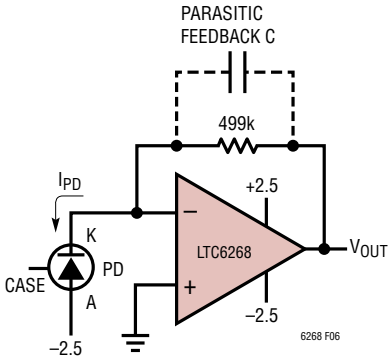


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Figure 6. LTC6268 and Low Capacitance Photodiode in a 499kΩ TIA

APPLICATIONS INFORMATION

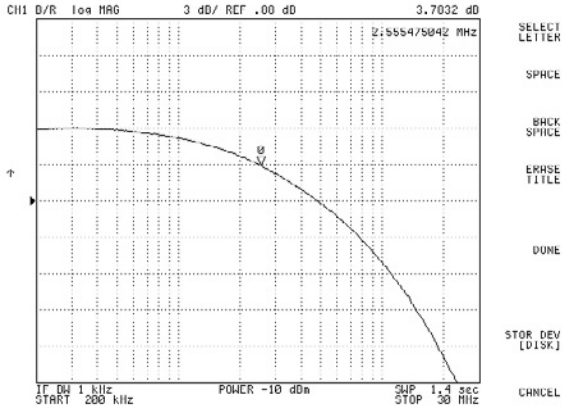


Figure 7. Frequency Response of 499kΩ TIA without Extra Effort to Reduce Feedback Capacitance is 2.5MHz

With some extra layout techniques to reduce feedback capacitance, the bandwidth can be increased. Note that we are increasing the effective "bandwidth" of the 499kΩ resistance. One of the main ways to reduce capacitance is to increase the distance between the plates, in this case the plates being the two endcaps of the component resistor. For that reason, it will serve our purposes to go to a longer resistor. An 0805 is longer than an 0603, but its endcaps are also larger in area, increasing capacitance again. However, increasing distance between the endcaps is not the only way to decrease capacitance, and the extra distance between the resistor endcaps also allows the easy application of another technique to reduce feedback capacitance. A very powerful method to reduce plate to plate capacitance is to shield the E field paths that give rise to the capacitance. In this particular case, the method is to place a short ground trace between the resistor pads, near the TIA output end. Such a ground trace shields the output field from getting to the summing node end of the resistor and effectively shunts the field to ground instead. Keeping the trace close to the output end increases the output load capacitance very slightly. See Figure 8 for a pictorial representation.

Figure 9 shows the dramatic increase in bandwidth simply by careful attention to low capacitance methods around the feedback resistance. Bandwidth was raised from 2.5MHz to 11.2MHz, a factor greater than 4. Methods implemented were two:

1) Minimal pad sizing. Check with your board assembler for minimum acceptable pad sizing, or assemble this resistor using other means, and

2) Shield the feedback capacitance using a ground trace under the feedback resistor near the output side.

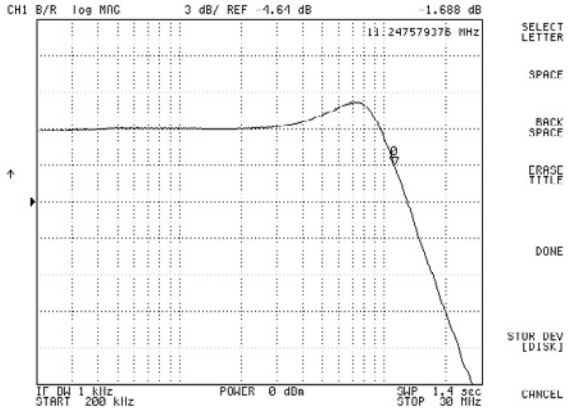


Figure 9. LTC6268 in a 499kΩ TIA with extra Layout Effort to Reduce Feedback Capacitance Achieves 11.2MHz BW

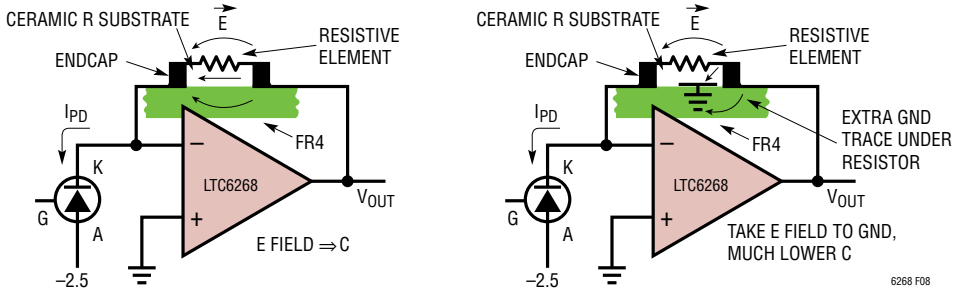


Figure 8. A Normal Layout at Left and a Field-Shunting Layout at Right. Simply Adding a Ground Trace Under the Feedback Resistor Does Much to Shunt Field Away from the Feedback Side and Dumps It to Ground. Note That the Dielectric Constant of Fr4 and Ceramic Is Typically 4, so Most of the Capacitance Is in the Solids and Not Through the Air. (Reduced Pad Size On Right Is Not Shown.)

APPLICATIONS INFORMATION

High Impedance Buffer

The very high input impedance of the LTC6268 makes it ideal for buffering high impedance or capacitive sources. The circuit of Figure 10 shows the LTC6268 applied as a buffer, after a simple RC filter. The RLC network after the buffer acts as an absorptive filter to avoid excessive time domain reflections of the ADC glitches. The 2.048V reference establishes a midpoint input "zero" reference voltage. The LT1395 high speed current feedback amplifier and its associated resistor network attenuate the buffered signal and render it differential by forcing the common mode to virtual ground (the V_{CM} voltage provided by the ADC).

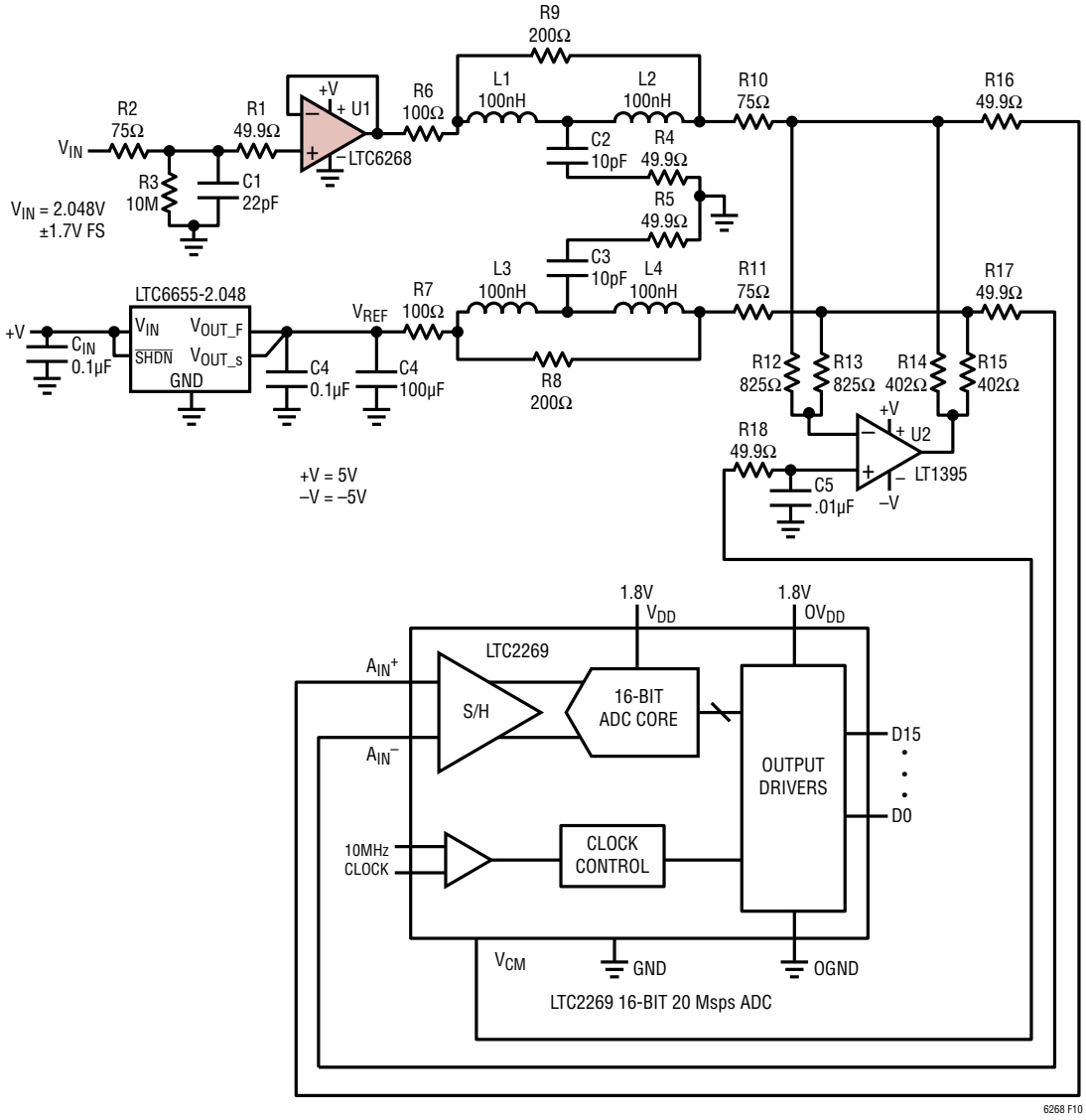


Figure 10. LTC6268 as a High-Z Buffer Driving an LT1395 as a Single-Ended to Differential Converter Into a 16-Bit ADC

APPLICATIONS INFORMATION

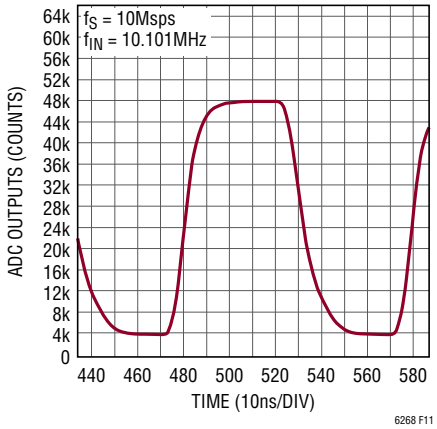


Figure 11. Sampled Time Domain Response of the Circuit of Figure 10

Figure 11 shows the time domain response of a 10.101MHz $3V_{P-P}$ input square wave, sampled at 10Msps, just 1ns slower than the waveform rate. At this rate, the waveform appears reconstructed at a rate of 1ns per sample, allowing for a more immediate view of the settling characteristics, even though each sample is really 100ns later.

Maintaining Ultralow Input Bias Current

Leakage currents into high impedance signal nodes can easily degrade measurement accuracy of fA signals. High temperature applications are especially susceptible to these issues. For humid environments, surface coating may be necessary to provide a moisture barrier.

There are several factors to consider in a low input bias current circuit. At the femtoamp level, leakage sources can come from unexpected sources including adjacent signals on the PCB, both on the same layer and from internal layers, any form of contamination on the board from the assembly process or the environment, other components on the signal path and even the plastic of the device package. Care taken in the design of the system can mitigate these sources and achieve excellent performance.

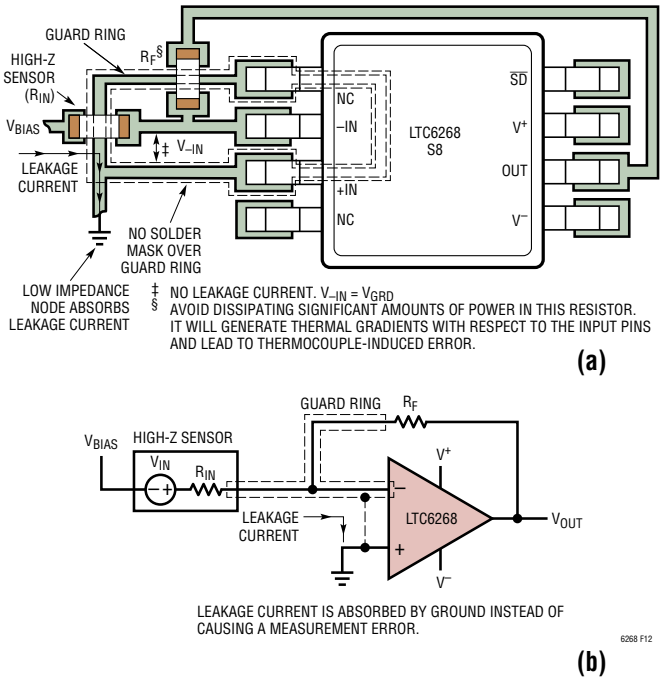


Figure 12. Example Layout of Inverting Amplifier (or Trans-Impedance) with Leakage Guard Ring

The choice of device package should be considered because although each has the same die internally, the pin spacing and adjacent signals influence the input bias current. The LTC6268/LTC6269 is available in SOIC, MSOP, DFN and SOT-23 packages. Of these, the SOIC has been designed as the best choice for low input bias current. It has the largest lead spacing which increases the impedance of the package plastic and the pinout is such that the two input pins are isolated on the far side of the package from the other signals. The gull-wing leads on this package also allow for better cleaning of the PCB and reduced contamination-induced leakage. The other packages have advantages in size and pin count but do so by reducing the input isolation. Leadless packages such as the DFN offer the minimum size but have the smallest pin spacing and may trap contaminants under the package.

APPLICATIONS INFORMATION

The material used in the construction of the PCB can sometimes influence the leakage characteristics of the design. Exotic materials such as Teflon can be used to improve leakage performance in specific cases but they are generally not necessary if some basic rules are applied in the design of conventional FR4 PCBs. It is important to keep the high impedance signal path as short as possible on the board. A node with high impedance is susceptible to picking up any stray signals in the system so keeping it as short as possible reduces this effect. In some cases, it may be necessary to have a metallic shield over this portion of the circuit. However, metallic shielding increases capacitance. Another technique for avoiding leakage paths is to cut slots in the PCB. High impedance circuits are also susceptible to electrostatic as well as electromagnetic effects. The static charge carried by a person walking by the circuit can induce an interference on the order of 100's of femtoamps. A metallic shield can reduce this effect as well.

The layout of a high impedance input node is very important. Other signals should be routed well away from this signal path and there should be no internal power planes under it. The best defense from coupling signals is distance and this includes vertically as well as on the surface. In cases where the space is limited, slotting the board around the high impedance input nodes can provide additional isolation and reduce the effect of contamination. In electrically noisy environments the use of driven guard rings around these nodes can be effective (see Figure 12). Adding any additional components such as filters to the high impedance input node can increase leakage. The leakage current of a ceramic capacitor is orders of magnitude larger than the bias current of this device. Any filtering will need to be done after this first stage in the signal chain.

Low Input Offset Voltage

The LTC6268 has a maximum offset voltage of ±2.5mV (PNP region) over temperature. The low offset voltage is essential for precision applications. There are 2 different input stages that are used depending on the input common mode voltage. To increase the versatility of the LTC6268, the offset voltages are trimmed for both regions of operation.

Rail-to-Rail Output

The LTC6268 has a rail-to-rail output stage that has excellent output drive capability. It is capable of delivering over ±40mA of output drive current over temperature. Furthermore, the output can reach within 200mV of either rail while driving ±10mA. Attention must be paid to keep the junction temperature of the IC below 150°C.

Input Protection

To prevent breakdown of internal devices in the input stage, the two op amp inputs should NOT be separated by more than 2.0V. To help protect the input stage, internal circuitry will engage automatically if the inputs are separated by >2.0V and input currents will begin to flow. In all cases, care should be taken so that these currents remain less than 1mA. Additionally, if only one input is driven, internal circuitry will prevent any breakdown condition under transient conditions. The worst-case differential input voltage usually occurs when the +input is driven and the output is accidentally shorted to ground while in a unity gain configuration.

APPLICATIONS INFORMATION

ESD

ESD Protection devices can be seen in the simplified schematic. The +IN and –IN pins use a sophisticated method of ESD protection that incorporates a total of 4 reverse-biased diodes connected as 2 series diodes to each rail. To maintain extremely low input bias currents, the center node of each of these series diode chains is driven by a buffered copy of the input voltage. This maintains the two diodes connected directly to the input pins at low reverse bias, minimizing leakage current of these ESD diodes to the input pins.

The remaining pins have traditional ESD protection, using reverse-biased ESD diodes connected to each power supply rail. Care should be taken to make sure that the voltages on these pins do not exceed the supply voltages by more than 100mV or these diodes will begin to conduct large amounts of current.

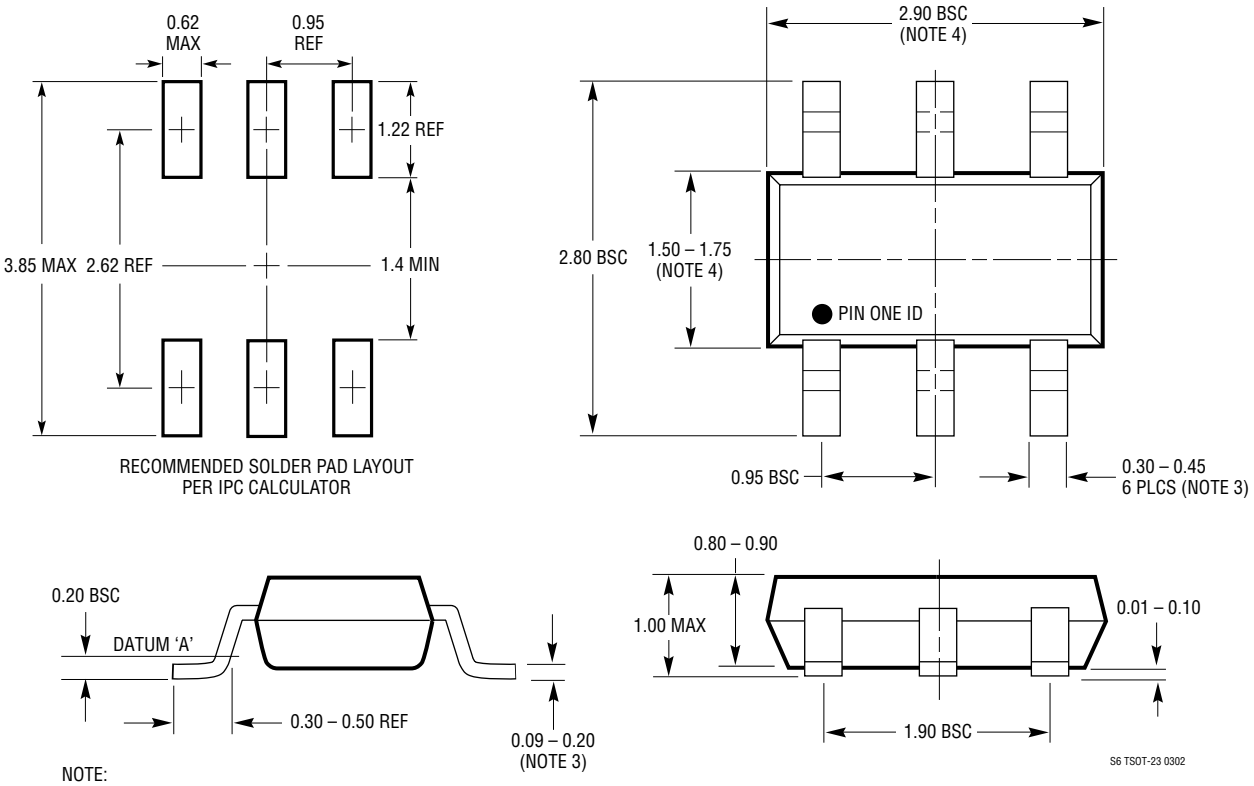
Shutdown

The LTC6268S6, LTC6268S8, and LTC6269DD have $\overline{SHDN}$ pins that can shut down the amplifier to less than 1.2mA supply current per amplifier. The $\overline{SHDN}$ pin voltage needs to be within 0.75V of V^- for the amplifier to shut down. During shutdown, the output will be in a high output resistance state, so the LTC6268 is suitable for multiplexer applications. The internal circuitry is kept in a low current active state for fast recovery. When left floating, the $\overline{SHDN}$ pin is internally pulled up to the positive supply and the amplifier is enabled.

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)

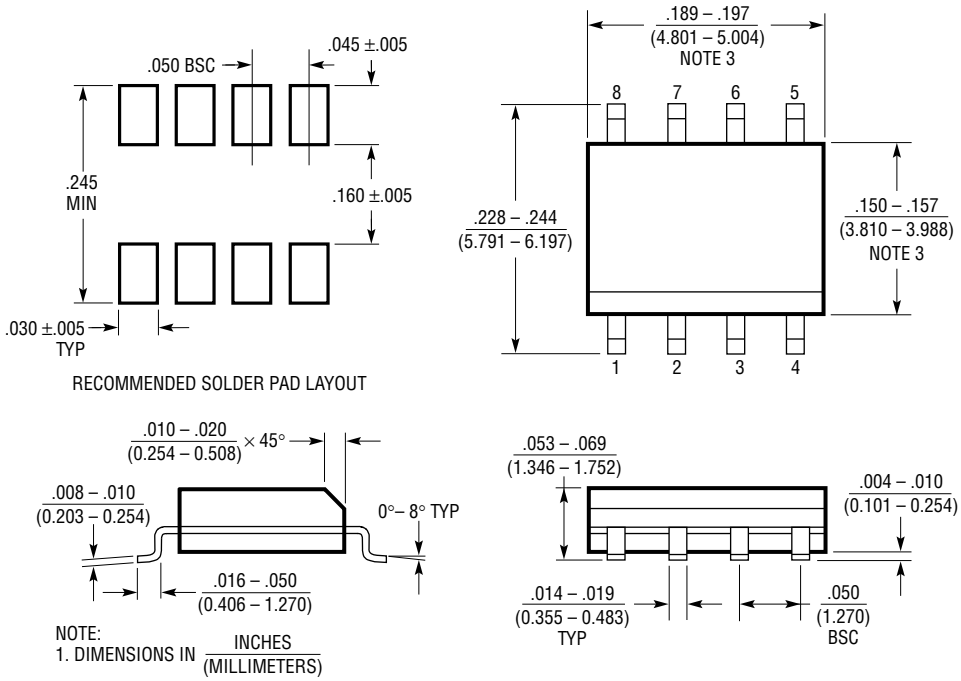


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



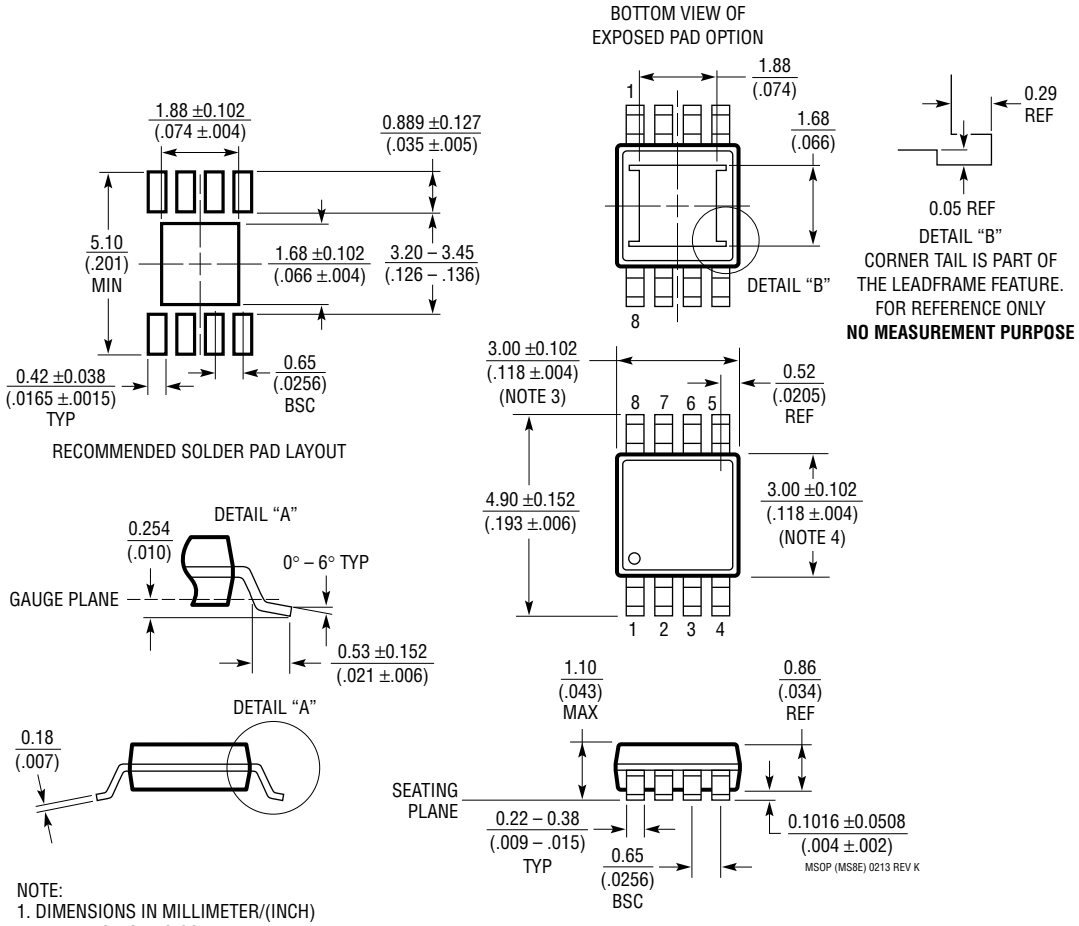
NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

S08 REV G 0212

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8E Package
8-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1662 Rev K)

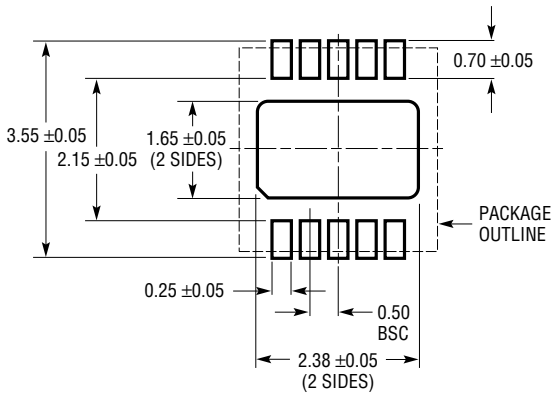


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

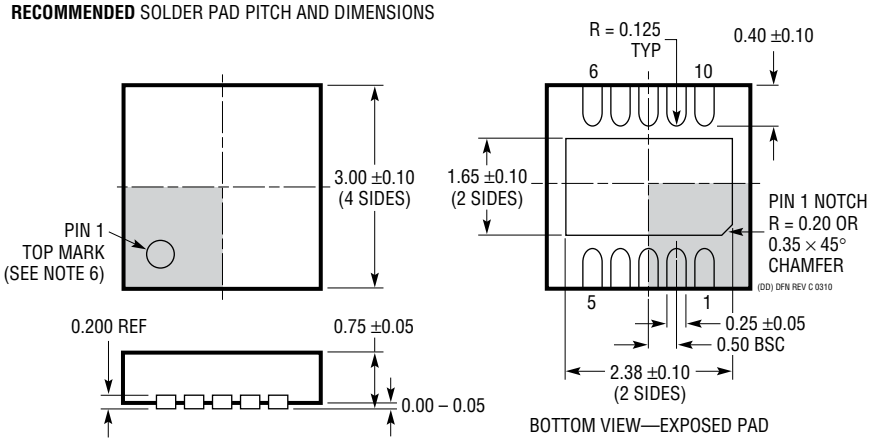
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE