# Isolated USB Data Transceiver

## FEATURES

- **Isolated USB Transceiver: 7500$V_{RMS}$ for 1 Minute**
- **CSA (IEC/UL) Approved, File #255632**
- **Reinforced Insulation**
- **USB 2.0 Full Speed and Low Speed Compatible**
- **Auto-Configuration of Bus Speed**
- **4.4V to 36V $V_{BUS}$ and $V_{BUS2}$ Operating Range**
- 3.3V LDO Output Supply Signal References $V_{LO}$ and $V_{LO2}$
- 50kV/µs Common Mode Transient Immunity
- ±20kV HBM ESD on USB Interface Pins
- 1414$V_{PEAK}$ Maximum Continuous Working Voltage
- 17.4mm Creepage Distance
- 22mm × 6.25mm Surface Mount BGA

## APPLICATIONS

- Isolated USB Interfaces
- Host, Hub, or Device Isolation
- Industrial/Medical Data Acquisition

## DESCRIPTION

The LTM®2894 is a complete galvanically-isolated USB 2.0 compatible µModule® (micromodule) transceiver.

The LTM2894 is ideal for isolation in host, hub, bus splitter or peripheral device applications. It is compatible with USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) operation. Automatic speed selection configures integrated pull-up resistors on the upstream port to match those sensed on the downstream device.

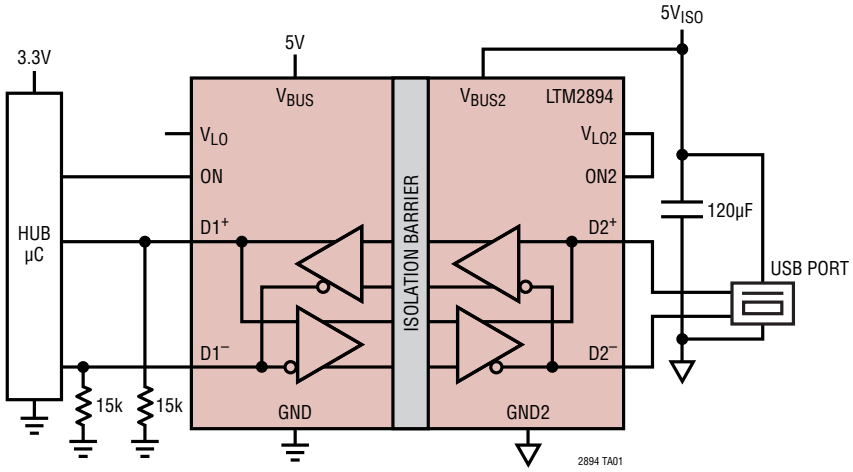
The isolator µModule technology uses coupled inductors to provide 7500$V_{RMS}$ of isolation and 17.4mm of creepage between the upstream and downstream USB interface. This device is ideal for systems requiring isolated ground returns or large common mode voltage variations. Uninterrupted communication is guaranteed for common mode transients greater than 50kV/µs.

Enhanced ESD protection allows this part to withstand up to ±20kV (human body model) on the USB transceiver interface pins to local supplies and ±20kV through the isolation barrier to supplies without latchup or damage.

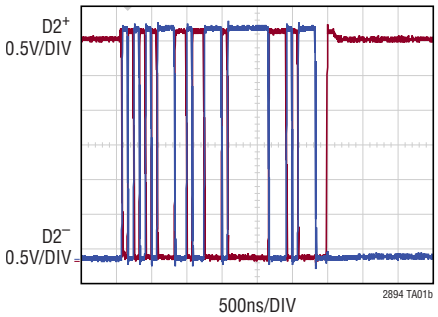


## TYPICAL APPLICATION

**Isolated V2.0 Full Speed Hub Port**




**Full Speed Data**



## ABSOLUTE MAXIMUM RATINGS

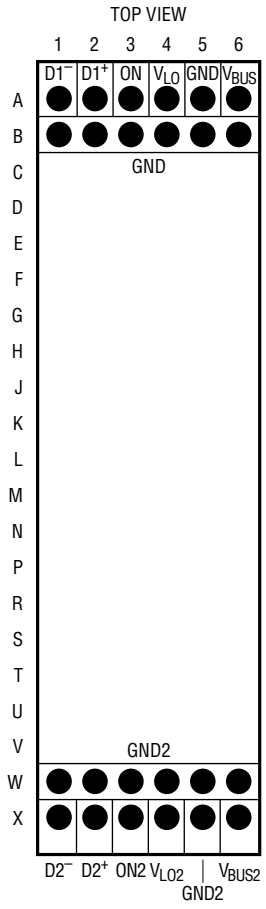
**(Note 1)**

Supply Voltages
- $V_{BUS}$ to GND ..... –0.3V to 45V
- $V_{BUS2}$ to GND2 ..... –0.3V to 45V

$V_{LO}$ to GND ..... –0.3V to 4V
$V_{LO2}$ to GND2..... –0.3V to 4V
ON to GND ..... –0.3V to ($V_{LO}$ + 0.3)
ON2 to GND2 ..... –0.3V to ($V_{LO2}$ + 0.3)
$D1^+$, $D1^-$ to GND ..... –0.3V to 5.3V
$D2^+$, $D2^-$ to GND2 ..... –0.3V to 5.3V
Operating Temperature Range
- LTM2894C (Notes 1, 3)..... 0 to 70°C
- LTM2894I (Notes 1, 3)..... –40 to 85°C
- LTM2894H (Notes 1, 3) ..... –40 to 125°C

Storage Temperature Range ..... –40 to 125°C
Maximum Internal Operating Temperature..... 125°C
Lead Temperature (Soldering, 10 sec)..... 260°C

## PIN CONFIGURATION




BGA PACKAGE
24-LEAD (22mm × 6.25mm × 2.06mm)

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 49.6°C/W, $\theta_{JB}$ = 33.7°C/W, $\theta_{JCTOP}$ = 26°CW, $\theta_{JCBOT}$ = 34°C/W,
WEIGHT = 0.5g

## ORDER INFORMATION

| PART NUMBER | PACKAGE TYPE | BALL FINISH | PART MARKING | | MSL RATING | TEMPERATURE RANGE |
|---|---|---|---|---|---|---|
| | | | DEVICE | FINISH CODE | | |
| LTM2894CY#PBF | BGA | SAC305 (RoHS) | LTM2894Y | e1 | 3 | 0°C to 70°C |
| LTM2894IY#PBF | | | | | | –40°C to 85°C |
| LTM2894HY#PBF | | | | | | –40°C to 125°C |

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- BGA Package and Tray Drawings
- This product is not recommended for second side reflow. This product is moisture sensitive. For more information, go to Recommended BGA PCB Assembly and Manufacturing Procedures.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{BUS}$ = 5V, $V_{BUS2}$ = 5V, GND = GND2 = 0V, ON = 3.3V, ON2 = 3.3V**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | | |
| $V_{BUS}$ | Operating Supply Range (USB Bus Power Input) | | ● | 4.4 | 5 | 36 | V |
| $I_{BUSPOFF}$ | $V_{BUS}$ Supply Current Power Off | ON = 0V | ● | | 1 | 20 | µA |
| $I_{BUS}$ | $V_{BUS}$ Supply Current Power On | Figure 1, $V_{BUS}$ = 5V, $I_{VLO}$ = 0mA | ● | | 5 | 9 | mA |
| $I_{BUSSPND}$ | $V_{BUS}$ Supply Current Suspend Mode | $V_{BUS}$ = 5V, USB Suspend Timeout | ● | | 1.5 | 2.0 | mA |
| $V_{BUS2}$ | Operating Supply Range (Isolated Power Input) | | ● | 4.4 | 5 | 36 | V |
| $I_{BUS2POFF}$ | $V_{BUS2}$ Supply Current Power Off | ON2 = 0V | ● | | 1 | 10 | µA |
| $I_{BUS2}$ | $V_{BUS2}$ Supply Current Power On | Figure 1, $V_{BUS2}$ = 5V, $I_{VLO2}$ = 0mA | ● | | 5 | 9 | mA |
| $I_{BUS2SPND}$ | $V_{BUS2}$ Supply Current Suspend Mode | $V_{BUS2}$ = 5V, USB Suspend Timeout | ● | | 5 | 9 | mA |
| $V_{LO}$ | $V_{LO}$ Regulated Output Voltage Signal Reference | Figure 1, $I_{VLO}$ = 0mA | ● | 3.05 | 3.3 | 3.55 | V |
| | $V_{LO}$ Output Voltage Maximum Current Source | Figure 1 | ● | | | 10 | mA |
| $V_{LO2}$ | $V_{LO2}$ Regulated Output Voltage Signal Reference | Figure 1, $I_{VLO2}$ = 0mA | ● | 3.05 | 3.3 | 3.55 | V |
| | $V_{LO2}$ Output Voltage Maximum Current Source | Figure 1 | ● | | | 10 | mA |
| **USB Input Levels (D1⁺, D1⁻, D2⁺, D2⁻)** | | | | | | | |
| | Single-Ended Input High Voltage | | ● | 2.0 | | | V |
| | Single-Ended Input Low Voltage | | ● | | | 0.8 | V |
| | Single-Ended Input Hysteresis | | ● | | 200 | | mV |
| | Differential Input Sensitivity | $\|(D1^+ - D1^-)\|$ or $\|(D2^+ - D2^-)\|$ | ● | 0.2 | | | V |
| | Common Mode Voltage Range | $(D1^+ + D1^-)/2$ or $(D2^+ + D2^-)/2$ | ● | 0.8 | | 2.5 | V |
| **Logic Input Levels (ON, ON2)** | | | | | | | |
| | Logic Input High Voltage | | ● | 2.0 | | | V |
| | Logic Input Low Voltage | | ● | | | 0.8 | V |
| | Logic Input Current | | ● | | | ±1 | µA |
| | Logic Input Hysteresis | | | | 200 | | mV |
| **USB Output Levels (D1⁺, D1⁻, D2⁺, D2⁻)** | | | | | | | |
| | Output Low Voltage | $R_{PU}$ = 1.5kΩ to 3.6V, Figure 2 | ● | 0 | | 0.3 | V |
| | Output High Voltage | $R_{PD}$ = 15kΩ to 0V | ● | 2.8 | | 3.6 | V |
| | Differential Output Signal Cross-Point Voltage | | ● | 1.3 | | 2.0 | V |
| **Terminations** | | | | | | | |
| $R_{PU}$ | Bus Pull-Up Resistance on Upstream Facing Port | $D2^+$ or $D2^-$ Pull-Up 1.5kΩ to 3.3V | ● | 1.425 | | 1.575 | kΩ |
| $R_{PD}$ | Bus Pull-Down Resistance on Downstream Facing Port ($D2^+$ and $D2^-$) | $D2^+$ and $D2^-$ Pull-Down to GND2 | ● | 14.25 | | 15.75 | kΩ |
| $Z_{DRV}$ | USB Driver Output Resistance | | ● | 28 | | 44 | Ω |
| | USB Transceiver Pad Capacitance to GND | (Note 2) | | | 10 | | pF |

## SWITCHING CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{BUS}$ = 5V, $V_{BUS2}$ = 5V, GND = GND2 = 0V, ON = 3.3V, ON2 = 3.3V.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Low Speed USB** | | | | | | | |
| $t_{LDR}$ | Low Speed Data Rate | $C_L$ = 50pF to 450pF (Note 4) | | | 1.5 | | Mbps |
| $t_{LR}$ | Rise Time | Figure 2, $C_L$ = 50pF to 600pF | ● | 75 | | 300 | ns |
| $t_{LF}$ | Fall Time | Figure 2, $C_L$ = 50pF to 600pF | ● | 75 | | 300 | ns |
| $t_{LPRR}$,$t_{LPFF}$ | Propagation Delay | Figure 2, $C_L$ = 50pF to 600pF | ● | | 200 | 300 | ns |
| | Differential Jitter | To Next Transition (Note 8) | | | | ±45 | ns |
| | Differential Jitter | To Paired Transitions (Note 8) | | | | ±15 | ns |
| **Full Speed USB** | | | | | | | |
| $t_{FDR}$ | Full Speed Data Rate | $C_L$ = 50pF (Note 4) | | | 12 | | Mbps |
| $t_{FR}$ | Rise Time | Figure 3, $C_L$ = 50pF | ● | 4 | | 20 | ns |
| $t_{FF}$ | Fall Time | Figure 3, $C_L$ = 50pF | ● | 4 | | 20 | ns |
| $t_{FPRR}$, $t_{FPFF}$ | Propagation Delay | Figure 3, $C_L$ = 50pF | ● | 60 | 80 | 115 | ns |
| | Differential Jitter | To Next Transition (Note 8) | | | 2 | | ns |
| | Differential Jitter | To Paired Transitions (Note 8) | | | 1 | | ns |
| **Suspend** | | | | | | | |
| | Wake Up from Suspend Mode | Resume Signal | ● | | 0.25 | 10 | µs |
| **ESD HBM (Note 8)** | | | | | | | |
| | Isolation Barrier | GND to GND2 | | | ±20 | | kV |
| | $D1^+$, $D1^-$, $D2^+$, $D2^-$ | $D1^+/D1^-$ to GND, $V_{BUS}$, or $V_{LO}$<br>$D2^+/D2^-$ to GND2, $V_{BUS2}$, or $V_{LO2}$ | | | ±20<br>±20 | | kV<br>kV |
| | ON or ON2 | | | | ±4 | | kV |

## ISOLATION CHARACTERISTICS

**Specifications are at $T_A$ = 25°C.**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Isolation Barrier: GND to GND2** | | | | | | |
| $V_{ISO}$ | Rated Dielectric Insulation Voltage (Notes 6, 7) | 1 Minute (Derived from 1 Second Test) | 7500 | | | $V_{RMS}$ |
| | | 1 Second (Note 5) | 9000 | | | $V_{RMS}$ |
| | Common Mode Transient Immunity | (Note 2) | 50 | 75 | | kV/µs |
| $V_{IORM}$ | Maximum Working Insulation Voltage | (Note 2) | 1414 | | | $V_{PEAK}$, $V_{DC}$ |
| | | | 1000 | | | $V_{RMS}$ |
| | Partial Discharge | $V_{PR}$ = 2650 $V_{PEAK}$ (Note 5) | | | 5 | pC |
| CTI | Comparative Tracking Index | IEC 60112 (Note 2) | 600 | | | $V_{RMS}$ |
| | Depth of Erosion | IEC 60112 (Note 2) | | 0.017 | | mm |
| DTI | Distance Through Insulation | (Note 2) | | 0.2 | | mm |
| | Input to Output Resistance | (Notes 2, 5) | 1 | 5 | | TΩ |
| | Input to Output Capacitance | (Notes 2, 5) | | 2 | | pF |
| | Creepage Distance | (Notes 2, 5) | | 18.1 | | mm |

**CSA (Note 9)**

CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1 +A2:
Basic Insulation at 910$V_{RMS}$
Reinforced Insulation at 455$V_{RMS}$

CSA 62368-1-14 and IEC 62368-1-14:2014, second edition:
Basic Insulation at 600$V_{RMS}$
Reinforced Insulation at 455$V_{RMS}$

CSA 60601-1:14 and IEC 60601-1, third edition, +A1:
Two means of patient protection (2 MOPP) at 287.5$V_{RMS}$

UL 1577-2015:
Single Protection, 6000$V_{RMS}$ Isolation Voltage

File 255632

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Guaranteed by design and not subject to test.

**Note 3:** This µModule transceiver includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above specified maximum operating junction temperature may result in device degradation or failure.

**Note 4:** Maximum data rate is guaranteed by other measured parameters and is not directly tested.

**Note 5:** Device considered a 2-terminal device. Measurement between groups of pins A1 through B6 shorted together and pins W1 through X6 shorted together.

**Note 6:** The rated dielectric insulation voltage should not be interpreted as a continuous voltage rating.

**Note 7:** In accordance with UL1577, each device is proof tested at the 7500$V_{RMS}$ rating by applying an acceleration factor of 1.2, 9000$V_{RMS}$, for one second.

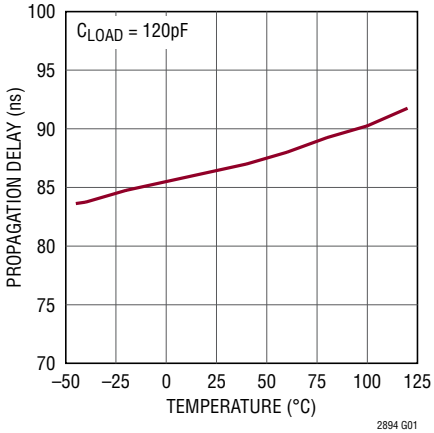
**Note 8:** Evaluated by design, not production tested.

**Note 9:** Ratings are for pollution degree 2, material group 3 and overvoltage category II where applicable. Ratings for other environmental and electrical conditions to be determined from the appropriate safety standard.

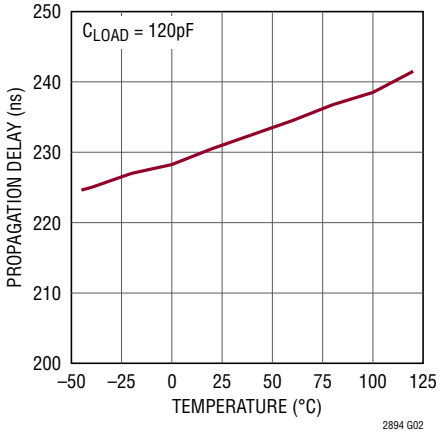
## TYPICAL PERFORMANCE CHARACTERISTICS

**$T_A$ = 25°C, unless otherwise noted. $V_{BUS}$ = 5V, $V_{BUS2}$ = 5V, GND = GND2 = 0V, ON = 3.3V, ON2 = 3.3V.**

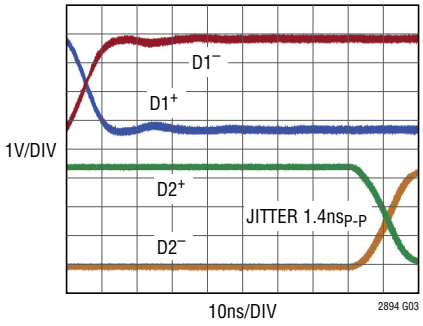
### Full Speed Propagation Delay vs Temperature



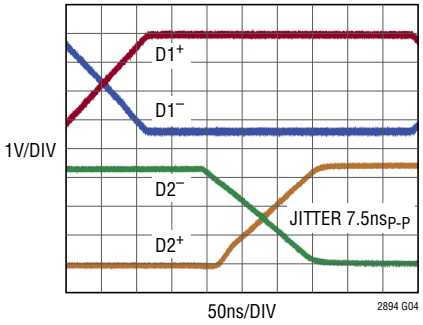

### Low Speed Propagation Delay vs Temperature



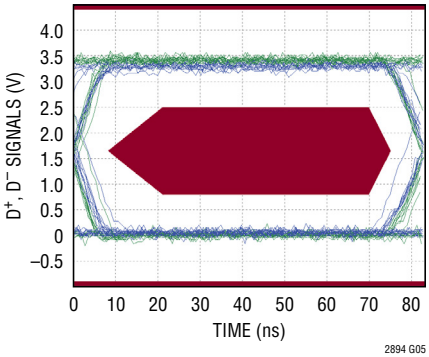

### Full Speed Differential Jitter



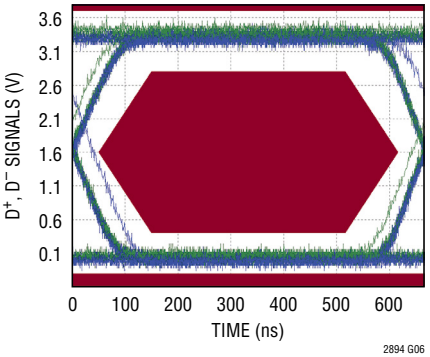

### Low Speed Differential Jitter



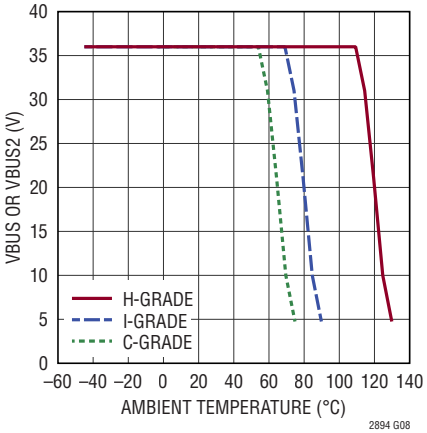

### Full Speed Eye Diagram




### Low Speed Eye Diagram

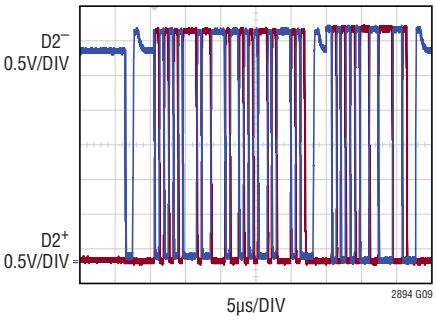



### Thermal Derating for Operating Temperature Range vs $V_{BUS}$ or $V_{BUS2}$




LIMITED BY JUNCTION TEMPERATURE RISE PER GRADE
$\theta_{JA}$ = 49.6°C/W

### Low Speed Data



# PIN FUNCTIONS

### Upstream Side

**D1⁻ (A1):** USB Data Bus Upstream Facing Negative Transceiver Pin. A 1.5k pull-up resistor is automatically configured to indicate the idle condition of the D1⁻ pin.

**D1⁺ (A2):** USB Data Bus Upstream Facing Positive Transceiver Pin. A 1.5k pull-up resistor is automatically configured to indicate the idle condition of the D1⁺ pin.

**ON (A3):** Enable. Enables data communication through the isolation barrier. If ON is high, the upstream side is enabled. If ON is low, the upstream side is held in reset. The ON pin is referenced between $V_{LO}$ and GND.

**$V_{LO}$ (A4):** Voltage Supply Output from the Upstream Side 3.3V LDO. The $V_{LO}$ pin is used as a positive reference for the ON pin and can support up to 10mA of surplus current to controlling devices. This pin contains internal ceramic bypass capacitance of 4.4µF.

**GND (A5, B1 - B6):** Upstream Circuit Ground.

**$V_{BUS}$ (A6):** Voltage Supply Input for Upstream USB Transceiver. Recommended operating range is 4.4V to 36V. Connect to the USB $V_{BUS}$ supply or an external source. This pin contains internal ceramic bypass capacitance of 0.3µF.

**PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.**

### Downstream Side

**GND2 (W1 - W6, X5):** Downstream Circuit Ground.

**D2⁻ (X1):** USB Data Bus Downstream Facing Negative Transceiver Pin. The pin has a 15k pull-down resistor to GND2.

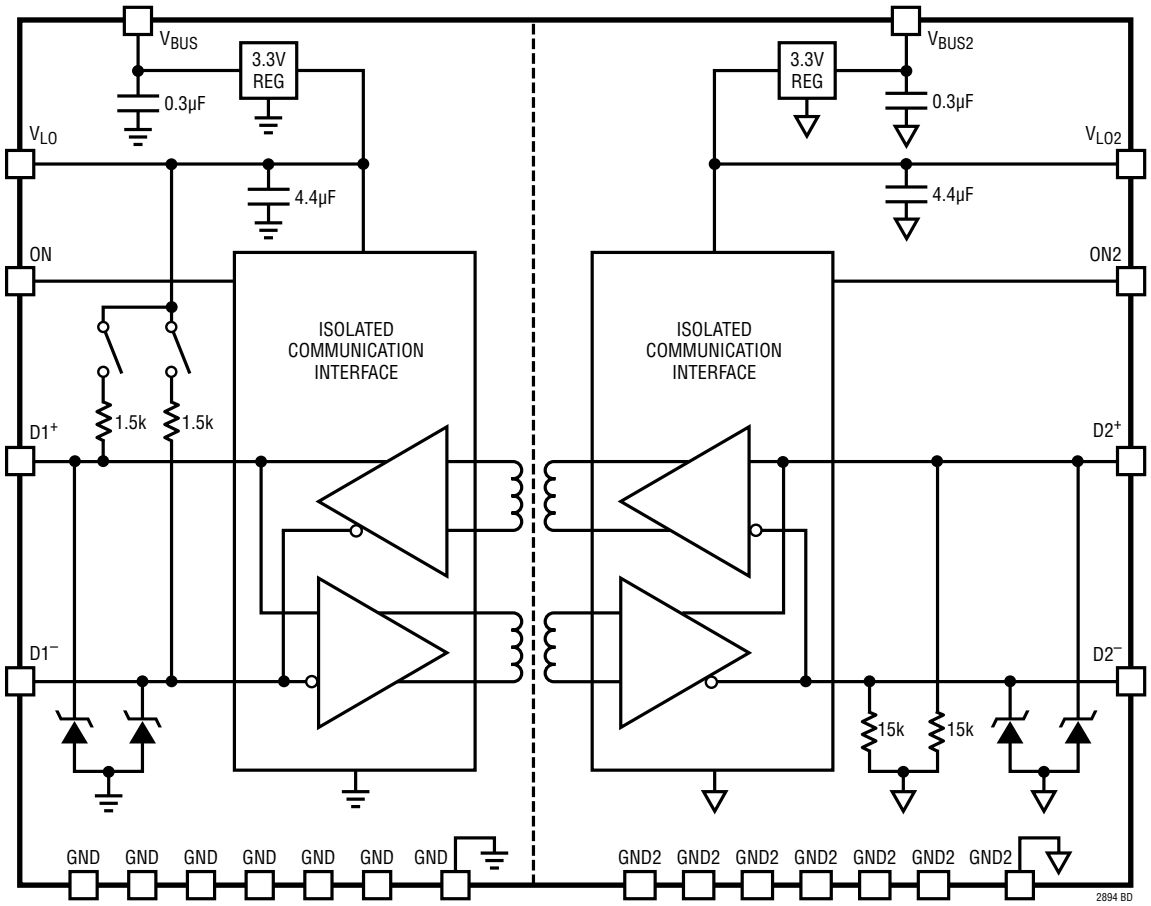
**D2⁺ (X2):** USB Data Bus Downstream Facing Positive Transceiver Pin. The pin has a 15k pull-down resistor to GND2.

**ON2 (X3):** Enable. Enables data communication through the isolation barrier. If ON2 is high, the downstream side is enabled. If ON2 is low, the downstream side is held in reset. The ON2 pin is referenced between $V_{LO2}$ and GND2.

**$V_{LO2}$ (X4):** Voltage Supply Output from the Downstream Side 3.3V LDO. The $V_{LO2}$ pin can support up to 10mA of surplus current for low voltage devices. This pin contains internal ceramic bypass capacitance of 4.4µF.

**$V_{BUS2}$ (X6):** Voltage Supply Input for the Isolated Downstream USB Transceiver. Recommended operating range is 4.4V to 36V referenced to GND2. This pin contains internal ceramic bypass capacitance of 0.3µF.

## BLOCK DIAGRAM




## TEST CIRCUITS

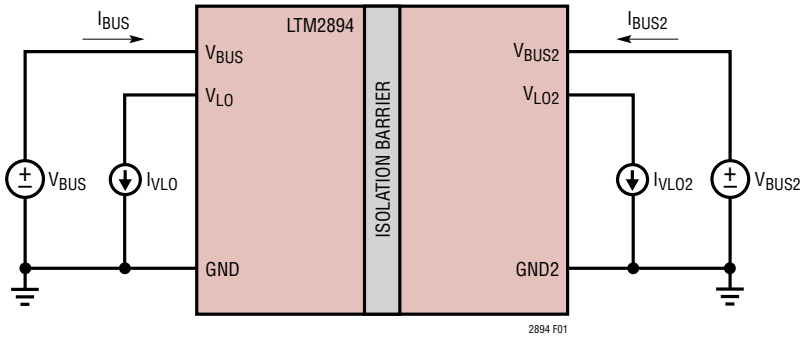



**Figure 1. Power Supply Loads**

# TEST CIRCUITS

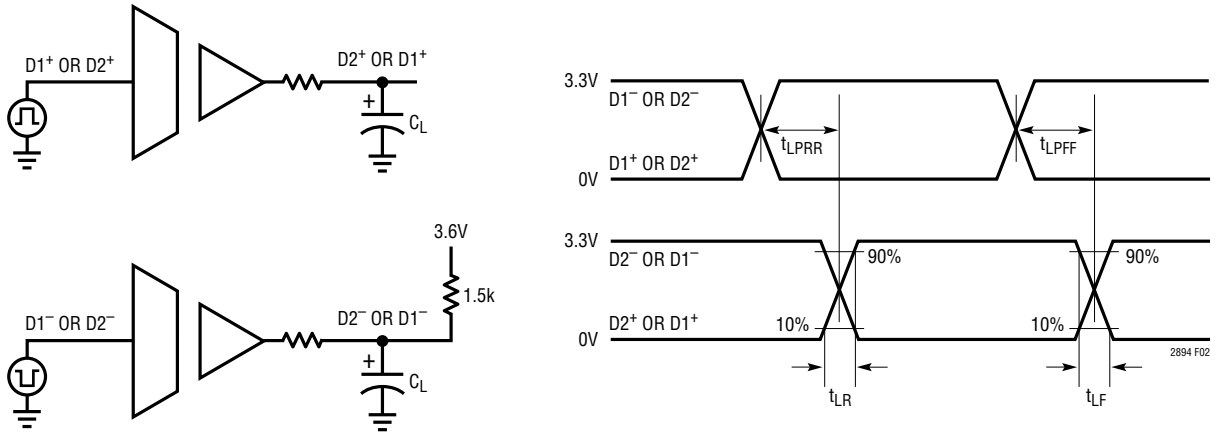



**Figure 2. Low Speed Timing Measurements**

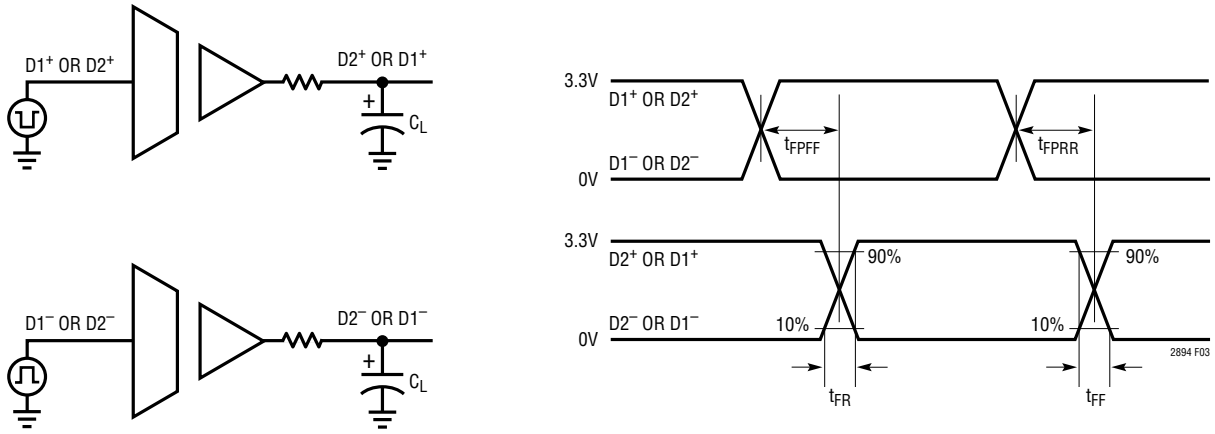



**Figure 3. Full Speed Timing Measurements**

# FUNCTIONAL TABLE

**USB Transceiver Functional Table**

| Mode | D1+ | D1– | Pull-Up Connection | D2+ | D2– |
|---|---|---|---|---|---|
| Full Speed (Idle) | 1.5kΩ Pull-Up | Host Pull-Down | D1+ | Peripheral Pull-Up | 15kΩ Pull-Down |
| Low Speed (Idle) | Host Pull-Down | 1.5kΩ Pull-Up | D1– | 15kΩ Pull-Down | Peripheral Pull-Up |
| Disconnected (Idle) | Host Pull-Down | Host Pull-Down | None | 15kΩ Pull-Down | 15kΩ Pull-Down |
| Suspend (Idle > 3ms) | Set During Idle Time | Set During Idle Time | Set During Idle Time | Peripheral or 15kΩ | Peripheral or 15kΩ |
| D1 to D2 data | IN+ | IN– | Set During Idle Time | OUT+ | OUT– |
| D2 to D1 data | OUT+ | OUT– | Set During Idle Time | IN+ | IN– |

## OPERATION

The LTM2894 µModule transceiver provides a galvanically isolated robust USB interface, complete with decoupling capacitors. An automatically configured pull up resistor is included to represent the condition of the isolated downstream USB bus to the upstream USB bus. The LTM2894 is ideal for use in USB connections where grounds between upstream hub/host and downstream devices can take on different voltages. Isolation in the LTM2894 blocks high voltage differences and eliminates ground loops and is extremely tolerant of common mode transients between ground potentials. Error free operation is maintained though common mode events exceeding 50kV/µs providing excellent noise isolation.

The integrated USB transceiver on both sides of the isolation barrier supports full and low speed modes defined in the USB 2.0 Specification. The communication through the isolation barrier for USB is bidirectional and as such the LTM2894 determines data flow direction based on which side a start of packet (SOP) begins first. The direction of data is maintained until an end of packet (EOP) pattern is observed or a timeout occurs due to a lack of activity. The USB interface maintains a small consistent propagation delay representative of a single connection or hub delay and transfers all bus state and data information.

Pull-up resistors integrated in the upstream interface automatically indicate device connections and disconnections. A downstream device connection automatically selects the proper pull-up resistor at the upstream facing port after sensing the idle state of the downstream device at connection time. Disconnection of a downstream device automatically releases the pull-up resistor on the upstream facing port allowing the upstream 15k pull-down resistors to pull the bus signals to a disconnect condition. This function makes the LTM2894 ideal for host, hub, bus splitter, or peripheral device integration.

### µModule Technology

The LTM2894 utilizes isolator µModule technology to translate signals across an isolation barrier. Signals on either side of the barrier are encoded into pulses and translated across the isolation boundary using coreless transformers formed in the µModule substrate. This system, complete with data refresh, error checking, safe shutdown on fail, and extremely high common mode immunity, provides a robust solution for bidirectional signal isolation. The µModule technology provides the means to combine the isolated signaling with our USB transceiver in one small package.

### USB Transceiver Pin Protection

The LTM2894 USB transceiver pins $D1^+$, $D1^-$, $D2^+$, and $D2^-$ have protection from ESD and short-circuit faults. The transceiver pins withstand ±20KV HBM ESD events. Overcurrent circuitry on the transceiver pins monitor fault conditions from $D1^+$ and $D1^-$ to GND, $V_{LO}$, or $V_{BUS}$ (5.3V MAX) and from $D2^+$ and $D2^-$ to GND2, $V_{LO2}$, or $V_{BUS2}$ (5.3V MAX). A current detection circuit disables the transceiver pin if the pin sinks about 40mA for greater than 600ns. The $V_{LO}$ and $V_{LO2}$ output supplies protect the USB transceiver pins from shorts to GND or GND2 respectively with a 40mA current limit.

## APPLICATIONS INFORMATION

### USB Connectivity

The LTM2894 µModule transceiver connects directly to USB ports on the upstream side and the downstream side without the addition of external components. The transceiver passes through all data and does not act as a hub or intelligent device. The bus lines are monitored for idle conditions, start of packet, and end of packet conditions to properly maintain bus speed and data direction. The series resistance, pull-up, and pull-down resistors are built into the LTM2894. The upstream facing USB port contains automatically configured 1.5k pull-up resistors which are switched in or out based on the downstream side peripheral device configuration. This implementation allows upstream reporting of the downstream bus speed and connection/disconnection conditions. Built-in 15k pull-down resistors are included from the $D2^+$ and $D2^-$ signals to GND2 supporting the downstream bus configuration.

# APPLICATIONS INFORMATION

Monitoring the USB data pins, the LTM2894 detects a K-state to begin a data packet and set the data direction. The data is monitored for an end of packet signature and a finishing J-state before the bus is released. The data pay load between the K-state and J-state is transferred through the LTM2894 isolator with a delay of approximately 80ns.

### Idle State Communication

The LTM2894 µModule transceiver maintains the conditions of the USB bus idle state by monitoring the downstream side bus idle condition and refreshing the state across the isolation barrier at a consistent rate. Furthermore, the LTM2894 monitors the speed of the downstream peripheral once connected and sets its own operation to match. Figure 4 shows the abbreviated circuitry of the automatic monitoring and reporting of the bus speeds. The $D2^+$ or $D2^-$ signals are monitored for a connection to pull-ups on $D2^+$ or $D2^-$ and the result is processed as full speed or low speed, otherwise disconnect. The idle state is communicated to the upstream side through a refresh transmission. The switches SW1 or SW2 are controlled based on the received information. SW1 is closed if $D2^+$ is detected to have a pull-up and $D2^-$ was open. SW2 is closed if $D2^-$ is detected to have a pull-up and $D2^+$ was open. Both SW1 and SW2 are opened if the downstream USB bus is disconnected. During a USB suspend, the pull-up resistor will maintain the condition prior to detecting the suspend command.

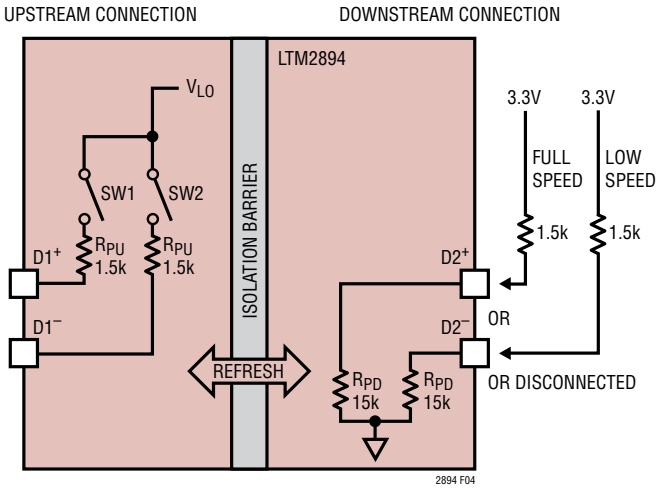



**Figure 4. Idle State Automatic Resistor Setting**

### Suspend Mode

When the upstream USB bus is idle for greater than 3ms the LTM2894 will enter suspend mode. Once the part enters suspend the $V_{BUS}$ supply current reduces below 2mA.

The LTM2894 wakes up from suspend due to disconnects, reconnects, and downstream initiated resume signaling when the LTM2894 is in a hub, host, or peripheral device. The upstream transceiver maintains observation and reports downstream transceiver disconnects and reconnects. Recovery from suspend mode occurs when a data state change is detected and may take up to 10µs.

During suspend mode, DC current drawn from $V_{LO}$ into external circuits will be supplied from $V_{BUS}$ and may exceed the limits set in the USB specification.

$V_{BUS2}$ current does not reduce in suspend mode.

### $V_{LO}$ and $V_{LO2}$ Supplies

The $V_{LO}$ and $V_{LO2}$ output supply pins are available for use as a low current 3.3V supply on both sides of the isolation barrier. They also serve as supplies for the USB interface circuitry. An internal linear regulator maintains 3.3 volts on $V_{LO}$ from the $V_{BUS}$ input supply. A separate linear regulator maintains 3.3V on $V_{LO2}$ from $V_{BUS2}$. The current is limited to 10mA for external applications. Exceeding this limit may cause degradation in the $V_{LO}$ or $V_{LO2}$ supplies and undesirable operation from the USB isolator. Connection of signals ON to $V_{LO}$ or ON2 to $V_{LO2}$ will not cause a significant change in the available current. These supplies are available to support interface logic to the isolated USB port. In order to meet the suspend mode current limit, minimize the DC current of external applications on the $V_{LO}$ output supply. $V_{LO}$ and $V_{LO2}$ are protected from over current and over temperature conditions.

### Supply Current

Loading on the multiple output supply pins of the LTM2894 affect the supply current consumption on $V_{BUS}$. The $V_{BUS}$ input supplies current to the upstream side of the transceiver and to the $V_{LO}$ pin. The $V_{BUS2}$ input supplies power to the downstream side of the transceiver and to the $V_{LO2}$ pin.

## APPLICATIONS INFORMATION

### Supply Current Equations (Typical)

Operating:

$I_{BUS} = 6mA + I_{VLO}$

$I_{BUS2} = 6mA + I_{VLO2}$

Suspend:

$I_{BUSSPND} = 1.5mA + I_{VLO}$

$I_{BUS2SPND} = 6mA + I_{VLO2}$

Off:

$I_{BUSPOFF} = 10\mu A$

$I_{BUS2POFF} = 10\mu A$

### USB 2.0 Compatibility

The LTM2894 µModule transceiver is compatible with the USB 2.0 specification of full and low speed operation. Some characteristics of the LTM2894 µModule transceiver may not support full compliance with the USB 2.0 specification.

The propagation delay for full speed data of 80ns exceeds the specification for a single hub of 44ns plus the attached cable delay of 26ns. This results from driving the data signal to the 3.3V rail prior to a K-state transition to maintain balanced crossover voltages equivalent to the cross over voltages of the successive data transitions. USB ports commonly drive the idle state bus to the 3.3V rail prior to the K-state start of packet transition. Further, the LTM2894 does not re-time the data transitions, and will propagate the edges as received, with the potential to add additional jitter or pulse width distortion.

### Hot Plug Protection

The $V_{BUS}$ and $V_{BUS2}$ inputs are bypassed with low ESR ceramic capacitors. During a hot-plug event, the supply inputs can overshoot the supplied voltage due to cable inductance. When using external power supply sources greater than 24V that can be hot-plugged, add an additional 2.2µF tantalum capacitor with greater than 1Ω of ESR, or a ceramic capacitor with a series 1Ω resistor to the $V_{BUS}$ or $V_{BUS2}$ input to reduce the possibility of exceeding absolute maximum ratings. Refer to Application Note AN88, Ceramic Capacitors Can Cause Overvoltage Transients, for a detailed discussion of this problem.

### PC Board Layout

The high integration of the LTM2894 makes PCB layout simple. However, to optimize its electrical isolation characteristics, and EMI, some layout considerations are necessary. The PCB layout in Figure 5 is a recommended configuration for a low EMI USB application. The following considerations optimize the performance of the LTM2894.

- Do not place copper between the inner columns of pads on the top or bottom on the PCB. This area must remain open to withstand the rated isolation voltage and maintain the creepage distance.
- Route $D1^-$ and $D1^+$ and $D2^-$ and $D2^+$ as differential pairs with 90Ω impedance, matching the USB cable impedance.

### RF, Magnetic Field Immunity

The isolator µModule technology used within the LTM2894 has been independently evaluated, and successfully passed the RF and magnetic field immunity testing requirements per European Standard EN 55024, in accordance with the following test standards:

EN 61000-4-3 Radiated, Radio-Frequency, Electromagnetic Field Immunity

EN 61000-4-8 Power Frequency Magnetic Field Immunity

EN 61000-4-9 Pulsed Magnetic Field Immunity

Tests were performed using an unshielded test card designed per the data sheet PCB layout recommendations. Specific limits per test are detailed in Table 2.

**Table 2. Test Frequency Field Strength**

| | |
|---|---|
| EN 61000-4-3, Annex D, 80MHz to 1GHz<br>1.4MHz to 2GHz<br>2GHz to 2.7GHz | 10V/m<br>3V/m<br>1V/m |
| EN 61000-4-8, Level 4 50Hz and 60Hz | 30A/m |
| EN 61000-4-8, Level 5 60Hz | 100A/m* |
| EN 61000-4-9, Level 5 Pulse | 1000A/m |

*Non-IEC Method

# APPLICATIONS INFORMATION

## EMI

Radiated emissions have been measured for the LTM2894 using a gigahertz transverse electromagnetic (GTEM) cell without a USB cable attached. The performance shown in Figure 7 EMI Plot was achieved with the layout structure in Figure 6. Results are corrected per IEC 61000-4-20.

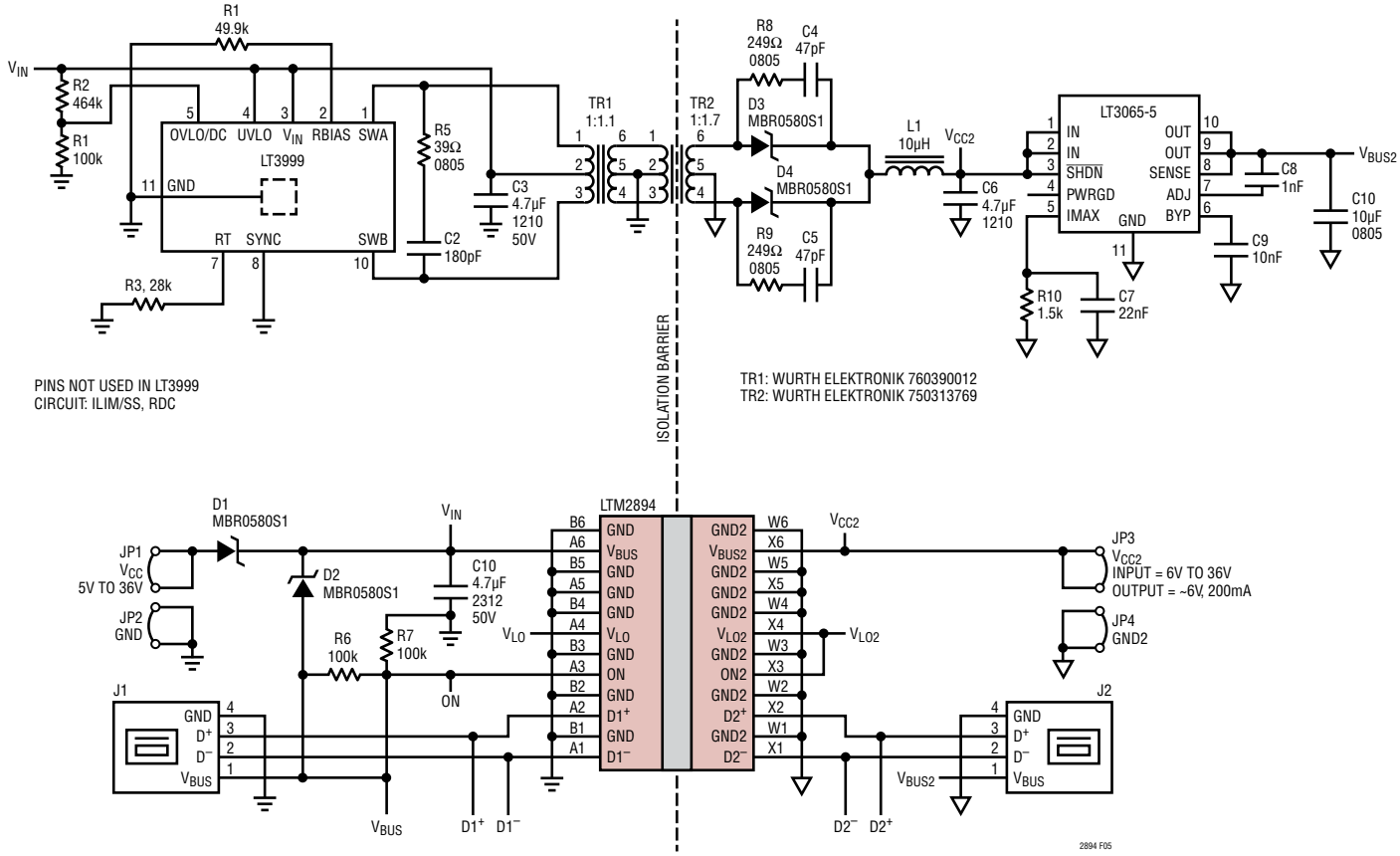
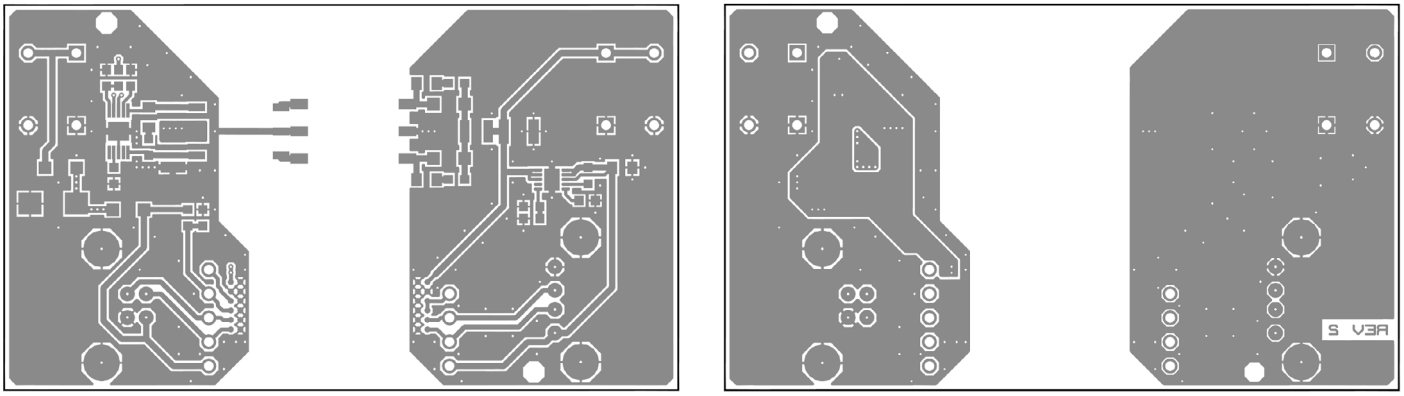



**Figure 5. Low Noise, Low EMI, 5kV$_{RMS}$, Reinforced USB Isolator Demo Circuit**

## APPLICATIONS INFORMATION



Top Layer

Bottom Layer

**Figure 6. PC Board Layout**

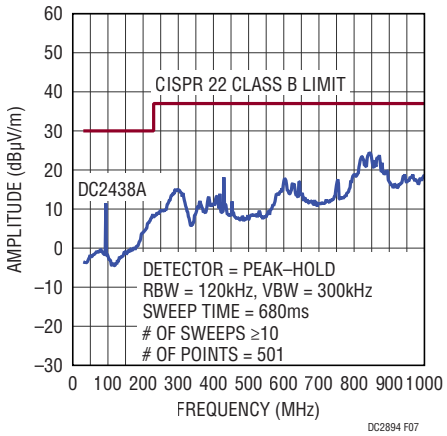



**Figure 7. EMI Plot**

## TYPICAL APPLICATIONS

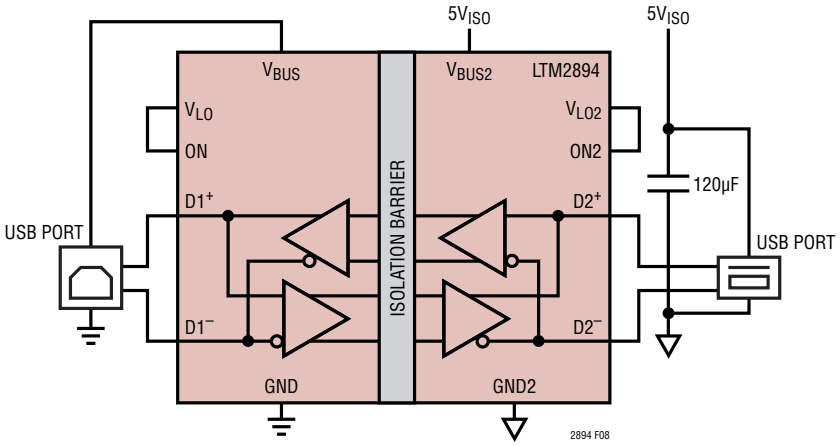



**Figure 8. Bus Splitter**

Rev A

## TYPICAL APPLICATIONS

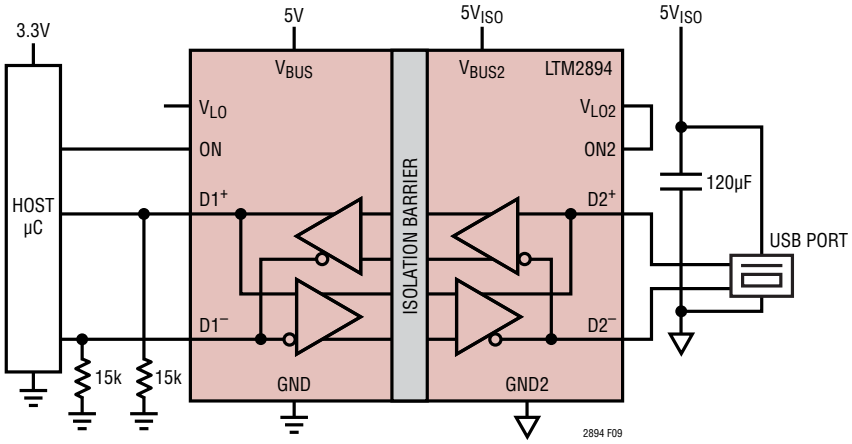



**Figure 9. USB Host Integration**

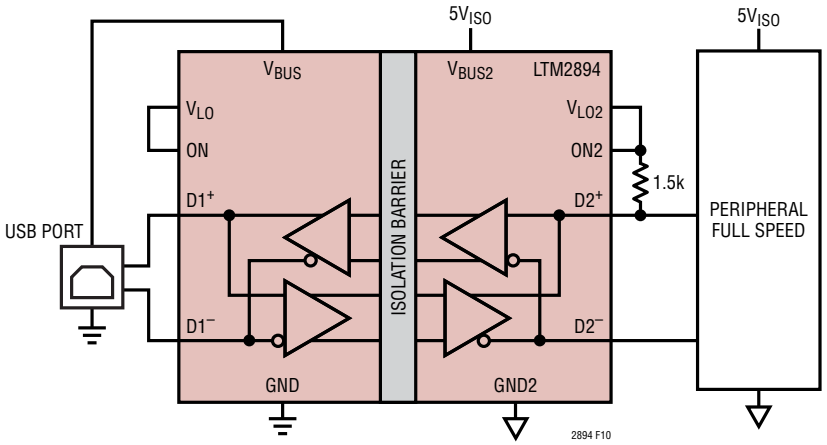



**Figure 10. Powered Peripheral Device**

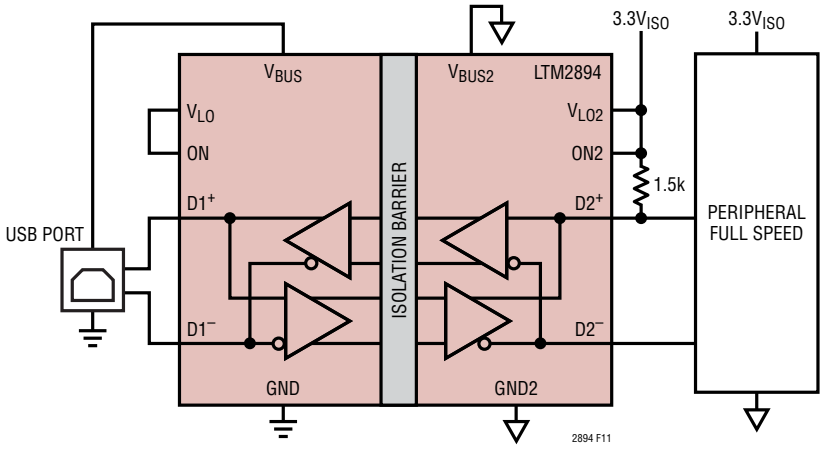
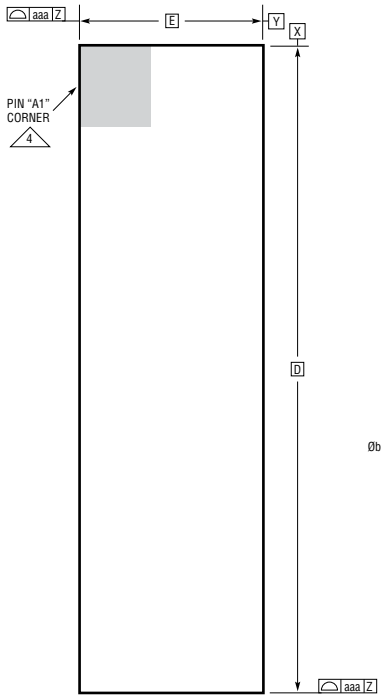


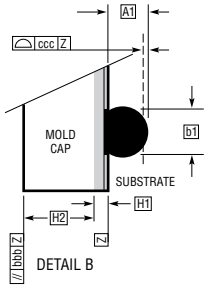

**Figure 11. Peripheral Powered with 3.3V Only**

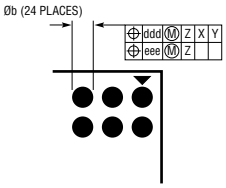
# PACKAGE DESCRIPTION

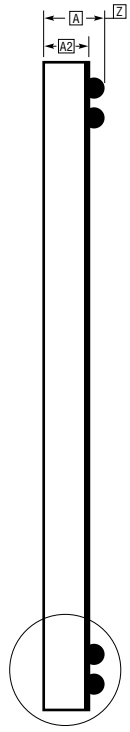
**BGA Package**
**24-Lead (22mm × 6.25mm × 2.06mm)**
(Reference LTC DWG# 05-08-1991 Rev Ø)



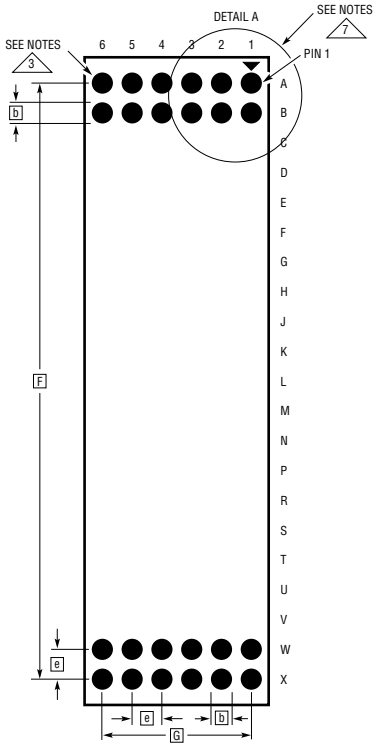

PACKAGE TOP VIEW



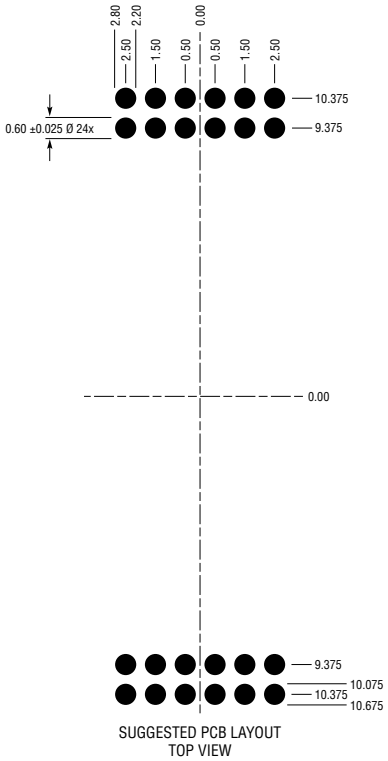




DETAIL B
PACKAGE SIDE VIEW



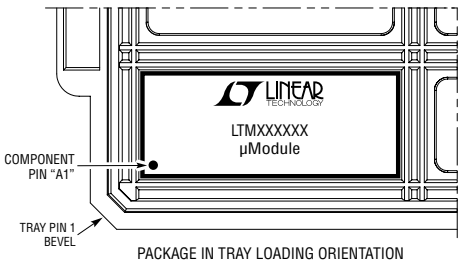

PACKAGE BOTTOM VIEW




SUGGESTED PCB LAYOUT
TOP VIEW

| DIMENSIONS | | | | |
|---|---|---|---|---|
| SYMBOL | MIN | NOM | MAX | NOTES |
| A | 1.81 | 2.06 | 2.31 | |
| A1 | 0.40 | 0.50 | 0.60 | |
| A2 | 1.41 | 1.56 | 1.71 | |
| b | 0.55 | 0.60 | 0.65 | |
| b1 | 0.45 | 0.50 | 0.55 | |
| D | | 22.0 | | |
| E | | 6.25 | | |
| e | | 1.0 | | |
| F | | 20.75 | | |
| G | | 5.0 | | |
| H1 | 0.46 | 0.56 | 0.66 | |
| H2 | 0.95 | 1.00 | 1.05 | |
| aaa | | | 0.15 | |
| bbb | | | 0.10 | |
| ccc | | | 0.15 | |
| ddd | | | 0.15 | |
| eee | | | 0.08 | |
| TOTAL NUMBER OF BALLS: 24 | | | | |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. SOLDER BALL COMPOSITION IS 96.5% Sn/3.0% Ag/0.5% Cu
7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY




PACKAGE IN TRAY LOADING ORIENTATION

BGA 24 1014 REV Ø

# REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 06/18 | Added UL/CSA Certifications | 1, 5 |
| | | Increased Typical Creepage Distance | 5 |