LF–7GHz Wideband Low Power Active Mixer

FEATURES

- **Wideband Frequency Range to 7GHz**
- **Low Power: 2.7V to 3.6V, 40mA Supply**
- **Supply Current Adjustable Down to 15mA**
- **Up or Downconversion**
- **OIP3: +20dBm at 3.6GHz Out**
- **Conversion Gain: +1dB**
- **Low LO Drive: –4dBm to +2dBm**
- LO Impedance Match Maintained During Shutdown
- Enable Control, 10µA Shutdown Current
- 2kV ESD (HBM and CDM)
- –40°C to 105°C Operation
- Small 2mm × 2mm 10-Lead QFN Package

APPLICATIONS

- Portable Radios
- Portable Test Instruments
- Wireless Infrastructure
- Fixed Wireless Access Equipment
- VHF & UHF Mixer
- Wireless Repeaters

DESCRIPTION

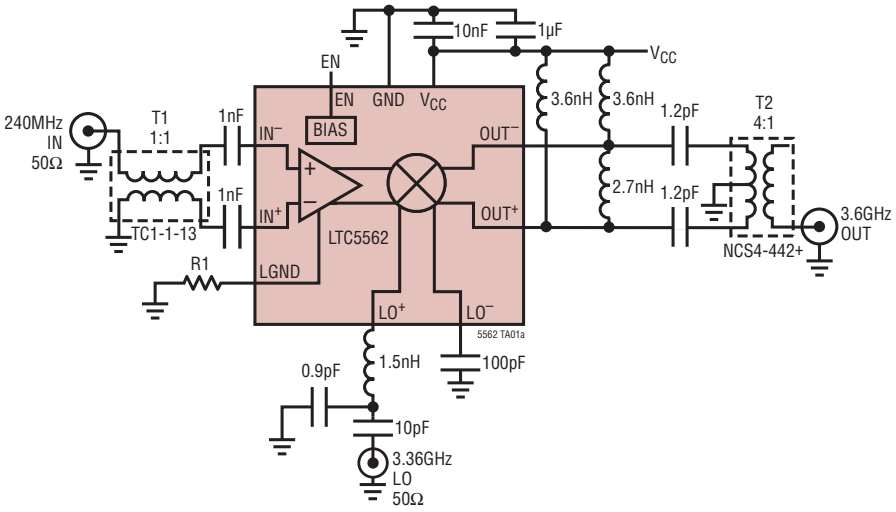
The LTC®5562 is a versatile low power mixer optimized for applications requiring wide input bandwidth, low distortion and low LO leakage. This mixer can be used for either upconverting or downconverting applications, and provides a nominal conversion gain of 1dB. The differential input is optimized for use with a 1:1 transmission-line balun, the input is 50Ω broadband matched from 30MHz to 7GHz.

The LO can be differential or single-ended and requires only –1dBm of LO power to achieve excellent distortion and noise performance. The impedance match at the LO input is maintained during shutdown. This mixer offers low LO leakage, greatly reducing the need for output filtering to meet LO suppression requirements.

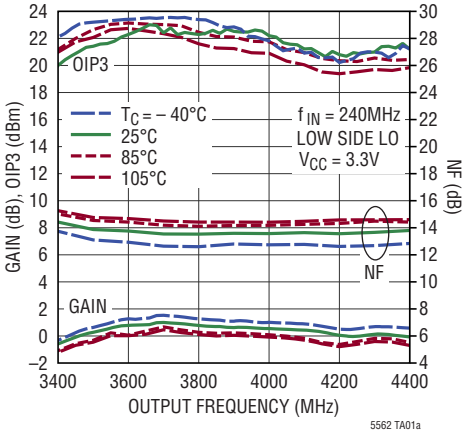
The LTC5562 uses a 3.3V supply for low power consumption and the enable control allows the part to be shut down for further power savings. The total mixer current is adjustable, by simply adding a resistor in series with the LGND pin, for applications requiring even lower power.

TYPICAL APPLICATION

3.6GHz Upconverting Mixer



Conversion Gain, OIP3 and NF vs f_{OUT}
P_{LO} = –2dBm, I_{TOTAL} = 35mA (R1 = 5Ω)

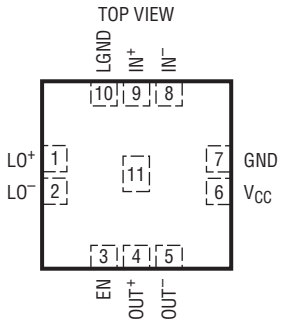


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}, OUT^+, OUT^-) 4.0V
EN Voltage ..... –0.3V to V_{CC}+0.3V
LO^+, LO^- Input Power ..... +10dBm
IN^+, IN^- Input Power ..... +15dBm
Operating Temperature Range (T_C) ..... –40°C to 105°C
Junction Temperature (T_J) ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UC PACKAGE
10-LEAD (2mm × 2mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JC} = 25°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC5562#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC5562IUC#PBF	LTC5562IUC#TRPBF	LGZQ	10-Lead (2mm × 2mm) Plastic QFN	–40°C to 105°C

Consult ADI Marketing for parts specified with wider operating temperature ranges.
Consult ADI Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at V_{CC} = 3.3V, T_C = 25°C. Test circuits shown in Figures 1 and 2. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})		●	2.7	3.3	3.6	V
Supply Current, EN = High	R1 = 0Ω R1 = 10Ω R1 = 20Ω R1 = 60Ω			40 30 25 15	46	mA
Supply Current, EN = Low	Shutdown			10		µA
Enable Logic Input (EN)						
EN Input High Voltage (On)		●	1.8			V
EN Input Low Voltage (Off)		●			0.5	V
EN Input Current	–0.3V to V_{CC} + 0.3V	●	–15		25	µA
Turn-On Time				0.1		µs
Turn-Off Time				0.5		µs

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at V_{CC} = 3.3V, EN = High, T_C = 25°C, P_{LO} = –1dBm, R1 = 0Ω. Test circuits shown in Figures 1 and 2. (Notes 2, 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LO Input Frequency Range	External Matching Required	●		LF-9		GHz
Input Frequency Range	External Matching Required	●		LF-7		GHz
Output Frequency Range	External Matching Required	●		DC-7		GHz
Input Return Loss	Z_O = 50Ω, External Matching Required Below 30MHz			>12		dB
LO Input Return Loss	Z_O = 50Ω, External Matching Required			>10		dB
Output Impedance	Differential at 900MHz Differential at 3.5GHz Differential at 5.8GHz			650Ω || 0.3pF 350Ω || 0.3pF 120Ω || 0.3pF		R || C R || C R || C
LO Input Power	Single-Ended or Differential		–4	–1	2	dBm
LO to IN Leakage	f_{LO} = 1MHz to 1.8GHz f_{LO} = 1.8GHz to 4.5GHz f_{LO} > 4.5GHz			< –45 < –35 < –30		dBm dBm dBm
LO to OUT Leakage	f_{LO} = 1MHz to 1.8GHz f_{LO} = 1.8GHz to 4.4GHz f_{LO} > 4.4GHz			< –37 < –35 < –30		dBm dBm dBm

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = High, P_{IN} = –12dBm (–12dBm/Tone for 2-tone tests), P_{LO} = –1dBm, R1 = 0Ω, unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3, 4)

Upconverting Applications

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Conversion Gain	f_{IN} = 140MHz, f_{OUT} = 900MHz, High Side LO f_{IN} = 240MHz, f_{OUT} = 3.6GHz, Low Side LO f_{IN} = 900MHz, f_{OUT} = 5.8GHz, Low Side LO		0.3	1.5 1 2		dB dB dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C, f_{OUT} = 3.6GHz	●		–0.01		dB/°C
Two-Tone Output 3rd Order Intercept (Δf = 2MHz)	f_{IN} = 140MHz, f_{OUT} = 900MHz, High Side LO f_{IN} = 240MHz, f_{OUT} = 3.6GHz, Low Side LO f_{IN} = 900MHz, f_{OUT} = 5.8GHz, Low Side LO		18	21 19 17		dBm dBm dBm
Two-Tone Output 2nd Order Intercept	Δf_{IN} = 141MHz, f_{OUT} = 900MHz, High Side LO Δf_{IN} = 241MHz, f_{OUT} = 3.6GHz, Low Side LO Δf_{IN} = 901MHz, f_{OUT} = 5.8GHz, Low Side LO			36 36 31		dBm dBm dBm
SSB Noise Figure	f_{IN} = 140MHz, f_{OUT} = 900MHz, High Side LO f_{IN} = 240MHz, f_{OUT} = 3.6GHz, Low Side LO f_{IN} = 900MHz, f_{OUT} = 5.8GHz, Low Side LO			13.5 14.6 15.9		dB dB dB
Output Noise Floor at P_{IN} = 0dBm	f_{IN} = 240MHz, f_{OUT} = 3.6GHz, Low Side LO			–157		dBm/Hz
Input 1dB Compression	f_{IN} = 140MHz, f_{OUT} = 900MHz, High Side LO f_{IN} = 240MHz, f_{OUT} = 3.6GHz, Low Side LO f_{IN} = 900MHz, f_{OUT} = 5.8GHz, Low Side LO			6 5 4.5		dBm dBm dBm
LO-OUT Leakage	f_{IN} = 140MHz, f_{OUT} = 900MHz, High Side LO f_{IN} = 240MHz, f_{OUT} = 3.6GHz, Low Side LO f_{IN} = 900MHz, f_{OUT} = 5.8GHz, Low Side LO			–37 –35 –30		dBm dBm dBm
LO-IN Leakage	f_{IN} = 140MHz, f_{OUT} = 900MHz, High Side LO f_{IN} = 240MHz, f_{OUT} = 3.6GHz, Low Side LO f_{IN} = 900MHz, f_{OUT} = 5.8GHz, Low Side LO			–50 –39 –30		dBm dBm dBm
IN to OUT Isolation	f_{IN} = 140MHz, f_{OUT} = 900MHz, High Side LO f_{IN} = 240MHz, f_{OUT} = 3.6GHz, Low Side LO f_{IN} = 900MHz, f_{OUT} = 5.8GHz, Low Side LO			65 68 68		dB dB dB
IN-LO Isolation	f_{IN} = 140MHz, f_{OUT} = 900MHz, High Side LO f_{IN} = 240MHz, f_{OUT} = 3.6GHz, Low Side LO f_{IN} = 900MHz, f_{OUT} = 5.8GHz, Low Side LO			60 56 62		dB dB dB

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = High, P_{RF} = –12dBm (–12dBm/Tone for 2-tone tests), P_{LO} = –1dBm, R1 = 0Ω. Test circuit shown in Figure 2. (Notes 2, 3, 4)

Downconverting Applications

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Conversion Gain	f_{IN} = 900MHz, f_{OUT} = 140MHz, High Side LO f_{IN} = 3.6GHz, f_{OUT} = 456MHz, High Side LO f_{IN} = 5.8GHz, f_{OUT} = 800MHz, Low Side LO			1.9 2 2		dB dB dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C, f_{OUT} = 3.6 GHz	●		–0.01		dB/°C
Two-Tone Input 3rd Order Intercept (Δf = 2MHz)	f_{IN} = 900MHz, f_{OUT} = 140MHz, High Side LO f_{IN} = 3.6GHz, f_{OUT} = 456MHz, High Side LO f_{IN} = 5.8GHz, f_{OUT} = 800MHz, Low Side LO			19 16 14		dBm dBm dBm
SSB Noise Figure	f_{IN} = 900MHz, f_{OUT} = 140MHz, High Side LO f_{IN} = 3.6GHz, f_{OUT} = 456MHz, High Side LO f_{IN} = 5.8GHz, f_{OUT} = 800MHz, Low Side LO			13.9 14.2 14.6		dB dB dB
Output Noise Floor at P_{IN} = 0dBm	f_{IN} = 3.6GHz, f_{OUT} = 350MHz, Low Side LO			–158		dBm/Hz
Input 1dB Compression	f_{IN} = 900MHz, f_{OUT} = 140MHz, High Side LO f_{IN} = 3.6GHz, f_{OUT} = 456MHz, High Side LO f_{IN} = 5.8GHz, f_{OUT} = 800MHz, Low Side LO			7 6 5.5		dBm dBm dBm
LO-OUT Leakage	f_{IN} = 900MHz, f_{OUT} = 140MHz, High Side LO f_{IN} = 3.6GHz, f_{OUT} = 456MHz, High Side LO f_{IN} = 5.8GHz, f_{OUT} = 800MHz, Low Side LO			–45 –55 –45		dBm dBm dBm
LO-IN Leakage	f_{IN} = 900MHz, f_{OUT} = 140MHz, High Side LO f_{IN} = 3.6GHz, f_{OUT} = 456MHz, High Side LO f_{IN} = 5.8GHz, f_{OUT} = 800MHz, Low Side LO			–55 –38 –39		dBm dBm dBm
IN to OUT Isolation	f_{IN} = 900MHz, f_{OUT} = 140MHz, High Side LO f_{IN} = 3.6GHz, f_{OUT} = 456MHz, High Side LO f_{IN} = 5.8GHz, f_{OUT} = 800MHz, Low Side LO			50 60 44		dB dB dB
IN-LO Isolation	f_{IN} = 900MHz, f_{OUT} = 140MHz, High Side LO f_{IN} = 3.6GHz, f_{OUT} = 456MHz, High Side LO f_{IN} = 5.8GHz, f_{OUT} = 800MHz, Low Side LO			42 39 58		dB dB dB
1/2 IF Output Spurious Product	f_{IN} = 5400MHz, f_{LO} = 5000MHz, f_{SPUR} = 800MHz			–62		dBc
1/3 IF Output Spurious Product	f_{IN} = 5249.67Hz, f_{LO} = 4983MHz, f_{SPUR} = 800MHz			–82		dBc

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

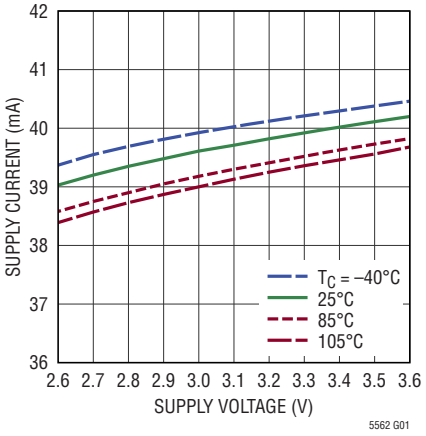
Note 2: The LTC5562 is guaranteed functional over the –40°C to 105°C case temperature range.

Note 3: SSB Noise Figure measured with a small-signal noise source, bandpass filter and 3dB matching pad on IN port, and bandpass filter on the LO input.

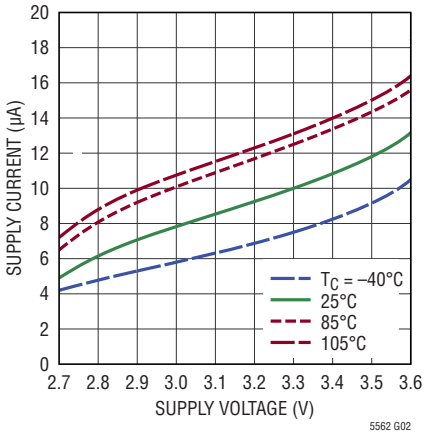
Note 4: Specified performance includes all external components and evaluation PCB losses.

TYPICAL DC PERFORMANCE CHARACTERISTICS (Test Circuit Shown in Figure 1)

Supply Current (EN = HIGH) vs Supply Voltage



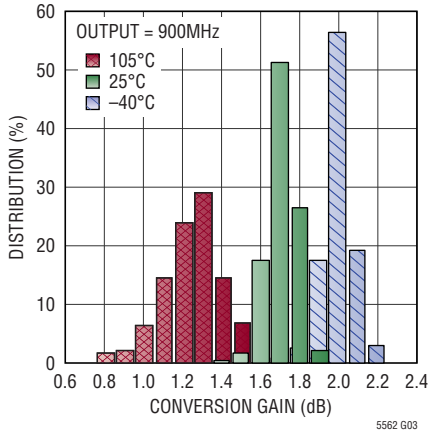
Shutdown Current (EN = LOW) vs Supply Voltage



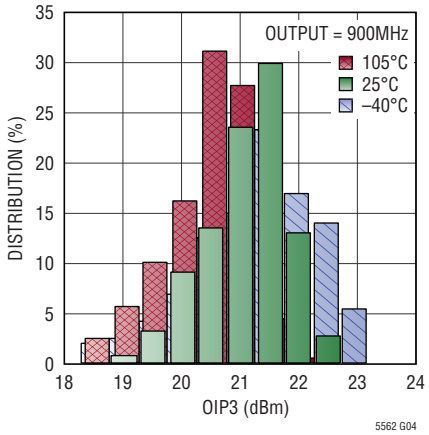
TYPICAL PERFORMANCE CHARACTERISTICS 900MHz Upconverting Application:

V_{CC} = 3.3VDC , T_C = 25°C, f_{IN} = 140MHz, P_{IN} = –12dBm (–12dBm/tone for 2-tone OIP3 tests, Δf = 2MHz). P_{LO} = 0dBm, f_{LO} = f_{IN} + f_{OUT}, High Side LO, Output Measured at 900MHz, R1 = 0Ω, unless otherwise noted.

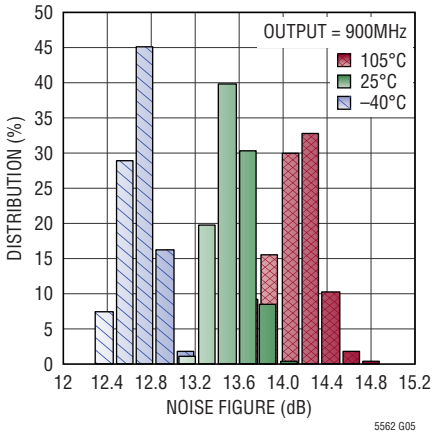
Conversion Gain Distribution



OIP3 Distribution



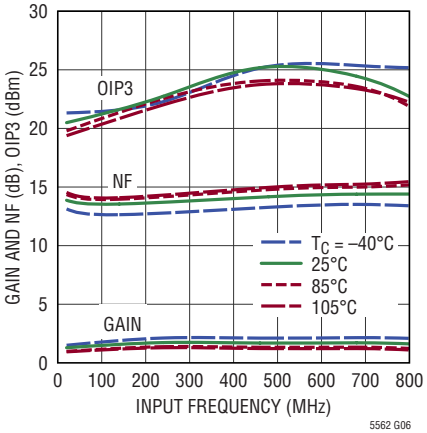
Noise Figure Distribution



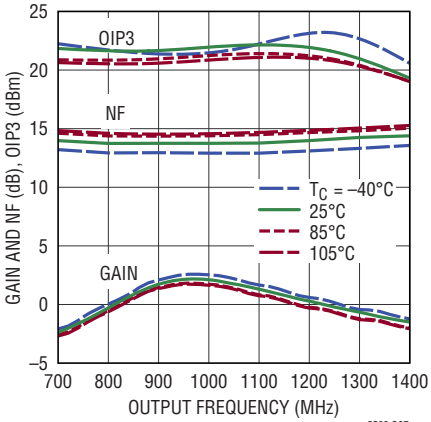
TYPICAL PERFORMANCE CHARACTERISTICS

900MHz Upconverting Application:
V_{CC} = 3.3VDC , T_C = 25°C, f_{IN} = 140MHz, P_{IN} = –12dBm (–12dBm/tone for 2-tone OIP3 tests, Δf = 2MHz). P_{LO} = –1dBm, f_{LO} = f_{OUT} + f_{IN}, High Side LO, Output Measured at 900MHz, R1 = 0Ω, unless otherwise noted. Test Circuit Shown in Figure 1.

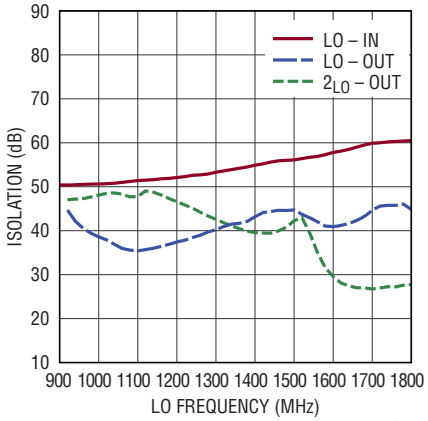
Conversion Gain, OIP3 and NF vs Input Frequency, f_{OUT} = 900MHz



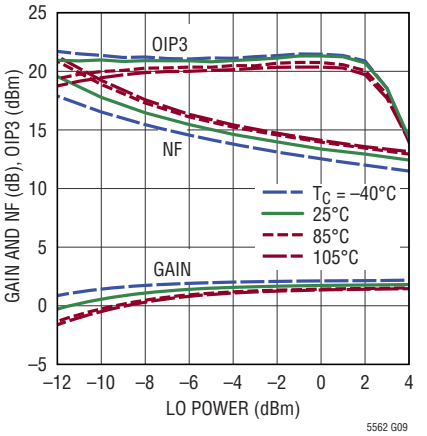
Conversion Gain, OIP3 and NF vs Output Frequency, f_{IN} = 140MHz



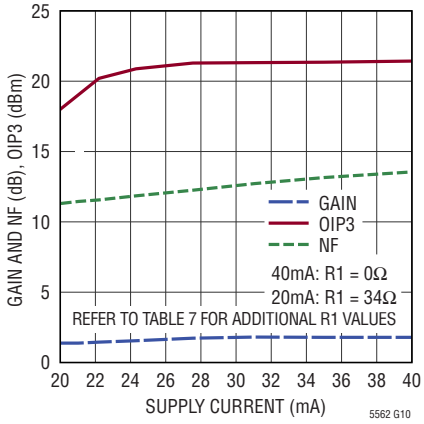
LO Isolation vs LO Frequency



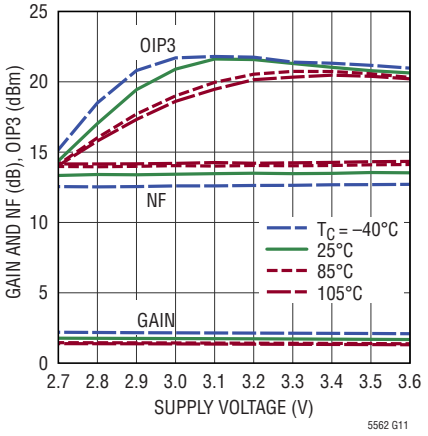
Conversion Gain, OIP3 and NF vs LO Power



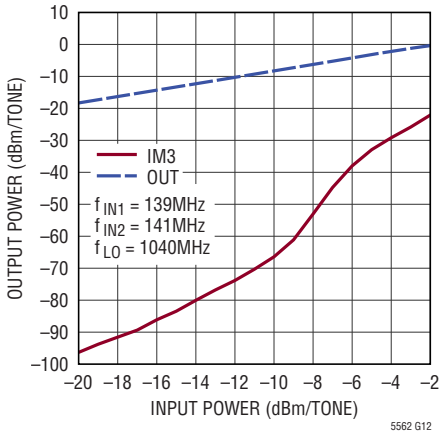
Conversion Gain, OIP3 and NF vs Supply Current



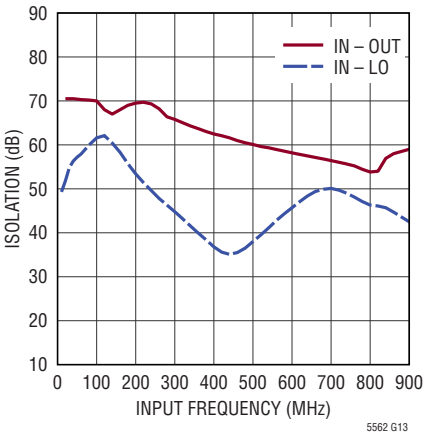
Conversion Gain, OIP3 and NF vs Supply Voltage



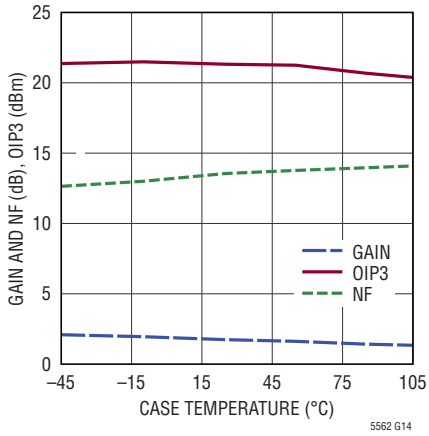
2-Tone Output and IM3 Power vs Input Power



Input Isolation vs Frequency



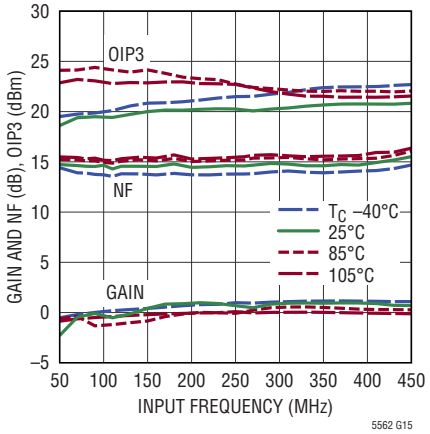
Conversion Gain, OIP3 and NF vs Case Temperature



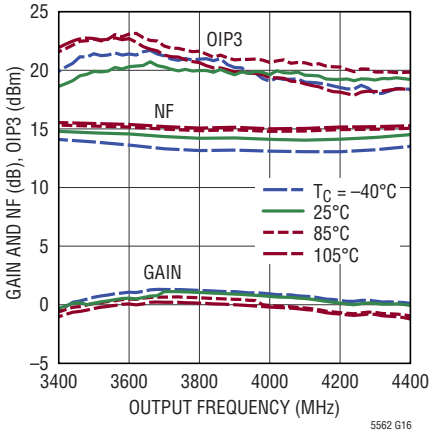
TYPICAL PERFORMANCE CHARACTERISTICS

3.6GHz Upconverting Application:
V_{CC} = 3.3VDC , T_C = 25°C, f_{IN} = 240MHz, P_{IN} = –12dBm (–12dBm/tone for 2-tone OIP3 tests, Δf = 2MHz). P_{LO} = –1dBm, f_{LO} = f_{OUT} – f_{IN}, Low Side LO, Output Measured at 3.6GHz, R1 = 0Ω, unless otherwise noted. Test Circuit Shown in Figure 1.

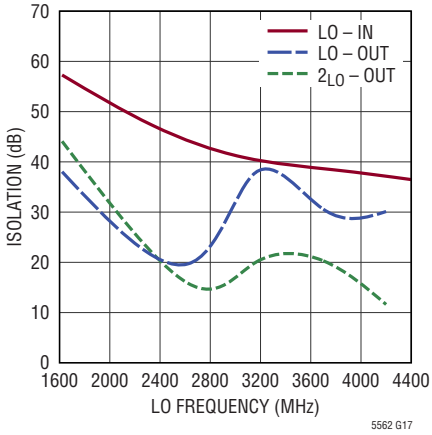
Conversion Gain, OIP3 and NF vs Input Frequency, f_{OUT} = 3.6GHz



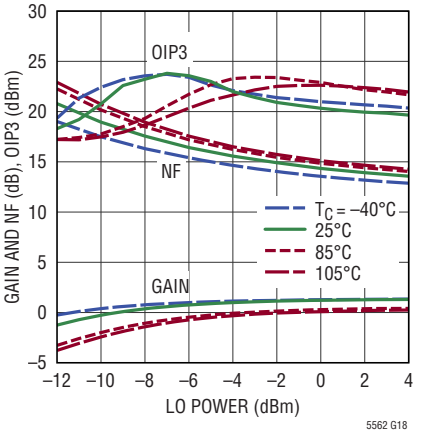
Conversion Gain, OIP3 and NF vs Output Frequency, f_{IN} = 240MHz



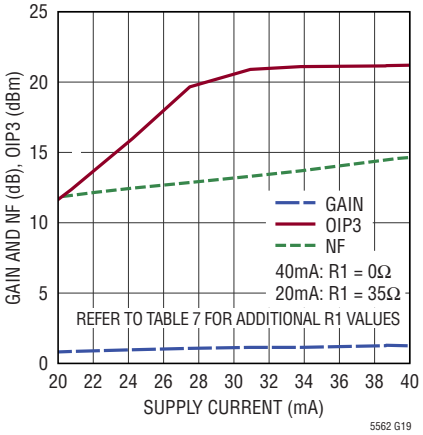
LO Isolation vs LO Frequency



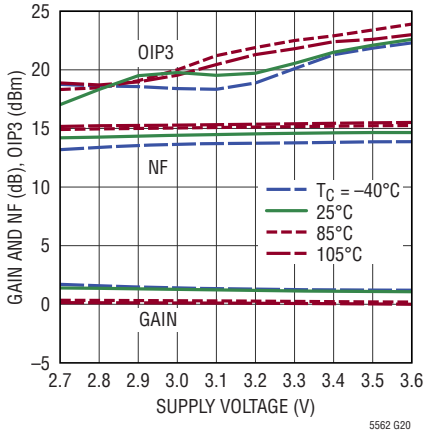
Conversion Gain, OIP3 and NF vs LO Power



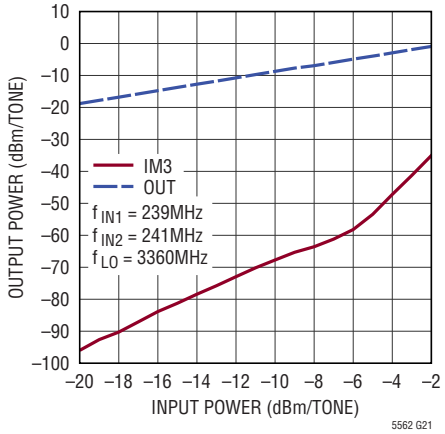
Conversion Gain, OIP3 and NF vs Supply Current



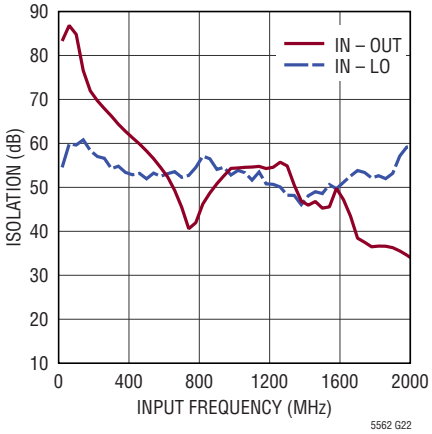
Conversion Gain, OIP3 and NF vs Supply Voltage



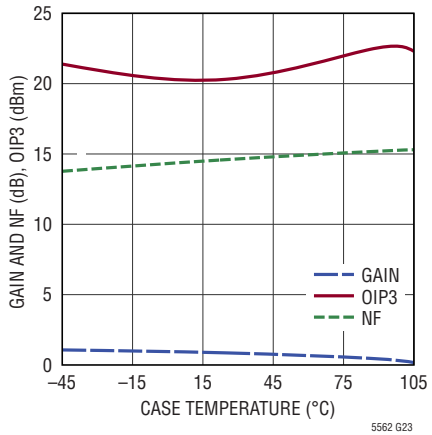
2-Tone Output and IM3 Power vs Input Power



Input Isolation vs Frequency



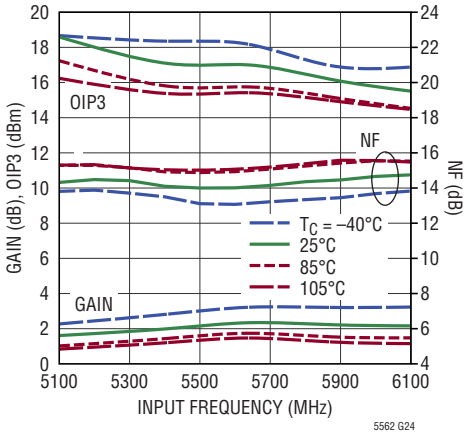
Conversion Gain, OIP3 and NF vs Case Temperature



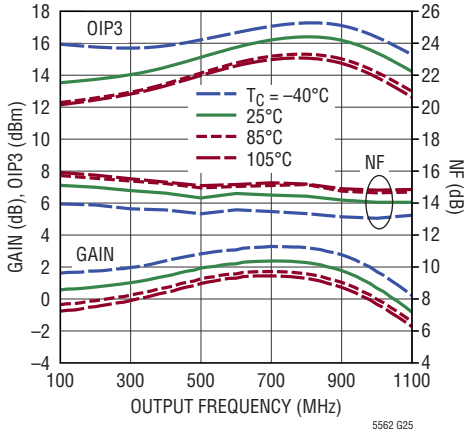
TYPICAL PERFORMANCE CHARACTERISTICS

5.8GHz Downconverting Application:
V_{CC} = 3.3VDC , T_C = 25°C, f_{IN} = 5.8GHz, P_{IN} = –12dBm (–12dBm/tone for 2-tone OIP3 tests, Δf = 2MHz). P_{LO} = –1dBm, $f_{LO} = f_{IN} – f_{OUT}$ Low Side LO, R1 = 0Ω, Output Measured at 800MHz, unless otherwise noted. Test Circuit Shown in Figure 2.

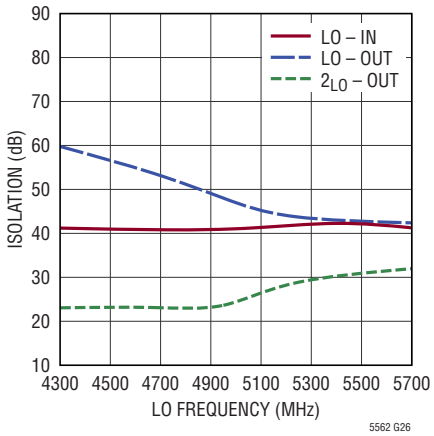
Conversion Gain, OIP3 and NF vs Input Frequency, f_{OUT} = 800MHz



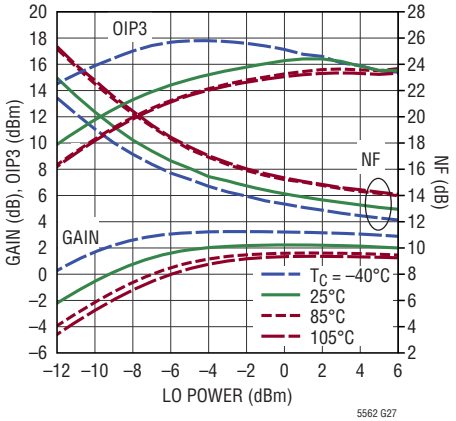
Conversion Gain, OIP3 and NF vs Output Frequency, f_{IN} = 5800MHz



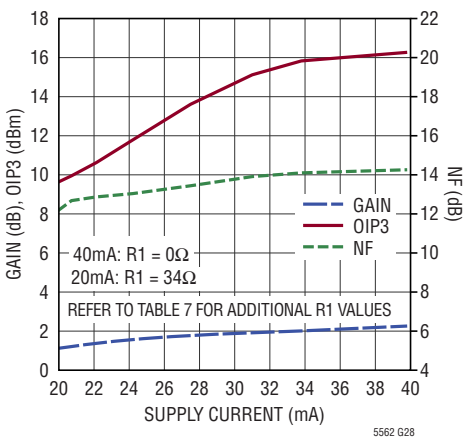
LO Isolation vs LO Frequency



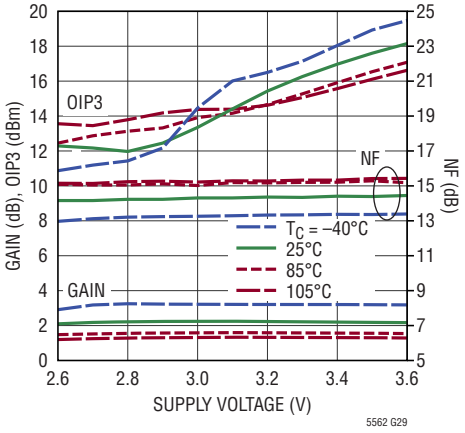
Conversion Gain, OIP3 and NF vs LO Power



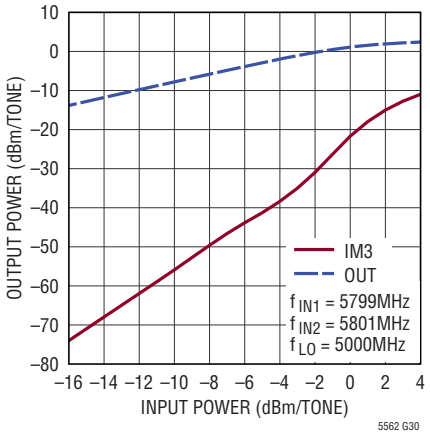
Conversion Gain, OIP3 and NF vs Supply Current



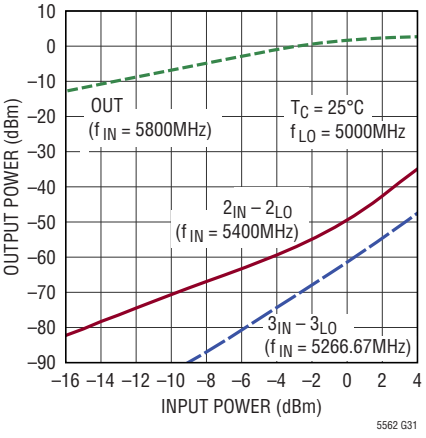
Conversion Gain, OIP3 and NF vs Supply Voltage



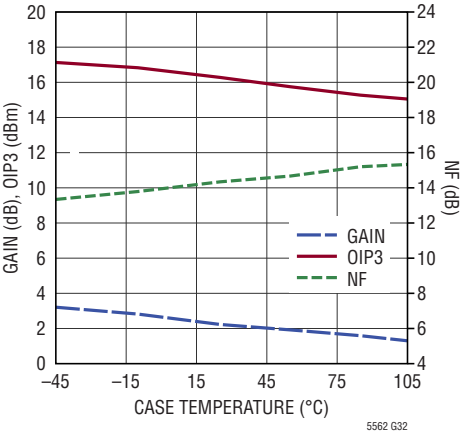
2-Tone Output and IM3 Power vs Input Power



Single Tone Output Power, 2×2 and 3×3 Spurs vs Input Power



Conversion Gain, OIP3, NF and vs Case Temperature



PIN FUNCTIONS

LO^+, LO^- (Pins 1, 2): Differential LO Input. The LO input impedance is approximately 220Ω, thus external impedance matching is recommended. An internal V_{CC} referenced bias voltage is provided to the LO inputs, therefore, DC blocking capacitors are required. The LTC5562 is characterized and production tested with a single-ended LO drive; though a differential LO drive can be used.

EN (Pin 3): Enable Pin. The LTC5562 is enabled when the applied voltage on this pin is greater than 1.8V. An applied voltage less than 0.5V will disable the IC. The voltage on the EN pin should never exceed V_{CC} by more than 0.3V.

OUT^+, OUT^- (Pins 4, 5): Differential Output. External components are required for impedance matching and differential to single-ended conversion. These pins require a low resistance DC path to V_{CC} to provide current to the mixer core. Typical DC current consumption is 18mA for each pin.

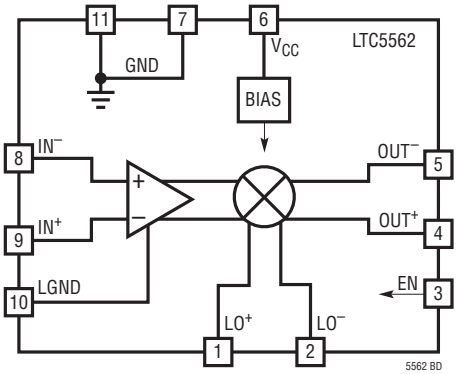
V_{CC} (Pin 6): Power Supply Pin. The supply range is 2.7V to 3.6V. This pin should be bypassed with a 10nF capacitor located close to the IC. A low impedance power plane is recommended. Typical current consumption is 4.8mA.

GND (Pins 7, 11(Exposed Pad)): Ground. These pins must be soldered to the RF ground plane on the circuit board. The exposed pad on the package provides both electrical contact to the ground and a good thermal contact to the printed circuit board.

IN^-, IN^+ (Pins 8, 9): Differential Signal Input. For optimum performance these pins should be driven with a differential signal. The input can be driven single-ended, with some performance degradation, by connecting the unused pin to RF ground through a capacitor. An internally generated 1.65V ground referenced bias voltage is present on these pins, thus DC blocking is required.

LGND (Pin 10): DC Ground Return for the Input Amplifier. For the best performance, this pin must be connected to a good low impedance ground. The typical current from this pin is 36mA. For some applications, an external resistor may be used to reduce the total current in the mixer core, which could affect performance.

BLOCK DIAGRAM



TEST CIRCUITS

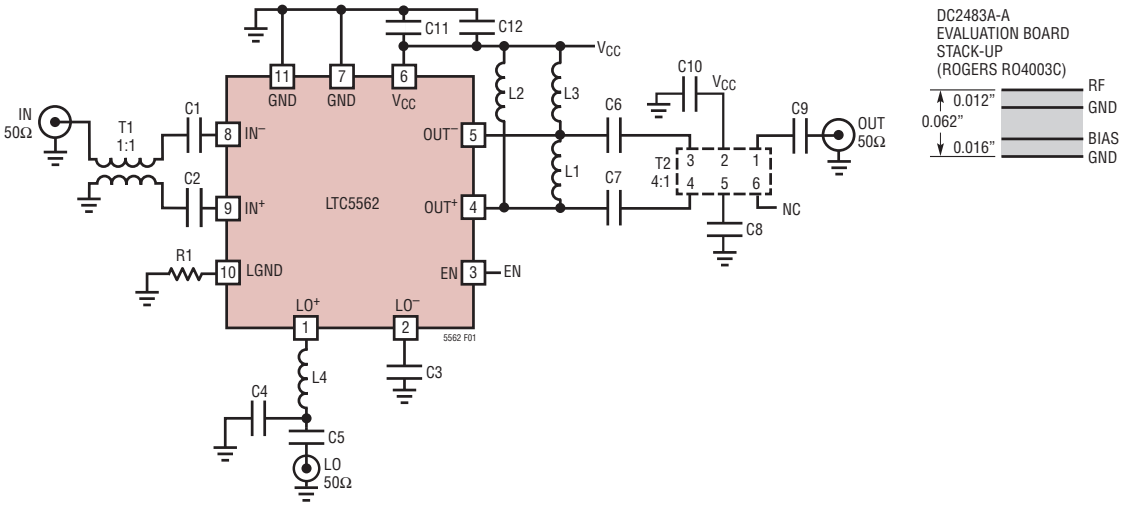


Figure 1. Low Power Upconverting Mixer Test Schematic

REF DES	VALUE	SIZE	VENDOR
C1, C2, C3, C8, C9, C10, C11	CAP, 1000pF	0402	Murata GRM Series
C12	CAP, 2.2µF	0603	Murata GRM Series
R1	0Ω	0402	
T1	XFMR, 1:1 (4.5MHz – 3000MHz)	AT224-1	Mini-Circuits TC1-1-13M+
f_{IN} = 140MHz, f_{LO} = 1040MHz, f_{OUT} = 900MHz			
C6, C7	CAP, 1.5pF	0402	Murata GRM Series
C4	Not Used	0402	
C5	CAP, 100pF	0402	Murata GRM Series
L1, L2, L3	IND, 40nH	0402	Coilcraft 0402HP Series
L4	IND, 7.5nH	0402	Coilcraft 0402HP Series
T2	XFMR, 4:1 (800MHz – 2.6GHz)	0805	Anaren Model BD0826J50200AHF
f_{IN} = 240MHz, f_{LO} = 3.36GHz, f_{OUT} = 3.6GHz*			
C4, C6, C7	CAP, 1.2pF	0402	Murata GRM Series
C5	CAP, 10pF	0402	Murata GRM Series
L1, L2, L3	IND, 3.6nH	0402	Coilcraft 0402HP Series
L4	IND, 1.5nH	0402	Murata LQG16HS1N5
T2	XFMR, 4:1 (3.3GHz – 4.2GHz)	GE0805C-1	Mini-Circuits NCS4-442+
f_{IN} = 900MHz, f_{LO} = 4.9GHz, f_{OUT} = 5.8GHz			
C6, C7	CAP, 100pF	0402	Murata GRM Series
C4	CAP, 0.2pF	0402	Murata GJM Series
C5	CAP, 0.5pF	0402	Murata GJM Series
L2, L3	IND, 3.9nH	0402	Coilcraft 0402HP Series
L1, L4	IND, 1nH	0402	Coilcraft 0402HP Series
T2	XFMR, 4:1 (4.5GHz – 6GHz)	GE0805C-1	Mini-Circuits NCS4-63+

*Standard Evaluation Board Schematic, DC2483A-A

TEST CIRCUITS

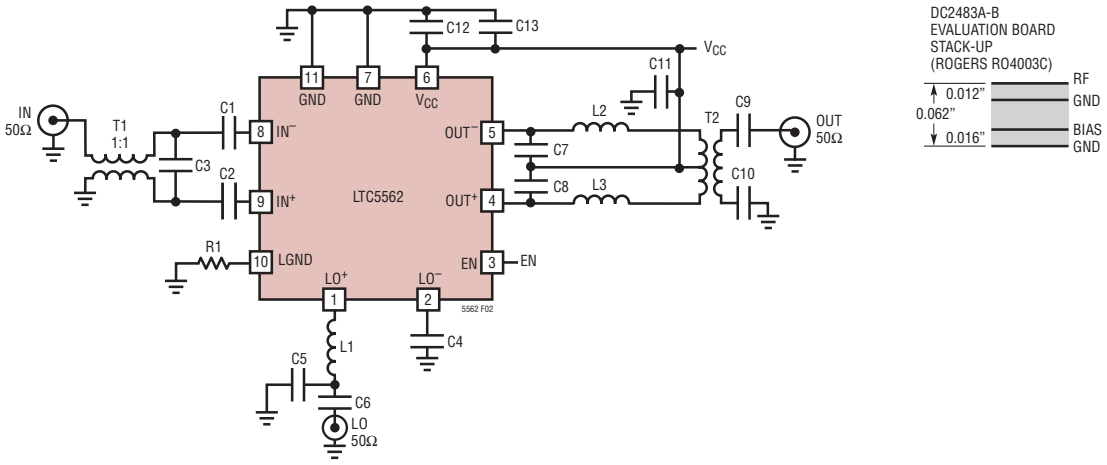


Figure 2. Low Power Downconverting Mixer Test Schematic

REF DES	VALUE	SIZE	VENDOR
C1, C2, C4, C9, C10	CAP, 1000pF	0402	Murata GRM Series
C11, C12	CAP, 10nF, 10%, X5R, 10V	0402	Murata GRM Series
C13	CAP, 2.2µF	0603	Murata GRM Series
R1	0Ω	0402	
f_{IN} = 900MHz, f_{LO} = 1040MHz, f_{OUT} = 140MHz*			
C3, C5, C7, C8	Not Used		
C6	CAP, 1000pF	0402	Murata GRM Series
L2, L3	IND, 100nH	0402	Coilcraft 0402AF
L1	IND, 7.5nH	0402	Coilcraft 0402HP
T1	XFMR, 1:1 (4.5MHz – 3000MHz)	AT224-1	Mini-Circuits TC1-1-13M+
T2	XFMR, 8:1 (2MHz – 500MHz)	AT224-1	Mini-Circuits TC8-1-10LN+
f_{IN} = 3.5GHz, f_{LO} = 3.044GHz, f_{OUT} = 456MHz			
L2, L3	CAP, 3.3pF	0402	Murata GRM Series
C3	Not Used		
C5	CAP, 0.9pF	0402	Murata GRM Series
C6	CAP, 10pF	0402	Murata GRM Series
C7, C8	IND, 56nH	0402	Coilcraft 0402HP
L1	IND, 1.5nH	0402	Murata LQG15HS1N5
T1	XFMR, 1:1 (10MHz – 8000MHz)	DB1627-1	Mini-Circuits TCM1-83X+
T2	XFMR, 4:1 (10MHz – 1900MHz)	DB714	Mini-Circuits TCM4-19
f_{IN} = 5.8GHz, f_{LO} = 4.9GHz, f_{OUT} = 800MHz			
C7, C8	Not Used		
C3, C6	CAP, 0.5pF	0402	Murata GRM Series
C5	CAP, 0.2pF	0402	Murata GRM Series
L2, L3	IND, 33nH	0402	Coilcraft 0402HP
L1	IND, 1.0nH	0402	Coilcraft 0402HP
T1	XFMR, 1:1 (10MHz – 8000MHz)	DB1627-1	Mini-Circuits TCM1-83X+
T2	XFMR, 4:1 (10MHz – 1900 MHz)	DB714	Mini-Circuits TCM4-19

*Standard Evaluation Board Schematic, DC2483A-B

APPLICATIONS INFORMATION

Introduction

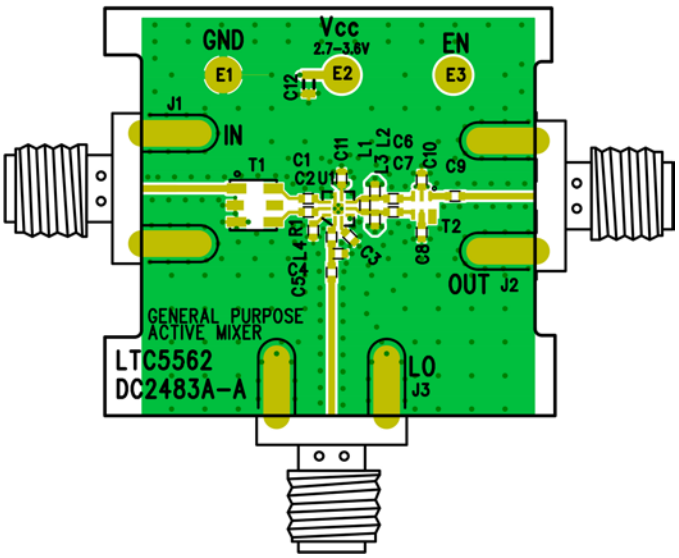
The LTC5562 is a general purpose, low power double balanced mixer. It can be configured as an upconverting or downconverting mixer that can be used in wideband or narrowband applications.

A differential common emitter stage at the mixer input allows for very broadband input matching. The IN port is differential but can be driven with a single-ended signal simply by adding a bypass cap to RF ground on one of the input pins. However, for best performance, the IN pins should be configured differentially. The LO port is differential, but can be driven with a single-ended signal, as well, simply by adding a bypass cap to RF ground on one of the input pins. LO leakage will be reduced if the LO is driven differentially. Additionally, low side or high side injection can be used on the LO port. The OUT ports have a higher impedance, designed to provide conversion gain while maintaining good linearity with lower current. External components are required to optimize the impedance match for the desired frequency range. See the Pin Functions and Block Diagram sections for a description of each pin.

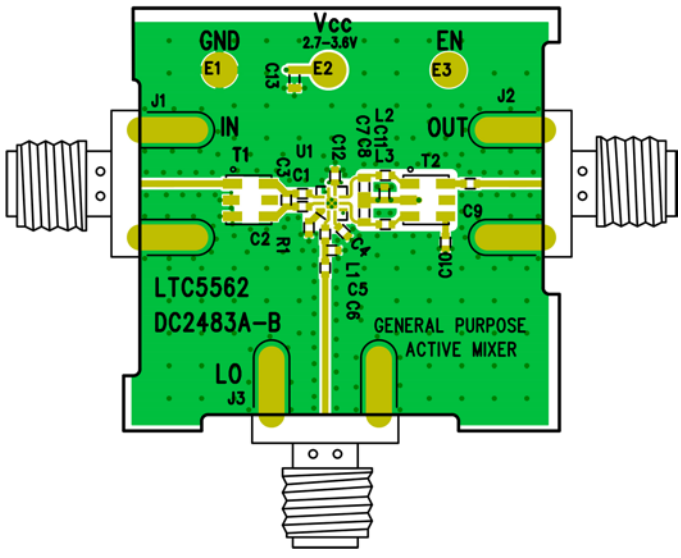
The upconverting test circuit, shown in Figure 1, utilizes bandpass matching and a 4:1 multilayer chip balun to realize a single-ended output. The downconverting test circuit, in Figure 2, uses a 8:1 wire-wound balun. The outputs may also be used to provide a differential signal, if DC blocking capacitors are used to isolate the output. Test circuit schematics showing all external components required for the data sheet specified performance are shown in Figures 1 and 2. Additional components may be used to modify the DC supply current or frequency response, which will be discussed in the following sections.

The LTC5562 can be powered down by applying a low logic signal to the EN pin. Bias voltages are maintained during shutdown to enable a fast turn-on time. The part will default to shutdown mode if the EN pin is left floating.

The upconverting and downconverting evaluation boards are shown in Figures 3(a) and 3(b).



(a) Upconversion (DC2483A-A)



(b) Downconversion (DC2483A-B)

Figure 3. LTC5562 Evaluation Board Layouts

APPLICATIONS INFORMATION

IN Port Interface

A simplified schematic of the mixer's input is shown in Figure 4. The IN+ and IN– pins drive the bases of the input amplifier and internal resistors are used for impedance matching. These pins are internally biased to a common mode voltage of 1.65V, thus capacitors C1 and C2 provide DC isolation and can be used for impedance matching. A small value capacitor, C3, can be used to improve the impedance match at higher frequencies. The 1:1 transformer, T1, provides the single-ended to differential conversion.

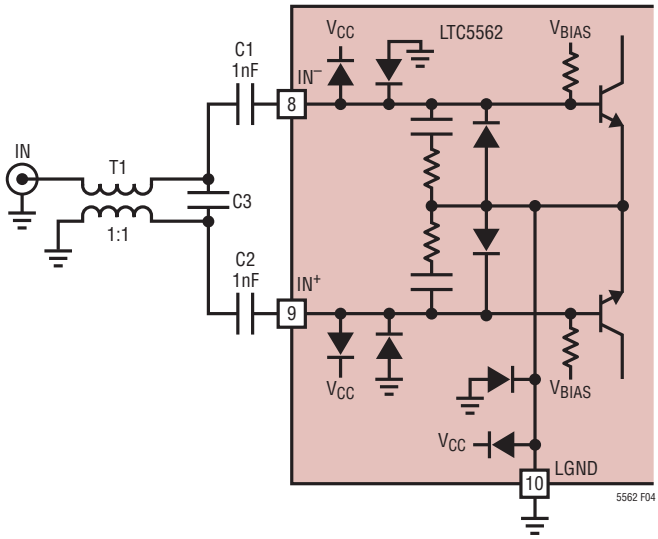


Figure 4. IN Port with External Matching

The typical return loss at the IN port is shown in Figure 5 for a selection of 1:1 transformers. Adding a 0.5pF capacitor at C3 will extend the impedance match.

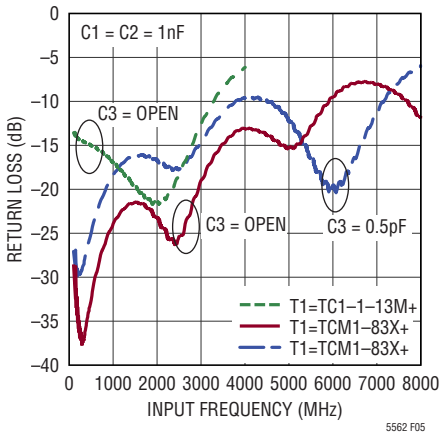


Figure 5. IN Port Return Loss

Parallel equivalent differential input impedances for various frequencies are listed in Table 1. At frequencies below 30MHz, the impedance match is limited by internal capacitors, thus additional external components may be needed to optimize the input impedance.

The tail current of the input amplifier flows through pin 10 (LGND). Typically this pin should be directly connected to ground; however, a resistor can be connected between LGND and the board ground plane to reduce the total current consumption of the LTC5562. See LGND (Reduced Current) section for more information.

Table 1. IN Port Differential Impedance

FREQ (MHz)	IMPEDANCE (Ω)			REFL. COEFF.	
	REAL*	IMAG*	PARALLEL EQUIVALENT	MAG	ANG (°)
10	133.3	–159.0	100.1pF	0.50	–39.6
100	73.3	–740.2	2.1pF	0.19	–14.3
500	72.1	–1376.5	0.2pF	0.18	–8.0
1000	71.5	–779.7	0.2pF	0.18	–14.2
1500	70.6	–498.5	0.2pF	0.18	–22.3
2000	68.1	–353.5	0.2pF	0.17	–32.7
2500	63.6	–249.3	0.3pF	0.16	–49.6
3000	59.3	–163.6	0.3pF	0.18	–72.3
3500	58.4	–110.3	0.4pF	0.25	–86.1
4000	63.5	–84.7	0.5pF	0.33	–88.5
4500	72.8	–77.3	0.5pF	0.40	–85.2
5000	78.3	–76.0	0.4pF	0.43	–83.1
5500	77.5	–74.9	0.4pF	0.43	–84.1
6000	71.7	–72.3	0.4pF	0.41	–88.6
6500	63.8	–68.1	0.4pF	0.40	–96.0
7000	54	–62.6	0.4pF	0.39	–107.2
7500	43.2	–56.6	0.4pF	0.38	–122.3
8000	33.4	–49.9	0.4pF	0.42	–138.3

* Parallel Equivalent Impedance

APPLICATIONS INFORMATION

LO Input Interface

The LTC5562 can be driven by a single-ended or differential LO. For the performance shown in the Electrical Characteristics tables and the Typical Performance curves, the LO is driven single-ended. If driven differentially, the LO to OUT leakage may improve. The LO input pins are internally biased to a V_{CC} referenced voltage, thus external capacitors are required to provide DC isolation. External components are required to optimize the impedance match for the desired frequency range. The impedance match will be maintained when the part is disabled, as well.

Table 2 lists the single-ended input impedance and reflection coefficient vs frequency for the LO input, configured as shown in Figure 6. The differential impedance versus frequency are shown in Table 3.

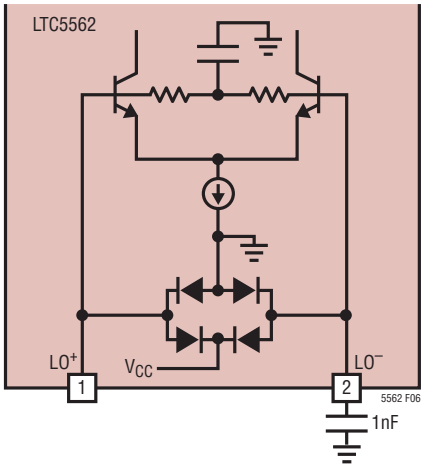


Figure 6. LO Input Schematic

Table 2. Single-Ended LO Input Impedance

FREQ (MHz)	IMPEDANCE (Ω)			REFL. COEFF.	
	REAL	IMAG	PARALLEL EQUIVALENT	MAG	ANG (°)
10	195.29	–2576.34	6.18pF	0.59	–2.38
100	146.83	–414.95	3.84pF	0.5	–15.49
500	109.66	–231.63	1.37pF	0.4	–30.07
1000	97.6	–134.35	1.18pF	0.39	–51.17
1500	83.74	–88.92	1.19pF	0.41	–73.77
2000	69.2	–61.86	1.29pF	0.45	–96.19
2500	55.43	–43.99	1.45pF	0.51	–115.94
3000	46.27	–33.62	1.58pF	0.58	–128.66
3500	41.73	–28.88	1.57pF	0.62	–134.75
4000	35.81	–26.5	1.5pF	0.63	–140.08
4500	27.13	–26.16	1.35pF	0.61	–147.71
5000	18.47	–27.4	1.16pF	0.6	–159.29
5500	12.46	–45.33	0.64pF	0.63	–172.3
6000	10.37	60.6	1.61nH	0.66	–184.12
6500	12.45	30.73	0.75nH	0.65	–190.37
7000	12.18	18.8	0.43nH	0.71	–193.06
7500	12.9	17.26	0.37nH	0.72	–194.49
8000	11.05	14.2	0.28nH	0.76	–192.46
8500	10.9	17.57	0.33nH	0.73	–191.44
9000	12.7	24.24	0.43nH	0.67	–192.41
9500	23.78	26.13	0.44nH	0.61	–208.38

Table 3. Differential LO Input Impedance

FREQ (MHz)	IMPEDANCE (Ω)			REFL. COEFF.	
	REAL	IMAG	PARALLEL EQUIVALENT	MAG	ANG (°)
10	222.3	–5085.3	3.1pF	0.63	–1.2
100	208.3	–2039.9	0.8pF	0.61	–3
500	201.4	–410.5	0.8pF	0.61	–14.8
1000	181.7	–200	0.8pF	0.59	–30.1
1500	155.7	–127.7	0.8pF	0.57	–46.5
2000	128.6	–88.6	0.9pF	0.56	–64.8
2500	104.5	–63.4	1pF	0.56	–84.6
3000	93.3	–49.1	1.1pF	0.61	–99
3500	97.8	–43.3	1.1pF	0.66	–104.5
4000	99.6	–40.2	1pF	0.69	–107.8
4500	77	–36.7	1pF	0.66	–115.1
5000	46.5	–31.4	1pF	0.61	–130.2
5500	25.7	–28.0	1pF	0.59	–149.1
6000	15.2	–31.6	0.8pF	0.61	–165.6
6500	11.9	–243.2	0.1pF	0.62	–178.6
7000	11.3	73.5	1.7nH	0.64	–184.1
7500	11.2	64.8	1.4nH	0.64	–184.5
8000	10.7	–109.2	0.2pF	0.65	–177.5
8500	12.1	–53.5	0.4pF	0.63	–173.8
9000	15.1	–100.4	0.2pF	0.55	–174.4
9500	21.2	62.7	1.1nH	0.46	–197.0

APPLICATIONS INFORMATION

The measured return loss of the matched LO input port, as drawn in Figure 7, is shown in Figure 8. The component values required for each frequency band are given in Table 4.

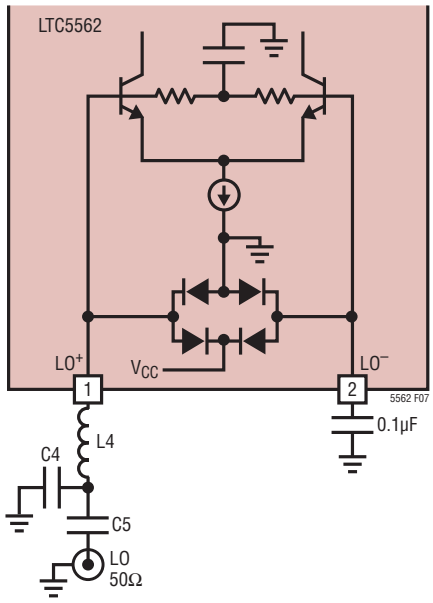


Figure 7. LO Input Schematic with External Matching

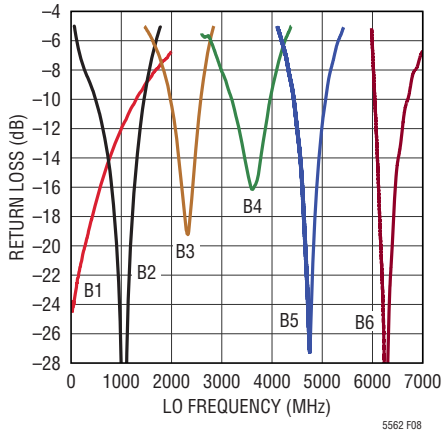


Figure 8. Single-Ended LO Input Return Loss

Table 4. Components for LO Match

FREQUENCY BAND	FREQUENCY RANGE (MHz)	L4 (Ω/nH)	C4 (Ω/pF)	C5 (pF)
B1	10 to 1200	0Ω	85Ω	1000
B2	500 to 1400	7.5nH	Open	1000
B3	2000 to 2550	3.3nH	1.2pF	3.3
B4	3200 to 3950	1.5nH	0.9pF	10
B5	4250 to 5050	1nH	0.2pF	0.5
B6	6050 to 6700	0Ω	Open	0.25

OUT Port Interface

The differential output interface is shown in Figure 9. The OUT+ and OUT– pins are open-collector outputs with internal load resistors that provide a 720Ω differential output resistance at very low frequencies. The output matching network must include a low resistance DC current path to V_{CC} to properly bias the mixer core. OUT+ and OUT– pins each require approximately 18mA of current at the maximum operating bias condition.

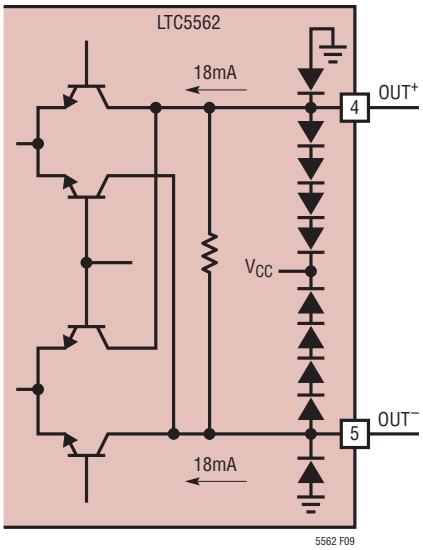


Figure 9. Output Interface

APPLICATIONS INFORMATION

Figure 10 shows the equivalent circuit of the output and Table 5 lists differential impedances for various frequencies. The impedance values are listed in parallel equivalent form, with equivalent capacitances also shown. For optimum single-ended performance, the differential output signal must be combined through an external transformer or a discrete balun circuit. In applications where differential filters or amplifiers follow the mixer, it is possible to eliminate the transformer and drive these components differentially.

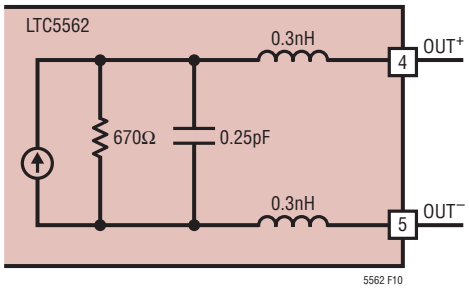


Figure 10. OUT Port Equivalent Circuit

Table 5. Differential OUT Port Impedance

FREQ (MHz)	IMPEDANCE (Ω)			REFL. COEFF.	
	REAL*	IMAG*	PARALLEL EQUIVALENT	MAG	ANG (°)
10	664.3	–26193.2	0.6pF	0.86	–0.2
100	626.6	–5116.1	0.3pF	0.85	–1.1
500	634.2	–858.4	0.4pF	0.85	–6.7
1000	598.9	–432.6	0.4pF	0.85	–13.3
1500	538	–293.7	0.4pF	0.83	–19.5
2000	487.5	–220.1	0.4pF	0.82	–25.9
2500	444.4	–168.6	0.4pF	0.81	–33.4
3000	413	–130.5	0.4pF	0.81	–42.4
3500	414.7	–107.9	0.4pF	0.82	–50.2
4000	477.6	–97.9	0.4pF	0.85	–54.5
4500	569.7	–94.7	0.4pF	0.87	–56.0
5000	587.8	–91.7	0.4pF	0.88	–57.5
5500	533.4	–86.8	0.3pF	0.87	–60.2
6000	454.2	–79.9	0.3pF	0.85	–64.5
6500	375.4	–73.3	0.3pF	0.83	–69.2
7000	334	–67.4	0.3pF	0.82	–73.9
7500	275.4	–59.6	0.4pF	0.81	–81.1
8000	249.7	–52.0	0.4pF	0.81	–89

* Parallel Equivalent Impedance

Output Matching

The output matching networks for several popular frequency bands are shown in Table 6 for both upconverting and downconverting applications. Please refer to the schematic shown in Figure 11 for component placement. Most of the matching networks in Table 6 are designed using a 4:1 impedance transformer which is convenient to transform the match from 200Ω to 50Ω, while providing a wide bandwidth output. For very low frequency applications, an 8:1 impedance transformer is used as shown in Table 6, Downconverting Application. The transformation network B1 provides a low frequency, wide bandwidth match with only 2 matching inductors. The return loss data for each matching network is shown in Figures 12 and 13.

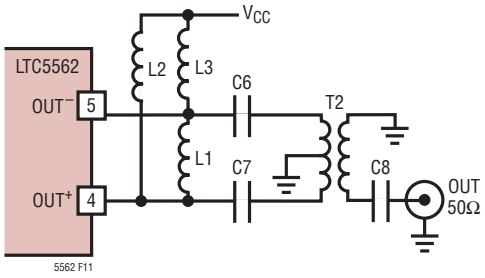


Figure 11. Output Matching Network Schematic

APPLICATIONS INFORMATION

Table 6. OUT Port Component Values

Upconverting Application						
FREQUENCY BAND	**FREQUENCY (GHz)**	**L2, L3 (nH)**	**L1 (nH)**	**C6, C7 (pF/nH)**	**C8 (pF)**	**T2**
B1	0.65 to 0.95	40	40	1.5pF	1000	Anaren 4:1 BD0826J50200AHF
B2	2.3 to 2.7	12	10	4.7nH	1000	Mini Circuits 4:1 NCS4-272+
B3	3.55 to 3.9	3.6	3.6	1.2pF	1000	Mini Circuits 4:1 NCS4-442+
B4	5.2 to 6.1	3.9	1	100pF	1000	Mini Circuits 4:1 NCS4-63+
Downconverting Application						
FREQUENCY BAND	**FREQUENCY (MHz)**	**L2, L3 (nH)**	**L1 (nH)**	**C6, C7 (pF/nH)**	**C8 (pF)**	**T2**
B1	2 to 400	Open	Open	100nH	1000	Mini Circuits TC8-1-10LN+
B2	600 to 980	Open	Open	33nH	1000	Mini Circuits 4:1 TCM4-19+
B3	1400 to 1600	5.6nH	Open	1.2pF	1000	Mini Circuits 4:1 TCM4-25+

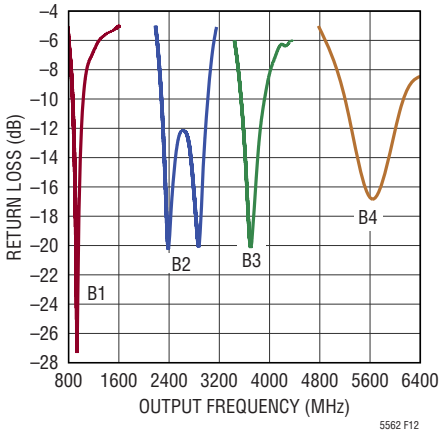


Figure 12. Output Return Loss for Upconverting Application (Refer to Table 6 for Component Values)

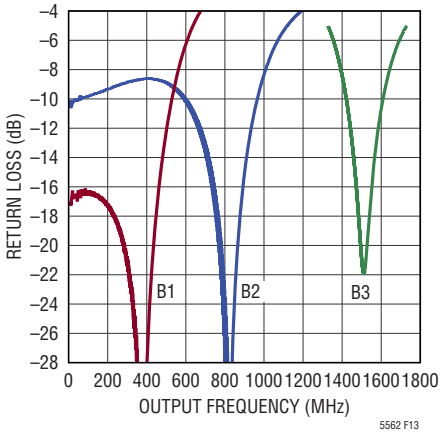


Figure 13. Output Return Loss for Downconverting Application (Refer to Table 6 for Component Values)

APPLICATIONS INFORMATION

DC and RF Grounding

The LTC5562 relies on the backside ground for both RF and thermal performance. The exposed pad must be soldered to the low impedance top-side ground plane of the board. The top-side ground should also be connected to other ground layers to aid in thermal dissipation and insure a low inductance RF ground. The LTC5562 evaluation boards (Figure 3) utilize 4 vias under the exposed pad for this purpose. In addition, pin 7, GND, is shorted to the exposed pad on the top layer.

Enable Interface

Figure 14 shows a simplified schematic of the EN pin interface. To enable the part, the applied EN voltage must be greater than 1.8V. If the enable function is not required, EN may be connected directly to V_{CC}. The voltage at the enable pin must not exceed the power supply voltage by more than 0.3V. Otherwise, supply current may be sourced through the upper ESD diode. If this is unavoidable, a current limiting resistor should be added in series with the EN pin.

When the EN voltage is less than 0.5V, the LTC5562 is in shutdown mode. Internal bias voltages are maintained to enable fast turn-on times. Refer to the Electrical Characteristics table for typical performance.

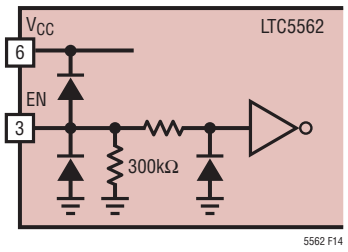


Figure 14. Enable Pin Interface

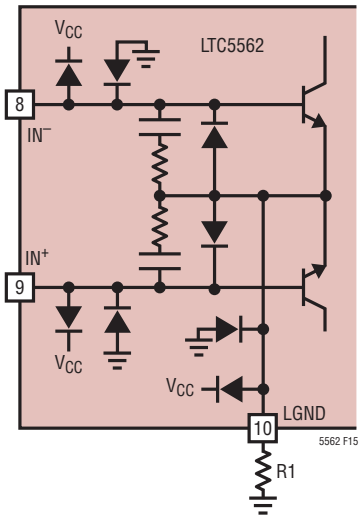


Figure 15. LGND Current Adjust Interface

LGND (Reduced Current)

To achieve the highest linearity, LGND, pin 10, should be connected directly to the ground plane. However, LGND may be used to reduce the DC current consumption of the LTC5562 by connecting a small series resistor between LGND and GND. In general, a lower bias current will reduce the linearity of the LTC5562, but will also reduce the noise figure. At low frequencies, the performance degradation due to reduced current will be small. As the operating frequency increases, the performance will decrease by a more significant amount. Refer to Table 7 for measured performance data vs LGND resistance.

Table 7. Performance Comparison vs LGND Resistance

UP MIXER		f_{IN} = 140MHz, f_{OUT} = 900MHz			f_{IN} = 240MHz, f_{OUT} = 3.6GHz		
R1 (Ω)	I_{Total} (mA)	Gain (dB)	OIP_3 (dBm)	NF (dB)	Gain (dB)	OIP_3 (dBm)	NF (dB)
0	40	1.7	21.4	13.5	1.2	21	14.6
5	35	1.7	21.3	13.1	1.2	21	13.4
10	30	1.7	21.3	12.5	1.1	20.5	13.1
20	25	1.55	20.9	11.8	1	16	12.2
33	20	1.38	17.5	11.2	0.8	11.1	11.9
60	15	1.3	12.2	10.8			
DOWN MIXER		f_{IN} = 5.8GHz, f_{OUT} = 800MHz					
R1 (Ω)	I_{Total} (mA)	Gain (dB)	OIP_3 (dBm)	NF (dB)			
0	40	2.2	16.3	14.3			
5	35	2	15.8	14.1			
10	30	1.8	14.5	13.7			
20	25	1.6	11.8	13			
33	20	1.1	8.9	12.2			

APPLICATIONS INFORMATION

Supply Voltage

High quality ceramic capacitors such as X5R or X7R should be used as bypass capacitors for V_{CC}. The capacitors should be located on the same side of the PCB as the LTC5562 and as close to pin 6 as possible. Wide, low inductance traces should be used. The ground connection to the bypass capacitor should connect to the top side ground and to the low inductance ground plane. If possible, multiple ground vias should be used.

Fast ramping of the supply voltage can cause a current glitch in the internal ESD protection circuits. Depending on the supply inductance, this could result in a supply voltage transient that exceeds the maximum rating. A supply voltage ramp time of greater than 1ms is recommended.

Spurious Output Levels

Mixer spurious output levels vs harmonics of the RF and LO are tabulated in Tables 8 and 9. The spur levels were measured on a standard evaluation board using the test circuit shown in Figures 1 and 2. The spur frequencies can be calculated using the following equation:

$$F_{SPUR} = |M \bullet f_{IN} \pm N \bullet f_{LO}|$$

Table 8. Downconversion Output Spur Levels (dBc), $F_{SPUR} = |M \bullet f_{IN} - N \bullet f_{LO}|$
(f_{IN} = 5.8GHz, P_{IN} = –12dBm, f_{LO} = 5.0GHz, P_{LO} = 0dBm, V_{CC} = 3.3V, f_{OUT} = 800MHz

		N					
		0	1	2	3	4	5
M	0	–	–41.6	–15.6	–59.4	–39.6	*
	1	53.6	0**	< –75	–38.5	< –75	–69.3
	2	–65.7	< –75	–73.9	< –75	< –75	< –75
	3	< –75	< –75	< –75	< –75	< –75	< –75
	4	*	< –75	< –75	< –75	< –75	< –75
	5	*	< –75	< –75	< –75	< –75	< –75

*Out of Range for Test Equipment
**Carrier Frequency

Table 9. Downconversion Output Spur Levels (dBc), $F_{SPUR} = |M \bullet f_{IN} + N \bullet f_{LO}|$
(f_{IN} = 5.8GHz, P_{IN} = –12dBm, f_{LO} = 5.0GHz, P_{LO} = 0dBm, V_{CC} = 3.3V, f_{OUT} = 800MHz

		N					
		0	1	2	3	4	5
M	0	–	–41.6	–15.7	–59.5	–39.6	*
	1	–53.7	–34.4**	–71.4	*	*	*
	2	–65.8	< –75	*	*	*	*
	3	< –75	*	*	*	*	*
	4	*	*	*	*	*	*
	5	*	*	*	*	*	*

*Out of Range for Test Equipment
**Image Frequency

TYPICAL APPLICATIONS

The following examples illustrate the wide ranging capabilities of the LTC5562, with performance in both up mixing and down mixing applications shown. These circuits were evaluated using the board layouts shown in Figures 3(a) and 3(b).

Upconverter with 2.45GHz Output

In this example, the LTC5562 was evaluated for an application with the input frequency at 140MHz, an RF output of 2.45GHz and low side LO injection. The schematic is shown in Figure 16 and the Gain, NF and OIP3 performance vs Input Frequency is shown in Figure 17. Also, for port matching data refer to Figures 5, 8 and 12.

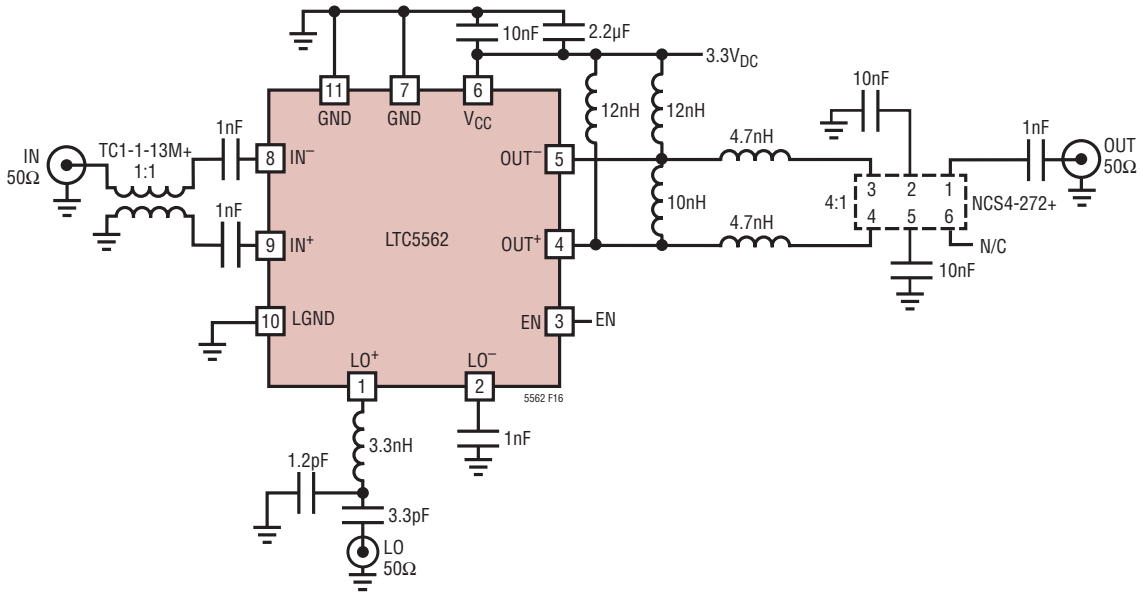


Figure 16. Upconverter Schematic with 2.45GHz Output

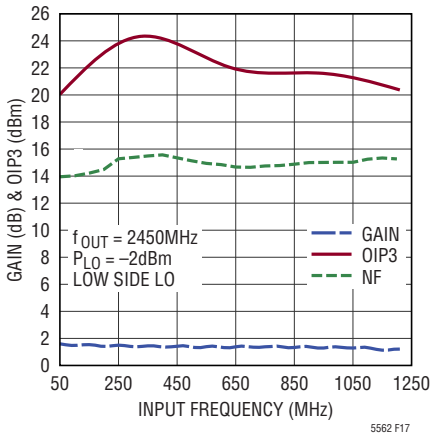


Figure 17. Gain, Noise Figure and OIP3 vs Input Frequency in the 2.45GHz Application

TYPICAL APPLICATIONS

LTC5562 Phase Detector

The output of the LTC5562 is DC-coupled and differential, therefore, it is suitable to be used as a phase detector with a positive or a negative response. The schematic is shown in Figure 18 and the phase detector gain and phase response with positive slope is shown in Figure 19 for a 200MHz input frequency. In this application, a 5V supply voltage is used to accommodate the voltage drop across the resistor network R1, R2 and R3 while providing the proper bias for the OUT pins. The EN pin is connected directly to V_{CC} to prevent exceeding the ABS MAX limit when powered down The IN and LO ports are matched between 20MHz to 600MHz, however, the LTC5562 can be used as a phase detector at higher frequencies with proper matching. The LTC5562 has a low 1/f corner and a low thermal noise floor. Refer to the Electrical Characteristics table for typical noise floor specifications.

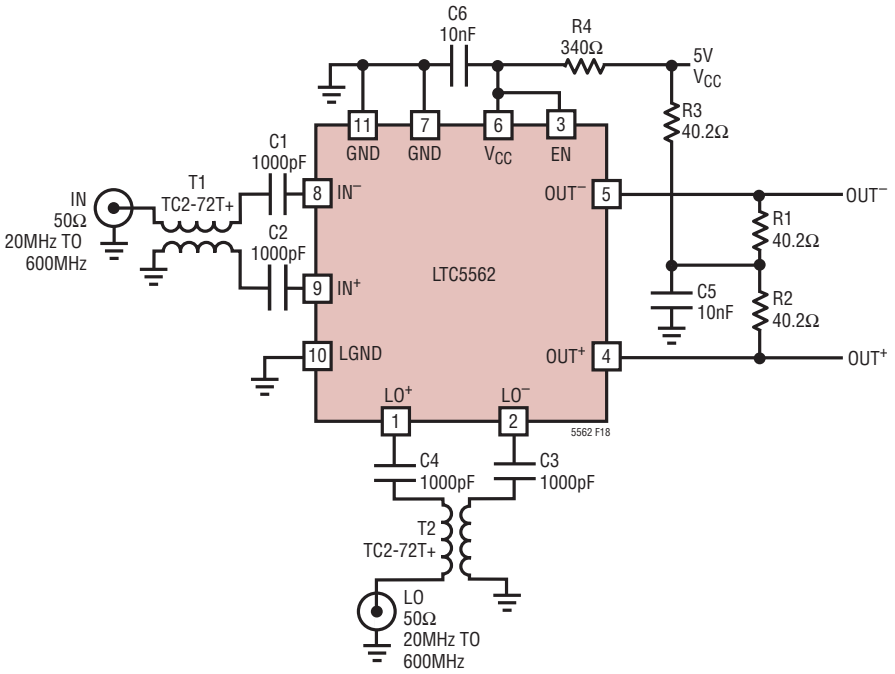


Figure 18. Phase Detector Test Schematic

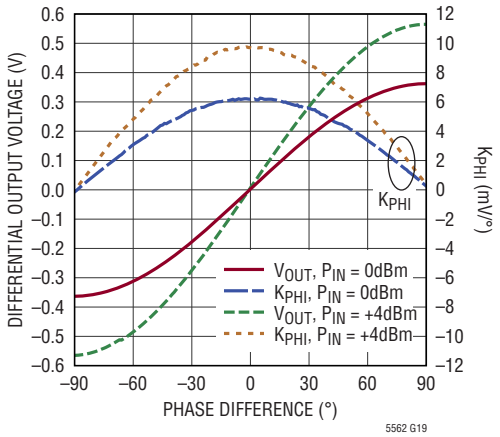


Figure 19. Phase Detector DC Output and Gain vs Phase
$f_{IN} = f_{LO} = 200MHz$, $P_{LO} = 0dBm$

TYPICAL APPLICATIONS

LTC5562 Low Power Broadband Downconverter with Single-Ended Input

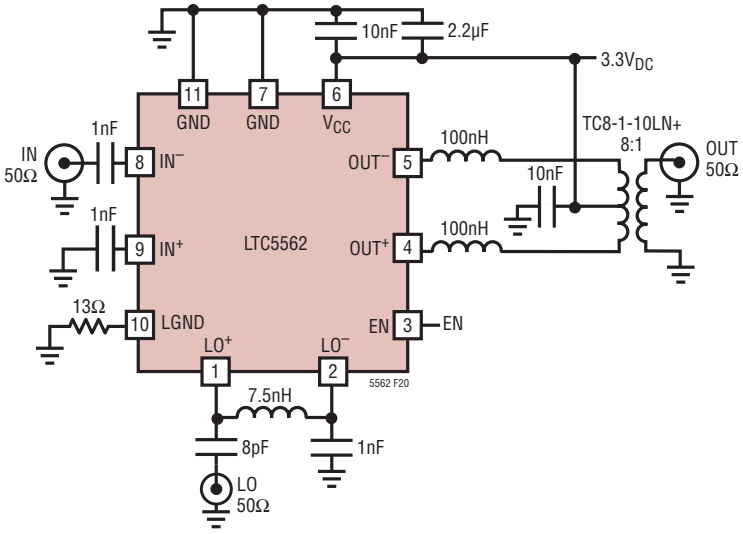


Figure 20. Low Power, Single-Ended Input, Downconverting Mixer

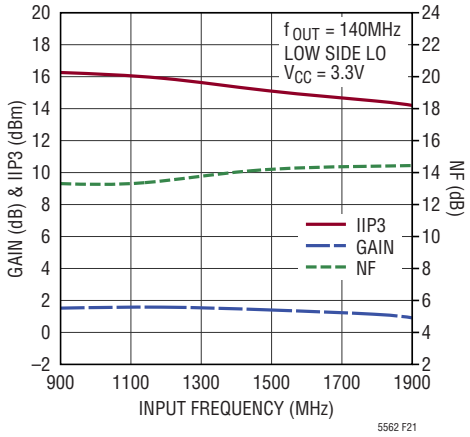


Figure 21. Conversion Gain, IIP3 and NF vs Input Frequency R1 = 13Ω, I_{TOTAL} = 28.5mA, P_{LO} = –2dBm

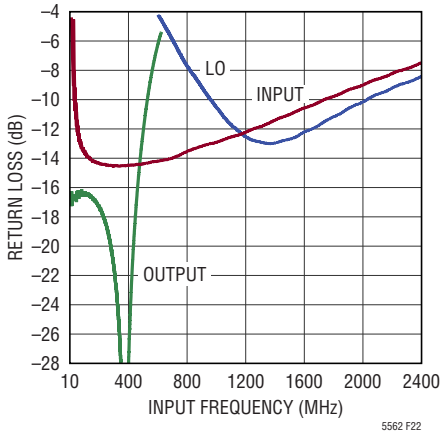


Figure 22. Return Loss vs Frequency R1 = 13Ω, I_{TOTAL} = 28.5mA

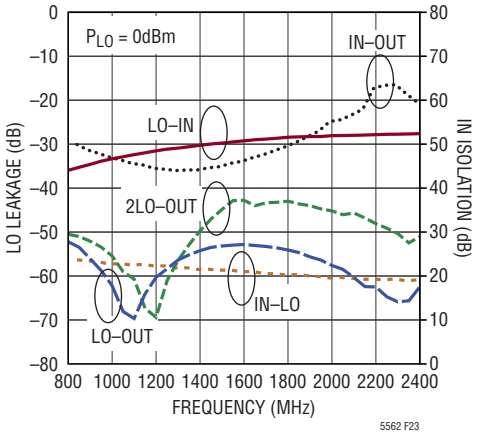
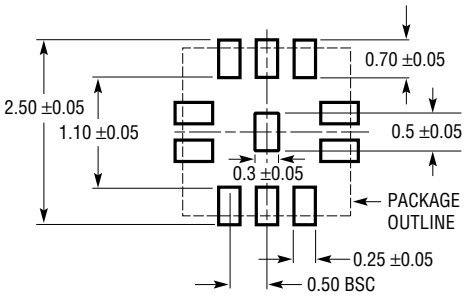


Figure 23. IN Isolation and LO Leakage vs Frequency

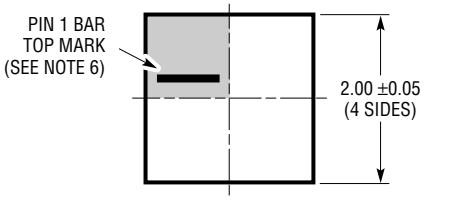
PACKAGE DESCRIPTION

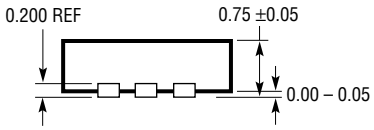
Please refer to http://www.linear.com/product/LTC5562#packaging for the most recent package drawings.

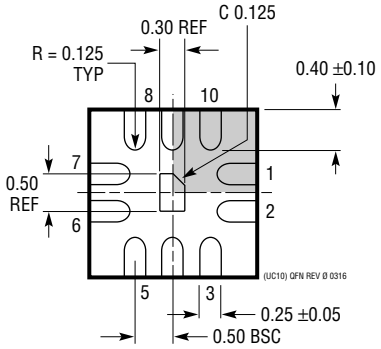
UC10 Package
10-Lead Plastic QFN (2mm × 2mm), Flip Chip
(Reference LTC DWG # 05-08-1534 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS







BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING NOT TO SCALE
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. EXPOSED PAD SHALL BE SOLDER PLATED
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE