42V, 2A/3A Peak Synchronous Step-Down Regulator with 2.5µA Quiescent Current

FEATURES

- **Silent Switcher® 2 Architecture**
  - **Ultralow EMI Emissions on Any PCB**
  - **Eliminates PCB Layout Sensitivity**
  - **Internal Bypass Capacitors Reduce Radiated EMI**
  - **Optional Spread Spectrum Modulation**
- **Wide Input Voltage Range: 3.0V to 42V**
- **Ultralow Quiescent Current Burst Mode® Operation:**
  - **<2.5µA I_Q Regulating $12V_{IN}$ to $3.3V_{OUT}$**
  - **Output Ripple <10mV_{P-P}**
- **High Efficiency 2MHz Synchronous Operation:**
  - **>93% Efficiency at 1A, $12V_{IN}$ to $5V_{OUT}$**
- **2A Maximum Continuous Output, 3A Peak Transient Output**
- **Fast Minimum Switch-On Time: 45ns**
- **Adjustable and Synchronizable: 200kHz to 2.2MHz**
- Allows Use of Small Inductors
- Low Dropout
- Peak Current Mode Operation
- Internal Compensation
- Output Soft-Start and Tracking
- Small 16-Lead 3mm × 3mm LQFN Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

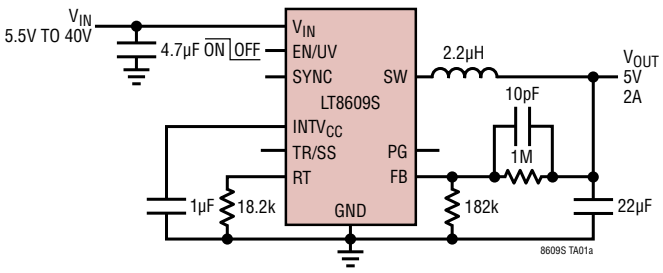
- General Purpose Step Down
- Low EMI Step Down

DESCRIPTION

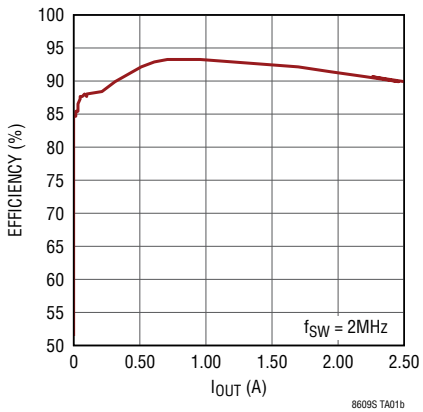
The LT®8609S is a compact, high efficiency, high speed synchronous monolithic step-down switching regulator that consumes only 1.7µA of non-switching quiescent current. The LT8609S can deliver 2A of continuous current with peak loads of 3A (<1sec) to support applications such as GSM transceivers which require high transient loads. Top and bottom power switches are included with all necessary circuitry to minimize the need for external components. Low ripple Burst Mode operation enables high efficiency down to very low output currents while keeping the output ripple below 10mV_{P-P}. A SYNC pin allows synchronization to an external clock, or spread spectrum modulation of switching frequencies for low EMI operation. Internal compensation with peak current mode topology allows the use of small inductors and results in fast transient response and good loop stability. The EN/UV pin has an accurate 1V threshold and can be used to program V_{IN} undervoltage lockout or to shut down the LT8609S reducing the input supply current to 1µA. A capacitor on the TR/SS pin programs the output voltage ramp rate during start-up while the PG flag signals when V_{OUT} is within ±8.5% of the programmed output voltage as well as fault conditions. The LT8609S is available in a small 16-lead 3mm × 3mm LQFN package.

TYPICAL APPLICATION

5V, 2MHz Step Down



$12V_{IN}$ to $5V_{OUT}$ Efficiency



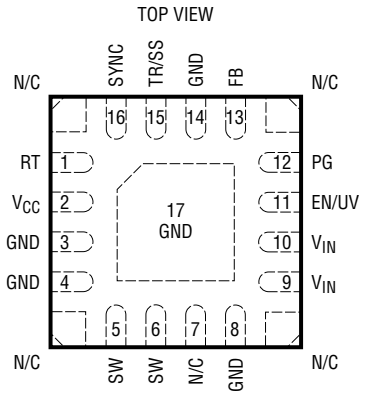
Rev. D

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, EN/UV, PG.....42V
FB, TR/SS 4V
SYNC Voltage 6V
Operating Junction Temperature Range (Note 2)
LT8609SE.....–40 to 125°C
LT8609SI.....–40 to 125°C
Storage Temperature Range .....–65 to 150°C
Maximum Reflow (Package Body)
Temperature.....260°C

PIN CONFIGURATION



LQFN PACKAGE
16-LEAD (3mm × 3mm) LQFN
JEDEC BOARD: θ_{JA} = 50°C/W, $\theta_{JC(PAD)}$ = 14°C/W (NOTE 4)
DEMOBOARD: θ_{JA} = 31°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

PART NUMBER	TAPE AND REEL	PART MARKING*	FINISH CODE	PAD FINISH	PACKAGE TYPE**	MSL RATING	TEMPERATURE RANGE
LT8609SEV#PBF	LT8609SEV#TRPBF	LGYN	e4	Au (RoHS)	LQFN (Laminate Package with QFN Footprint	3	–40°C to 125°C
LT8609SIV#PBF	LT8609SIV#TRPBF	LGYN					–40°C to 125°C
AUTOMOTIVE PRODUCTS**							
LT8609SEV#WPBF	LT8609SEV#WTRPBF	LGYN	e4	Au (RoHS)	LQFN (Laminate Package with QFN Footprint	3	–40°C to 125°C
LT8609SIV#WPBF	LT8609SIV#WTRPBF	LGYN					–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended PCB Assembly and Manufacturing Procedures.
- Package and Tray Drawings
- Parts ending with PBF are RoHS and WEEE compliant.

** The LT8609S package has the same footprint as a standard 3mm × 3mm QFN Package.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		 ●		 2.7	3.0 3.2	V
V_{IN} Quiescent Current	$V_{EN/UV}$ = 0V, V_{SYNC} = 0V $V_{EN/UV}$ = 2V, Not Switching, V_{SYNC} = 0V, $V_{IN} \leq$ 36V	 ●		1 1.7	5 12	µA µA
V_{IN} Current in Regulation	V_{IN} = 6V, V_{OUT} = 2.7V, Output Load = 100µA V_{IN} = 6V, V_{OUT} = 2.7V, Output Load = 1mA	● ●		46 480	90 700	µA µA
Feedback Reference Voltage	V_{IN} = 6V, I_{LOAD} = 100mA V_{IN} = 6V, I_{LOAD} = 100mA	 ●	0.770 0.758	0.774 0.774	0.778 0.794	V V
Feedback Voltage Line Regulation	V_{IN} = 4.0V to 40V	●		0.02	0.06	%/V
Feedback Pin Input Current	V_{FB} = 1V	●			±20	nA
Minimum On-Time	I_{LOAD} = 1.75A, SYNC = 0V I_{LOAD} = 1.75A, SYNC = 1.9V	● ●		45 45	75 60	ns ns
Minimum Off Time				90	130	ns
Oscillator Frequency	R_T = 221k, I_{LOAD} = 0.5A R_T = 60.4k, I_{LOAD} = 0.5A R_T = 18.2k, I_{LOAD} = 0.5A	● ● ●	155 640 1.925	200 700 2.00	245 760 2.075	kHz kHz MHz
Top Power NMOS On-Resistance	I_{LOAD} = 1A			185		mΩ
Top Power NMOS Current Limit		●	3.4	4.75	5.7	A
Bottom Power NMOS On-Resistance				115		mΩ
SW Leakage Current	V_{IN} = 42V, V_{SW} = 40V				5	µA
EN/UV Pin Threshold	EN/UV Rising	●	0.99	1.05	1.11	V
EN/UV Pin Hysteresis				50		mV
EN/UV Pin Current	$V_{EN/UV}$ = 2V	●			±20	nA
PG Upper Threshold Offset from V_{FB}	V_{FB} Rising	●	5.0	8.5	13.0	%
PG Lower Threshold Offset from V_{FB}	V_{FB} Falling	●	5.0	8.5	13.0	%
PG Hysteresis				0.5		%
PG Leakage	V_{PG} = 42V	●			±200	nA
PG Pull-Down Resistance	V_{PG} = 0.1V			550	1200	Ω
Sync Low Input Voltage		●	0.4	0.9		V
Sync High Input Voltage	$INTV_{CC}$ = 3.5V	●		2.7	3.2	V
TR/SS Source Current		●	1	2	3	µA
TR/SS Pull-Down Resistance	Fault Condition, TR/SS = 0.1V			300	900	Ω
Spread Spectrum Modulation Frequency	V_{SYNC} = 3.3V		0.5	3	6	kHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

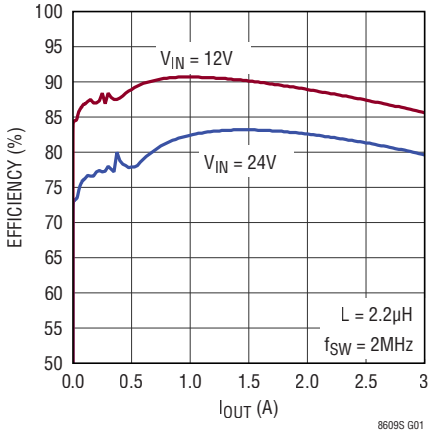
Note 2: The LT8609SE is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LT8609SI is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 3: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

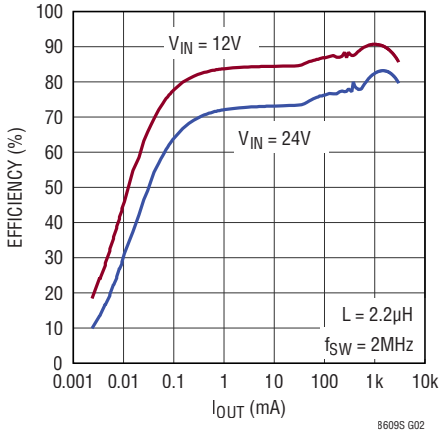
Note 4: θ values determined per JEDEC 51-7, 51-12. See the Applications Information Section for information on improving the thermal resistance and for actual temperature measurements of a demo board in typical operating conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

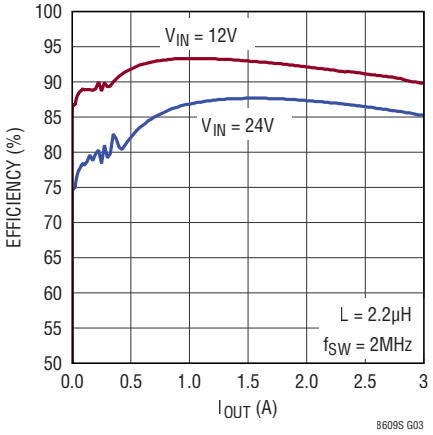
Efficiency (3.3V Output, 2MHz, Burst Mode Operation)



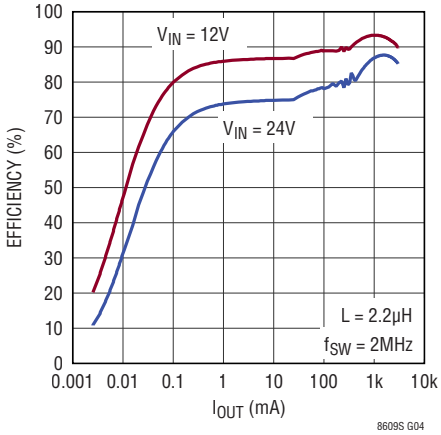
Efficiency (3.3V Output, 2MHz, Burst Mode Operation)



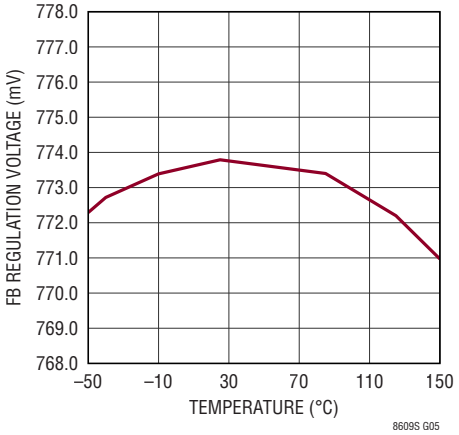
Efficiency (5V Output, 2MHz, Burst Mode Operation)



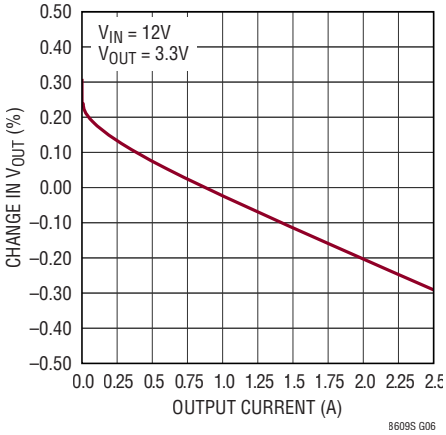
Efficiency (5V Output, 2MHz, Burst Mode Operation)



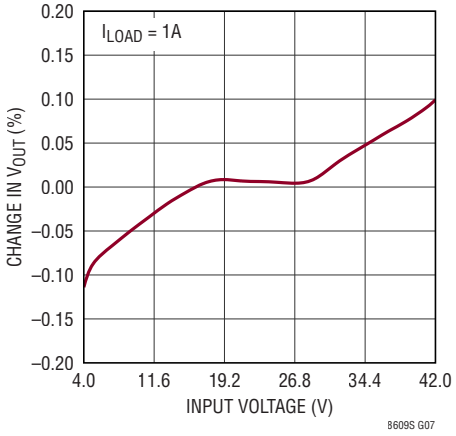
FB Voltage



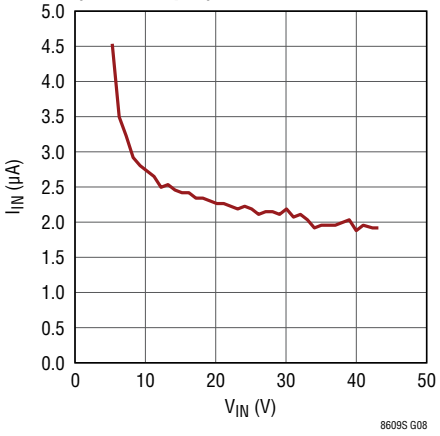
Load Regulation



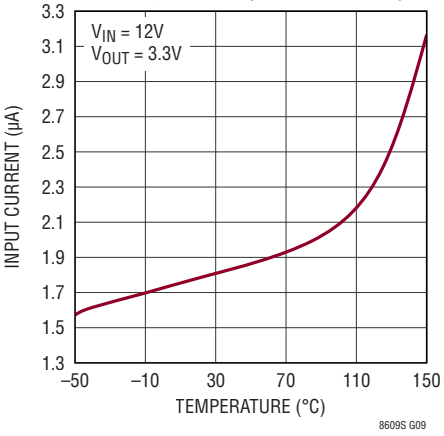
Line Regulation



No-Load Supply Current (3.3V Output)

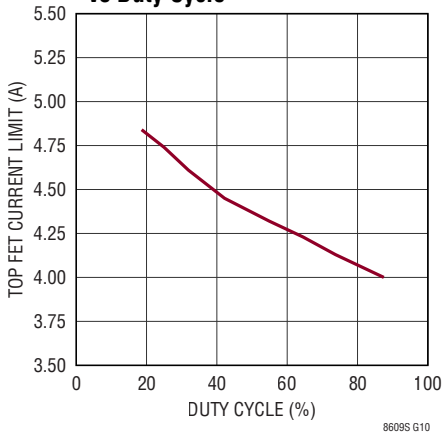


No-Load Supply Current vs Temperature (Not Switching)

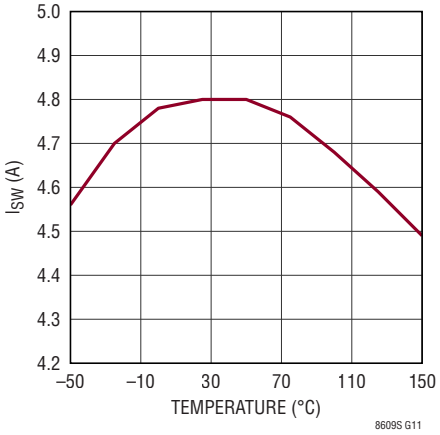


TYPICAL PERFORMANCE CHARACTERISTICS

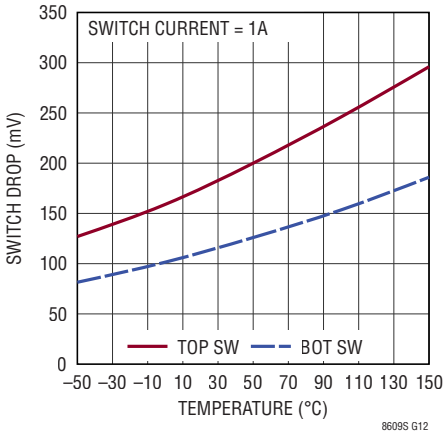
Top FET Current Limit vs Duty Cycle



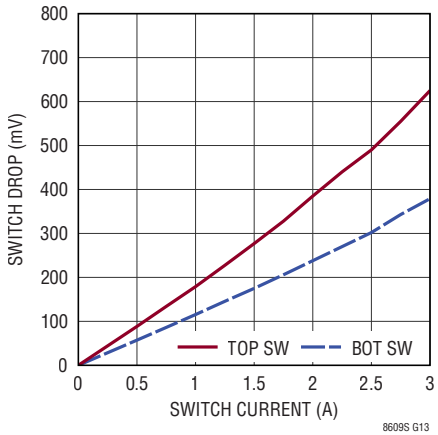
Top FET Current Limit vs Temperature



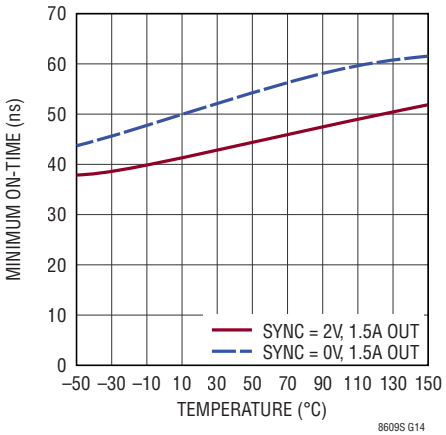
Switch Drop vs Temperature



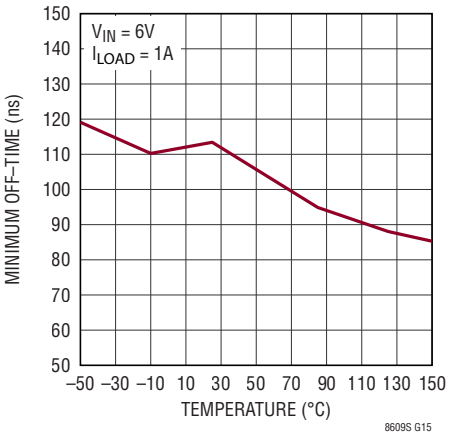
Switch Drop vs Switch Current



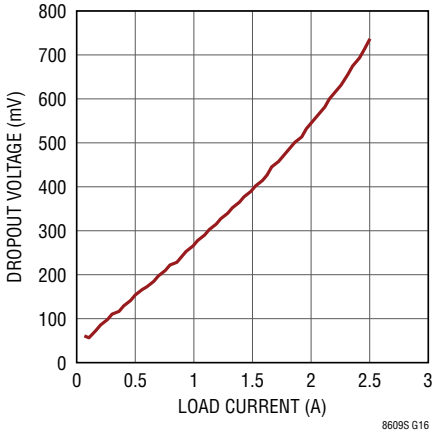
Minimum On-Time vs Temperature



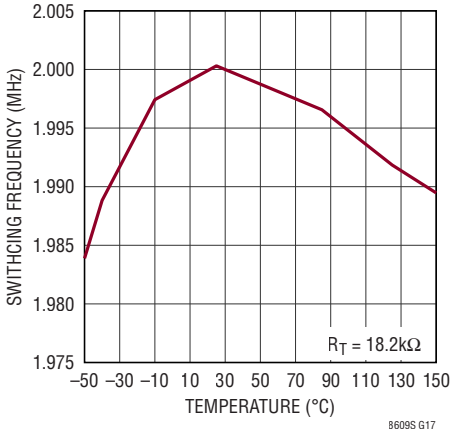
Minimum Off-Time vs Temperature



Dropout Voltage vs Load Current

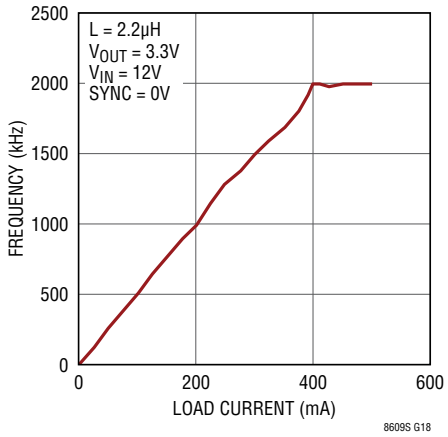


Switching Frequency vs Temperature

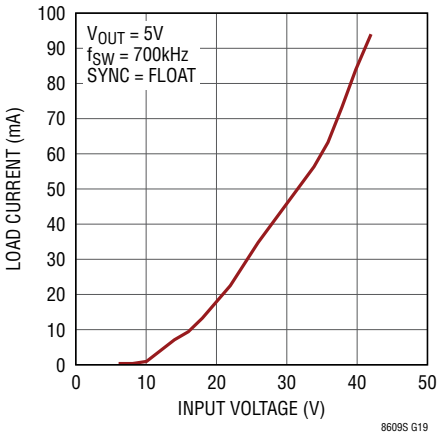


TYPICAL PERFORMANCE CHARACTERISTICS

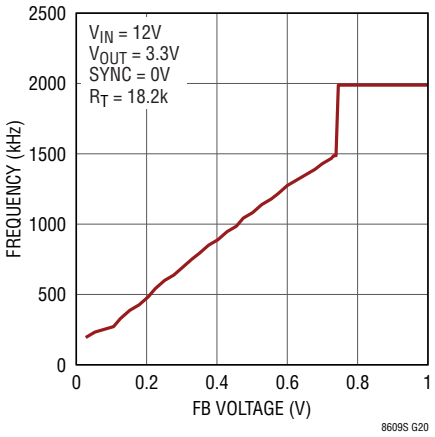
Burst Frequency vs Load Current



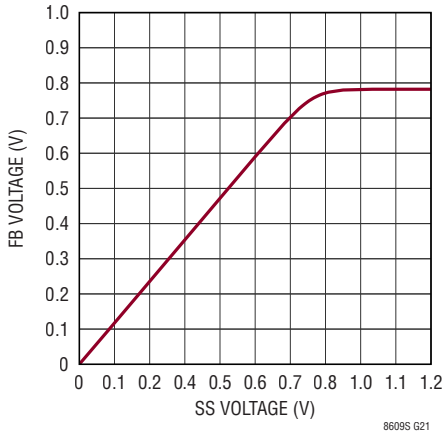
Minimum Load to Full Frequency (SYNC Float to 1.9V)



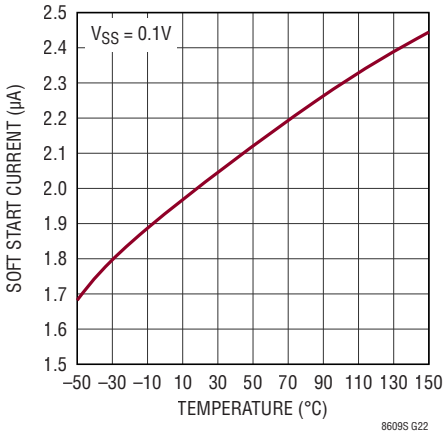
Frequency Foldback



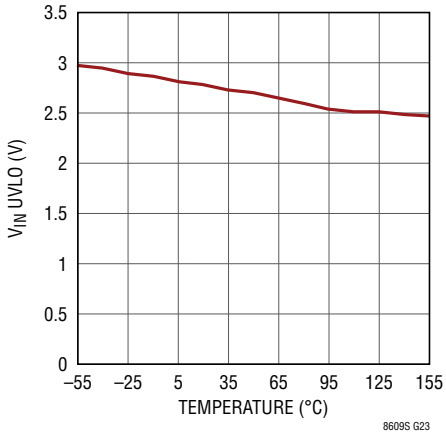
Soft-Start Tracking



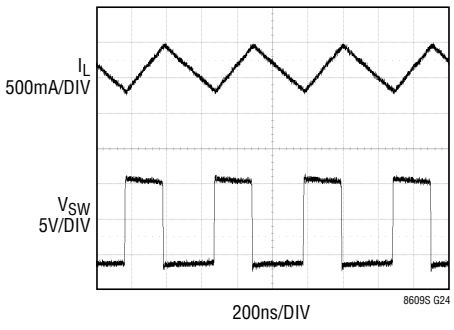
Soft-Start Current vs Temperature



V_{IN} UVLO

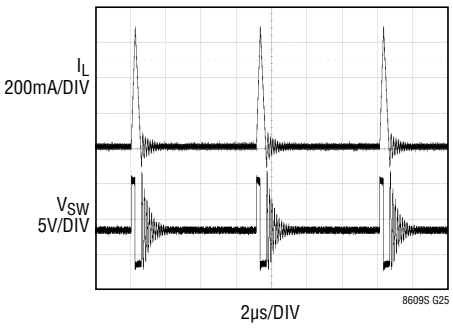


Switching Waveforms



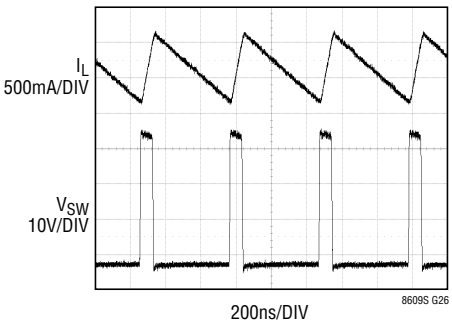
12V_{IN} TO 5V_{OUT} AT 1A

Switching Waveforms



12V_{IN} TO 5V_{OUT} AT 25mA
SYNC = 0 (Burst Mode OPERATION)

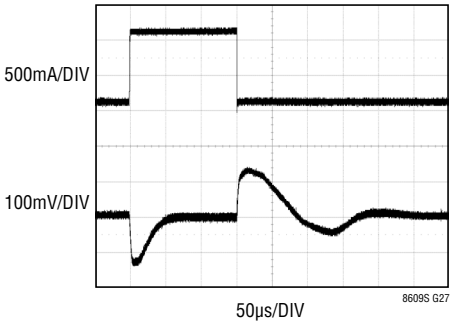
Switching Waveforms



36V_{IN} TO 5V_{OUT} AT 1A

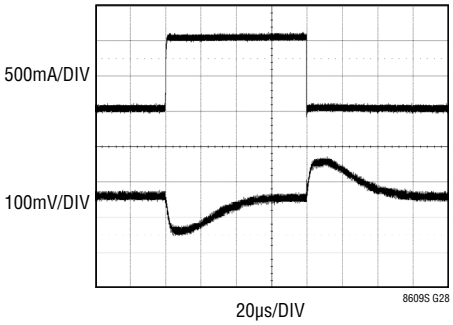
TYPICAL PERFORMANCE CHARACTERISTICS

Transient Response



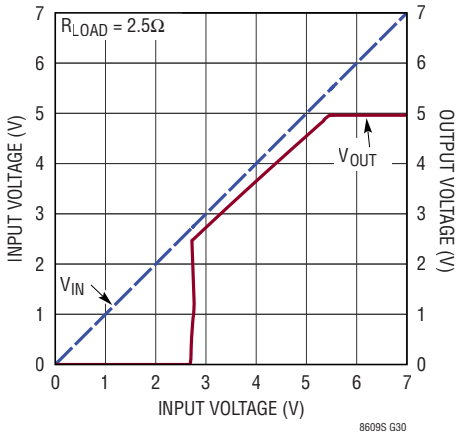
50mA TO 1A TRANSIENT
$12V_{IN}$ TO $5V_{OUT}$
C_{OUT} = 47µF

Transient Response

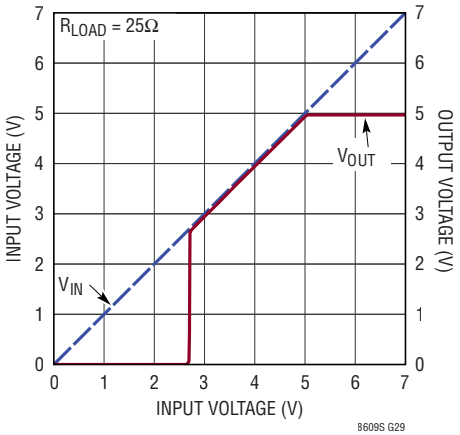


0.5A TO 1.5A TRANSIENT
$12V_{IN}$ TO $5V_{OUT}$
C_{OUT} = 47µF

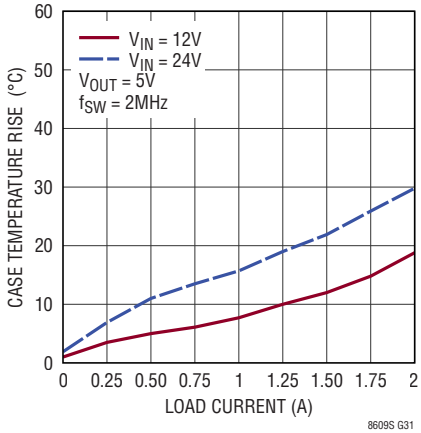
Start-Up Dropout



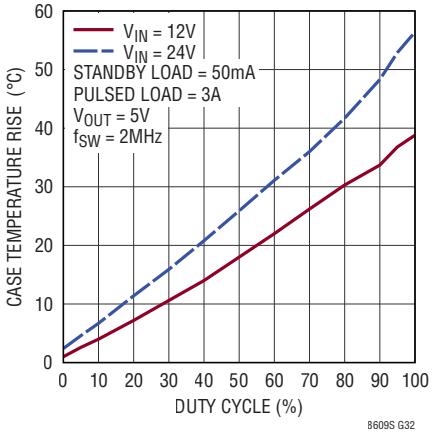
Start-Up Dropout



Case Temperature vs Load Current

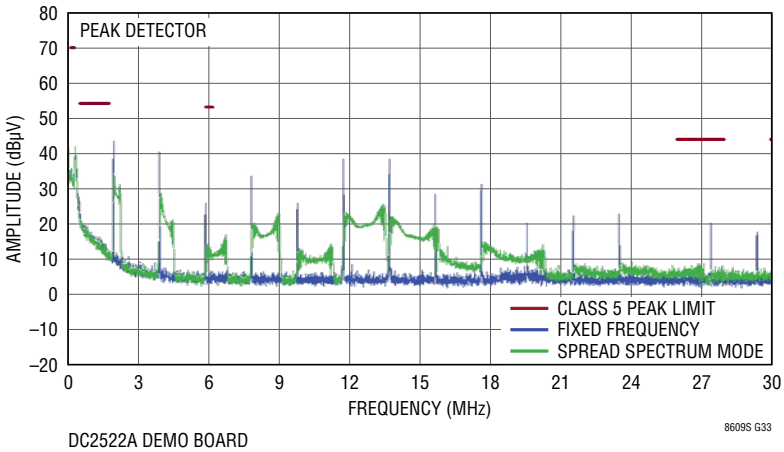


Case Temperature vs 3A Pulsed Load



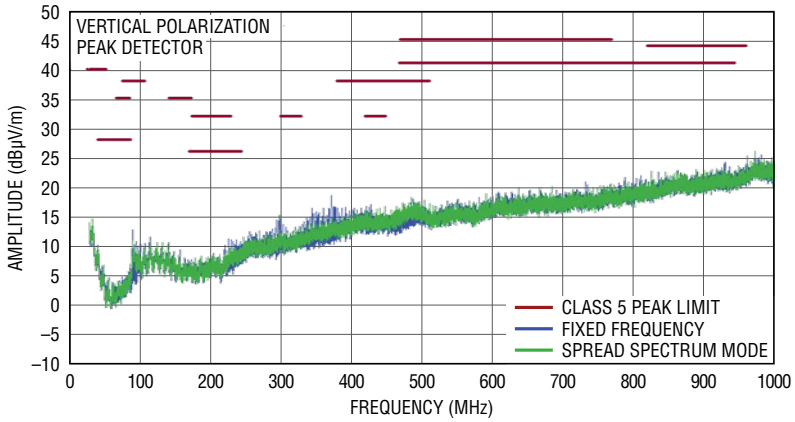
TYPICAL PERFORMANCE CHARACTERISTICS

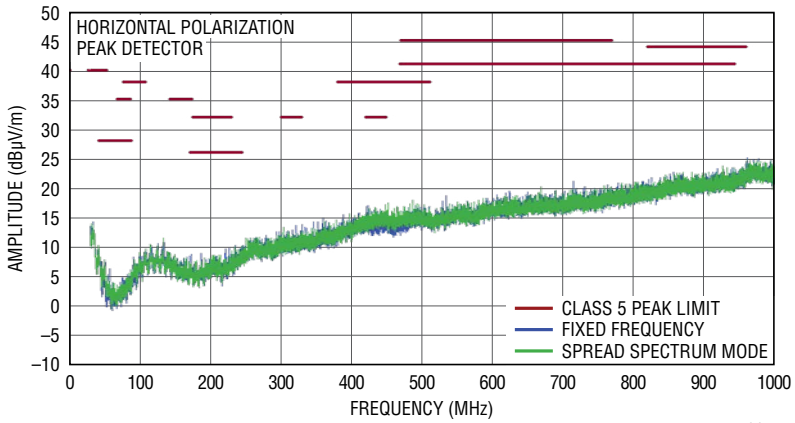
Conducted EMI Performance



DC2522A DEMO BOARD
WITH EMI FILTER INSTALLED
14V INPUT TO 5V OUTPUT AT 2A, f_{SW} = 2MHz

Radiated EMI Performance
(CISPR25 Radiated Emission Test with Class 5 Peak Limits)





DC2522A DEMO BOARD
WITH EMI FILTER INSTALLED
14V INPUT TO 5V OUTPUT AT 2A, f_{SW} = 2MHz

PIN FUNCTIONS

RT (Pin 1): A resistor is tied between RT and ground to set the switching frequency.

$INTV_{CC}$ (Pin 2): Internal 3.5V Regulator Bypass Pin. The internal power drivers and control circuits are powered from this voltage. $INTV_{CC}$ max output current is 20mA. Voltage on $INTV_{CC}$ will vary between 2.8V and 3.5V. Decouple this pin to power ground with at least a 1µF low ESR ceramic capacitor. Do not load the $INTV_{CC}$ pin with external circuitry.

GND (Pins 3, 4, 8, 14, 17): Exposed Pad Pin. These pads must be connected to the negative terminal of the input capacitor and soldered to the PCB in order to lower the thermal resistance.

SW (Pins 5, 6): The SW pin is the output of the internal power switches. Connect this pin to the inductor and boost capacitor. This node should be kept small on the PCB for good performance.

N/C (Corner Pins, Pin 7): Connect these pins to the ground plane for improved mechanical performance while temperature cycling.

V_{IN} (Pins 9, 10): The V_{IN} pin supplies current to the LT8609S internal circuitry and to the internal topside power switch. This pin must be locally bypassed. Be sure to place the positive terminal of the input capacitor as close as possible to the V_{IN} pins, and the negative capacitor terminal as close as possible to the GND pins.

EN/UV (Pin 11): The LT8609S is shut down when this pin is low and active when this pin is high. The hysteretic threshold voltage is 1.05V going up and 1.00V going down. Tie to V_{IN} if the shutdown feature is not used. An external resistor divider from V_{IN} can be used to program a V_{IN} threshold below which the LT8609S will shut down.

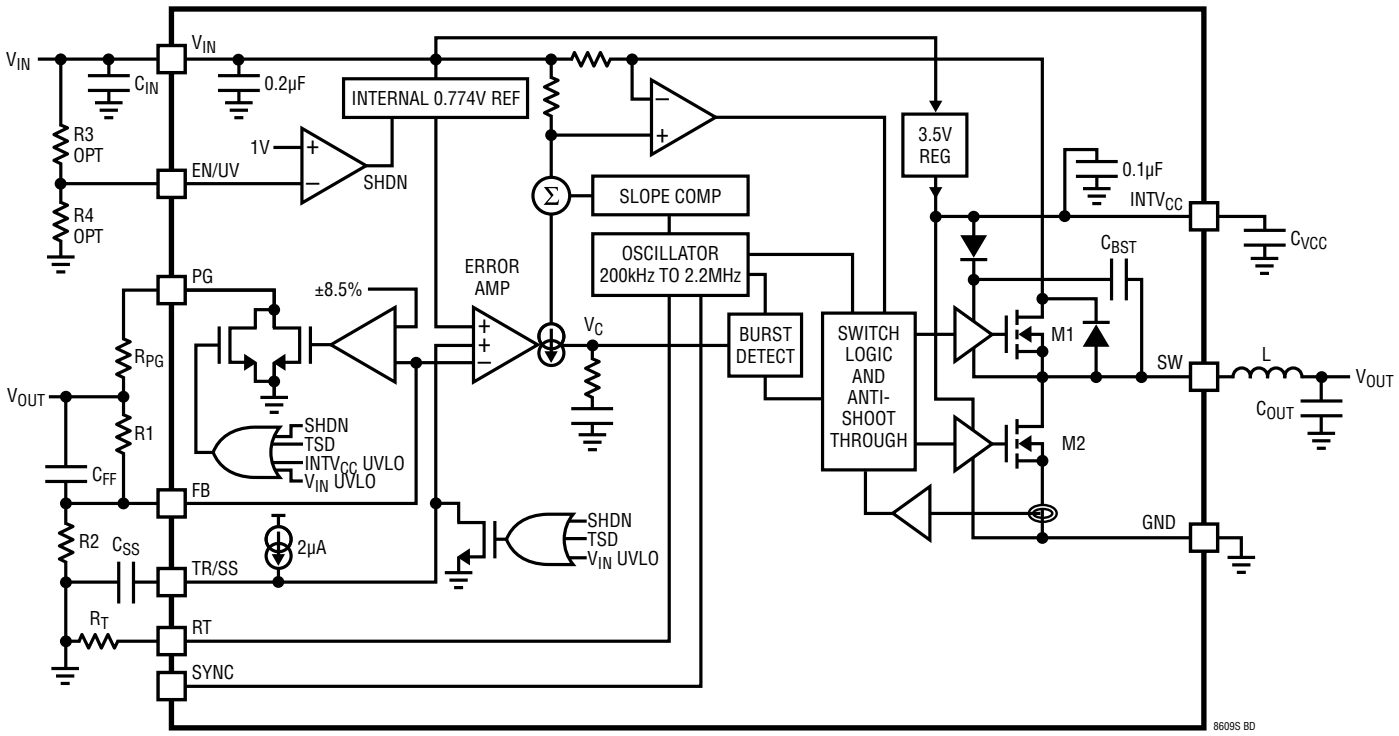
PG (Pin 12): The PG pin is the open-drain output of an internal comparator. PG remains low until the FB pin is within ±8.5% of the final regulation voltage, and there are no fault conditions. PG is valid when V_{IN} is above 3.2V and EN/UV is high. PG will pull low when V_{IN} is above 3.2V and EN/UV is low. PG will be high impedance when V_{IN} is low.

FB (Pin 13): The LT8609S regulates the FB pin to 0.774V. Connect the feedback resistor divider tap to this pin.

TR/SS (Pin 15): Output Tracking and Soft-Start Pin. This pin allows user control of output voltage ramp rate during start-up. A TR/SS voltage below 0.774V forces the LT8609S to regulate the FB pin to equal the TR/SS pin voltage. When TR/SS is above 0.774V, the tracking function is disabled and the internal reference resumes control of the error amplifier. An internal 2µA pull-up current from $INTV_{CC}$ on this pin allows a capacitor to program output voltage slew rate. This pin is pulled to ground with a 300Ω MOSFET during shutdown and fault conditions; use a series resistor if driving from a low impedance output.

SYNC (Pin 16): External Clock Synchronization Input. Ground this pin for low ripple Burst Mode operation at low output loads. Tie to a clock source for synchronization to an external frequency. Leave floating for pulse-skipping mode with no spread spectrum modulation. Tie to $INTV_{CC}$ or tie to a voltage between 3.2V and 5.0V for pulse-skipping mode with spread spectrum modulation. When in pulse-skipping mode, the I_Q will increase to several mA.

BLOCK DIAGRAM



OPERATION

The LT8609S is a monolithic constant frequency current mode step-down DC/DC converter. An oscillator with frequency set using a resistor on the RT pin turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by the voltage on the internal VC node. The error amplifier servos the VC node by comparing the voltage on the V_{FB} pin with an internal 0.774V reference. When the load current increases it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the VC voltage until the average inductor current matches the new load current. When the top power switch turns off the synchronous power switch turns on until the next clock cycle begins or inductor current falls to zero. If overload conditions result in excess current flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

If the EN/UV pin is low, the LT8609S is shut down and draws 1µA from the input. When the EN/UV pin is above 1V, the switching regulator becomes active.

To optimize efficiency at light loads, the LT8609S enters Burst Mode operation during light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 1.7µA. In a typical application, 2.5µA will be consumed from the input supply when regulating with no load. The SYNC pin is tied low to use Burst Mode operation and can be floated to use pulse-skipping mode. If a clock is applied to the SYNC pin the part will synchronize to an external clock frequency and operate in pulse-skipping mode. While in pulse-skipping mode the oscillator operates continuously and positive SW transitions are aligned to the clock. During light loads, switch pulses are skipped to regulate the output and the quiescent current will be several mA. The SYNC pin may be tied high for spread spectrum modulation mode, and the LT8609S will operate similar to pulse-skipping mode but vary the clock frequency to reduce EMI.

Comparators monitoring the FB pin voltage will pull the PG pin low if the output voltage varies more than ±8.5% (typical) from the set point, or if a fault condition is present.

The oscillator reduces the LT8609S's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the inductor current when the output voltage is lower than the programmed value which occurs during start-up. When a clock is applied to the SYNC pin the frequency foldback is disabled. Frequency foldback is only enabled when the SYNC pin is tied to ground.

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Achieving Ultralow Quiescent Current

To enhance efficiency at light loads, the LT8609S enters into low ripple Burst Mode operation, which keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and minimizing output voltage ripple. In Burst Mode operation the LT8609S delivers single small pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode the LT8609S consumes 1.7µA.

As the output load decreases, the frequency of single current pulses decreases (see Figure 1) and the percentage of time the LT8609S is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. By maximizing the time between pulses, the converter quiescent current approaches 2.5µA for a typical application when there is no output load. Therefore, to optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current.

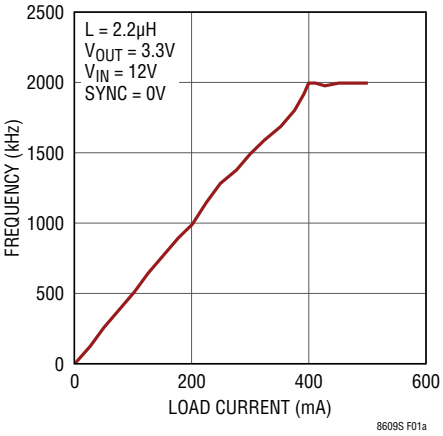

Figure 1a. SW Burst Mode Frequency vs Load

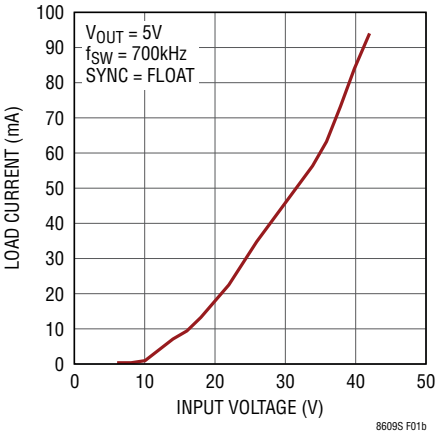

Figure 1b. Full Switching Frequency Minimum Load vs V_{IN} in Pulse Skipping Mode

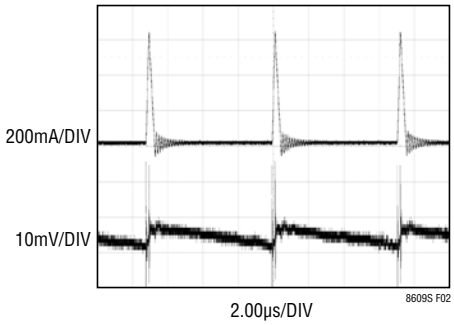

Figure 2. Burst Mode Operation

While in Burst Mode operation the current limit of the top switch is approximately 600mA resulting in output voltage ripple shown in Figure 2. Increasing the output capacitance will decrease the output ripple proportionally. As load ramps upward from zero the switching frequency will increase but only up to the switching frequency programmed by the resistor at the RT pin as shown in Table 1. The output load at which the LT8609S reaches the programmed frequency varies based on input voltage, output voltage, and inductor choice.

For some applications it is desirable for the LT8609S to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. First is the clock stays awake at all times and all switching cycles are aligned to the clock. In this mode much of the internal circuitry is awake at all times, increasing quiescent current to several hundred µA. Second is that full switching frequency is reached at lower output load than in Burst Mode operation as shown in Figure 1b. To enable pulse-skipping mode the SYNC pin is floated. To achieve spread spectrum modulation with pulse-skipping mode, the SYNC pin is tied high. While a clock is applied to the SYNC pin the LT8609S will also operate in pulse-skipping mode.

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FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to:

$$R1 = R2\left(\frac{V_{OUT}}{0.774V} - 1\right)$$

1% resistors are recommended to maintain output voltage accuracy.

The total resistance of the FB resistor divider should be selected to be as large as possible when good low load efficiency is desired: The resistor divider generates a small load on the output, which should be minimized to optimize the quiescent current at low loads.

When using large FB resistors, a 10pF phase lead capacitor should be connected from V_{OUT} to FB.

Setting the Switching Frequency

The LT8609S uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 2.2MHz by using a resistor tied from the RT pin to ground. A table showing the necessary R_T value for a desired switching frequency is in Table 1. When in spread spectrum modulation mode, the frequency is modulated upwards of the frequency set by R_T.

Table 1. SW Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.2	221
0.300	143
0.400	110
0.500	86.6
0.600	71.5
0.700	60.4
0.800	52.3
0.900	46.4
1.000	40.2
1.200	33.2
1.400	27.4
1.600	23.7
1.800	20.5
2.000	18.2
2.200	16.2

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency and a smaller input voltage range.

The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)}\left(V_{IN} - V_{SW(TOP)} + V_{SW(BOT)}\right)}$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.4V, ~0.25V, respectively at max load) and $t_{ON(MIN)}$ is the minimum top switch on-time (see Electrical Characteristics). This equation shows that slower switching frequency is necessary to accommodate a high V_{IN}/V_{OUT} ratio.

For transient operation V_{IN} may go as high as the Abs Max rating regardless of the R_T value, however the LT8609S will reduce switching frequency as necessary to maintain control of inductor current to assure safe operation.

The LT8609S is capable of maximum duty cycle approaching 100%, and the V_{IN} to V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch. In this mode the LT8609S skips switch cycles, resulting in a lower switching frequency than programmed by R_T.

For applications that cannot allow deviation from the programmed switching frequency at low VIN/VOUT ratios use the following formula to set switching frequency:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{SW(BOT)}}{1 - f_{SW} \bullet t_{OFF(MIN)}} - V_{SW(BOT)} + V_{SW(TOP)}$$

where $V_{IN(MIN)}$ is the minimum input voltage without skipped cycles, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.4V, ~0.25V, respectively at max load), f_{SW} is the switching frequency (set by R_T), and $t_{OFF(MIN)}$ is the minimum switch off-time. Note that higher switching frequency will increase the minimum input voltage below which cycles will be dropped to achieve higher duty cycle.

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Inductor Selection and Maximum Output Current

The LT8609S is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. During overload or short circuit conditions the LT8609S safely tolerates operation with a saturated inductor through the use of a high speed peak-current mode architecture.

A good first choice for the inductor value is:

$$L = \frac{V_{OUT} + V_{SW(BOT)}}{f_{SW}}$$

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, $V_{SW(BOT)}$ is the bottom switch drop (~0.25V) and L is the inductor value in µH.

To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus 1/2 of in inductor ripple current:

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{1}{2}\Delta_L$$

where ΔI_L is the inductor ripple current as calculated several paragraphs below and $I_{LOAD(MAX)}$ is the maximum output load for a given application.

As a quick example, an application requiring 1A output should use an inductor with an RMS rating of greater than 1A and an I_{SAT} of greater than 1.3A. To keep the efficiency high, the series resistance (DCR) should be less than 0.04Ω, and the core material should be intended for high frequency applications.

The LT8609S limits the peak switch current in order to protect the switches and the system from overload faults. The top switch current limit (I_{LIM}) is typically 4.75A at low duty cycles and decreases linearly to 4.0A at D = 0.8. The inductor value must then be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the switch current limit (I_{LIM}) and the ripple current:

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2}$$

The peak-to-peak ripple current in the inductor can be calculated as follows:

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

where f_{SW} is the switching frequency of the LT8609S, and L is the value of the inductor. Therefore, the maximum output current that the LT8609S will deliver depends on the minimum switch current limit, the inductor value, and the input and output voltages. The inductor value may have to be increased if the inductor ripple current does not allow sufficient maximum output current ($I_{OUT(MAX)}$) given the switching frequency, and maximum input voltage used in the desired application.

The optimum inductor for a given application may differ from the one indicated by this design guide. A larger value inductor provides a higher maximum load current and reduces the output voltage ripple. For applications requiring smaller load currents, the value of the inductor may be lower and the LT8609S may operate with higher ripple current. This allows use of a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. Be aware that low inductance may result in discontinuous mode operation, which further reduces maximum load current.

The internal circuitry of the LT8609S is capable of supplying $I_{OUT(MAX)}$ up to 3A. Thermal limitations of the LT8609S prevent continuous output of 3A loads due to unsafe operating temperatures. In order to ensure safe operating temperature, the average LT8609S current must be kept below 2A, but will allow transient peaks up to 3A or $I_{OUT(MAX)}$. If high average currents cause unsafe heating of the part, the LT8609S will stop switching and indicate a fault condition to protect the internal circuitry.

For more information about maximum output current and discontinuous operation, see Analog Devices Application Note 44.

Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid sub-harmonic oscillation. See Analog Devices Application Note 19.

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Input Capacitor

Bypass the input of the LT8609S circuit with a ceramic capacitor of X7R or X5R type. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 4.7µF to 10µF ceramic capacitor is adequate to bypass the LT8609S and will easily handle the ripple current. Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT8609S and to force this very high frequency switching current into a tight local loop, minimizing EMI. A 4.7µF capacitor is capable of this task, but only if it is placed close to the LT8609S (see the PCB Layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT8609S. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT8609S circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8609S's voltage rating. This situation is easily avoided (see Analog Devices Application Note 88).

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT8609S to produce the DC output. In this role it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT8609S's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. A good starting value is:

$$C_{OUT} = \frac{100}{V_{OUT} \bullet f_{SW}}$$

where f_{SW} is in MHz, and C_{OUT} is the recommended output capacitance in µF. Use X5R or X7R types. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value output capacitor and the addition of a feedforward capacitor placed between V_{OUT} and FB. Increasing the output capacitance will also decrease the output voltage ripple. A lower value of output capacitor can be used to save space and cost but transient performance will suffer and may cause loop instability. See the Typical Applications in this data sheet for suggested capacitor values.

When choosing a capacitor, special attention should be given to the data sheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

Ceramic Capacitors

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8609S due to their piezoelectric nature. When in Burst Mode operation, the LT8609S's switching frequency depends on the load current, and at very light loads the LT8609S can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT8609S operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LT8609S. As previously mentioned, a ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT8609S circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8609S's rating. This situation is easily avoided (see Analog Devices Application Note 88).

Enable Pin

The LT8609S is in shutdown when the EN pin is low and active when the pin is high. The rising threshold of the EN comparator is 1.05V, with 50mV of hysteresis. The EN pin

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can be tied to V_{IN} if the shutdown feature is not used, or tied to a logic level if shutdown control is required.

Adding a resistor divider from V_{IN} to EN programs the LT8609S to regulate the output only when V_{IN} is above a desired voltage (see Block Diagram). Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. This threshold can be adjusted by setting the values R3 and R4 such that they satisfy the following equation:

$$V_{IN(EN)} = \left(\frac{R3}{R4} + 1\right) \bullet 1V$$

where the LT8609S will remain off until V_{IN} is above $V_{IN(EN)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $V_{IN(EN)}$.

When in Burst Mode operation for light-load currents, the current through the $V_{IN(EN)}$ resistor network can easily be greater than the supply current consumed by the LT8609S. Therefore, the $V_{IN(EN)}$ resistors should be large to minimize their effect on efficiency at low loads.

$INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces the 3.5V supply from V_{IN} that powers the drivers and the internal bias circuitry. The $INTV_{CC}$ can supply enough current for the LT8609S's circuitry and must be bypassed to ground with a minimum of 1µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. Applications with high input voltage and high switching frequency will increase die temperature because of the higher power dissipation across the LDO. Do not connect an external load to the $INTV_{CC}$ pin.

Output Voltage Tracking and Soft-Start

The LT8609S allows the user to program its output voltage ramp rate by means of the TR/SS pin. An internal 2µA pulls up the TR/SS pin to $INTV_{CC}$. Putting an external capacitor on TR/SS enables soft-starting the output to prevent current surge on the input supply. During the soft-start ramp the output voltage will proportionally track the TR/SS pin voltage. For output tracking applications, TR/SS can be externally driven by another voltage source. From 0V to 0.774V, the TR/SS voltage will override the internal 0.774V reference input to the error amplifier, thus regulating the FB pin voltage to that of TR/SS pin. When TR/SS is above 0.774V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage.

An active pull-down circuit is connected to the TR/SS pin which will discharge the external soft-start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the EN/UV pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

Output Power Good

When the LT8609S's output voltage is within the ±8.5% window of the regulation point, which is a V_{FB} voltage in the range of 0.716V to 0.849V (typical), the output voltage is considered good and the open-drain PG pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal drain pull-down device will pull the PG pin low. To prevent glitching both the upper and lower thresholds include 0.5% of hysteresis.

The PG pin is also actively pulled low during several fault conditions: EN/UV pin is below 1V, $INTV_{CC}$ has fallen too low, V_{IN} is too low, or thermal shutdown.

Synchronization

To select low ripple Burst Mode operation, tie the SYNC pin below 0.4V (this can be ground or a logic low output). To synchronize the LT8609S oscillator to an external frequency connect a square wave (with 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below 0.9V and peaks above 2.7V (up to 5V).

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The LT8609S will not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead will pulse skip to maintain regulation. The LT8609S may be synchronized over a 200kHz to 2.2MHz range. The R_T resistor should be chosen to set the LT8609S switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the R_T should be selected for 500kHz. The slope compensation is set by the R_T value, while the minimum slope compensation required to avoid subharmonic oscillations is established by the inductor size, input voltage, and output voltage. Since the synchronization frequency will not change the slopes of the inductor current waveform, if the inductor is large enough to avoid subharmonic oscillations at the frequency set by R_T, then the slope compensation will be sufficient for all synchronization frequencies.

For some applications it is desirable for the LT8609S to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. First is the clock stays awake at all times and all switching cycles are aligned to the clock. Second is that full switching frequency is reached at lower output load than in Burst Mode operation as shown in Figure 1b in an earlier section. These two differences come at the expense of increased quiescent current. To enable pulse-skipping mode the SYNC pin is floated.

For some applications, reduced EMI operation may be desirable, which can be achieved through spread spectrum modulation. This mode operates similar to pulse skipping mode operation, with the key difference that the switching frequency is modulated up and down by a 3 kHz triangle wave. The modulation has the frequency set by R_T as the low frequency, and modulates up to approximately 20% higher than the frequency set by R_T. To enable spread spectrum mode, tie SYNC to $INTV_{CC}$ or drive to a voltage between 3.2V and 5V.

The LT8609S does not operate in forced continuous mode regardless of SYNC signal.

Shorted and Reversed Input Protection

The LT8609S will tolerate a shorted output. Several features are used for protection during output short-circuit and brownout conditions. The first is the switching frequency will be folded back while the output is lower than the set point to maintain inductor current control (only if SYNC = 0V).. Second, the bottom switch current is monitored such that if inductor current is beyond safe levels switching of the top switch will be delayed until such time as the inductor current falls to safe levels. This allows for tailoring the LT8609S to individual applications and limiting thermal dissipation during short circuit conditions.

Frequency foldback behavior depends on the state of the SYNC pin: If the SYNC pin is low or high, or floated the switching frequency will slow while the output voltage is lower than the programmed level. If the SYNC pin is connected to a clock source, the LT8609S will stay at the programmed frequency without foldback and only slow switching if the inductor current exceeds safe levels.

There is another situation to consider in systems where the output will be held high when the input to the LT8609S is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode ORed with the LT8609S's output. If the V_{IN} pin is allowed to float and the EN pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT8609S's internal circuitry will pull its quiescent current through its SW pin. This is acceptable if the system can tolerate several µA in this state. If the EN pin is grounded the SW pin current will drop to near 0.7µA. However, if the V_{IN} pin is grounded while the output is held high, regardless of EN, parasitic body diodes inside the LT8609S can pull current from the output through the SW pin and the V_{IN} pin. Figure 3 shows a connection of the V_{IN} and EN/UV pins that will allow the LT8609S to run only when the input voltage is present and that protects against a shorted or reversed input.

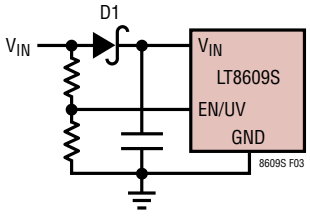

Figure 3. Reverse V_{IN} Protection

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PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 4 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT8609S's V_{IN} pins, GND pins, and the input capacitor (C_{IN}). The loop formed by the input capacitor should be as small as possible by placing the capacitor adjacent to the V_{IN} and GND pins. When using a physically large input capacitor the resulting loop may become too large in which case using a small case/value capacitor placed close to the V_{IN} and GND pins plus a larger capacitor further away is preferred. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW node should be as small as possible. Finally, keep the FB and RT nodes small so that the ground traces will shield them from the SW node. The exposed pad on the bottom of the package must be soldered to ground so that the pad is connected to ground electrically and also acts as a heat sink thermally. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT8609S to additional ground planes within the circuit board and on the bottom side. For mechanical performance during temperature cycles, solder the corner N/C pins to the ground plane.

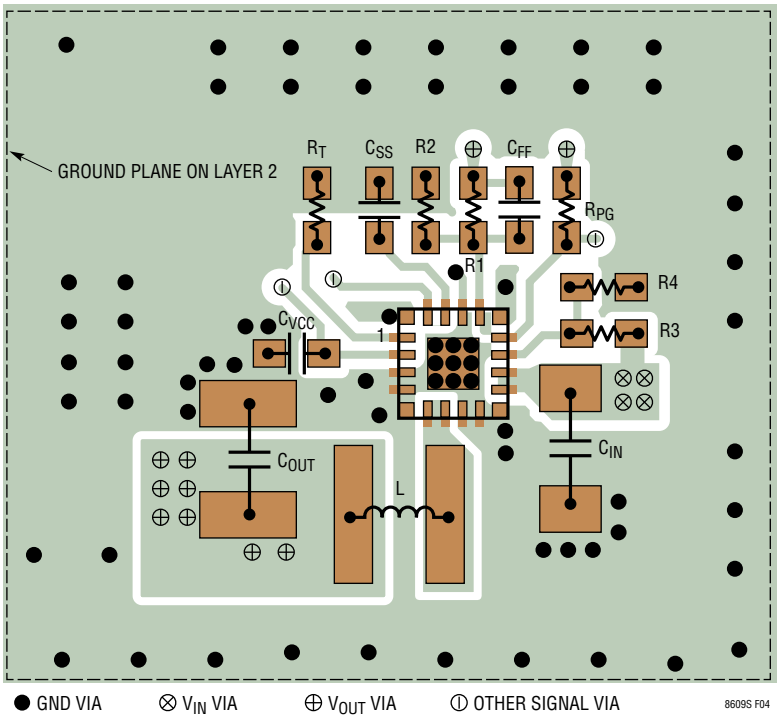

Figure 4. PCB Layout

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Thermal Considerations and Peak Current Output

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT8609S. The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT8609S. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LT8609S can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The die temperature is calculated by multiplying the LT8609S power dissipation by the thermal resistance from junction to ambient. The LT8609S will stop switching and indicate a fault condition if safe junction temperature is exceeded.

Temperature rise of the LT8609S is worst when operating at high load, high V_{IN}, and high switching frequency. If the case temperature is too high for a given application, then either V_{IN}, switching frequency or load current can be decreased to reduce the temperature to an acceptable level. Figure 5 shows how case temperature rise can be managed by reducing V_{IN}.

The LT8609S's internal power switches are capable of safely delivering up to 3A of peak output current. However, due to thermal limits, the package can only handle 3A loads for short periods of time. This time is determined by how quickly the case temperature approaches the maximum junction rating. Figure 6 shows an example of how case temperature rise changes with the duty cycle of a 10Hz pulsed 3A load. Junction temperature will be higher than case temperature.

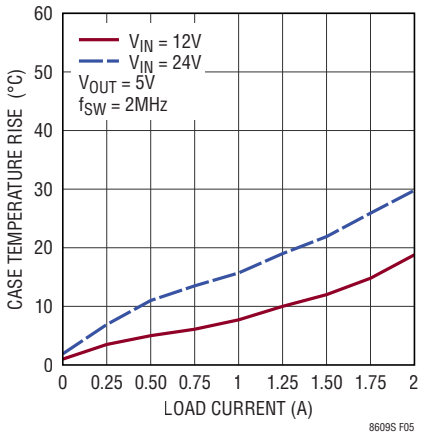


Figure 5. Case Temperature Rise vs Load Current

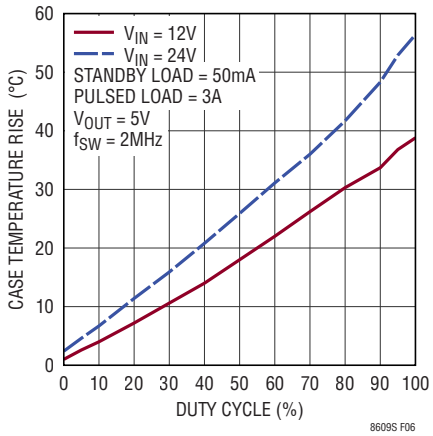
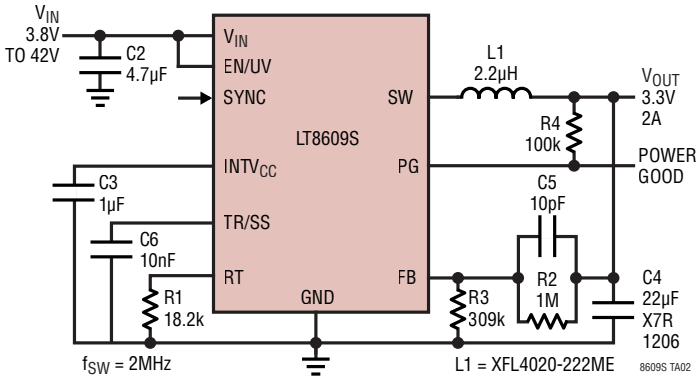


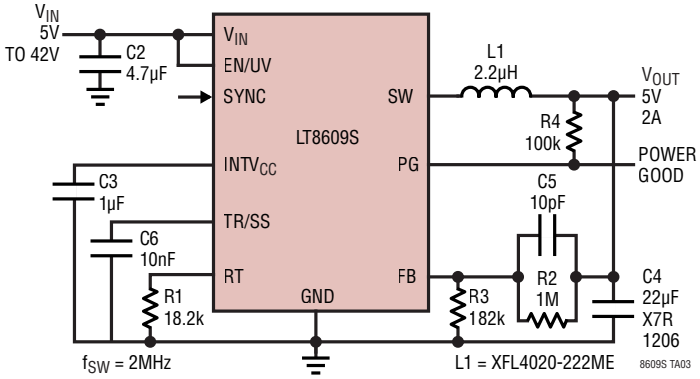
Figure 6. Case Temperature Rise vs 3A Pulsed Load

TYPICAL APPLICATIONS

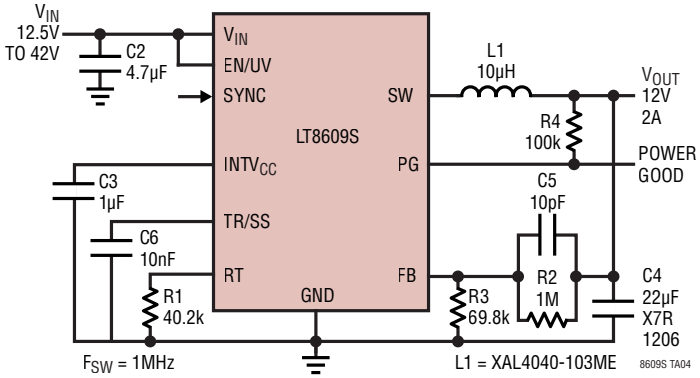
3.3V Step Down



5V Step Down

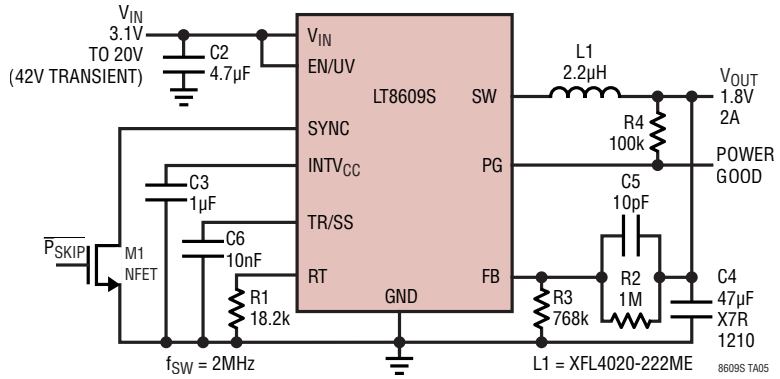


12V Step Down

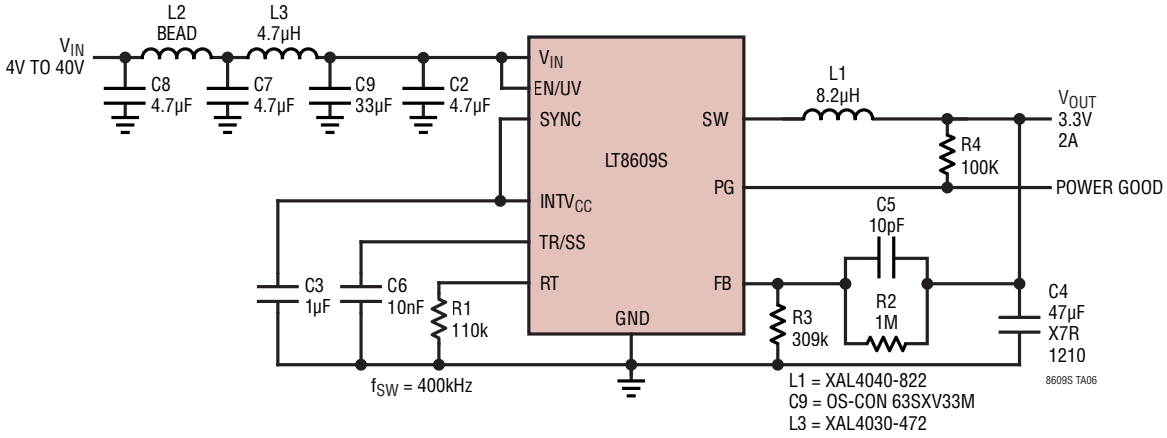


TYPICAL APPLICATIONS

1.8V 2MHz Step-Down Converter

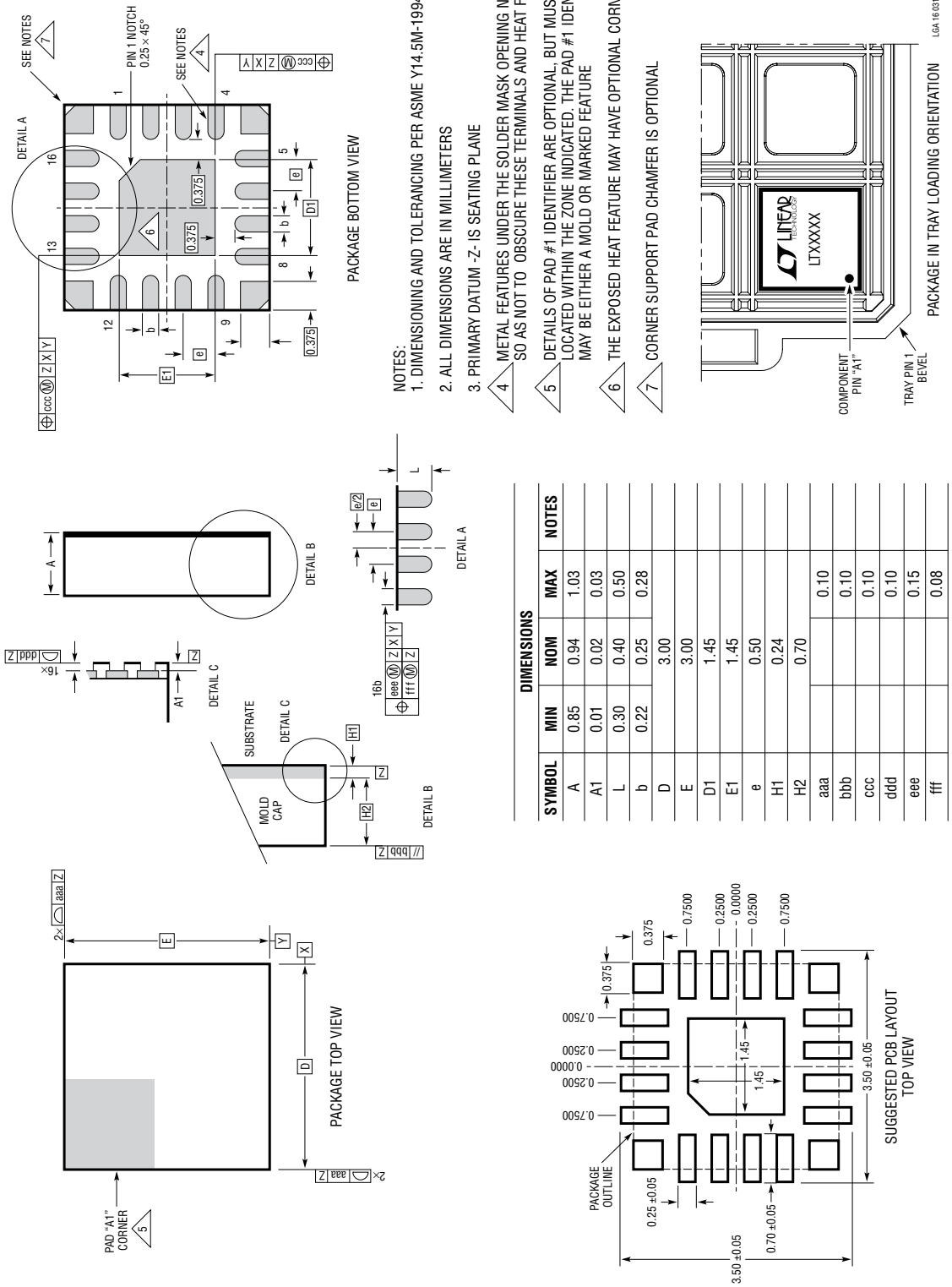


Ultralow EMI 3.3V 2A Step-Down Converter



PACKAGE DESCRIPTION

LQFN Package
16-Lead (3mm × 3mm × 0.94mm)
(Reference LTC DWG # 05-08-1516 Rev B)



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.85	0.94	1.03	
A1	0.01	0.02	0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		3.00		
E		3.00		
D1		1.45		
E1		1.45		
e		0.50		
H1		0.24		
H2		0.70		
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

Rev. D

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/17	Clarified Oscillator Frequency R_T Conditions	3
		Clarified Frequency Foldback Graph	6
		Clarified Block Diagram	11
		Clarified Operating Frequency Selection in Applications Information	14
		Clarified PCB Layout in Figure 4	18
		Clarified Figure 5 and 6	19
B	04/20	Updated θ_{JA} in Pin Configuration Diagram	2
		Added Note 4	3
		Update Electrical Characteristics table Minimum On-Time parameter with I_{LOAD} from 1.5A to 1.75A	3
C	10/20	Added AEC-Q statement and #W ordering information	1, 2
D	02/21	Added Tape and Reel in the Order Information table	2