1.5GHz to 7GHz Programmable Gain Downconverting Mixer

FEATURES

- **Optimized Gain Flatness from 2.5GHz to 7GHz**
- **31dBm Output IP3**
- **9dB Power Conversion Gain**
- **15.5dB Adjustable Gain Range**
- SPI or Parallel Gain Control in 0.5dB Steps
- Very Small Solution Size
- 3.3V Single Supply
- Low Power and Shutdown Modes
- 28-Lead (4mm × 5mm) QFN Package

APPLICATIONS

- 3.6GHz, 4.8GHz and 5.8GHz Band Wireless Infrastructure Receivers
- Wireless Repeaters
- Military Radar and Communications Receivers
- Test and Measurement Equipment
- Software-Defined Radios

DESCRIPTION

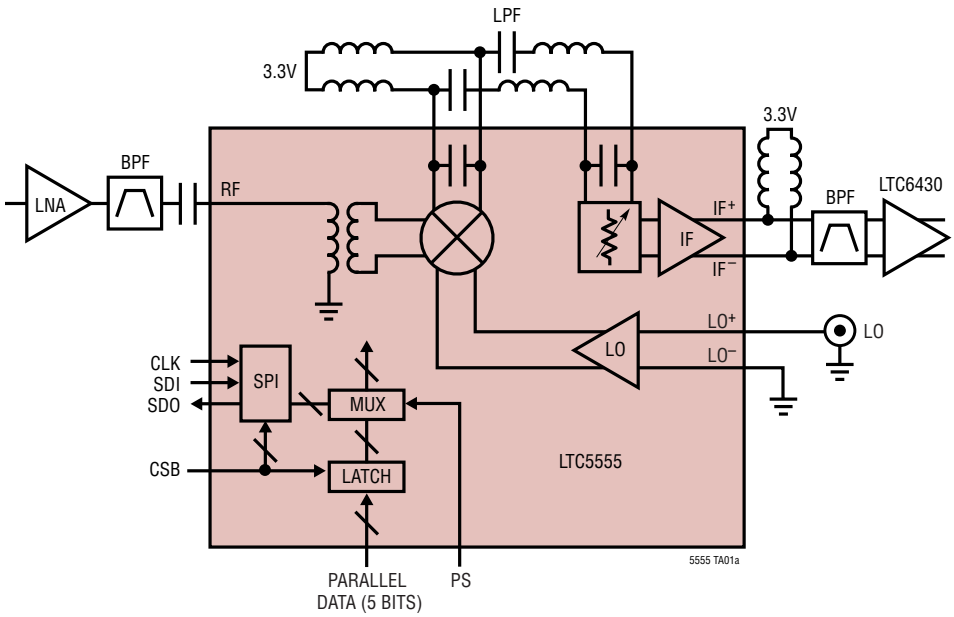
The LTC®5555 programmable gain downconverting mixer is ideal for receivers that require precise gain setting. The IC incorporates an active mixer and a digital IF VGA with 15.5dB gain control range. The IF gain is programmed in 0.5dB steps through the SPI or parallel interface.

An enable pin allows for fast turn-on and shutdown. A reduced power modes is also available.

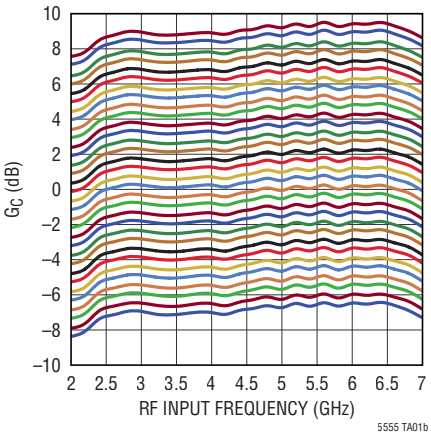
An integrated RF transformer provides a single-ended 50Ω input. The differential LO input is designed for single-ended or differential drive. The differential IF output simplifies the interface to differential IF filters and amplifiers. The mixer is optimized for the 3GHz to 7GHz RF frequency range but may be used down to 1.5GHz with degraded performance.

TYPICAL APPLICATION

Receiver with Programmable 0.5dB Gain Steps



LTC5555 Conversion Gain vs RF Frequency and IF Attenuation (0.5dB Gain Steps)



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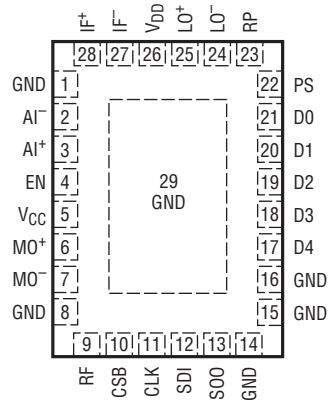
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}, V_{CC}, IF^+, IF^-) 4V
EN Input Voltage ..... –0.3V to V_{CC} + 0.3V, 4V MAX
LO^+, LO^- Input Power (500MHz to 8GHz) ..... +10dBm
RF Input Power (1.5GHz to 7GHz) ..... +20dBm
LO^+, LO^- DC Voltage ..... ±0.5V
IF DVGA Peak Differential Input Voltage ..... ±4V
PS Input Voltage ..... –0.3V to V_{DD} + 0.3V, 4V MAX
SDI, CLK, CSB, RP, D_X Input
Voltages ..... –0.3V to V_{DD} + 0.3V, 4V MAX
SDO Voltage ..... –0.3V to V_{DD} + 0.3V, 4V MAX
Operating Temperature Range (T_C) ..... –40°C to 105°C
Junction Temperature (T_J) ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JC} = 6°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	CASE TEMPERATURE RANGE
LTC5555IUFD#PBF	LTC5555IUFD#TRPBF	5555	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 105°C

Contact the factory for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = V_{DD} = 3.3V. Test circuit shown in Figure 1. (Notes 3, 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})		●	3.0	3.3	3.6	V
Logic Supply Voltage (V_{DD})		●	1.6		3.6	V
Supply Current (I_{CC})	Full Power Mode Reduced Power Mode Shutdown			192 147 0.52	225 0.9	mA mA mA
Logic Supply Current (I_{DD})	Operating: CSB = Low, f_{CLK} =10MHz Idle: CSB = High			0.2 10	1	mA µA
Enable and Parallel Select Inputs (EN, PS) Internal Pull-Down Resistors on Each Pin						
Input High Voltage (On)		●	1.4			V
Input Low Voltage (Off)		●			0.5	V
Input Current	V_{IN} = V_{CC} = 3.6V				100	µA
Enable Turn-On Time				0.3		µs
Enable Turn-Off Time				0.1		µs
Parallel Data Inputs and Reduced Power Select (D_X, RP) Internal Pull-Down Resistor on RP						
Input High Voltage		●	0.7 • V_{DD}			V
Input Low Voltage		●			0.3 • V_{DD}	V
Input Current	V_{IN} = V_{DD} = 3.6V				50	µA
Latch Enable Setup Time (Note 5)			10			ns
Latch Enable Hold Time (Note 5)			15			ns
SPI Port Logic Inputs (CSB, CLK, SDI)						
Input High Voltage		●	0.7 • V_{DD}			V
Input Low Voltage		●			0.3 • V_{DD}	V
Input Current	V_{IN} = V_{DD} = 3.6V				25	µA
Input Hysteresis				200		mV
SPI Port Logic Output (SDO)						
Output High Voltage	I_{SOURCE} = 3mA	●	V_{DD} – 0.4V			V
Output Low Voltage	I_{SINK} = 3mA	●			0.4	V
Output Leakage Current (High-Z)	V_{CSB} = V_{DD} = 3.6V				±20	µA
SPI Port Timing (Note 5)						
SDI Setup Time			5			ns
SDI Hold Time			10			ns
CLK Falling to SDO Valid Time	C_{SDO} = 20pF				15	ns
SDO Rise/Fall Time	C_{SDO} = 20pF			5		ns
SDO Enable Time					10	ns
SDO Disable Time					10	ns
CSB Setup Time			15			ns
CSB Hold Time			5			ns
CLK Frequency	C_{SDO} = 20pF				20	MHz

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = V_{DD} = 3.3V, EN = High, P_{LO} = 0dBm. Test circuit shown in Figure 1. (Notes 3, 4, 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF Input Frequency Range	External Matching Required	●		1.5 to 7		GHz
LO Input Frequency Range		●		0.5 to 8		GHz
IF Output Frequency Range	External Matching Required	●		1 to 900		MHz
1dB IF Gain Rolloff	Relative to 100MHz Gain			700		MHz
IF Gain Error at 150MHz	Differential; Between Any Two 0.5dB Atten Steps Integral; Over Entire 15.5dB IF Atten Range			±0.04 0.39		dB dB
IF Phase Error	IF = 150MHz, Full 15.5dB Atten Range IF = 350MHz, Full 15.5dB Atten Range			3.6 5.1		Deg Deg
LO Input Return Loss	Single-Ended, Z_O = 50Ω, 500MHz to 7GHz			>9		dB
LO Input Power	Single-Ended or Differential	●	–6	0	6	dBm
Mixer IF Output Impedance	Differential, 10MHz to 1GHz			200Ω || 1pF		R || C
IF DVGA Input Impedance	Differential, 10MHz to 1GHz			200Ω || 1pF		R || C
IF DVGA Output Impedance	Differential, 10MHz to 1GHz			206Ω || 1pF		R || C
RF to LO Isolation	RF = 1.5GHz to 1.7GHz RF = 1.7GHz to 7GHz			>51 >43		dB dB
RF to Unbalanced IF Isolation	RF = 1.5GHz to 1.8GHz RF = 1.8GHz to 7GHz			>55 >52		dB dB
LO to Unbalanced IF Port Leakage	LO = 500MHz to 1.3GHz LO = 1.3GHz to 8GHz			<–26 <–40		dBm dBm

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = V_{DD} = 3.3V, EN = High, P_{RF} = –6dBm/Tone, P_{LO} = 0dBm, unless otherwise noted. Test circuit shown in Figure 1. (Notes 3, 4, 5)

2.6GHz to 6.4GHz RF Input Matching (See Figure 1): RF = 3.6GHz, IF = 270MHz, Low Side LO

PARAMETER	CONDITIONS		FULL PWR MIN	FULL PWR TYP	FULL PWR MAX	REDUCED PWR TYP	UNITS
RF Input Return Loss	Z_O = 50Ω, 2.6GHz to 6.4GHz			>10		>10	dB
Power Conversion Gain	0dB IF ATTEN			9.2		8.7	dB
	3dB IF ATTEN		4.4	6.1		5.6	dB
	6dB IF ATTEN			3.0		2.5	dB
	9dB IF ATTEN			0.0		–0.5	dB
	12dB IF ATTEN			–3.1		–3.6	dB
	15dB IF ATTEN			–6.2		–6.7	dB
Conversion Gain Flatness	RF = 3.6GHz ±100MHz, LO = 3.33GHz			±0.30		±0.30	dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C	●		–0.013		–0.013	dB/°C
Two-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN			22.0		17.7	dBm
	3dB IF ATTEN			22.6		18.1	dBm
	6dB IF ATTEN			23.2		18.4	dBm
	9dB IF ATTEN			23.4		18.5	dBm
	12dB IF ATTEN			23.4		18.6	dBm
	15dB IF ATTEN			23.5		18.6	dBm
Two-Tone Output 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN			31.1		26.4	dBm
	3dB IF ATTEN			28.7		23.7	dBm
	6dB IF ATTEN			26.2		20.9	dBm
	9dB IF ATTEN			23.4		18.0	dBm
	12dB IF ATTEN			20.3		15.0	dBm
	15dB IF ATTEN			17.4		11.9	dBm
Two-Tone Input 2nd Order Intercept (Δf_{RF} = 271MHz = f_{IM2})	0dB to 15.5dB IF ATTEN			56		53	dBm
SSB Noise Figure	0dB IF ATTEN			13.8		12.9	dB
	3dB IF ATTEN			15.1		14.4	dB
	6dB IF ATTEN			16.6		16.2	dB
	9dB IF ATTEN			18.6		18.5	dB
	12dB IF ATTEN			21.2		21.1	dB
	15dB IF ATTEN			23.9		24.0	dB
SSB Noise Figure Under Blocking (3.7GHz Blocker)	+2dBm BLOCKER, 3dB IF ATTEN			19.1		18.9	dB
	+5dBm BLOCKER, 3dB IF ATTEN			21.6		21.6	dB
LO to RF Leakage	LO = 1.5GHz to 7GHz			<–42		<–42	dBm
1/2 IF Output Spurious Product (f_{RF} Offset to Produce Spur at f_{IF} = 270MHz)	f_{RF} = 3465MHz, P_{RF} = –6dBm 0dB to 15.5dB IF ATTEN			–59		–58	dBc
1/3 IF Output Spurious Product (f_{RF} Offset to Produce Spur at f_{IF} = 270MHz)	f_{RF} = 3420MHz, P_{RF} = –6dBm 0dB to 15.5dB IF ATTEN			–64		–60	dBc
Input 1dB Compression	0dB IF ATTEN			8.9		7.8	dBm
	3dB IF ATTEN			10.8		9.4	dBm
	6dB IF ATTEN			11.3		9.7	dBm
	9dB IF ATTEN and Higher			11.3		9.8	dBm
Output 1dB Compression	0dB IF ATTEN			17.0		15.6	dBm
	3dB IF ATTEN			15.7		14.1	dBm
	6dB IF ATTEN			13.2		11.4	dBm
	9dB IF ATTEN			10.1		8.4	dBm

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = V_{DD} = 3.3V, EN = High, P_{RF} = –6dBm/Tone, P_{LO} = 0dBm, unless otherwise noted. Test circuit shown in Figure 1. (Notes 3, 4, 5)

2.6GHz to 6.4GHz RF Input Matching (See Figure 1): RF = 5.5GHz, IF = 270MHz, Low Side LO

PARAMETER	CONDITIONS		FULL PWR MIN	FULL PWR TYP	FULL PWR MAX	REDUCED PWR TYP	UNITS
Power Conversion Gain	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			9.5 3.3 –2.8		8.9 2.7 –3.4	dB dB dB
Conversion Gain Flatness	RF = 5.5GHz ±200MHz, LO = 5.23GHz			±0.7		±0.7	dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C	●		–0.014		–0.014	dB/°C
Two-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			20.2 20.5 20.5		14.4 14.8 14.8	dBm dBm dBm
Two-Tone Input 2nd Order Intercept (Δf_{RF} = 271MHz = f_{IM2})	0dB to 15.5dB IF ATTEN			43		45	dBm
SSB Noise Figure	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			14.0 16.5 20.8		12.7 15.9 20.6	dB dB dB
SSB Noise Figure Under Blocking (F_{RF} = 5.735GHz, F_{BLOCK} = 5.835GHz)	+2dBm Blocker, 3dB IF ATTEN +5dBm Blocker, 3dB IF ATTEN			18.8 20.9		18.7 21.0	dB dB
Input 1dB Compression	0dB IF ATTEN 3dB IF ATTEN 6dB IF ATTEN 9dB IF ATTEN and Higher			7.9 9.1 9.3 9.3		7.4 8.8 9.1 9.1	dBm dBm dBm dBm

RF = 4.6GHz, IF = 270MHz, Low Side LO

PARAMETER	CONDITIONS		FULL PWR MIN	FULL PWR TYP	FULL PWR MAX	REDUCED PWR TYP	UNITS
Power Conversion Gain	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			9.3 3.2 –3.0		8.7 2.6 –3.6	dB dB dB
Conversion Gain Flatness	RF = 4.6GHz ±200MHz, LO = 4.33GHz			±0.6		±0.6	dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C	●		–0.013		–0.013	dB/°C
Two-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			22.3 21.9 21.6		16.1 16.5 16.6	dBm dBm dBm
Two-Tone Input 2nd Order Intercept (Δf_{RF} = 271MHz = f_{IM2})	0dB to 15.5dB IF ATTEN			42		41	dBm
SSB Noise Figure	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			14.3 16.7 21.1		13.2 16.2 21.0	dB dB dB
SSB Noise Figure Under Blocking (F_{RF} = 4.9GHz, F_{BLOCK} = 5.0GHz)	+2dBm Blocker, 3dB IF ATTEN +5dBm Blocker, 3dB IF ATTEN			19.3 21.4		19.1 21.3	dB dB
Input 1dB Compression	0dB IF ATTEN 3dB IF ATTEN 6dB IF ATTEN 9dB IF ATTEN and Higher			8.3 9.8 10.2 10.2		7.7 9.4 9.7 9.8	dBm dBm dBm dBm

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = V_{DD} = 3.3V, EN = High, P_{RF} = –6dBm/Tone, P_{LO} = 0dBm, unless otherwise noted. Test circuit shown in Figure 1. (Notes 3, 4, 5)

2.2GHz to 3.2GHz RF Input Matching (See Figure 1): RF = 2.6GHz, IF = 270MHz, Low Side LO

PARAMETER	CONDITIONS		FULL PWR MIN	FULL PWR TYP	FULL PWR MAX	REDUCED PWR TYP	UNITS
RF Input Return Loss	Z_O = 50Ω, 2.2GHz to 3.2GHz			>10		>10	
LO to RF Leakage	LO = 1.4GHz to 3.8GHz			<–48		<–48	
Power Conversion Gain	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			9.0 2.8 –3.3		8.4 2.3 –3.9	dB dB dB
Conversion Gain Flatness	RF = 2.6GHz ±100MHz, LO = 2.33GHz			±0.25		±0.25	dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C	●		–0.012		–0.012	dB/°C
Two-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			26.2 27.7 27.4		19.1 20.1 20.3	dBm dBm dBm
Two-Tone Input 2nd Order Intercept (Δf_{RF} = 271MHz = f_{IM2})	0dB to 15.5dB IF ATTEN			52		56	dBm
SSB Noise Figure	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			12.8 16.1 21.0		12.1 15.8 21.3	dB dB dB
SSB Noise Figure Under Blocking (F_{IN} = 2.6GHz, F_{BLOCK} = 2.7GHz)	+2dBm Blocker +5dBm Blocker			18.3 20.5		18.3 20.6	dB dB
Input 1dB Compression	0dB IF ATTEN 3dB IF ATTEN 6dB IF ATTEN 9dB IF ATTEN and Higher			9.6 11.5 12.3 12.4		8.5 10.6 11.0 11.2	dBm dBm dBm dBm

1.5GHz to 2.1GHz RF Input Matching (See Figure 1): RF = 1.8GHz, IF = 270MHz, Low Side LO

PARAMETER	CONDITIONS		FULL PWR MIN	FULL PWR TYP	FULL PWR MAX	REDUCED PWR TYP	UNITS
RF Input Return Loss	Z_O = 50Ω, 1.5GHz to 2.1GHz			>10		>10	dB
LO to RF Leakage	LO = 500MHz to 3GHz			<–54		≤–54	dBm
Power Conversion Gain	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			8.9 2.7 –3.4		8.4 2.3 –3.8	dB dB dB
SSB Noise Figure	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			12.6 16.2 21.2		12.1 16.1 21.4	dB dB dB
SSB Noise Figure Under Blocking (F_{IN} = 1860MHz, F_{BLOCK} = 1960MHz)	+2dBm Blocker +5dBm Blocker			18.6 20.7		18.5 20.8	dB dB
Two-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			22.3 23.6 24.0		19.6 20.8 21.1	dBm dBm dBm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The mixer output pins on this device are sensitive to ESD greater than 1kV (HBM). Proper ESD handling precautions must be observed. All other pins withstand 2kV.

Note 3: The LTC5555 is guaranteed functional over the –40°C to 105°C case temperature range.

Note 4: SSB Noise Figure measured with a small-signal noise source, bandpass filter and 2dB matching pad on RF input, and bandpass filter on the LO input.

Note 5: SPI and parallel timing guaranteed by design, not subject to test.

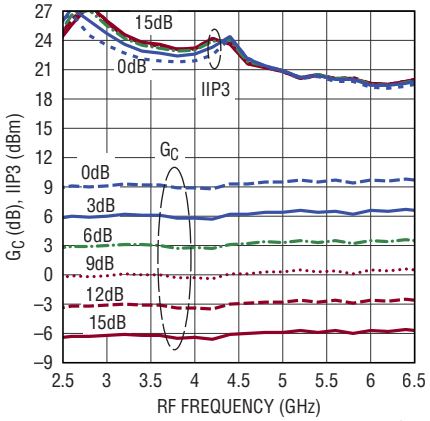
TYPICAL PERFORMANCE CHARACTERISTICS

Test circuit shown in Figure 1.

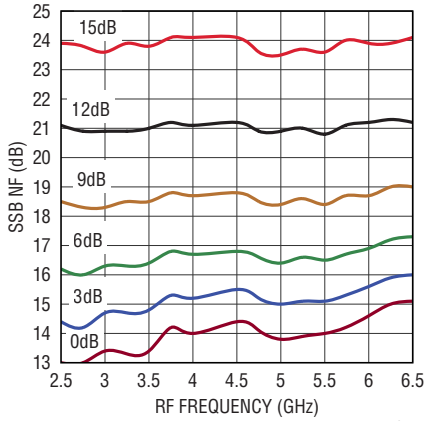
P_{RF} = –6dBm/Tone, Δf = 2MHz, P_{LO} = 0dBm, V_{CC} = 3.3V, V_{DD} = 3.3V, T_C = 25°C, full power mode, unless otherwise noted.

2.6GHz to 6.4GHz RF Input Matching: IF = 270MHz, Low Side LO

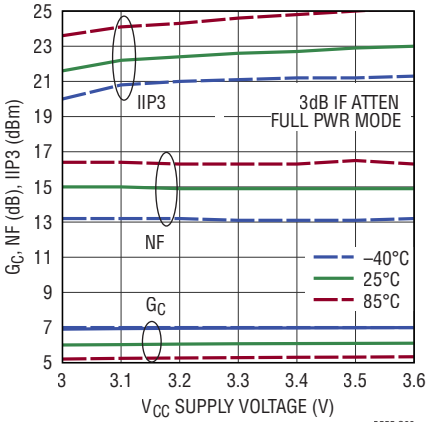
Conv Gain and IIP3 vs RF Frequency and IF Attenuation (3dB Steps)



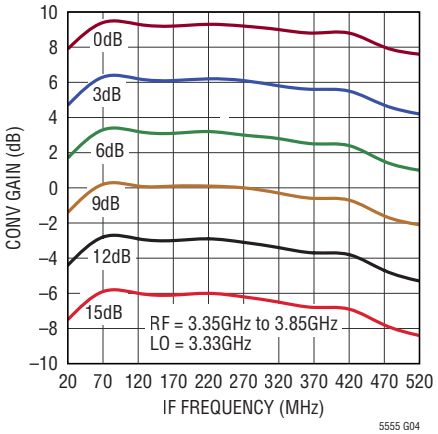
SSB NF vs RF Frequency and IF Attenuation (3dB Steps)



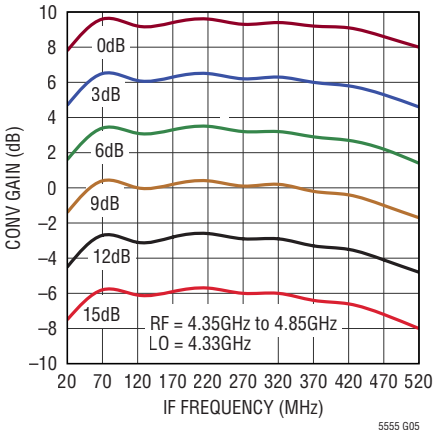
3.6GHz Conv Gain IIP3 and SSB NF vs V_{CC} and Case Temperature



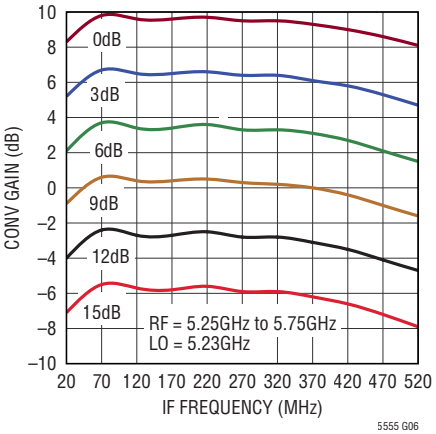
3.6GHz Conv Gain vs IF Frequency and Attenuation, Swept RF/Fixed LO



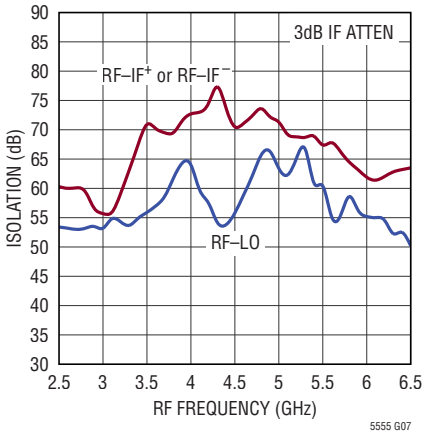
4.6GHz Conv Gain vs IF Frequency and Attenuation, Swept RF/Fixed LO



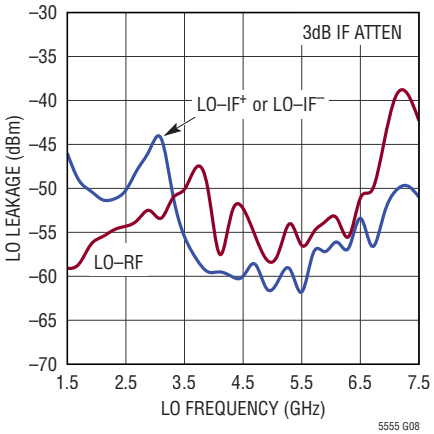
5.5GHz Conv Gain vs IF Frequency and Attenuation, Swept RF/Fixed LO



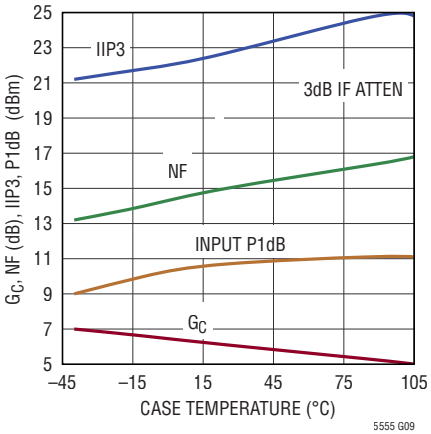
RF Isolation vs RF Frequency



LO Leakage vs LO Frequency



3.6GHz Conv Gain, IIP3, NF and RF Input P1dB vs Temperature



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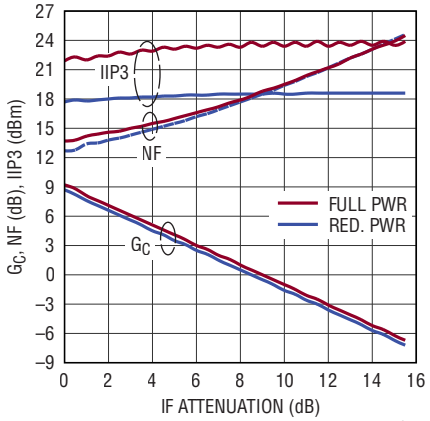
TYPICAL PERFORMANCE CHARACTERISTICS

Test circuit shown in Figure 1.

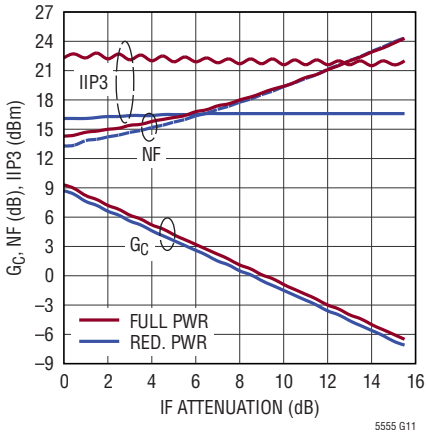
P_{RF} = –6dBm/Tone, Δf = 2MHz, P_{LO} = 0dBm, V_{CC} = 3.3V, V_{DD} = 3.3V, T_C = 25°C, full power mode, unless otherwise noted.

2.6GHz to 6.4GHz RF Input Matching: IF = 270MHz, Low Side LO

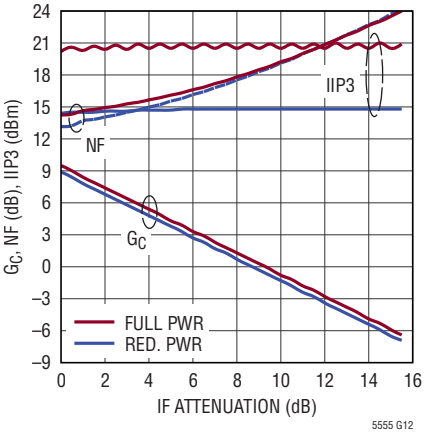
3.6GHz Conv Gain, IIP3, and SSB NF vs IF Attenuation (0.5dB Steps)



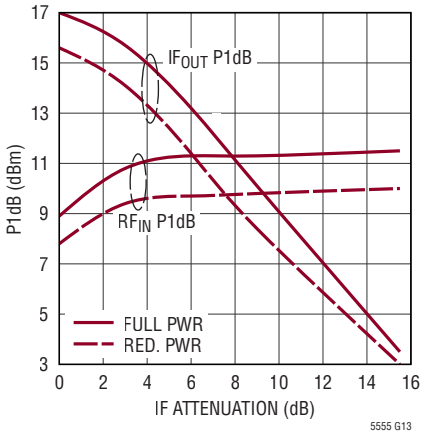
4.6GHz Conv Gain, IIP3, and SSB NF vs IF Attenuation (0.5dB Steps)



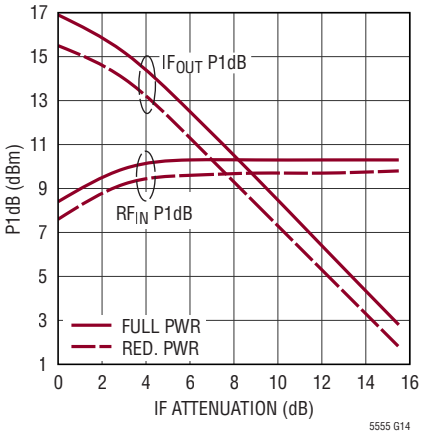
5.5GHz Conv Gain, IIP3, and SSB NF vs IF Attenuation (0.5dB Steps)



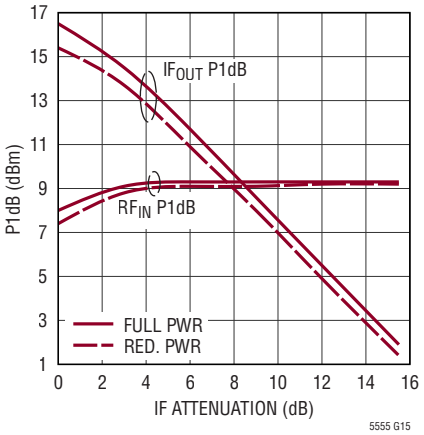
3.6GHz RF Input and IF Output P1dB vs IF Attenuation



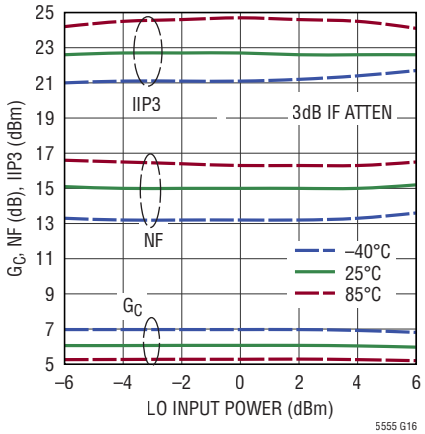
4.6GHz RF Input and IF Output P1dB vs IF Attenuation



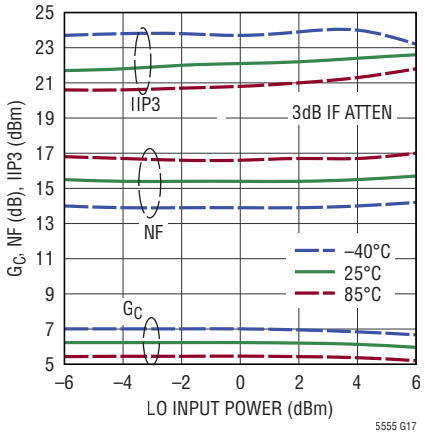
5.5GHz RF Input and IF Output P1dB vs IF Attenuation



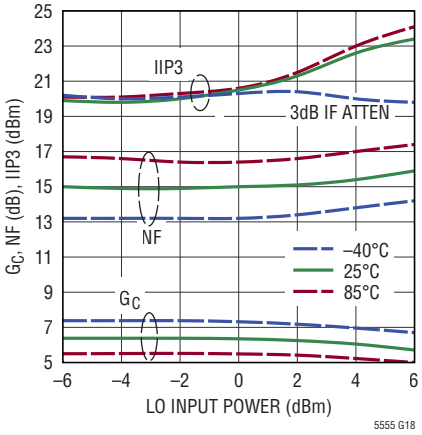
3.6GHz Conv Gain, IIP3 and SSB NF vs LO Power and Case Temperature



4.6GHz Conv Gain, IIP3 and SSB NF vs LO Power and Case Temperature



5.5GHz Conv Gain, IIP3 and SSB NF vs LO Power and Case Temperature



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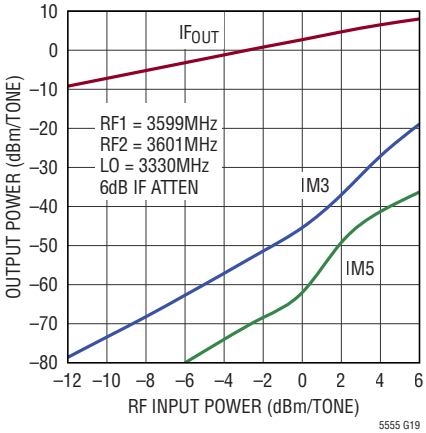
TYPICAL PERFORMANCE CHARACTERISTICS

Test circuit shown in Figure 1.

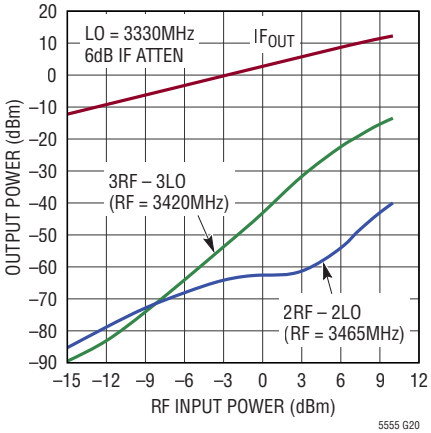
P_{RF} = –6dBm/Tone, Δf = 2MHz, P_{LO} = 0dBm, V_{CC} = 3.3V, V_{DD} = 3.3V, T_C = 25°C, full power mode, unless otherwise noted.

2.6GHz to 6.4GHz RF Input Matching: IF = 270MHz, Low Side LO

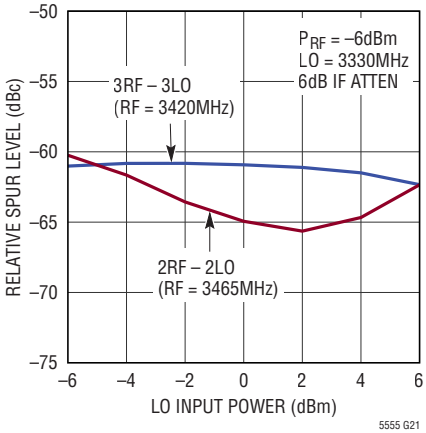
2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



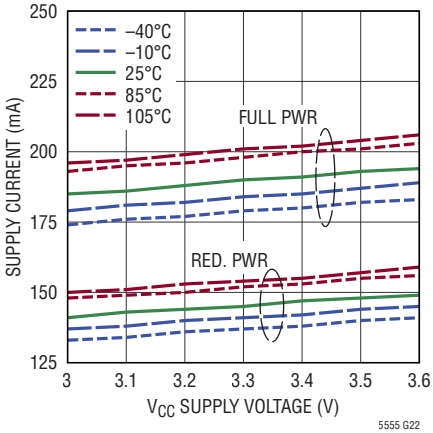
Single-Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power



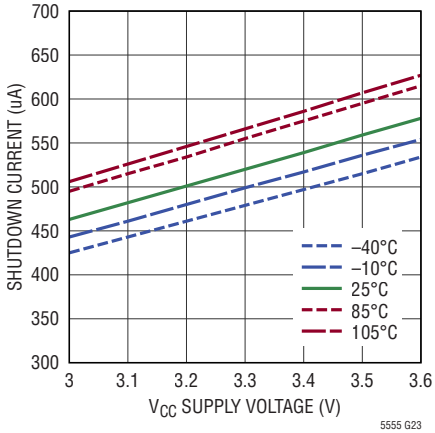
2 × 2 and 3 × 3 Spur Suppression vs LO Power



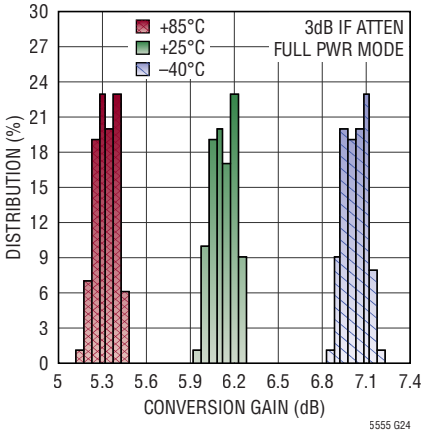
V_{CC} Supply Current vs Supply Voltage



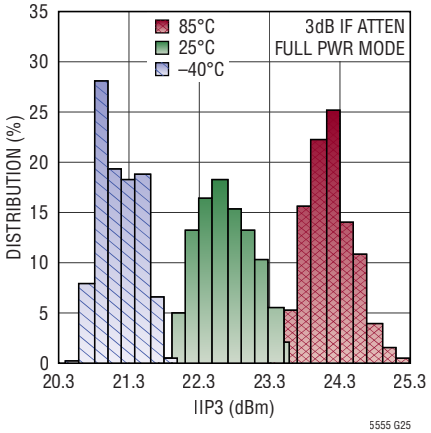
V_{CC} Shutdown Current vs Supply Voltage



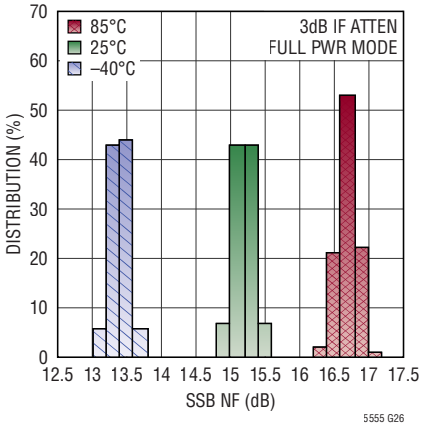
3.6GHz Conversion Gain Distribution



3.6GHz IIP3 Distribution



3.6GHz SSB NF Distribution



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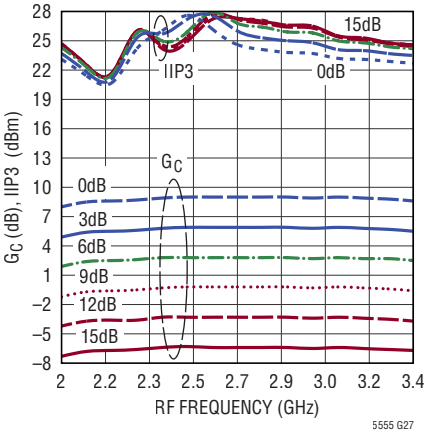
TYPICAL PERFORMANCE CHARACTERISTICS

Test circuit shown in Figure 1.

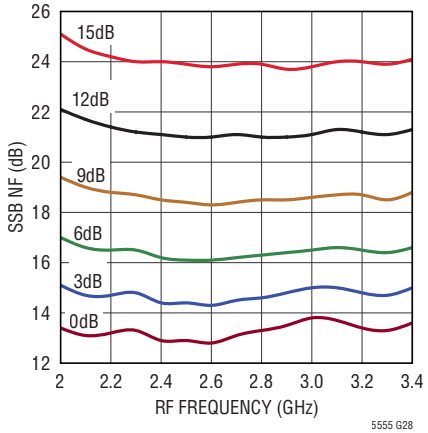
P_{RF} = –6dBm/Tone, Δf = 2MHz, P_{LO} = 0dBm, V_{CC} = 3.3V, V_{DD} = 3.3V, T_C = 25°C, full power mode, unless otherwise noted.

2.2GHz to 3.2GHz RF Input Matching: RF = 2.6GHz, IF = 270MHz, Low Side LO

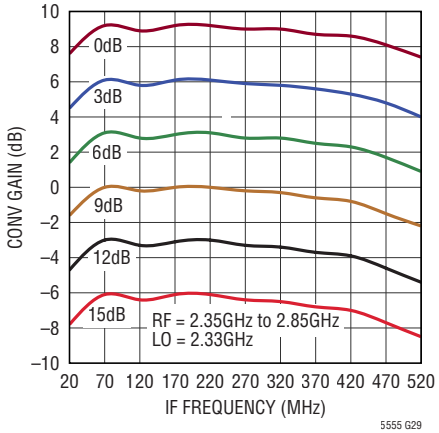
Conv Gain and IIP3 vs RF Frequency and IF Attenuation (3dB Steps)



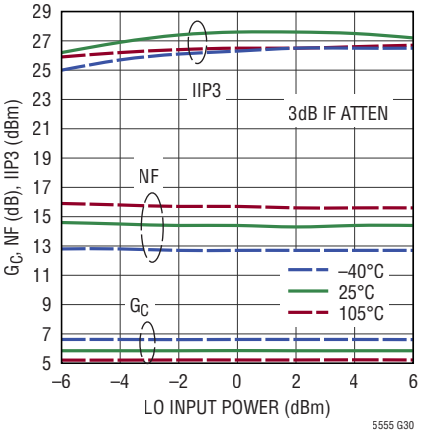
SSB NF vs RF Frequency and IF Attenuation (3dB Steps)



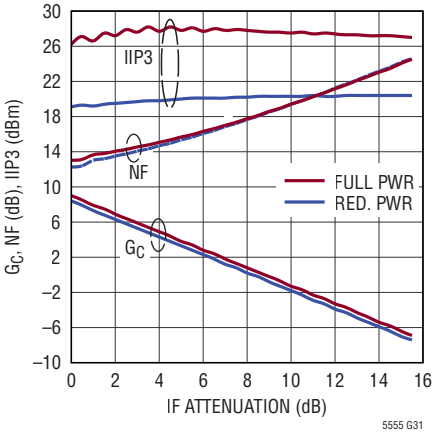
Conv Gain vs IF Frequency and Attenuation, Swept RF/Fixed LO



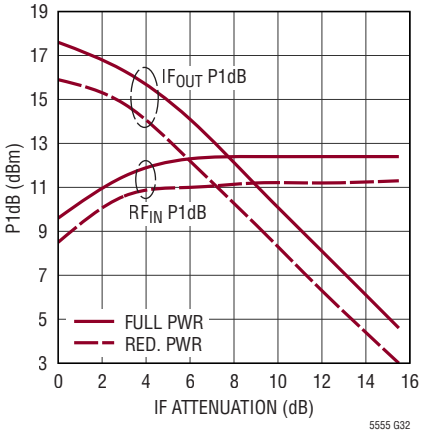
2.6GHz Conv Gain, IIP3 and SSB NF vs LO Power and Case Temperature



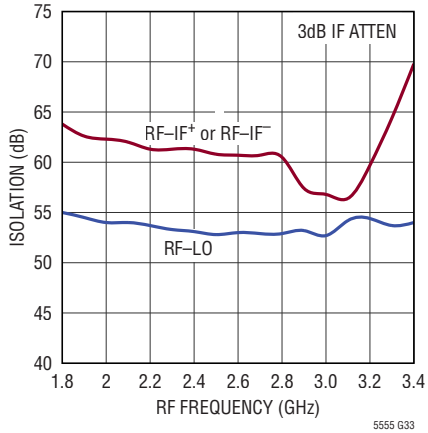
2.6GHz Conv Gain, IIP3 and SSB NF vs IF Attenuation (0.5dB Steps)



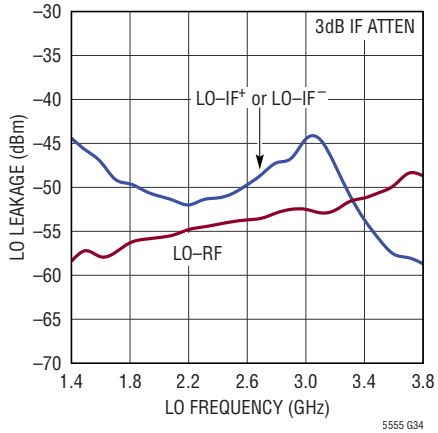
2.6GHz RF Input and IF Output P1dB vs IF Attenuation



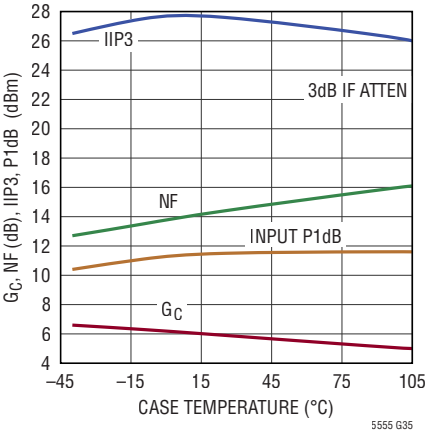
RF Isolation vs RF Frequency



LO Leakage vs LO Frequency



2.6GHz Conv Gain, IIP3, NF and RF Input P1dB vs Temperature



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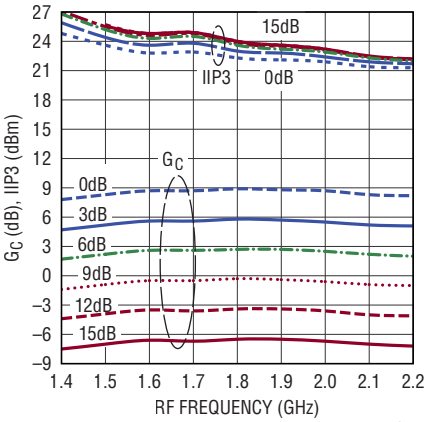
TYPICAL PERFORMANCE CHARACTERISTICS

Test circuit shown in Figure 1.

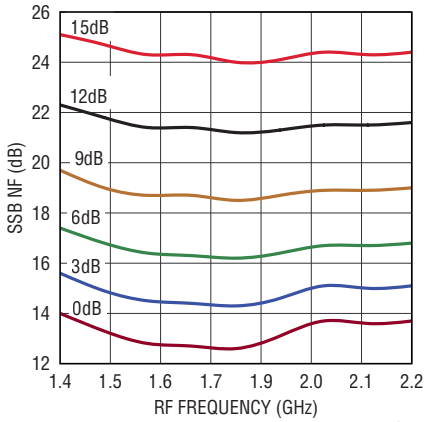
P_{RF} = –6dBm/Tone, Δf = 2MHz, P_{LO} = 0dBm, V_{CC} = 3.3V, V_{DD} = 3.3V, T_C = 25°C, full power mode, unless otherwise noted.

1.5GHz to 2.1GHz RF Input Matching: RF = 1.8GHz, IF = 270MHz, Low Side LO

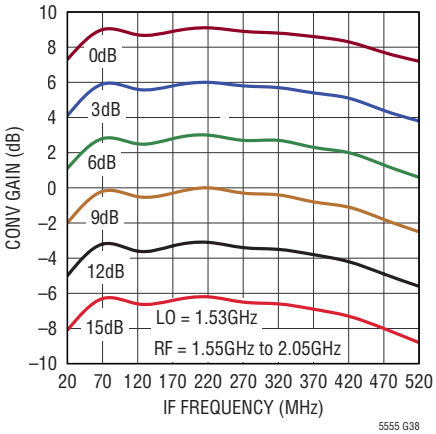
Conv Gain and IIP3 vs RF Frequency and IF Attenuation (3dB Steps)



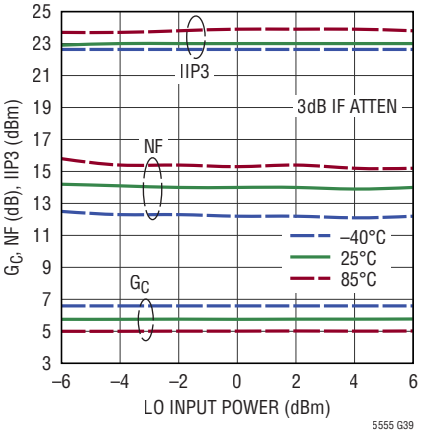
SSB NF vs RF Frequency and IF Attenuation (3dB Steps)



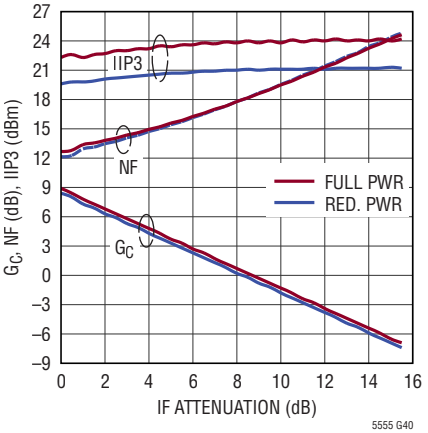
Conv Gain vs IF Frequency and Attenuation, Swept RF/Fixed LO



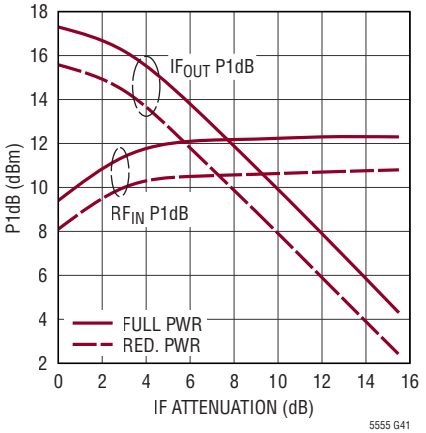
1.8GHz Conv Gain, IIP3 and SSB NF vs LO Power and Case Temperature



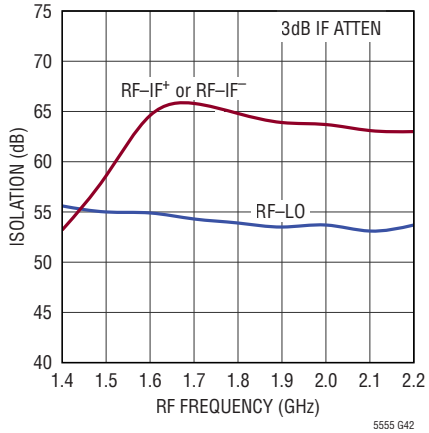
1.8GHz Conv Gain, IIP3 and SSB NF vs IF Attenuation



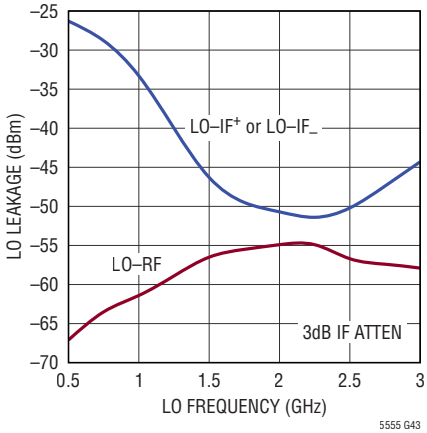
1.8GHz RF Input and IF Output P1dB vs IF Attenuation



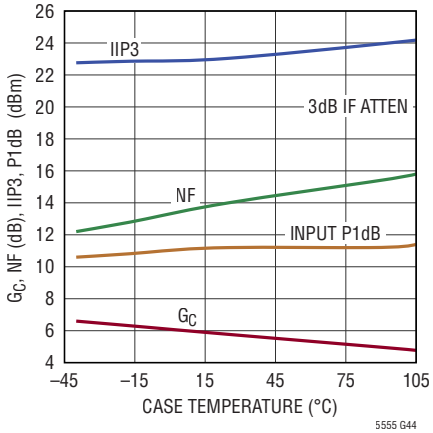
RF Isolation vs RF Frequency



LO Leakage vs LO Frequency



1.8GHz Conv Gain, IIP3, NF and RF Input P1dB vs Temperature



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PIN FUNCTIONS

GND (Pins 1, 8, 14, 15, 16 Exposed Pad Pin 29): Ground. These pins must be soldered to the RF ground plane on the circuit board. The exposed pad provides both electrical ground contact and thermal contact to the printed circuit board.

AI$^-$, AI$^+$ (Pins 2, 3): Differential IF Attenuator Inputs. These pins are internally biased to $V_{CC/2}$ when V_{CC} is applied. Therefore, a series DC-blocking capacitor must be used.

EN (Pin 4): Enable Control Pin. A CMOS logic high will enable the IC. This pin has an internal 330k pull-down resistor, so if unconnected, the IC will be disabled.

V_{CC} (Pin 5): Power Supply Pin. This pin must be connected to a regulated 3.3V supply with a bypass capacitor located close to the pin. Typical DC current consumption is 41mA. The Supply voltage on this pin defines the logic levels for the EN and PS pins.

MO$^+$, MO$^-$ (Pins 6, 7): Mixer Open-Collector Differential IF Outputs. These pins must be connected to V_{CC} through pull-up inductors or transformer windings. Typical DC current is 27mA into each pin.

RF (Pin 9): Single-Ended RF Input. This pin is internally biased to $V_{CC/2}$ when V_{CC} is applied. Therefore, a series DC-blocking capacitor must be used.

CSB (Pin 10): Serial Port Chip Select and Parallel Data Latch. In serial control mode this CMOS input allows serial port communication when driven low and ends the burst when taken back high. In parallel mode, a rising edge on this pin loads the parallel data on pins 17 – 21 into the internal data latch. See the Applications Information section for more details.

CLK (Pin 11): Serial Port Clock. This CMOS input clocks serial port input data on its rising edge. See the Applications Information section for more details. This pin is inactive when PS is high.

SDI (Pin 12): Serial Port Data Input. This CMOS input is used to load serial data into the 8-bit register. See Applications Information section for more details. This pin is inactive when PS is high.

SDO (Pin 13): Serial Port Data Output. This CMOS tri-state output presents data from the serial port during a read communication burst. Optionally, attach a resistor of >200k to GND to prevent a floating output. See the Applications Information section for more details. This pin is inactive when PS is high.

D4, D3, D2, D1, D0 (Pins 17 – 21): Parallel Control Pins for Gain. These CMOS inputs control the IF DVGA gain when the CSB pin transitions from low to high. The gain may also be controlled through the serial port when PS is low. For serial only control, it is recommended that these pins be grounded.

PS (Pin 22): Parallel Select Pin. A CMOS logic high will enable IF DVGA control using the parallel data pins (pins 17 – 21). A CMOS logic low allows the SPI port to control the gain while ignoring the voltages on the parallel data pins. This pin has an internal 330k pull-down resistor.

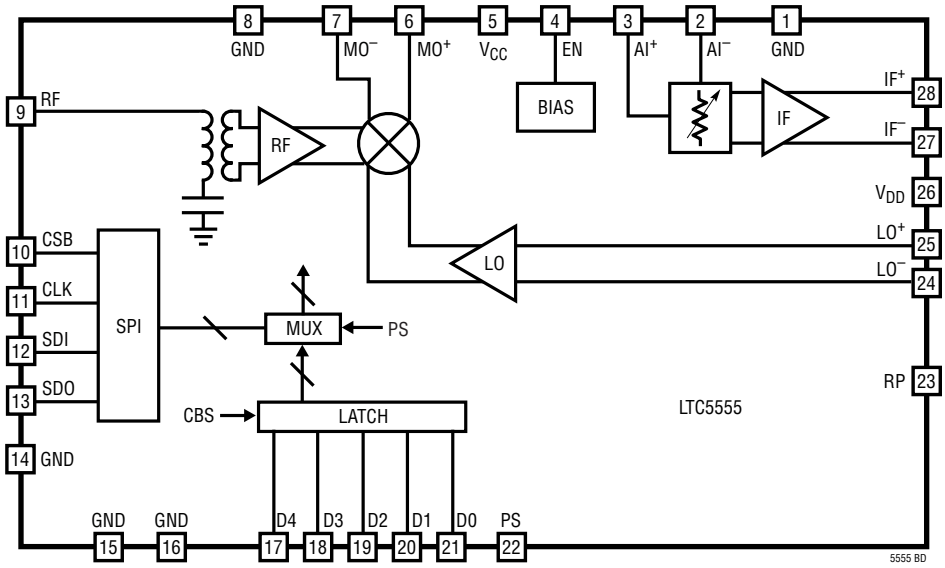
RP (Pin 23): Reduced Power Select Pin. A CMOS logic low on this pin sets the IC to full power mode, unless programmed to reduced power mode by the SPI. A CMOS logic high programs the IC to reduced power mode, independent of the SPI. This pin has an internal 330k pull-down resistor.

LO$^-$, LO$^+$ (Pins 24, 25): Differential Local Oscillator Input. These pins are internally connected to ESD diodes to ground. Therefore, series DC-blocking capacitors must be used if the LO source has a DC voltage present. Single-ended or differential drive may be used. Each pin is internally matched to 50Ω, even when the mixer is disabled.

V_{DD} (Pin 26): Power Supply Pin for SPI and Parallel Interface Logic. This pin must be connected to a regulated 1.8V to 3.3V supply. Typical DC current consumption is less than 1mA with CSB low and the clock running at 10MHz. When idle, typical current consumption is less than 500µA. The Supply voltage on this pin defines the logic levels for the SPI I/O pins (CSB, CLK, SDI, and SDO), the parallel data pins (D0 – D4) and the RP pin.

IF$^-$, IF$^+$ (Pins 27, 28): Open Collector Differential IF Buffer Output. These pins must be connected to V_{CC} through pull-up inductors. Typical DC current is 48mA per pin.

BLOCK DIAGRAM



TEST CIRCUIT

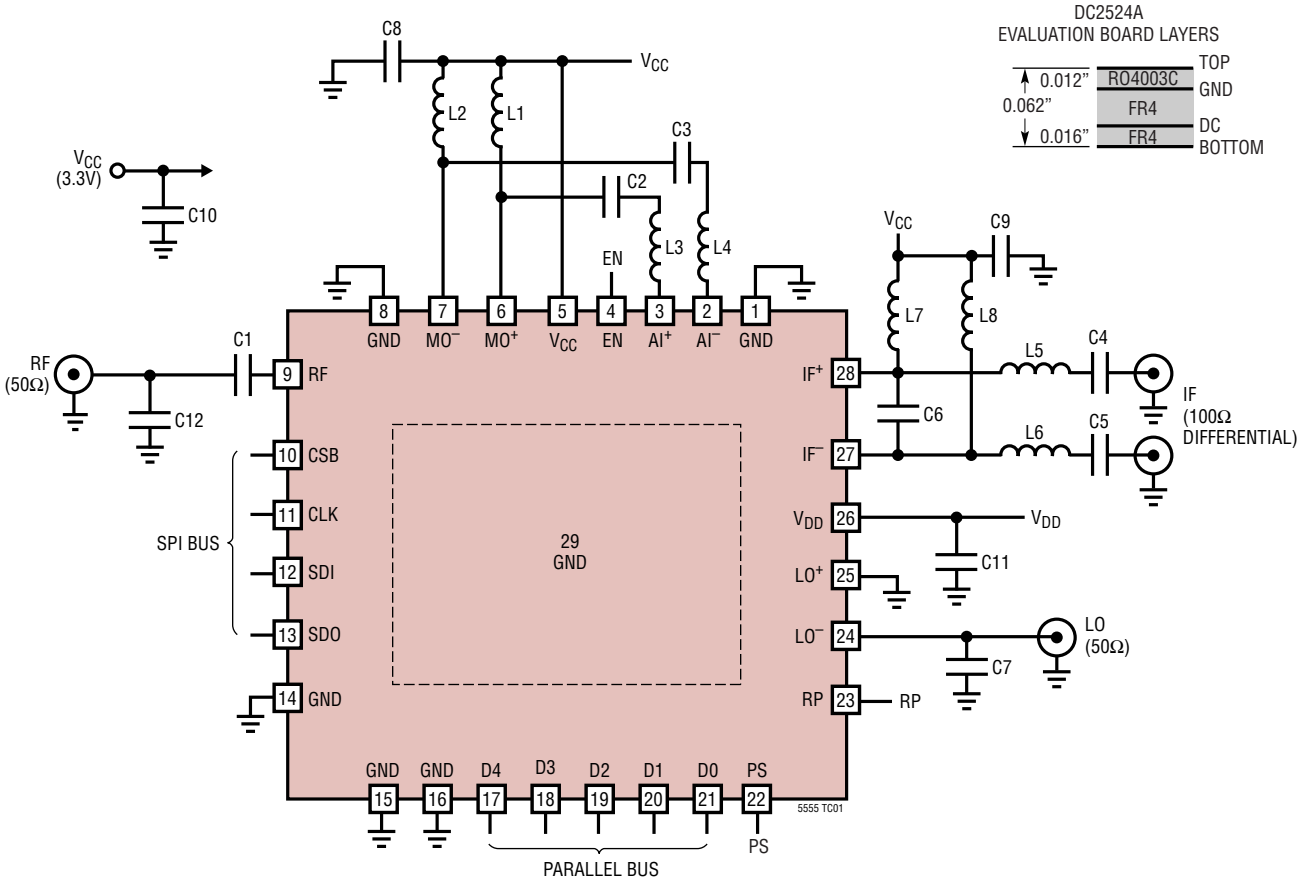


Figure 1. Test Circuit Schematic with 100Ω Matched Differential IF Outputs

RF INPUT MATCHING			
BAND	**RF RANGE (GHz)**	**C1**	**C12**
B1	1.5 to 2.1	6.8pF	1.8pF
B2	2.2 to 3.2	1.8pF	0.4pF
B3	2.6 to 6.4	1.2pF	–
B4	5.6 to 7.2	0.9pF	0.2pF

REF DES	VALUE	SIZE	VENDOR	REF DES	VALUE	SIZE	VENDOR
C1	See Table	0402	Murata 50V NPO	C10, C11	1µF	0603	Murata 50V X5R
C2, C3	1nF	0201	Murata 50V NPO	C12	See Table	0402	Murata 50V NPO
C4, C5, C8, C9	10nF	0402	Murata 50V X7R	L1, L2, L7, L8	680nH	0603	Coilcraft 0603AF
C6	1.2pF	0402	Murata 50V NPO	L3, L4	18nH	0402	Coilcraft 0402HP
C7	0.2pF	0402	Murata 25V NPO	L5, L6	20nH	0402	Coilcraft 0402HP

APPLICATIONS INFORMATION

Introduction

The LTC5555 is an RF-to-IF downconversion mixer with an integrated LO buffer. The IC also includes an IF DVGA (digital variable gain amplifier) consisting of a programmable 15.5dB range digital IF attenuator with 0.5dB steps, and a fixed-gain IF buffer amplifier. The cascaded RF-to-IF conversion gain ranges from 9.2dB at maximum IF gain, to –6.7dB at minimum IF gain. The IF frequency response is flat within 1dB from 30MHz to 450MHz, and may be modified by adjusting the values of the external pull-up inductors.

The IC can be programmed to a reduced power mode via the RP pin, resulting in a 23% power savings, with reduced linearity performance. The test circuit schematic in Figure 1 shows the external components used to characterize the IC. The evaluation board is shown in Figure 2.

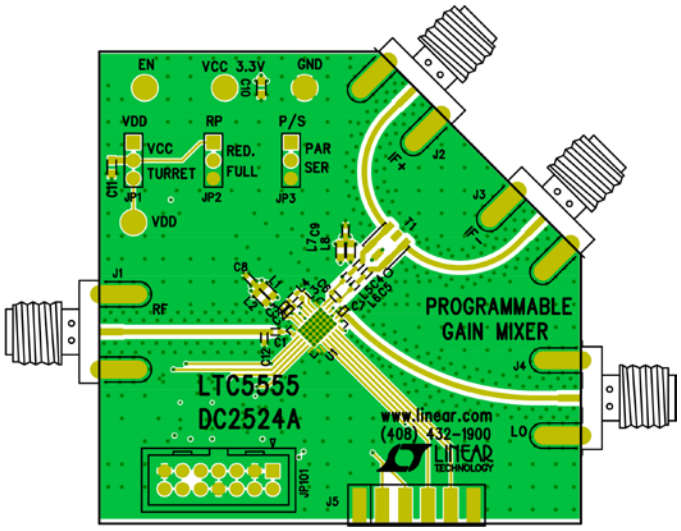


Figure 2. Evaluation Board

RF Inputs

A block diagram of the RF input is shown in Figure 3. The input includes an integrated transformer and a differential RF buffer amplifier. The transformer's primary winding is biased at $V_{CC}/2$ and therefore requires an external DC-blocking capacitor.

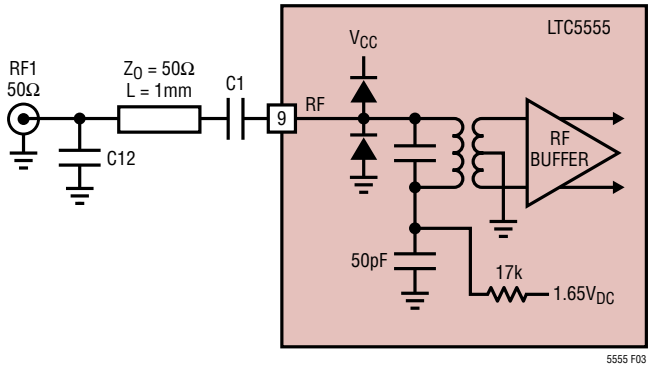


Figure 3. RF Input Block Diagram

The RF inputs are 50Ω matched from 2.6GHz to 6.4GHz, requiring only a 1.2pF series capacitor (C1) for DC-blocking. Shunt reactance C12 is used to tune the inputs down to 1.5GHz, or up to 7GHz. Figure 1 summarizes the external matching component values for all bands. Measured RF input return loss for each band is shown in Figure 4.

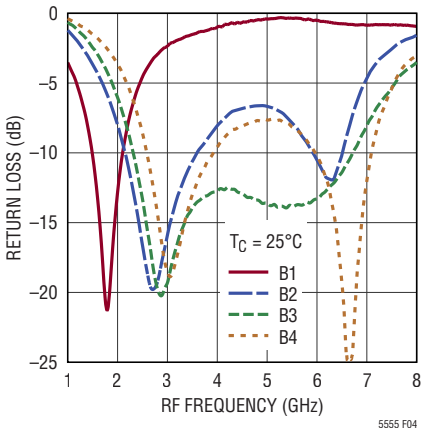


Figure 4. RF Input Return Loss for Each Band

LO Input

A simplified schematic of the LO input is shown in Figure 5. A differential input is provided, although the IC is characterized and production-tested with single-ended drive. Differential LO drive may improve performance slightly. The LO input is internally matched to 50Ω from 500MHz to 5GHz, requiring no external components. Adding shunt capacitor C7(0.2pF), extends the LO input match up to 7GHz. ESD protection diodes on each input

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limit the peak voltage swing to approximately ±700mV (+7dBm), although higher LO drive, up to 10dBm will not damage the input. An external DC-blocking capacitor is only needed if the LO source has DC voltage present. The measured LO input return loss is shown in Figure 6, with and without C7.

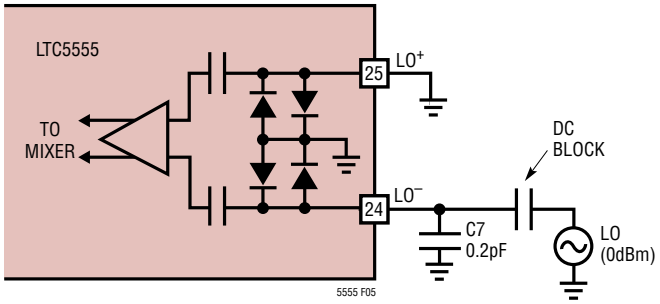

Figure 5. LO Input Schematic

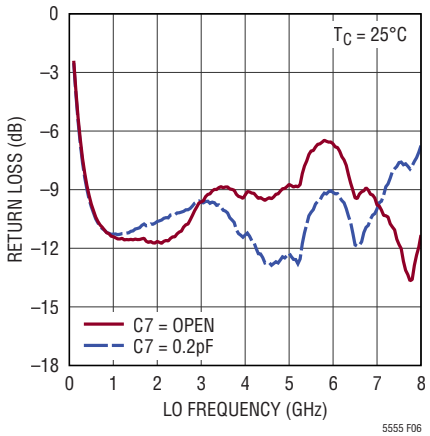

Figure 6. LO Input Return Loss

IF Outputs

A simplified IF output schematic, with external matching components, is shown in Figure 7. The final output stage is differential open-collector with integrated matching resistors, capacitors and ESD protection diodes. Each output pin must be biased at the supply voltage (V_{CC}) using external chokes (L7 and L8). Each pin draws approximately 48mA of DC supply current (96mA total), therefore, inductors with low DC resistance (<1Ω), are required for the highest output IP3 and P1dB.

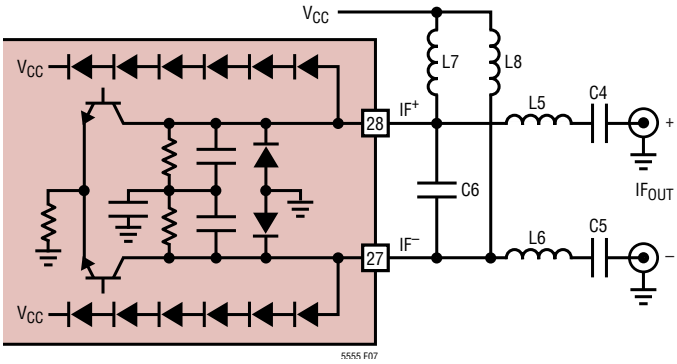

Figure 7. IF Output Schematic

The integrated output resistors set the differential output resistance at 206Ω. C6, L5 and L6 form a 2:1 impedance transformer which transforms the output to 100Ω differential. If a 200Ω output is desired, C6 is not used and the values of L5 and L6 are reduced to the values shown in Table 1. C4 and C5 are DC-blocking capacitors, which may be omitted if the following stage is already DC-blocked.

The standard evaluation board is built with 100Ω differential IF outputs, but also has pads which allow the use of IF transformers to provide 50Ω single-ended outputs. To implement this, it is recommended to use the 200Ω matching shown in Table 1 and 4:1 IF transformers. Figure 17 shows the circuit schematic and measured performance using this approach.

Table 1. IF Output Matching Element Values

DIFFERENTIAL Z_{OUT}	C6	L5, L6	9dB RETURN LOSS BANDWIDTH
200Ω	–	10nH	23MHz to 440MHz
100Ω	3.9pF	47nH	70MHz to 242MHz
	2.2pF	33nH	87MHz to 352MHz
	1.2pF	20nH	115MHz to 495MHz
	0.6pF	16nH	155MHz to 610MHz
	–	12nH	190MHz to 1100MHz

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The differential IF output impedance vs frequency is listed in Table 2. The impedances are at the package pins with no external components. Measured IF output return losses vs frequency for 100Ω differential matching is shown in Figure 8.

Table 2. Differential IF Output Impedance vs Frequency

IF FREQUENCY (MHz)	DIFFERENTIAL IMPEDANCE (R_{IF} || C_{IF})
10	210 || 1.10pF
50	209 || 1.09pF
100	209 || 1.04pF
150	208 || 0.97pF
200	207 || 0.94pF
300	206 || 0.92pF
400	203 || 0.93pF
500	200 || 0.91pF
600	196 || 0.91pF
700	192 || 0.91pF
800	186 || 0.91pF
900	179 || 0.90pF
1000	172 || 0.89pF

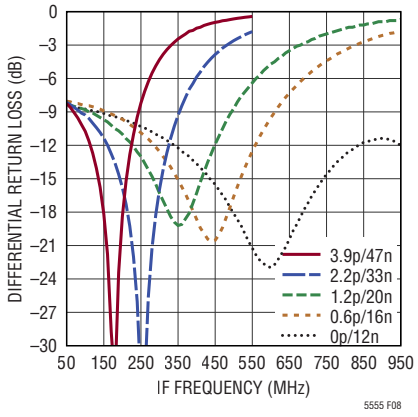

Figure 8. IF Output Return Loss (100Ω Differential Matching)

Mixer Output to IF DVGA Interface

The mixer's 200Ω differential output impedance matches the IF DVGA's 200Ω differential input impedance, even over normal process variation due to the monolithic implementation. This assures minimal and repeatable DNL and INL over the full IF attenuation range. Furthermore, the mixer output and DVGA input include integrated matched capacitors, which simplify the realization of a lowpass filter between the mixer and DVGA. This filter attenuates undesired high frequency mixing products and LO leakage before entering the DVGA.

A simplified schematic of the interface is shown in Figure 9. L3 and L4 connect the mixer output to the DVGA input, while forming a 1GHz 3rd-order, 0.2dB ripple Chebyshev lowpass filter. L1 and L2 supply DC current to the mixer and C2 and C3 are DC-blocking capacitors.

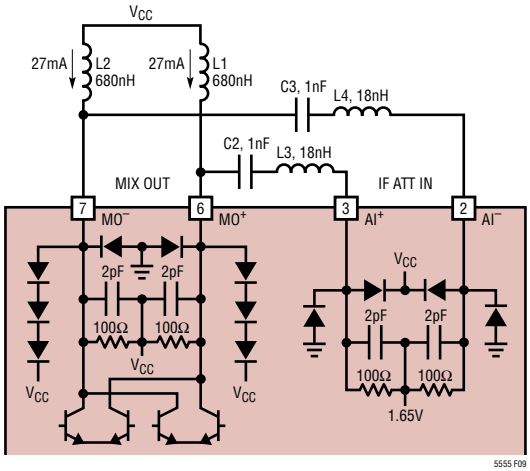

Figure 9. Mixer to IF DVGA Interface

An equivalent AC schematic of the lowpass filter is shown in Figure 10, where the mixer output and DVGA input are modeled as 200Ω in parallel with 1pF. The mixer supply chokes and series DC blocking capacitors are ignored in this schematic.

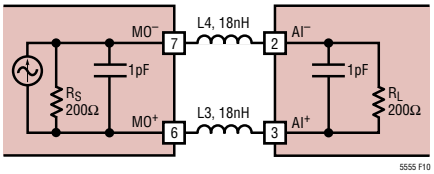

Figure 10. Equivalent Lowpass Filter Schematic

It's also possible to implement a bandpass filter between the mixer and DVGA. An example is shown in Figure 11, where a 3rd-order bandpass filter is realized by changing the values of the reactive components and adding C13, C14 and L9. Figure 20 shows measured conversion gain vs IF output frequency using this bandpass topology.

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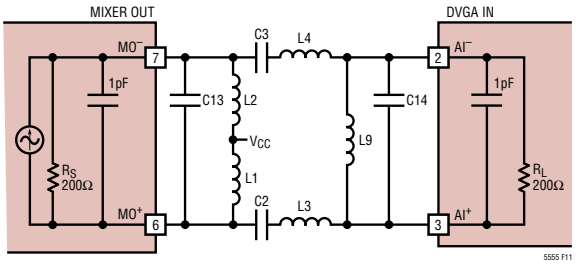

Figure 11. 3rd-Order Bandpass Filter Realization

IF DVGA Phase vs IF Attenuation

Ideally, the phase of the IF output would be constant over the full IF attenuation range. Practically, there is some phase shift due to circuit parasitics in the attenuator. The LTC5555's IF DVGA is optimized for the lowest possible phase variation (or phase error) over the full IF attenuation range. Phase error vs IF attenuation for the complete IF section is listed in Table 3.

Table 3. IF Phase Error vs IF Attenuation

ATT (dB)	250MHz	350MHz	500MHz
0	REF	REF	REF
3	–1.4°	–2.3°	–1.6°
6	–2.5°	–3.5°	–3.3°
9	–3.2°	–4.4°	–4.5°
12	–3.7°	–5.0°	–5.1°
15	–3.6°	–4.7°	–4.5°

Downconverter Performance vs IF Attenuation

RF-IF conversion gain, IIP3, OIP3 and noise figure over the full 15.5dB attenuation range is shown in Figure 12. The same data is listed in Table 4 with the INL and DNL at each attenuator setting.

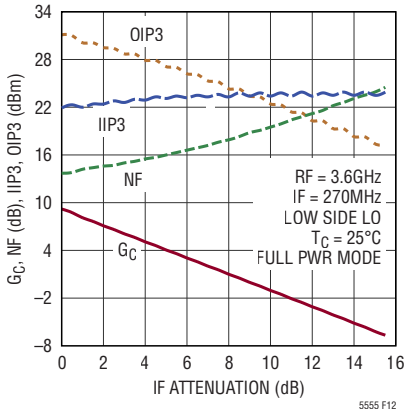

Figure 12. Downconverter RF-IF Conversion Gain, IIP3, OIP3 and Noise Figure vs IF Attenuation.

Table 4. Conversion Gain, IIP3, OIP3 and SSB NF vs IF Attenuation (RF = 3.6GHz, IF = 270MHz, Low Side LO)

A (dB)	IF[4:0]	G_C (dB)	IIP3 (dBm)	OIP3 (dBm)	NF (dB)	DNL (dB)	INL (dB)
0	0	9.20	21.9	31.1	13.8	—	—
0.5	1	8.75	22.3	31.0	13.8	–0.05	–0.05
1.0	2	8.10	22.0	30.1	14.2	0.15	0.10
1.5	3	7.65	22.4	30.1	14.4	–0.05	0.06
2.0	4	7.09	22.4	29.5	14.6	0.06	0.11
2.5	5	6.63	22.8	29.4	14.7	–0.04	0.07
3.0	6	6.08	22.6	28.7	15.1	0.05	0.12
3.5	7	5.63	23.0	28.7	15.2	–0.04	0.08
4.0	8	5.07	22.9	27.9	15.5	0.05	0.13
4.5	9	4.61	23.3	27.9	15.7	–0.04	0.09
5.0	10	4.05	23.1	27.1	16.0	0.06	0.15
5.5	11	3.59	23.4	27.0	16.3	–0.04	0.11
6.0	12	3.04	23.2	26.2	16.6	0.05	0.16
6.5	13	2.57	23.5	26.1	16.9	–0.03	0.13
7.0	14	2.02	23.3	25.3	17.2	0.05	0.18
7.5	15	1.56	23.6	25.2	17.6	–0.03	0.15
8.0	16	1.00	23.3	24.3	17.9	0.05	0.20
8.5	17	0.53	23.8	24.3	18.3	–0.03	0.17
9.0	18	–0.02	23.4	23.4	18.6	0.05	0.22
9.5	19	–0.49	23.8	23.3	19.1	–0.03	0.19
10.0	20	–1.04	23.4	22.4	19.5	0.05	0.24
10.5	21	–1.51	23.8	22.3	19.9	–0.03	0.21
11.0	22	–2.07	23.4	21.4	20.4	0.05	0.27
11.5	23	–2.54	23.9	21.3	20.8	–0.03	0.24
12.0	24	–3.09	23.4	20.3	21.2	0.06	0.30
12.5	25	–3.56	23.8	20.3	21.6	–0.03	0.26
13.0	26	–4.12	23.5	19.3	22.2	0.06	0.32
13.5	27	–4.59	23.9	19.3	22.6	–0.03	0.29
14.0	28	–5.15	23.5	18.3	23.1	0.06	0.36
14.5	29	–5.62	23.9	18.3	23.5	–0.03	0.32
15.0	30	–6.19	23.5	17.4	23.9	0.06	0.39
15.5	31	–6.66	23.9	17.3	24.5	–0.03	0.36

Individual Stage Performance

The LTC5555 is characterized, specified and production-tested as a complete downconverter, from the RF input to the final IF output. For some applications, it may be preferred to insert a higher selectivity IF filter between the mixer and IF DVGA. To help with system performance

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calculations, the nominal performance of the mixer is shown in Table 5 and the IF DVGA performance is listed in Table 6. This information is provided for reference only as these blocks are not production-tested independently.

Table 5. Mixer Power Conversion Gain, IIP3 and SSB NF (RF = 3.6GHz, IF = 270MHz, Low Side LO)

FULL PWR MODE			REDUCED PWR MODE		
G_P (dB)	IIP3 (dBm)	NF (dB)	G_P (dB)	IIP3 (dBm)	NF (dB)
–1	26	13	–1.3	21	11

Table 6. IF DVGA Power Gain, OIP3 and SSB NF (270MHz)

IF ATT (dB)	FULL PWR MODE			REDUCED PWR MODE		
	GAIN (dB)	OIP3 (dBm)	NF (dB)	GAIN (dB)	OIP3 (dBm)	NF (dB)
0	10.2	36.5	6.2	10.0	33.5	6.2
3	7.2	36.5	9.9	7.0	33.2	10.0
6	4.2	36.5	13.0	4.0	33.2	12.9
9	1.2	36.5	15.9	1.0	33.2	15.9
12	–1.8	36.2	18.9	–2.0	33.1	18.9
15	–4.8	36.0	21.9	–5.0	32.7	21.9

Control and Data Pin Interfaces

Figure 13 shows a schematic of the control and data pin interfaces. As shown, all of the pins are protected by ESD diodes. The positive ESD diode for EN is connected to V_{CC} while the positive ESD diodes on the other pins are connected to V_{DD}. If the enable function is not needed, the enable pin can be connected directly to the adjacent V_{CC} pin. The EN, PS and RP pins have 330k pull-down resistors, so if left floating, the pins will be pulled low. The voltage on the enable pin should never exceed V_{CC} by more than 0.3V, otherwise supply current may be sourced through the upper ESD diodes. The other pins should not exceed V_{DD} by 0.3V for the same reason. Voltage should not be applied to the control and data pins before the supply voltages are applied to V_{CC} and V_{DD}. If this occurs, damage to the IC may result.

Supply Voltage Ramping

Fast ramping of the supply can cause a current glitch in the internal ESD protection circuits. Depending on the supply inductance, this could result in a supply voltage transient

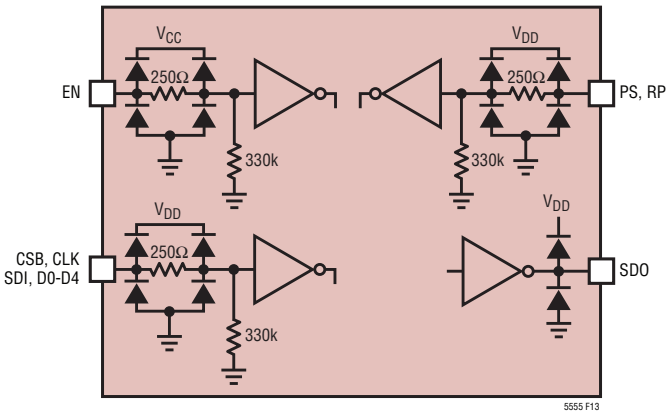

Figure 13. Control and Data Pin Interfaces

that exceeds the maximum rating. A supply voltage ramp time greater than 1ms is recommended.

Supply voltage for V_{CC} (Pin 5) and the IF amplifier (Pins 27 and 28) are connected on the evaluation board, which assures that they all ramp up and down at the same rate. If they are powered independently in the final application circuit, care must be taken to assure that the IF amplifier supply pins go high before the V_{CC} pin and go low after the V_{CC} pin.

SPI DESCRIPTION

IF DVGA attenuator control and power mode may be programmed through the 3-wire SPI consisting of CSB, CLK and SDI. A fourth pin, SDO, is a serial output available to read out the contents of the registers. The SDO pin may also be used to daisy-chain multiple SPI interfaces on a single bus. For example, in a 4-channel receiver application, all four LTC5555 down converters can be programmed with a single, 32-bit load, while sharing a common CSB line.

A block diagram of the SPI is shown in Figure 14. As shown, it is an 8-bit double-buffered FIFO slave architecture. Logic levels for the digital inputs and SDO output are 1.8V to 3.3V CMOS compatible, determined by the supply voltage on the V_{DD} pin. An internal POR (power-on-reset) connected to the V_{DD} pin, resets all 8-bits to logic 0 at power-up, or when V_{DD} drops below 0.5V and then rises back above 1.2V. The POR requires approximately 100µs to reset the registers.

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SPI PROGRAMMING

Data transfers to the part are accomplished by first taking CSB low to enable the port. Then, serial input data on SDI is captured on the rising edge of CLK and shifted into an 8-bit shift register, MSB first. Serial data from the registers is driven out to SDO on the clock's falling edge. The communication burst is terminated by taking CSB high. The rising edge on CSB will then latch the shift-register's contents into an 8-bit buffer D-latch. The buffer latch prevents the downconverter's gain and power mode from changing while data is loaded. See Figure 15 for timing details.

When CSB is high, the clock and data inputs are internally gated off, minimizing current consumption when not selected, and the SDO output is high impedance. However, it is recommended that the serial interface signals should remain idle between data transfers to avoid digital noise coupling into the RF signal paths.

A memory map of the register contents is shown in Table 7, with detailed bit descriptions in Table 8. Each bit's default power-up value is also shown in Table 8, which is:

- 0dB IF attenuation (maximum gain)
- Full power mode

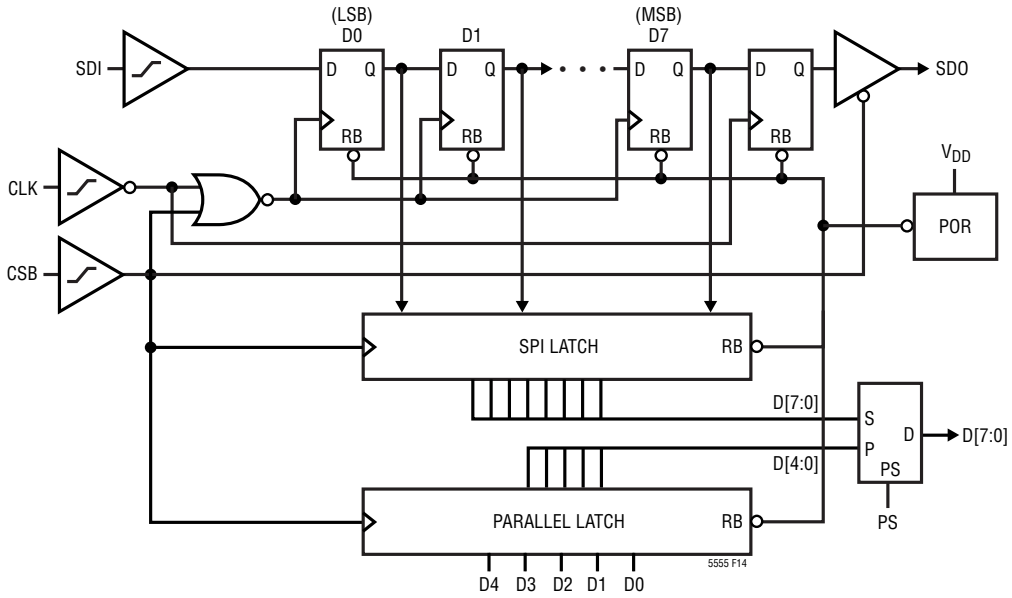

Figure 14. SPI Block Diagram

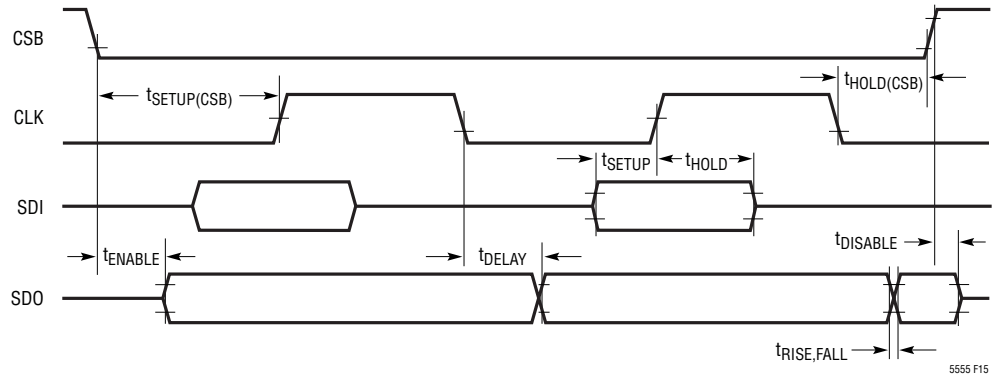

Figure 15. SPI Timing Diagram

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Table 7. Serial Port Register Contents

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
RP	X	X	IF[4]	IF[3]	IF[2]	IF[1]	IF[0]

Table 8. Serial Port Register Bit Field Summary

BITS	DESCRIPTION	DEFAULT
X	Not Used	Don't Care
IF[4:0]	IF Attenuator Control	00000 (Max Gain)
RP	Reduced Power	0 (Full Power)

PARALLEL PROGRAMMING MODE

The IF gain can be programmed directly using the parallel input pins (pins 17 – 21) when the Parallel Select pin (PS) is set high. (See the Pin Functions section for descriptions of the parallel data input pins.) As illustrated in Figure 14, the parallel data input pins are connected to an internal data latch and the CSB pin functions as the latch enable. When the CSB input transitions from logic low to high, the data present at pins 17 – 21 are latched in and take effect. See Figure 16 for timing details.

Logic levels for the parallel data inputs are 1.8V to 3.6V CMOS compatible, as determined by the supply voltage on the V_{DD} pin. An internal POR (power-on-reset) connected to the V_{DD} pin, resets the internal latch outputs to logic 0 at power-up, or when V_{DD} drops below 0.5V and then rises back above 1.2V. The POR requires approximately 100µs to reset the parallel data latch.

Spurious Output Levels

Spurious output levels vs harmonics of the RF and LO are tabulated in Table 9. The spur levels were measured using the test circuit shown in Figure 1, with an RF input power of –6dBm and 6dB of IF attenuation. Table 9(a) shows the relative spur levels in full power mode and Table 9(b) shows the relative spur levels in reduced power mode. The mixer spur levels are insensitive to the IF attenuation setting.

The spur frequencies can be calculated using the following equation:

$$f_{SPUR} = (M \bullet f_{RF}) - (N \bullet f_{LO})$$

Table 9. IF Output Spur Levels (dBc).
(RF = 3.6GHz, P_{RF} = –6dBm, IF = 270MHz, Low Side LO, P_{LO} = 0dBm, 3dB IF Attenuation, T_C = 25°C)

(a). Full Power Mode

		N					
		0	1	2	3	4	5
M	0		–54	*	*	*	*
	1	–72	0	–75	*	*	*
	2	*	*	–76	*	*	*
	3	*	*	*	–72	*	*
	4	*	*	*	*	*	*
	5	*	*	*	*	*	*

*Less than –85dBc

(b). Reduced Power Mode

		N					
		0	1	2	3	4	5
M	0		–54	*	*	*	*
	1	–71	0	–76	*	*	*
	2	*	*	–71	*	*	*
	3	*	*	*	–68	*	*
	4	*	*	*	*	*	*
	5	*	*	*	*	*	*

*Less than –85dBc

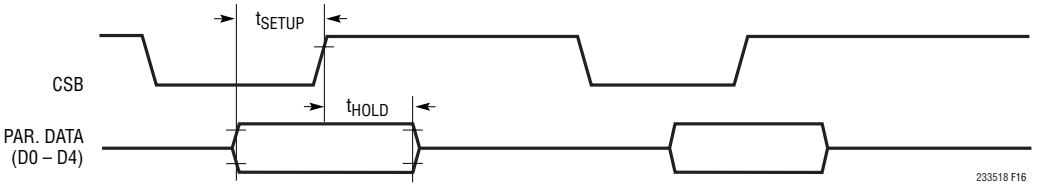

Figure 16. Parallel Timing Diagram

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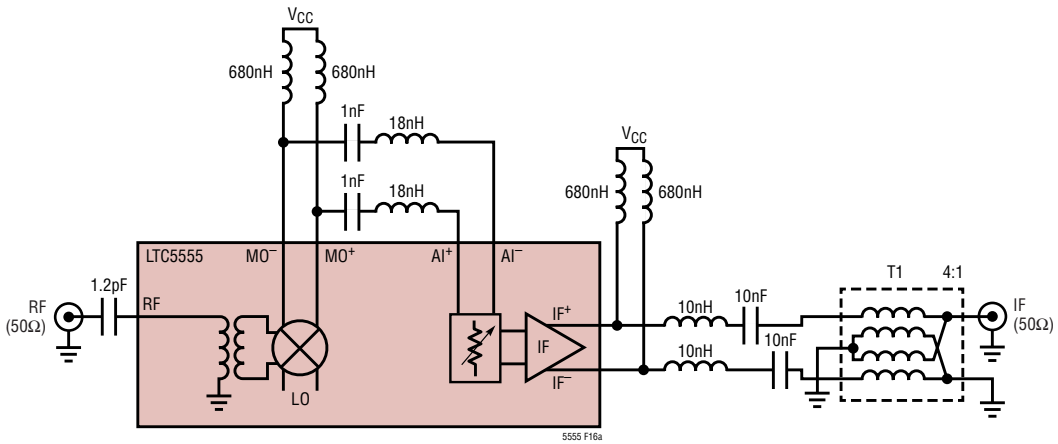
Single-Ended IF Outputs Using a Balun

The LTC5555 evaluation board has differential IF outputs, but can be modified for single-ended operation by inserting a 4:1 balun, as shown in Figure 17. The 10nH series inductors at the differential IF output compensate for the IF amplifier's output capacitance, producing a 200Ω differential output up to approximately 500MHz. The 4:1 balun then converts the 200Ω differential output to 50Ω single-ended. For applications with IF frequency less than 250MHz, the series 10nH inductors are not needed.

Figure 17 shows the measured conversion gain vs IF output frequency, using a Mini-Circuits TCM4-19+ balun. The RF input was swept from 3.35GHz to 3.85GHz using a fixed 3.33GHz LO, producing an IF output ranging from 20MHz to 520MHz. Measured conversion gain for the standard 100Ω differential output matching is also shown on the same graph for comparison, highlighting the insertion loss of the balun.



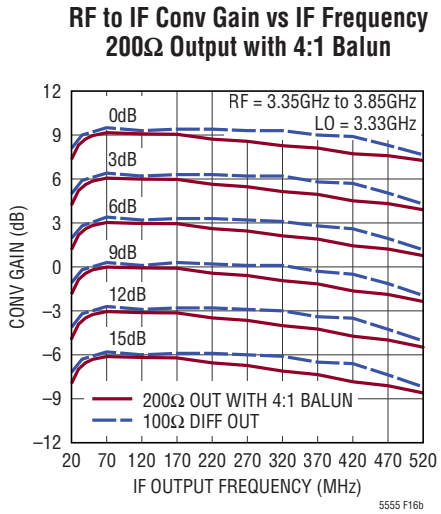


Figure 17. Test Circuit and Measured Conversion Gain Using 200Ω Output Matching with a 4:1 IF Transformer to Realize a 50Ω Single-Ended IF Output

TYPICAL APPLICATIONS

5.6GHz to 7.2GHz RF Application with Wideband IF

The LTC5555's RF inputs are optimized for operation up to 6GHz, but may be used up to 8GHz with degraded performance. Figure 18 shows an example where the RF input is matched from 5.6GHz to 7.2GHz and the IF output is matched for wideband operation up to 800MHz. The measured performance is summarized in Figure 19, where the RF input is swept from 6.1GHz to 6.9GHz, with a fixed 6.03GHz LO, resulting in a wideband 70MHz to 870MHz IF output, centered at 470MHz.

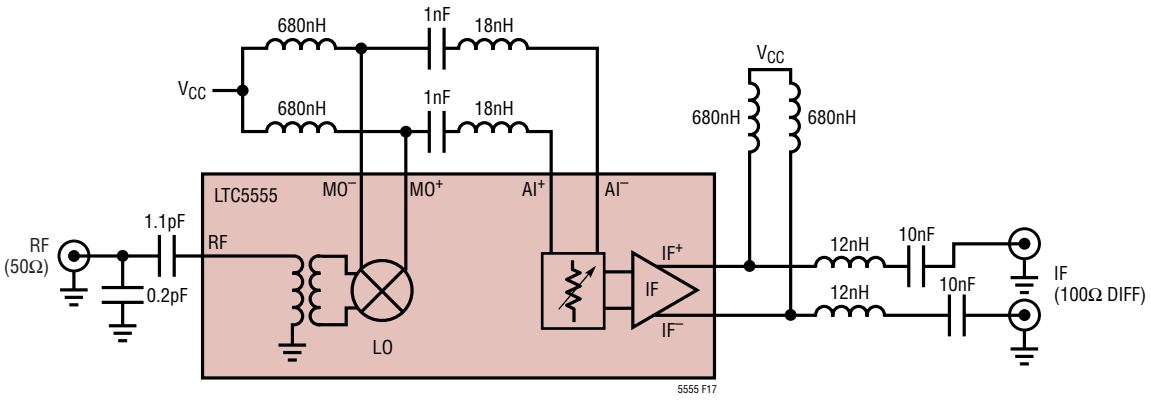


Figure 18. 5.6GHz to 7.2GHz Input Matching with Wideband IF Output Match

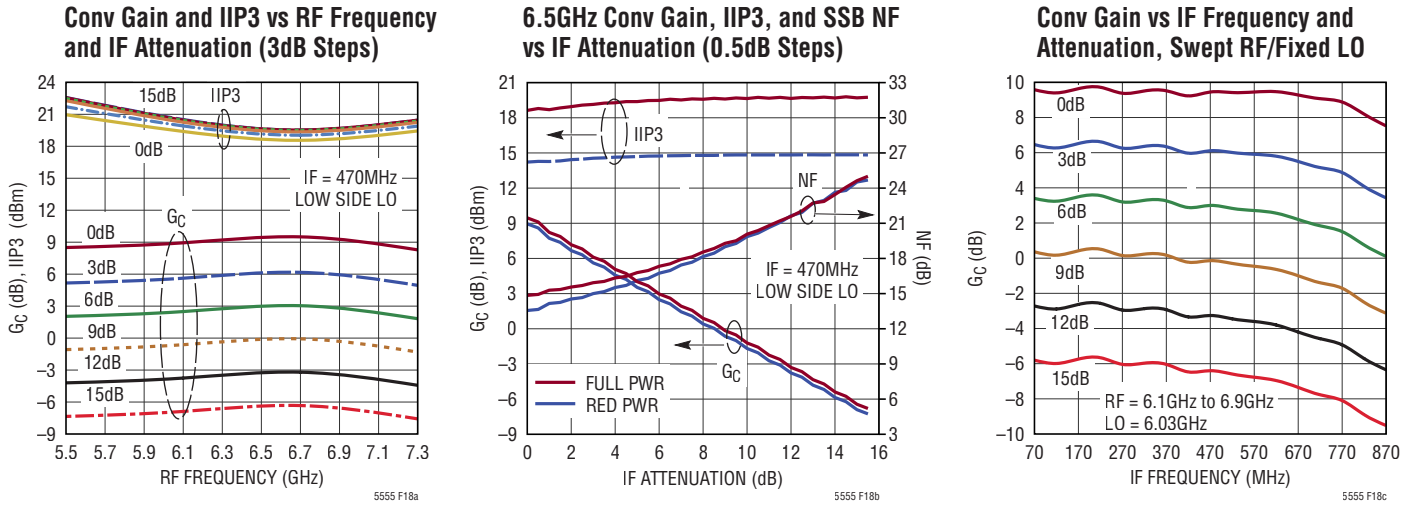
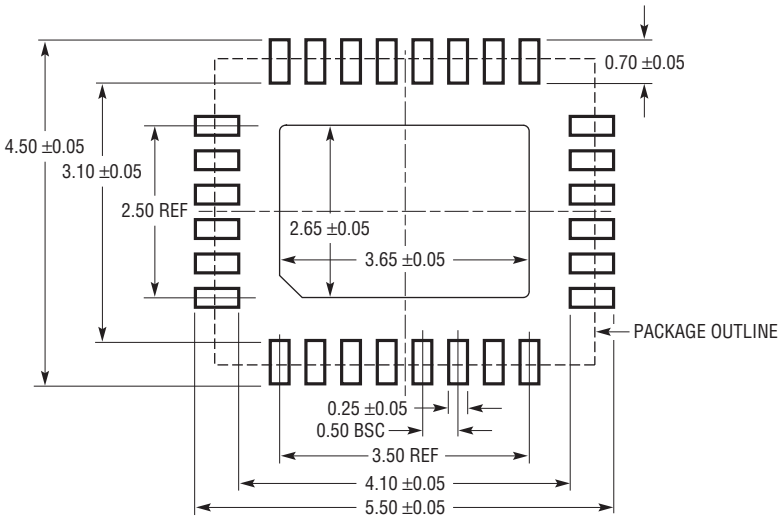


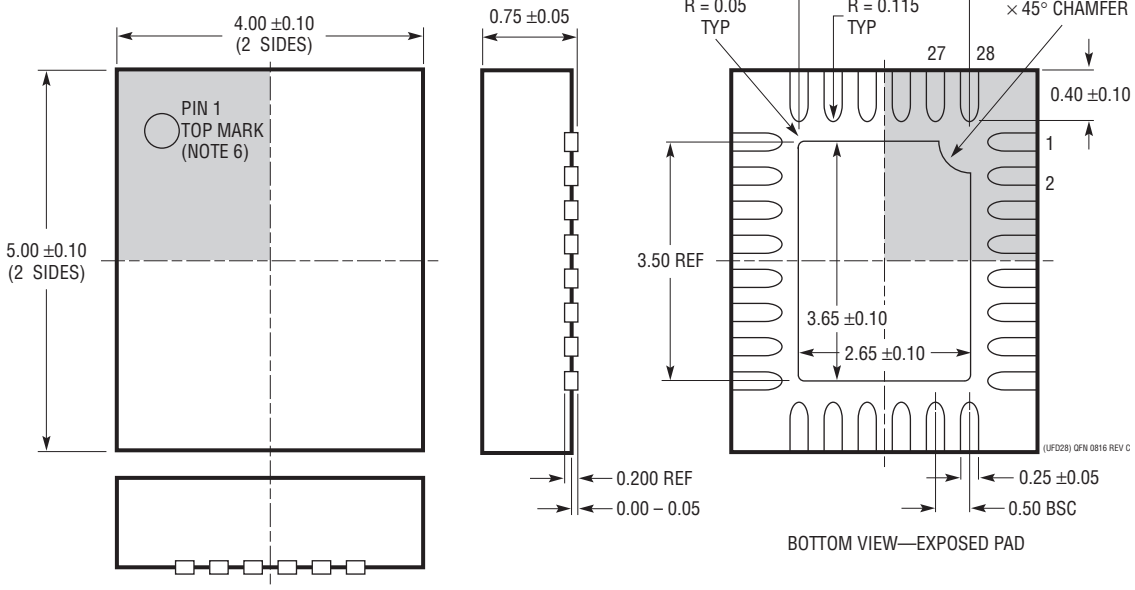
Figure 19. Measured Performance for 5.6GHz to 7.2GHz Downconverter with Wideband IF Output

PACKAGE DESCRIPTION

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE