Single Port PoE/PoE+/ LTPoE++ PSE Controller

FEATURES

- **Compliant with IEEE 802.3at Type 1 and 2**
- **Supports LTPoE++® Up to 90W**
- **Supports Dual-Signature PDs**
- **Fully Autonomous Operation without Microcontroller**
- **Very Low Power Dissipation**
  - **0.1Ω Sense Resistance**
  - **Low $R_{DS(ON)}$ External MOSFET**
- **Very High Reliability 4-Point PD Detection**
  - **2-Point Forced Voltage and Forced Current**
- Robust Short-Circuit Protection
- Cable Surge Protected ±80V OUT Pin
- Classification Dependent I_{CUT} and I_{LIM} Current Thresholds
- Supports 2-Pair and 4-Pair Output Power
- UltraPWR Mode Supports Custom PDs Up to 123W
- Pin-Selectable Detection Backoff Timer for Midspans
- Pin Programmable Legacy PD Detection
- Pin Programmable Maximum Power Mode
- Status LED Pin
- Available in 20-Pin QFN and 16-Pin SO Packages

APPLICATIONS

- PoE PSE Endpoints (Switch/Router)
- PoE Midspan Power Injectors
- Power Forwarders
- Femto Cells
- Security Systems

DESCRIPTION

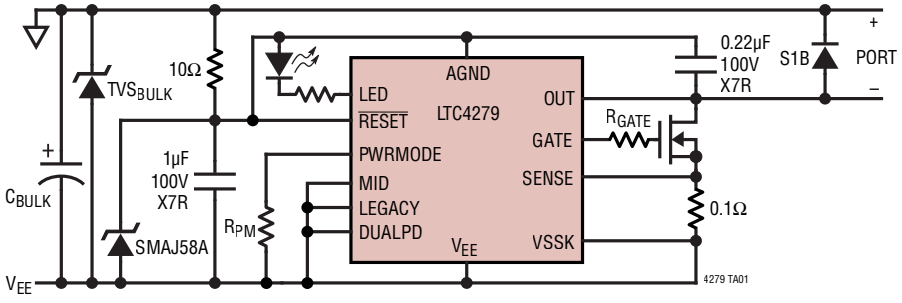
The LTC®4279 is an autonomous single port power sourcing equipment (PSE) controller designed for use in IEEE 802.3at Type 1, Type 2 and LTPoE++ compliant Power over Ethernet (PoE) systems. The LTC4279 provides fully autonomous IEEE 802.3 and LTPoE++ compliant operation without a microcontroller. The LTC4279 simplifies PSE implementation, requiring only a single supply and a small number of passive support components.

The LTC4279 delivers lowest-in-industry heat dissipation by utilizing a low-$R_{DS(ON)}$ external MOSFET and a 0.1Ω sense resistor, eliminating the need for expensive heat sinks and increasing efficiency.

PD discovery uses a proprietary dual-mode 4-point detection mechanism ensuring excellent immunity from false PD detection. Midspan PSEs are supported with physical layer classification and a 2.5 second backoff timer.

Legacy and custom PDs are supported with pin-selectable LEGACY and UltraPWR modes. LEGACY mode detects and powers pre-IEEE specification PDs. UltraPWR mode aggressively turns on and powers custom PDs requiring high inrush and/or operational currents.

TYPICAL APPLICATION



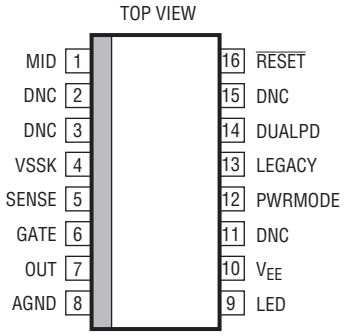
MAXIMUM PD INPUT POWER	R_{PM} (±1%)
Type 1 (13W)	2.37k
Type 2 (25.5W)	3.32k
LTPoE++ 38.7W	4.64k
LTPoE++ 52.7W	5.90k
LTPoE++ 70W	7.87k
LTPoE++ 90W	10.0k
UltraPWR – (Up to 123W*)	13.0k

*Depending on V_{PSE}

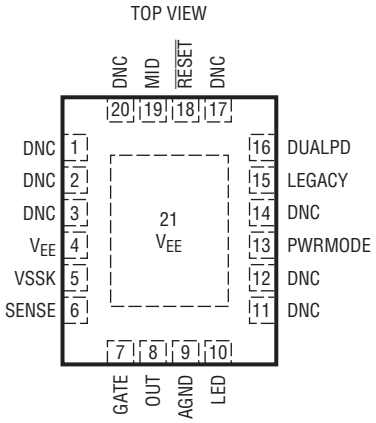
ABSOLUTE MAXIMUM RATINGS (Notes 1 and 4)

Supply Voltages
AGND – V_{EE} ..... –0.3V to 80V
VSSK ..... V_{EE} – 0.3V to V_{EE} + 0.3V
LEGACY, MID, DUALPD, LED,
$\overline{RESET}$, GATE, PWRMODE..... V_{EE} – 0.3V to V_{EE} + 80V
OUT..... V_{EE} – 80V to V_{EE} + 80V
SENSE..... V_{EE} – 20V to V_{EE} + 80V
Operating Ambient Temperature Range
LTC4279I ..... –40°C to 85°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PIN CONFIGURATION



S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 125°C, θ_{JA} = 80°C/W, θ_{JC} = 30°C/W



UFD PACKAGE
20-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 21) IS V_{EE}

ORDER INFORMATION http://www.linear.com/product/LTC4279#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4279IUFD#PBF	LTC4279IUFD#TRPBF	4279	20-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LTC4279IS#PBF	LTC4279IS#TRPBF	LTC4279S	16-Lead Plastic SO	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3 and 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{EE}	Main PoE Supply Voltage	AGND – V_{EE}					
		For IEEE Type 1 Compliant Output	●	45		57	V
		For IEEE Type 2, DUALPD, LTPoE++ 38.7W and LTPoE++ 52.7W Compliant Output	●	51		57	V
		For LTPoE++ 70W and LTPoE++ 90W Compliant Output	●	54.75		57	V
		For UltraPWR Output	●	51		65	V
V_{UVLO_VEE}	Undervoltage Lockout	AGND – V_{EE}	●	20	25	30	V
I_{EE}	V_{EE} Supply Current	AGND – V_{EE} = 55V			–1.7		mA
R_{EE}	V_{EE} Supply Resistance	V_{EE} < V_{UVLO_VEE}	●			12	kΩ
Detection							
	Detection Current – Forced Current	First Point, AGND – V_{OUT} = 10V	●	220	240	260	µA
		Second Point, AGND – V_{OUT} = 3.5V	●	143	160	180	µA
	Detection Voltage – Forced Voltage	AGND – V_{OUT}, 5µA ≤ I_{OUT} ≤ 500µA					
		First Point	●	7	8	9	V
		Second Point	●	3	4	5	V
	Detection Current Compliance	AGND – V_{OUT} = 0V	●		0.8	0.9	mA
V_{OC}	Detection Voltage Compliance	AGND – V_{OUT}, Open Port	●		10.4	12	V
	Detection Voltage Slew Rate	AGND – V_{OUT}, C_{PORT} = 0.15µF (Note 6)	●			0.01	V/µs
	Min. Valid Signature Resistance		●	15.5	17	18.5	kΩ
	Max. Valid Signature Resistance		●	27.5	29.7	32	kΩ
Classification							
V_{CLASS}	Classification Voltage	AGND – V_{OUT}, 0mV ≤ V_{SENSE} ≤ 8.8mV	●	16		20.5	V
	Classification Current Compliance	SENSE – VSSK, V_{OUT} = AGND	●	8.8	9.4	10	mV
V_{MARK}	Mark State Voltage	AGND – V_{OUT}, 0.1mV ≤ V_{SENSE} ≤ 0.5mV	●	7.5		10	V
	Mark State Current Compliance	SENSE – VSSK, V_{OUT} = AGND	●	8.8	9.4	10	mV
	Classification Threshold Voltage	SENSE – VSSK					
		Class 0 to 1	●	0.5	0.65	0.8	mV
		Class 1 to 2	●	1.3	1.45	1.6	mV
		Class 2 to 3	●	2.1	2.3	2.5	mV
		Class 3 to 4	●	3.1	3.3	3.5	mV
		Class 4 to Overcurrent	●	4.5	4.8	5.1	mV
Gate Driver							
	GATE Pin Pull-Down Current	Port Off, V_{GATE} = V_{EE} + 5V	●	0.4			mA
		Port Off, V_{GATE} = V_{EE} + 1V	●	0.08	0.12		mA
	GATE Pin Fast Pull-Down Current	V_{GATE} = V_{EE} + 5V			30		mA
	GATE Pin On Voltage	V_{GATE} – V_{EE}, I_{GATE} = 1µA	●	8		14	V
Output Voltage Sense							
	Power Good Threshold Voltage	V_{OUT} – V_{EE}	●	2	2.4	2.8	V
	OUT Pin Pull-Up Resistance to AGND	0V ≤ (AGND – V_{OUT}) ≤ 5V	●	300	500	700	kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3 and 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Sense							
V_{CUT}	Overcurrent Sense	SENSE – VSSK					
		Class 0, Class 3	●	35.6	37.5	39.6	mV
		Class 1	●	10.0	11.2	12.0	mV
		Class 2	●	19.6	20.8	22.0	mV
		Class 4	●	60.8	63.6	67.2	mV
		LTPoE++ 38.7W	●	89.0	91.9	95.0	mV
		LTPoE++ 52.7W, Dual-Signature PD	●	130	135	140	mV
		LTPoE++ 70W	●	160	165	170	mV
		LTPoE++ 90W	●	225	232	240	mV
V_{LIM}	Active Current Limit	SENSE – VSSK, $V_{EE} \le$ OUT $\le V_{EE}$ + 10V					
		Class 0 to 3	●	40.8	42.5	44.2	mV
		Class 4	●	81.6	85.0	88.4	mV
		LTPoE++ 38.7W	●	120	127	135	mV
		LTPoE++ 52.7W, Dual-Signature PD	●	140	148	160	mV
		LTPoE++ 70W	●	180	191	200	mV
		LTPoE++ 90W	●	240	255	270	mV
		UltraPWR	●	280	295	310	mV
	Inrush Active Current Limit	SENSE – VSSK, $V_{EE} \le$ OUT $\le$ AGND – 29V,					
		Class 0 to 4, LTPoE++	●	40.8	42.5	44.2	mV
		Dual-Signature PD	●	81.6	85.0	88.4	mV
		UltraPWR	●	140	148	160	mV
V_{MIN}	DC Disconnect Sense Voltage	SENSE – VSSK (Note 10)	●	0.5	0.75	1	mV
V_{SC}	Short-Circuit Sense	SENSE – VSSK – V_{LIM}	●	30	60	90	mV
Digital Interface							
	Digital Input Low Voltage	MID, LEGACY, DUALPD, $\overline{\text{RESET}}$ (Note 9)	●			0.8	V
	Digital Input High Voltage	MID, LEGACY, DUALPD, $\overline{\text{RESET}}$ (Note 9)	●	2.1			V
	Internal Pull-Down to V_{EE}	MID, LEGACY, DUALPD			10		µA
	Internal Pull-Up to V_{ROC}	$\overline{\text{RESET}}$			–10		µA
V_{ROC}	Input Open Circuit Voltage	$\overline{\text{RESET}}$ (Note 9)			3.6		V
LED Pin							
	Output Low	$V_{LED} – V_{EE}$, I_{LED} = 1mA	●			0.4	V
	LED Pin Current Limit		●	10			mA
PSE Timing Characteristics							
t_{DET}	Detection Time	Beginning to End of Detection (Note 6)	●	380	410	440	ms
t_{CLE1}	Class Event Duration, Single Class Event	(Note 6)	●	12	15	18	ms
t_{CLE}	Class Event Duration	(Note 6)	●	9.6	12	14.4	ms
t_{CLEON}	Class Event Turn-On Duration	C_{PORT} = 0.6µF (Note 6)	●			0.1	ms
t_{ME}	Mark Event Duration	(Note 6, Note 8)	●	6.8	8.6	10.8	ms
t_{MEL}	Last Mark Event Duration	(Note 6, Note 8)	●	16	20	24	ms
t_{PON}	Power-On Delay	From End of Valid Detect to Application of Power to Port (Note 6)	●			82	ms
	Turn-On Rise Time	(AGND – V_{OUT}): 10% to 90% of (AGND – V_{EE}), C_{PORT} = 0.15µF (Note 6)	●	15	24		µs
	Turn-On Ramp Rate	C_{PORT} = 0.15µF (Note 6)	●			10	V/µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3 and 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{TOCL}	Turn-On Class Transition	C_{PORT} = 0.15µF (Note 6)	●			0.1	ms
t_{ED}	Fault Delay	From I_{CUT} or I_{LIM} Fault to Next Detect (Note 6)	●	1	1.3		s
	LEGACY Mode Detection Backoff	LEGACY Enabled, R_{PORT} = 150Ω (Note 6)	●	2.7	3	3.3	s
	Midspan Mode Detection Backoff	LEGACY Disabled, MID Enabled, R_{PORT} = 15.5kΩ (Note 6)	●	2.3	2.5	2.7	s
	Power Removal Detection Delay	From Power Removal after t_{DIS} to Next Detect (Note 6)	●	1	1.3	2.5	s
t_{START}	Maximum Current Limit Duration During Port Start-Up	(Note 6)	●	52	59	66	ms
t_{CUT}	Maximum Overcurrent Duration after Port Start-Up	(Note 6)	●	52	59	66	ms
	Maximum Overcurrent Duty Cycle	(Note 6)	●	5.8	6.3	6.7	%
t_{LIM}	Maximum Current Limit Duration after Port Start-Up	LTPoE++ PD, Dual-Signature PD or UltraPWR Mode Enabled (Note 6)	●	10	12	14	ms
		(Legacy or IEEE PD) and UltraPWR Mode Disabled (Note 6)	●	52	59	66	ms
t_{MPS}	Maintain Power Signature (MPS) Pulse Width Sensitivity	Current Pulse Width to Reset Disconnect Timer (Notes 6 and 7)	●	1.6		3.6	ms
t_{DIS}	Maintain Power Signature (MPS) Dropout Time	(Notes 5 and 6)	●	320	350	380	ms
	Minimum Pulse Width for $\overline{RESET}$		●	4.5			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 140°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: All currents into device pins are positive; all currents out of device pins are negative.

Note 4: The LTC4279 operates with a negative supply voltage (with respect to AGND). To avoid confusion, voltages in this data sheet are referred to in terms of absolute magnitude.

Note 5: t_{DIS} is the same as t_{MPDO} defined by IEEE 802.3.

Note 6: Guaranteed by design, not subject to test.

Note 7: The IEEE 802.3at specification allows a PD to present its Maintain Power Signature (MPS) on an intermittent basis without being disconnected. In order to stay powered, the PD must present the MPS for t_{MPS} within any t_{MPDO} time window.

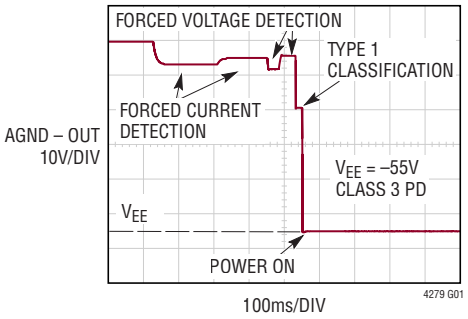
Note 8: Load characteristics of the LTC4279 during Mark: 7V < (AGND – V_{OUT}) < 10V or I_{OUT} < 50µA.

Note 9: The LTC4279 Digital Interface operates with respect to V_{EE}. All logic levels are measured with respect to V_{EE}.

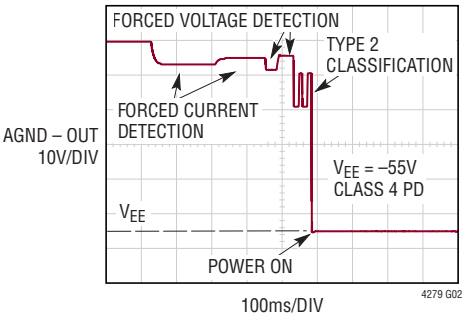
Note 10: See Main PoE Power Supply section for DC disconnect related power supply requirements.

TYPICAL PERFORMANCE CHARACTERISTICS

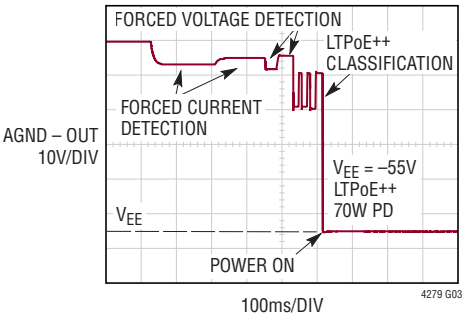
Type 1 Power On Sequence



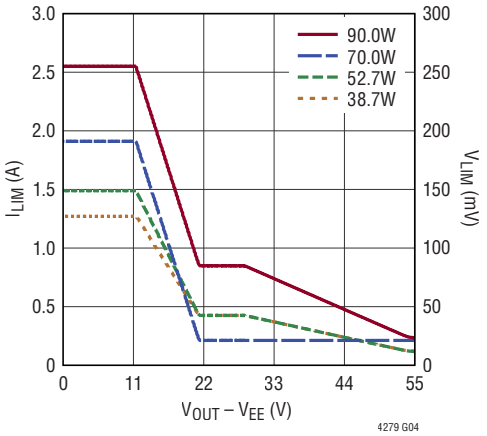
Type 2 Power On Sequence



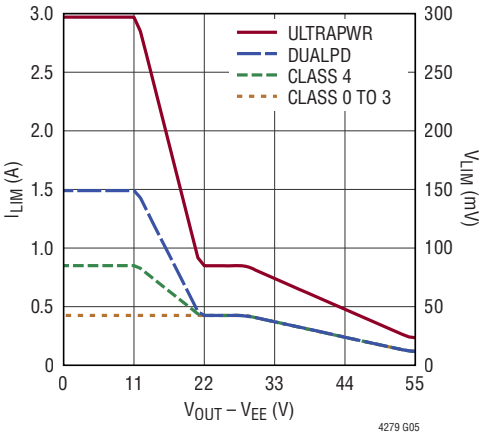
LTPoE++ Power-On Sequence



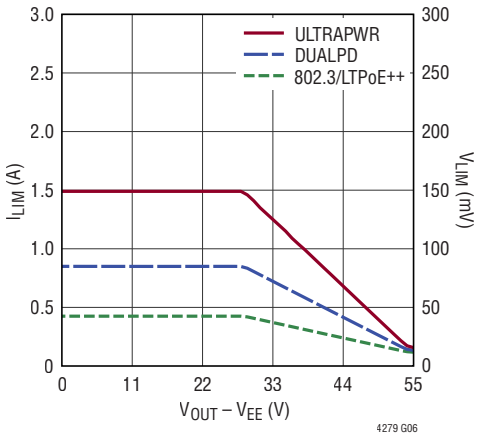
LTPoE++ Current Limits



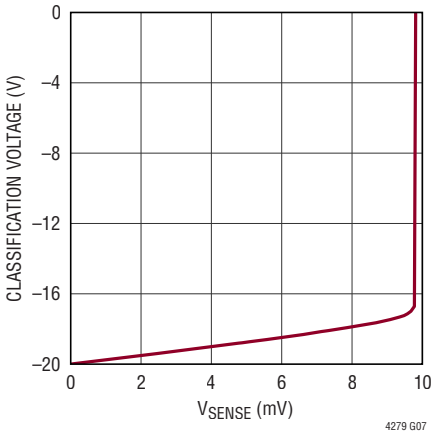
UltraPWR, DUALPD, 802.3 Current Limits



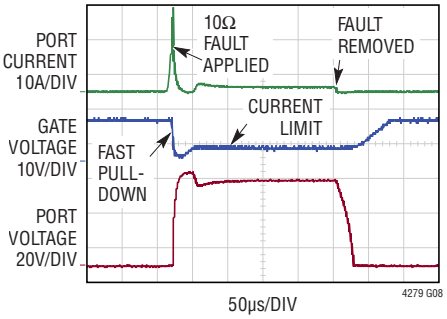
Inrush Current Limits



Classification Current Compliance

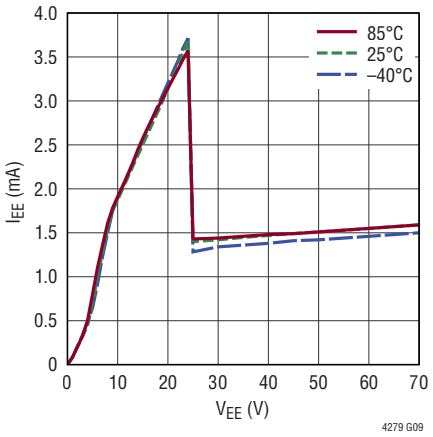


MOSFET Gate Drive with Fast Pull-Down

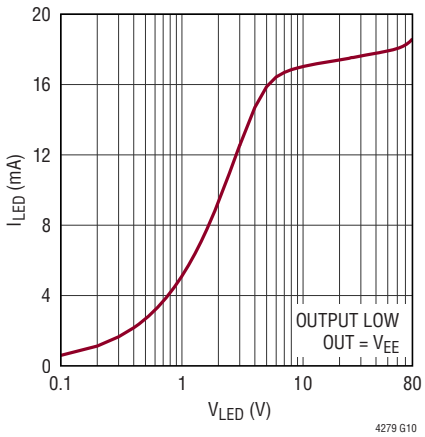


TYPICAL PERFORMANCE CHARACTERISTICS

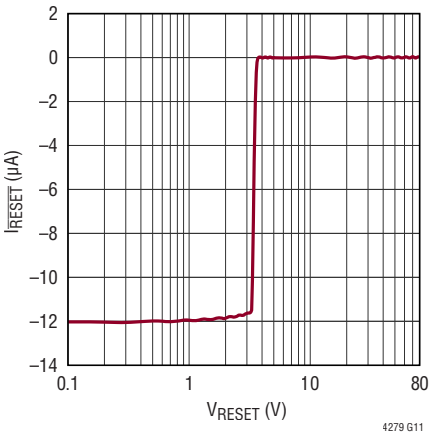
V_{EE} Supply Current vs Voltage



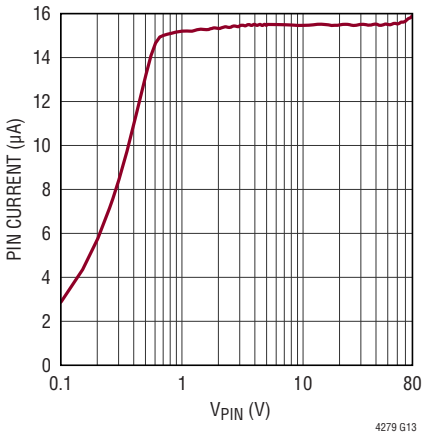
LED Current vs Voltage



$\overline{RESET}$ Current vs Voltage



DUALPD, MID and LEGACY Current vs Voltage



TEST TIMING DIAGRAMS

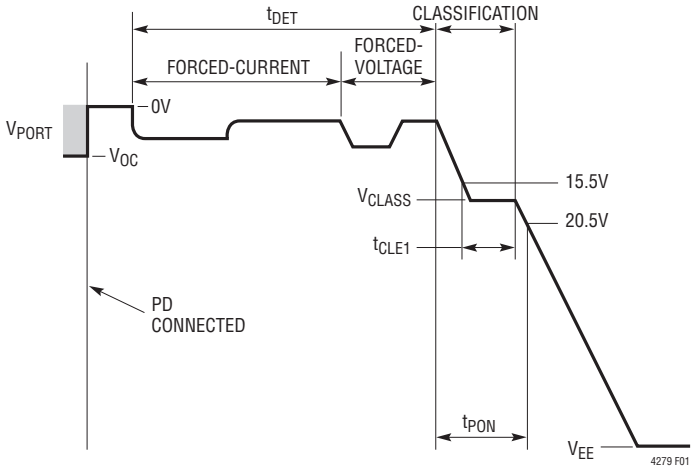


Figure 1. Detect, Single Event Class and Turn-On Timing

TEST TIMING DIAGRAMS

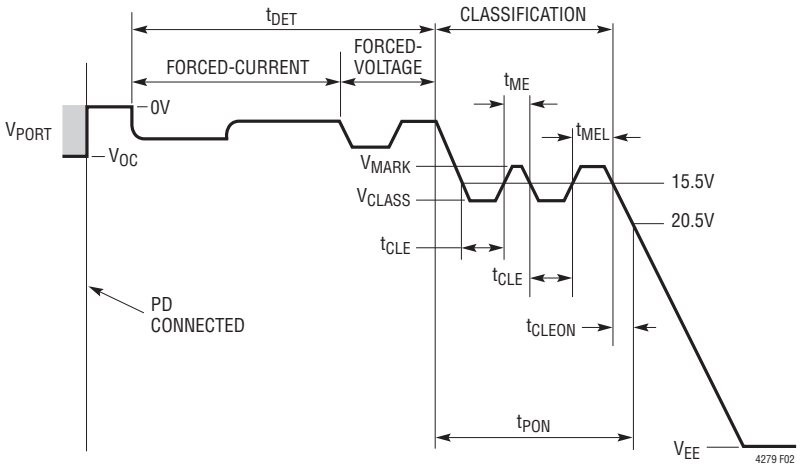


Figure 2. Detect, Two Event Class and Turn-On Timing

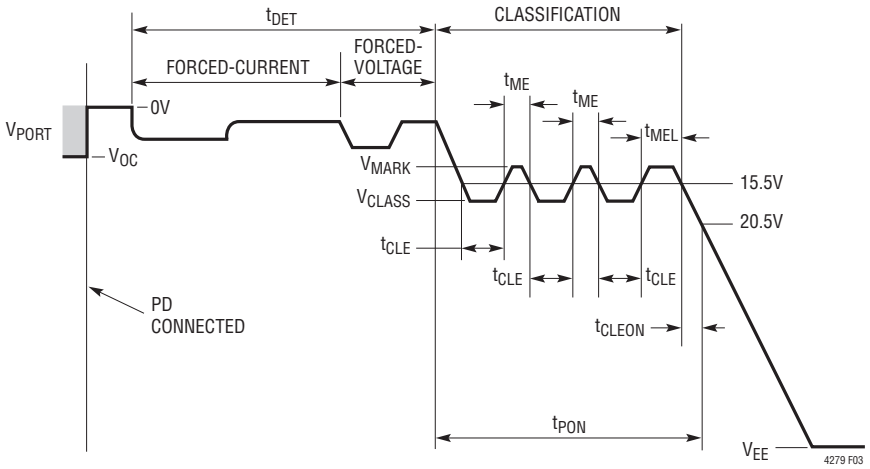


Figure 3. Detect, Three Event Class and Turn-On Timing

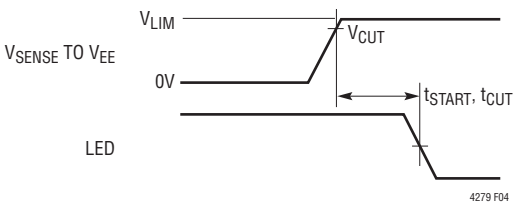


Figure 4. Current Limit Timing

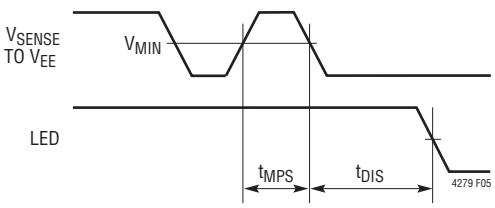


Figure 5. DC Disconnect Timing

PIN FUNCTIONS

$\overline{\text{RESET}}$: Reset Input, Active Low. When logic low, the LTC4279 is held inactive with the port off. When logic high, the LTC4279 begins normal operation. $\overline{\text{RESET}}$ can be connected to an external capacitor or RC network to provide a power turn-on delay. Internal filtering of the $\overline{\text{RESET}}$ pin prevents glitches less than 4.5µs wide from resetting the LTC4279. Internally pulled up to V_{ROC}. See Configuration Pin Protection section for proper connection.

MID: Midspan Mode Input. When logic high, midspan mode is enabled and the LTC4279 acts as a midspan device. When logic low, midspan mode is disabled and the LTC4279 acts as an endpoint device. Internally pulled down to V_{EE}. See Configuration Pin Protection section for proper connection.

LEGACY: LEGACY Mode Input. When logic high, LEGACY mode is enabled. With LEGACY mode enabled, valid detection results include R_{SIG} too Low, Detect Good, R_{SIG} too High, and C_{PD} too High as defined in Table 2; all Class 0, 1, 2 and 3 PDs presenting a valid detection signature are allocated 13W to ensure pre-802.3af PDs receive sufficient power; IEEE PoE PDs and LTPoE++ PDs are detected and classified as normal. When logic low, LEGACY mode is disabled. With LEGACY mode disabled only Detect Good is considered a valid detection result. Warning: LEGACY mode is, by definition, not IEEE compliant. Internally pulled down to V_{EE}. See Configuration Pin Protection section for proper connection.

DUALPD: Dual-Signature PD Mode Input. When logic high, DUALPD mode is enabled and the LTC4279 detects, classifies and powers dual-signature PDs. Valid dual-signature PDs are present when two Type 2 PD signatures are detected and classified in parallel. PWRMODE must be set to 52.7W or greater. When logic low, dual-signature PD support is disabled. Internally pulled down to V_{EE}. See Configuration Pin Protection section for proper connection.

PWRMODE: Maximum Power Mode. A single resistor from the PWRMODE pin to V_{EE} sets the LTC4279 maximum deliverable power. See Applications Information for the resistor value to desired maximum power mappings. The resistor tolerance must be 1% or better. The PWRMODE pin can be set to 13W (Type 1), 25.5W (Type 2), LTPoE++ 38.7W, 52.7W, 70W, 90W or UltraPWR maximum power levels.

LED: Port Powered LED. This pin is an open drain output that pulls down to V_{EE} when the port is powered. See the LED Drive section for details on this circuit.

AGND: Analog Ground. AGND pin should be connected to the return for the V_{EE} supply through a 10Ω resistor.

V_{EE}: Supply Input. Connect to a negative voltage of between –45V and –57V for Type 1 PSEs, –51V to –57V for Type 2 PSEs and LTPoE++ 38.7W/52.7W PSEs, –54.75V to –57V for LTPoE++ 70W/90W PSEs or –51V to –65V for UltraPWR PSEs, relative to AGND.

VSSK: Kelvin Sense to V_{EE}. Connect to sense resistor common node. Do not connect directly to V_{EE} plane. See Kelvin Sense section for proper connection.

SENSE: Current Sense Input. SENSE monitors the external MOSFET current via a 0.1Ω sense resistor between SENSE and V_{EE}. Whenever the voltage across the sense resistor exceeds the overcurrent detection threshold V_{CUT}, the current limit fault timer counts up. If the voltage across the sense resistor reaches the current limit threshold V_{LIM}, the GATE pin voltage is lowered to maintain constant current in the external MOSFET. See Applications Information for further details. See Kelvin Sense section for proper connection.

GATE: Gate Drive. GATE should be connected to the gate of the external MOSFET through the R_{GATE} resistor. When the MOSFET is turned on, the gate voltage is driven to 12V (typ) above V_{EE}. During a current limit condition, the voltage at GATE will be reduced to maintain constant current through the external MOSFET. If the fault timer expires, GATE is pulled down, turning the MOSFET off.

OUT: Output Voltage Monitor. OUT should be connected to the output port. A current limit foldback circuit limits the power dissipation in the external MOSFET by reducing the current limit threshold when the drain-to-source voltage exceeds 10V. A 500k resistor is connected internally from OUT to AGND when the port is idle.

DNC: Do Not Connect. All pins identified with DNC must be left unconnected.

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OVERVIEW

Power over Ethernet, or PoE, is a standard protocol for sending DC power over copper Ethernet data wiring. The IEEE group that administers the 802.3 Ethernet data standards added PoE powering capability in 2003. This original PoE spec, known as 802.3af, allowed for 48V DC power at up to 13W. This initial specification was widely popular, but 13W was not adequate for some requirements. In 2009, the IEEE released a new standard, known as 802.3at or PoE+, increasing the voltage and current requirements to provide 25.5W of power.

The IEEE standard also defines PoE terminology. A device that provides power to the network is known as a PSE, or power sourcing equipment, while a device that draws power from the network is known as a PD, or powered device. PSEs come in two types: Endpoints (typically network switches or routers), which provide data and power; and Midspans, which provide power but pass through data. Midspans are typically used to add PoE capability to existing non-PoE networks. PDs are typically IP phones, wireless access points, security cameras, and similar devices.

LTPoE++ Evolution

Even during the process of creating the IEEE PoE+ 25.5W specification it became clear that there was a significant and increasing need for more than 25.5W of delivered power. The LTC4279 responds to this market by allowing a reliable means of providing up to 90W of delivered power to an LTPoE++ PD. The LTPoE++ specification provides reliable detection and classification extensions to the existing IEEE PoE protocols that are backward compatible and interoperable with existing Type 1 and Type 2 PDs. Unlike other proprietary PoE++ solutions, Linear's LTPoE++ provides mutual identification between the PSE and PD. This ensures the LTPoE++ PD knows it may use the requested power at start-up because it has detected an LTPoE++ PSE.

Dual-Signature PD Systems

There exist proprietary solutions in which the data and spare pairs present two separate and individually valid PD signatures. Such systems provide roughly 51W at the PD interface. Each PD power channel, viewed in isolation, is fully compatible with IEEE 802.3at.

One example of a dual-signature PD system is shown in Figure 7. As shown, the PSE controller simultaneously detects and classifies both PDs. Once successfully identified, the lumped PD channel is provided twice the Class 4 Current Inrush, twice the Class 4 Current Cutoff, twice the Class 4 Current Limit, and normal Class 4 DC Disconnect allocations.

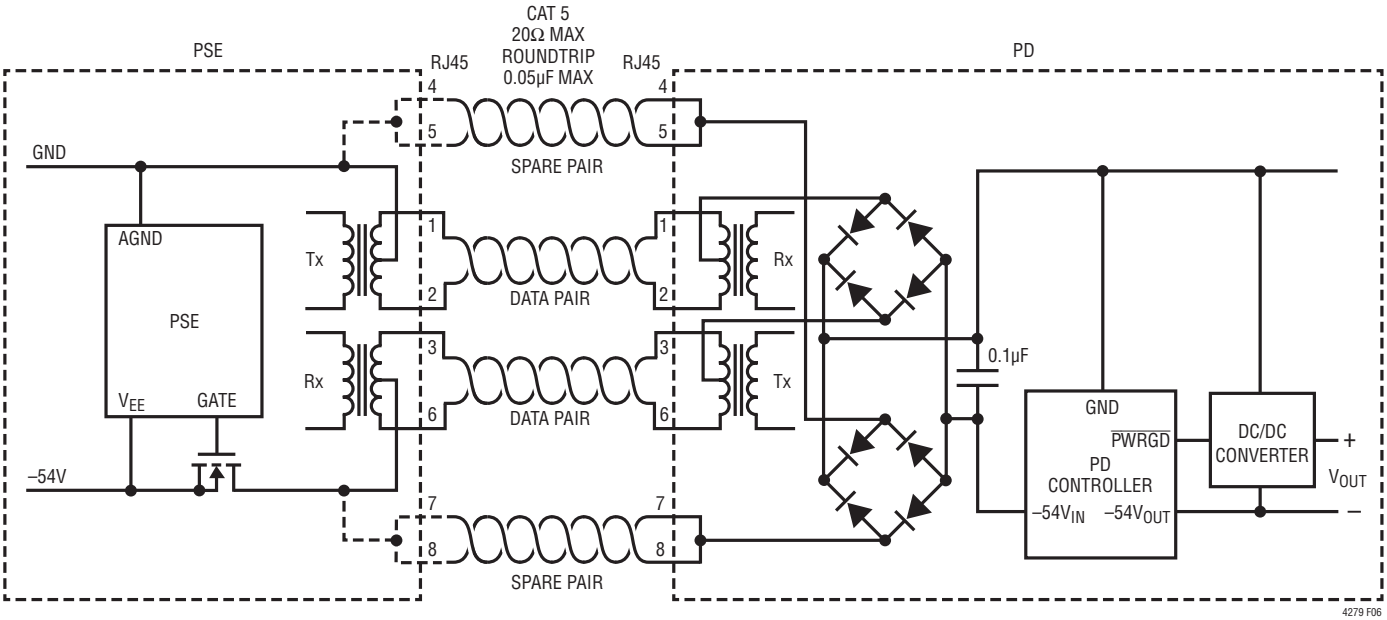

Figure 6. Power over Ethernet System Diagram

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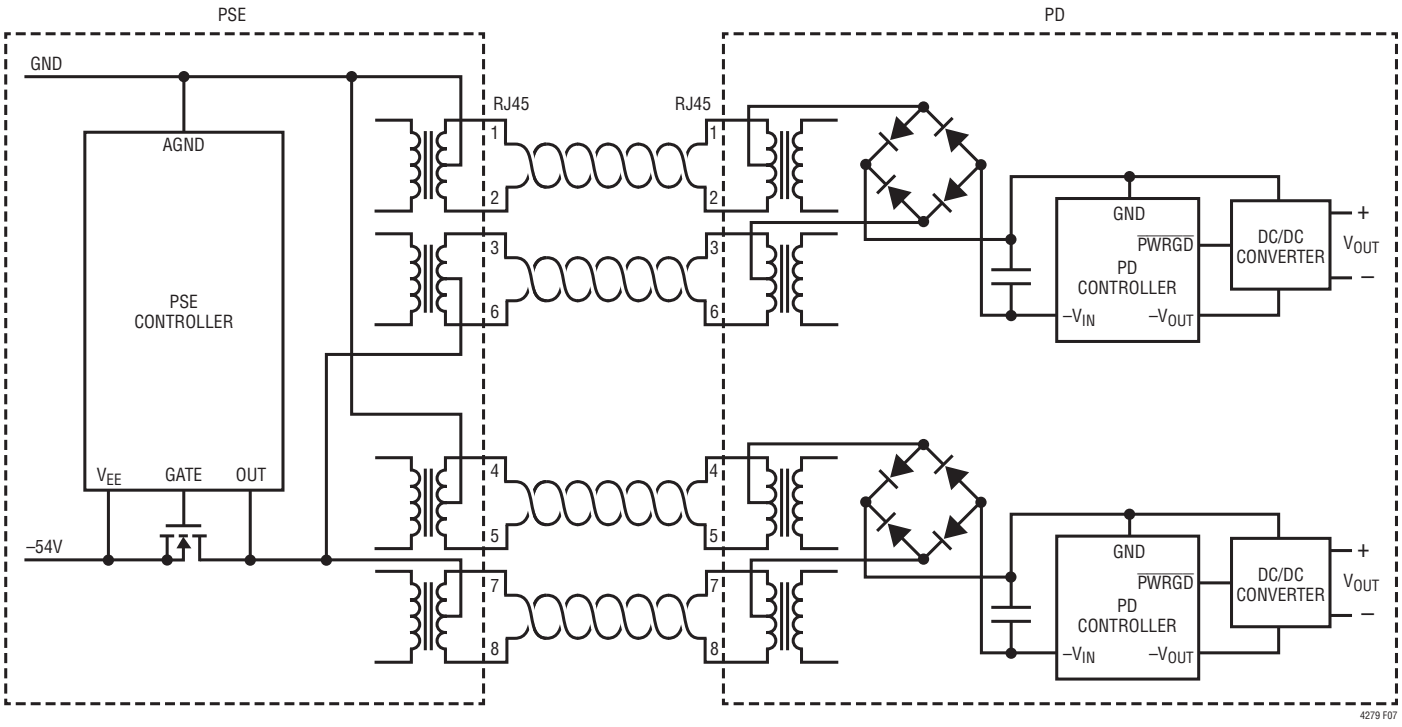

Figure 7. Dual-Signature PD Power over Ethernet System Diagram

LTC4279 Single Port PSE

The LTC4279 is a fourth-generation single port PSE controller. Virtually all necessary circuitry is included to implement an IEEE 802.3at compliant PSE design, requiring only an external power MOSFET and sense resistor; these minimize power loss compared to alternative designs with an on-board MOSFET and sense resistor.

The LTC4279 supports seven PD power levels. The mode is set by the PWRMODE resistor, as sampled during reset exit.

When in LTPoE++ mode, the LTC4279 extends PoE power delivery capabilities to one of four LTPoE++ levels. LTPoE++ is a Linear Technology proprietary specification allowing for the delivery of up to 90W to LTPoE++ compliant PDs. The LTPoE++ architecture extends the 802.3at physical power negotiation to include 38.7W, 52.7W, 70W and 90W power levels.

When DUALPD is enabled, the LTC4279 supports dual-signature PD topologies. Dual-signature PDs are defined as two PDs whose signature appears at the PD Power Interface (PI) as the parallel combination of two Type 2 PDs. Dual-signature PDs are autonomously detected, classified and powered on by the LTC4279. Current inrush, cutoff, and limit are doubled to support dual-signature PD topologies.

When in LTPoE++ or Type 2 mode, the LTC4279 is a fully IEEE-compliant Type 2 PSE supporting autonomous detection, classification and powering of Type 1 and Type 2 PDs.

When in Type 1 mode, the LTC4279 is a fully autonomous 802.3af Type 1 PSE solution. Two-event classification is prohibited and Class 4 PDs are automatically treated as Class 0 PDs.

UltraPWR mode enables the PSE to power all PDs presenting a valid detection and classification signature with enhanced inrush and operational current limits, regardless of classification result. This mode aggressively powers nonstandard PDs.

PoE BASICS

Common Ethernet data connections consist of two or four twisted pairs of copper wire (commonly known as CAT-5 cable), transformer-coupled at each end to avoid ground

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loops. PoE systems take advantage of this coupling arrangement by applying voltage between the center-taps of the data transformers to transmit power from the PSE to the PD without affecting data transmission. Figure 6 shows a high-level PoE system schematic.

To avoid damaging legacy data equipment that does not expect to see DC voltage, the PoE specification defines a protocol that determines when the PSE may apply and remove power. Valid PDs are required to have a specific 25k common mode resistance at their input. When such a PD is connected to the cable, the PSE detects this signature resistance and turns on the power. When the PD is later disconnected, the PSE senses the open circuit and turns power off. The PSE also turns off power in the event of a current fault or short-circuit.

When a PD is detected, the PSE looks for a classification signature that tells the PSE the maximum power the PD will draw. The PSE can use this information to reject a PD that will draw more power than the PSE has available.

OPERATING MODES

The LTC4279 is a fully autonomous PSE controller and provides a complete PSE solution for detection, classification and powering of PDs in an IEEE 802.3 or LTPoE++ compliant system.

The LTC4279 will power all valid PDs with I_{CUT} and I_{LIM} values based on the PWRMODE pin and the PD classification result.

The LTC4279 will remove power automatically if the port generates a current cutoff or limit fault. The LTC4279 senses removal of a PD and turns off power when the PD is disconnected. Internal control circuits comply with IEEE timing and electrical parameters.

Power-On Reset and the Configuration Pins

The initial LTC4279 configuration depends on the state of the MID, LEGACY, DUALPD and PWRMODE pins during reset exit. Reset occurs at power-up or whenever the $\overline{RESET}$ pin is pulled low. Changing any of the configuration pins after power-up will not change the behavior of the LTC4279 until a subsequent reset occurs.

Table 1 shows the PWRMODE encodings. The PWRMODE pin is configured by connecting R_{PM} between the PWRMODE pin and V_{EE}. The PWRMODE effect on PSE behavior is described in the Classification and Power Control sections.

Table 1. PWRMODE Encodings

PWRMODE	R_{PM} (± 1%)
Type 1 (13W)	2.37k
Type 2 (25.5W)	3.32k
LTPoE++ 38.7W	4.64k
LTPoE++ 52.7W	5.90k
LTPoE++ 70W	7.87k
LTPoE++ 90W	10.0k
UltraPWR	13.0k

The LEGACY pin determines whether pre-IEEE standard legacy PDs are powered.

The MID pin determines whether midspan detection timing is enabled. The MID pin should be logic high if the standalone application is a midspan.

DETECTION

Detection Overview

To avoid damaging network devices that were not designed to tolerate DC voltage, a PSE must determine whether the connected device is a valid PD before applying power. The IEEE specification requires that a valid PD have a common mode resistance of 25k ±5% at any port voltage below 10V. The PSE must accept resistances that fall between 19k and 26.5k, and it must reject resistances above 33k or below 15k (shaded regions in Figure 8). The PSE may choose to accept or reject resistances in the undefined areas between the must-accept and must-reject ranges. In particular, the PSE must reject standard computer network ports, many of which have 150Ω common mode termination resistors that will be damaged if power is applied to them (the black region at the left of Figure 8).

Table 2 shows the possible detection results. If a Detect Good result is acquired the LTC4279 will proceed to classification.

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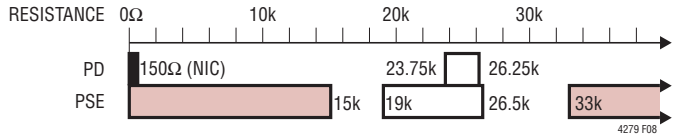

Figure 8. IEEE 802.3at Signature Resistance Ranges

Table 2. Detection Status

MEASURED PD SIGNATURE (TYPICAL)	DETECTION RESULT
Incomplete or Not Yet Tested	Detect Status Unknown
<2.4k	Short-Circuit
Capacitance > 2.7µF	C_{PD} too High
2.4k < R_{PD} < 17k	R_{SIG} too Low
17k < R_{PD} < 29k	Detect Good
>29k	R_{SIG} too High
>50k	Open Circuit
Voltage > 10V	Port Voltage Outside Detect Range

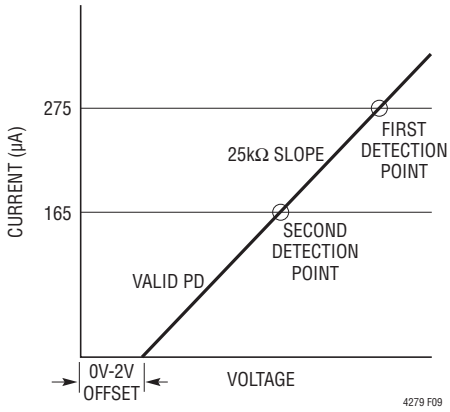

Figure 9. PD Detection

Detection of Legacy PDs

Proprietary PDs that predate the original IEEE 802.3af standard are commonly referred to today as legacy PDs. One type of legacy PD uses a large common mode capacitance (>10µF) as the detection signature. Note that PDs in this range of capacitance are defined as invalid, so a PSE that detects legacy PDs is technically noncompliant with the IEEE specification. The LTC4279 can be configured to detect this type of legacy PD when LEGACY is enabled. When LEGACY is enabled, valid detection results include C_{PD} too High, R_{SIG} too low, Detect Good, and R_{SIG} too High. PDs presenting Class 0, 1, 2 or 3 are assigned Class 0 power allocation to ensure pre-802.3af PDs receive sufficient power. When LEGACY is disabled, only PDs presenting Detect Good (including compliant IEEE PoE and LTPoE++ PDs) will be considered valid.

Detection of Dual-Signature PDs

Proprietary PDs that employ a dual-signature PD topology are detected in parallel. Such PDs will present a parallel resistance of one half of the Detect Good resistance. This parallel detection resistance is located in the R_{SIG} too Low range as shown in Table 2. When DUALPD is enabled, dual-signature PDs (R_{SIG} too Low detection results) will proceed to classification regardless of the LEGACY mode.

CLASSIFICATION

802.3af Classification

A PD must present a classification signature to the PSE to indicate the maximum power it will draw while operating. The IEEE specification defines this signature as a constant current draw when the PSE port voltage is in the V_{CLASS} range (between 15.5V and 20.5V), with the current level indicating one of 5 possible PD classes. Figure 10 shows a typical PD load line, starting with the slope of the 25k signature resistor below 10V, then transitioning to the classification signature current (in this case, Class 3) in the V_{CLASS} range. Table 3 shows the possible classification values.

When LEGACY is enabled all Class 0, 1, 2 and 3 PDs are allocated 13W to ensure legacy PDs receive sufficient power. Legacy PDs may have an IEEE-like detection signature and do not support physical classification. Therefore, allocating 13W to all Type 1 and legacy PDs ensures full legacy PD support.

Table 3. 802.3af and 802.3at Classification Values (LEGACY = Disabled)

CLASS	PWRMODE = TYPE 1	PWRMODE = TYPE 2
Class 0	No Class Signature Present; Treat Like Class 3	
Class 1	3W	
Class 2	7W	
Class 3	13W	
Class 4	13W (Demote to Class 0)	25.5W (Type 2)

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The PSE will classify the PD immediately after a successful detection cycle. The PSE measures the PD classification signature by applying 18V for 12ms (both values typical) to the port via the OUT pin and measuring the resulting current. If a valid classification result is obtained, the LTC4279 will use the result to set the I_{CUT} and I_{LIM} thresholds.

The LTC4279 supports 802.3af 1-event classification regardless of the PWRMODE setting. A Class 0 to 3 result during the first classification event will result in the PD receiving the appropriate amount of power as shown in Table 3.

When a Class 4 result is obtained the LTC4279 response depends on PWRMODE, as shown in Table 3. If PWRMODE is set to Type 1 then the PD will be powered on after receiving only a single class event and will be allocated only 13W. If PWRMODE is set to Type 2 or higher, additional class events will be issued as described in the following sections.

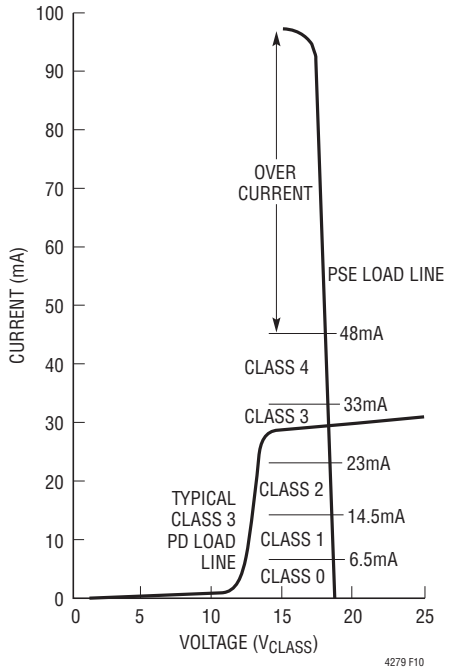

Figure 10. PD Classification

802.3at 2-Event Classification

The LTC4279 supports 802.3at 2-event physical classification when PWRMODE is set to Type 2 or higher.

A Type 2 PD that is requesting more than 13W will indicate Class 4 during normal 802.3af classification. If the LTC4279 sees Class 4, it forces the port to a specified lower voltage (called the mark voltage, typically 9V), pauses briefly, and then re-runs classification to verify the Class 4 reading (Figure 2). The second cycle informs the PD that it is connected to a Type 2 PSE capable of supplying Type 2 power levels.

Note that the LTC4279 only runs the second classification cycle when it detects a Class 4 device; if the first cycle returns Class 0 to 3, the port determines it is connected to a Type 1 PD and does not run the second classification cycle.

Invalid Type 2 Class Combinations

The 802.3at specification defines a Type 2 PD class signature as two consecutive Class 4 results; a Class 4 followed by a Class 0 to 3 is not a valid signature. If the PD presents an invalid Type 2 signature (Class 4 followed by Class 0 to 3), the LTC4279 will not provide power and will restart the detection process.

Dual-Signature PD Classification

Dual-signature PDs are supported by performing a parallel classification. When a dual-signature PD is present, each PD will draw a nominal classification current of up to 40mA, for a total possible of 80mA. A dual-signature PD is validated when the LTC4279 observes both an R_{SIG} too Low detection result and a multiple-event overcurrent classification result.

Extended Power LTPoE++ Classification

The 802.3at 2-event physical classification method is extended using LTPoE++ 3-event classification signaling methods (Figure 3).

LTPoE++ 3-event classification and power levels are enabled by setting PWRMODE to 38.7W or higher.

The higher levels of LTPoE++ delivery impose additional layout and component selection constraints. LTPoE++ PDs requesting more than the available power limits are not powered. For example, if PWRMODE is set to 70W and an LTPoE++ 90W PD is detected and classified, the PD will not be powered.

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Power Allocation

LTC4279 allocates power based on the PWRMODE setting as described in Table 1. The PWRMODE informs the PSE how much power is available. Based on the PD class result the PD is allocated power if sufficient power is available as shown in Figure 11. In some situations the PD will be denied power in accordance with the LTPoE++ protocol.

DEVICE			PSE PWRMODE SETTING					
	STANDARD		802.3at		LTPoE++			
		TYPE	TYPE 1	TYPE 2	38.7W	52.7W	70W	90W
PD	802.3at	TYPE 1	13W	13W	13W	13W	13W	13W
		TYPE 2	13W	25.5W	25.5W	25.5W	25.5W	25.5W
	LTPoE++	38.7W	13W	25.5W	38.7W	38.7W	38.7W	38.7W
		52.7W	13W	25.5W	–	52.7W	52.7W	52.7W
		70W	13W	25.5W	–	–	70W	70W
		90W	13W	25.5W	–	–	–	90W

Figure 11. PSE PWRMODE vs PD Class Power Allocation

For example, an LTPoE++ 70W PSE will refuse power to an LTPoE++ 90W PD, but will power IEEE 802.3at PDs and LTPoE++ PDs requesting 70W and under with their full power allocation. In comparison, an IEEE Type 2 PSE will issue full power allocation to Type 1 and Type 2 PDs; all LTPoE++ PDs will be powered with a demoted allocation of 25.5W. An IEEE Type 1 PSE will issue full power allocation to IEEE Type 1 PDs; all Type 2 and LTPoE++ PDs will be powered with a demoted allocation of 13W.

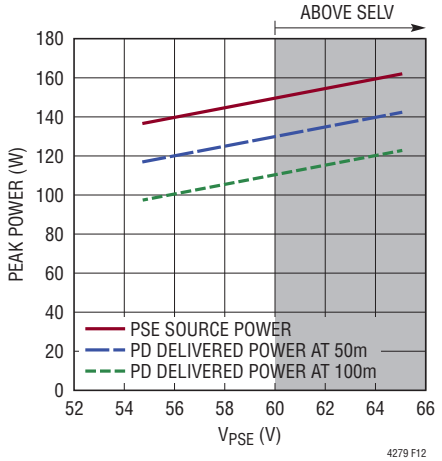

Figure 12. UltraPWR Power vs V_{PSE}

UltraPWR MODE

A PSE in UltraPWR mode issues up to three class events and powers all valid PDs with maximum deliverable power, as determined by V_{PSE}. Figure 12 shows PSE source power (at the PSE RJ45 jack) and PD delivered power (at the PD RJ45 jack) vs V_{PSE}. The gray shaded area above 60V shows voltages exceeding SELV maximum; systems exceeding SELV maximum voltage may incur additional regulatory hurdles.

POWER CONTROL

The primary function of the LTC4279 is to control the delivery of power to the PSE port. It does this by controlling the gate drive voltage of an external power MOSFET while monitoring the current via an external sense resistor and the output voltage at the OUT pin. This circuitry serves to couple the raw V_{EE} input supply to the port in a controlled manner that satisfies the PD's power needs while minimizing both power dissipation in the MOSFET and disturbances on the V_{EE} backplane.

Inrush Control

Once the decision has been made to turn on a port, the LTC4279 ramps up the GATE pin of the external MOSFET in a controlled manner. Under normal power-up circumstances, the MOSFET gate voltage will rise until the port current reaches the inrush current limit level, at which point the GATE pin will be servoed to maintain the specified I_{INRUSH} current. During this inrush period, a timer (t_{START}) runs. When output charging is complete, the port current will fall and the GATE pin will be allowed to continue rising to fully enhance the MOSFET and minimize its on-resistance. The final V_{GS} is nominally 12V. If the t_{START} timer expires and the PD is over the current limit level, the port will be turned off.

Per the IEEE specification, the LTC4279 will normally set the inrush current limit (I_{LIM}) to 425mA during inrush at port turn-on, and then switch to the classified I_{LIM} setting once inrush has completed.

When DUALPD is enabled and a dual-signature PD is successfully detected and classified, the inrush current will be doubled. This allows dual-signature PDs to be powered up in parallel.

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When UltraPWR mode is enabled and a legacy, dual-signature, LTPoE++ or IEEE PD is detected and classified, I_{LIM} will be set to 1.5A to provide more substantial inrush current for custom PDs.

Current Cutoff and Limit

The LTC4279 automatically maintains two current thresholds (I_{CUT} and I_{LIM}), each with a corresponding timer (t_{CUT} and t_{LIM}). The I_{CUT} and I_{LIM} thresholds depend on several factors: the PD Class, the UltraPWR mode, and the DUALPD and LEGACY pin states.

Table 4 shows the I_{CUT} and I_{LIM} values that will be automatically set depending on LEGACY pin, the UltraPWR state and the negotiated PD class. When UltraPWR is enabled, I_{CUT} is disabled and I_{LIM} is 2950mA (typical) regardless of classification result.

Table 4. Typical I_{CUT} and I_{LIM} Values

CLASS	ULTRAPWR	LEGACY	I_{CUT}	I_{LIM}
Class 1	Disabled	Disabled	112mA	425mA
Class 2	Disabled	Disabled	206mA	425mA
Class 3, 0	Disabled	Disabled	375mA	425mA
Class 0, 1, 2, 3	Disabled	Enabled	375mA	425mA
Class 4	Disabled	Don't Care	638mA	850mA
LTPoE++ 38.7W	Disabled	Don't Care	919mA	1275mA
Dual-Signature PD/ LTPoE++ 52.7W	Disabled	Don't Care	1350mA	1488mA
LTPoE++ 70W	Disabled	Don't Care	1650mA	1913mA
LTPoE++ 90W	Disabled	Don't Care	2325mA	2550mA
All Classes	Enabled	Don't Care	Disabled	2950mA

Per the IEEE specification, the LTC4279 will allow the port current to exceed I_{CUT} for a limited period of time before removing power from the port, whereas it will actively control the MOSFET gate drive to keep the port current below I_{LIM}. The port does not take any action to limit the current when only the I_{CUT} threshold is exceeded, but does start the t_{CUT} timer. If the current drops below the I_{CUT} current threshold before its timer expires, the t_{CUT} timer counts back down, but at 1/16 the rate that it counts up. If the t_{CUT} timer reaches 60ms (typical) the port is turned off. This allows the current limit circuitry to tolerate intermittent overload signals with duty cycles below about 6%; longer duty cycle overloads will turn the port off.

The I_{LIM} current limiting circuit is always enabled and actively limits port current. I_{CUT} is set to a lower value than I_{LIM} to allow the port to tolerate minor faults without current limiting.

A second timer, t_{LIM}, is enabled when a PD is allocated more than 25.5W to provide more aggressive MOSFET protection and turn off a port before MOSFET damage can occur. The t_{LIM} timer starts when the I_{LIM} threshold is exceeded. When the t_{LIM} timer reaches 12ms (typical) the port is turned off.

t_{LIM} is not enabled when a PD is allocated 25.5W or less. Instead, t_{LIM} behaviors are tracked by the t_{CUT} timer, which counts up during both I_{LIM} and I_{CUT} events.

I_{LIM} Foldback

The LTC4279 features a two-stage foldback circuit that reduces the port current if the port voltage falls below the normal operating voltage. This helps keep MOSFET power dissipation at safe levels.

The LTC4279 will support current levels well beyond the maximum values in the 802.3at specification. High power PSE implementations require a larger external MOSFET and possibly additional heat sinking. Due to the high inrush current extra care is required during MOSFET selection. See the External Component Selection – External MOSFET section for more information.

MOSFET Fault Detection

The LTC4279 is designed to tolerate significant levels of abuse, but in extreme cases it is possible for the external MOSFET to be damaged. A failed MOSFET may short source to drain, which will make the port appear to be on when it should be off; this condition may also cause the sense resistor to fuse open, turning off the port but causing the LTC4279 SENSE pin to rise to an abnormally high voltage. A failed MOSFET may also short from gate to drain, causing the LTC4279 GATE pin to rise to an abnormally high voltage. The LTC4279 OUT, SENSE and GATE pins are designed to tolerate up to 80V faults without damage.

If the LTC4279 sees any of these conditions for more than 180µs, it resets the entire chip.

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Disconnect

The LTC4279 monitors the powered port to ensure the PD continues to draw the minimum specified current. A disconnect timer counts up whenever port current is below 7.5mA (typ), indicating that the PD has been disconnected. If the t_{DIS} timer expires, the port will be turned off. If the current returns before the t_{DIS} timer runs out, the timer resets. As long as the PD exceeds the minimum current level for t_{MPS} more often than t_{DIS}, it will remain powered.

EXTERNAL COMPONENT SELECTION

Main PoE Power Supply and Bypassing

The LTC4279 requires one supply voltage to operate at V_{EE}. V_{EE} requires a negative voltage relative to AGND within the range specified in the Electrical Characteristics for each PSE Type.

V_{EE} is the main isolated PoE supply that provides power to the PD. Because it supplies a relatively large amount of power and is subject to significant current transients, it requires more design care than a simple logic supply. For minimum IR loss and best system efficiency, set V_{EE} near maximum amplitude (57V, or 65V for UltraPWR), leaving enough margin to account for transient over- or undershoot, temperature drift, and the line regulation specifications of the particular power supply used.

Bypass capacitance between AGND and V_{EE} is very important for reliable operation. If a short-circuit occurs at the port output, it can take as long as 1µs for the LTC4279 to begin regulating the current. During this time the current is limited only by the small impedances in the circuit. A high current spike typically occurs, causing a voltage transient on the V_{EE} supply and possibly causing the LTC4279 to reset due to a UVLO fault. A 1µF, 100V X7R capacitor placed near the AGND and V_{EE} pins along with an electrolytic bulk capacitor of at least 47µF across the main supply is recommended to minimize spurious resets.

To ensure compliance with DC disconnect, V_{EE} supply ripple and noise must be less than $100mV_{P-P}$ at frequencies above 150kHz. Note that supply ripple and noise is also limited by the IEEE 802.3at standard.

For UltraPWR applications only, limit dV/dt on the V_{EE} supply to less than 10V/ms when the supply is starting up.

External MOSFET

Careful selection of the power MOSFET is critical to system reliability. LTC recommends the NXP PSMN075-100MSE for proven reliability in Type 1 and Type 2 PSE applications. LTC recommends the NXP PSMN040-100MSE for dual-signature PD and LTPoE++ PSE applications. SOA curves are not a reliable specification for MOSFET selection. Contact LTC Applications before using a MOSFET other than one of these recommended parts. R_{GATE} (Figure 13) is an essential part of the current limit control loop. The R_{GATE} value may depend upon MOSFET selection. An additional RC network across the MOSFET drain and gate is required for the UltraPWR MOSFET. See the UltraPWR Endpoint PSE application circuit for details.

Sense Resistor

The LTC4279 is designed to use a 0.1Ω current sense resistor to reduce power dissipation. In order to meet the I_{CUT} and I_{LIM} accuracy required by the IEEE specification, the sense resistor should have ±1% tolerance or better, and no more than ±200ppm/°C temperature coefficient. The sense resistor must be sized according to power dissipation. See the Layout Guidelines section for proper Kelvin sensing.

Port Output Capacitor

The port requires a 0.22µF capacitor across the LTC4279 OUT pin and AGND pin to keep the LTC4279 stable while in current limit during startup or overload. Common ceramic capacitors often have significant voltage coefficients; this means the capacitance is reduced as the applied voltage increases. To minimize this problem, X7R ceramic capacitors rated for at least 100V are recommended and must be located close to the OUT pin and AGND pin (see Layout Guidelines).

Surge Protection

Ethernet ports can be subject to significant cable surge events. To keep PoE voltages below a safe level and protect the application against damage, protection components (Figure 13) are required at the main supply, at the LTC4279 supply pins and at the output port.

Bulk transient voltage suppression (TVS_{BULK}) and bulk capacitance (C_{BULK}) are required across the main PoE

APPLICATIONS INFORMATION

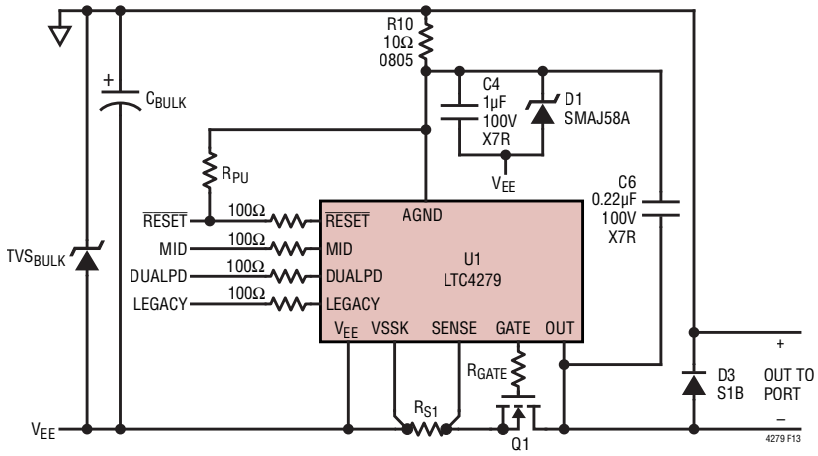


Figure 13. LTC4279 Surge Protection

supply and should be sized to accommodate system level surge requirements.

The LTC4279 (U1) requires a 10Ω, 0805 resistor (R10) in series from supply AGND to the LTC4279 AGND pin. Across the LTC4279 AGND pin and V_{EE} pin are an SMAJ58A, 58V TVS (D1) and a 1µF, 100V bypass capacitor (C4). These components must be placed close to the LTC4279 pins.

Finally, the port requires an S1B clamp diode (D3) from OUT to supply AGND. The diode protects the port from harmful surges that could cause OUT to go above AGND. This diode must have low impedance paths to the port.

See Layout Guidelines for additional information on parts placement.

Configuration Pin Protection

The logic input pins ($\overline{\text{RESET}}$, MID, LEGACY and DUALPD) may be hard tied to the AGND pin or to V_{EE}. Alternatively, if a pull-up resistor (R_{PU}) is implemented from a logic input pin to the LTC4279 supply, connect the resistor to the protected side of the 10Ω resistor at the AGND pin. For logic input pins configured off board through a connector, add a 100Ω resistor in series with the respective pin for protection during high voltage transients.

LED Drive

Connect an LED to the LTC4279 LED pin for a port on status indicator. The LED pin open drain pull-down output pulls down to V_{EE} when the port is powered on and is high impedance when the port is off. Pull the LED up to a supply with a current limiting resistor. Select the resistor value to provide enough LED current for adequate LED brightness and limit the current to below the LTC4279 LED pin current limit over the full supply range. The resistor must also have a power rating capable of the maximum supply voltage minus the LED drop and LED current. If the main PoE power supply is driving the LED, the pull-up resistor must connect to the LTC4279 AGND pin side of the surge protection 10Ω resistor. Refer to the Typical Application figure.

LAYOUT GUIDELINES

Strict adherence to parts placement and board layout is critical for optimal current reading accuracy, IEEE compliance, system robustness and thermal dissipation. Refer to the DC2541 demo board as a layout reference. Figure 14 is a cutout portion of the DC2541 that displays the focus topics in this section. The components are referenced in Figure 13.

Kelvin Sense

Proper connection of the port current Kelvin sense lines is important for current threshold accuracy and IEEE compliance. Refer to Figure 14 for an example layout of these Kelvin sense lines. The LTC4279 VSSK pin connects to a Kelvin sense trace to the sense resistor (V_{EE} side) pad and is not connected directly to V_{EE} copper areas. Similarly, the LTC4279 SENSE pin connects to a Kelvin sense trace that leads to the sense resistor (SENSE side) pad and is not

APPLICATIONS INFORMATION

connected in the power path between the sense resistor and the MOSFET. Figure 14 shows the two Kelvin traces from the LTC42479 (U1) to the sense resistor (R_{S1}). The LTC4249 V_{EE} pins and the sense resistor V_{EE} pad connect to the V_{EE} copper areas.

Parts Placement

The placement of key components around the LTC4279 is essential for application accuracy, stability and robustness. Figure 14 shows the port OUT capacitor (C6) and LTC4279 surge protection components located near the LTC4279.

Thermal Considerations

The power paths from the main power supply to the port output will have high currents pass through at peak port power. Use wide traces and copper areas, along multiple vias to keep the power path resistance low. Use copper areas around power path components to help spread heat out away from the components. This is particularly important around the power MOSFET (Q1) during current limit conditions.

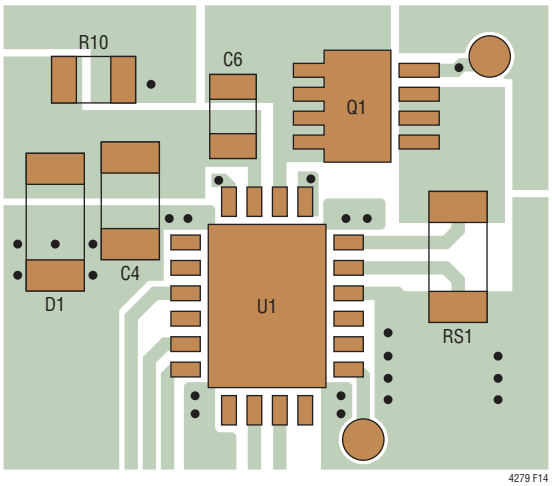
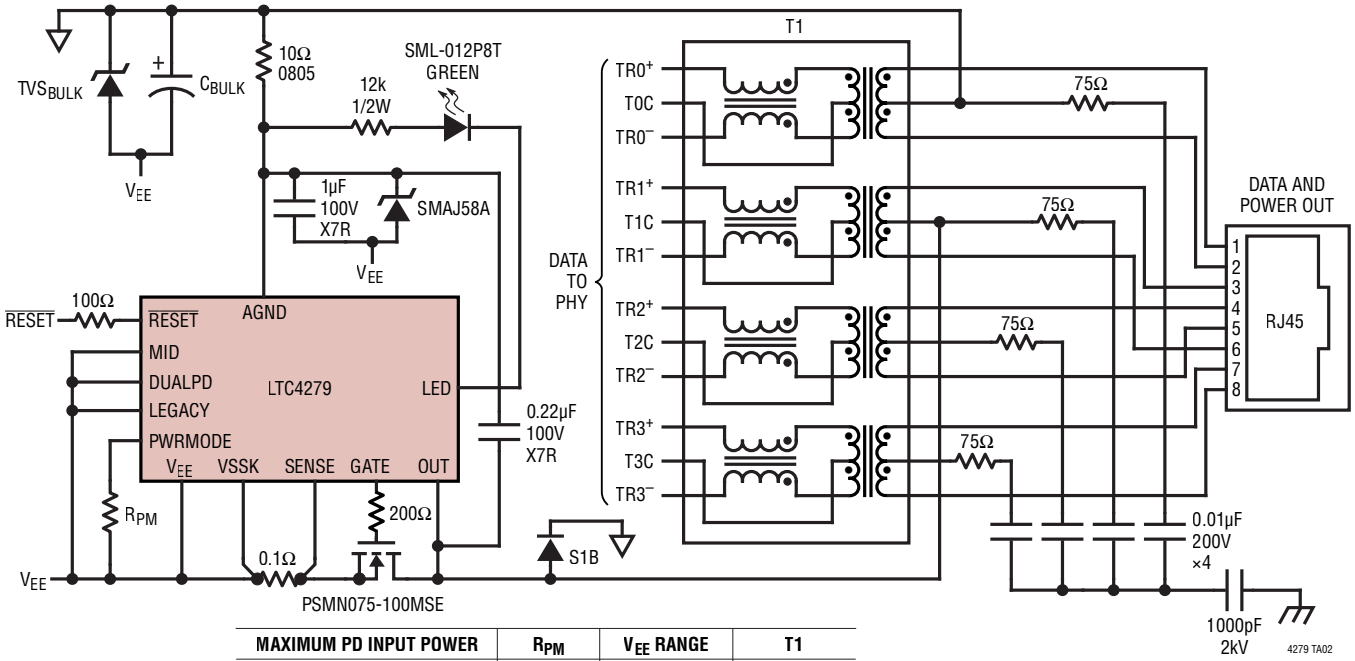


Figure 14. Example LTC4279 Layout

TYPICAL APPLICATIONS

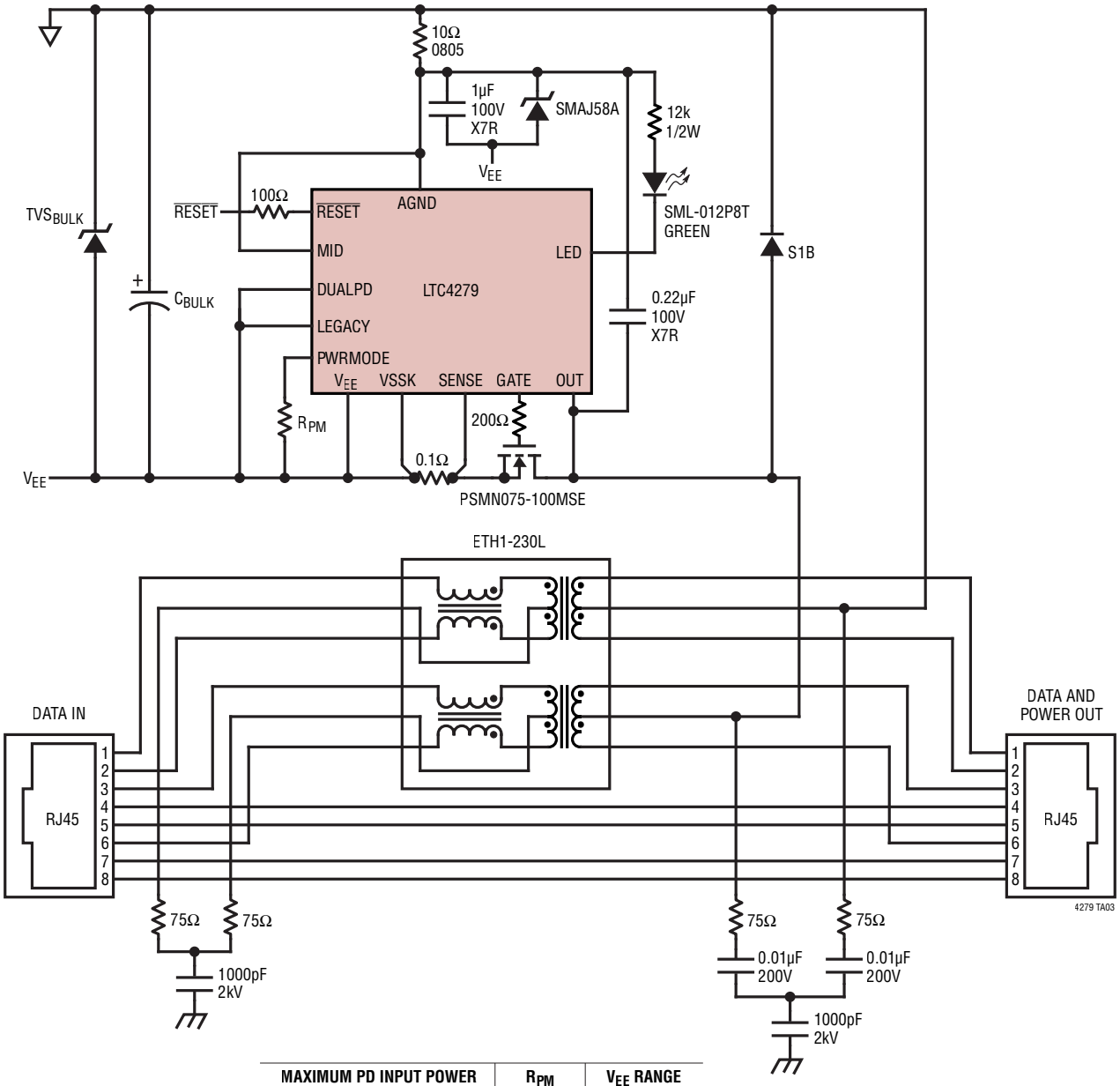
IEEE 802.3at, Type 1 or Type 2, Endpoint PSE



MAXIMUM PD INPUT POWER	R_{PM}	V_{EE} RANGE	T1
TYPE 1 (13W)	2.37k	–45V to –57V	749023015
TYPE 2 (25.5W)	3.32k	–51V to –57V	749022017

TYPICAL APPLICATIONS

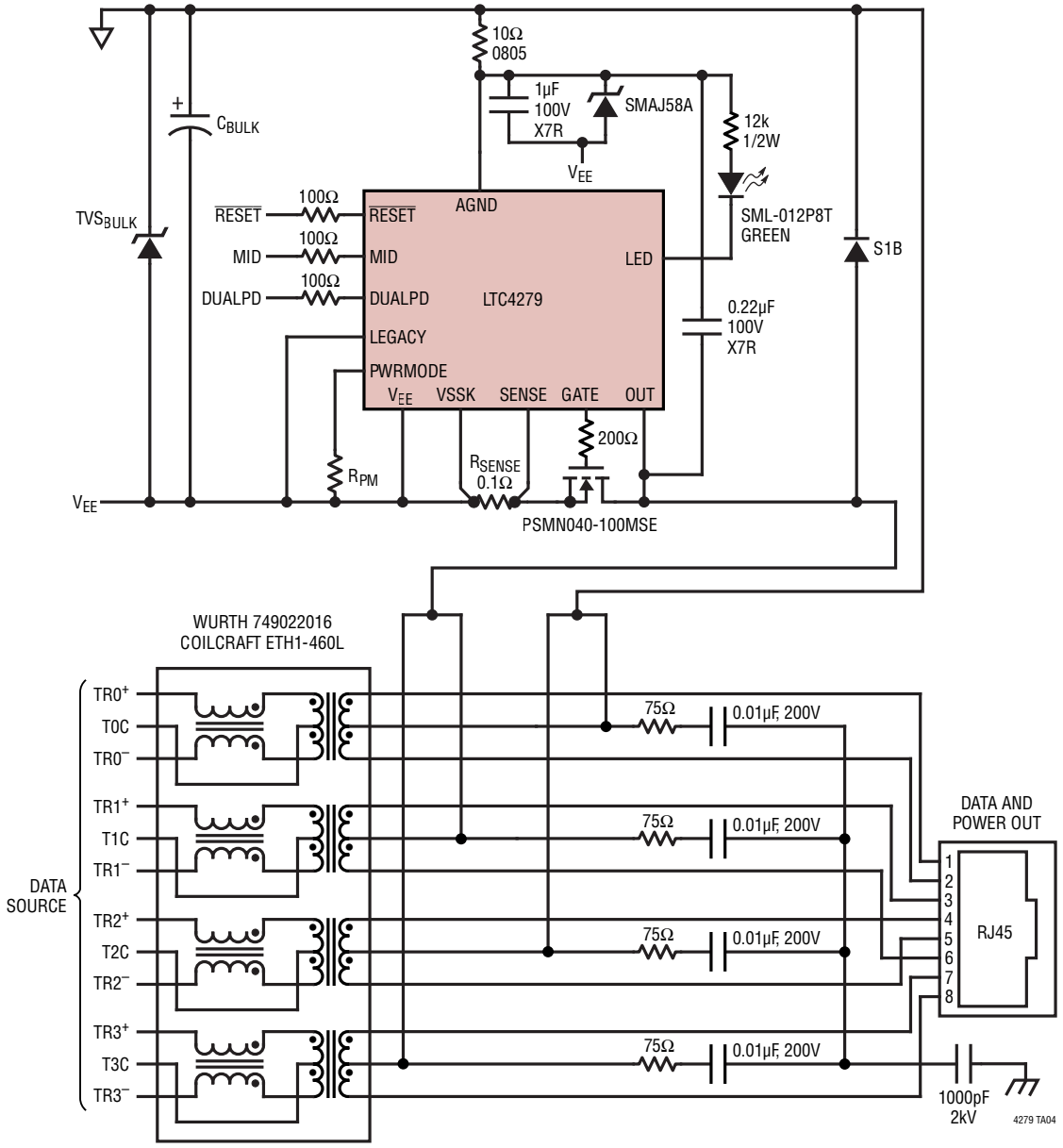
IEEE 802.3at, Type 1 or Type 2, Midspan PSE



MAXIMUM PD INPUT POWER	R_{PM}	V_{EE} RANGE
TYPE 1 (13W)	2.37k	–45V to –57V
TYPE 2 (25.5W)	3.32k	–51V to –57V

TYPICAL APPLICATIONS

LTPoE++ or Dual-Signature PD, Midspan or Endpoint, 4-Pair PSE Options

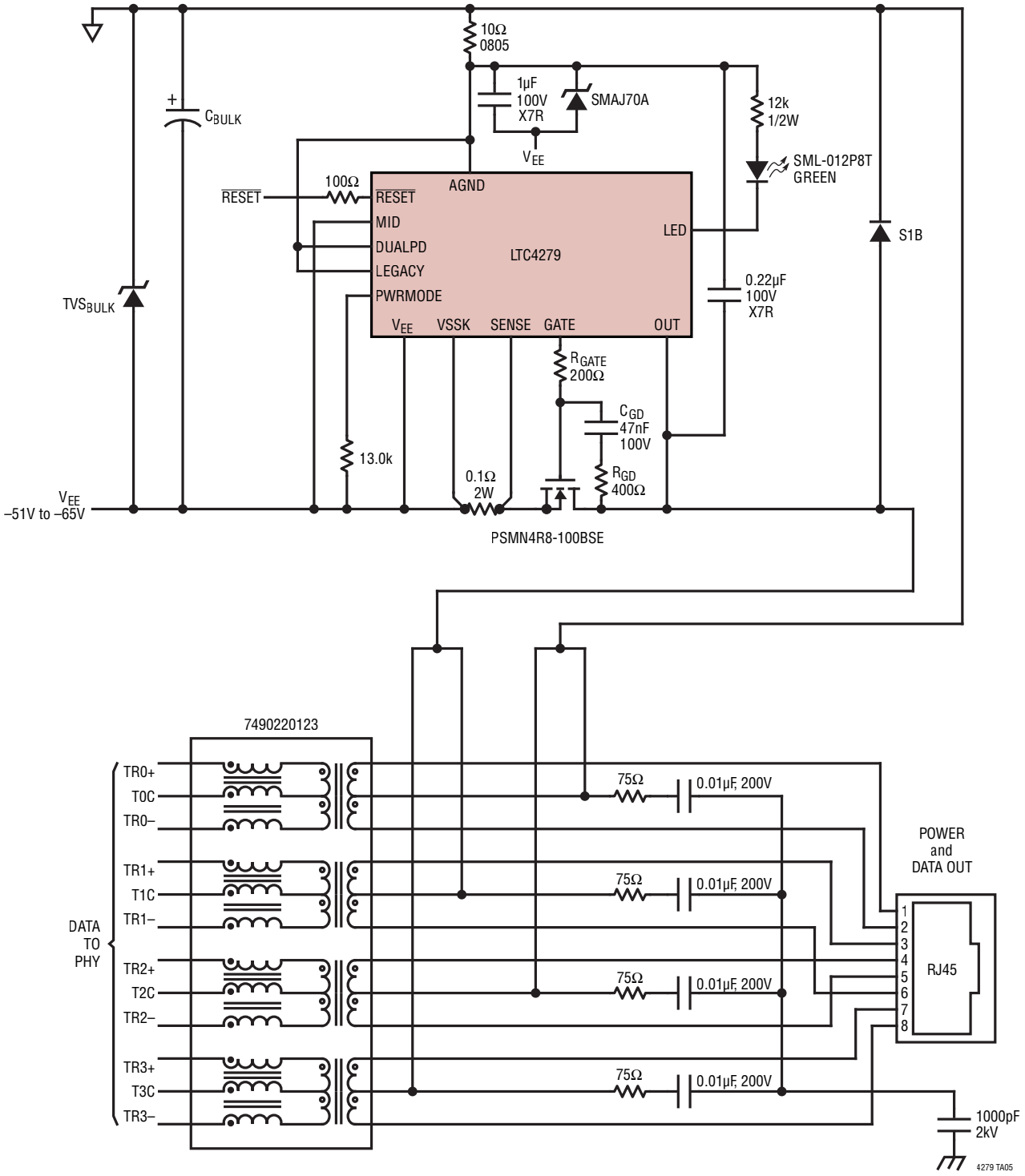


MAXIMUM PD INPUT POWER	V_{EE} RANGE	R_{PM}	DUALPD PIN	R_{SENSE} POWER RATING
LTPoE++ 38.7W	–51V to –57V	4.64k	LOW	1/4W
LTPoE++ 52.7W	–51V to –57V	5.90k	LOW	1/2W
DUALPD (52.7W)	–51V to –57V	5.90k	HIGH	1/2W
LTPoE++ 70W	–54.75V to –57V	7.87k	LOW	1/2W
LTPoE++ 90W	–54.75V to –57V	10.0k	LOW	1W

DEVICE TYPE	DATA SOURCE	MID PIN
ENDPOINT SWITCH	PHY	LOW
MIDSPAN POWER INJECTOR	DATA IN RJ45	HIGH

TYPICAL APPLICATIONS

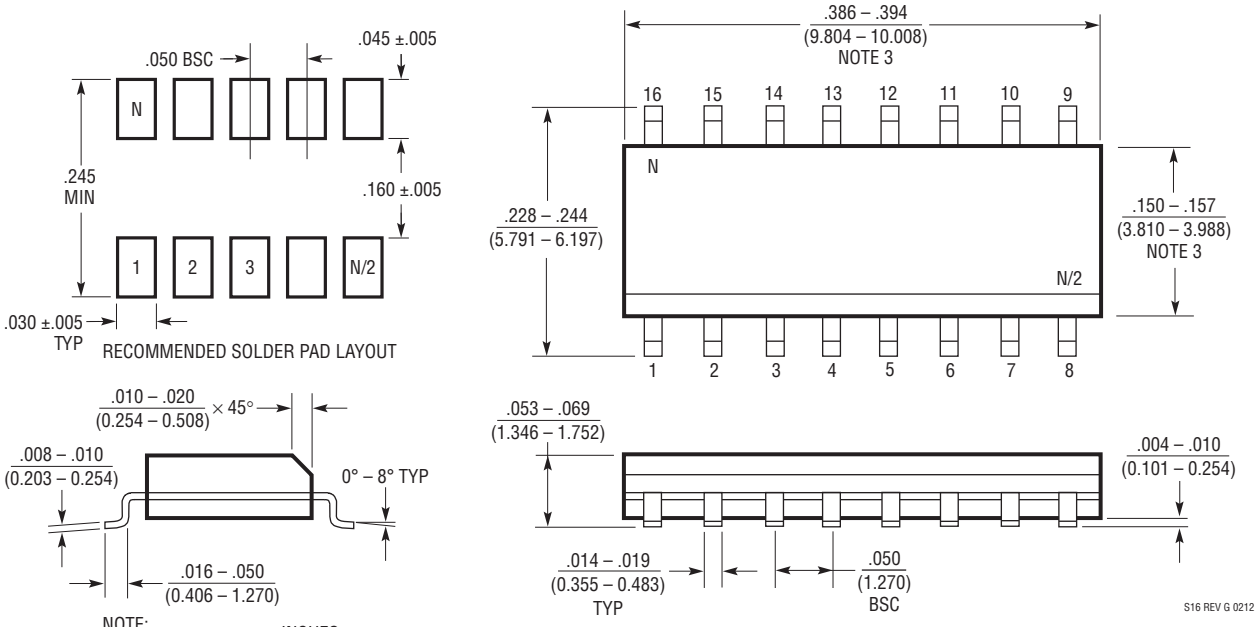
UltraPWR Endpoint PSE



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC4279#packaging for the most recent package drawings.

S Package
16-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)

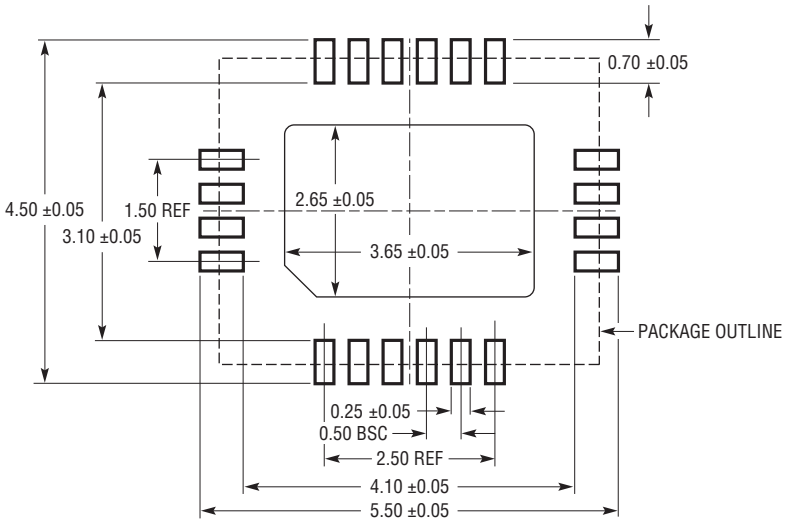


NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

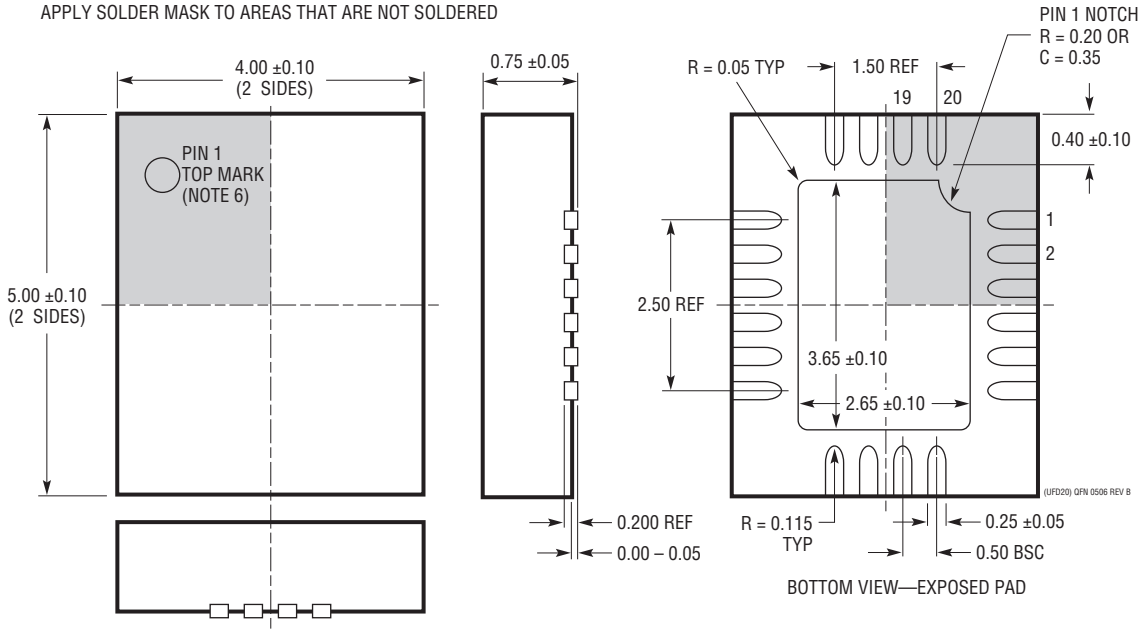
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC4279#packaging for the most recent package drawings.

UFD Package
20-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1711 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/17	Changed minimum/maximum limits for t_{CLE1}, t_{CLE} and t_{ME}.	4
		Corrected transformer P/Ns.	21, 22