Fixed Ratio High Power Inductorless (Charge Pump) DC/DC Controller

FEATURES

- **Low Profile, High Power Density, Capable of 500W+**
- **Soft Switching: 99% Peak Efficiency and Low EMI**
- **V_{IN} Max for Voltage Divider (2:1): 72V**
- **V_{IN} Max for Voltage Doubler (1:2)/Inverter (1:1): 36V**
- **Wide Bias V_{CC} Range: 6V to 72V**
- **Soft Startup into Steady State Operation**
- **6.5V to 40V $EXTV_{CC}$ Input for Improved Efficiency**
- Input Current Sensing and Overcurrent Protection
- Wide Operating Frequency Range: 100kHz to 1MHz
- Output Short-Circuit/OV/UV Protections with Programmable Timer and Retry
- Thermally Enhanced 28-Pin 4mm × 5mm QFN Package

APPLICATIONS

- Bus Converters
- High Power Distributed Power Systems
- Communications Systems
- Industrial Applications

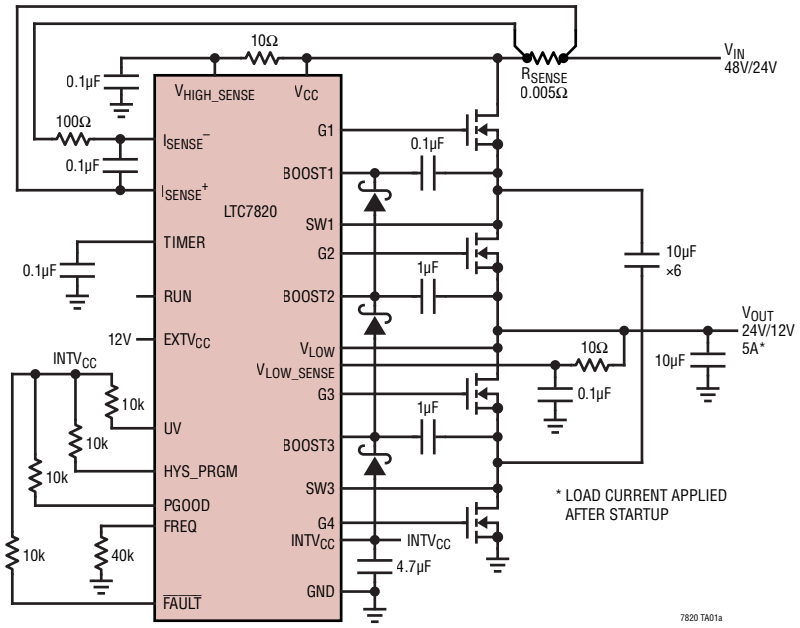
DESCRIPTION

The LTC®7820 is a fixed ratio high voltage high power switched capacitor/charge pump controller. The device includes four N-channel MOSFET gate drivers to drive external power MOSFETs in voltage divider, doubler or inverter configurations. The device achieves a 2:1 step-down ratio from an input voltage as high as 72V, a 1:2 step-up ratio from an input voltage as high as 36V, or a 1:1 inverting ratio from an input voltage up to 36V. Each power MOSFET is switched with 50% duty cycle at a constant pre-programmed switching frequency. System efficiency can be optimized to over 99%. The LTC7820 provides a small and cost effective solution for high power, non-isolated intermediate bus applications with fault protection.

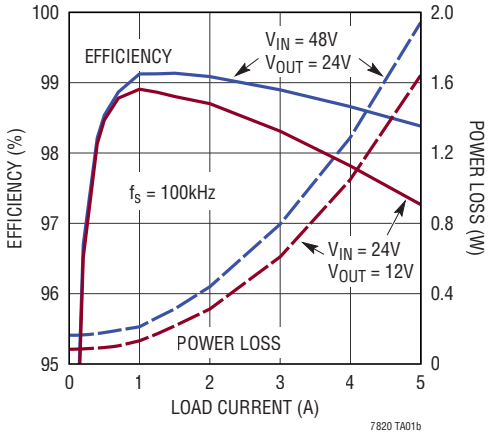
The LTC7820 switching frequency can be linearly programmed from 100kHz to 1MHz. The device is available in a thermally enhanced 28-lead QFN package with some no-connect pins for high voltage compatible pin spacing.

TYPICAL APPLICATION

Very High Efficiency 5A Voltage Divider



Efficiency and Power Loss vs Load Current

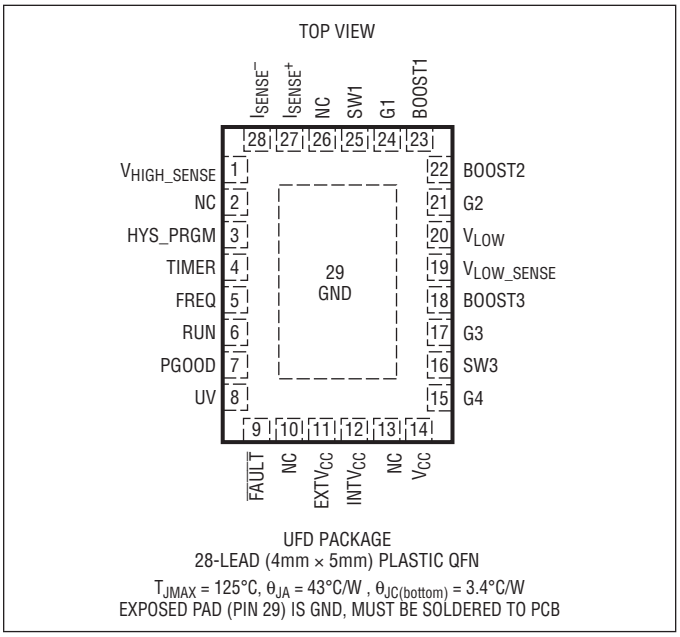


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 3)

V_{CC}, V_{HIGH_SENSE} ..... –0.3V to 80V
BOOST1 ..... –0.3V to 86V
BOOST2, BOOST3 ..... –0.3V to 51V
SW1 ..... –5V to 80V
SW3 ..... –5V to 45V
V_{LOW}, V_{LOW_SENSE} ..... –0.3V to 45V
I_{SENSE}^+, I_{SENSE}^- ..... –0.3V to 80V
(BOOST1 - SW1), (BOOST2 - V_{LOW}) ..... –0.3V to 6V
(BOOST3 - SW3) ..... –0.3V to 6V
$INTV_{CC}$, RUN ..... –0.3V to 6V
$EXTV_{CC}$, PGOOD ..... –0.3V to 45V
HYS_PRGM, FREQ, TIMER, UV ..... –0.3V to $INTV_{CC}$
$\overline{FAULT}$ ..... –0.3V to 80V
$INTV_{CC}$ Peak Current (Note 10) 150mA
Operating Junction Temperature
Range (Notes 2, 11) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W , $\theta_{JC(bottom)}$ = 3.4°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC7820#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7820EUFD#PBF	LTC7820EUFD#TRPBF	7820	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC7820IUFD#PBF	LTC7820IUFD#TRPBF	7820	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = 12V, V_{RUN} = 5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input/Output Voltage							
V_{CC}	IC Bias Voltage Range			6		72	V
V_{VHIGH_SENSE}	V_{HIGH_SENSE} Voltage Range	(Note 6)		0		72	V
V_{VLOW_SENSE}	V_{LOW_SENSE} Voltage Range			0		36	V
V_{VLOW}	V_{LOW} Voltage Range	(Note 5)		0		36	V
I_Q	Input DC Supply Current Shutdown Normal Operation	 V_{RUN} = 0V V_{RUN} = 5V, No Switching			 60 1.5		 µA mA
V_{UVLO}	Undervoltage Lockout Threshold	V_{INTVCC} Falling V_{INTVCC} Rising			4.85 5.05		V V
Overcurrent Protection							
I_{ISENSE^+}	I_{SENSE^+} Pin Current	I_{SENSE^+} = I_{SENSE^-} = 24V			220	350	µA
		Pre-Balance Phase, V_{HIGH_SENSE} = 24V, I_{SENSE^+} = I_{SENSE^-} = 24V, V_{VLOW} = 12V, V_{VLOW_SENSE} = 11V			93		mA
I_{ISENSE^-}	I_{SENSE^-} Pin Current		●	–5	1	5	µA
V_{ISENSE}	Current Limit Threshold (V_{ISNESE^+} – V_{ISENSE^-})		●	45	50	55	mV
Gate Drivers							
$R_{G2,4}$	Pull-Up On-Resistance Pull-Down On-Resistance				2.5 1.5		Ω Ω
$R_{G1,3}$	Pull-Up On-Resistance Pull-Down On-Resistance				2.4 1.1		Ω Ω
G1/G2 t_D	G1 Off to G2 On Delay Time G2 Off to G1 On Delay Time	(Note 4)			50 50		ns ns
G3/G4 t_D	G3 Off to G4 On Delay Time G4 Off to G3 On Delay Time	(Note 4)			60 60		ns ns
G1/G3 t_D	G1 On to G3 On Delay Time G3 Off to G1 Off Delay Time	(Note 4)			5 10		ns ns
G2/G4 t_D	G2 On to G4 On Delay Time G4 Off to G2 Off Delay Time	(Note 4)			5 10		ns ns
RUN Pin							
V_{RUN}	Run Pin On Threshold	V_{RUN} Rising	●	1.1	1.22	1.35	V
$V_{RUN,HYS}$	Run Pin On Hysteresis				80		mV
$INTV_{CC}$ Regulator							
V_{INTVCC_VCC}	$INTV_{CC}$ Voltage No Load	6V < V_{CC} < 72V, V_{EXTVCC} = 0V		5.4	5.6	5.9	V
	$INTV_{CC}$ Load Regulation	I_{CC} = 0 to 60mA, V_{EXTVCC} = 0V			0.8	±2	%
V_{INTVCC_EXT}	$INTV_{CC}$ Voltage No Load with $EXTV_{CC}$	12V < V_{EXTVCC} < 45V (Note 7)		5.4	5.6	5.9	V
	$INTV_{CC}$ Load Regulation with $EXTV_{CC}$	I_{CC} = 0 to 50mA, V_{EXTVCC} = 12V			0.5	±2	%
	$EXTV_{CC}$ Switchover Voltage	V_{EXTVCC} Ramping Positive (Note 9)		6.35	6.5	6.65	V
	$EXTV_{CC}$ HYSTERESIS				400		mV
V_{HIGH_SENSE} and V_{LOW_SENSE}							
R_{VHIGH_SENSE}	V_{HIGH_SENSE} to GND Resistance				1		MΩ
I_{VLOW_SENSE}	V_{LOW_SENSE} Pin Current	V_{CC} = 51V, V_{LOW_SENSE} = 45V			±1	±10	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = 12V, V_{RUN} = 5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{LOW}							
$I_{SOURCEVLOW}$	Source Current to V_{LOW} Pin from I_{SENSE}^+	$I_{SENSE}^+ = V_{HIGH\_SENSE}$ = 24V, V_{LOW_SENSE} = 11V, V_{LOW} = 12V, Timer = 1V			93		mA
$I_{SINKVLOW}$	Sink Current from V_{LOW} Pin to GND	$I_{SENSE}^+ = V_{HIGH\_SENSE}$ = 24V, V_{LOW_SENSE} = 13V, V_{LOW} = 12V, Timer = 1V			50		mA
Oscillator							
f_S	Oscillator Frequency Range			100		1000	kHz
f_{NOM}	Nominal Frequency	V_{FREQ} = 1.02V			500		kHz
I_{FREQ}	FREQ Setting Current	V_{FREQ} = 1.02V (Note 3)		–9.5	–10	–10.5	µA
FAULTB and HYS_PRGM							
$R_{\overline{FAULT}}$	$\overline{FAULT}$ Pull-Down Resistance	$V_{\overline{FAULT}}$ = 0.5V			200	400	Ω
$I_{\overline{FAULT}\_LEAK}$	$\overline{FAULT}$ Leakage Current	$V_{\overline{FAULT}}$ = 80V				±2	µA
I_{HYS_PRGM}	HYS_PRGM Setting Current	V_{HYS_PRGM} = 1V (Note 3)	●	–9.3	–10	–10.7	µA
$V_{VLOW\_SENSE\_\overline{FAULT}}$	V_{LOW_SENSE} Voltage Trigger Fault	V_{VHIGH_SENSE} = 24V, V_{HYS_PRGM} = 0V					
		V_{VLOW_SENSE} Ramp Up	●	12.2	12.3	12.4	V
		V_{VLOW_SENSE} Ramp Down	●	11.6	11.7	11.8	V
		V_{VHIGH_SENSE} = 24V, V_{HYS_PRGM} = 5V					
		V_{VLOW_SENSE} Ramp Up	●	12.7	12.8	12.9	V
		V_{VLOW_SENSE} Ramp Down	●	11.1	11.2	11.3	V
		V_{VHIGH_SENSE} = 24V, V_{HYS_PRGM} = 2.4V					
		V_{VLOW_SENSE} Ramp Up	●	14.15	14.3	14.45	V
		V_{VLOW_SENSE} Ramp Down	●	9.5	9.65	9.8	V
UV Comparator and PGOOD							
V_{UVTH}	UV Pin Comparator Threshold	UV Pin Voltage Rising		0.985	1.01	1.035	V
V_{UVHYS}	Undervoltage Hysteresis				120		mV
R_{PGOOD}	PGOOD Pull-Down Resistance	V_{PGOOD} = 0.5V			150	300	Ω
I_{PGOOD_LEAK}	PGOOD Leakage Current	V_{PGOOD} = 45V				±1	µA
Timer							
I_{TIMER}	Timer Pin Current	V_{TIMER} < 0.5V or V_{TIMER} > 1.2V (Note 3)			–3.5		µA
		0.5V < V_{TIMER} < 1.2V (Note 3)			–7		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7820 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7820E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7820I is guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$T_J = T_A + (P_D \bullet 43°C/W)$.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Delay times are measured using 50% levels with SW3 = V_{LOW} = 6V, SW1 = 12V.

Note 5: The maximum output operating voltage for divider applications is 36V, the maximum input operating voltage for doubler applications is 36V.

Note 6: The maximum input operating voltage for divider applications is 72V, the maximum output operating voltage for doubler applications is 72V.

Note 7: When V_{CC} > 15V, $EXTV_{CC}$ lower than V_{CC} is recommended to improve efficiency and reduce IC Temperature.

Note 8: All the voltage is referred to the GND pin unless otherwise specified.

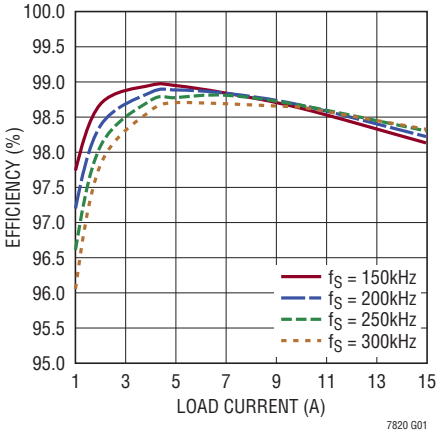
Note 9: $EXTV_{CC}$ is enabled only if V_{CC} is higher than 7V.

Note 10: Guaranteed by design.

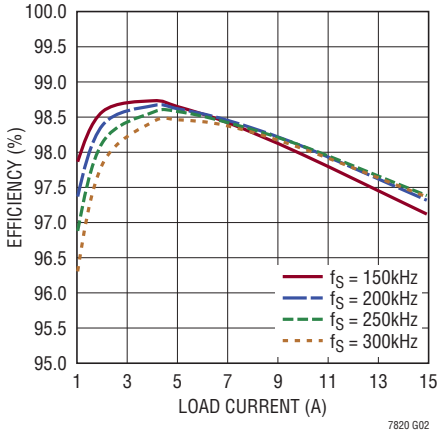
Note 11: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum junction temperature may impair device reliability or permanently damage the device.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

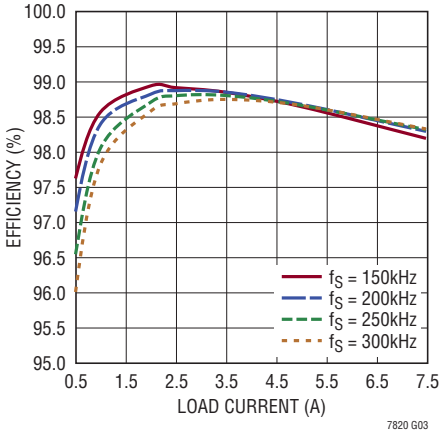
Efficiency vs Load Current 48V to 24V Voltage Divider in Figure 7



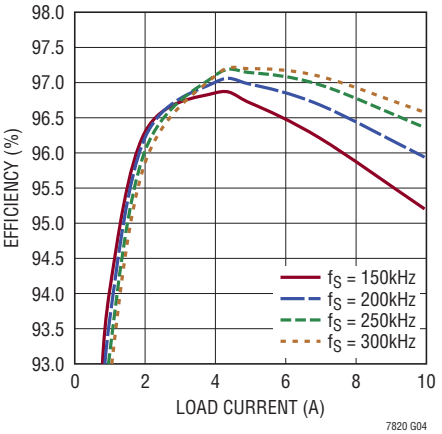
Efficiency vs Load Current 24V to 12V Voltage Divider in Figure 7



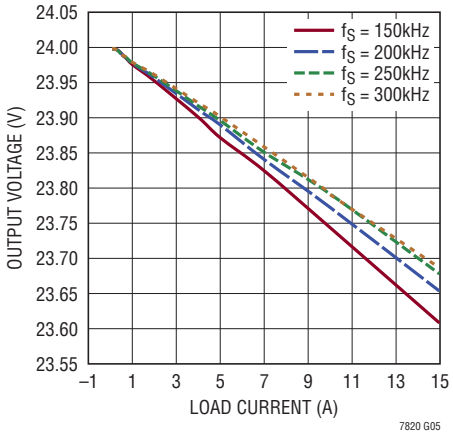
Efficiency vs Load Current 24V to 48V Voltage Doubler in Figure 8



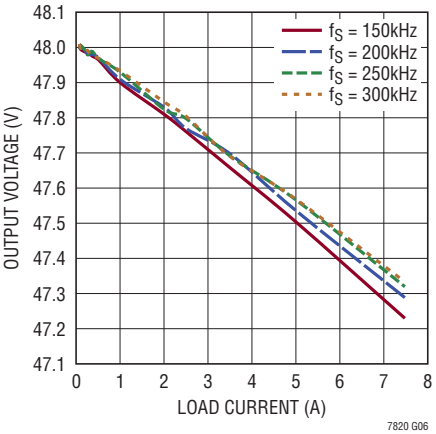
Efficiency vs Load Current 24V to –24V Inverter in Figure 9



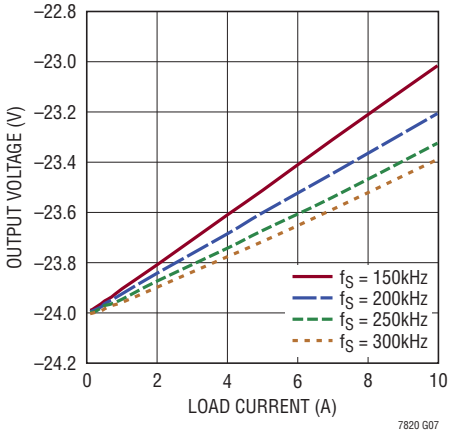
Output Voltage vs Load Current 48V to 24V Voltage Divider in Figure 7



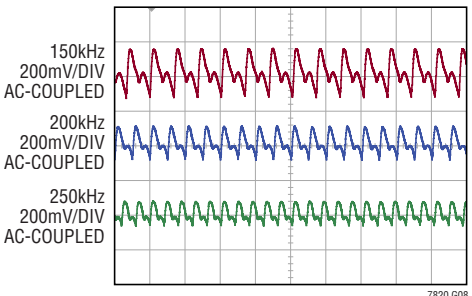
Output Voltage vs Load Current 24V to 48V Voltage Doubler in Figure 8



Output Voltage vs Load Current 24V to –24V Inverter in Figure 9



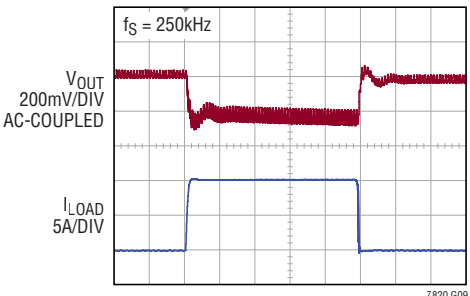
Steady State Output Ripple in Figure 7



V_{IN} = 48V
V_{OUT} = 24V
I_{LOAD} = 10A

10µs/DIV

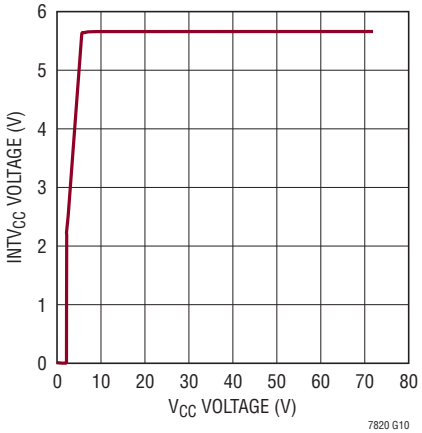
Load Transient 0A-10A-0A 48V to 24V Divider in Figure 7



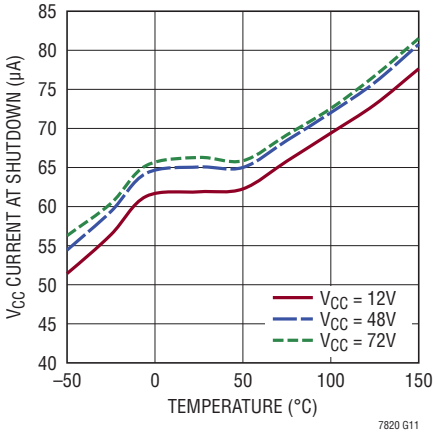
50µs/DIV

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

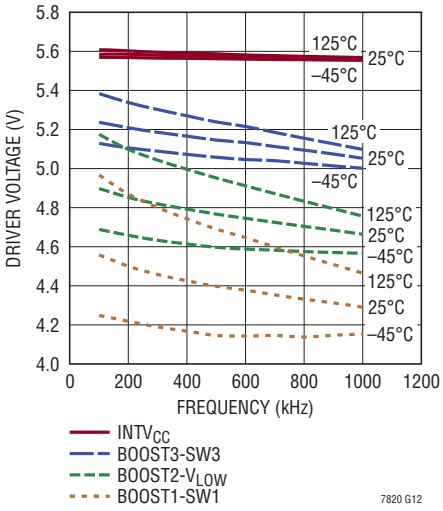
$INTV_{CC}$ Line Regulation



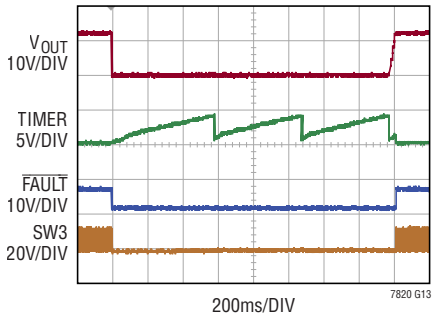
V_{CC} Shutdown Current vs Temperature



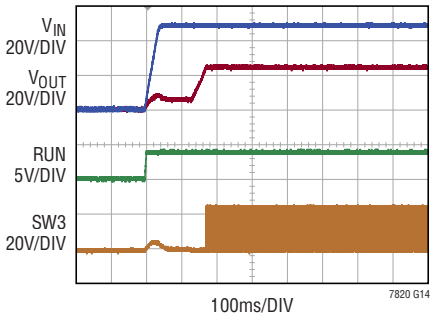
Driver Voltage vs Frequency, in Figure 7



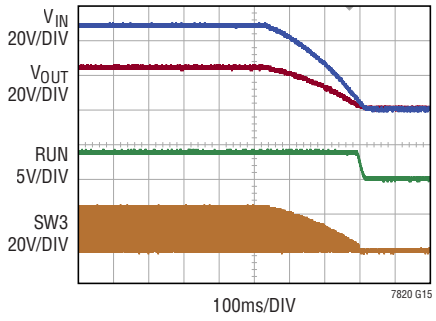
Short-Circuit and Retry 24V to 12V Divider



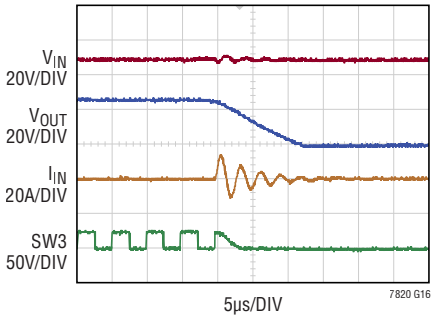
Start-Up 48V to 24V Voltage Divider, RUN Pin FLOAT



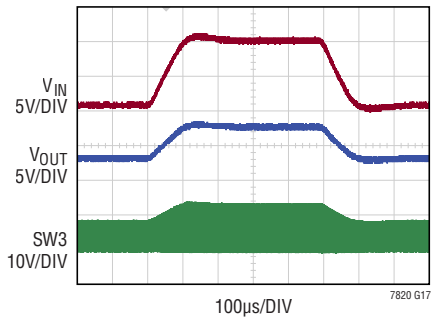
Shutdown 48V to 24V Voltage Divider, RUN Pin FLOAT



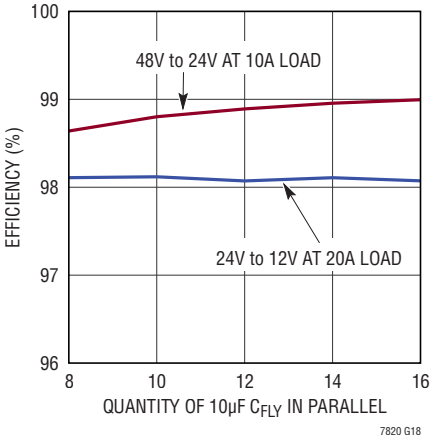
Input Current During Short Circuit 48V to 24V Divider



Voltage Divider Line Transient $t_r = t_f$ = 100µs, f_S = 500kHz



Divider Efficiency vs C_{FLY} in Figure 11



PIN FUNCTIONS

UV (Pin 8): Undervoltage Comparator Input. If the UV pin voltage is lower than 0.9V, the PGOOD pin is pulled down while the controller keeps switching. If the UV pin voltage is higher than 1V and no faults exist, PGOOD pin is released. Connect to $INTV_{CC}$ if not used.

I_{SENSE}^+ (Pin 27): Current Sense Comparator Positive Input. Kelvin connected to the positive node of the current sensing resistor. The current sensing resistor has to be connected to the drain of the very top MOSFET. When the voltage between I_{SENSE}^+ pin and I_{SENSE}^- pin is higher than 50mV, the controller indicates an overcurrent fault by pulling the $\overline{FAULT}$ pin down. The I_{SENSE}^+ pin is also used to source 93mA current to the V_{LOW} pin during the capacitor's pre-balancing time at power-up in voltage divider applications. Connect directly to the drain of the very top MOSFET if not used.

I_{SENSE}^- (Pin 28): Current Sense Comparator Negative Input. Kelvin connected to the negative node of the current sensing resistor. Short to I_{SENSE}^+ if not used.

RUN (Pin 6): Run Control Input. Forcing RUN below 1.14V shuts down the controller. When RUN is higher than 1.22V, internal circuitry starts up. There is a 1µA pull-up current flowing out of RUN pin when the RUN pin voltage is below 1.14V and additional 5µA current flowing out of RUN pin when the Run pin voltage is above 1.22V.

TIMER (Pin 4): Charge Balance and Fault Timer Control Input. A capacitor between this pin and ground sets the amount of time to charge V_{LOW} to $V_{HIGH\_SENSE}/2$ voltage during power-up. It also sets the short-circuit retry time. See the Application Information section for details.

$\overline{FAULT}$ (Pin 9): Open Drain Output Pin. $\overline{FAULT}$ is pulled to ground when the V_{LOW_SENSE} voltage is out of its window thresholds or the voltage between I_{SENSE}^+ and I_{SENSE}^- is higher than 50mV. $\overline{FAULT}$ pin is also pulled to ground under $INTV_{CC}$ UVLO.

PGOOD (Pin 7): Open Drain Output Pin. PGOOD is pulled to ground if there are any faults or if the UV pin indicates an undervoltage condition.

HYS_PRGM (Pin 3): A resistor connected between this pin and ground will program the two thresholds of the window comparator that monitors the voltage difference between $V_{HIGH\_SENSE}/2$ and V_{LOW_SENSE}. There is a 10µA current flowing out of this pin.

G4 (Pin 15): High Current Gate Drive for the Bottom (Synchronous) N-Channel MOSFET. Voltage swing at this pin is from ground to $INTV_{CC}$.

G3 (Pin 17): High Current Gate Drive for the Third Upper Most N-Channel MOSFET. This is the output of the floating driver with a voltage swing from BOOST3 to SW3.

G2 (Pin 21): High Current Gate Drive for the Second Upper most N-Channel MOSFET. This is the output of the floating driver with a voltage swing from BOOST2 to V_{LOW}.

G1 (Pin 24): High Current Gate Drive for the Upper most N-Channel MOSFET. This is the output of the floating driver with a voltage swing from BOOST1 to SW1.

SW1/SW3 (Pin 25/Pin 16): Switch Node Connections.

BOOST1, BOOST2, BOOST3 (Pins 23, 22, 18): Bootstrapped supplies to the floating drivers. Capacitors are connected between these BOOST pins and their respective SWn and V_{LOW} pins.

$EXTV_{CC}$ (Pin 11): External Power Input to $EXTV_{CC}$ LDO. This LDO supplies $INTV_{CC}$ power whenever $EXTV_{CC}$ is higher than 6.5V and V_{CC} is higher than 7V. Do not exceed 40V on this pin.

$INTV_{CC}$ (Pin 12): Output of the Internal Linear Low Dropout Regulator. The driver and control circuits are powered from this voltage source. Must be bypassed to power ground with a minimum of 4.7µF ceramic or other low ESR capacitor.

V_{CC} (Pin 14): Power Supply for Internal Circuitry and $INTV_{CC}$ Linear Regulator. A bypass capacitor should be tied between this pin and the power ground.

V_{HIGH_SENSE} (Pin 1): Kelvin Sensing Input. Monitor the voltage of the drain of the top MOSFET.

PIN FUNCTIONS

V_{LOW} (Pin 20): Half Supply from V_{HIGH_SENSE}. Connect a bypass capacitor from this node to PGND.

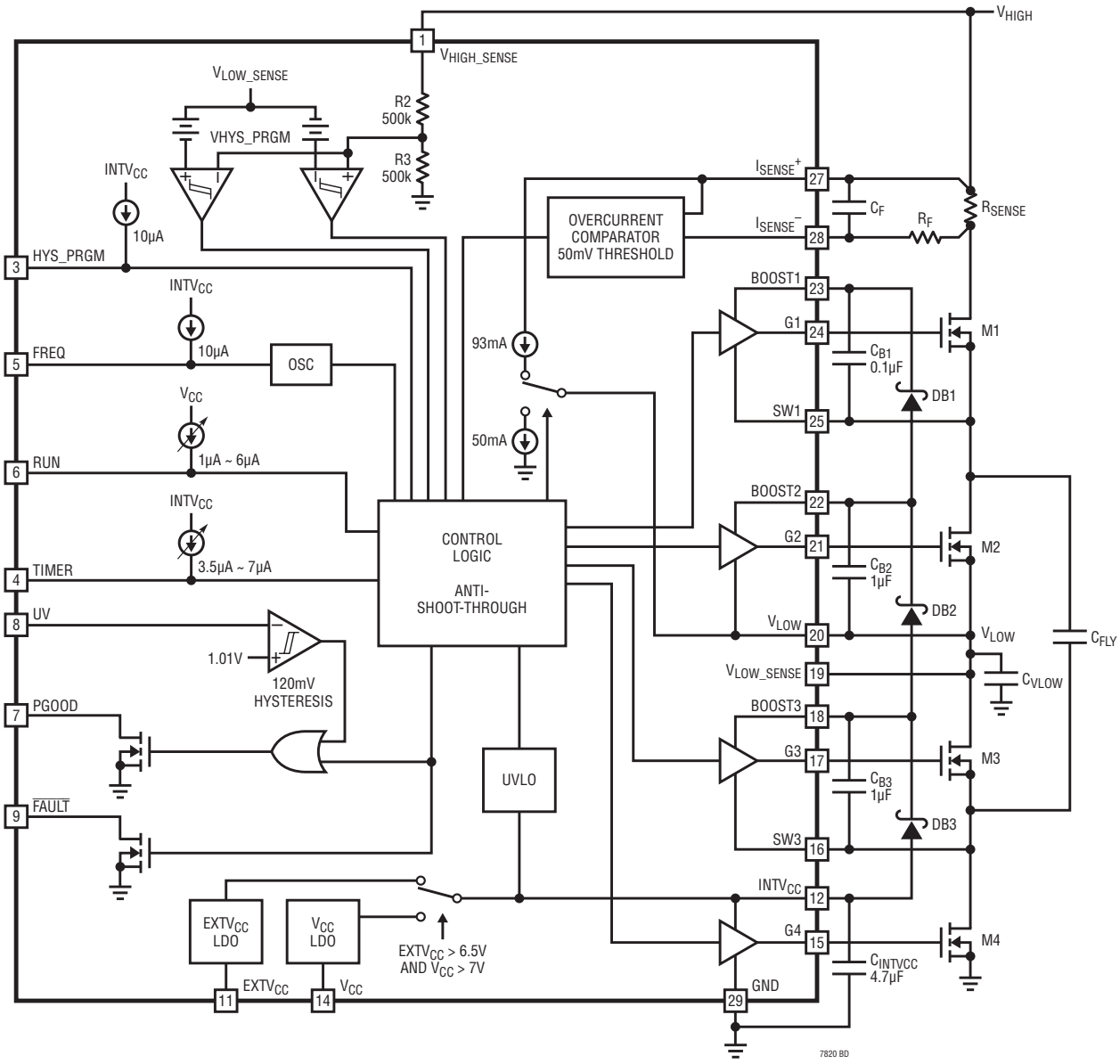
V_{LOW_SENSE} (Pin 19): Kelvin Sensing Input. Monitors the voltage on V_{LOW}.

FREQ (Pin 5): Frequency Set Pin. There is a precision 10µA current flowing out of this pin. A resistor to ground sets a voltage which in turn programs the frequency. See the Applications Information section for detailed information.

NC (Pins 2, 10, 13, 26): No Connection. Always keep these pins floating. These pins are intentionally skipped to isolate adjacent high voltage pins.

GND (Exposed Pad Pin 29): Signal and Power Ground. All small-signal components should connect to this ground, which in turn connects to system power ground at one point. The exposed pad must be soldered to the PCB, providing a local ground for the control components of the IC, which should be tied to system power ground under the IC. For inverter applications, GND should connect to the negative output and all small signal components still referred to GND pin.

BLOCK DIAGRAM



OPERATION

Main Control

The LTC7820 is a constant frequency, open loop switched capacitor/charge pump controller for high power and high voltage applications. Please refer to the Block Diagram for the following discussion on its operation. In steady state operation, the N-channel MOSFETs M1 and M3 are turned on and off in the same phase with around 50% duty cycle at a pre-programmed switching frequency. The N-channel MOSFETs M2 and M4 are turned on and off complementarily to MOSFETs M1 and M3. The gate drive waveforms are shown in Figure 1.

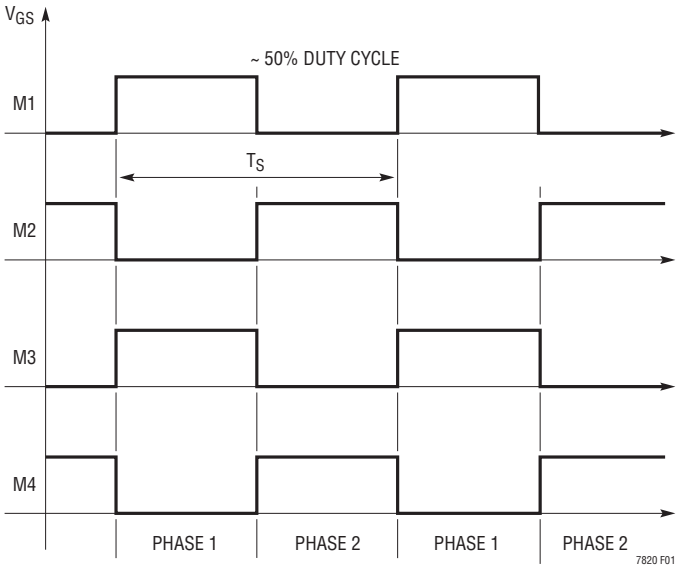


Figure 1. Gate Drive Waveforms

During phase 1, M1 and M3 are on and the flying capacitor C_{FLY} is in series with C_{VLOW}. During phase 2, M2 and M4 are on and C_{FLY} is in parallel with C_{VLOW}. The V_{LOW} pin voltage is always close to half of the top voltage at the drain of MOSFET M1 (refer to GND pin) in steady state, and it is not sensitive to variable loads due to the very low impedance at its output. The LTC7820 does not regulate the output voltage with a closed-loop feedback system. However, it stops switching when fault conditions occur, such as V_{LOW} pin voltage overvoltage or undervoltage, an overcurrent event or an overtemperature protection event.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the quad N-channel MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. Normally an internal 5.5V linear regulator supplies $INTV_{CC}$ power from V_{CC}. If V_{CC} is connected to a high input voltage, an optional external voltage source on the $EXTV_{CC}$ pin enables a second 5.5V linear regulator and supplies $INTV_{CC}$ power from the $EXTV_{CC}$ pin. To enable this more efficient second regulator, V_{CC} needs to be higher than 7V and the $EXTV_{CC}$ pin voltage has to be higher than 6.5V. Do not exceed 40V on the $EXTV_{CC}$ pin. Each top MOSFET driver is biased from the floating bootstrap capacitors C_B, which are normally recharged during each off cycle through an external Schottky diode when the respective top MOSFET turns off.

Start-Up and Shutdown

The LTC7820 is in shutdown mode when the RUN pin is lower than 1.14V. In this mode, most internal circuitry is turned off including the $INTV_{CC}$ regulator and the LTC7820 consumes less than 100µA current. All gates G1/G2/G3/G4 are actively pulled low to turn off the external power MOSFETs in shutdown. Releasing RUN allows an internal 1µA current to pull up this pin and enable the controller. Once the run pin rises above 1.22V, an additional 5µA flows out of this pin. Alternately, the RUN pin may be externally pulled up or driven directly by logic. Do not exceed the Absolute Maximum Rating of 6V on this pin.

After the Run pin is released and the $INTV_{CC}$ voltage passes UVLO, the LTC7820 starts up and monitors the V_{HIGH_SENSE} and V_{LOW_SENSE} voltages continuously. The LTC7820 starts switching only if V_{LOW_SENSE} voltage is close to half of V_{HIGH_SENSE} voltage or both V_{LOW_SENSE} and V_{HIGH_SENSE} voltages are close to GND. In voltage divider applications, V_{LOW} is pre-balanced to half the V_{HIGH_SENSE} voltage and the LTC7820 may start up with capacitors at different initial conditions.

Fault Protection and Thermal Shutdown

The LTC7820 monitors system voltage, current and temperature for faults. It stops switching and pulls down the $\overline{FAULT}$ pin when fault conditions occur. To clear voltage faults, the V_{LOW_SENSE} pin voltage has to be within the

OPERATION

programmed window around half of V_{HIGH_SENSE} voltage or the V_{HIGH_SENSE} and V_{LOW_SENSE} voltages must be lower than 1V and 0.5V respectively. To clear the current fault, the voltage drop from I_{SENSE}^+ pin to I_{SENSE}^- pin has to be lower than 50mV. To clear temperature faults, the IC temperature has to be lower than 165°C.

The $\overline{FAULT}$ pin may be pulled up by external resistors to voltages up to 80V. It can be used to control an external disconnect FET to isolate the input and output during fault conditions.

High Side Current Sensing

For over current protection, the LTC7820 uses a sense resistor R_{SENSE} to monitor the current. The sensing resistor has to be placed at the drain of the very top MOSFET M1. For voltage divider and inverter applications, the current flows into the drain of the MOSFET M1, so the I_{SENSE}^+ pin should be connected to the sensing resistor then to the drain of the MOSFET M1. For voltage doubler applications, the current flows out of the drain of the MOSFET M1, so the I_{SENSE}^+ pin should be connected directly to the drain of the MOSFET M1. See Typical Applications section for examples. In most applications, the current through the sense resistor is a pulse current and the peak value is much higher than the average load current. A RC filter on the I_{SENSE}^- pin, with a time constant lower than the switching frequency, may be used to set the precision average current protection. If overcurrent protection is not desired, short the I_{SENSE}^+ and I_{SENSE}^- pins together and connect them to the drain of the top MOSFET M1 directly.

Frequency Selection

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger capacitance to maintain low output ripple voltage and low output impedance. The FREQ pin can be used to program the controller's operating frequency from 100kHz to 1MHz. There is a precision 10µA current flowing out of the FREQ pin, so the user can program the controller's switching frequency with a single resistor to GND. The voltage on the FREQ pin is equal to the resistance multiplied by 10µA current (e.g. the voltage is 1V with a 100k resistor from the FREQ pin to GND). In the linear region, the switching frequency, f_S, can be estimated based on the equation:

$$f_S\,(kHz) = R_{FREQ}(k\Omega) \bullet 8 - 317kHz$$

Figure 2 also shows the relationship between the voltage on the FREQ pin and switching frequency.

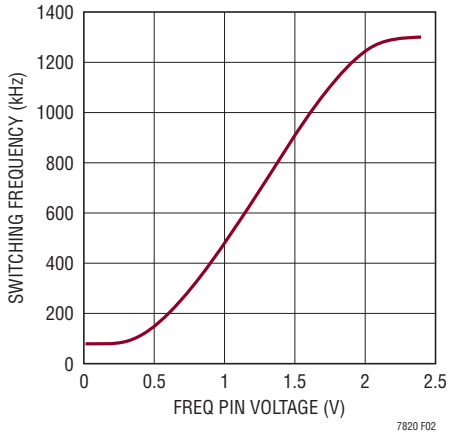


Figure 2. Relationship Between Switching Frequency and Voltage at the FREQ Pin

Power Good and UV (PGOOD and UV pins)

When the UV pin voltage is lower than 1V, the PGOOD pin is pulled low. The PGOOD pin is also pulled low when the RUN pin is low or when the LTC7820 is starting up. The PGOOD pin is released only when the LTC7820 is switching and UV pin is higher than 1V. The PGOOD pin will flag power bad immediately when the UV pin is low. However, there is an internal 20µs power good mask and 120mV hysteresis when UV goes higher than 1V. The PGOOD pin may be pulled up by external resistors to sources up to 45V.

PGOOD signal can be used to enable or disable the output loads. If the loads are switching mode converters or LDOs with ENABLE/RUN pins, this allows easy for interfacing. With proper setup on the UV pin, PGOOD can enable the loads at the output when the output voltage is above a certain value. PGOOD can also be used to control the RUN pin of another LTC7820 if two or more parts are cascaded to achieve higher step-down ratios.

APPLICATIONS INFORMATION

The Typical Application on the first page of this data sheet is a LTC7820 voltage divider circuit. For voltage divider applications, the input voltage is at the drain of very top MOSFET M1 and the output voltage is at the V_{LOW} pin, which is connected to the source of MOSFET M2 and the drain of MOSFET M3. The output voltage is around half of the input voltage in steady state. Alternately, by swapping the input and output voltages, the voltage divider circuit can be transformed into a voltage doubler circuit. For voltage doubler applications, the input voltage is at the V_{LOW} pin while output voltage is available at the drain of the top MOSFET M1 and equals two times the input voltage as shown in Figure 8. Similarly, for inverter applications, the input voltage is applied between the drain of the top MOSFET M1 and V_{LOW}, and the output voltage equals the negative input voltage at the GND pin with respect to the V_{LOW} pin as shown in Figure 9. For divider applications, if the load current is applied before startup or heavy resistive loads are connected to the VLOW pin, the LTC7820 may not start up due to the limited drive ability of the pre-balance circuit. A disconnect FET may be used at the output for soft-start up. For doubler and inverter applications, a disconnect FET may also be required for soft start-up and shutdown. The disconnect FETs in divider/doubler/inverter applications may be also controlled by hot swap controllers to achieve more programmable slew rates and fault protections.

Voltage Divider Pre-Balance before Switching

In voltage divider applications, the V_{LOW_SENSE} voltage should be always close to $V_{HIGH\_SENSE}/2$ in steady state. The voltages across the flying capacitors and V_{LOW} capacitors are close to each other and close to half of the input voltage. The charging inrush current is minimized during each switching cycle because the voltage difference between capacitors is small. However, without special methods such as the LTC7820 pre-charging circuitry, during start-up or fault conditions such as V_{LOW} short to GND, the difference between capacitors can be large and charging currents may be great enough to cause permanent MOSFET damage.

When the power MOSFETs are on, ideally, the inrush charge current,

$$I = \frac{V_{IN} - V_{CFLY} - V_{LOW}}{R_{ON\_M1} + R_{ON\_M3}}$$

when switches M1 and M3 are on and:

$$I = \frac{V_{CFLY} - V_{LOW}}{R_{ON\_M2} + R_{ON\_M4}}$$

when switches M2 and M4 are on. Both currents are limited by the power MOSFET saturation current. With very low $R_{DS(ON)}$ of the external power MOSFETs, the inrush charge current could easily achieve several hundreds of Amperes which can be higher than the MOSFET's Safe Operating Area (SOA).

The LTC7820 provides a proprietary pre-balance method to minimize the inrush charging current in voltage divider applications. The LTC7820 controller detects the V_{LOW_SENSE} pin voltage before switching and compares it with the $V_{HIGH\_SENSE}/2$ internally. If the V_{LOW_SENSE} pin voltage is much lower than the $V_{HIGH\_SENSE}/2$, a current source will source 93mA current to the V_{LOW} pin to pull the V_{LOW} pin up. If the V_{LOW_SENSE} pin voltage is much higher than the $V_{HIGH\_SENSE}/2$, another current source will sink 50mA from V_{LOW} pin to pull the V_{LOW} pin down. If the V_{LOW_SENSE} pin voltage is close to $V_{HIGH\_SENSE}/2$ and within the pre-programmed window, both current sources are disabled and LTC7820 starts switching. If the V_{LOW_SENSE} voltage is still within the window after 36 switching cycles, the $\overline{FAULT}$ pin is released.

For voltage divider with pre-balance startup, the LTC7820 assumes *no load* current or a very small load current (less than 50mA) at the V_{LOW} (output) otherwise the V_{LOW} voltage cannot reach $V_{HIGH\_SENSE}/2$ and the LTC7820 never starts up. This no load condition can be achieved by connecting the $\overline{FAULT}$ pin to the enable pins of the following electrical loads such as switching regulators and LDOs. If load current cannot be controlled off such as resistive loads, a disconnect FET is required to disconnect the load during startup as shown in the typical applications.

APPLICATIONS INFORMATION

If the LTC7820 divider input voltage is controlled by a front end supply or hot swap controller and ramps up slowly, the LTC7820 capacitor voltages are naturally balanced. In this case the pre-balance and no load start-up requirements are not necessary.

Voltage Doubler and Inverter Startup and Disconnect

In voltage doubler and inverter applications, LTC7820 can startup without capacitor inrush charging current if the input voltage is ramping slowly up from zero. As long as the input voltage ramps up slow (in milliseconds), the output voltage can track the input voltage and the voltage difference between capacitors are always small resulting in no huge inrush currents. The slew rate control of the input voltage can be achieved by using a disconnect FET at input or using hot swap controllers as shown in the typical application section. Different from voltage dividers, the voltage doubler and inverter applications have to start up from zero input voltage every time, but they can start up with heavy load currents directly.

Note that voltage divider applications can also startup with a slow ramping input voltage from zero to the steady state operation if there is a hot swap in front of the LTC7820, (pre-balance is not required).

Overcurrent Protection

The LTC7820 provides overcurrent protection through a sensing resistor placed on the high voltage side. A precision rail to rail comparator monitors the differential voltage between the I_{SENSE}^+ pin and the I_{SENSE}^- pin which are Kelvin connected to a sensing resistor. Whenever the I_{SENSE}^+ pin voltage is 50mV higher than the I_{SENSE}^- pin voltage, an over current fault is triggered and the $\overline{FAULT}$ pin is pulled down to ground. At the same time the LTC7820 stops switching and starts retry mode based on the timer pin setup. The overcurrent fault will be cleared when the timer pin voltage reaches 4V and the voltage across the sensing resistor is less than 50mV. The current through the sensing resistor is a pulse current during charging/discharging of the flying capacitors, which may result a voltage higher than the 50mV threshold at heavy loads. To prevent the inrush current from falsely triggering the overcurrent protection, an RC filter is required at the I_{SENSE}^+ pin and I_{SENSE}^-. The RC filter timer constant has to be larger than a switching period. Typically a 100Ω and 0.1µF filter is good for most of applications. Due to the current flowing into the I_{SENSE}^+ pin, the resistor of the RC filter has to be placed at the I_{SENSE}^- pin. I_{SENSE}^+ pin needs to be connected to the sensing resistor directly. The current limit can be selected by choosing different sense resistor values. For example, the 10mΩ sense resistor sets current limit at 50mV/10mΩ = 5A ideally. Due to the switching ripple, the actual current limit is always lower than the ideal case. In real circuits, the current limit is around 4.2A with 0.1µF/100Ω filter and 200kHz switching frequency. The LTspice® simulation tool can be used to quantify the switching ripple.

The overcurrent protection can also be used in doubler and inverter applications for overcurrent and short-circuit conditions at both startup and steady state operation. If over current protection is not used, short the I_{SENSE}^+ pin and the I_{SENSE}^- pin together and connect them to the drain of the top MOSFET M1.

Window Comparator Programming

In normal operation, V_{LOW_SENSE} voltage should be always close to half of the V_{HIGH_SENSE} voltage. A floating window comparator monitors the voltage on the V_{LOW_SENSE} pin and compares it with $V_{HIGH\_SENSE}/2$. The hysteresis window voltage can be programmed and is equal to the voltage at the HYS_PRGM pin. There is a precision 10µA current flowing out of HYS_PRGM pin. A single resistor from HYS_PRGM pin to GND sets the HYS_PRGM pin voltage, which equals the resistor value multiplied by 10µA current (e.g. the voltage is 1V with a 100k resistor from the HYS_PRGM pin to GND). With a 100k resistor on the HYS_PRGM pin, the $V_{HIGH\_SENSE}/2$ voltage has to be within a (V_{LOW_SENSE} ±1V) window during startup and normal operation, otherwise a fault is triggered and the LTC7820 stops switching.

APPLICATIONS INFORMATION

The hysteresis window voltage can be linearly programmed from 0.3V to 2.4V as shown in Figure 3 with different resistor values on the HYS_PRGM pin. If the HYS_PRGM pin is tied to $INTV_{CC}$, a default 0.8V hysteresis window is applied internally. The hysteresis window voltage has to be programmed large enough to tolerate the V_{LOW} pin voltage ripple and voltage drop at maximum load conditions.

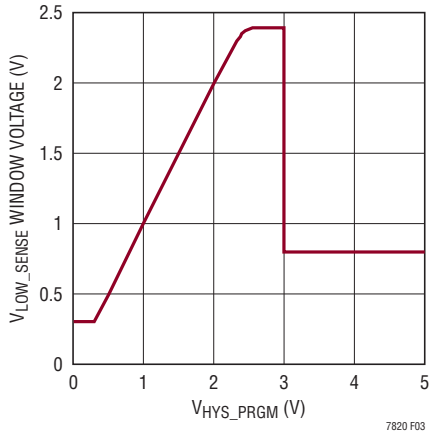


Figure 3. Relationship Between HYS_PRGM Pin Voltage and V_{LOW_SENSE} Window Comparator Voltage

During an input line transient, as long as the change of the input voltage in each switching cycle is less than the window hysteresis voltage, LTC7820 keeps switching and the output voltage tracks the input voltage cycle by cycle. If the input voltage step is large enough to force V_{LOW_SENSE} out of the window within one switching period, a fault is triggered. The LTC7820 stops switching and starts its retry sequence based on the TIMER pin setup.

To make the window comparator work precisely, V_{HIGH_SENSE} and V_{LOW_SENSE} pins are provided for Kelvin connection to the capacitor at the drain of the top MOSFET M1 and the capacitors from V_{LOW} to GND respectively. Small RC filters may be used on these two pins to reject noise higher than the switching frequency.

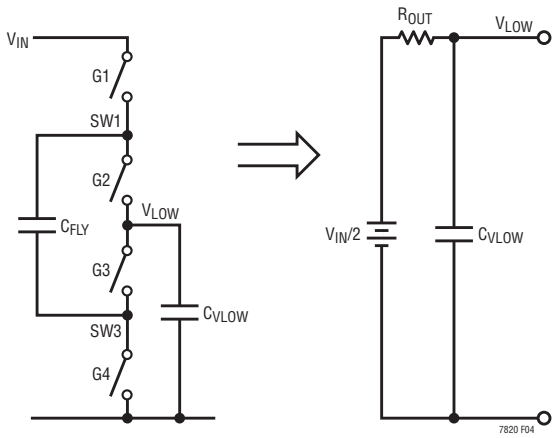


Figure 4. Thevenin Equivalent Circuit of Voltage Divider

Effective Open Loop Output Resistance and Load Regulation

The LTC7820 does not regulate the output voltage through a closed loop feedback system. However, the output voltage is not sensitive to load conditions due to the low output resistance when it is operating with large flying capacitors and high switching frequency. The Thevenin equivalent circuit of voltage divider circuit is shown in the Figure 4.

When duty cycle is around 50%,

$$R_{OUT} = \frac{1+e^{-\frac{1}{4f_S R_{DS(ON)} C_{FLY}}}}{4f_S C_{FLY}\left(1-e^{-\frac{1}{4f_S R_{DS(ON)} C_{FLY}}}\right)}$$

where:

f_S is the switching frequency

C_{FLY} is the flying capacitor

$R_{DS(ON)}$ is the on resistance of one MOSFET (G1 to G4)

APPLICATIONS INFORMATION

At low switching frequencies, $R_{OUT} = 1/(4f_SC_{FLY})$. As frequency increases, R_{OUT} finally approaches $2R_{DS(ON)}$. In high power applications, it is suggested to select the switching frequency around $1/(16C_{FLY}R_{DS(ON)})$ or higher for decent load regulation and efficiency. At heavy load conditions, the output voltage will drop from $V_{IN}/2$ by $R_{OUT} \bullet I_{LOAD}$. In many applications, multi-layer ceramic capacitors (MLCC) are selected as flying capacitors. The voltage coefficients of MLCC capacitors strongly depend on the type and size of capacitors. Normally larger size X7R MLCC capacitors are better than X5R in terms of voltage coefficient. The capacitance still drops 20% to 30% with high DC bias voltage. Capacitance derating needs to be considered when estimating the output resistance of these switched capacitor circuits.

$INTV_{CC}$ Regulators and $EXTV_{CC}$

The LTC7820 features an internal PMOS LDO that supplies power to $INTV_{CC}$ from the V_{CC} supply. $INTV_{CC}$ powers the gate drivers and most of the LTC7820's internal circuitry. The linear regulator regulates the voltage at the $INTV_{CC}$ pin to 5.5V when V_{CC} is greater than 6V. $EXTV_{CC}$ connects to $INTV_{CC}$ through another PMOS LDO and can supply the needed power when its voltage is higher than 6.5V and V_{CC} is higher than 7V. Each of these can supply a peak current of 150mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and GND pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC7820 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, may be supplied by either the 5.5V linear regulator from V_{CC} or the linear regulator from $EXTV_{CC}$. When the voltage on the $EXTV_{CC}$ pin is less than 6.5V, the linear regulator from V_{CC} is enabled. Power dissipation for the IC in this case is highest and is equal to $V_{CC} \bullet I_{INTVCC}$. The gate charge current is dependent on operating frequency. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics.

For example, the LTC7820 $INTV_{CC}$ current is limited to less than 27mA from a 48V supply in the UFD package and not using the $EXTV_{CC}$ supply:

$$T_J = 70°C + (27mA)(48V)(43°C/W) = 125°C$$

Where ambient temperature is 70°C and thermal resistance from junction to ambient is 43°C/W

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating at maximum V_{IN}. When the voltage applied to $EXTV_{CC}$ rises above 6.5V and V_{CC} above 7V, the $INTV_{CC}$ linear regulator is turned off and the $EXTV_{CC}$ linear regulator is turned on. Using the $EXTV_{CC}$ allows the MOSFET driver and control power to be derived from other high efficiency sources such as the V_{LOW} pin of a 48V to 24V voltage divider or other voltage rails in the system. Using $EXTV_{CC}$ can significantly reduce the IC temperature in high V_{IN} applications. Tying $EXTV_{CC}$ to the output (24V) reduces the junction temperature in the previous example to:

$$T_J = 70°C + (27mA)\ (24V)\ (43°C/W)$$

$$= 98°C$$

Do not apply more than 40V to the $EXTV_{CC}$ pin.

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitors $C_{B1}/C_{B2}/C_{B3}$ in the Block Diagram, connected to the BOOST pins, supply the gate drive voltages for the top side MOSFETs M1/M2/M3. Capacitor C_{B3} in the Block Diagram is charged though external Schottky diode D_{B3} from $INTV_{CC}$ when the SW3 pin is low. Capacitor C_{B2} is charged through D_{B2} from BOOST3 when the SW3 pin is high. Capacitor C_{B1} is charged through D_{B1} from BOOST2 when the SW1 pin is low. When the MOSFETs M1/M2/M3 are to be turned on, the driver places the $C_{B1}/C_{B2}/C_{B3}$ voltage across the gate source of the MOSFETs M1/M2/M3. This enhances the MOSFETs and turns them on. The switch node voltage, SW1/SW3, rises to I_{SENSE}^+/V_{LOW} and the BOOST pin follows. With continuous switching, the gate driver voltages on $C_{B1}/C_{B2}/C_{B3}$ are:

$$V_{CB3} = V_{INTVCC} - V_{DB3}$$

$$V_{CB2} = V_{INTVCC} - V_{DB3} - V_{DB2}$$

$$V_{CB1} = V_{INTVCC} - V_{DB3} - V_{DB2} - V_{DB1}$$

APPLICATIONS INFORMATION

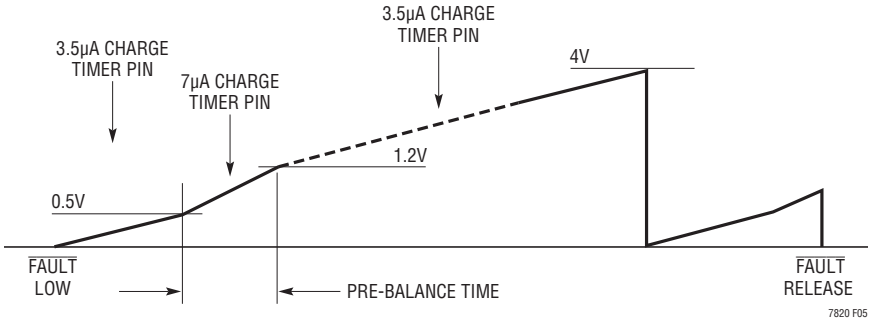


Figure 5. Timer Behavior During Fault or Startup

The value of the boost capacitors, $C_{B1}/C_{B2}/C_{B3}$, needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The standard 6.3V MLCC ceramic capacitors are good for $C_{B1}/C_{B2}/C_{B3}$. The reverse breakdown of the external Schottky diodes must be greater than the maximum operation voltage between the V_{LOW} and GND pins. When adjusting the gate drive level, the final arbiter is the threshold voltage of the top MOSFET M1. The Top driver voltage V_{CB1} has to be higher than the top FET M1 threshold voltage in all conditions. Logic level MOSFET should be used, otherwise lower operating switching frequency and lower forward voltage drop diodes are necessary to raise the gate driver voltages.

Undervoltage Lockout

The LTC7820 has a precision UVLO comparator constantly monitoring the $INTV_{CC}$ voltage to ensure that an adequate gate-drive voltage is present. It locks out the switching action when $INTV_{CC}$ is below 4.9V. To prevent oscillation when there is a disturbance on $INTV_{CC}$, the UVLO comparator has 200mV of precision hysteresis.

Another way to detect an undervoltage condition is to monitor the input supply. Because the RUN pin has a precision turn-on reference of 1.22V, one can use a resistor divider to the input to turn on the IC when the input voltage is high enough. An extra 5µA of current flows out of the RUN pin once the RUN pin voltage passes 1.22V. One can program the hysteresis of the RUN comparator by adjusting the values of the resistive divider.

Fault Response and Timer Programming

The LTC7820 stops switching and pulls the $\overline{FAULT}$ pin low during fault conditions. A capacitor connected from the TIMER pin to GND sets the retry time to start-up if fault conditions are removed. A typical waveform on the TIMER pin during a fault condition is shown in Figure 5.

After the $\overline{FAULT}$ pin is pulled low, a 3.5µA pull-up current flows out of TIMER pin and starts to charge the Timer capacitor. The pull-up current increases to 7µA when the TIMER pin voltage is higher than 0.5V and back to 3.5µA when the TIMER pin voltage is higher than 1.2V. The TIMER pin will be strongly pulled down whenever the fault conditions are removed or the TIMER pin voltage is higher than 4V. When the TIMER pin voltage is between 0.5V and 1.2V, the internal pre-balance circuit will source or sink current to the V_{LOW} pin and regulate the V_{LOW} pin to $V_{HIGH\_SENSE}/2$ with around 93mA/50mA capability. The pre-balance time can be calculated based on the capacitor C_{TIMER} on the TIMER pin:

$$T_{PRE\text{-}BALANCE} = C_{TIMER} \bullet 0.7V/7\mu A$$

So the pre-balance time is 100ms/µF (e.g. the pre-balance time is 10ms with 0.1µF C_{TIMER}).

For voltage divider applications, the output capacitors and the flying capacitors are pre-balanced to half of the input voltage during the startup. Assuming zero initial conditions, the time to charge the capacitors, t_{CHARGE}, can be estimated from the equation:

$$t_{CHARGE} = (C_{OUT} + C_{FLY}) \bullet V_{IN}/2/93mA$$

APPLICATIONS INFORMATION

Select the C_{TIMER} such that the $t_{CHARGE} < t_{PRE\text{-}BALANCE}$. If the flying capacitor C_{FLY} and the output capacitor are very large and input voltage is high, it may take several pre-balance time periods to pre-balance the V_{LOW} pin to $V_{HIGH\_SENSE}/2$ with a fixed C_{TIMER}. A longer start-up time is expected. If there is a resistive load on the output, the load current needs to be smaller than 93mA and still meet $t_{CHARGE} = (C_{OUT} + C_{FLY}) \bullet V_{IN}/2/(93mA - I_{LOAD}) < t_{PRE\text{-}BALANCE}$. Otherwise a disconnect FET may be required to disconnect the load during startup.

Input/Output Capacitor and Flying Capacitor Selection

In high power switched capacitor applications, large AC currents flow through the flying capacitors and input/output capacitors. Low ESR ceramic capacitors are highly recommended for high power switch capacitor applications. Make sure the maximum RMS capacitor current is within the spec; or higher RMS current rated capacitors are preferred. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose capacitors rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design.

The RMS current on the flying capacitors depends on their capacitance and the switching frequency. Higher capacitance and higher switching frequency results in lower RMS current. For a good trade-off between efficiency and power density, the RMS current on the flying capacitors should be lower than 140% of the maximum load current. If there are N identical flying capacitors in parallel, the maximum RMS current through each capacitor is:

$$I_{RMS\_CFLY} = I_{OUT(MAX)} \bullet 140\%/N$$

The input capacitor RMS current is approximately half of the load current. The input capacitor has to be selected to accommodate the maximum load conditions. LTspice simulation tool can be used to quantify the RMS current.

Power MOSFETs and Schottky Diodes Selection

Four external N-channel MOSFETs must be selected for each LTC7820 controller. Four internal gate drivers are designed to drive the MOSFETs. The driver voltages are decided by the $INTV_{CC}$ voltage, schottky diodes forward voltage drop and switching frequency. The lowest driver voltage is the top MOSFET M1 drive voltage running at high switching frequency and cold temperature. It is normally around 4.2V. Consequently, logic-level threshold MOSFETs must be used in most applications. Be aware that the threshold voltage of some logic-level MOSFET varies with temperature. If switching frequency is high and temperature range is wide for specific applications, the top driver voltage of MOSFET M1 may be as low as 4V, and sub-logic level threshold MOSFETs ($V_{GS(TH)} < 3V$) should be used. Selection criteria for the power MOSFETs also include the on-resistance $R_{DS(ON)}$, output capacitance C_{OSS}, input voltage, and maximum output current. Generally, low $R_{DS(ON)}$ and low C_{OSS} MOSFETs are preferred in switched capacitor applications since they will minimize both conduction loss and switching loss. For a given input and output voltage, the uppermost MOSFET M1 always sees high voltage during start-up and shutdown. The Drain to Source voltage of M1 has to be high enough to survive at full input voltage range. Other MOSFETs normally only see half of the input voltage, so the breakdown voltage of M2/M3/M4 can be lower than M1 to optimize $R_{DS(ON)}$ and C_{OSS}. If the reliability of M1 is a major concern, the same high voltage MOSFETs could also be used as M2/M3/M4 to protect against M1 short conditions.

External schottky diodes are needed for the bootstrap circuits, and provide voltage for the floating drivers. To minimize the voltage drop on the top gate driver, low forward voltage drop schottky diodes are preferred with load current in the range of 10mA to 50mA. The reverse breakdown voltage of the diodes should be high enough to survive at the maximum operation voltage between the V_{LOW} and GND pins.

APPLICATIONS INFORMATION

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

1. Are the top 2 N-channel MOSFETs M1 and M2 located within 1cm of each other? Are the bottom 2 N-channel MOSFETs M3 and M4 located within 1cm of each other?
2. Is the exposed GND pad solid connected to the source of bottom MOSFET M4 and the negative terminal of C_{VLOW} capacitors? In divider and doubler applications, a solid ground plane is preferred for noise and thermal improvement.
3. Are the I_{SENSE}^+ and I_{SENSE}^- leads routed together with minimum PC trace spacing? The filter capacitor between I_{SENSE}^+ and I_{SENSE}^- should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor.
4. Is the $INTV_{CC}$ bypassing capacitor connected close to the IC, between the $INTV_{CC}$ and the ground plane? This capacitor carries the MOSFET drivers current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and GND can substantially improve noise performance.
5. Keep the switching nodes (SW1, SW3), top gate nodes (G1, G2, G3), and boost nodes (BOOST1, BOOST3) away from sensitive small-signal nodes. All of these nodes have very large and fast moving signals and therefore should be kept on the output side of the LTC7820 and occupy minimum PC trace area.
6. Use a modified star ground technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ bypass capacitor.

   Figure 6 illustrates the high current paths requiring thick and wide copper trace connection. Refer to demo boards on www.linear.com/demo for PCB layout examples.

PC Board Layout Debugging

Start with one controller at a time. Monitor the switching nodes (SW1/SW3 pin) and probe the V_{LOW} voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the full input voltage range down to dropout.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, G1/2/3/4 connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, Schottky and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the GND pin of the IC.

APPLICATIONS INFORMATION

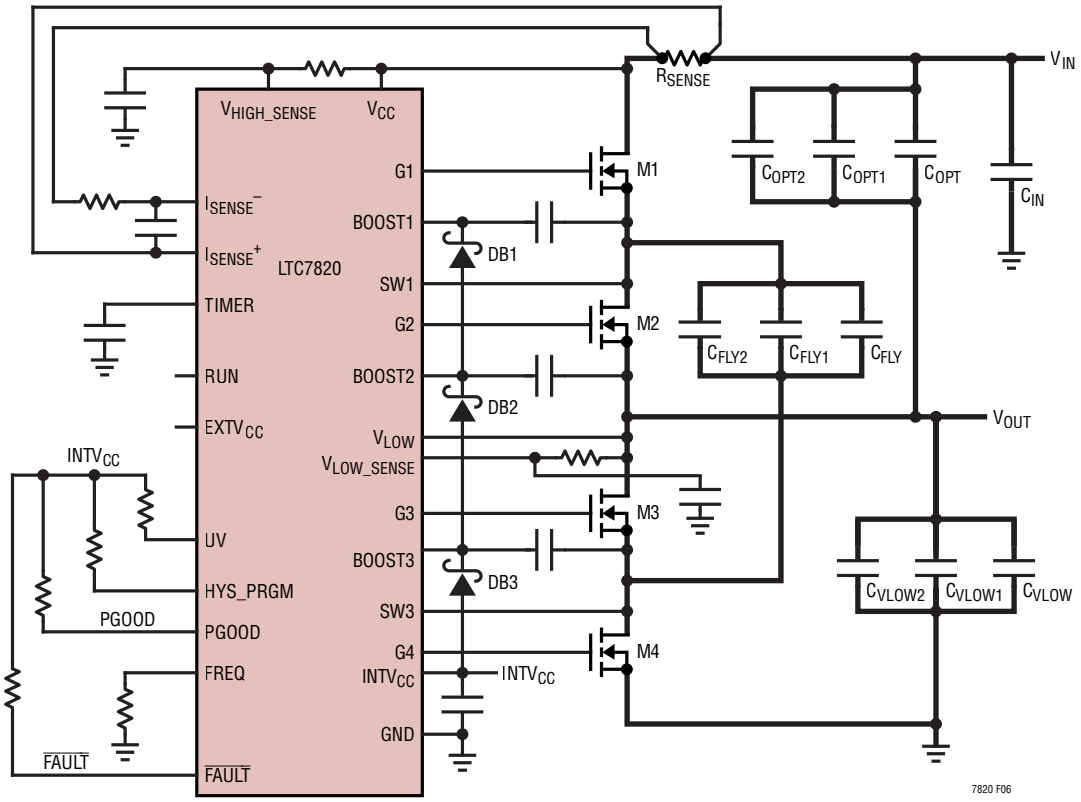


Figure 6. High Current Path in Printed Circuit Board Layout Diagram

APPLICATIONS INFORMATION

Design Example

As a design example using LTC7820 for a high voltage high power voltage divider, assume V_{IN} = 48V (nominal), V_{IN} = 55V (maximum), V_{OUT} = 24V (nominal), I_{OUT} = 15A (maximum).

For high power and high voltage applications, always start with a low switching frequency e.g. 200kHz to minimize the switching losses. To set the 200kHz switching frequency, a 60.4k/1% resistor is connected from Freq pin to ground.

Setting the C_{FLY} voltage ripple to be 2% of the output voltage is a good starting point with trade-off between efficiency and power density. The C_{FLY} can be calculated based on the equation below:

$$C_{FLY} = \frac{I_{OUT(MAX)}}{2 f_S V_{CFLY(RIPPLE)}} = \frac{15A}{2 \bullet 200kHz \bullet 0.48V}$$
$$= 78.125\mu F$$

Considering the ceramic capacitance derating at 24V DC bias voltage, 16 of 10µF/X7R/50V ceramic capacitors are paralleled as flying capacitors. The worst case RMS current may be 40% higher than the maximum output current. So the worst case RMS on each capacitor can be estimated by this equation:

$$I_{RMS(MAX)} = \frac{I_{OUT(MAX)} \bullet 140\%}{N} = \frac{15A \bullet 140\%}{16} = 1.3125A$$

where N is the number of flying capacitors. Double check and make sure the RMS current on each capacitor is below the ripple current ratings and temperature rise is below the limits.

The output capacitor selection is similar to the flying capacitor selection. More output capacitors resulting smaller output voltage ripple. Because of the lower RMS current, the output capacitor value can be much less than the flying capacitor. Some of the capacitors may be connected between input and output to serve as input/output capacitors at the same time, as shown in Figure 6. However the voltage rating of those capacitors has to be selected based on the input voltage instead of the output voltage.

For MOSFET selection, the top MOSFET M1 drain to source voltage has to be higher than the maximum input voltage, while the other three MOSFETs drain to source voltage only needs to be higher than half of the maximum input voltage. Since logic level FETs are preferred, an Infineon BSC100N06LS is chosen as the top MOSFET M1 and BSC032N04LS are used as M2/3/4. Based on the output resistance equation in the application section, the output resistance is around 20mΩ, which will result 300mV drop at the 24V output at 15A load current. In reality, due to the finite dead time and parasitic resistance on the PCB, the voltage drop may be higher than the calculated value. Taking into account the output voltage ripple, a window comparator with ±1V programmed hysteresis is used to monitor the output voltage and compares it with the half of the input voltage during operation. To set the 1V hysteresis, a 100k/1% resistor is connected from HYS_PRGM pin to ground.

TYPICAL APPLICATIONS

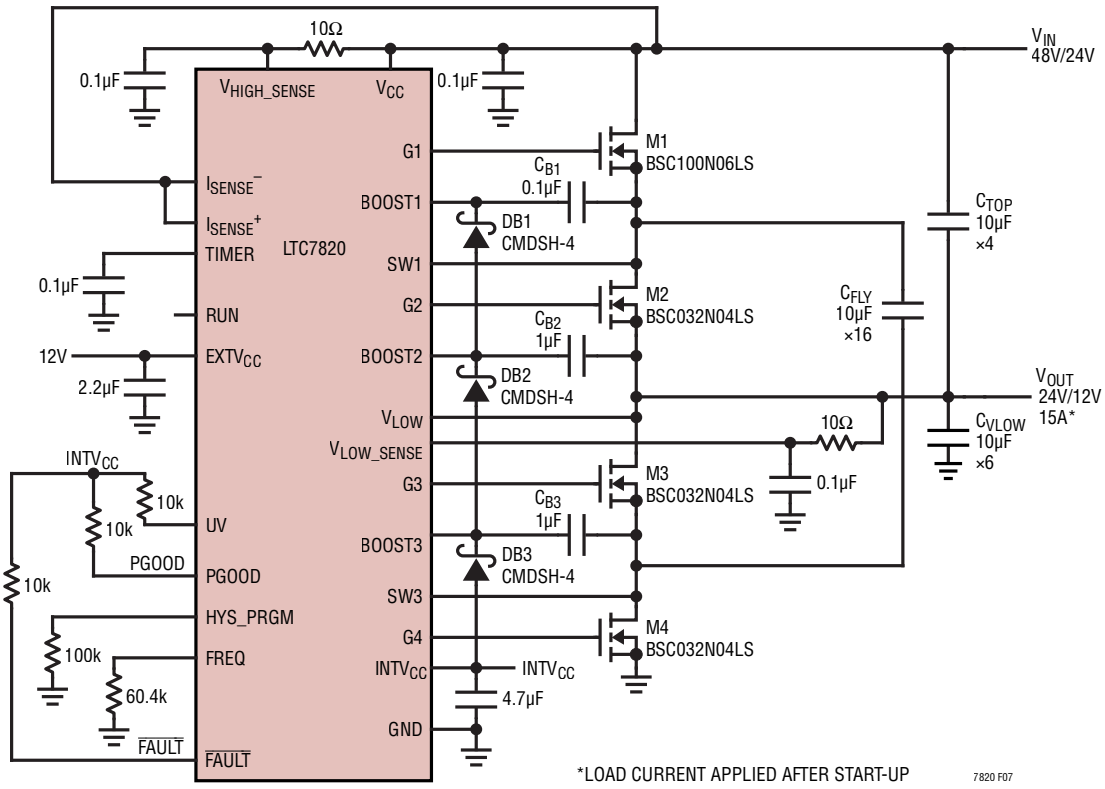


Figure 7. High Efficiency 48V/24V to 24V/12V, 15A Voltage Divider

TYPICAL APPLICATIONS

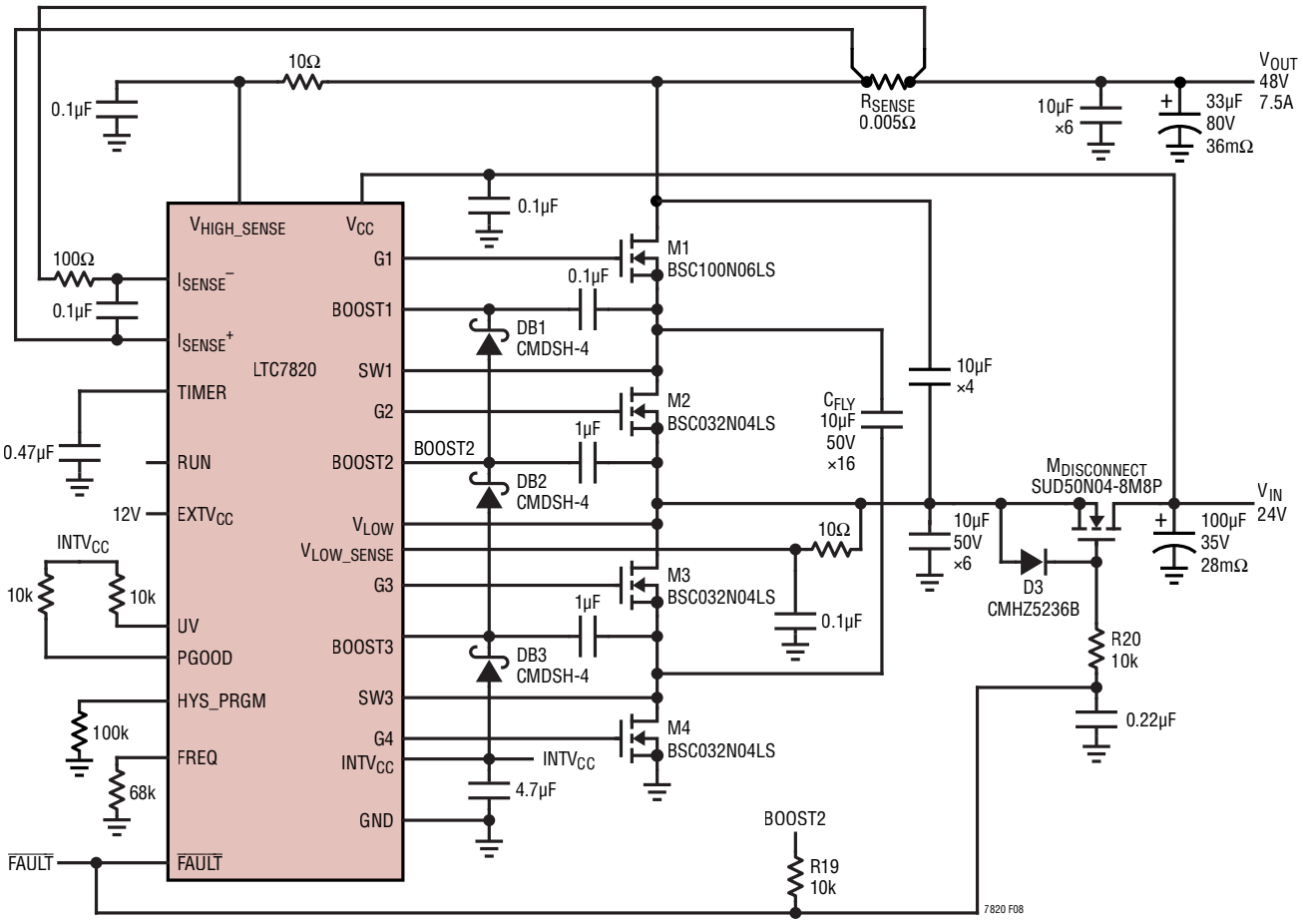
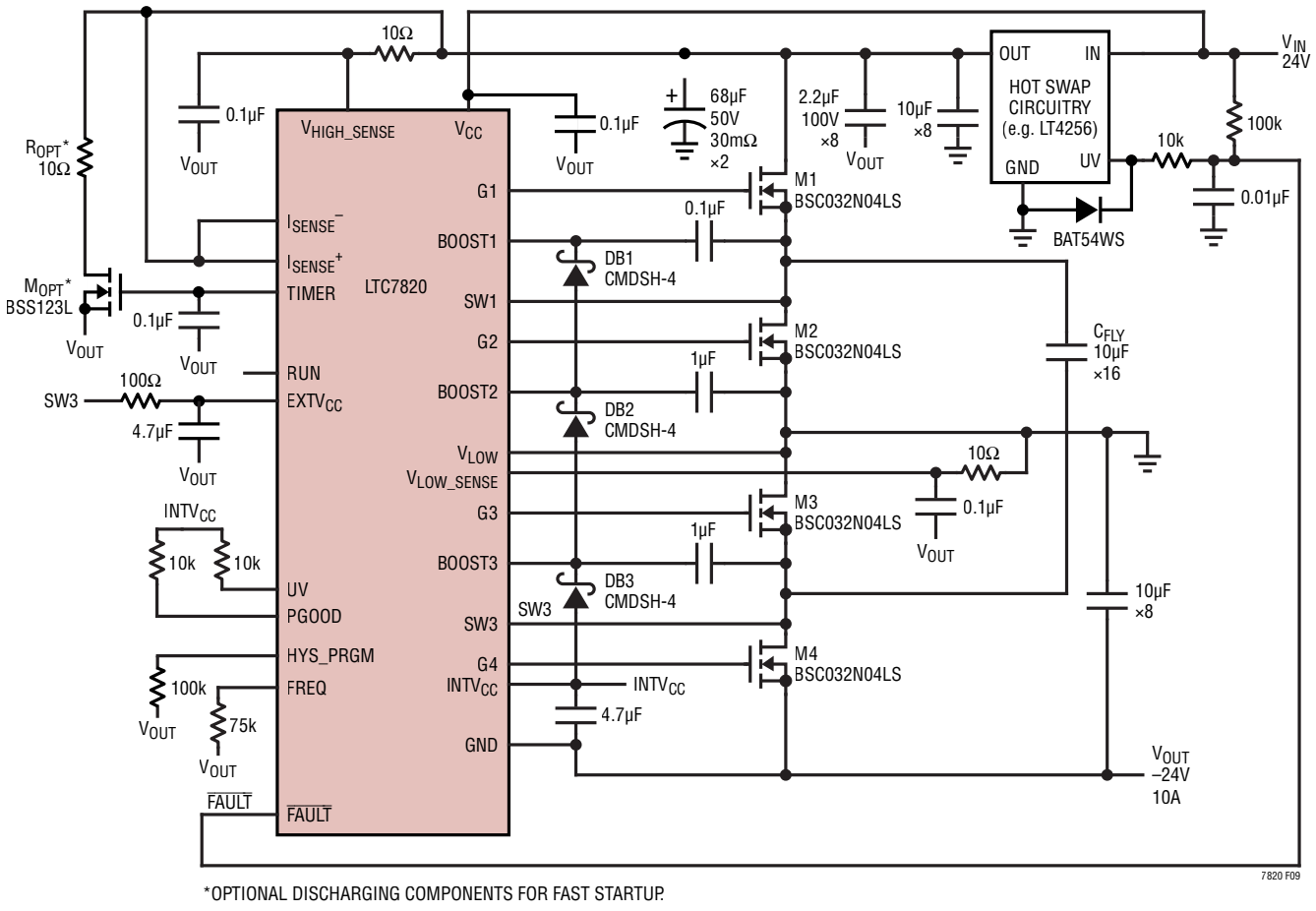


Figure 8. High Efficiency 24V to 48V, 7.5A Voltage Doubler with Disconnect FET at Input

TYPICAL APPLICATIONS



*OPTIONAL DISCHARGING COMPONENTS FOR FAST STARTUP.

Figure 9. High Efficiency 24V to –24V, 10A Voltage Inverter with Hot Swap at Input

TYPICAL APPLICATIONS

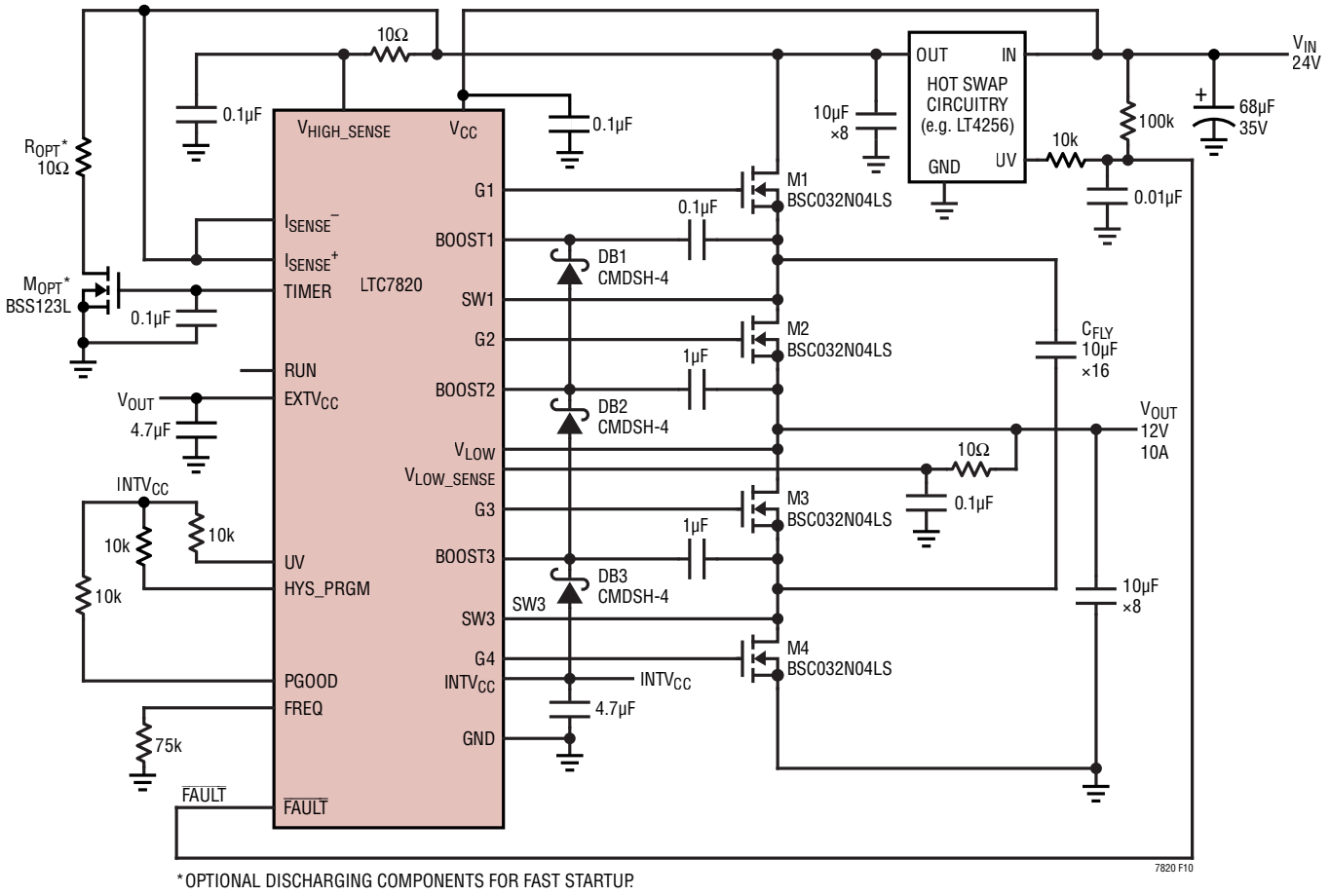


Figure 10. High Efficiency 24V to 12V, 10A Voltage Divider with Hot Swap at Input

TYPICAL APPLICATIONS

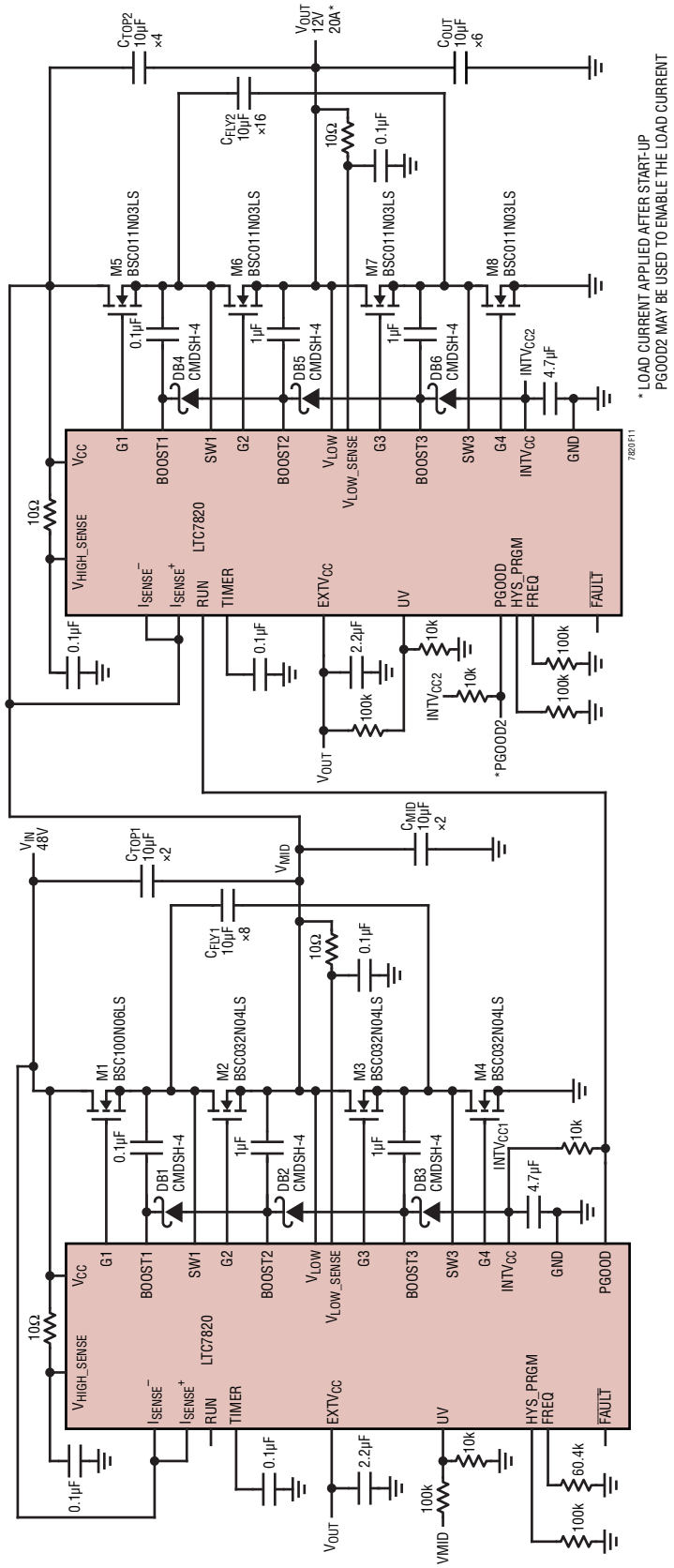
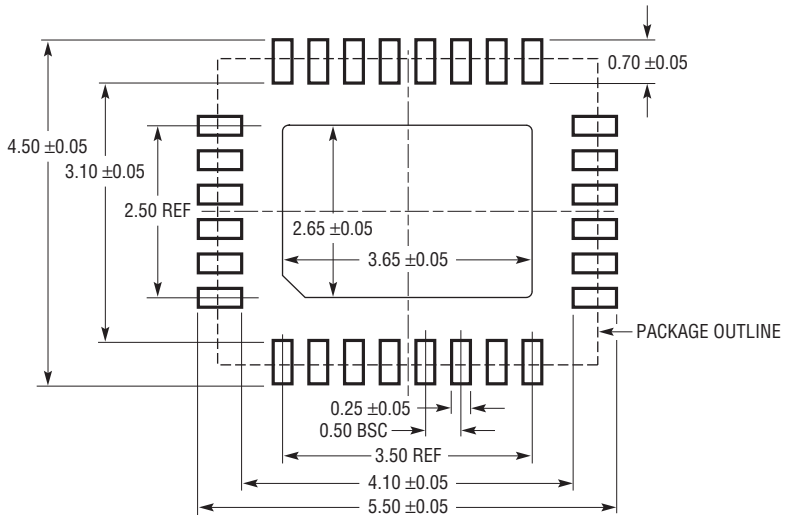


Figure 11. High Efficiency 48V to 12V, 20A Voltage Divider

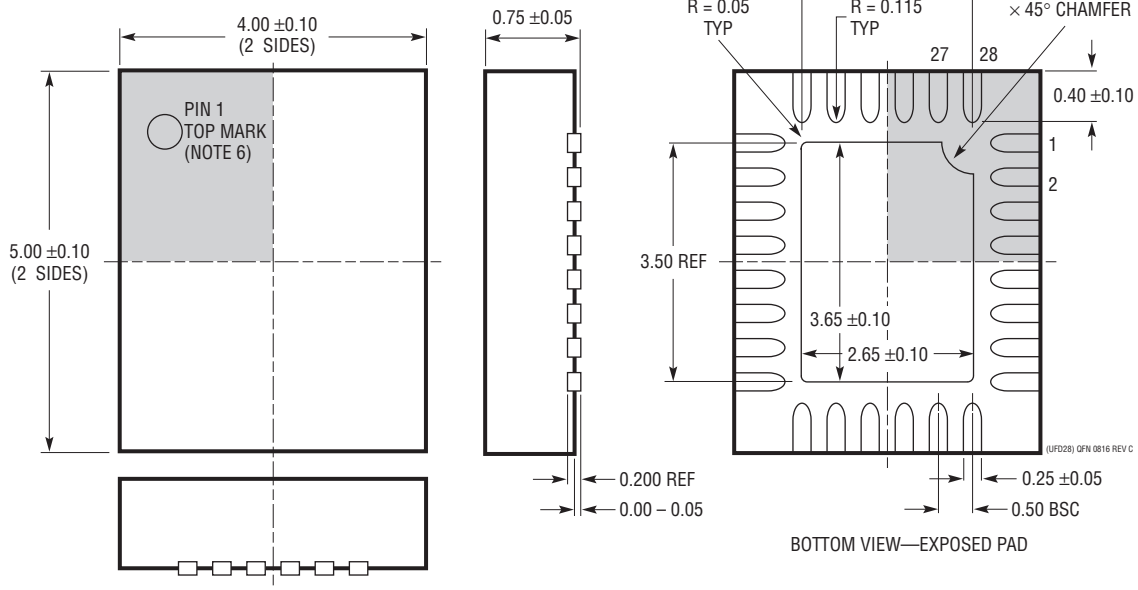
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC7820#packaging for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/17	Removed TG/BG from EC tables	3S
B	07/17	Changed the # of Switching Cycles in Voltage Divider section	12
		Modified $INTV_{CC}$ pin description	7
		Changed hysteresis voltage in Power Good Section	11
C	10/17	Corrected hot swap part number call-out.	23, 24