3GHz to 20GHz Microwave Mixer

FEATURES

- **Upconversion or Downconversion**
- **High IIP3: +24.3dBm at 10GHz**
  +21.5dBm at 17GHz
- **9dB Conversion Loss at 10GHz**
- **+16dBm Input P1dB at 10GHz**
- **Integrated LO Buffer: 0dBm LO Drive**
- **Low LO-RF Leakage: <–25dBm**
- 50Ω Wideband Matched RF, LO and IF Ports
- 3.3V/132mA Supply
- Fast Turn ON/OFF for TDD Operation
- 3mm × 2mm, 12-Lead QFN Package

APPLICATIONS

- 5G Broadband Wireless Access
- Microwave Transceivers
- Wireless Backhaul
- Point-to-Point Microwave
- Phased-Array Antennas
- C, X and Ku Band RADAR
- Test Equipment
- Satellite Modems

DESCRIPTION

The LTC®5553 is a high performance, microwave double balanced passive mixer that can be used for frequency upconversion or downconversion.

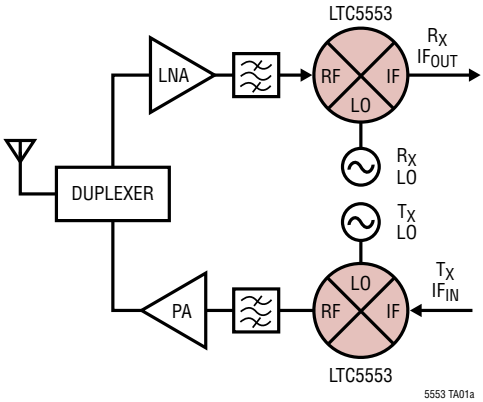
The LTC5553's mixer and integrated RF balun are optimized to cover the 3GHz to 20GHz RF frequency range. The device includes an integrated LO amplifier optimized for the 1GHz to 20GHz frequency range, requiring only 0dBm drive. The integrated IF balun is optimized to cover a very wide, 500MHz to 9GHz, frequency range while providing a single-ended 50Ω interface.

The LTC5553 delivers exceptionally high IIP3 and P1dB, in addition to low LO to RF and LO to IF leakages. The part also offers a high level of integration in a small package.

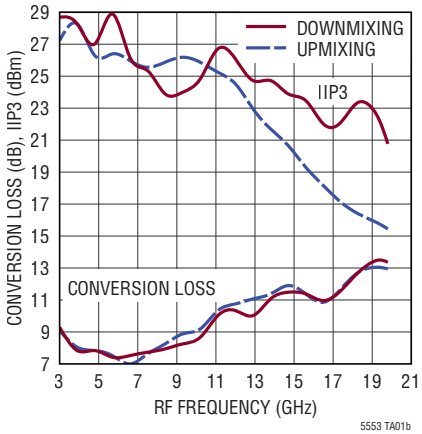
Electrostatic Sensitive Device

Observe Handling Precautions
ESD Sensitivity:
HBM = Class 0 on Pin 11
Class 1C All Other Pins
CDM = 500V All Pins

TYPICAL APPLICATION



Conversion Loss and IIP3 (Low Side LO, IF = 1890MHz)

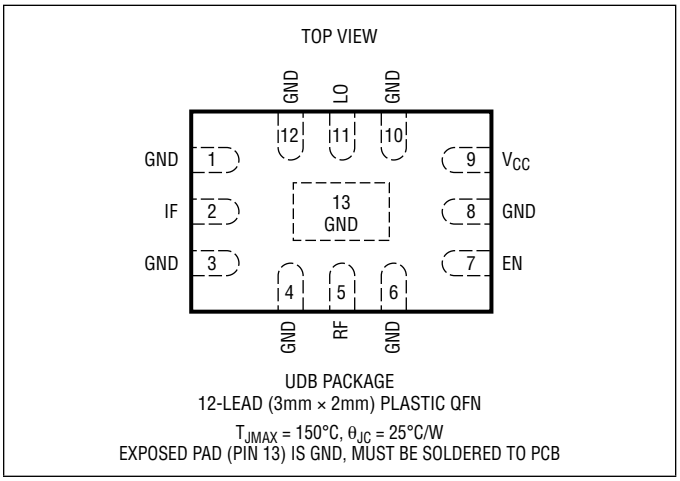


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 4V
Enable Input Voltage (EN) ..... –0.3V to V_{CC} + 0.3V
LO Input Power (1GHz to 20GHz) ..... ….+10dBm
LO Input DC Voltage ..... ±0.1V
RF Power (3GHz to 20GHz) ..... +20dBm
RF DC Voltage ..... ±0.1V
IF Power (500MHz to 9GHz) ..... +20dBm
IF DC Voltage ..... ±0.1V
Operating Temperature Range (T_C) ..... –40°C to 105°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature (T_J) ..... 150°C

PIN CONFIGURATION



UDB PACKAGE
12-LEAD (3mm × 2mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JC} = 25°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

(http://www.linear.com/product/LTC5553#orderinfo)

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	CASE TEMPERATURE RANGE
LTC5553IUDB#TRMPBF	LTC5553IUDB#TRPBF	LGZX	12-Lead (3mm × 2mm) Plastic QFN	–40°C to 105°C

TRM = 500 pieces.

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = High, unless otherwise noted. Test circuit shown in Figure 1. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Requirements						
Supply Voltage (V_{CC})		●	3.0	3.3	3.6	V
Supply Current	EN = High			132	150	mA
Shutdown Current	EN = Low				100	µA
Enable (EN) Logic Input						
Input High Voltage (On)		●	1.2			V
Input Low Voltage (Off)		●			0.3	V
Input Current	–0.3V to V_{CC} + 0.3V		–30		100	µA
Chip Turn-On Time				0.2		µs
Chip Turn-Off Time				0.1		µs

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = High, P_{LO} = 0dBm, P_{RF} = –6dBm (–6dBm/tone for two-tone IIP3 tests), unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LO Frequency Range		●		1 to 20		GHz
RF Frequency Range		●		3 to 20		GHz
IF Frequency Range		●		500 to 9000		MHz
RF Return Loss	Z_O = 50Ω, 3GHz to 17GHz			>9		dB
LO Input Return Loss	Z_O = 50Ω, 1GHz to 20GHz			>10		dB
LO Input Power			–6	0	6	dBm
Downmixer Application, IF = 1890MHz, Low Side LO						
Conversion Loss	RF Input = 4GHz RF Input = 10GHz RF Input = 14GHz RF Input = 17GHz			8.2 9.0 11.3 11.6		dB dB dB dB
Conversion Loss vs Temperature	T_C = –40°C to 105°C, RF Input = 9.8GHz	●		0.006		dB/°C
2-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	RF Input = 4GHz RF Input = 10GHz RF Input = 14GHz RF Input = 17GHz			27.6 24.3 23.9 21.5		dBm dBm dBm dBm
SSB Noise Figure	RF Input = 10GHz RF Input = 15.7GHz			10.9 12.8		dB dB
LO to RF Leakage	f_{LO} = 1GHz to 20GHz			<–23		dBm
LO to IF Leakage	f_{LO} = 1GHz to 20GHz			<–13		dBm
RF to LO Isolation	f_{RF} = 3GHz to 20GHz			>40		dB
RF Input to IF Output Isolation	f_{RF} = 3GHz to 20GHz			>32		dB
Input 1dB Compression	RF Input = 10GHz			16		dBm
Upmixer Application, IF = 1890MHz, Low Side LO						
Conversion Loss	RF Output = 4GHz RF Output = 10GHz RF Output = 14GHz RF Output = 17GHz			8.3 9.3 11.9 11.5		dB dB dB dB
Conversion Loss vs Temperature	T_C = –40°C to 105°C, RF Output = 5.8GHz			0.006		dB/°C
2-Tone Input 3rd Order Intercept (Δf_{IF} = 2MHz)	RF Output = 4GHz RF Output = 10GHz RF Output = 14GHz RF Output = 17GHz			27.2 25.6 21.2 17.3		dBm dBm dBm dBm
SSB Noise Figure	RF Output = 10GHz RF Output = 15.7GHz			10.1 12.1		dB dB
LO to RF Output Leakage	f_{LO} = 1GHz to 20GHz			<–25		dBm
LO to IF Input Leakage	f_{LO} = 1GHz to 20GHz			<–26		dBm
IF to LO Isolation	f_{IF} = 500MHz to 9GHz			>50		dB
IF to RF Isolation	f_{IF} = 500MHz to 9GHz			>40		dB
Input 1dB Compression	RF Output = 10GHz			14.8		dBm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

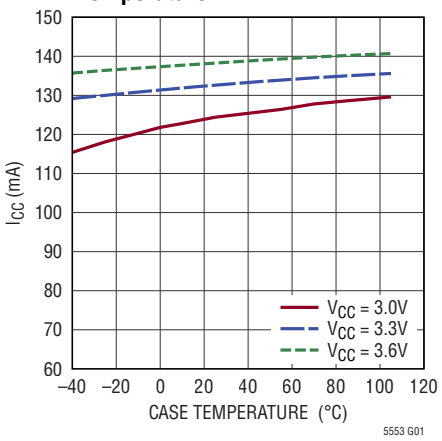
Note 2: The LTC5553 is guaranteed functional over the –40°C to 105°C case temperature range (θ_{JC} = 25°C/W).

Note 3: SSB noise figure measurements performed with a small-signal noise source, bandpass filter and 2dB matching pad on input, with bandpass filters on LO, and output.

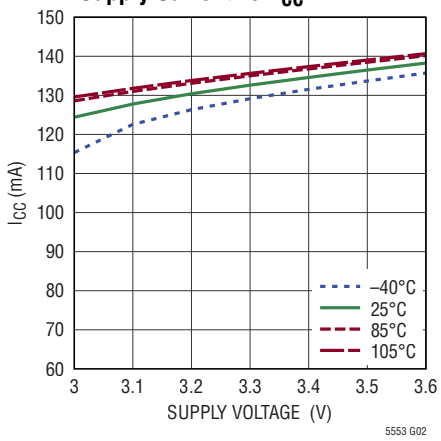
TYPICAL PERFORMANCE CHARACTERISTICS

EN = high, test circuit shown in Figure 1.

Supply Current vs Case Temperature



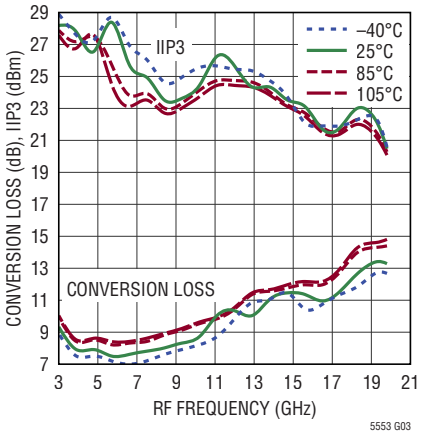
Supply Current vs V_{CC}



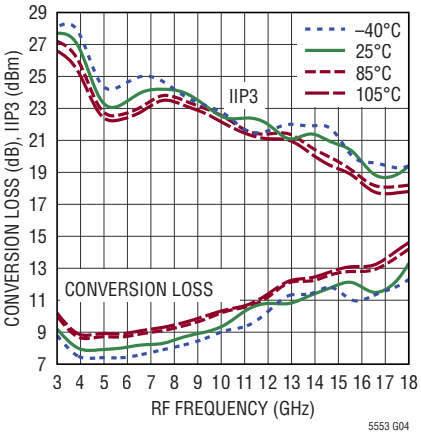
TYPICAL PERFORMANCE CHARACTERISTICS

3GHz to 20GHz downmixer application.
V_{CC} = 3.3V, EN = high, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = –6dBm (–6dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 1890MHz, unless otherwise noted. Test circuit shown in Figure 1.

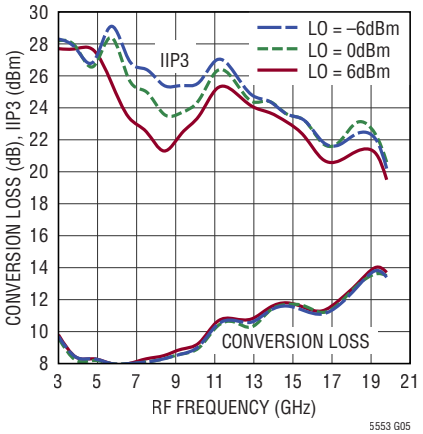
Conversion Loss and IIP3 vs RF Frequency (Low Side LO)



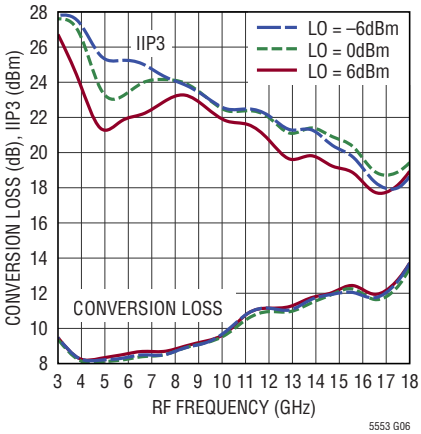
Conversion Loss and IIP3 vs RF Frequency (High Side LO)



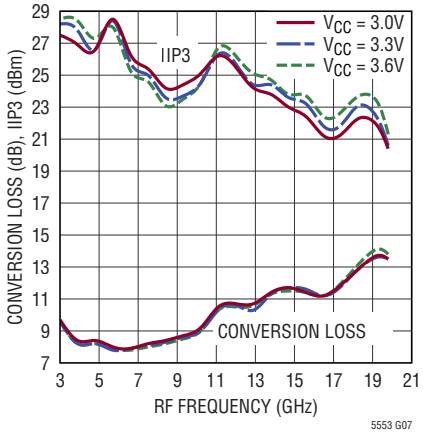
Conversion Loss and IIP3 vs RF Frequency (Low Side LO)



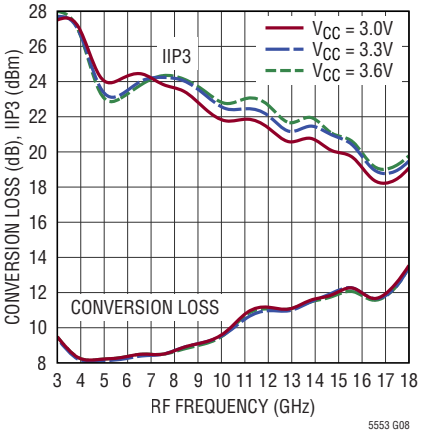
Conversion Loss and IIP3 vs RF Frequency (High Side LO)



Conversion Loss and IIP3 vs RF Frequency (Low Side LO)



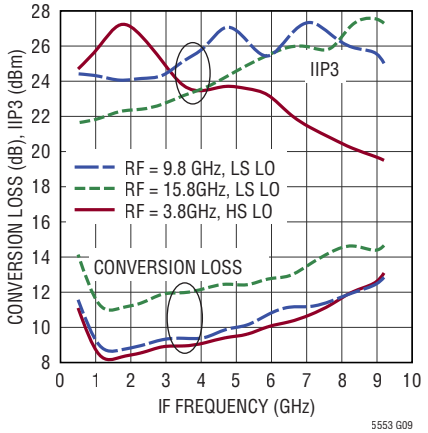
Conversion Loss and IIP3 vs RF Frequency (High Side LO)



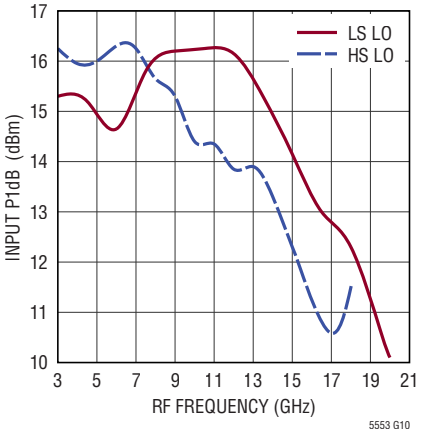
TYPICAL PERFORMANCE CHARACTERISTICS

3GHz to 20GHz downmixer application.
V_{CC} = 3.3V, EN = high, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = –6dBm (–6dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 1890MHz, unless otherwise noted. Test circuit shown in Figure 1.

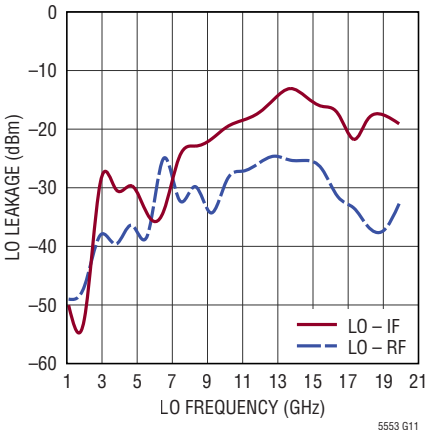
Conversion Loss and IIP3 vs IF Frequency (Low Side LO)



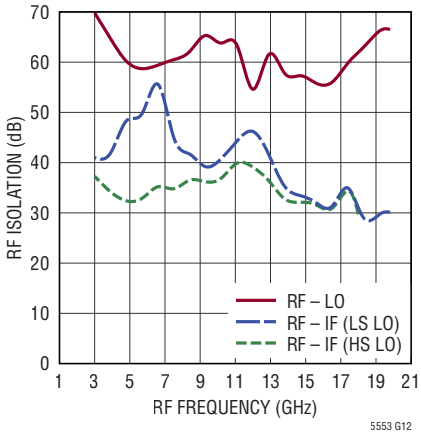
Input P1dB vs RF Frequency



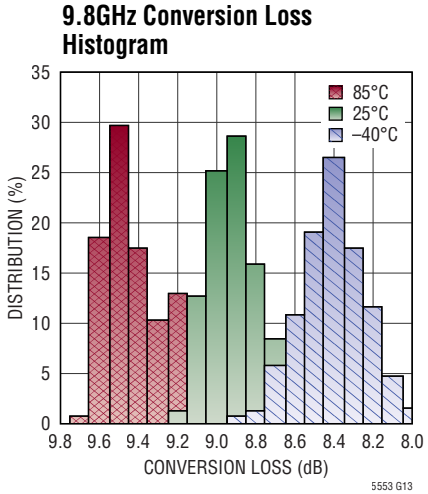
LO Leakage



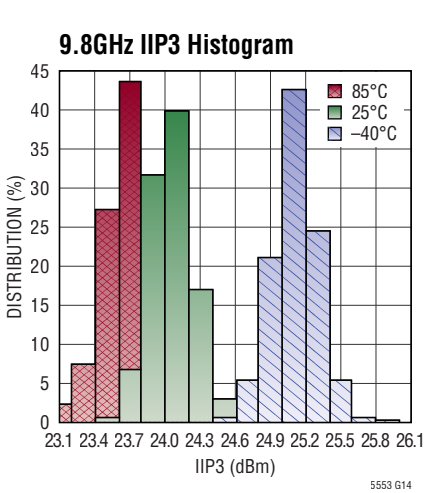
RF Isolation



9.8GHz Conversion Loss Histogram



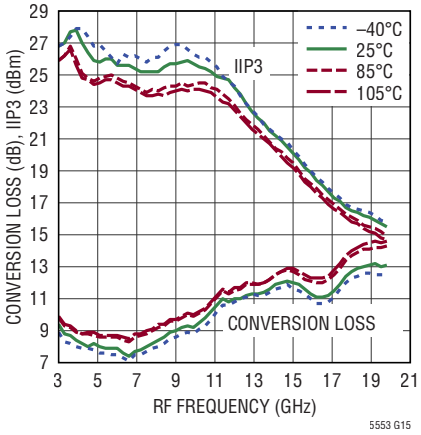
9.8GHz IIP3 Histogram



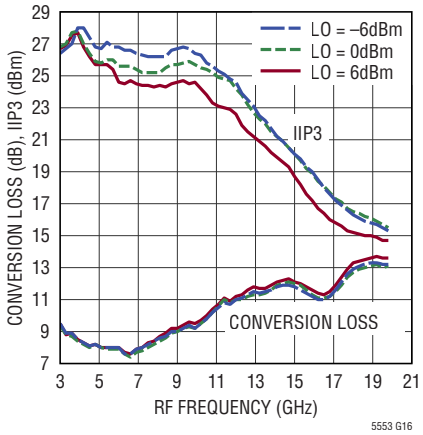
TYPICAL PERFORMANCE CHARACTERISTICS

3GHz to 20GHz upmixer application.
V_{CC} = 3.3V, EN = high, T_C = 25°C, P_{LO} = 0dBm, P_{IF} = –6dBm (–6dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 1890MHz, unless otherwise noted. Test circuit shown in Figure 1.

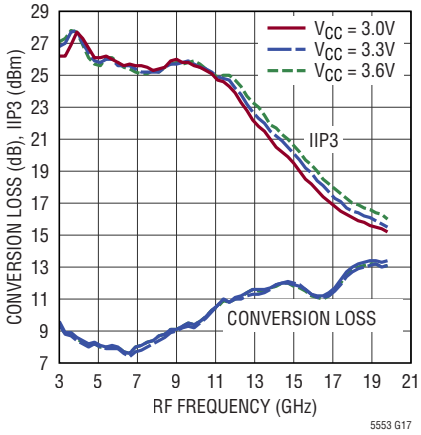
Conversion Loss and IIP3 vs RF Frequency (Low Side LO)



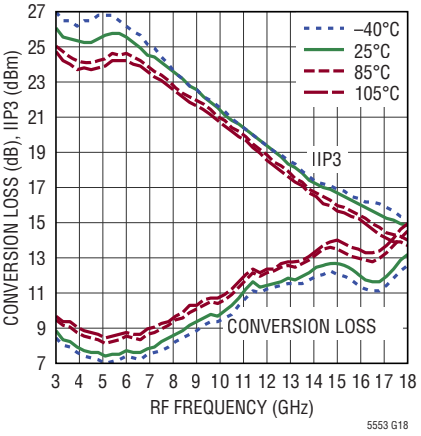
Conversion Loss and IIP3 vs RF Frequency (Low Side LO)



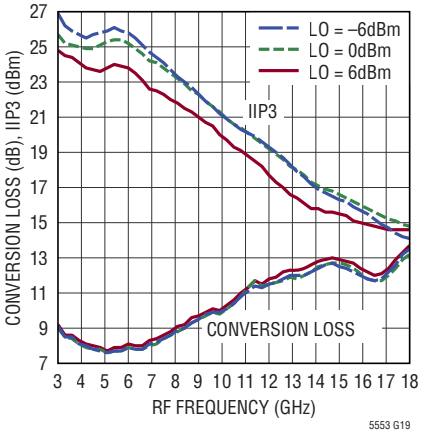
Conversion Loss and IIP3 vs RF Frequency (Low Side LO)



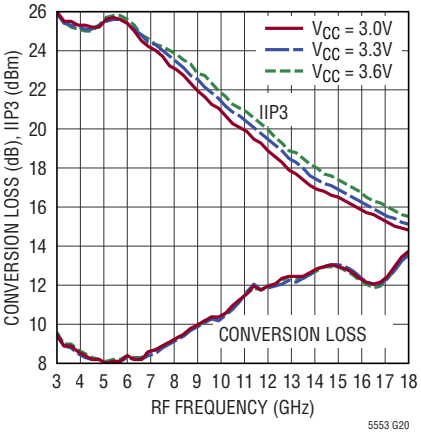
Conversion Loss and IIP3 vs RF Frequency (High Side LO)



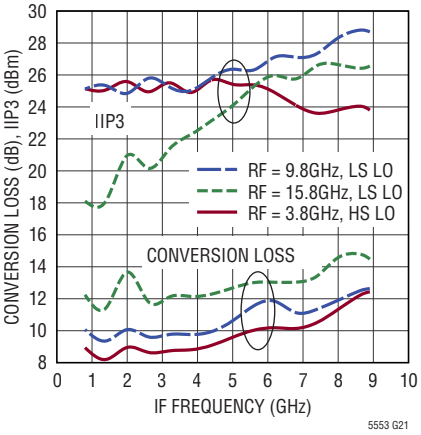
Conversion Loss and IIP3 vs RF Frequency (High Side LO)



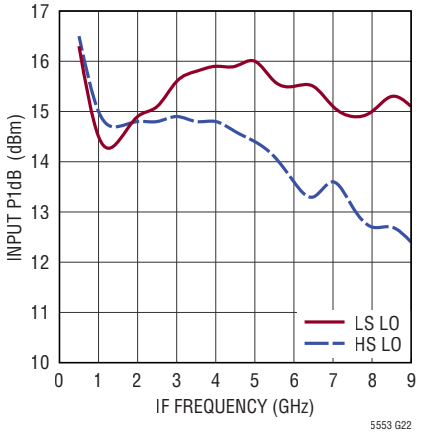
Conversion Loss and IIP3 vs RF Frequency (High Side LO)



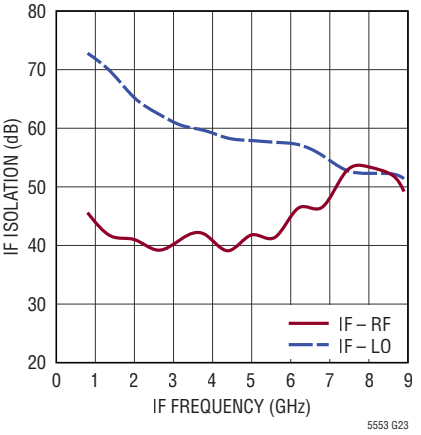
Conversion Loss and IIP3 vs IF Frequency (Low Side LO)



Input P1dB vs IF Frequency



IF Isolation



PIN FUNCTIONS

GND (Pins 1, 3, 4, 6, 8, 10, 12, Exposed Pad Pin 13): Ground. These pins must be soldered to the RF ground on the circuit board. The exposed pad metal of the package provides both electrical contact to ground and good thermal contact to the printed circuit board.

IF (Pin 2): Single-Ended Terminal for the IF Port. This pin is internally connected to the primary side of the IF transformer, which has low DC resistance to ground. A series DC blocking capacitor should be used to avoid damage to the integrated transformer if DC voltage is present. The IF port is impedance matched from 500MHz to 9GHz, as long as the LO is driven with a 0 ±6dBm source between 1GHz and 20GHz.

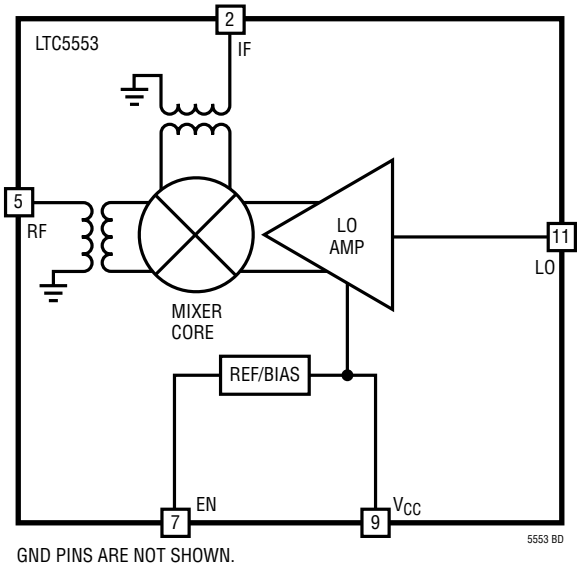
RF (Pin 5): Single-Ended Terminal for the RF Port. This pin is internally connected to the primary side of the RF transformer, which has low DC resistance to ground. A series DC blocking capacitor must be used to avoid damage to the integrated transformer if DC voltage is present. The RF port is impedance matched from 3GHz to 20GHz as long as the LO is driven with a 0 ±6dBm source between 1GHz and 20GHz.

EN (Pin 7): Enable Pin. When the voltage applied to this pin is greater than 1.2V, the mixer is enabled. When the voltage is less than 0.3V, the mixer is disabled. Typical input current is less than 30µA. This pin has an internal 376kΩ pull-down resistor.

V_{CC} (Pin 9): Power Supply Pin. This pin must be externally connected to a regulated 3.3V supply, with a bypass capacitor located close to the pin. Typical current consumption is 132mA when the part is enabled.

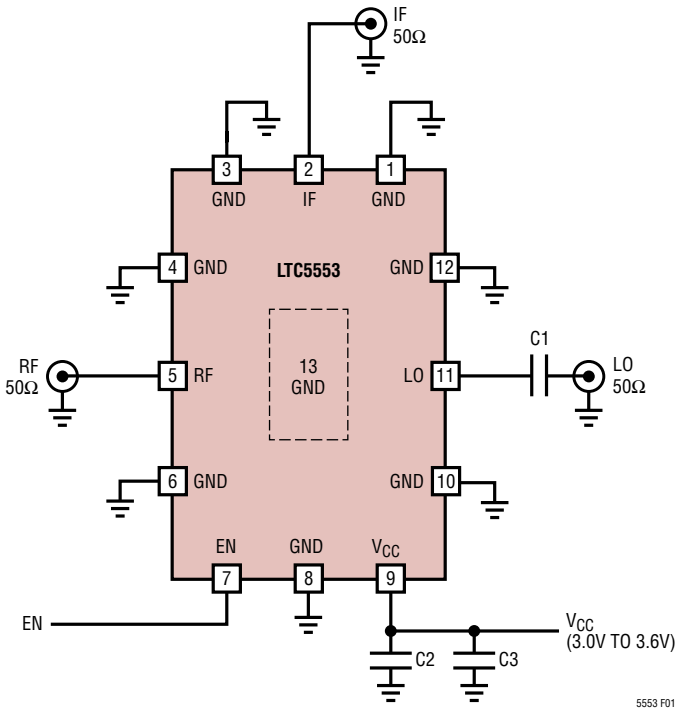
LO (Pin 11): Input for the Local Oscillator (LO). A series DC blocking capacitor must be used. Typical DC voltage at this pin is 1.6V.

BLOCK DIAGRAM



GND PINS ARE NOT SHOWN.

TEST CIRCUIT



REF DES	VALUE	SIZE	VENDOR	COMMENT
C1	18pF	0402	AVX	0402ZK180GBS
C2	18pF	0402	Murata	GJM1555C1H180FB01
C3	1µF	0603	Murata	GRM188R71A105KA61

* Standard Evaluation Board Configuration

Figure 1. Standard Test Circuit Schematic

APPLICATIONS INFORMATION

Introduction

The LTC5553 consists of a high linearity double-balanced mixer core, LO buffer amplifier and bias/enable circuits. See the Block Diagram section for a description of each pin function. The RF, LO and IF are single-ended 50Ω ports. The LTC5553 can be used as a frequency downconverter where the RF is used as an input and IF is used as an output. It can also be used as a frequency upconverter where the IF is used as an input and RF is used as an output. Low side or high side LO injection can be used. The evaluation circuit and the evaluation board layout are shown in Figure 1 and Figure 2, respectively.

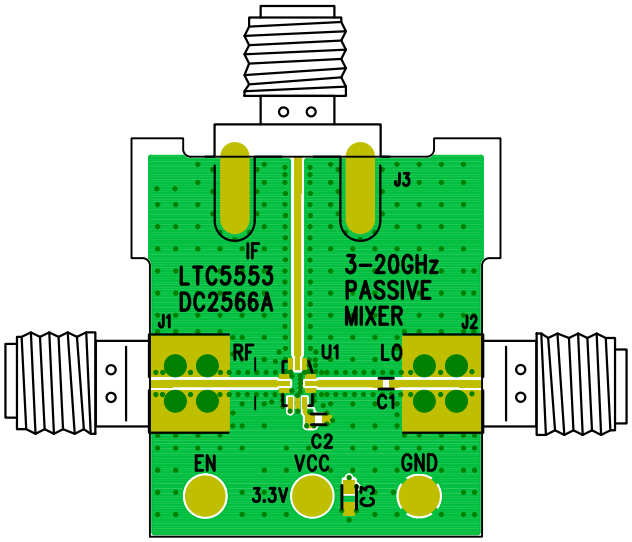


Figure 2. Evaluation Board Layout

RF Port

The mixer's RF port, shown in Figure 3, is connected to the primary winding of an integrated transformer. The primary side of the RF transformer is DC–grounded internally and the DC resistance of the primary side is approximately 2.5Ω. A DC blocking capacitor is needed if the RF source has DC voltage present. The secondary winding of the RF transformer is internally connected to the mixer core.

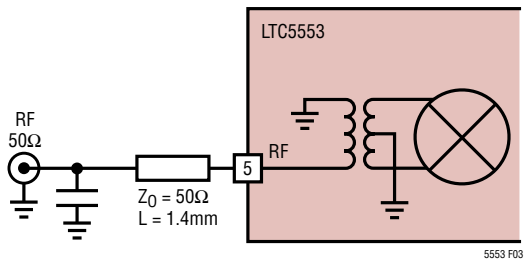
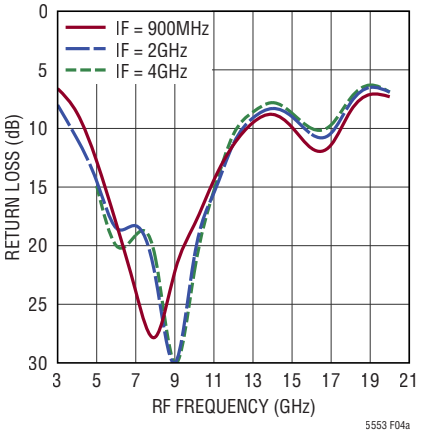
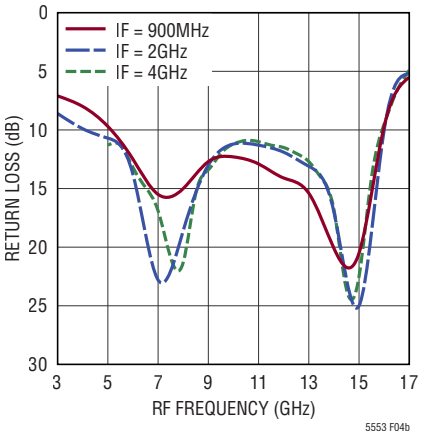


Figure 3. Simplified RF Port Interface Schematic

The RF port is internally broadband matched from 3GHz to 20GHz. A 0.15pF shunt capacitor located 1.4mm away from the RF pin can be used to improve the RF port matching between the 13GHz to 15GHz frequency range. LO power between –6dBm and 6dBm is required for good RF impedance matching. The measured RF input return loss is shown in Figure 4 for IF frequencies of 900MHz, 2GHz and 4GHz with low side LO.



(a) No Matching



(b) With Shunt 0.15pF at 1.4mm

Figure 4. RF Port Return Loss

APPLICATIONS INFORMATION

The RF input impedance and input reflection coefficient versus RF frequency is listed in Table 1. The reference plane for this data is Pin 5 of the IC, with no external matching, and the LO is driven at 12GHz.

Table 1. RF Port Impedance and S11 (at Pin 5, No External Matching, LO Input Driven at 12GHz)

FREQUENCY (GHz)	RF IMPEDANCE	S11	
		MAG	ANGLE
3	62.7 + j40.8	0.36	52.8
4	69.5 + j7.7	0.18	17.9
5	55.7 + j2.4	0.06	21.3
6	55.4 + j10.1	0.11	56.3
7	53.5 + j2.6	0.04	35.3
8	54.1 – j1.7	0.04	–21.8
9	52.7 – j7.3	0.08	–65.8
10	48.4 – j10.4	0.11	–92.5
11	46.6 – j14.8	0.16	–94.2
12	29.4 – j40.8	0.51	–89.6
13	28.7 – j15.6	0.33	–132.5
14	25.6 – j17.7	0.39	–130.8
15	26.0 – j15.4	0.37	–135.9
16	26.2 – j7.6	0.33	–156.5
17	25.4 + j5.2	0.33	164.3
18	21.6 + j14.8	0.44	140.8
19	19.8 + j18.9	0.49	132.9
20	19.6 + j17.2	0.49	136.5

LO Input

The mixer's LO input, shown in Figure 5, consists of a single-ended to differential conversion and high speed limiting differential amplifier. The LO amplifier is optimized for the 1GHz to 20GHz LO frequency range. LO frequencies above or below this frequency range may be used with degraded performance.

The DC voltage at the LO input is about 1.6V. A DC blocking capacitor (C1) is required.

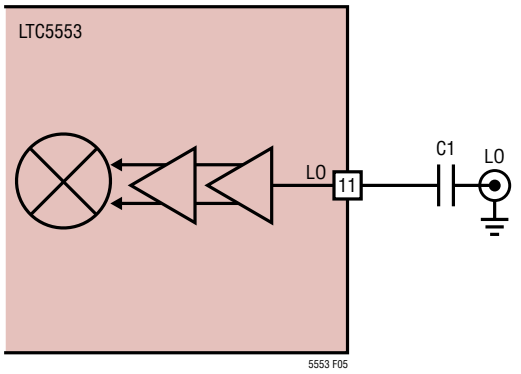


Figure 5. Simplified LO Input Schematic

The LO is 50Ω matched from 1GHz to 20GHz. External matching components may be needed for extended LO operating frequency range. The measured LO input return loss is shown in Figure 6. The nominal LO input level is 0dBm, although the limiting amplifiers will deliver excellent performance over a ±6dBm input power range.

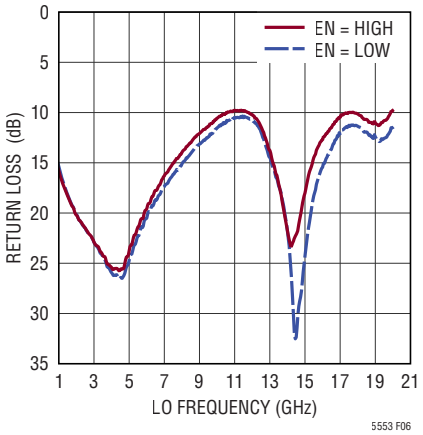


Figure 6. LO Input Return Loss

The LO input impedance and input reflection coefficient versus frequency, is shown in Table 2.

APPLICATIONS INFORMATION

Table 2. LO Input Impedance vs Frequency (at Pin 11, No External Matching with C1 = 18pF Connected)

FREQUENCY (GHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
1	56.6 – j16.2	0.16	–59.1
2	54.1 – j9.2	0.10	–60.9
3	52.4 – j6.4	0.07	–65.6
4	50.4 – j5.0	0.05	–82.1
5	48.7 – j5.9	0.06	–99.1
6	46.7 – j9.5	0.10	–103.6
7	44.4 – j13.3	0.15	–104.8
8	41.4 – j17.2	0.21	–105.8
9	39.0 – j20.2	0.25	–105.8
10	38.7 – j25.9	0.31	–97.3
11	40.8 – j30.3	0.33	–88.5
12	49.2 – j34.7	0.33	–72.1
13	58.2 – j26.8	0.25	–59.1
14	55.9 – j11.6	0.12	–57.0
15	40.9 – j5.2	0.12	–146.9
16	29.1 – j8.4	0.28	–152.1
17	24.1 – j13.5	0.39	–142.1
18	25.2 – j16.8	0.39	–133.3
19	27.8 – j14.1	0.33	–137.2
20	24.1 – j7.6	0.36	–157.8

IF Port

The mixer's IF port, shown in Figure 7, is connected to the primary winding of an integrated transformer. The primary side of the IF transformer is DC-grounded internally and the DC resistance is approximately 6.2Ω. A DC blocking capacitor is needed if the IF source has DC voltage present. The secondary winding of the IF transformer is internally connected to the mixer core.

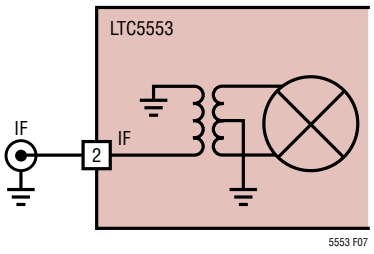


Figure 7. Simplified IF Port Schematic

The measured IF port return loss is shown in Figure 8.

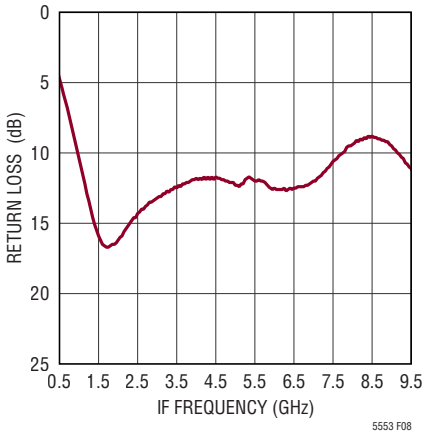


Figure 8. IF Port Return Loss

The IF port impedance and input reflection coefficient versus frequency are shown in Table 3.

Table 3. IF Port Impedance vs Frequency (at Pin 2, No External Matching)

FREQUENCY (GHz)	IF IMPEDANCE	S11	
		MAG	ANGLE
0.5	16.0 + j30.4	0.63	113.4
1.0	58.3 + j36.2	0.33	58.6
1.5	66.5 – j6.3	0.15	–17.7
2.0	45.5 – j16.8	0.18	95.0
2.5	36.2 – j14.2	0.23	–124.7
3.0	32.9 – j11.3	0.24	–138.6
3.5	32.1 – j7.2	0.23	–152.9
4.0	31.6 – j2.3	0.23	–171.4
4.5	31.1 + j2.4	0.23	171.2
5.0	31.8 + j7.3	0.24	152.9
5.5	31.7 + j10.3	0.25	143.3
6.0	32.5 + j12.7	0.26	135.3
6.5	29.6 + j10.8	0.29	144.5
7.0	27.8 + j9.0	0.31	151.3
7.5	25.6 + j6.8	0.33	159.2
8.0	23.4 + j5.0	0.37	165.6
8.5	22.8 + j4.8	0.38	166.2
9.0	24.6 + j5.8	0.35	162.8
9.5	30.5 + j8.6	0.26	150.0
10.0	42.7 + j15.3	0.18	106.2

APPLICATIONS INFORMATION

Enable Interface

Figure 9 shows a simplified schematic of the EN pin interface. To enable the chip, the EN voltage must be higher than 1.2V. The voltage at the EN pin should never exceed V_{CC} by more than 0.3V. If this should occur, the supply current could be sourced through the ESD diode, potentially damaging the IC. If the EN pin is left floating, its voltage will be pulled low by the internal pull-down resistor and the chip will be disabled.

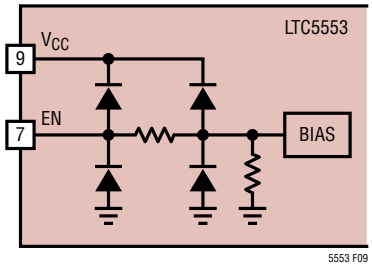


Figure 9. Simplified Enable Input Circuit

Supply Voltage Ramping

Fast ramping of the supply voltage can cause a current glitch in the internal ESD protection circuits. Depending on the supply inductance, this could result in a supply voltage transient that exceeds the maximum rating. A supply voltage ramp time of greater than 1ms is recommended.

Spurious Output Levels

Mixer spurious output levels versus harmonics of the RF and LO are tabulated in Table 4. The spur levels were measured on a standard evaluation board using the test circuit shown in Figure 1. The spur frequencies can be calculated using the following equation:

Frequency Downconversion: $f_{SPUR} = (M \bullet f_{RF}) \pm (N \bullet f_{LO})$

Frequency Upconversion: $f_{SPUR} = (M \bullet f_{IF}) \pm (N \bullet f_{LO})$

Table 4a. Downconversion IF Output Spur Levels (dBc): $f_{SPUR} = (M \bullet f_{RF}) - (N \bullet f_{LO})$

RF = 5250MHz, P_{RF} = –6dBm, P_{LO} = 0dBm, LO = 4900MHz

		N					
		0	1	2	3	4	5
M	0		–15	–11	–16	–5	–21
	1	–48	0	–28	–13	–39	–27
	2	–63	–55	–65	–61	–63	–58
	3	–73	–73	< –75	–73	< –75	–69
	4	*	–72	–72	< –75	–75	< –75
	5	*	*	*	–73	–72	< –75

*Out of the test equipment range.

Table 4b. Upconversion RF Output Spur Levels (dBc): $f_{SPUR} = (M \bullet f_{RF}) + (N \bullet f_{LO})$

RF = 5835MHz, P_{IF} = –6dBm, P_{LO} = 0dBm, IF = 1890MHz, Low-Side LO, V_{CC} = 3.3V, EN = High, T_C = 25°C

		N					
		0	1	2	3	4	8
M	0		–24	–15	–16	–20	–27
	1	–51	0	–42	–13	–43	*
	2	–58	–64	–58	–61	–62	*
	3	< –75	–72	–72	–71	*	*
	4	< –75	< –75	–73	–73	*	*
	5	< –75	–73	–73	*	*	*
	6	< –75	–73	–73	*	*	*
	7	–72	–73	*	*	*	*

*Out of the test equipment range.

APPLICATIONS INFORMATION

Evaluation Board Insertion Loss

The LTC5553 performance in the data sheet is measured using the evaluation board shown in Figure 2. The insertion loss of the board traces and SMA connectors are not de-embedded. These insertion losses are shown in Figure 10, and the actual performance of the LTC5553 can be estimated using this data. Figure 11 compares the de-embedded performance to the performance measured at the SMA connectors.

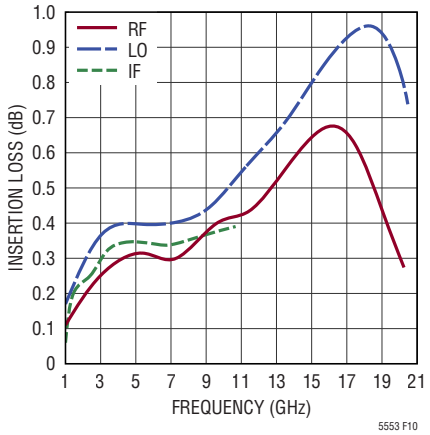


Figure 10. Insertion Loss of the RF, LO and IF ports

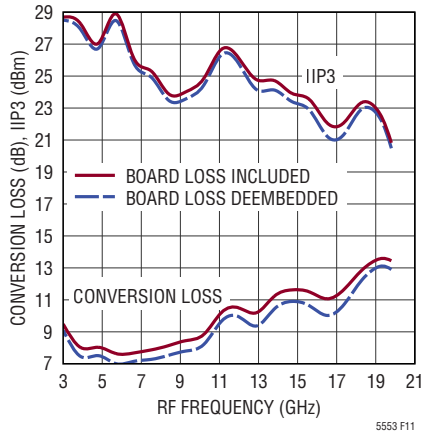
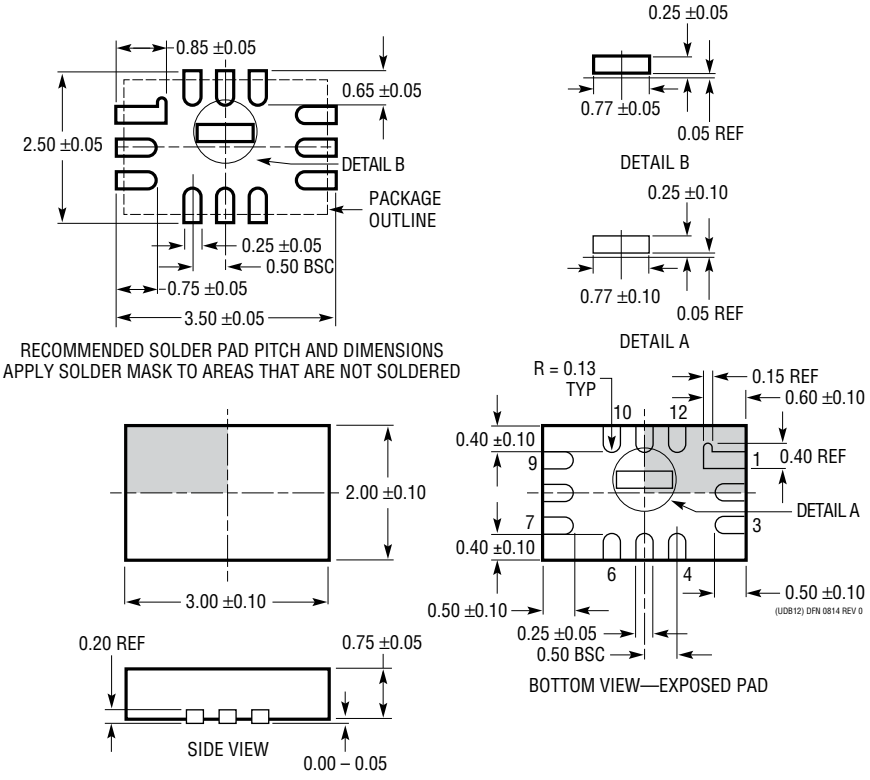


Figure 11. Comparison of the LTC5553 Performance Before and After De-Embedding the Insertion Loss of the Evaluation Board and SMA Connectors. Downconversion Application with Low Side LO, IF = 1890MHz, V_{CC} = 3.3V, EN = High, T_C = 25°C

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC5553#packaging for the most recent package drawings.

UDB Package
Variation A
12-Lead Plastic QFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1985 Rev Ø)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE