EN55022B Compliant 40V, Dual 4A or Single 8A Step-Down or 50W Inverting µModule Regulator

FEATURES

- **Dual 4A/Single 8A Low EMI Switch Mode Power Supply**
- **EN55022 Class B Compliant**
- **Two Fully Independent Channels, Each Configurable for Positive or Negative Output Voltage Polarity**
- **Output Voltage Range: 0.5V ≤ $|V_{OUTn}^{+} - V_{OUTn}^{-}|$ ≤ 26.5V**
- **Wide Input Voltage Range: Up to 40V**
  - **3.1V or 3.6V Start-Up, Configuration-Dependent**
- **±1.67% Total DC Output Voltage Error Over Line, Load and Temperature**
- **Analog Output Current Indicator (Positive-V_{OUT} Only)**
- **LDO_{OUT}: 5V Fixed, 25mA Capable LDO**
- **Parallelable with LTM4651/LTM4653**
- Constant-Frequency Current Mode Control
- Power Good Indicators and Programmable Soft-Start
- Overcurrent and Overtemperature Protection
- 16mm × 16mm × 5.01mm BGA Package

APPLICATIONS

- Automated Test and Measurement
- Avionics and Industrial Control Systems
- Video, Imaging and Instrumentation

DESCRIPTION

The LTM®4655 is an ultralow noise 40V, dual 4A or single 8A DC/DC µModule® regulator designed to meet the radiated emissions requirements of EN55022. Its channels are fully independent, parallelable and capable of delivering positive or negative output polarity. Conducted emission requirements can be met by adding standard filter components. Included in the package are the switching controllers, power MOSFETs, inductors, filters and support components. A 5V, 25mA LDO and clock generator enable phase interleaving of the power switching stages, for improved EMC performance.

The LTM4655 can regulate positive V_{OUTn}^{+} voltages between 0.5V and 26.5V from a 3.1V to 40V input. The LTM4655 can regulate negative V_{OUTn}^{-} voltages between –0.5V and –26.5V from a maximum input range of 3.6V to 40V, with the span from V_{INn} to V_{OUTn}^{-} not to exceed 40V. A switching frequency range of 250kHz to 3MHz is supported.

The LTM4655 is offered in a 16mm × 16mm × 5.01mm BGA package with SnPb or RoHS compliant terminal finish.

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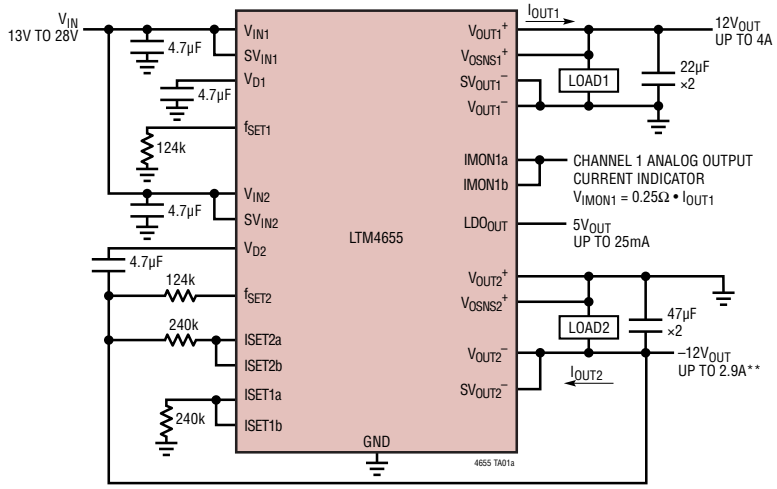
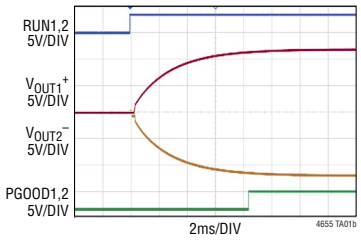
TYPICAL APPLICATION

Concurrent, ±12V Output DC/DC µModule Regulator*



Output Voltage Start-Up Waveforms



* FOR COMPLETE CIRCUIT, SEE FIGURE 50.

** FOR CHANNELS CONFIGURED TO REGULATE NEGATIVE V_{OUTn}^{-}: CURRENT LIMIT FREQUENCY-FOLDBACK INCEPTION IS A FUNCTION OF V_{INn}, V_{OUTn}-, AND f_{SWn}. CONTINUOUS OUTPUT CURRENT CAPABILITY IS SUBJECT TO DETAILS OF APPLICATION IMPLEMENTATION. SEE NOTES 2 AND 3 AND THE APPLICATIONS INFORMATION SECTION, FOR DETAILS.

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ABSOLUTE MAXIMUM RATINGS

(Note 1 and Note 5)

Channel 1 Terminal Voltages **(All Channel 1 Terminal Voltages Relative to V_{OUT1}^- Unless Otherwise Indicated)**

V_{IN1}, V_{D1}, SV_{IN1}, SV_{INF1}, SW1 ..... –0.3V to 42V
GND, $EXTV_{CC1}$, V_{OUT1}^+, V_{OSNS1}^+,
ISET1a , ISET1b ..... –0.3V to 28V
$INTV_{CC1}$, PGDFB1, VINREG1, COMP1a,
IMON1a, IMON1b ..... –0.3V to 4V
f_{SET1} ..... –0.3V to $INTV_{CC1}$
RUN1 ..... GND–0.3V to V_{OUT1}^- + 32V
PGOOD1, CLKIN1 (Relative to GND)..... –0.3V to 6V

Channel 2 Terminal Voltages **(All Channel 2 Terminal Voltages Relative to V_{OUT2}^- Unless Otherwise Indicated)**

V_{IN2}, V_{D2}, S_{VIN2}, SV_{INF2}, SW2 ..... –0.3V to 42V
GND, $EXTV_{CC2}$, V_{OUT2}^+, V_{OSNS2}^+,
ISET2a, ISET2b..... –0.3V to 28V
$INTV_{CC2}$, PGDFB2, VINREG2, COMP2a,
IMON2a, IMON2b ..... –0.3V to 4V
f_{SET2} ..... –0.3V to $INTV_{CC2}$
RUN2 ..... GND–0.3V to V_{OUT2}^- + 32V
PGOOD2, CLKIN2 (Relative to GND) ..... –0.3V to 6V

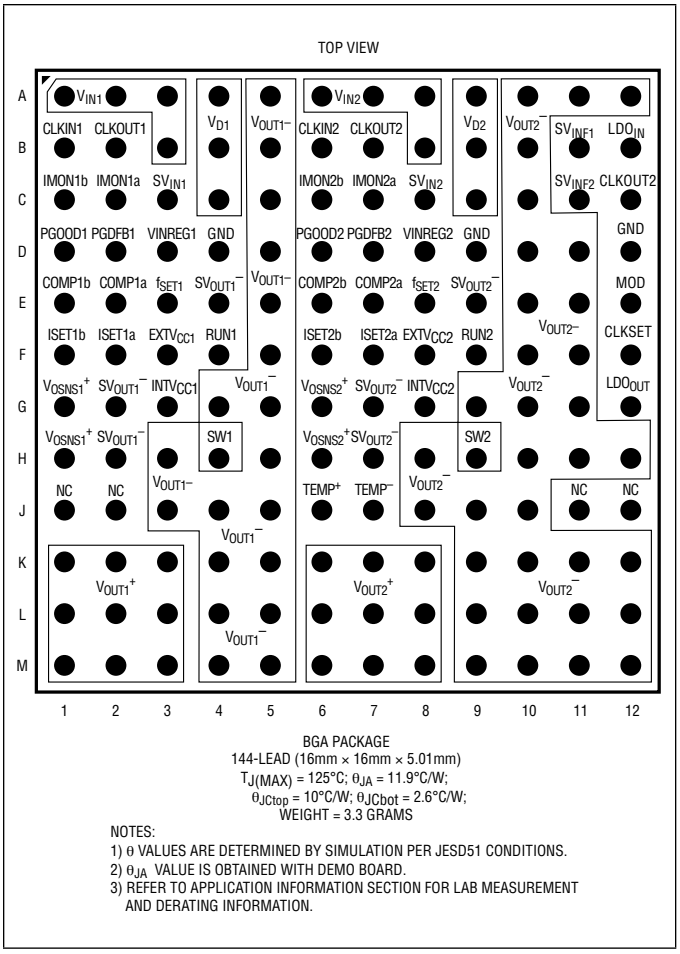
LDO and Clock Generator Voltages (**All LDO and Clock Generator Terminal Voltages Relative to GND Unless Otherwise Indicated)**

LDO_{IN} ..... –0.3V to 42V
CLKSET, MOD ..... –0.3V to LDO_{OUT} + 0.3V

Terminal Currents
$INTV_{CCn}$ Peak Output Current (Note 10) 30mA
$TEMP^+$ .....–1mA to 10mA
$TEMP^-$ .....–10mA to 1mA

Temperatures Internal Operating Temperature
Range (Note 2 and Note 9)
E- and I-Grade ..... –40°C to 125°C
MP-Grade ..... –55°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Package Body Temperature During Reflow .. 245°C

PIN CONFIGURATION



BGA PACKAGE
144-LEAD (16mm × 16mm × 5.01mm)
$T_{J(MAX)}$ = 125°C; θ_{JA} = 11.9°C/W;
θ_{JCtop} = 10°C/W; θ_{JCbot} = 2.6°C/W;
WEIGHT = 3.3 GRAMS

NOTES:
1) θ VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS.
2) θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD.
3) REFER TO APPLICATION INFORMATION SECTION FOR LAB MEASUREMENT AND DERATING INFORMATION.

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4655EY#PBF	SAC305 (RoHS)	LTM4655Y	e1	BGA	3	–40°C to 125°C
LTM4655IY#PBF	SAC305 (RoHS)	LTM4655Y	e1	BGA	3	–40°C to 125°C
LTM4655MPY#PBF	SAC305 (RoHS)	LTM4655Y	e1	BGA	3	–55°C to 125°C
LTM4655IY	SnPb (63/37)	LTM4655Y	e0	BGA	3	–40°C to 125°C
LTM4655MPY	SnPb (63/37)	LTM4655Y	e0	BGA	3	–55°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 5). T_A = 25°C, Test Circuit 1 (positive-V_{OUT}, noninverting step-down configuration with V_{OUTn^-} = GND), V_{INn} = SV_{INn} = 36V, $EXTV_{CCn}$ = 24V, $RUNn$ = 3.3V, R_{ISETn} = 480k, R_{fSETn^+} = 57.6kΩ, f_{SWn} = 1.5MHz ($CLKINn$ driven with 1.5MHz clock signal) and voltages referred to GND unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$SV_{INn(DC)}$, $V_{INn(DC)}$	Input DC Voltage in Positive-V_{OUT} Configuration	V_{OUTn^-} = GND	●	3.1		40	V
$V_{OUTn(RANGE)^+}$	Range of Positive Output Voltage Regulation	0.5V ≤ ISET*n*a–SV_{OUTn^-} ≤ 26.5V, I_{OUTn^+} = 0A (See Note 7)	●	0.5		26.5	V
$V_{OUTn(24VDC)^+}$	Output Voltage Total Variation with Line and Load at V_{OUTn^+} = 24V	29V ≤ V_{INn} ≤ 40V, 0A ≤ I_{OUTn^+} ≤ 4A, C_{INHn} = 4.7µF, C_{Dn} = 4.7µF, C_{OUTHn} = 2 × 47µF, CLKIN*n* Driven with 1.5MHz Clock	●	23.6	24	24.4	V
$V_{OUTn(0.5VDC)^+}$	Output Voltage Total Variation with Line and Load at V_{OUTn^+} = 0.5V	Measuring V_{OSNSn^+} to ISET*n*a 3.1V ≤ V_{INn} ≤ 13.2V, 0A ≤ I_{OUTn^+} ≤ 4A, C_{INHn} = 4.7µF, C_{Dn} = 4.7µF, C_{OUTHn} = 2 × 47µF, ISET*n*a = 500mV, R_{fSETn} = N/U (Note 6)	●	–15	0	15	mV
R_{SVINFn}	Resistor Between SV_{INn} and SV_{INFn}				1		Ω
Input Specifications							
$V_{INn(UVLO)}$	SV_{INn} Undervoltage Lockout Threshold	SV_{INn} Rising SV_{INn} Falling Hysteresis	● ● ●	 2.4 150	2.85 2.6 250	3.1 2.9	V V mV
$I_{INRUSH(VINn)}$	Input Inrush Current at Start-Up	C_{INHn} = 4.7µF, C_{Dn} = 4.7µF, C_{OUTHn} = 2 × 47µF; I_{OUTn^+} = 0A, ISET*n*a Electrically Connected to ISET*n*b			300		mA
$I_{Q(SVINn)}$	Input Supply Bias Current	Shutdown, $RUNn$ = GND $RUNn$ = 3.3V			16 450	30	µA µA
$I_{S(VINn)}$	Input Supply Current	CLKIN*n* Open Circuit, I_{OUTn^+} = 4A			2.9		A
$I_{S(VINn, SHUTDOWN)}$	Input Supply Current in Shutdown	Shutdown, $RUNn$ = GND			4		µA
Output Specifications							
I_{OUTn^+}	V_{OUTn^+} Output Continuous Current Range	(Note 3)		0		4	A
$\Delta V_{OUTn(LINE)^+}/V_{OUTn^+}$	Line Regulation Accuracy	I_{OUTn^+} = 0A, 29V ≤ V_{INn} ≤ 40V	●		0.05	0.1	%
$\Delta V_{OUTn(LOAD)^+}/V_{OUTn^+}$	Load Regulation Accuracy	V_{INn} = 36V, 0A ≤ I_{OUTn^+} ≤ 4A	●		0.05	0.75	%
$V_{OUTn(AC)^+}$	Output Voltage Ripple, V_{OUTn^+}	V_{INn} = 12V, ISET*n*a = 5V			2		mV_{P-P}

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 5). T_A = 25°C, Test Circuit 1 (positive-V_{OUTn}^+, noninverting step-down configuration with V_{OUTn^-} = GND), V_{INn} = SV_{INn} = 36V, $EXTV_{CCn}$ = 24V, RUN*n* = 3.3V, R_{ISETn} = 480k, R_{fSETn}^+ = 57.6kΩ, f_{SWn} = 1.5MHz (CLKIN*n* driven with 1.5MHz clock signal) and voltages referred to GND unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{Sn}	V_{OUTn}^+ Ripple Frequency	R_{fSETn} = 57.6k, CLKIN*n* Open Circuit	●	1.7	1.95	2.2	MHz
$\Delta V_{OUTn(START)}^+$	Turn-On Overshoot				8		mV
t_{STARTn}	Turn-On Start-Up Time	Delay Measured from V_{INn} Toggling from 0V to 36V to PGOOD*n* Exceeding 3V; PGOOD*n*. Having a 100kΩ Pull-Up to 3.3V with Respect to GND, VPGFB*n* Resistor Divider Network as Shown in Test Circuit 1, R_{ISETna} = 480kΩ and ISET*n*a Electrically Connected to ISET*n*b and CLKIN Driven with 1.5MHz Clock	●		4	9	ms
$\Delta V_{OUTn(LS)}^+$	Peak Output Voltage Deviation for Dynamic Load Step	I_{OUTn}^+: 0A to 2A and 2A to 0A Load Steps in 1µs, C_{OUTHn} = 47µF × 2			400		mV
$t_{SETTLEn}$	Settling Time for Dynamic Load Step	I_{OUTn}^+: 0A to 2A and 2A to 0A Load Steps in 1µs, C_{OUTHn} = 47µF × 2			50		µs
$I_{OUTn(OCL)}^+$	I_{OUTn}^+ Output Current Limit				5.5		A
Control Section							
I_{ISETna}	Reference Current of ISET*n*a Pin	V_{ISETna} = 0.5V, 3.1V ≤ V_{INn} ≤ 13.2V V_{ISETna} = 24V, 29V ≤ V_{INn} ≤ 40V	● ●	49.3 49	50 50	50.7 51	µA µA
I_{VOSNSn}^+	V_{OSNSn}^+ Leakage Current	V_{VOSNSn}^+ = 28V			290		µA
$t_{ONn(MIN)}$	Minimum On-Time	(Note 4)			60		ns
V_{RUNn}	RUN*n* Turn-On/-Off Thresholds	RUN*n* Input Turn-On Threshold, RUN*n* Rising RUN*n* Hysteresis	●	1.08	1.2 130	1.32	V mV
I_{RUNn}	RUN*n* Leakage Current	RUN*n* = 3.3V	●		0.1	50	nA
Oscillator and Phase-Locked Loop (PLL)							
f_{OSCn}	Oscillator Frequency Accuracy	V_{INn} = 12V, ISET*n*a = 5V, and: f_{SETn} Open-Circuit R_{fSETn} = 57.6kΩ (See f_{SN} Specification)	●	360	400 1.95	440	kHz MHz
f_{SYNCn}	PLL Synchronization Capture Range	V_{INn} = 12V, ISET*n*a = 5V, $CLKIN_n$ Driven with a GND Referred Clock Toggling from 0.4V to 1.2V and Having a Clock Duty Cycle: From 10% to 90%; f_{SETn} Open Circuit From 40% to 60%; R_{fSETn} = 57.6kΩ		250 1.3		550 3	kHz MHz
V_{CLKINn}	CLKIN*n* Input Threshold	V_{CLKINn} Rising V_{CLKINn} Falling		1.2		 0.4	V V
I_{CLKINn}	CLKIN*n* Input Current	V_{CLKINn} = 5V V_{CLKINn} = 0V		 –20	230 –5	500	µA µA
Power Good Feedback Input and Power Good Output							
OV_{PGDFBn}	Output Overvoltage PG00D*n* Upper Threshold	PGDFB*n* Rising	●	620	645	675	mV
UV_{PGDFBn}	Output Undervoltage PGOOD*n* Lower Threshold	PGDFB*n* Falling	●	525	555	580	mV
ΔV_{PGDFBn}	PGOOD*n* Hysteresis	PGDFB*n* Returning			8		mV
R_{PGDFBn}	Resistor Between PGDFB1*n* and SV_{OUTn}^-			4.94	4.99	5.04	kΩ
R_{PGOODn}	PGOOD*n* Pull-Down Resistance	V_{PGOODn} = 0.1V, V_{PGDFBn} < UV_{PGDFBn} or V_{PGDFBn} > OV_{PGDFBn}			700	1500	Ω
$I_{PGOODn(LEAK)}$	PGOOD*n* Leakage Current	V_{PGOODn} = 3.3V, UV_{PGDFBn} < V_{PGDFBn} < OV_{PGDFBn}			0.1	1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 5). T_A = 25°C, Test Circuit 1 (positive-V_{OUTn}^+, noninverting step-down configuration with V_{OUTn^-} = GND), V_{INn} = SV_{INn} = 36V, $EXTV_{CCn}$ = 24V, RUN*n* = 3.3V, R_{ISETn} = 480k, R_{fSETn}^+ = 57.6kΩ, f_{SWn} = 1.5MHz (CLKIN*n* driven with 1.5MHz clock signal) and voltages referred to GND unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{PGOODn(DELAY)}$	PGOOD*n* Delay	PGOOD*n* Low to High (Note 4) PGOOD*n* High to Low (Note 4)			$16/f_{SW(Hz)}$ $64/f_{SW(Hz)}$		s s
Current Monitor and Input Voltage Regulation Pins							
h_{IMONna}	I_{OUTn}^+/I_{IMONna}	Ratio of V_{OUTn}^+ Output Current to I_{IMONna} Current, I_{OUTn}^+ = 4A	●	36	40	44	k
$I_{OSn(IMON)}$	I_{IMONna} Offset Current	I_{IMONna} at I_{OUTn}^+ = 0A		–5		5	µA
IMON*n*b Resistor	Resistor Between IMON*n*b and SV_{OUTn}^-			9.8	10	10.2	kΩ
V_{IMONna}	IMON*n*a Servo Voltage	IMON*n*a Voltage During Output Current Regulation	●	1.9	2.0	2.1	V
$V_{VINREGn}$	V_{INREGn} Servo Voltage	VINREG*n* Voltage During Output Current Regulation	●	1.8	2.0	2.2	V
$I_{VINREGn}$	V_{INREGn} Leakage Current	VINREG*n* = 2V			1		nA
$INTV_{CCn}$ Regulator							
$V_{INTVCCn}$	Channel Internal V_{CC} Voltage, No $INTV_{CCn}$ Loading ($I_{INTVCCn}$ = 0mA)	3.6V ≤ SV_{INn} ≤ 40V, $EXTV_{CCn}$ Open Circuit 5V ≤ SV_{INn} ≤ 40V, 3.2V ≤ $EXTV_{CCn}$ ≤ 26.5V		3.15 2.85	3.4 3.0	3.65 3.15	V V
$V_{EXTVCCn(TH)}$	$EXTV_{CCn}$ Switchover Voltage	(Note 4)			3.15		V
$\Delta V_{INTVCCn(LOAD)}/V_{INTVCCn}$	$INTV_{CCn}$ Load Regulation	0mA ≤ $I_{INTVCCn}$ ≤ 30mA		–2	0.5	2	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 5). T_A = 25°C, Test Circuit 2 (negative-V_{OUTn}^-, inverting buck-boost configuration with V_{OUTn}^+ = GND), V_{INn} = 12V and electrically connected to SV_{INn}, RUN*n*–GND = 3.3V, ISET*n*a–SV_{OUTn}^- = 24V, $EXTV_{CCn}$ = GND, CLKIN*n* open circuit, R_{fSETn} = 57.6kΩ and R_{ISETn} = 480kΩ and voltages referred to GND unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$SV_{INn(DC)}$, $V_{INn(DC)}$	Input DC Voltage in Negative-V_{OUT}^- Configuration	$V_{INn}^+ \lvert V_{OUTn}^- \rvert$ ≤ 40V	●	3.6		40	V
$V_{OUTn(RANGE)}^-$	Range of Negative Output Voltage Regulation	0.5V ≤ ISET*n*a–SV_{OUTn}^- ≤ 26.5V	●	–26.5		–0.5	V
$V_{OUTn(–24VDC)}^-$	Output Voltage Total Variation with Line and Load at V_{OUTn}^- = –24V	3.6V ≤ V_{INn} ≤ 16V, 0A ≤ I_{OUTn}^- ≤ 0.3A, CLKIN*n* Driven per Note 8, C_{INHn} = 4.7µF, C_{Dn} = 4.7µF × 2, C_{OUTHn} = 47µF × 2	●	–24.4	–24	–23.6	V
$V_{OUTn(–5VDC)}^-$	Output Voltage Total Variation with Line and Load at V_{OUTn}^- = –5V	Measuring V_{OSNSn}^+ – ISET*n*a, 12V ≤ V_{INn} ≤ 35V, 0A ≤ I_{OUT}^- ≤ 3A, CLKIN*n* Driven by 550kHz Clock, C_{INHn} = 4.7µF, C_{Dn} = 4.7µF × 2, C_{OUTHn} = 47µF × 2, ISET*n*a–SV_{OUTn}^- = 5V	●	–15	0	15	mV
R_{SVINFn}	Resistor Between SV_{INn} and SV_{INFn}				1		Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 5). T_A = 25°C, Test Circuit 2 (negative-V_{OUTn}^-, inverting buck-boost configuration with V_{OUTn}^+ = GND), V_{INn} = 12V and electrically connected to SV_{INn}, RUN*n*–GND = 3.3V, ISET*n*a–SV_{OUTn}^- = 24V, $EXTV_{CCn}$ = GND, CLKIN*n* open circuit, R_{fSETn} = 57.6kΩ and R_{ISETn} = 480kΩ and voltages referred to GND unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Specifications							
$V_{INn(UVLO)}$	SV_{INn} Undervoltage Lockout Threshold	SV_{INn} Rising SV_{INn} Falling Hysteresis	● ● ●	 2.1 400	3.2 2.5 700	3.6 2.8	V V mV
$I_{INRUSH(VINn)}$	Input Inrush Current at Start-Up	C_{INHn} = 4.7µF, CD*n* = 4.7µF × 2, C_{OUTHn} = 47µF × 2; I_{OUTn}^- = 0A, ISET*n*a Electrically Connected to ISET*n*b			1.1		A
$I_{Q(SVINn)}$	Input Supply Bias Current	Shutdown, RUN*n* = GND RUN*n*–GND = 3.3V			16 450	30	µA µA
$I_{S(VINn)}$	Input Supply Current	CLKIN*n* Open Circuit, I_{OUTn}^- = 1.25A			3.0		A
$I_{S(VINn, SHUTDOWN)}$	Input Supply Current in Shutdown	Shutdown, RUN*n* = GND			4		µA
Output Specifications							
I_{OUTn}^-	V_{OUTn}^- Output Continuous Current Range	V_{INn} = 12V, Regulating V_{OUTn}^- = –24V at f_{SWn} = 1MHz V_{INn} = 12V, Regulating V_{OUTn}^- = –5V at f_{SWn} = 550kHz (See Note 3. Capable of Up to 4A Output Current for Some Combinations of V_{INn}, V_{OUTn}^- and f_{SWn})		0 0		1.25 3	A A
$\Delta V_{OUTn(LINE)}^-/V_{OUTn}^-$	Line Regulation Accuracy	I_{OUTn}^- = 0A, 3.6V ≤ V_{INn} ≤ 16V, ISET*n*a–SV_{OUTn}^- = 24V, CLKIN*n* Driven by 1.8MHz Clock	●		0.05	0.25	%
$\Delta V_{OUTn(LOAD)}^-/V_{OUTn}^-$	Load Regulation Accuracy	V_{INn} = 12V, 0A ≤ I_{OUTn}^- ≤ 1.25A, CLKIN*n* Driven by 1.5MHz Clock, R_{fSETn} = 57.6kΩ, and R_{ISETn} = 480kΩ	●		0.05	0.75	%
$V_{OUTn(AC)}^-$	Output Voltage Ripple, V_{OUTn}^-	V_{INn} = 12V, I_{SETna}–SV_{OUTn}^- = 5V			10		mV_{P-P}
f_{SN}	V_{OUTn}^- Ripple Frequency	V_{INn} = 12V, I_{SETna}–SV_{OUTn}^- = 5V	●	1.7	1.95	2.2	MHz
$\Delta V_{OUTn(START)}^-$	Turn-On Overshoot				8		mV
t_{STARTn}	Turn-On Start-Up Time	Delay Measured from V_{INn} Toggling from 0V to 12V to PGOOD*n* Exceeding 3V Above GND; PGOOD*n* Having a 100kΩ Pull-Up to 3.3V with Respect to GND, V_{PGFBn} Resistor Divider Network as Shown in Test Circuit 2, R_{ISETna} = 480kΩ, ISET*n*a Electrically Connected to ISETnb, and CLKIN*n* Driven with 1.2MHz Clock	●		4	9	ms
$\Delta V_{OUTn(LS)}^-$	Peak Output Voltage Deviation for Dynamic Load Step	I_{OUTn}^-: 0A to 1A and 1A to 0A Load Steps in 1µs, C_{OUTHn} = 47µF × 2			400		mV
$t_{SETTLEn}$	Settling Time for Dynamic Load Step	I_{OUTn}^-: 0A to 1A and 1A to 0A Load Steps in 1µs, C_{OUTH2} = 47µF × 2 X5R			50		µs
$I_{OUTn(OCL)}^-$	I_{OUTn}^- Output Current Limit				1.7		A
Control Section							
I_{ISETna}	Reference Current of ISET*n*a Pin	V_{ISETna}–SV_{OUTn}^- = 0.5V, 3.6V ≤ V_{INn} ≤ 28V 0V ≤ V_{ISETna}–SV_{OUTn}^- ≤ V_{INn}–SV_{OUT}^- ≤ 40V	● ●	49.3 49	50 50	50.7 51	µA µA
I_{VOSNSn}^+	V_{OSNSn}^+ Leakage Current	V_{OSNSn}^+ – SV_{OUTn}^- = 28V			290		µA
$t_{ONn(MIN)}$	Minimum On-Time	(Note 4)			60		ns
V_{RUNn}	RUN*n* Turn-On/-Off Thresholds	RUN*n* Input Turn-On Threshold, RUN*n* Rising RUN*n* Hysteresis (RUN*n* Thresholds Measured with Respect to GND)	●	1.08	1.2 130	1.32	V mV
I_{RUNn}	RUN*n* Leakage Current	V_{INn} = 12V, RUN*n*–GND = 3.3V	●		0.1	50	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 5). T_A = 25°C, Test Circuit 2 (negative-V_{OUT}, inverting buck-boost configuration with V_{OUT}^+ = GND), V_{IN} = 12V and electrically connected to SV_{IN}, RUN–GND = 3.3V, ISET–SV_{OUT}^- = 24V, $EXTV_{CC}$ = GND, CLKIN open circuit, R_{fSET} = 57.6kΩ and R_{ISET} = 480kΩ and voltages referred to GND unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator and Phase-Locked Loop (PLL)							
f_{OSC}	Oscillator Frequency Accuracy	V_{IN} = 12V, ISET–SV_{OUT}^- = 5V, and: f_{SET} Open Circuit R_{fSET} = 57.6kΩ (See f_{SN} Specification)	●	360	400 1.95	440	kHz MHz
f_{SYNC}	PLL Synchronization Capture Range	V_{IN} = 12V, ISET–SV_{OUT}^- = 5V, CLKINn Driven with a GND Referred Clock Toggling from 0.4V to 1.2V and Having a Clock Duty Cycle: From 10% to 90%; f_{SET} Open Circuit From 40% to 60%; R_{fSET} = 57.6kΩ		250 1.3		550 3	kHz MHz
V_{CLKIN}	CLKIN Input Threshold	V_{CLKIN} Rising with Respect to GND V_{CLKIN} Falling with Respect to GND		1.2		 0.4	V V
I_{CLKIN}	CLKINn Input Current	V_{CLKIN} = 5V with Respect to GND V_{CLKIN} = 0V with Respect to GND		 –20	230 –5	500	µA µA
Power Good Feedback Input and Power Good Output							
OV_{PGDFBn}	Output Overvoltage PGOOD Upper Threshold	PGDFB Rising, Differential Voltage from PGDFB to SV_{OUT}^-	●	620	645	675	mV
UV_{PGDFBn}	Output Undervoltage PGOOD Lower Threshold	PGDFB Falling, Differential Voltage from PGDFB to SV_{OUT}^-	●	525	555	580	mV
ΔV_{PGDFB}	PGOOD Hysteresis	PGDFB Returning			8		mV
R_{PGDFB}	Resistor Between PGDFB and SV_{OUT}^-			4.94	4.99	5.04	kΩ
R_{PGOOD}	PGOOD Pull-Down Resistance	V_{PGOOD} = 0.1V with Respect to GND, V_{PGDFB}–SV_{OUT}^- < UV_{PGDFB} or V_{PGDFB}–SV_{OUT}^- > OV_{PGDFB}			700	1500	Ω
$I_{PGOODn(LEAK)}$	PGOOD Leakage Current	V_{PGOOD} = 3.3V with Respect to GND, UV_{PGDFB} < V_{PGDFB}–SV_{OUT}^- < OV_{PGDFB}			0.1	1	µA
$t_{PGOOD(DELAY)}$	PGOOD Delay	PGOOD Low to High (Note 4) PGOOD High to Low (Note 4)			$16/f_{SW(Hz)}$ $64/f_{SW(Hz)}$		s s
Input Voltage Regulation Pin							
V_{VINREG}	V_{INREG} Servo Voltage	V_{INREG} Voltage During Output Current Regulation, Measured with Respect to SV_{OUT}^-	●	1.8	2.0	2.2	V
I_{VINREG}	V_{INREG} Leakage Current	V_{INREG}–SV_{OUT}^- = 2V			1		nA
$INTV_{CC}$ Regulator							
V_{INTVCC}	Channel Internal V_{CC} Voltage, No $INTV_{CC}$ Loading (I_{INTVCC} = 0mA)	3.6V ≤ SV_{IN}–SV_{OUT}^- ≤ 40V, $EXTV_{CC}$ = Open Circuit 5V ≤ SV_{IN}–SV_{OUT}^- ≤ 40V, 3.2V ≤ $EXTV_{CC}^-$ V_{OUT}^- ≤ 26.5V ($INTV_{CC}$ Measured with Respect to SV_{OUT}^-)		3.15 2.85	3.4 3.0	3.65 3.15	V V V
$V_{EXTVCC(TH)}$	$EXTV_{CC}$ Switchover Voltage	($EXTV_{CC}$ Measured with Respect to SV_{OUT}^-) (Note 4)			3.15		V
$\Delta V_{INTVCC(LOAD)}$/ V_{INTVCC}	$INTV_{CC}$ Load Regulation	0mA ≤ I_{INTVCC} ≤ 30mA		–2	0.5	2	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). T_A = 25°C, Test Circuit 3 and voltages referred to GND unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$LDO_{IN(DC)}$	LDO Input DC Voltage		●	4.5		40	V
$V_{LDOOUT(DC)}$	LDO Output Voltage	V_{LDOIN} = 36V, 0mA ≤ I_{LDOOUT} ≤ 25mA V_{LDOIN} = 4.5V, 0mA ≤ I_{LDOOUT} ≤ 20mA	● ●	4.8 2.7	5.0 4.1	5.2	V V
$V_{LDOOUT(AC)}$	Output Voltage Ripple				2		mV_{P-P}
$I_{LDOOUT(OCL)}$	Output Current Limit, 5V LDO	LDO_{IN} = 36V			140		mA
Clock Generator							
Δf_{OUT}	Clock-Generator Frequency Accuracy	2.7V ≤ LDO_{OUT} ≤ 5.2V, 200kHz ≤ f_{OUT} ≤ 3MHz, MOD Connected to CLKOUT2	●		±2.5 ±2.5	±7.5 ±3	% %
$R_{CLKSET(RANGE)}$	Frequency Setting Resistor Range	R_{CLKSET} Resistance for Which –7.5% ≤ Δf_{OUT} ≤ 7.5%, Over 2.7V ≤ LDO_{OUT} ≤ 5.2V, MOD Electrically Connected to CLKOUT2	●	33.2		499	kΩ
	Period Variation (Frequency Spreading)	LDO_{OUT} = 5V, R_{CLKSET} = 100kΩ, MOD Open Circuit			±10		%
	Duty Cycle	2.7V ≤ LDO_{OUT} ≤ 5.2V, 200kHz ≤ f_{OUT} ≤ 3MHz, MOD Electrically Connected to CLKOUT2	●	40		60	%
$\theta_{CLKOUT1}$/ $\theta_{CLKOUT2}$	Phase Relationship of CLKOUT2 to CLKOUT1	2.7V ≤ LDO_{OUT} ≤ 5.2V, 200kHz ≤ f_{OUT} ≤ 3MHz, MOD Electrically Connected to CLKOUT2			180		Deg
$V_{OH\_CLKOUTn}$	CLKOUT*n* Output Voltage, Logic High	CLKOUT*n* V_{OH} Measured with Respect to LDO_{OUT}, 2.7V ≤ LDO_{OUT} ≤ 5.2V, $I_{CLKOUTn}$ = –100µA		–0.4			V
$V_{OL\_CLKOUTn}$	CLKOUT*n* Output Voltage, Logic Low	CLKOUT*n* V_{OL} Measured with Respect to GND, 2.7V ≤ LDO_{OUT} ≤ 5.2V, $I_{CLKOUTn}$ = 100µA				0.4	V
Temperature Sensor							
ΔV_{TEMP}	Temperature Sensor Forward Voltage, V_{TEMP+} to V_{TEMP-}	I_{TEMP+} = 100µA and I_{TEMP-} = –100µA at T_A = 25°C			0.598		V
$TC_{\Delta V(TEMP)}$	ΔV_{TEMP} Temperature Coefficient				–2.0		mV/°C
η	Ideality Factor				1.004		

Note 1: Stresses beyond those listing under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating conditions for extended periods may affect device reliability and lifetime.

Note 2: The LTM4655 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4655E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls.

The LTM4655I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM4655MP is tested and guaranteed over the full –55°C to 125°C operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: See output current derating curves for different V_{IN}, V_{OUT}, and T_A, located in the Applications Information section.

Note 4: Minimum on-time, PGOOD delay, and $EXTV_{CCn}$ switchover threshold are tested at wafer sort.

Note 5: The two power inputs—V_{IN1} and V_{IN2}—and their respective power outputs—V_{OUT1}^+ or V_{OUT1}^-, and V_{OUT2}^+ or V_{OUT2}^-, depending on operational configuration—are tested independently in production, in both positive-V_{OUT} (noninverting step-down) and negative-V_{OUT}^- (inverting buck-boost) configurations. On occasion, a shorthand notation is used in this document that allows V_{INn} to refer to both V_{IN1} and V_{IN2} by virtue of *n* being permitted to take on a value of 1 or 2. This italicized *n* notation and convention is extended to all such pin names.

Note 6: To ensure minimum on-time criteria is met, V_{OUTn} $(0.5V_{DC})^+$ high line regulation is tested at $13.2V_{IN}$, with f_{SETn} and CLKIN*n* open circuit. V_{OUTn} $(–0.5V_{DC})^-$ low line regulation is tested at $3.6V_{IN}$, with f_{SETn} and CLKIN*n* open circuit.

V_{OUTn} $(–0.5V_{DC})^-$ high line regulation is tested at $28V_{IN}$, and with CLKIN*n* driven at 200kHz—so as to ensure minimum on-time criteria is met. The LTM4655 is not recommended for applications where the minimum on-time criteria (guardband to 90ns) is continuously violated. The LTM4655 can ride through events (such as V_{IN} surge) where the on-time criteria is transiently violated. See the Applications Information section.

Note 7: See the Applications Information section for dropout criteria.

Note 8: V_{OUTn} $(–24V_{DC})^-$ is tested at $3.6V_{IN}$ and $16V_{IN}$, with CLKIN*n* driven with a 1.8MHz clock, ISET*n*a to SV_{OUTn}^- = 12V, and R_{fSET} = 57.6k. It is also tested at $12V_{IN}$, with CLKIN*n* driven with a 1.5MHz clock, R_{fSETn} = 57.6k, and R_{ISETn} = 480k.

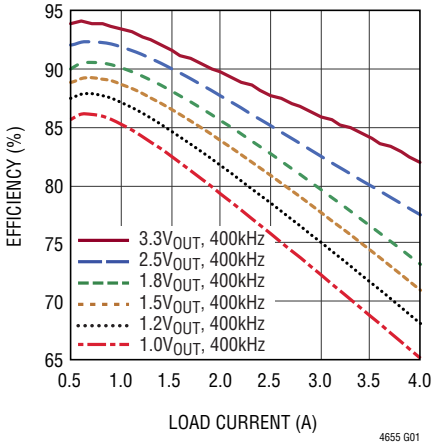
Note 9: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 10: The $INTV_{CCn}$ Abs Max peak output current is specified as the sum of current drawn by circuits internal to the module biased off of $INTV_{CCn}$ and current drawn by external circuits biased off of $INTV_{CCn}$. Specified independently, for each channel. See the Applications Information section.

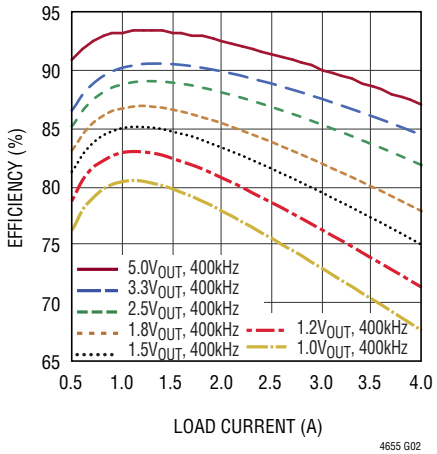
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, single channel positive-V_{OUTn}^+ operation only, unless otherwise noted.

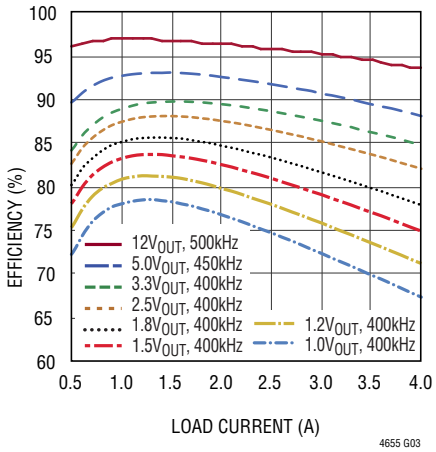
Efficiency vs Load Current at $5V_{IN}$, Forced Continuous Mode



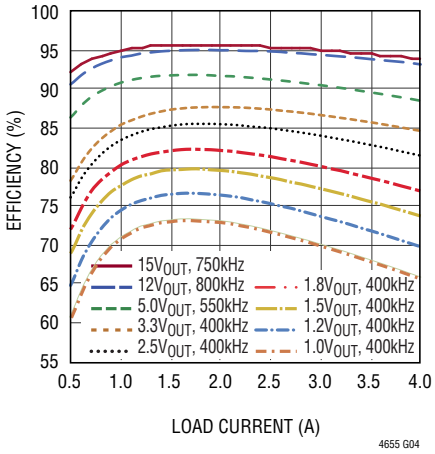
Efficiency vs Load Current at $12V_{IN}$, Forced Continuous Mode



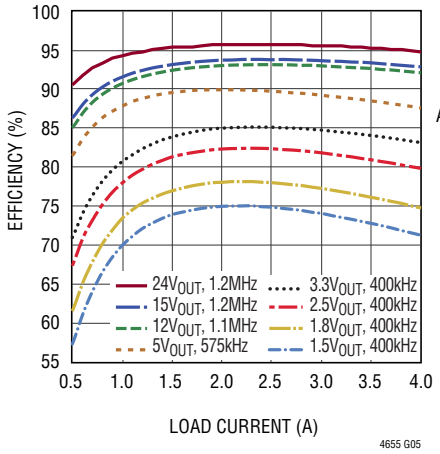
Efficiency vs Load Current at $15V_{IN}$, Forced Continuous Mode



Efficiency vs Load Current at $24V_{IN}$, Forced Continuous Mode



Efficiency vs Load Current at $36V_{IN}$, Forced Continuous Mode



1V Transient Response, $24V_{IN}$

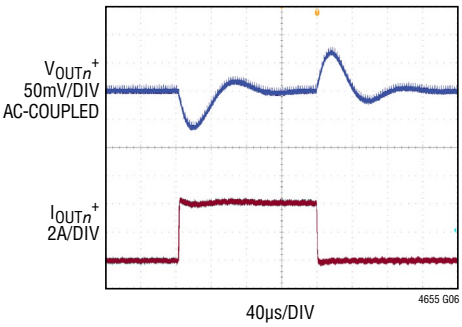


FIGURE 51 CIRCUIT, $24V_{IN}$,
C_{INHn} = C_{Dn} = 4.7µF, C_{OUTn} = 3 x 100µF,
R_{fSETn} = N/A, R_{ISETn} = 20kΩ,
C_{THn} = 6.8nF, R_{THn} = 681Ω,
$R_{EXTVCCn}$ = N/A, $C_{EXTVCCn}$ = N/A,
2A to 4A LOAD STEP AT 2A/µs

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, single channel positive-V_{OUTn}^+ operation only, unless otherwise noted.

Start-Up, No Load

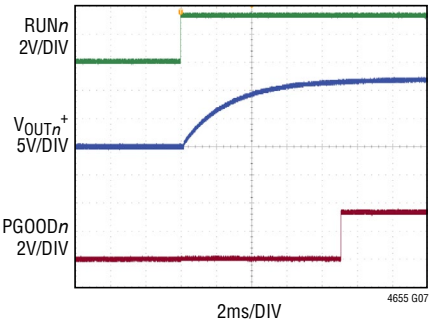


FIGURE 51 CIRCUIT, $36V_{IN}$,
C_{INHn} = C_{Dn} = 4.7µF, C_{OUTn} = 2 x 22µF,
R_{fSETn} = 124k, R_{ISETn} = 240kΩ,
R_{PGDFBn} = 95.3kΩ,
C_{THn} = 10nF, R_{THn} = 562Ω,
$R_{EXTVCCn}$ = 49.9Ω, $C_{EXTVCCn}$ = 1µF,
NO LOAD

Start-Up, 4A Load

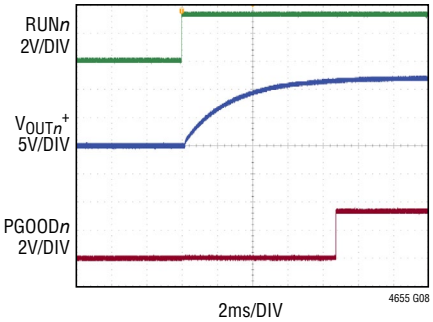


FIGURE 51 CIRCUIT, $36V_{IN}$,
C_{INHn} = C_{Dn} = 4.7µF, C_{OUTn} = 2 x 22µF,
R_{fSETn} = 124k, R_{ISETn} = 240kΩ,
R_{PGDFBn} = 95.3kΩ,
C_{THn} = 10nF, R_{THn} = 562Ω,
$R_{EXTVCCn}$ = 49.9Ω, $C_{EXTVCCn}$ = 1µF,
3Ω RESISTIVE LOAD

Start-Up, Pre-Bias

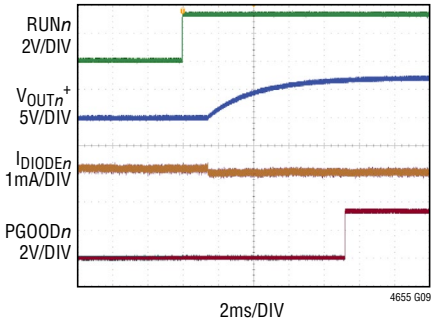


FIGURE 51 CIRCUIT, $36V_{IN}$,
C_{INHn} = C_{Dn} = 4.7µF, C_{OUTn} = 2 x 22µF,
R_{fSETn} = 124k, R_{ISETn} = 240kΩ,
R_{PGDFBn} = 95.3kΩ,
C_{THn} = 10nF, R_{THn} = 562Ω,
$R_{EXTVCCn}$ = 49.9Ω, $C_{EXTVCCn}$ = 1µF,
V_{OUTn}^+ PRE-BIASED TO 5V
THROUGH 1N4148 DIODE

Short Circuit, No Load

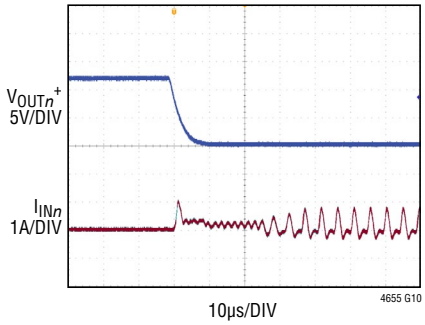


FIGURE 51 CIRCUIT, $36V_{IN}$,
C_{INHn} = C_{Dn} = 4.7µF, C_{OUTn} = 2 x 22µF,
R_{fSETn} = 124k, R_{ISETn} = 240kΩ,
R_{PGDFBn} = 95.3kΩ,
C_{THn} = 10nF, R_{THn} = 562Ω,
$R_{EXTVCCn}$ = 49.9Ω, $C_{EXTVCCn}$ = 1µF,
NO LOAD PRIOR TO APPLICATION
OF OUTPUT SHORT-CIRCUIT

Short Circuit, 4A Load

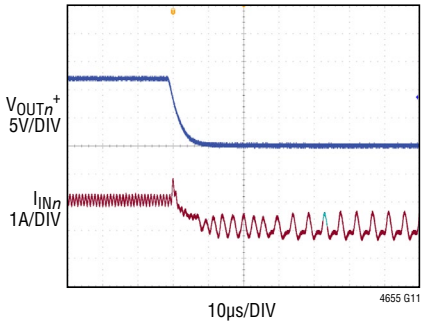
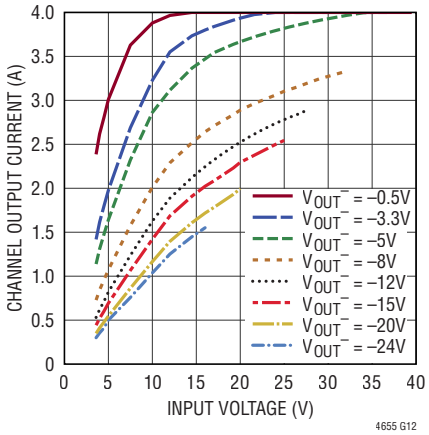


FIGURE 51 CIRCUIT, $36V_{IN}$,
C_{INHn} = C_{Dn} = 4.7µF, C_{OUTn} = 2 x 22µF,
R_{fSETn} = 124k, R_{ISETn} = 240kΩ,
R_{PGDFBn} = 95.3kΩ,
C_{THn} = 10nF, R_{THn} = 562Ω,
$R_{EXTVCCn}$ = 49.9Ω, $C_{EXTVCCn}$ = 1µF,
4Ω RESISTIVE LOAD PRIOR TO
APPLICATION OF OUTPUT
SHORT-CIRCUIT

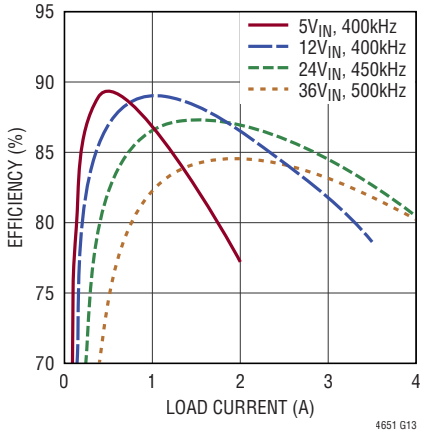
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, single channel negative-V_{OUTn}^- operation only, unless otherwise noted.

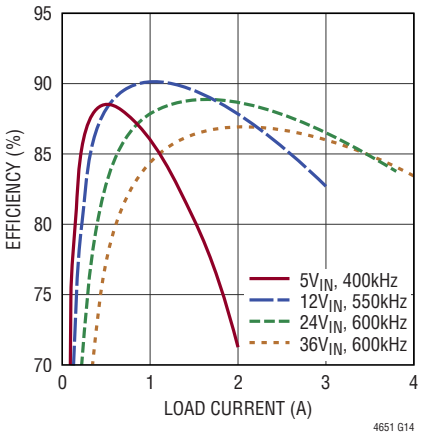
Output Current Capability*



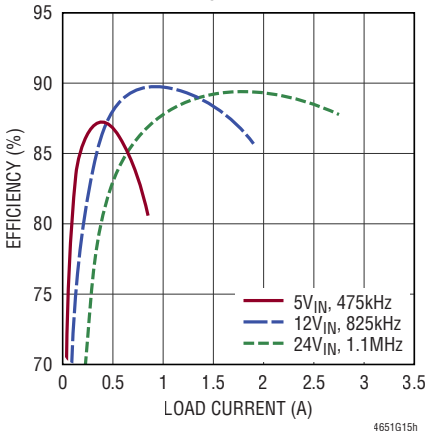
–3.3V Efficiency vs Load Current



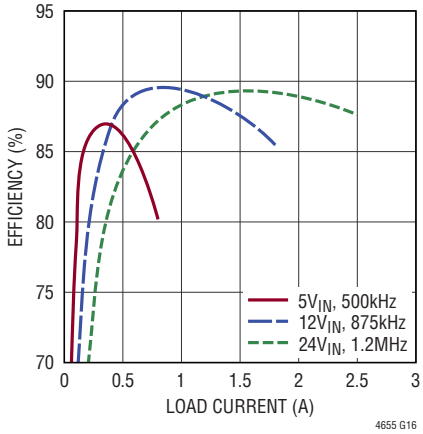
–5V Efficiency vs Load Current



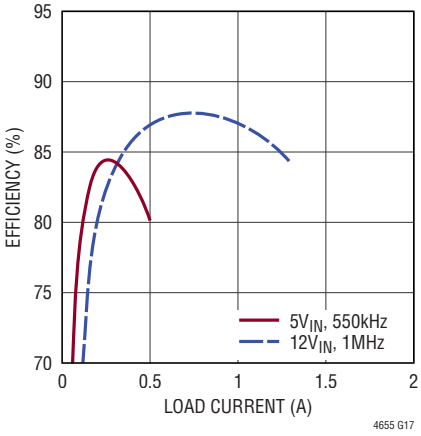
–12V Efficiency vs Load Current



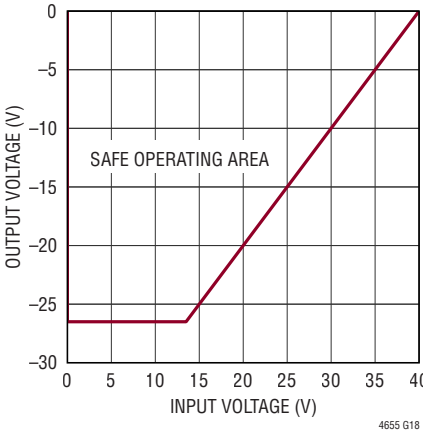
–15V Efficiency vs Load Current



–24V Efficiency vs Load Current



Rated Operating Output Voltage



*Current limit frequency-foldback activates at load currents higher than indicated curves. Continuous channel output current capability subject to details of application implementation. Switching frequency set per Table 1. See Notes 2 and 3.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, single channel negative-V_{OUTn}^- operation only, unless otherwise noted.

–5V Transient Response, 24V_{IN}

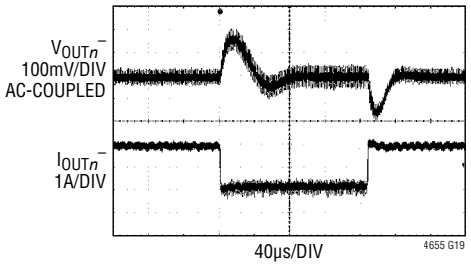


FIGURE 48 CIRCUIT, 24V_{IN},
C_{INOUTn} = C_{INHn} = C_{DGNDn} = C_{Dn} = 4.7µF,
C_{OUTn} = 47µF ×2, R_{fSETn} = 665kΩ,
R_{ISETn} = 100kΩ, R_{PGDFBn} = 36.5kΩ,
$R_{EXTVCCn}$ = 20Ω, 1.8A TO 3.8A LOAD STEP AT 2A/µs

–24V Transient Response, 12V_{IN}

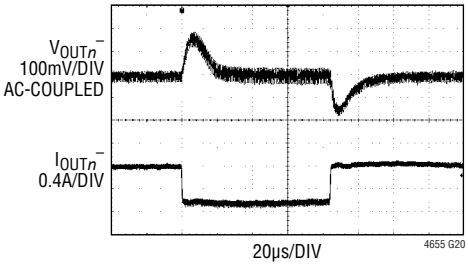


FIGURE 48 CIRCUIT,
0.625A TO 1.25A LOAD STEP AT 0.625A/µs

Start-Up, No Load

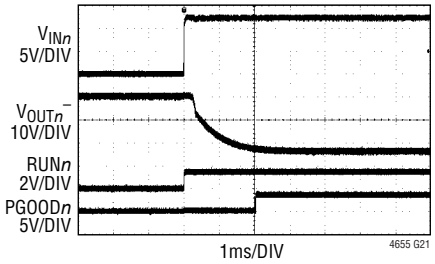


FIGURE 48 CIRCUIT, APPLICATION OF 12V_{IN},
START-UP INTO NO LOAD

Start-Up, 1.25A Load

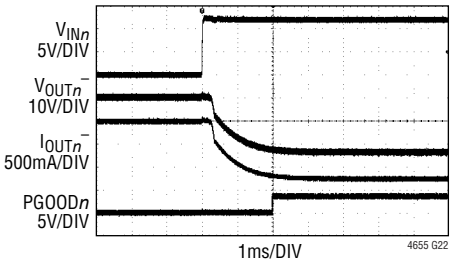


FIGURE 48 CIRCUIT, APPLICATION OF 12V_{IN},
START-UP INTO 19.2Ω LOAD

Start-Up, Pre-Bias

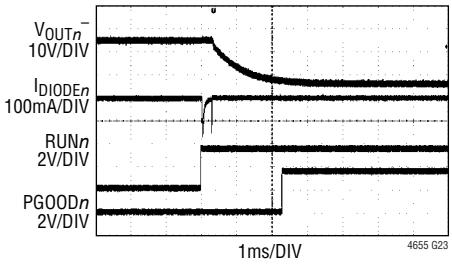


FIGURE 48 CIRCUIT, V_{OUTn}^- PRE-BIASED
TO –5V THROUGH A 1N4148 DIODE PRIOR
TO RUN*n* TOGGLING HIGH

Short Circuit, No Load

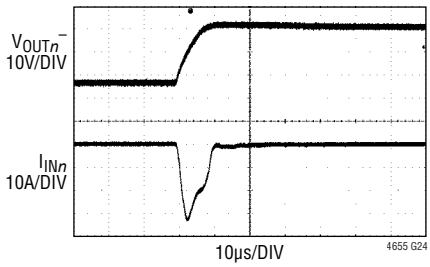


FIGURE 48 CIRCUIT,
NO LOAD PRIOR TO APPLICATION OF
V_{OUTn}^- SHORT-CIRCUIT

Short Circuit, 1.25A Load

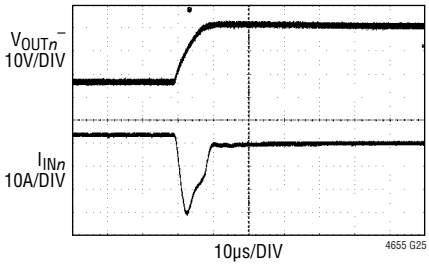


FIGURE 48 CIRCUIT,
19.2Ω LOAD PRIOR TO APPLICATION OF
V_{OUTn}^- SHORT-CIRCUIT

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{IN1} (A1–A3, B3): Channel 1 Power Input Pins. Apply input voltage and input decoupling capacitance directly between V_{IN1} and a power ground (PGND) plane. Either connect PGND to V_{OUT1}^- in noninverting step-down applications, where V_{OUT1}^+ is the regulated positive output voltage—or, connect PGND to V_{OUT1}^+ in inverting buck-boost applications, where V_{OUT1}^- is the regulated negative output voltage.

V_{D1} (A4, B4, C4): Drain of Channel 1's Primary Switching MOSFET. Apply at least one 4.7µF high frequency ceramic decoupling capacitor directly from V_{D1} to V_{OUT1}^-. Give this capacitor higher layout priority (closer proximity to the module) than any V_{IN1} decoupling capacitors.

V_{OUT1}^- (A5, B5, C5, D5, E5, F5, G4–5, H3, H5, J3–5, K4–5, L4–5, M4–5): Negative Power Output of Channel 1. Either connect V_{OUT1}^- to a PGND plane in noninverting step-down applications, where V_{OUT1}^+ is the regulated positive output voltage—or, connect V_{OUT1}^+ to PGND in inverting buck-boost applications, where V_{OUT1}^- is the regulated negative output voltage.

V_{IN2} (A6–A8, B8): Channel 2 Power Input Pins. Apply input voltage and input decoupling capacitance directly between V_{IN2} and a power ground (PGND) plane. Either connect PGND to V_{OUT2}^- in noninverting step-down applications, where V_{OUT2}^+ is the regulated positive output voltage—or, connect PGND to V_{OUT2}^+ in inverting buck-boost applications, where V_{OUT2}^- is the regulated negative output voltage.

V_{D2} (A9, B9, C9): Drain of Channel 2's Primary Switching MOSFET. Apply at least one 4.7µF high frequency ceramic decoupling capacitor directly from V_{D2} to V_{OUT2}^-. Give this capacitor higher layout priority (closer proximity to the module) than any V_{IN2} decoupling capacitors.

V_{OUT2}^- (A10–12, B10, C10, D10–11, E10–11, F10–11, G9–11, H8, H10–12, J8–10, K9–12, L9–12, M9–12): Negative Power Output of Channel 2. Either connect V_{OUT2}^- to a PGND plane in noninverting step-down applications, where V_{OUT2}^+ is the regulated positive output voltage—or, connect V_{OUT2}^+ to PGND in inverting buck-boost applications, where V_{OUT2}^- is the regulated negative output voltage.

CLKIN1 (B1): Channel 1 Mode Select and Oscillator Synchronization Input. Referred to GND. Leave CLKIN1 open circuit for forced continuous mode operation.

Alternatively, this pin can be driven so as to synchronize the switching frequency of channel 1 to a clock signal. In this condition, channel 1 operates in forced continuous mode and the cycle-by-cycle turn-on of its primary MOSFET is coincident with the rising edge of the clock applied to CLKIN1. Note the synchronization range of CLKIN1 is approximately ±40% of the oscillator frequency programmed by the f_{SET1} pin. (See the Applications Information section.) The LTM4655 contains a built-in dual 180° out-of-phase clock generator. Electrically connect CLKIN1 to CLKOUT1 with a short trace, if desired, to synchronize the switching frequency of channel 1 to CLKOUT1. If 0° phase interleaving is desired, connect CLKOUT1 to both CLKIN1 and CLKIN2.

CLKOUT1 (B2): Squarewave Output of Clock Generator for Channel 1. 180° out-of-phase from CLKOUT2. Minimize stray capacitance to this pin. Connect CLKOUT1 to CLKIN1, if desired, to synchronize channel 1 to CLKOUT1. If 0° phase interleaving is desired, connect CLKOUT1 to both CLKIN1 and CLKIN2.

CLKIN2 (B6): Channel 2 Mode Select and Oscillator Synchronization Input. Referred to GND. Leave CLKIN2 open circuit for forced continuous mode operation.

Alternatively, this pin can be driven so as to synchronize the switching frequency of channel 2 to a clock signal. In this condition, channel 2 operates in forced continuous mode and the cycle-by-cycle turn-on of its primary MOSFET is coincident with the rising edge of the clock applied to CLKIN2. Note the synchronization range of CLKIN2 is approximately ±40% of the oscillator frequency programmed by the f_{SET2} pin. (See the Applications Information section.) The LTM4655 contains a built-in dual 180° out-of-phase clock generator. Electrically connect CLKIN2 to CLKOUT2 with a short trace, if desired, to synchronize the switching frequency of channel 2 to CLKOUT2. If 0° phase interleaving is desired, connect CLKOUT1 to both CLKIN1 and CLKIN2.

PIN FUNCTIONS

CLKOUT2 (B7, C12): Squarewave Output of Clock Generator for Channel 2. 180° out-of-phase from CLKOUT1. Minimize stray capacitance to these pins. Connect CLKOUT2 (pin B7, only) to CLKIN2, if desired, to synchronize channel 2 to CLKOUT2. If 0° phase interleaving is desired, connect CLKOUT1 to both CLKIN1 and CLKIN2.

To disable spread spectrum frequency modulation (SSFM), connect CLKOUT2 (pin C12, only) to the MOD pin (pin E12) with a short trace.

The CLKOUT2 pins at locations B7 and C12 are electrically connected together by a signal trace internal to the module. It is pinned out as described purely to facilitate routing of short traces to CLKIN2 and MOD. CLKOUT2 should be routed with minimal trace lengths. Minimize stray capacitance to these pins.

SV_{INF1} (B11): Channel 1 Filtered Voltage Supply for Small Signal Circuits. If powering the LTM4655's 5V LDO from channel 1's supply for small signal circuits, electrically connect SV_{INF1} and LDO_{IN} with a short trace capable of carrying up to 25mA.

LDO_{IN} (B12): Input to 5V LDO. Connect LDO_{IN} to either SV_{INF1} or SV_{INF2} with a short trace capable of carrying up to 25mA, depending on which input rail is better suited for powering the 5V LDO. If LDO_{IN} is being powered from SV_{INF1} or SV_{INF2}, no bypass capacitance from LDO_{IN} to GND is needed; otherwise, 0.1µF-to-1µF local bypass capacitance is recommended.

IMON1b (C1): Channel 1 Power Inductor Analog Indicator Current Default Termination R-C Network. A 10k resistor in parallel with a 10nF capacitor and terminating to SV_{OUT1}^- connect to this pin. Connect IMON1b to IMON1a to achieve default power inductor analog indicator current characteristics: 1V (with respect to SV_{OUT1}^-) at full-scale (4A) load current in positive-V_{OUT}, noninverting step-down applications. (See IMON1a.) If unused, IMON1b can be left open circuit or connected to SV_{OUT1}^-.

IMON1a (C2): Channel 1 Power Inductor Current Analog Indicator Pin and Current Limit Programming Pin. In positive-V_{OUT} step-down applications, only, the current flowing out of this pin is equal to 1/40,000 of the average channel 1 power inductor current. Optionally apply a parallel resistor-capacitor network to this pin and terminate it to SV_{OUT1}^- in order to construct a voltage (V_{IMON1a}–SV_{OUT1}^-) that is proportional to channel 1's power inductor current.

IMON1a can be connected to IMON1b if the default resistor capacitor termination network provided by IMON1b is desired. If this analog indicator feature is not desired—or, in negative-V_{OUT}^- buck-boost applications: connect IMON1a to SV_{OUT1}^-.

If IMON1a–SV_{OUT1}^- exceeds a trip threshold of approximately 2V, an IMON1 control loop servos channel 1 power inductor current accordingly and thus regulates IMON1a–SV_{OUT1}^- at 2V. In this manner, the current limit inception threshold of channel 1 can be configured. (See the Applications Information section.)

SV_{IN1} (C3): Channel 1 Input Voltage Supplies for Small Signal Circuits. SV_{IN1} is the input to the $INTV_{CC1}$ LDO. Connect SV_{IN1} directly to V_{IN1}.

IMON2b (C6): Channel 2 Power Inductor Analog Indicator Current Default Termination R-C Network. A 10k resistor in parallel with a 10nF capacitor and terminating to SV_{OUT2}^- connect to this pin. Connect IMON2b to IMON2a to achieve default power inductor analog indicator current characteristics: 1V (with respect to SV_{OUT2}^-) at full-scale (4A) load current in positive-V_{OUT}, noninverting step-down applications. (See IMON2a.) If unused, IMON2b can be left open circuit or connected to SV_{OUT2}^-.

IMON2a (C7): Channel 2 Power Inductor Current Analog Indicator Pin and Current Limit Programming Pin. In positive-V_{OUT} step-down applications, only, the current flowing out of this pin is equal to 1/40,000 of the average channel 2 power inductor current. Optionally apply a parallel resistor-capacitor network to this pin and terminate it to SV_{OUT2}^- in order to construct a voltage (V_{IMON2a}–SV_{OUT2}^-) that is proportional to channel 2's power inductor current.

IMON2a can be connected to IMON2b if the default resistor capacitor termination network provided by IMON2b is

PIN FUNCTIONS

desired. If this analog indicator feature is not desired—or, in negative-V_{OUT}^- buck-boost applications: connect IMON2a to SV_{OUT2}^-.

If IMON2a–SV_{OUT2}^- exceeds a trip threshold of approximately 2V, an IMON2 control loop servos channel 2 power inductor current accordingly and thus regulates IMON2a–SV_{OUT2}^- at 2V. In this manner, the current limit inception threshold of channel 2 can be configured. (See the Applications Information section.)

SV_{IN2} (C8): Channel 2 Input Voltage Supplies for Small Signal Circuits. SV_{IN2} is the input to the $INTV_{CC2}$ LDO. Connect SV_{IN2} directly to V_{IN2}.

SV_{INF2} (C11): Channel 2 Filtered Voltage Supply for Small Signal Circuits. If powering the LTM4655's 5V LDO from channel 2's supply for small signal circuits, electrically connect SV_{INF2} and LDO_{IN} with a short trace capable of carrying up to 25mA.

PGOOD1 (D1): Channel 1 Power Good Indicator, Open-Drain Output Pin. PGOOD1 is high impedance when PGDFB1–SV_{OUT1}^- is within approximately ±7.5% of 0.6V. PGOOD1 is pulled to GND when PGDFB1 is outside this range.

PGDFB1 (D2): Channel 1 Power Good Feedback Programming Pin. Connect PGDFB1 to V_{OSNS1}^+ through a resistor, R_{PGDFB1}. R_{PGDFB1} configures the voltage threshold of ($V_{OUT1}^+ – V_{OUT1}^-$) for which PGOOD1 toggles its state. If the PGOOD1 feature is used, set R_{PGDFB1} to:

$$R_{PGDFB1} = \left[\frac{V_{OUT1}^+ - V_{OUT1}^-}{0.6V} - 1\right] \bullet 4.99k \qquad (1)$$

Otherwise, leave PGDFB1 open circuit.

A small filter capacitor (220pF) internal to the LTM4655 on this pin provides high frequency noise immunity for the PGOOD1 output indicator.

VINREG1 (D3): Channel 1 Input Voltage Regulation Programming Pin. Optionally connect this pin to the midpoint node formed by a resistor divider between V_{D1} and V_{OUT1}^-. If VINREG1–SV_{OUT1}^- falls below approximately 2V, a VINREG1 control loop servos the power inductor current accordingly and thus regulates VINREG1 at 2V with respect to SV_{OUT1}^-. (See the Applications Information section.)

If this input voltage regulation feature is not desired on channel 1, connect VINREG1 to $INTV_{CC1}$.

GND (D4, D9, D12): Ground Pins. The logic thresholds for RUN*n*, PGOOD*n*, and CLKINn are electrically referred to GND. GND is also the reference voltage for the 5V-fixed LDO and the CLKOUT*n* clock generator. Connect all GND pins to a solid ground plane, PGND.

PGOOD2 (D6): Channel 2 Power Good Indicator, Open-Drain Output Pin. PGOOD2 is high impedance when PGDFB2–SV_{OUT2}^- is within approximately ±7.5% of 0.6V. PGOOD2 is pulled to GND when PGDFB2 is outside this range.

PGDFB2 (D7): Channel 2 Power Good Feedback Programming Pin. Connect PGDFB2 to V_{OSNS2}^+ through a resistor, R_{PGDFB2}. R_{PGDFB2} configures the voltage threshold of ($V_{OUT2}^+ – V_{OUT2}^-$) for which PGOOD2 toggles its state. If the PGOOD2 feature is used, set R_{PGDFB2} according to Equation 2.

$$R_{PGDFB2} = \left[\frac{V_{OUT2}^+ - V_{OUT2}^-}{0.6V} - 1\right] \bullet 4.99k \qquad (2)$$

Otherwise, leave PGDFB2 open circuit.

A small filter capacitor (220pF) internal to the LTM4655 on this pin provides high frequency noise immunity for the PGOOD2 output indicator.

VINREG2 (D8): Channel 2 Input Voltage Regulation Programming Pin. Optionally connect this pin to the midpoint node formed by a resistor divider between V_{D2} and V_{OUT2}^-. If VINREG2–SV_{OUT2}^- falls below approximately 2V, a VINREG2 control loop servos the power inductor current accordingly and thus regulates VINREG2 at 2V with respect to SV_{OUT2}^-. (See the Applications Information section.)

If this input voltage regulation feature is not desired on channel 2, connect VINREG2 to $INTV_{CC2}$.

PIN FUNCTIONS

COMP1b (E1): Channel 1 Internal Loop Compensation Network. For a majority of applications, the internal, default loop compensation of the LTM4655 is suitable to apply "as is", and yields very satisfactory results: apply the default loop compensation to channel 1's control loop by simply connecting COMP1a to COMP1b. When more specialized applications require a personal touch to the optimization of control loop response, this can be easily accomplished by connecting a series resistor-capacitor network from COMP1a to SV_{OUT1}^- and leaving COMP1b open circuit.

COMP1a (E2): Current Control Threshold and Error Amplifier Compensation Node for Channel 1. The trip threshold of channel 1's current comparator increases with a respective rise in COMP1a voltage. A small filter cap (10pF) internal to the LTM4655 on this pin introduces a high frequency roll-off of the error amplifier response, yielding good noise rejection in the control loop. Often, COMP1a is electrically connected to COMP1b in one's application, thus applying default loop compensation. Loop compensation (a series resistor capacitor) can be applied externally from COMP1a to SV_{OUT1}^-, if desired or needed, instead. (See COMP1b.)

f_{SET1} (E3): Channel 1 Oscillator Frequency Programming Pin. The default switching frequency of channel 1 is 400kHz. If needed, the programmed frequency can be increased by connecting a resistor between f_{SET1} and SV_{OUT1}^-. Keep f_{SET1}-related trace lengths short. (See the Applications Information section.) Note the synchronization range of CLKIN1 is approximately ±40% of the oscillator frequency programmed by this f_{SET1} pin.

SV_{OUT1}^- (E4, G2, H2): Signal Return of Channel 1. The SV_{OUT1}^- pins are the reference node for channel 1's control loop. A small island of SV_{OUT1}^- copper should be extended from the module and used to shield sensitive channel 1 pins and signals from noise—such as those routing to f_{SET1}, ISET1a/b, and COMP1a/b. All SV_{OUT1}^- pins are connected to each other internal to the module. Connect Pin H2 to V_{OUT1}^- directly under the LTM4655. The remaining SV_{OUT1}^- pins can be used for redundant connectivity or routed to an ICT test point for design-for-test considerations, as desired. See the Applications Information section for the layout checklist.

COMP2b (E6): Channel 2 Internal Loop Compensation Network. For a majority of applications, the internal, default loop compensation of the LTM4655 is suitable to apply "as is", and yields very satisfactory results: apply the default loop compensation to channel 2's control loop by simply connecting COMP2a to COMP2b. When more specialized applications require a personal touch to the optimization of control loop response, this can be easily accomplished by connecting a series resistor-capacitor network from COMP2a to SV_{OUT2}^- and leaving COMP2b open circuit.

COMP2a (E7): Current Control Threshold and Error Amplifier Compensation Node for Channel 2. The trip threshold of channel 2's current comparator increases with a respective rise in COMP2a voltage. A small filter cap (10pF) internal to the LTM4655 on this pin introduces a high frequency roll-off of the error amplifier response, yielding good noise rejection in the control loop. Often, COMP2a is electrically connected to COMP2b in one's application, thus applying default loop compensation. Loop compensation (a series resistor capacitor) can be applied externally from COMP2a to SV_{OUT2}^-, if desired or needed, instead. (See COMP2b.)

f_{SET2} (E8): Channel 2 Oscillator Frequency Programming Pin. The default switching frequency of channel 2 is 400kHz. If needed, the programmed frequency can be increased by connecting a resistor between f_{SET2} and SV_{OUT2}^-. Keep f_{SET2}-related trace lengths short. (See the Applications Information section.) Note the synchronization range of CLKIN2 is approximately ±40% of the oscillator frequency programmed by this f_{SET2} pin.

SV_{OUT2}^- (E9, G7, H7): Signal Return of Channel 2. The SV_{OUT2}^- pins are the reference node for channel 2's control loop. A small island of SV_{OUT2}^- copper should be extended from the module and used to shield sensitive channel 2 pins and signals from noise—such as those routing to f_{SET2}, ISET2a/b, and COMP2a/b. All SV_{OUT2}^- pins are connected to each other internal to the module. Connect Pin H7 to V_{OUT2}^- directly under the LTM4655. The remaining SV_{OUT2}^- pins can be used for redundant connectivity or routed to an ICT test point for design-for-test considerations, as desired. See the Applications Information section for the layout checklist.

PIN FUNCTIONS

MOD (E12): Modulation Setting Input. This three-state input selects among four modulation rate settings. The MOD pin should be tied to GND for the f_{OUT}/16 modulation rate. Leaving the MOD pin open circuit selects the f_{OUT}/32 modulation rate. The MOD pin should be electrically connected to LDO_{OUT} for the f_{OUT}/64 modulation rate. Electrically connecting CLKOUT2 (pin C12, only) to the MOD pin (pin E12) turns the modulation off. Do not route high speed digital logic or signals with fast edges near MOD. Be advised that the f_{OUT}/16, f_{OUT}/32 and f_{OUT}/64 modulation rates are not explicitly tested in factory ATE to demonstrate their stated typical modulation rates; the **modulation off** setting, however, is.

ISET1b (F1): 1.5nF Soft-Start Capacitor for Channel 1. Connect ISET1b to ISET1a to achieve default soft-start characteristics on channel 1, if desired. See ISET1a.

ISET1a (F2): Accurate 50µA Current Source. Positive input to the error amplifier of channel 1. Connect a resistor $R_{ISET1a} = ((V_{OUT1}^+ – V_{OUT1}^–)/50µA)$ from this pin to $SV_{OUT1}^–$ local to the module to program the desired channel 1 output voltage magnitude, $V_{OUT1}^+ – V_{OUT1}^–$. A capacitor can be connected from ISET1a to $SV_{OUT1}^–$ to soft-start channel 1's output voltage, i.e., reduce its start-up inrush current. Connect ISET1a to ISET1b in order to achieve default soft-start characteristics if desired. (See ISET1b.)

$EXTV_{CC1}$ (F3): External Bias, Auxiliary Input to the $INTV_{CC1}$ Regulator. When $EXTV_{CC1}–V_{OUT1}^–$ > 3.2V and SV_{IN1} > 5V and RUN1–GND > 1.2V, the $INTV_{CC1}$ LDO derives power from $EXTV_{CC1}$ bias instead of SV_{IN1}. This technique reduces LDO losses considerably, resulting in a corresponding reduction in module junction temperature. For applications in which $4V < V_{OUT1}^+ – V_{OUT1}^– <$ 28V, connect $EXTV_{CC1}$ to V_{OUT1}^+ through a 15Ω~110Ω resistor and locally decouple $EXTV_{CC1}$ to $V_{OUT1}^–$ with a 1µF ceramic capacitor. Otherwise, connect $EXTV_{CC1}$ to $V_{OUT1}^–$ or leave $EXTV_{CC1}$ open circuit. See the Applications Information section.

RUN1 (F4): Channel 1 Run Control Pin. A voltage above ~1.2V (with respect to GND) commands the module to regulate its output voltage. Undervoltage lockout (UVLO) can be implemented by connecting RUN1 to the midpoint node formed by a resistor divider between V_{IN1} and GND. RUN1 features ~130mV of hysteresis.

ISET2b (F6): 1.5nF Soft-Start Capacitor for Channel 2. Connect ISET2b to ISET2a to achieve default soft-start characteristics on channel 2, if desired. See ISET2a.

In addition, the channel 1 output of the LTM4655 can track a voltage applied to this pin. (See the Applications Information section.)

ISET2a (F7): Accurate 50µA Current Source. Positive input to the error amplifier of channel 1. Connect a resistor $R_{ISET2a} = ((V_{OUT2}^+ – V_{OUT2}^–)/50µA)$ from this pin to $SV_{OUT2}^–$ local to the module to program the desired channel 2 output voltage magnitude, $V_{OUT2}^+ – V_{OUT2}^–$. A capacitor can be connected from ISET2a to $SV_{OUT2}^–$ to soft-start channel 2's output voltage, i.e., reduce its start-up inrush current. Connect ISET2a to ISET2b in order to achieve default soft-start characteristics if desired. (See ISET2b.)

In addition, the channel 2 output of the LTM4655 can track a voltage applied to this pin. (See the Applications Information section.)

$EXTV_{CC2}$ (F8): External Bias, Auxiliary Input to the $INTV_{CC2}$ Regulator. When $EXTV_{CC2}–V_{OUT2}^–$ > 3.2V and SV_{IN2} > 5V and RUN2–GND >1.2V, the $INTV_{CC2}$ LDO derives power from $EXTV_{CC2}$ bias instead of SV_{IN2}. This technique reduces LDO losses considerably, resulting in a corresponding reduction in module junction temperature. For applications in which $4V < V_{OUT2}^+ – V_{OUT2}^– <$ 28V, connect $EXTV_{CC2}$ to V_{OUT2}^+ through a 15Ω~110Ω resistor and locally decouple $EXTV_{CC2}$ to $V_{OUT2}^–$ with a 1µF ceramic capacitor. Otherwise, connect $EXTV_{CC2}$ to $V_{OUT2}^–$ or leave $EXTV_{CC2}$ open circuit. See the Applications Information section.

RUN2 (F9): Channel 2 Run Control Pin. A voltage above ~1.2V (with respect to GND) commands the module to regulate its output voltage. Undervoltage lockout (UVLO) can be implemented by connecting RUN2 to the midpoint node formed by a resistor divider between V_{IN2} and GND. RUN2 features ~130mV of hysteresis.

PIN FUNCTIONS

CLKSET (F12): Clock Generator Frequency Setting Resistor Input. Apply a resistor, R_{CLKSET}, between LDO_{OUT} and CLKSET. The clock frequency of CLKOUT1 and CLKOUT2 is set by R_{CLKSET}, according Equation 3.

$$f_{(CLKOUT1,\ CLKOUT2)} = 10MHz \bullet \frac{10k\Omega}{R_{CLKSET}(k\Omega)} \qquad (3)$$

Resistor values between 32.2k and 499k are supported, corresponding to oscillator frequency settings of 3MHz to 200kHz, respectively. Minimize stray capacitance to this pin.

V_{OSNS1}^+ (G1, H1): Positive Voltage Sense Input for Channel 1. Route a signal trace from V_{OSNS1}^+ to V_{OUT1}^+ at channel 1's point-of-load (POL). This provides the feedback signal to channel 1's control loop. In noisy environments, shield V_{OSNS1}^+ from electrical noise by sandwiching the trace between PGND copper. Pins G1 and H1 are electrically connected to each other internal to the module, and thus it is only necessary to connect one V_{OSNS1}^+ pin to V_{OUT1}^+ at the POL. The remaining V_{OSNS1}^+ pin can be used for redundant connectivity or routed to an ICT test point for design-for-test considerations, as desired.

$INTV_{CC1}$ (G3): Channel 1 Internal Regulator, 3.3V Output with Respect to V_{OUT1}^-. Channel 1 internal control circuits and MOSFET drivers derive power from $INTV_{CC1}$ bias. Leave $INTV_{CC1}$ open circuit. An LDO generates $INTV_{CC1}$ from either SV_{IN1} or $EXTV_{CC1}$, when RUN1 is logic high (RUN1–GND > 1.2V). The $INTV_{CC1}$ LDO is turned off when RUN1 is logic low (RUN1–GND < 1.2V). (See $EXTV_{CC1}$.)

V_{OSNS2}^+ (G6, H6): Positive Voltage Sense Input for Channel 2. Route a signal trace from V_{OSNS2}^+ to V_{OUT2}^+ at channel 2's point-of-load (POL). This provides the feedback signal to channel 2's control loop. In noisy environments, shield V_{OSNS2}^+ from electrical noise by sandwiching the trace between PGND copper. Pins G6 and H6 are electrically connected to each other internal to the module, and thus it is only necessary to connect one V_{OSNS2}^+ pin to V_{OUT2}^+ at the POL. The remaining V_{OSNS2}^+ pin can be used for redundant connectivity or routed to an ICT test point for design-for-test considerations, as desired.

$INTV_{CC2}$ (G8): Channel 2 Internal Regulator, 3.3V Output with Respect to V_{OUT2}^-. Channel 2 internal control circuits and MOSFET drivers derive power from $INTV_{CC2}$ bias. Leave $INTV_{CC2}$ open circuit. An LDO generates $INTV_{CC2}$ from either SV_{IN2} or $EXTV_{CC2}$, when RUN2 is logic high (RUN2–GND > 1.2V). The $INTV_{CC2}$ LDO is turned off when RUN2 is logic low (RUN2–GND < 1.2V). (See $EXTV_{CC2}$.)

LDO_{OUT} (G12): Output of the LTM4655's GND Referenced 5V-Fixed LDO. No bypass capacitance is needed. Powers the clock generator internal to the LTM4655. Can deliver up to 25mA of current.

SW1 (H4): Switching Node of Channel 1 Switching Converter Stage. Used for test purposes. May be routed a short distance with a thin trace to a local test point to monitor switching action of the converter, if desired, but do not route near any sensitive signals; otherwise, leave electrically open circuit.

SW2 (H9): Switching Node of Channel 2 Switching Converter Stage. Used for test purposes. May be routed a short distance with a thin trace to a local test point to monitor switching action of the converter, if desired, but do not route near any sensitive signals; otherwise, leave electrically open circuit.

NC (J1–2, J11–12): No Connect Pins, i.e., Pins with No Internal Connection. The NC pins predominantly serve to provide improved mounting of the module to the board. For drop-in compatibility of the LTM4651/LTM4653 into either half of a LTM4655 layout, these NC are recommended to be left electrically open circuit.

$TEMP^+$ (J6): Temperature Sensor, Positive Input. Emitter of a 2N3906-genre PNP bipolar junction transistor (BJT). Optionally interface to temperature monitoring circuitry such as LTC®2997, LTC2990, LTC2974 or LTC2975. Otherwise leave electrically open.

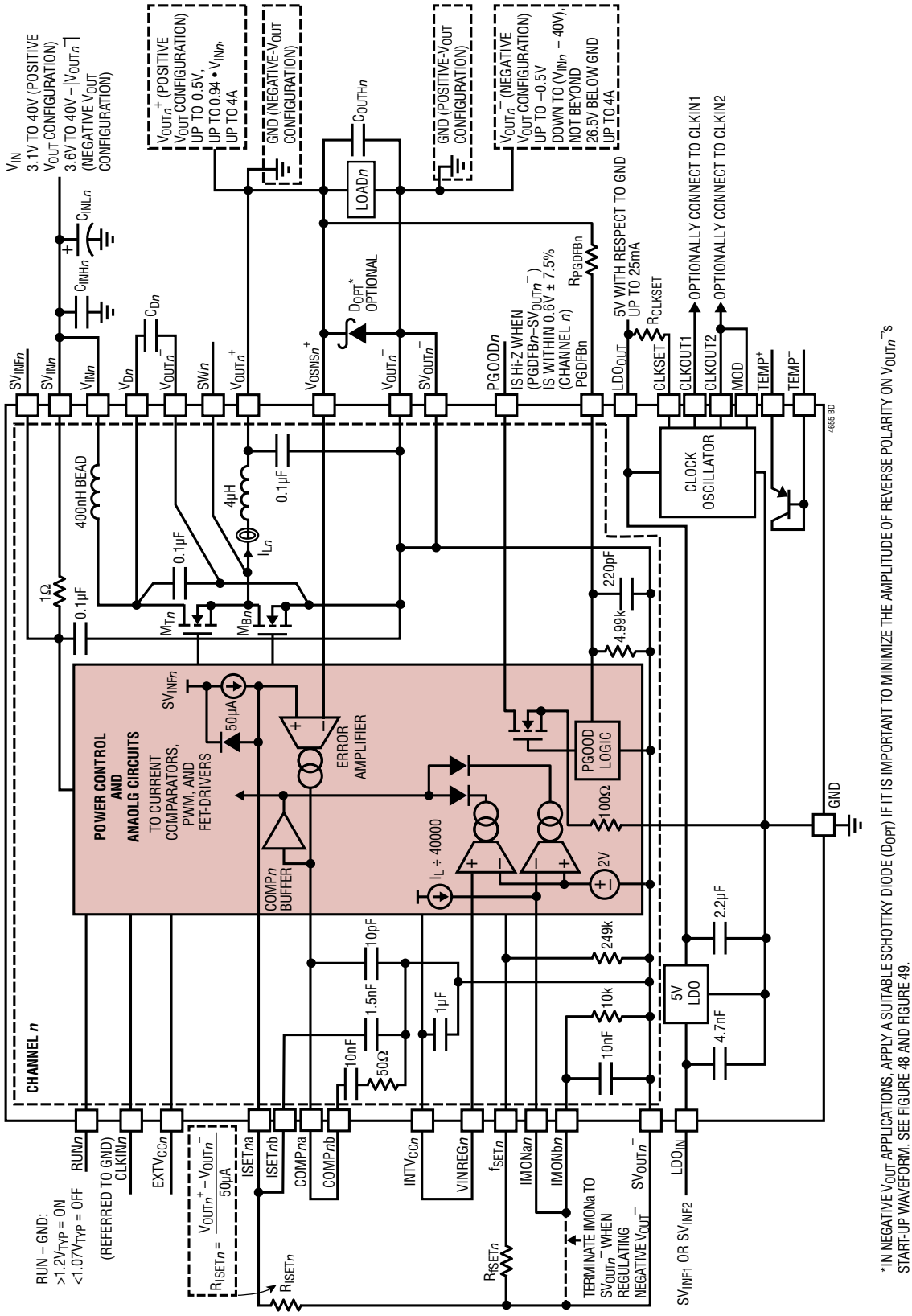
$TEMP^-$ (J7): Temperature Sensor, Negative Input. Collector and base of a 2N3906-genre PNP bipolar junction transistor (BJT). Optionally interface to temperature monitoring circuitry such as LTC2997, LTC2990, LTC2974 or LTC2975. Otherwise leave electrically open.

PIN FUNCTIONS

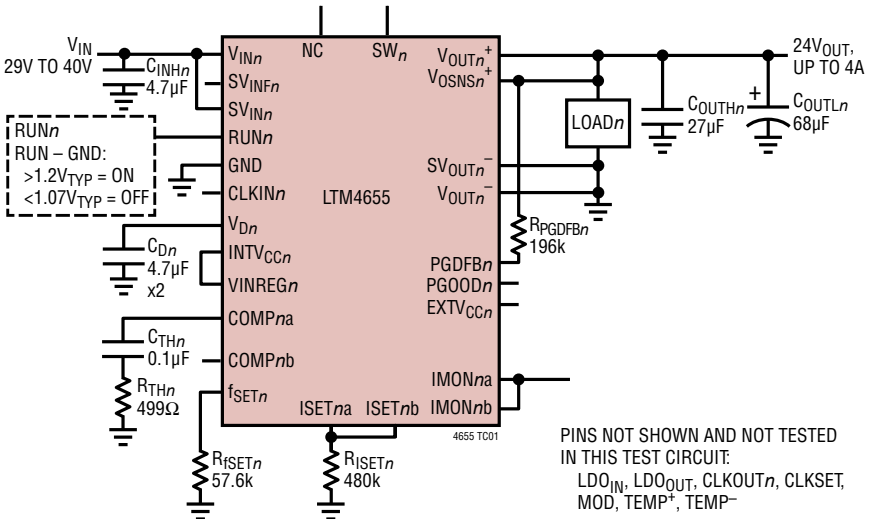
V_{OUT1}^+ (K1–3, L1–3, M1–3): Positive Power Output of Channel 1. Bypass V_{OUT1}^+ to V_{OUT1}^- local to the module with at least 1µF. The remainder of V_{OUT1}^+ to V_{OUT1}^- bypass caps should be located near channel 1's load. Either connect V_{OUT1}^+ to a PGND plane in inverting buck-boost applications, where V_{OUT1}^- is the regulated negative output voltage—or, connect V_{OUT1}^- to a PGND plane noninverting step-down applications, where V_{OUT1}^+ is the regulated positive output voltage.

V_{OUT2}^+ (K6–8, L6–8, M6–8): Positive Power Output of Channel 2. Bypass V_{OUT2}^+ to V_{OUT2}^- local to the module with at least 1µF. The remainder of V_{OUT2}^+ to V_{OUT2}^- bypass caps should be located near channel 2's load. Either connect V_{OUT2}^+ to a PGND plane in inverting buck-boost applications, where V_{OUT2}^- is the regulated negative output voltage—or, connect V_{OUT2}^- to a PGND plane noninverting step-down applications, where V_{OUT2}^+ is the regulated positive output voltage.

SIMPLIFIED BLOCK DIAGRAM (Only One Channel Shown Within Dotted Outlines)

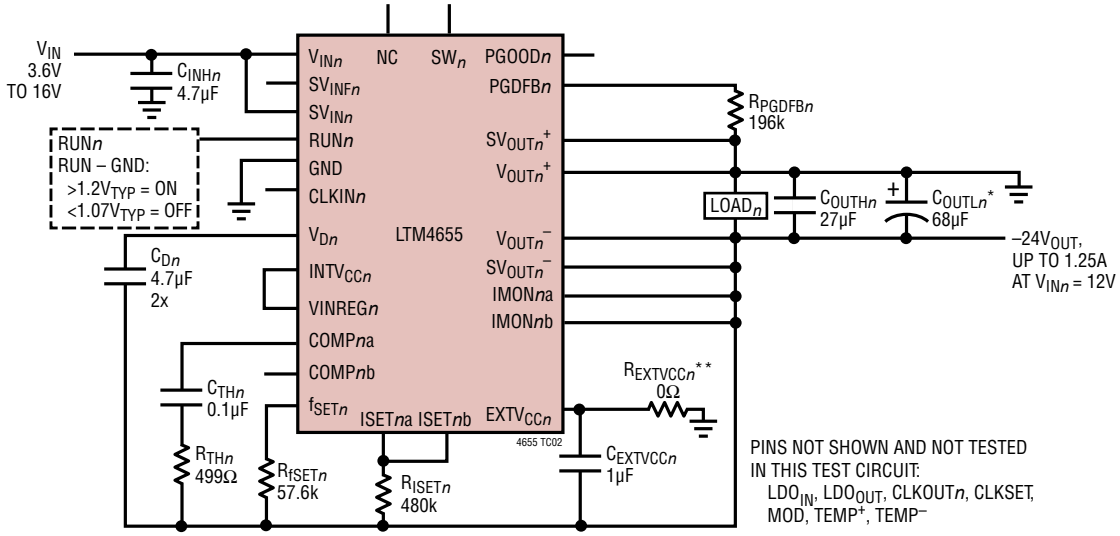


TEST CIRCUIT



Test Circuit 1. Positive-V_{OUT} Configuration, Regulating V_{OUTn}^{+}, One Channel Shown

TEST CIRCUIT

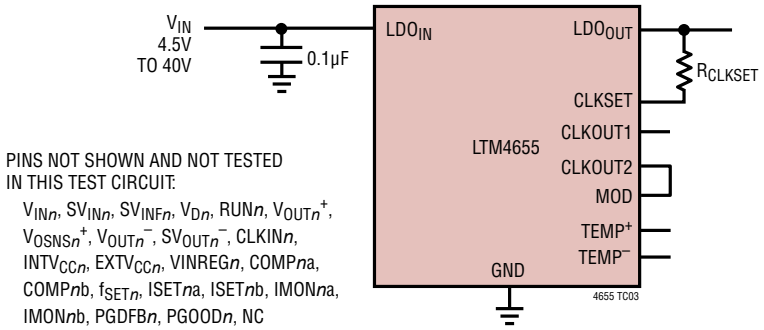


*Polarized output capacitors C_{OUTL}, if used, must be rated to withstand ~0.3V typical reverse polarity prior to LTM4655 start-up, stemming from a weakly forward-biased body diode. In such cases, a Schottky diode should be placed local to the LTM4655 and electrically connected between PGND and V_{OUTn}^- to limit the voltage. See the Applications Information section and Figures 49a and 49b.

**Outside the ATE Test environment, $R_{EXTVCCn}$, if used, should not be 0Ω. See the Applications Information section.

Test Circuit 2. Negative-V_{OUT}^- Configuration, Regulating V_{OUTn}^-, One Channel Shown

TEST CIRCUIT



Test Circuit 3. Clock-Generator, 5V LDO and Temperature-Sensor

DECOUPLING REQUIREMENTS

T_A = 25°C. Refer to Test Circuit 1 and Test Circuit 2.

APPLICATION	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Positive-V_{OUT} Operation (Noninverting Step-Down) (Test Circuit 1)	C_{INHn}, C_{Dn}	External High Frequency Input Capacitor Requirement, 27V ≤ V_{IN1}–GND1 ≤40V, V_{OUT}^+ = 24V	I_{OUT}^+ = 4A		9.4		µF
	C_{OUTHn}	External High Frequency Output Capacitor Requirement 27V ≤ V_{IN1}–GND1 ≤ 40V, V_{OUT}^+ = 24V	I_{OUT}^+ = 4A		22		µF
Negative-V_{OUT}^- Operation (Inverting Output Buck-Boost) (Test Circuit 2)	C_{INHn}, C_{Dn}	External High Frequency Input Capacitor Requirement, 3.6V ≤ V_{IN2}–GND2 ≤ 16V, V_{OUT}^- = –24V	I_{OUT}^- = 2A		9.4		µF
	C_{OUTHn}	External High Frequency Output Capacitor Requirement 3.6V ≤ V_{IN2}–GND2 ≤ 16V, V_{OUT}^- = –24V	I_{OUT}^- = 2A		22		µF

OPERATION

Power Module Overview

The LTM4655 is a dual-channel non-isolated switch mode DC/DC power supply. Each channel is fully independent of the other. Each output can be configured for positive or negative polarity. A channel configured for positive-V_{OUT} operation performs step-down DC/DC conversion and regulates a positive output voltage, V_{OUTn}^+. A channel configured for negative-V_{OUT}^- operation performs two-switch buck-boost DC/DC conversion and regulates a negative output voltage, V_{OUTn}^- (this topology is also known as a ground-referred buck converter).

An integrated LDO provides up to 25mA of output current at +5V (LDO_{OUT}) with respect to GND. This LDO powers an internal 2-phase clock oscillator, yielding flexibility to operate the switching channels 180° out-of-phase from each other.

A channel in positive-V_{OUT} configuration (see Test Circuit 1) can deliver up to 4A output current with a few external input and output capacitors. Set by a single resistor, R_{ISETn}, an LTM4655 channel regulates a positive output voltage, V_{OUTn}^+. V_{OUTn}^+ can be set to as low as 0.5V to as high as 26.5V. Channels in this positive-V_{OUT} configuration can operate from a positive input supply rail, V_{INn}, between 3.1V and 40V. The typical application schematic is shown in Figure 45.

A channel in negative-V_{OUT}^- configuration (see Test Circuit 2) can deliver up to 4A output current with a few external input and output capacitors. The output current capability of the LTM4655 channel in this configuration is dependent on its V_{INn} and V_{OUTn}, as indicated in Figure 6. Set by a single resistor, R_{ISETn}, the LTM4655 channel regulates a negative output voltage, V_{OUTn}^-. V_{OUTn}^- can be set to as low as –26.5V to as high as –0.5V. In this negative-V_{OUT} configuration, an LTM4655 channel can operate from a positive input supply rail, V_{INn}, between 3.6V and 40V. The LTM4655 channel's safe operating area is defined by: $V_{INn} + |V_{OUTn}^-| \leq 40V$. The typical application schematic is shown in Figure 48. Though an LTM4655 channel configured to regulate V_{OUTn}^- is a ground-referred buck topology, built-in level-shift circuitry on the RUN*n*, CLKIN*n*, and PGOOD*n* pins result in these pins being conveniently referred to GND (not SV_{OUTn}^-).

Each channel of the LTM4655 contains an independent, integrated constant-frequency current mode regulator, power MOSFETs, power inductor, EMI filter and other supporting discrete components. The nominal switching frequency range is from 400kHz to 3MHz, and the default operating frequency is 400kHz. Each channel can optionally be synchronized to its built-in clock oscillator CLKOUT*n* pins or to an externally applied clock, from 250kHz to 3MHz. See the Applications Information section. Each channel of the LTM4655 supports internal and external control loop compensation. Internal loop compensation is selected by connecting the COMP*n*a and COMP*n*b pins. Using internal loop compensation, the LTM4655 has sufficient stability margins and good transient performance with a wide range of output capacitors—even ceramic-only output capacitors. For external loop compensation, see the Applications Information section. LTpowerCAD® is available for transient load step and stability analysis. Input filter and noise cancellation circuitry reduces noise-coupling to the module's inputs and outputs, ensuring the module's electromagnetic interference (EMI) meets the limits of EN55022 Class B (see Figure 7 through Figure 9).

Pulling the RUN*n* pin below 1.2V (with respect to GND) forces the corresponding LTM4655 channel into a shutdown state. A capacitor can be applied from ISET*n*a to SV_{OUTn}^- to program the output voltage ramp rate; or, the default LTM4655 ramp rate can be set by connecting ISET*n*a to ISET*n*b; or, voltage tracking can be implemented by interfacing rail voltages to the ISET*n*a pin. See the Applications Information section.

Multiphase operation can be employed by connecting the CLKOUT*n* pins to their respective CLKIN*n* pins—or, by connecting an external clock source to the LTM4655's CLKIN*n* pins. See the Typical Applications section.

LDO losses within the module incurred primarily due to MOSFET driver power are optionally reduced by connecting $EXTV_{CCn}$ to V_{OUTn}^+ through an RC filter or by connecting $EXTV_{CCn}$ to a suitable voltage source.

For channels configured for positive-V_{OUT} operation, the IMON*n*a pin is an analog output current indicator that sources a current proportional to its channel's load current. (For channels configured for negative-V_{OUT}^- operation, the

OPERATION

IMON*n*a pin does not support such a feature and must be connected to V_{OUTn}–.) When IMON*n*a is electrically connected to IMON*n*b, the voltage on the IMON*n*a/IMON*n*b node is proportional to load current—with 1V corresponding to 4A load. If desired, IMON*n*a can be interfaced to an external parallel RC network instead of the one provided by IMON*n*b. If IMON*n*a ever exceeds 2V, a servo loop reduces the LTM4655's output current in order to keep IMON*n*a at or below 2V. Through this servo mechanism, a parallel RC network can be connected to IMON*n*a to implement an average current limit function—if desired. When the feature is not needed, connect IMON*n*a to V_{OUTn}–.

The LTM4655 features an additional control pin called VINREG*n*, which has a 2V servo threshold. This pin can be used to as an extra control pin, e.g., to reduce channel input current draw during input line sag ("brownout") conditions. Connect VINREG*n* to $INTV_{CCn}$ when this feature is not needed.

$TEMP^+$ and $TEMP^-$ pins give access to a diode-connected PNP transistor, making it possible to monitor the LTM4655's internal temperature—if desired.

External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 11 and Table 12 and the Test Circuits for recommended external component values.

V_{IN} to V_{OUT} Conversion Ratios

There are restrictions on the V_{IN} to V_{OUT} conversion ratios that the LTM4655 can achieve. The maximum duty cycle of the LTM4655 is 96% typical. The V_{IN} to V_{OUT} minimum dropout voltage is a function of load current when operating in high duty cycle applications. As an example, $V_{OUTn(24VDC)}$ from the Electrical Characteristics table highlights the LTM4655's ability to regulate $24V_{OUT}$ at up to 4A from $29V_{IN}$, when running at a switching frequency, f_{SW}, of 1.5MHz.

At very low duty cycles, the LTM4655's on-time of M_T each switching cycle should be designed to exceed the LTM4655 control loop's specified minimum on-time of 60ns, $t_{ON(MIN)}$, (guardband to 90ns) see Equation 4.

$$\frac{D_n}{f_{SWn}} > T_{ON(MIN)n} \quad (4)$$

where D_n (unitless) is the duty-cycle of M_{Tn}, given by Equation 5:

$$D_n = \frac{V_{OUTn}^+ - V_{OUTn}^-}{V_{INn} - V_{OUTn}^-} \quad (5)$$

In rare cases where the minimum on-time restriction is violated, the channel *n* frequency of the LTM4655 automatically and gradually folds back down to approximately one-fifth of its programmed switching frequency to allow V_{OUT} to remain in regulation. See the Frequency Adjustment section. Be reminded of Notes 2 and 3 in the Electrical Characteristics section regarding output current guidelines.

Input Capacitors, Positive-V_{OUT} Operation

The LTM4655 achieves low input conducted EMI noise due to tight layout and high frequency bypassing of MOSFETs M_{Tn} and M_{Bn} within the module itself. A small filter inductor (400nH) is integrated in the input line (from V_{INn} to V_{Dn}), providing further noise attenuation—again, local to the switching MOSFETs. The V_{Dn} and V_{INn} pins are available for external input capacitors—C_{Dn} and C_{INHn}—to form a high-frequency π filter. As shown in the Simplified Block Diagram, the ceramic capacitor C_{Dn} on the LTM4655's V_{Dn} pins handles the majority of the RMS current into the DC/DC converter power stage and requires careful selection, for that reason.

See Figure 7 through Figure 9 for demonstration of LTM4655's EMI performance, meeting the radiated emissions requirements of EN55022B.

The input capacitance, C_{Dn}, is needed to filter the pulsed current drawn by M_{Tn}. To prevent excessive voltage sag on V_{Dn}, a low-effective series resistance (low-ESR, such as an X7R ceramic) input capacitor should be used, sized appropriately for the maximum C_{Dn} RMS ripple current (Equation 6)

$$I_{CDn(RMS)} = \frac{I_{OUTn(MAX)}}{\eta_n\%} \bullet \sqrt{D_n \bullet (1-D_n)} \quad (6)$$

where η_n% is the estimated efficiency of the channel *n* power module. (See Typical Performance Characteristics graphs.)

OPERATION

Several capacitors may be paralleled to meet the application's target size, height, and C_{Dn} RMS ripple current rating. For lower input voltage applications, sufficient bulk input capacitance is needed to counteract line sag and transient effects during output load changes. The bulk capacitor can be a switcher-rated aluminum electrolytic capacitor or a Polymer capacitor. Suggested values for C_{Dn} and C_{INHn} are found in Table 11.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM4655's V_{INn}, SV_{INn}, and V_{Dn} pins. A ceramic input capacitor combined with trace or cable inductance forms a high Q (underdamped) tank circuit. If the LTM4655 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot Plugging Safely section.

Output Capacitors, Positive-V_{OUT} Operation

Output capacitors C_{OUTHn} and C_{OUTLn} are applied across the LTM4655's V_{OUTn}^+/V_{OUTn}^- power output pins. Sufficient capacitance and low ESR are called for, to meet the output voltage ripple, loop stability, and transient requirements. C_{OUTLn} can be a low ESR tantalum or polymer capacitor. C_{OUTHn} is a ceramic capacitor. The typical output capacitance is 22µF (type X5R material, or better), if ceramic-only output capacitors are used.

Table 11 shows a matrix of suggested output capacitors optimized for 2A transient step-loads applied at 2A/µs. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spike is required. The LTpowerCAD design tool is available for transient and stability analysis. Stability criteria are considered in the Table 11 matrix, and LTpowerCAD is available for stability analysis. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. LTpowerCAD can be used to calculate the output ripple reduction as the number of implemented phases increases by N times.

External loop compensation can be applied from COMPna to SV_{OUTn}^-, if needed, for transient response optimization.

Forced Continuous Operation

Leave the CLKIN*n* pin open circuit to command channel *n* of the LTM4655 for forced continuous operation. In this mode, the control loop is allowed to command the inductor peak current to approximately –1A, allowing for significant negative average current. Clocking the CLKIN*n* pin at a frequency within ±40% of the target switching frequency commanded by the f_{SETn} pin synchronizes M_{Tn}'s turn-on to the rising edge of the CLKIN*n* pin.

Output Voltage Programming, Tracking and Soft-Start

The LTM4655 regulates its output voltage, $V_{OUTn}^+ - V_{OUTn}^-$, according to the differential voltage present from ISET*n*a to SV_{OUTn}^-. In most applications, the output voltage is set by simply connecting a resistor, R_{ISETn}, from ISET*n*a to SV_{OUTn}^-, according to Equation 7.

$$R_{ISETn} = \frac{V_{OUTn}^+ - V_{OUTn}^-}{50\mu A} \quad (7)$$

Since the LTM4655 control loop servos its output voltage according to the voltage between ISET*n*a and SV_{OUTn}^-: placing a capacitor, C_{SSn}, parallel to R_{ISETn} configures the ramp-up rate of ISET*n*a and thus the output. In the time domain, the output voltage ramp-up after the RUN*n* pin is toggled from low to high (t = 0s) is given by Equation 8.

$$V_{OUTn}(t)^+ V_{OUTn}(t)^- = I_{ISETna} \bullet R_{ISETn} \bullet \left(1 - e^{-\frac{t}{R_{ISETn} \bullet C_{SSn}}}\right) \quad (8)$$

The soft-start time, t_{SS}, is defined as the time it takes for channel n's output voltage to ramp from 0V to 90% of its final value (Equation 9 or Equation 10)

$$t_{SSn} = -R_{ISETn} \bullet C_{SSn} \bullet \ln(1-0.9) \quad (9)$$

or

$$t_{SSn} = 2.3 \bullet R_{ISETn} \bullet C_{SSn} \quad (10)$$

OPERATION

A default value of C_{SSn} = 1.5nF can be implemented by connecting ISET*n*a to ISET*n*b. For other ramp-up rates, connect an external C_{SS} capacitor parallel to R_{ISET}.

When starting up into a pre-biased V_{OUT}, the LTM4655 stays in a sleep mode, keeping M_{Tn} and M_{Bn} off until V_{ISETna} equals V_{OSNSn}^+—after which, the DC/DC converter commences switching action and V_{OUT} is ramped according to the voltage commanded by ISET*n*a.

Since the LTM4655 control loop servos its V_{OSNSn}^+ voltage to match that of ISET*n*a's, the LTM4655's channel *n* output can be configured to track any voltage applied to ISET*n*a, referenced to SV_{OUTn}^-. See Figure 52 for an example of the LTM4655 configured as a DAC-controlled bipolar-output programmable power supply.

The LTM4655 can track the mirror-image of a positive rail to generate the negative half of a split-supply, as seen in Figure 50 (note the use of R_{TRACK} and $R_{ISET2} = R_{ISET1} \,||\, R_{TRACK}$).

Frequency Adjustment

The default switching frequency (f_{SWn}) of channel *n* of the LTM4655 is 400kHz. This is suitable for low-V_{IN} ($V_{INn} \leq$ 5V) applications and low-V_{OUT} ($V_{OUTn}^+ - V_{OUTn}^- \leq 3.3V$) applications. For a practical design, the LTM4655's inductor ripple current (ΔI_{nPK-PK}) is suggested to be less than ~$2A_{PK-PK}$. Choose f_{SWn} according to Equation 11.

$$f_{SWn} = \frac{V_{OUTn}^+ - V_{OUTn}^- \bullet (1 - D_n)}{L_n \bullet \Delta I_{nPK-PK}} \quad (11)$$

where the value of LTM4655's power inductor, L_n, is 4µH.

To avoid cycle-skipping, impose restrictions on f_{SWn}, to ensure minimum on-time criteria is met (Equation 12).

$$f_{SWn} < \frac{D_n}{T_{ONn(MIN)}} \quad (12)$$

The LTM4655's minimum on-time, $t_{ONn(MIN)}$, is specified as 60ns. For a practical design, it is recommended to guardband to 90ns.

To configure channel *n* of the LTM4655 for a higher switching frequency than its default of 400kHz, apply a resistor, R_{fSETn}, between the f_{SETn} pin and SV_{OUTn}^+. R_{fSETn} is given (in MΩ) by Equation 13.

$$R_{fSETn}(M\Omega) = \frac{1}{10pF \bullet [f_{SWn}(MHz) - 0.4(MHz)]} \quad (13)$$

The relationship of R_{fSETn} to programmed f_{SWn} is shown in Figure 1. See Table 11 and Table 12 for recommended f_{SWn} and corresponding R_{fSETn} values for various combinations of V_{INn}, V_{OUTn}^+ and V_{OUTn}^-.

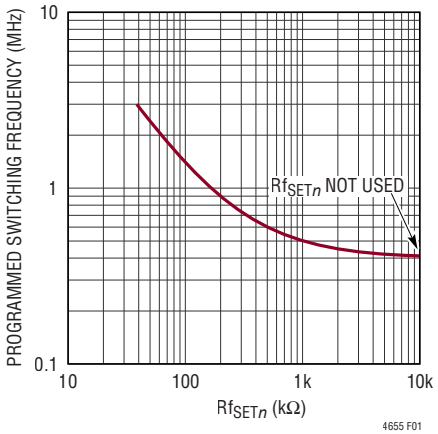


Figure 1. Relationship Between R_{fSETn} and Target f_{SWn}

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Power Module Protection

The LTM4655's current mode control architecture provides fast cycle-by-cycle current limit in an overcurrent condition, as shown in the Typical Performance Characteristics section. If the output voltage collapses sufficiently due to an overload or short-circuit condition, minimum on-time will be violated and the internal oscillator will then fold-back automatically to one-fifth of the LTM4655's programmed switching frequency—thereby reducing the output current and affording the load a chance to recover.

The LTM4655 ceases channel *n* switching action if the channel's internal temperatures exceed 165°C. The channel's control IC resumes operation after a 10°C cool-down hysteresis. Note that these typical parameters are based on measurements in a lab oven and are not production tested. This overtemperature protection is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this overtemperature protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device. See Note 1 of the Electrical Characteristics table.

The LTM4655 does not feature any specialized output overvoltage protection beyond what is inherent to the control loop's servo mechanism.

RUN Pin Enable

The RUN*n* pin is used to enable the power module or sequence the power module. The threshold is 1.2V. The RUN*n* pin can be used to provide an undervoltage lockout (UVLO) function by connecting a resistor divider from the input supply to the RUN*n* pin, as shown in Figure 2. Undervoltage lockout keeps channel *n* of the LTM4655 in shutdown until the supply input voltage is above a certain voltage programmed by the user. The RUN*n* pin hysteresis voltage prevents noise from falsely tripping UVLO. Resistors are chosen by first selecting R_{Bn} (refer to Figure 2 and Equation 14). Then:

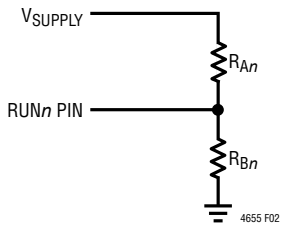

Figure 2. Undervoltage Lockout Resistive Divider

$$R_{An} = R_{Bn} \bullet \left(\frac{V_{INn(ON)}}{1.2V} - 1 \right) \quad (14)$$

where $V_{INn(ON)}$ is the input voltage at which the undervoltage lockout is overcome and the supply turns on. The V_{INn} turn-off voltage, $V_{INn(OFF)}$ is given by Equation 15.

$$V_{INn(OFF)} = 1.07V \bullet \left(\frac{R_{An}}{R_{Bn}} + 1 \right) \quad (15)$$

If UVLO is not needed, RUN*n* can be connected to LTM4655's LDO_{OUT} pin.

When RUN*n* is below its threshold, UVLO of channel *n* is engaged, M_{Tn} and M_{Bn} are turned off, $INTV_{CCn}$ ceases to be regulated, and ISET*n*a is discharged to SV_{OUTn}^- by internal circuitry.

Loop Compensation

External loop compensation may be preferred for some applications and can be implemented easily, as follows: leave COMP*n*b open circuit; connect a series-RC network R_{THn} and C_{THn} from COMP*n*b to SV_{OUTn}^-; in some instances, connect a capacitor (C_{THPn}) from COMP*n*a to SV_{OUTn}^- (paralleling the R_{THn}–C_{THn} series-RC network). See Table 11 and Table 12 for suggested input and output capacitances for a variety of operating conditions. Additionally, the LTpowerCAD design tool is available for transient and stability analysis.

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Hot Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitors (C_{Dn} and C_{INHn}) of the LTM4655. However, these capacitors can cause problems if the LTM4655 is plugged into a live supply (see Analog Devices Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an under damped tank circuit, and the voltage at the V_{INn} pin of the LTM4655 can ring to twice the nominal input voltage, possibly exceeding the LTM4655's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM4655 into an energized supply, the input network should be designed to prevent this overshoot by introducing a damping element into the path of current flow. This is often done by adding an inexpensive electrolytic bulk capacitor (C_{INLn}) across the input terminals of the LTM4655. The selection criteria for C_{INLn} calls for: an ESR high enough to damp the ringing; a capacitance value several times larger than C_{INHn}; a suitable ripple current rating. C_{INLn} does not need to be located physically close to the LTM4655; it should be located close to the application board's input connector, instead.

Input Disconnect/Input Short Considerations

If at any point the input supply is removed with the output voltage still held high through its capacitor, power will be drawn from the output capacitor to power the module, until the output voltage drops below the minimum SV_{INn}/V_{INn} requirements of the module.

However, if the SV_{INn}/V_{INn} pins are grounded while the output is held high, regardless of the RUN*n* state, parasitic body diodes inside the LTM4655 will pull current from the output through the V_{OUTn}^+ pins. Depending on the size of the output capacitor and the resistivity of the short, high currents may flow through the internal body diode, and cause damage to the part. If discharge of SV_{INn}/V_{INn} by the input source is possible, preventative measures should be taken to prevent current flow through the internal body diode. Simple solutions would be placing a Schottky diode in series with the supply (Figure 3), or placing a Schottky diode from V_{OUTn}^+ to SV_{INn}/V_{INn} (Figure 4). Applications with loads that experience large load-step release, load dump or other mechanisms that invoke reverse energy flow in the Figure 3 circuit may need a suitably-rated Zener diode protection clamp, to limit the resulting transient voltage rise on SV_{INn}/V_{INn} and C_{INHn}.

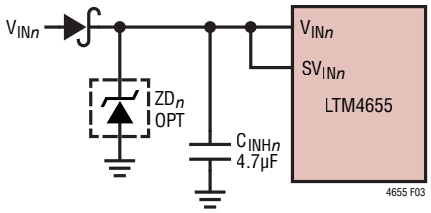

Figure 3. Schottky Diode in Series with the Supply

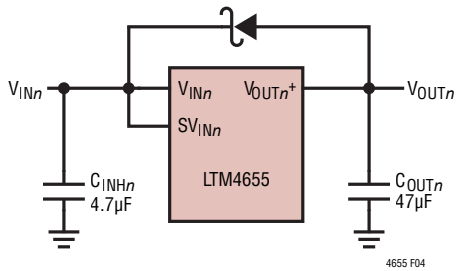

Figure 4. Schottky Diode from V_{OUTn}^+ to V_{INn}

$INTV_{CCn}$ and $EXTV_{CCn}$ Connection

When RUN*n* is logic high, an internal low dropout regulator regulates an internal supply, $INTV_{CCn}$, that powers the control circuitry for driving LTM4655's channel *n* internal MOSFETs. $INTV_{CCn}$ is regulated at 3.3V. In this manner, the LTM4655's $INTV_{CCn}$ is directly powered from SV_{INn}, by default. The gate driver current through the $INTV_{CCn}$ LDO is about 20mA for a typical 1MHz application. The internal LDO power dissipation can be calculated as shown in Equation 16.

$$P_{LDO\_LOSSn(INTVCC)} = 20mA \bullet (SV_{INn}^- - V_{OUTn}^- - 3V) \quad (16)$$

The LDO draws current off of $EXTV_{CCn}$ instead of SV_{INn} when $EXTV_{CCn}$–V_{OUTn}^- exceeds 3.2V and SV_{INn}–SV_{OUTn}^- exceeds 5V. For output voltages of 4V and higher, $EXTV_{CCn}$

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can be connected to V_{OUTn}^+ through an RC-filter. When the internal LDO derives power from $EXTV_{CCn}$ instead of SV_{INn}, the internal LDO power dissipation is shown in Equation 17.

$$P_{LDO\_LOSSn(EXTVCC)} = 20mA \bullet (V_{OUTn}^+ - V_{OUTn}^- - 3V) \quad (17)$$

The recommended value of the resistor between V_{OUTn}^+ and $EXTV_{CCn}$ is roughly $(V_{OUTn}^+ - V_{OUTn}^-) \bullet 4\Omega/V$. This resistor, $R_{EXTVCCn}$, must be rated to continually dissipate $(0.02A)^2 \bullet R_{EXTVCCn}$. The primary purpose of this resistor is to prevent $EXTV_{CCn}$ overstress under a fault condition. For example, when an inductive short-circuit is applied to the module's output, V_{OUT}^+ may be briefly dragged below V_{OUTn}^-—forward biasing the V_{OUTn}^--to-$EXTV_{CCn}$ body diode. This resistor limits the magnitude of current flow in $EXTV_{CCn}$. If the application requires a low resistive path to $EXTV_{CCn}$, apply a protective Schottky diode across $EXTV_{CCn}$ and V_{OUTn}^-; see Figure 52. Bypass $EXTV_{CCn}$ to V_{OUTn}^- with 1µF of X5R (or better) MLCC.

Multiphase Operation

Multiple LTM4655 channels and modules can be paralleled for higher output current applications. For lowest input and output voltage and current ripples, it is advisable to synchronize paralleled LTM4655s to a clock (within ±40% of the target switching frequency set by f_{SETn}.

LTM4655 channels and modules can be paralleled without synchronizing circuits: just be aware that some beat-frequency ripple will be present in the output voltage and reflected input current by virtue of the fact that such modules are not operating at identical, synchronized switching frequencies.

The LTM4655 device is an inherently current mode controlled device, so parallel channels and modules will have good current sharing as shown in Figure 45 and Figure 47.

To parallel LTM4655 channels and/or modules, connect the respective COMP*n*a, ISET*n*a, and V_{OSNSn}^+ pins of each LTM4655 together to share the current evenly. In addition, tie the respective RUN*n* pins of paralleled LTM4655 channels and/or modules together, to ensure proper start-up and shutdown behavior.

Note that for parallel applications, V_{OUT} can be set by a single, common resistor on the ISET*n*a net (see Equation 18).

$$R_{ISETn} = \frac{V_{OUTn}^+ - V_{OUTn}^-}{50\mu A \bullet N} \quad (18)$$

where N is the number of LTM4655 channels in parallel configuration.

Depending on the duty cycle of operation, the output voltage ripple achieved by paralleled, synchronized LTM4655 modules may be considerably smaller than what is yielded by a single-phase solution. Application Note 77 provides a detailed explanation of multiphase operation (relevant to parallel LTM4655 applications) pertaining to noise reduction and output and input ripple current cancellation. Regardless of ripple current cancellation, it remains important for the output capacitance of paralleled LTM4655 applications to be designed for loop stability and transient response. LTpowerCAD is available for such analysis.

Figure 5 illustrates the RMS ripple current reduction as a function of the number of interleaved (paralleled and synchronized) LTM4655 modules—derived from Application Note 77.

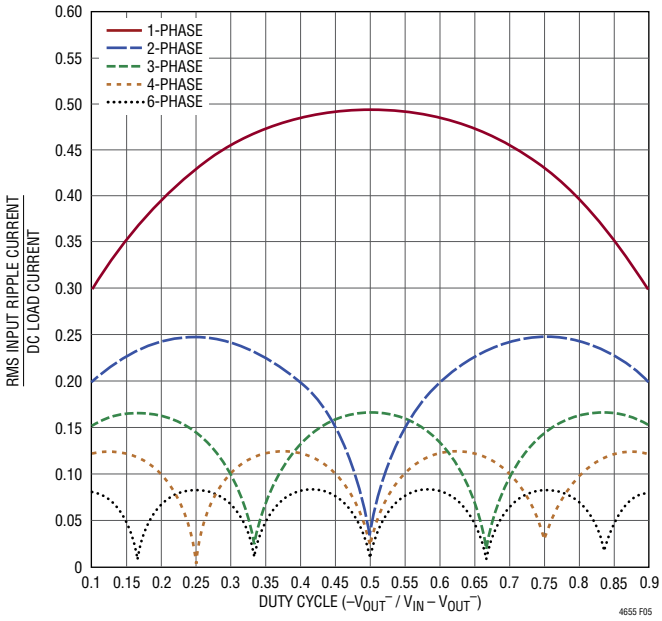

Figure 5. Normalized Input RMS Ripple Current vs Duty Cycle for One to Six LTM4655 Channels (Phases)

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Negative Output Current Capability Varies as a Function of V_{INn} to V_{OUTn}^- Conversion Ratios, Negative-V_{OUT}^- Operation

In negative-V_{OUT} operation, the output current capability of the LTM4655 has a strong dependency on the operating input (V_{INn}) and output (V_{OUTn}^-) voltages. See Figure 6.

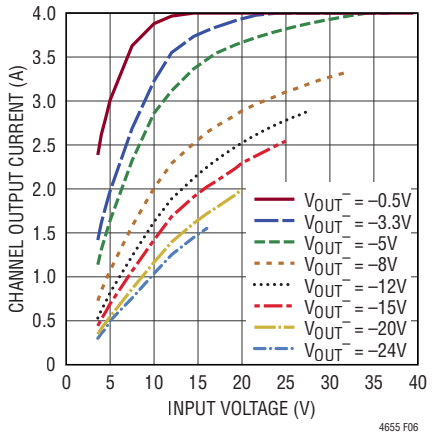

Figure 6. Channel Output Current Capability*, Negative-V_{OUT} Operation

*Current limit frequency-foldback activates at load currents higher than indicated curves. Continuous channel output current capability subject to details of application implementation. Switching frequency set per Table 1. See Notes 2 and 3.

The reason for this is inherent in the two-switch buck-boost topology employed by the LTM4655 when so-configured for negative-V_{OUT} operation. To protect the primary power MOSFET (M_{Tn}) from overstress (see Simplified Block Diagram), its peak current (I_{nPK}) is limited by control circuitry to 6A. When M_{Tn} is on, observe that no current flows to LTM4655's output; furthermore, observe that only when M_{Tn} is off does current flow to the output of the LTM4655. As a consequence of this arrangement: for a given output voltage, current limit inception activates sooner at low line (higher, larger duty cycle) than at high line (lower, smaller duty cycle). A further consequence is: for a given input voltage, the output power capability of the LTM4655 is higher for lower-magnitude V_{OUTn}^- (lower, smaller duty cycle) than for higher-magnitude V_{OUTn}^- (higher, larger duty cycle). The combination of these effects is shown the plots in Figure 6 and described by Equation 19.

$$I_{OUTn(CAPABILITY)} = \frac{V_{INn} \bullet \left(I_{nPK} - \frac{\Delta I_{nPK-PK}}{2} \right) \bullet \eta_n}{V_{INn} - V_{OUTn}^-} \quad (19)$$

where:

ΔI_{nPK-PK} is the channel n inductor ripple current, in amps, and η_n (unitless) is the channel efficiency of the LTM4655.

For completeness, ΔI_{nPK-PK} is given by Equation 20.

$$\Delta I_{nPK-PK} = \frac{1}{L_n \bullet f_{SWn} \bullet \left(\frac{1}{V_{INn}} - \frac{1}{V_{OUTn}^-} \right)} \quad (20)$$

where:

L_n is 4µH, the LTM4655 channel's power inductor value, and f_{SWn} is the switching frequency of the LTM4655's channel, in MHz.

For a practical design, ΔI_{nPK-PK} is designed to be less than ~$2A_{PK-PK}$.

For a practical design, the LTM4655's on-time of M_{Tn} each switching cycle should be designed to exceed the LTM4655 control loop's specified minimum on-time of 60ns, $t_{ON(MIN)}$, (guardband to 90ns). For example, Equation 21.

$$\frac{D_n}{f_{SWn}} > T_{ONn(MIN)} \quad (21)$$

where D_n (unitless) is the duty-cycle of M_{Tn}, given by Equation 22.

$$D = \frac{V_{OUTn}^+ - V_{OUTn}^-}{V_{INn} - V_{OUTn}^-} \quad (22)$$

Combining Equation 22 with Equation 19, it can be illustrative to see Equation 23.

$$I_{OUTn(CAPABILITY)} = (1 - Dn) \bullet \left(I_{nPK} - \frac{\Delta I_{nPK-PK}}{2} \right) \bullet \eta_n \quad (23)$$

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In rare cases where the minimum on-time restriction is violated, the frequency of the affected LTM4655 channel(s) automatically and gradually folds back down to one-fifth of its programmed switching frequency to allow V_{OUTn}^- to remain in regulation.

Be reminded of Notes 2, and 3 in the Electrical Characteristics section regarding output current guidelines.

Input Capacitors, Negative-V_{OUT}^- Operation

The LTM4655 achieves low input conducted EMI noise due to tight layout and high-frequency bypassing of MOSFETs M_{Tn} and M_{Bn} within the module itself. A small filter inductor (400nH) is integrated in the input line (from V_{INn} to V_{Dn}) provides further noise attenuation—again, local to the switching MOSFETs. The V_{Dn} and V_{INn} pins are available for external input capacitors—C_{Dn} and C_{INHn}—to form a high-frequency π filter. As shown in the Simplified Block Diagram, the ceramic capacitor C_{Dn} on the LTM4655's V_{Dn} pins handles the majority of the RMS current into the DC/DC converter power stage and requires careful selection, for that reason.

To meet the radiated emissions requirements of EN55022B, an additional filter capacitor, C_{INOUTn}, is needed—connecting from V_{INn} to V_{OUTn}–. See Figure 7 through Figure 9 for EMI performance.

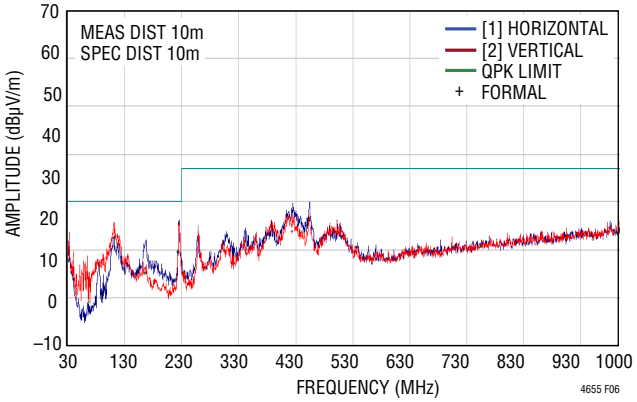

Figure 7. Radiated Emissions Scan of the LTM4655. Producing $24V_{OUT}$ at 7A, from $36V_{IN}$. DC2898A Hardware. f_{SW} = 1.2MHz. Measured in a 10m Chamber. Peak Detect Method

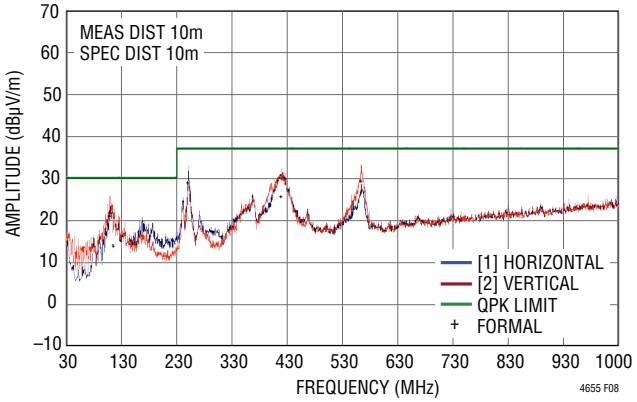

Figure 8. Radiated Emissions Scan of the LTM4655. Producing $-24V_{OUT}$ at 2A, from $12V_{IN}$, DC2899A Hardware. f_{SW} = 1.2MHz. Measured in a 10m Chamber. Peak Detect Method

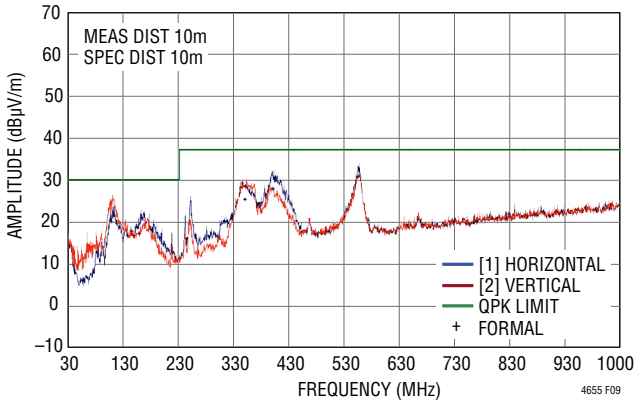

Figure 9. Radiated Emissions Scan of the LTM4655. Producing $-12V_{OUT}$ at 4A, from $12V_{IN}$. DC2899A Hardware. f_{SW} = 700kHz. Measured in a 10m Chamber. Peak Detect Method

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The input capacitance, C_{Dn}, is needed to filter the pulsed current drawn by M_{Tn}. To prevent excessive voltage sag on V_{Dn}, a low-effective series resistance (low-ESR) input capacitor should be used, sized appropriately for the maximum C_{Dn} RMS ripple current (see Equation 24).

$$I_{CDn(RMS)} = I_{nPK} \bullet \sqrt{D_n \bullet (1-D_n)} \quad (24)$$

$I_{CDn(RMS)}$ is maximum for D_n = 1/2. For D_n = 1/2, $I_{CDn(RMS)}$ = 1/2 • I_{nPK} or 3A. This simplification of the worst-case condition is commonly used for design purposes because even significant deviations in D_n do not offer much relief, in practice. Furthermore: note that ripple current ratings from capacitor manufacturers are often based on 2000 hours of life; therefore, it is advisable to significantly over-design C_{Dn}, and/or choose a capacitor rated at a higher temperature than required. Err on the side of caution and contact the capacitor manufacturer to understand the capacitor vendor's derating methodology.

Several capacitors may be paralleled to meet the application's target size, height, and C_{Dn} RMS ripple current rating. For lower input voltage applications, sufficient bulk input capacitance is needed for C_{INLn} to counteract line sag and transient effects during output load changes. Suggested values for C_{Dn} and C_{INHn} are found in Table 12. Take note that C_{Dn} is connected from V_{Dn} to V_{OUTn}–, whereas C_{INHn} and C_{INLn} are connected from V_{INn} to power ground; this is deliberate.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM4655's V_{INn}, SV_{INn}, and V_{Dn} pins. A ceramic input capacitor combined with trace or cable inductance forms a high Q (underdamped) tank circuit. If the LTM4655 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot Plugging Safely section.

Output Capacitors, Negative-V_{OUT}^- Operation

Output capacitors C_{OUTHn} and C_{OUTLn} are applied across the LTM4655's V_{OUTn}^+/V_{OUTn}^- power output pins: sufficient capacitance and low ESR are called for, to meet the output voltage ripple, loop stability, and transient requirements. C_{OUTLn} can be a low ESR tantalum or polymer capacitor. C_{OUTHn} is a ceramic capacitor. The typical output capacitance is 22µF (type X5R material, or better), if ceramic-only output capacitors are used.

For highest reliability designs, polarized output capacitors (C_{OUTLn}) are not recommended, as there is a possibility of a diode-drop of reverse voltage appearing transiently on V_{OUTn}^- during rapid application of input voltage or when RUN*n* is toggled logic high (see Figure 49). When polarized capacitors are used on V_{OUTn}^-, contact the capacitor vendor to understand what reverse voltage their polarized capacitor can withstand. Be advised, polarized capacitor reverse voltage rating is sometimes temperature-dependent.

Output voltage ripple ($\Delta V_{OUTn(PK-PK)}^-$) is governed by charge lost in C_{OUTHn} and C_{OUTLn} while M_{Tn} is on, in addition to the contribution of a resistive drop across the ESR of the output capacitors. This is expressed by Equation 25.

$$\Delta V_{OUTn(PK-PK)} \approx \frac{I_{LOADn} \bullet D}{C_{OUTn} \bullet f_{SWn}} + \frac{I_{LOADn} \bullet ESR_n}{D_n} \quad (25)$$

Table 12 shows a matrix of suggested output capacitors optimized for transient step-loads that are 50% of the full load capability for that combination of V_{INn}, V_{OUTn}^-, and f_{SWn}. The table optimizes total equivalent ESR and total bulk capacitance to yield the stated transient-load performance. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spike is required. The LTpowerCAD design tool is available for transient and stability analysis.

Optional Diodes to Guard Against Overstress, Negative-V_{OUT}^- Operation

Just prior to output voltage start-up, a mechanism exists whereby a diode-drop of reverse polarity can appear on V_{OUTn}^-. See the Simplified Block Diagram and observe: just prior to output voltage start-up, SV_{INn} bias current (I_{SVINn}) flows through the module's control IC, to SV_{OUTn}^-; from there, the bias current (now I_{SVOUTn}^-) flows into V_{OUTn}^- and through M_{Bn}'s body diode, to SW_n. This current (now I_{Ln}) continues to flow—though the 4µH power inductor—to V_{OUTn}^+ and thus ground, closing the control IC bias circuit's path. It is this current through M_{Bn}'s

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body diode that creates a diode-drop of reverse polarity (positive voltage) on V_{OUTn}^-, as shown in Figure 49. The voltage excursion is highest when RUN*n* toggles high because that is the instant when $INTV_{CCn}$ powers-up, with a corresponding increase in $I_{SVINn}/I_{SVOUTn}^-/I_{Ln}$ current flow. With higher current flow, the forward voltage drop (V_F) of M_{Bn}'s body diode—and thus, the positive voltage excursion on V_{OUTn}^- is higher.

If this transient voltage excursion is unwelcome for the load or polarized output capacitors, minimize it with a low V_F Schottky diode that straddles V_{OUTn}^- and V_{OUTn}^+ (see Figure 48 circuit and Figure 49 performance). Additionally, the voltage excursion can be empirically reduced by increasing output capacitance.

Lastly: in applications where it is anticipated that V_{INn} may be rapidly applied (e.g., <10µs) and C_{INOUTn} is used, the resulting capacitor-divider network formed by C_{INOUTn} and $C_{INLn}||C_{INHn}$ may transiently drag V_{OUTn}^- positive. It is recommended to apply a low V_F Schottky diode from V_{OUTn}^- to V_{OUTn}^+ in such applications. The reverse mechanism applies, as well: in applications where it is anticipated that V_{INn} may be rapidly discharged and C_{INOUTn} is used, the resulting capacitor-divider network formed by C_{INOUTn} and $C_{INLn}||C_{INHn}$ may transiently drag V_{OUTn}^- excessively negative. It is recommended to straddle V_{OUTn}^- and V_{OUTn}^+ with a TVS diode, if output voltage excursions during V_{INn}-discharge are anticipated.

Frequency Adjustment, Negative-V_{OUT}^- Operation

The default switching frequency (f_{SWn}) of channel *n* of the LTM4655 is 400kHz. This is suitable for mainly low-V_{IN} or low-V_{OUT}^- applications (V_{INn} < 5V or $|V_{OUTn}^-|$ < 5V). For a practical design, the LTM4655's inductor ripple current (Δ_{nPK-PK}) is suggested to be less than ~$2A_{PK-PK}$. From Equation 20, it follows that f_{SW} should be chosen such that Equation 26).

$$f_{SWn} = \frac{1}{L_n \bullet \Delta I_{nPK\text{-}PK} \bullet \left(\frac{1}{V_{INn}} - \frac{1}{V_{OUTn}^-} \right)} \quad (26)$$

In some cases, the value of f_{SWn} yielded by Equation 26 violates the supported minimum on-time of the LTM4655 (see Equation 21). If this occurs, choose f_{SWn} instead according to Equation 12.

The primary consequence of using a lower switching frequency than that dictated by Equation 26 is that the output current capability of the LTM4655 is reduced, according to Equation 23.

To configure the channel *n* of the LTM4655 for a higher switching frequency than 400kHz default, apply a resistor, R_{fSETn}, between the f_{SETn} pin and SV_{OUTn}^-. R_{fSETn} is given (in MΩ) by Equation 13.

The relationship of R_{fSETn} to programmed f_{SWn} is shown in Figure 1.

See Table 1 and Table 12 for Recommended f_{SWn} and associated R_{fSETn} values for various combinations of V_{INn} and V_{OUTn}^-.

Table 1. Recommended Channel *n* Switching Frequency (f_{SWn}) and R_{fSETn} for Common Combinations of V_{INn} and V_{OUTn}^-, Negative-V_{OUTn}^- Operation

V_{INn} (V) \ V_{OUTn}^- (V)	–0.5	–3.3	–5	–8	–12	–15	–20	–24
3.6	400kHz, No R_{fSETn}	400kHz, No R_{fSETn}	400kHz, No R_{fSETn}	400kHz, No R_{fSETn}	400kHz, No R_{fSETn}	400kHz, No R_{fSETn}	425kHz, 4.3MΩ	450kHz, 2.2MΩ
5				450kHz, 2.2MΩ	475kHz, 1.3MΩ	500kHz, 1MΩ	525kHz, 806kΩ	550kHz, 665kΩ
12			550kHz, 665kΩ	700kHz, 332kΩ	825kHz, 237kΩ	875kHz, 210kΩ	900kHz, 200kΩ	1MHz, 165kΩ
24	Drive $CLKIN_n$ with a 200kHz Clock, No R_{fSETn}	450kHz, 2.2MΩ	600kHz, 499kΩ	800kHz, 249kΩ	1.1MHz, 143kΩ	1.2MHz, 124kΩ	N/A	N/A
36	Not Recommended Due to On-Time Criteria Violation	500kHz, 1MΩ	N/A Due to SOA Criteria Violation					

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Radiated EMI Noise

The generation of radiated EMI noise is an inherent disadvantage of switching regulators. Fast switching turn-on and turn-off of the power MOSFETs—necessary for achieving high efficiency—create high-frequency (~30MHz+) Δ_I/Δ_t changes within DC/DC converters. This activity tends to be the dominant source of high-frequency EMI radiation in such systems. The high level of device integration within LTM4655—including optimized gate-driver and critical front-end π filter inductor—delivers low radiated EMI noise performance. Figure 7 through Figure 9 show typical examples of LTM4655 meeting the radiated emission limits established by EN55022 Class B.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board. The motivation for providing these thermal coefficients is found in JESD51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to predict the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are, in and of themselves, not relevant to providing guidance of thermal performance; instead, the derating curves provided in this data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction-to-ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.
3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.
4. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule regulator and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD51-9.

A graphical representation of the aforementioned thermal resistances is given in Figure 10; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

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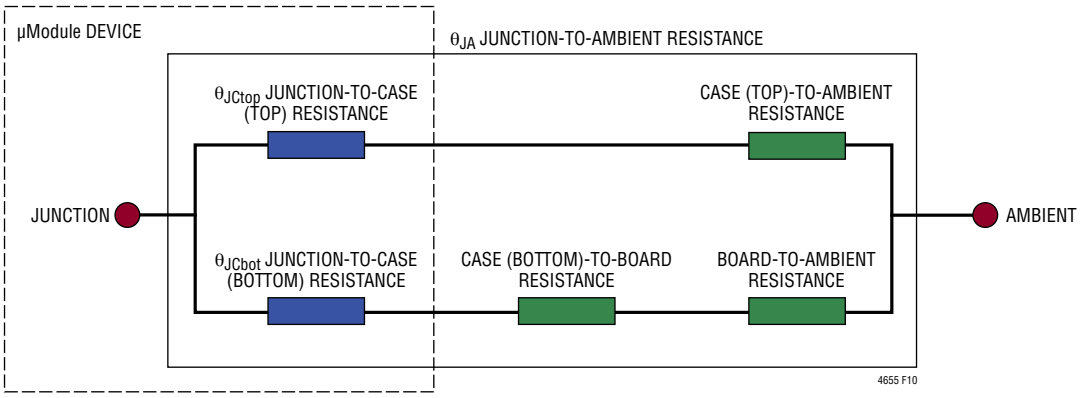

Figure 10. Graphical Representation of JESD51-12 Thermal Coefficients

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4655, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4655 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-9 and JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4655 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled environment chamber while operating the device at the same power loss as that which was simulated. The outcome of this process and due diligence yields the set of derating curves provided in later sections of this data sheet, along with well-correlated JESD51-12-defined θ values provided in the Pin Configuration section.

For positive-V_{OUT} applications, the $12V_{IN}$ and $24V_{IN}$ power loss curves in Figure 11 and Figure 12, respectively, can be used with the load current derating curves in Figure 13 to Figure 24 for calculating an approximate θ_{JA} thermal resistance for the LTM4655 with various heat sinking and air flow conditions. For negative-V_{OUT} applications: use instead the $-5V_{OUT}$, $-12V_{OUT}$ and $-24V_{OUT}$ power loss curves in Figure 25 to Figure 27, respectively, in combination with the load current derating curves in Figure 28 to Figure 43. For split-supply applications, total power loss within the module will dictate the thermal derating; interpolate the relevant derating curves. These thermal resistances represent demonstrated performance of the LTM4655 on DC2898A and DC2899A hardware; 4-layer FR4 PCB measuring 97mm × 116mm × 1.6mm using outer and inner copper weights of 2oz and 1oz,

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respectively. The power loss curves are taken at room temperature, and are increased with multiplicative factors with ambient temperature. These approximate factors are listed in Table 1. (Compute the factor by interpolation, for intermediate temperatures.) The derating curves are plotted with the LTM4655's outputs paralleled and inteleaved, sourcing its maximum output capability, in an environment with temperature-controlled ambient. The output voltages are $1V_{OUT}$, $5V_{OUT}$, $15V_{OUT}$, $–5V_{OUT}$, $–15V_{OUT}$ and $–24V_{OUT}$. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without air flow, and with and without a heat sink attached with thermally conductive adhesive tape. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current decreases the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 30, the load current is derated to 3.05A per channel (6.1A, combined) at 60°C ambient with no airflow and no heat sink and the room temperature (25°C) per channel power loss for this $24V_{IN}$ to $–5V_{OUT}$ at 3.05A out condition is 2.45W; 4.9W, combined. A 5.39W loss is calculated by multiplying the 4.9W room temperature loss from the $24V_{IN}$ to $–5V_{OUT}$ power loss curve at 4.9W (Figure 25), with the 1.1 multiplying factor at 60°C ambient (from Table 2). If the 60°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 60°C divided by 5.39W yields a thermal resistance, θ_{JA}, of 11.1°C/W—in good agreement with Table 6. Table 3 to Table 5 provide equivalent thermal resistances for 1V, 5V, and 15V outputs with and without airflow and heatsinking. Table 6 to Table 8 provide equivalent thermal resistances for –5V, –15V and –24V outputs with and without airflow and heatsinking. The derived thermal resistances in Table 3 to Table 8 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with ambient temperature multiplicative factors from Table 2.

Table 2. Power Loss Multiplicative Factors vs Ambient Temperature

AMBIENT TEMPERATURE	POWER LOSS MULTIPLICATIVE FACTOR
Up to 40°C	1.00
50°C	1.05
60°C	1.10
70°C	1.15
80°C	1.20
90°C	1.25
100°C	1.30
110°C	1.35
120°C	1.40

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Table 3. 1V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 13, Figure 14, Figure 15	5, 12, 24	Figure 11, Figure 12	0	None	11.9
Figure 13, Figure 14, Figure 15	5, 12, 24	Figure 11, Figure 12	200	None	10.9
Figure 13, Figure 14, Figure 15	5, 12, 24	Figure 11, Figure 12	400	None	10.0
Figure 16, Figure 17, Figure 18	5, 12, 24	Figure 11, Figure 12	0	BGA Heat Sink	11.2
Figure 16, Figure 17, Figure 18	5, 12, 24	Figure 11, Figure 12	200	BGA Heat Sink	10.1
Figure 17, Figure 17, Figure 18	5, 12, 24	Figure 11, Figure 12	400	BGA Heat Sink	9.1

Table 4. 5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 19, Figure 20	12, 24	Figure 11, Figure 12	0	None	11.9
Figure 19, Figure 20	12, 24	Figure 11, Figure 12	200	None	10.9
Figure 19, Figure 20	12, 24	Figure 11, Figure 12	400	None	10.0
Figure 21, Figure 22	12, 24	Figure 11, Figure 12	0	BGA Heat Sink	11.2
Figure 21, Figure 22	12, 24	Figure 11, Figure 12	200	BGA Heat Sink	10.1
Figure 21, Figure 22	12, 24	Figure 11, Figure 12	400	BGA Heat Sink	9.1

Table 5. 15V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 23	24	Figure 12	0	None	11.9
Figure 23	24	Figure 12	200	None	10.9
Figure 23	24	Figure 12	400	None	10.0
Figure 24	24	Figure 12	0	BGA Heat Sink	11.2
Figure 24	24	Figure 12	200	BGA Heat Sink	10.1
Figure 24	24	Figure 12	400	BGA Heat Sink	9.1

APPLICATIONS INFORMATION

Table 6. –5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 28, Figure 29, Figure 30	5, 12, 24	Figure 25	0	None	11.9
Figure 28, Figure 29, Figure 30	5, 12, 24	Figure 25	200	None	10.9
Figure 28, Figure 29, Figure 30	5, 12, 24	Figure 25	400	None	10.0
Figure 31, Figure 32, Figure 33	5, 12, 24	Figure 25	0	BGA Heat Sink	11.2
Figure 31, Figure 32, Figure 33	5, 12, 24	Figure 25	200	BGA Heat Sink	10.1
Figure 31, Figure 32, Figure 33	5, 12, 24	Figure 25	400	BGA Heat Sink	9.1

Table 7. –15V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 34, Figure 35, Figure 36	5, 12, 24	Figure 26	0	None	11.9
Figure 34, Figure 35, Figure 36	5, 12, 24	Figure 26	200	None	10.9
Figure 34, Figure 35, Figure 36	5, 12, 24	Figure 26	400	None	10.0
Figure 37, Figure 38, Figure 39	5, 12, 24	Figure 26	0	BGA Heat Sink	11.2
Figure 37, Figure 38, Figure 39	5, 12, 24	Figure 26	200	BGA Heat Sink	10.1
Figure 37, Figure 38, Figure 39	5, 12, 24	Figure 26	400	BGA Heat Sink	9.1

Table 8. –24V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 40, Figure 41	5, 12	Figure 27	0	None	11.9
Figure 40, Figure 41	5, 12	Figure 27	200	None	10.9
Figure 40, Figure 41	5, 12	Figure 27	400	None	10.0
Figure 42, Figure 43	5, 12	Figure 27	0	BGA Heat Sink	11.2
Figure 42, Figure 43	5, 12	Figure 27	200	BGA Heat Sink	10.1
Figure 42, Figure 43	5, 12	Figure 27	400	BGA Heat Sink	9.1

Table 9. Heat Sink Manufacturer (Thermally Conductive Adhesive Tape Pre-Attached)

HEAT SINK MANUFACTURER	PART NUMBER	WEBSITE
Aavid Thermalloy	375424B00034G	www.aavid.com
Cool Innovations	4-050503PT411	www.coolinnovations.com
Wakefield Engineering	LTN20069	www.wakefield.com

Table 10. Thermally Conductive Adhesive Tape Vendor

THERMALLY CONDUCTIVE ADHESIVE TAPE MANUFACTURER	PART NUMBER	WEBSITE
Chomerics	T411	www.chomerics.com

APPLICATIONS INFORMATION

Table 11. Positive Output Voltage Response vs Component Matrix. Performance of a Channel of LTM4655 in Figure 51 Circuit, with Values Here Indicated. Load-Stepping from 2A to 4A Load Current, at 2A/µs. Typical Measured Values

C_{OUTHn} VENDORS	PART NUMBER	C_{OUTHn} VENDORS	PART NUMBER
AVX	12066D107MAT2A (100µF, 6.3V, 1206 Case Size)	AVX	12105D106MAT2A (10µF, 50V, 1210 Case Size)
Murata	GRM31CR60J107M (100µF, 6.3V, 1206 Case Size)	Murata	GRM32ER61H106M (10µF, 50V, 1210 Case Size)
Taiyo Yuden	JMK316BBJ107MLHT (100µF, 6.3V, 1206 Case Size)	Taiyo Yuden	UMK325BJ106M (10µF, 50V, 1210 Case Size)
TDK	C3216X5R0J107M (100µF, 6.3V, 1206 Case Size)	TDK	C3225X5R1H106M (10µF, 50V, 1210 Case Size)
AVX	1210YD476MAT2A (47µF, 16V, 1210 Case Size)	C_{INHn}/C_{Dn} VENDORS	PART NUMBER
Murata	GRM32ER61C476M (47µF, 16V, 1210 Case Size)	Murata	GRM32ER71K475M (4.7µF, 80V, 1210 Case Size)
Taiyo Yuden	EMK325BJ476MM (47µF, 16V, 1210 Case Size)	AVX	12065C475MAT2A (4.7µF, 50V, 1206 Case Size)
AVX	12103D226MAT2A (22µF, 25V, 1210 Case Size)	Murata	GRM31CR71H475M (4.7µF, 50V, 1206 Case Size)
Taiyo Yuden	TMK325BJ226MM (22µF, 25V, 1210 Case Size)	Taiyo Yuden	UMK316AB7475ML (4.7µF, 50V, 1206 Case Size)
TDK	C3225X5R1E226M (22µF, 25V, 1210 Case Size)	TDK	C3216X5R1H475M (4.7µF, 50V, 1206 Case Size)

V_{OUTn} (V)	V_{INn} (V)	C_{INHn}	C_{Dn}	C_{OUTHn}	R_{THn} (Ω)	C_{THn} (nF)	R_{ISETn} (kΩ)	R_{PGDFBn} (kΩ)	f_{SWn} (kHz)	R_{ISETn} (kΩ)	$R_{EXTVCCn}$ (Ω)	LOAD STEP TRANSIENT DROOP (mV)	LOAD STEP PK-PK DEVIATION (mV)	RECOVERY TIME (µs)
1	5	4.7µF	4.7µF	100µF x 3	681	6.8	20	3.32	400	N/A	N/A	70	145	55
1	12	4.7µF	4.7µF	100µF x 3	681	6.8	20	3.32	400	N/A	N/A	70	145	50
1	24	4.7µF	4.7µF	100µF x 3	681	6.8	20	3.32	400	N/A	N/A	70	145	50
1.2	5	4.7µF	4.7µF	100µF x 3	665	6.8	24	4.99	400	N/A	N/A	70	145	50
1.2	12	4.7µF	4.7µF	100µF x 3	665	6.8	24	4.99	400	N/A	N/A	70	145	50
1.2	24	4.7µF	4.7µF	100µF x 3	665	6.8	24	4.99	400	N/A	N/A	70	145	50
1.5	5	4.7µF	4.7µF	100µF x 3	665	6.8	30.1	7.5	400	N/A	N/A	70	145	50
1.5	12	4.7µF	4.7µF	100µF x 3	665	6.8	30.1	7.5	400	N/A	N/A	70	145	50
1.5	24	4.7µF	4.7µF	100µF x 3	665	6.8	30.1	7.5	400	N/A	N/A	70	145	50
1.5	36	4.7µF	4.7µF	100µF x 3	665	6.8	30.1	7.5	400	N/A	N/A	70	145	50
1.8	5	4.7µF	4.7µF	100µF x 3	665	8.2	36	10	400	N/A	N/A	70	145	50
1.8	12	4.7µF	4.7µF	100µF x 3	665	8.2	36	10	400	N/A	N/A	70	145	50
1.8	24	4.7µF	4.7µF	100µF x 3	665	8.2	36	10	400	N/A	N/A	70	145	50
1.8	36	4.7µF	4.7µF	100µF x 3	665	8.2	36	10	400	N/A	N/A	70	145	50
2.5	5	4.7µF	4.7µF	100µF x 3	649	8.2	50	15.8	400	N/A	N/A	70	145	50
2.5	12	4.7µF	4.7µF	100µF x 3	649	8.2	50	15.8	400	N/A	N/A	70	145	50
2.5	24	4.7µF	4.7µF	100µF x 3	649	8.2	50	15.8	400	N/A	N/A	70	145	50
2.5	36	4.7µF	4.7µF	100µF x 3	649	8.2	50	15.8	400	N/A	N/A	70	145	50
3.3	5	4.7µF	4.7µF	100µF x 2	604	10	66.5	22.6	400	N/A	N/A	90	190	50
3.3	12	4.7µF	4.7µF	100µF x 2	604	10	66.5	22.6	400	N/A	N/A	90	190	50
3.3	24	4.7µF	4.7µF	100µF x 2	604	10	66.5	22.6	400	N/A	N/A	90	185	50
3.3	36	4.7µF	4.7µF	100µF x 2	604	10	66.5	22.6	400	N/A	N/A	90	180	50
5	12	4.7µF	4.7µF	47µF x 2	499	10	100	36.5	400	N/A	20	130	260	45
5	24	4.7µF	4.7µF	47µF x 2	499	10	100	36.5	550	665	20	130	260	45
5	36	4.7µF	4.7µF	47µF x 2	499	10	100	36.5	575	576	20	130	260	45
12	15	4.7µF	4.7µF	22µF x 2	499	10	240	95.3	500	1000	49.9	170	350	40
12	24	4.7µF	4.7µF	22µF x 2	499	10	240	95.3	800	249	49.9	170	350	40
12	36	4.7µF	4.7µF	22µF x 2	499	10	240	95.3	1100	143	49.9	170	350	40
15	24	4.7µF	4.7µF	22µF x 2	499	10	301	121	750	287	60.4	170	350	40
15	36	4.7µF	4.7µF	22µF x 2	499	10	301	121	1200	124	60.4	170	350	40
24	36	4.7µF	4.7µF	10µF x 2	499	10	481	196	1200	124	100	220	430	35

APPLICATIONS INFORMATION

Table 12. Negative Output Voltage Response vs Component Matrix. Performance of Figure 48 Circuit with Values Here Indicated. Load-Stepping from 50% of Full Scale (F.S.) to 100% of F.S. Load Current, in 1µs. Typical Measured Values.

C_{OUTHn} VENDORS	PART NUMBER	C_{INHn}/C_{Dn} VENDORS	PART NUMBER
AVX	12066D107MAT2A (100µF, 6.3V, 1206 Case Size)	Murata	GRM32ER71K475M (4.7µF, 80V, 1210 Case Size)
Murata	GRM31CR60J107M (100µF, 6.3V, 1206 Case Size)	AVX	12065C475MAT2A (4.7µF, 50V, 1206 Case Size)
Taiyo Yuden	JMK316BBJ107MLHT (100µF, 6.3V, 1206 Case Size)	Murata	GRM31CR71H475M (4.7µF, 50V, 1206 Case Size)
TDK	C3216X5R0J107M (100µF, 6.3V, 1206 Case Size)	Taiyo Yuden	UMK316AB7475ML (4.7µF, 50V, 1206 Case Size)
AVX	1210YD476MAT2A (47µF, 16V, 1210 Case Size)	TDK	C3216X5R1H475M (4.7µF, 50V, 1206 Case Size)
Murata	GRM32ER61C476M (47µF, 16V, 1210 Case Size)		
Taiyo Yuden	EMK325BJ476MM (47µF, 16V, 1210 Case Size)		
AVX	12103D226MAT2A (22µF, 25V, 1210 Case Size)		
Taiyo Yuden	TMK325BJ226MM (22µF, 25V, 1210 Case Size)		
TDK	C3225X5R1E226M (22µF, 25V, 1210 Case Size)		
AVX	12105D106MAT2A (10µF, 50V, 1210 Case Size)		
Murata	GRM32ER61H106M (10µF, 50V, 1210 Case Size)		
Taiyo Yuden	UMK325BJ106M (10µF, 50V, 1210 Case Size)		
TDK	C3225X5R1H106M (10µF, 50V, 1210 Case Size)		

V_{OUTn}^- (V)	V_{INn} (V)	F.S. LOAD (A)	C_{INHn} (V_{INn}^- TO GND BYPASS CAP)	C_{INOUTn} (V_{INn}^- TO V_{OUTn}^- BYPASS CAP)	C_{Dn} (V_{Dn}^- TO V_{OUTn}^- BYPASS CAP)	$CDGND_n$ (V_{Dn}^- TO GND BYPASS CAP)	C_{OUTHn} (CERAMIC OUTPUT CAP)	R_{ISETn} (kΩ)	R_{PGDFBn} (kΩ)	f_{SWn} (kHz)	R_{fSETn} (kΩ)	$R_{EXTVCCn}$ (Ω)	LOAD STEP TRANSIENT DROOP (mV)	LOAD STEP PK-PK DEVIATION (mV)	RECOVERY TIME (µs)
–0.5	5	3.2	4.7µF	4.7µF	4.7µF	4.7µF	100µF × 4	10	N/A	400	N/A	2.2	75	150	55
–0.5	12	4	4.7µF	4.7µF	4.7µF	4.7µF	100µF × 4	10	N/A	400	N/A	2.2	90	190	60
–0.5*	24	4	4.7µF	4.7µF	4.7µF	4.7µF	100µF × 4	10	N/A	200**	N/A	2.2	90	190	60
–3.3	5	2.2	4.7µF	4.7µF	4.7µF	4.7µF	100µF	66.5	22.6	400	N/A	15	65	130	25
–3.3	12	3.5	4.7µF	4.7µF	4.7µF	4.7µF	100µF × 2	66.5	22.6	400	N/A	15	165	330	50
–3.3	24	4	4.7µF	4.7µF	4.7µF	4.7µF	100µF × 2	66.5	22.6	450	2200	15	175	355	50
–3.3	36	4	4.7µF	4.7µF	4.7µF	4.7µF	100µF × 2	66.5	22.6	500	1000	15	160	310	40
–5	5	1.75	4.7µF	4.7µF	4.7µF	4.7µF	47µF × 2	100	36.5	400	N/A	20	125	235	45
–5	12	3.2	4.7µF	4.7µF	4.7µF	4.7µF	47µF × 2	100	36.5	550	665	20	175	340	60
–5	24	3.85	4.7µF	4.7µF	4.7µF	4.7µF	47µF × 2	100	36.5	600	499	20	185	380	55
–8	5	1.2	4.7µF	4.7µF	4.7µF	4.7µF	47µF	160	61.9	450	2200	32.4	125	235	30
–8	12	2.3	4.7µF	4.7µF	4.7µF	4.7µF	47µF	160	61.9	700	332	32.4	185	340	30
–8	24	3.1	4.7µF	4.7µF	4.7µF	4.7µF	47µF	160	61.9	800	249	32.4	180	330	27
–12	5	0.9	4.7µF	4.7µF	4.7µF	4.7µF	22µF	240	95.3	475	1300	49.9	140	270	32
–12	12	1.9	4.7µF	4.7µF	4.7µF	4.7µF	22µF	240	95.3	825	237	49.9	157	290	25
–12	24	2.75	4.7µF	4.7µF	4.7µF	4.7µF	22µF	240	95.3	1100	143	49.9	170	325	25
–15	5	0.75	4.7µF	4.7µF	4.7µF	4.7µF	22µF	301	121	500	1000	60.4	90	170	25
–15	12	1.75	4.7µF	4.7µF	4.7µF	4.7µF	22µF	301	121	875	210	60.4	200	380	32
–15	24	2.5	4.7µF	4.7µF	4.7µF	4.7µF	22µF	301	121	1200	124	60.4	205	400	28
–24	5	0.55	4.7µF	4.7µF	4.7µF × 2	4.7µF × 2	10µF × 2	481	196	550	665	100	105	220	45
–24	12	1.25	4.7µF	4.7µF	4.7µF × 2	4.7µF × 2	10µF × 2	481	196	1000	165	100	140	275	30

*Internal loop compensation is used with Table 12 settings. COMP*n*a connects to COMP*n*b in Figure 48.

**To avoid violating minimum on-time criteria, drive CLKIN with a 200kHz, 50% duty cycle clock.

APPLICATIONS INFORMATION—DERATING CURVES

Settings per Table 11 and Table 12.

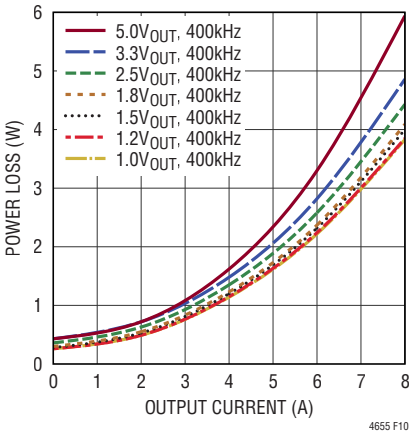


Figure 11. $12V_{IN}$ Power Loss Curve

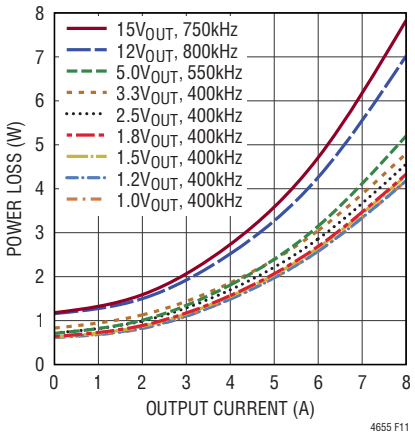


Figure 12. $24V_{IN}$ Power Loss Curve

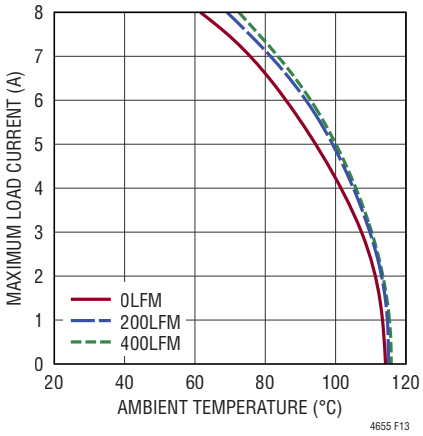


Figure 13. 5V to $1V_{OUT}$ Derating Curve, No Heat Sink

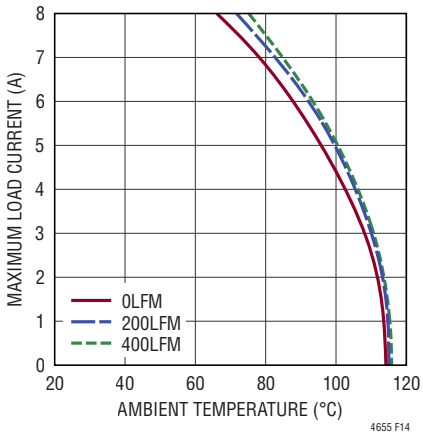


Figure 14. 12V to $1V_{OUT}$ Derating Curve, No Heat Sink

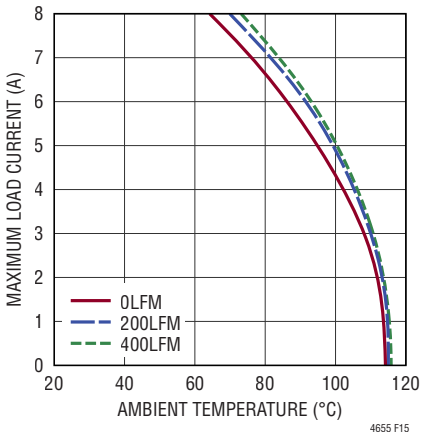


Figure 15. 24V to $1V_{OUT}$ Derating Curve, No Heat Sink

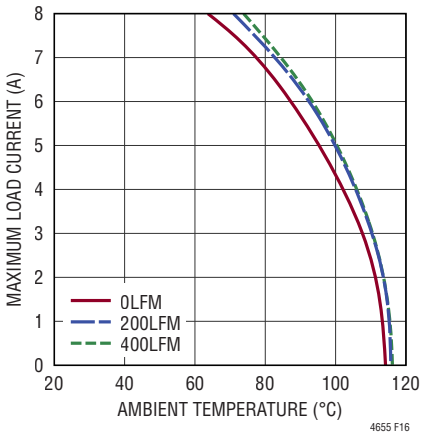


Figure 16. 5V to $1V_{OUT}$ Derating Curve, with BGA Heat Sink

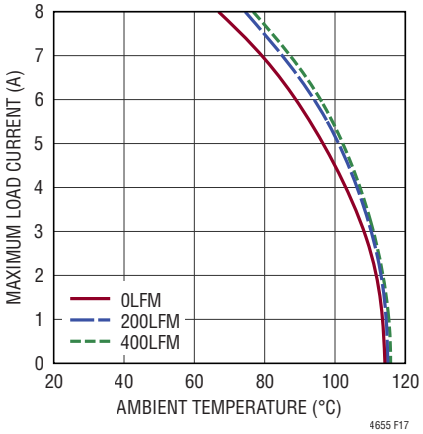


Figure 17. 12V to $1V_{OUT}$ Derating Curve, with BGA Heat Sink

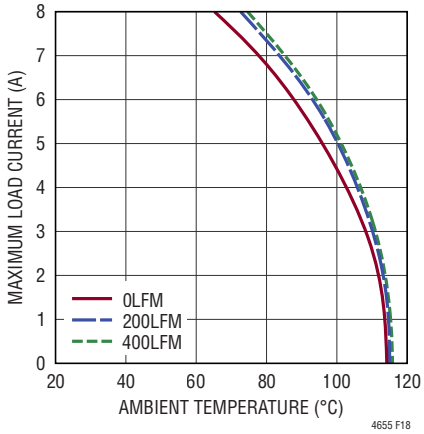


Figure 18. 24V to $1V_{OUT}$ Derating Curve, with BGA Heat Sink

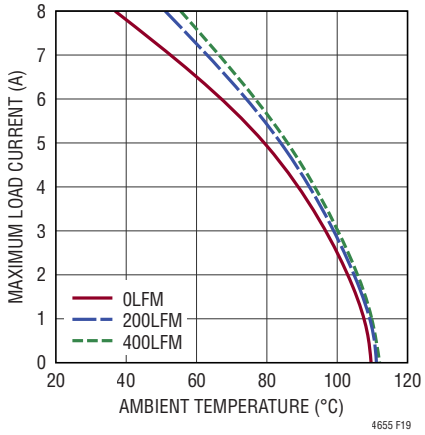


Figure 19. 12V to $5V_{OUT}$ Derating Curve, No Heat Sink

APPLICATIONS INFORMATION—DERATING CURVES

Settings per Table 11 and Table 12.

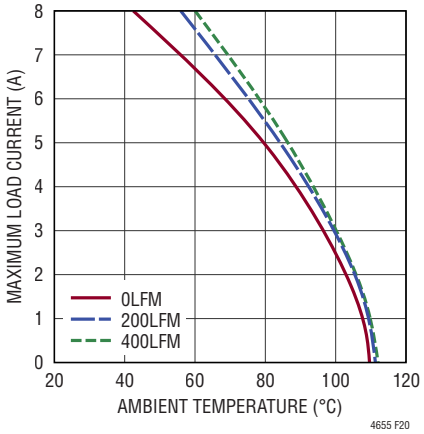


Figure 20. 24V to $5V_{OUT}$ Derating Curve, No Heat Sink

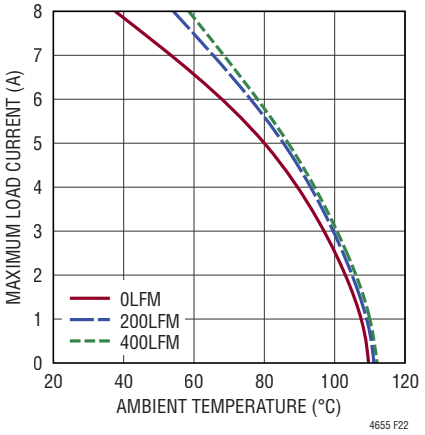


Figure 21. 12V to $5V_{OUT}$ Derating Curve, with BGA Heat Sink

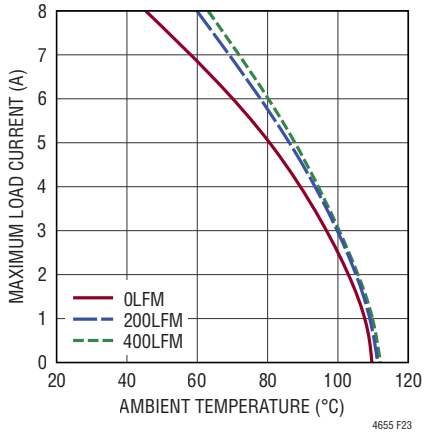


Figure 22. 24V to $5V_{OUT}$ Derating Curve, with BGA Heat Sink

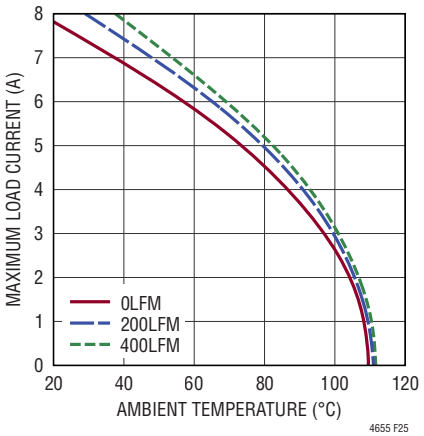


Figure 23. 24V to $15V_{OUT}$ Derating Curve, No Heat Sink

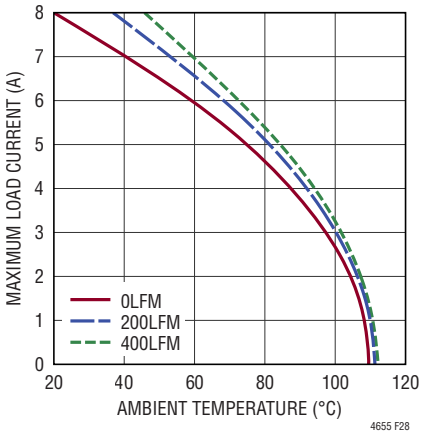


Figure 24. 24V to $15V_{OUT}$ Derating Curve, with BGA Heat Sink

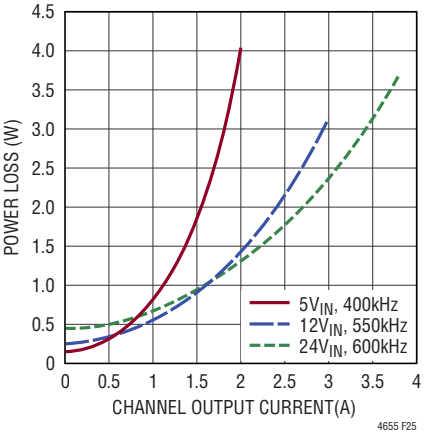


Figure 25. $-5V_{OUT}$ Power Loss Curve

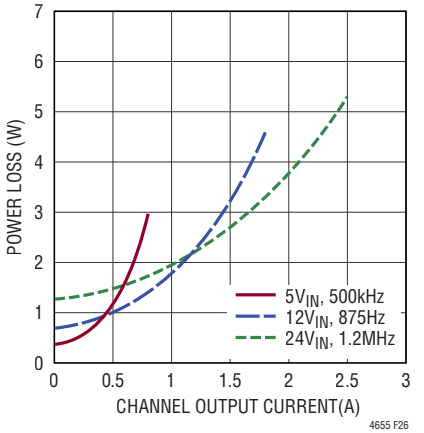


Figure 26. $-15V_{OUT}$ Power Loss Curve

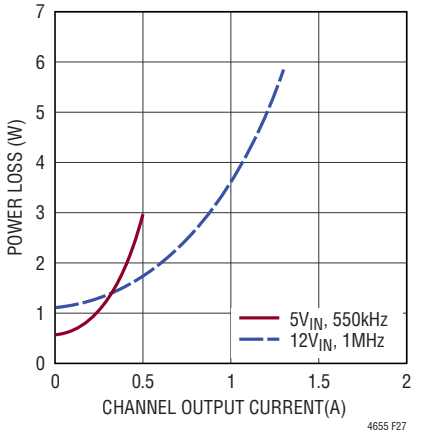


Figure 27. $-24V_{OUT}$ Power Loss Curve

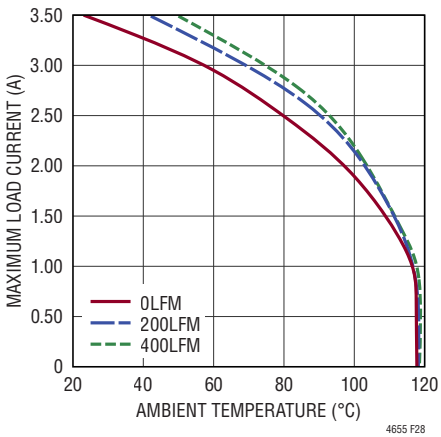


Figure 28. 5V to $-5V_{OUT}$ Derating Curve, No Heat Sink

APPLICATIONS INFORMATION—DERATING CURVES

Settings per Table 11 and Table 12.

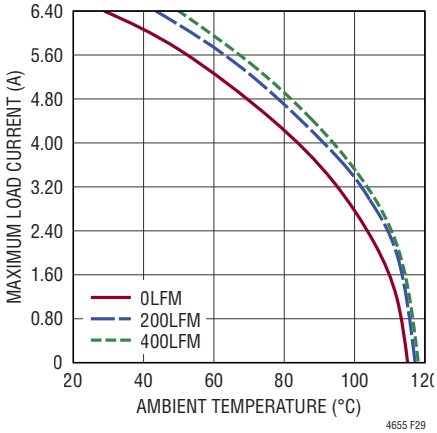


Figure 29. 12V to –5V$_{OUT}$ Derating Curve, No Heat Sink

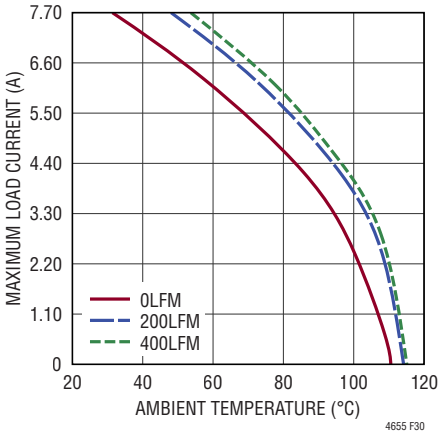


Figure 30. 24V to –5V$_{OUT}$ Derating Curve, No Heat Sink

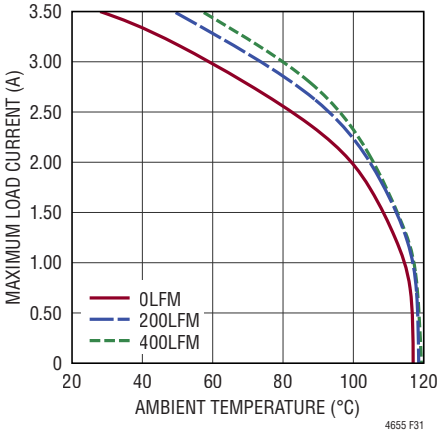


Figure 31. 5V to –5V$_{OUT}$ Derating Curve, with BGA Heat Sink

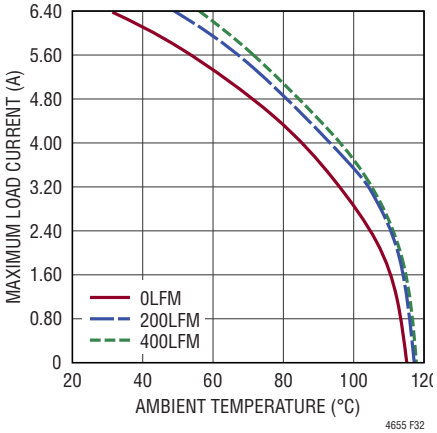


Figure 32. 12V to –5V$_{OUT}$ Derating Curve, with BGA Heat Sink

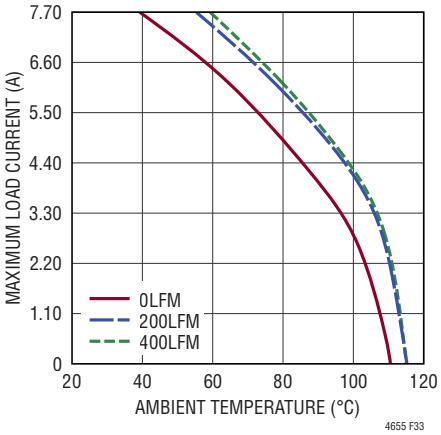


Figure 33. 24V to –5V$_{OUT}$ Derating Curve, with BGA Heat Sink

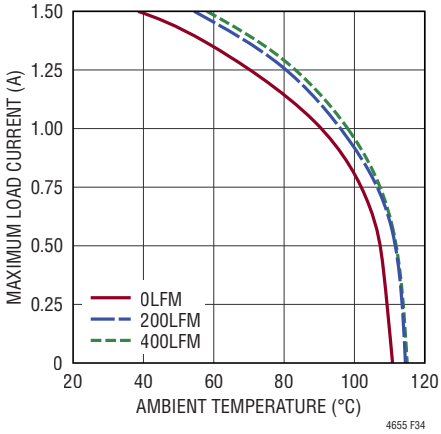


Figure 34. 5V to –15V$_{OUT}$ Derating Curve, No Heat Sink

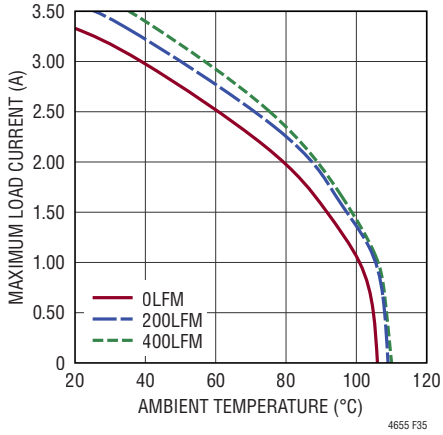


Figure 35. 12V to –15V$_{OUT}$ Derating Curve, No Heat Sink

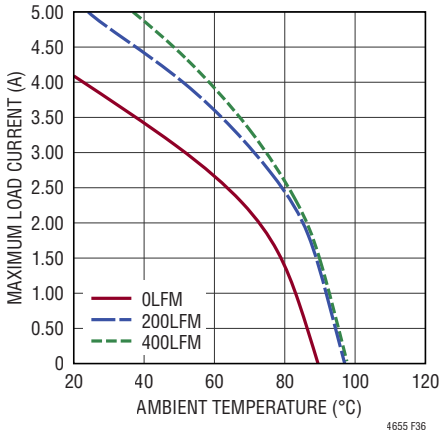


Figure 36. 24V to –15V$_{OUT}$ Derating Curve, No Heat Sink

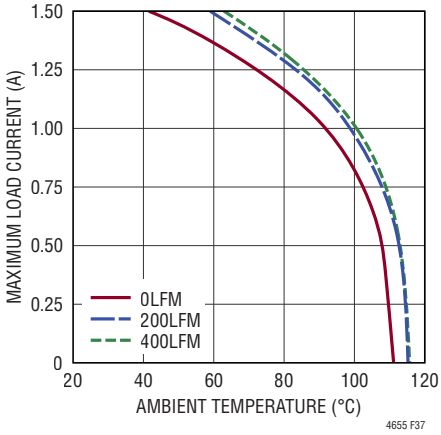


Figure 37. 5V to –15V$_{OUT}$ Derating Curve, with BGA Heat Sink

APPLICATIONS INFORMATION—DERATING CURVES

Settings per Table 11 and Table 12.

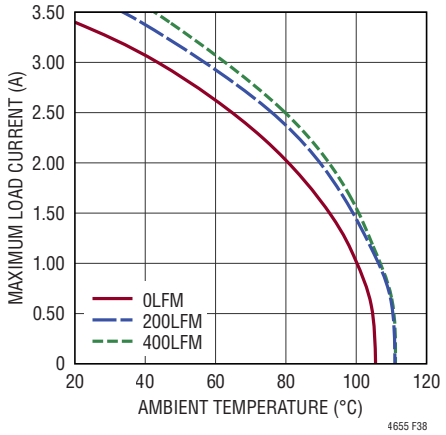


Figure 38. 12V to –15V_{OUT} Derating Curve, with BGA Heat Sink

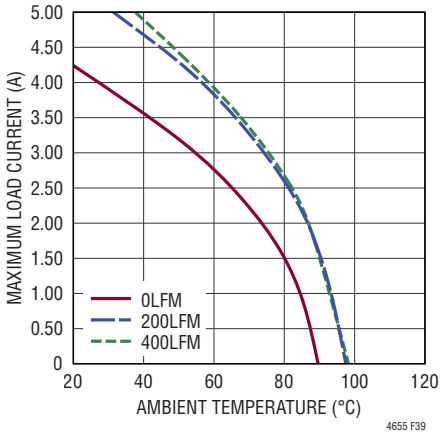


Figure 39. 24V to –15V_{OUT} Derating Curve, with BGA Heat Sink

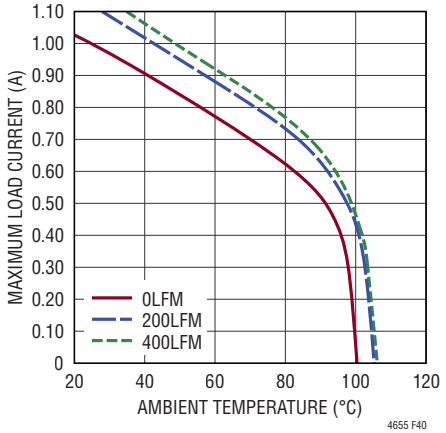


Figure 40. 5V to –24V_{OUT} Derating Curve, No Heat Sink

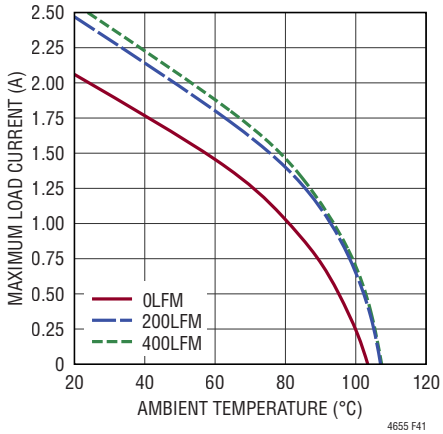


Figure 41. 12V to –24V_{OUT} Derating Curve, No Heat Sink

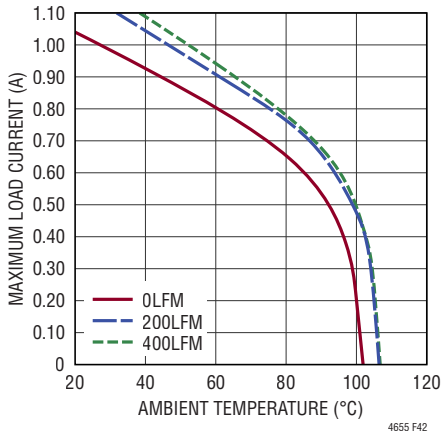


Figure 42. 5V to –24V_{OUT} Derating Curve, with BGA Heat Sink

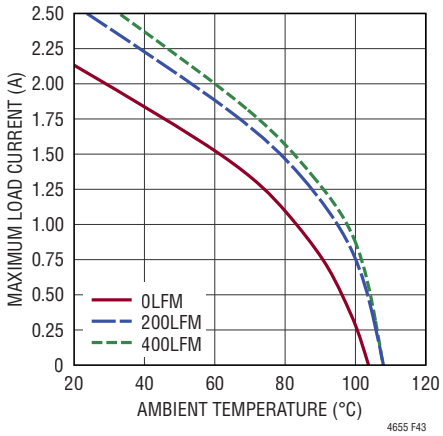


Figure 43. 12V to –24V_{OUT} Derating Curve, with BGA Heat Sink

APPLICATIONS INFORMATION

Safety Considerations

The LTM4655 does not provide galvanic isolation from V_{INn} to V_{OUTn}^+/V_{OUTn}^-. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect the unit from catastrophic failure.

The fuse or circuit breaker, if used, should be selected to limit the current to the regulator in case of a M_{Tn} MOSFET fault. If M_{Tn} fails, the system's input supply will source very large currents to V_{OUTn}^+ through M_{Tn}. This can cause excessive heat and board damage depending on how much power the input voltage can deliver to this system. A fuse or circuit breaker can be used as a secondary fault protector in this situation. Each channel of the LTM4655 features its own, independent overcurrent and overtemperature protection.

Layout Checklist/Example

The high integration of LTM4655 makes the PCB board layout straightforward. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{INn}, V_{OUTn}^+ and V_{OUTn}^-. Doing so helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output (and, if used, input-to-output) capacitors next to the V_{INn}, V_{Dn}, V_{OUTn}^+/V_{OUTn}^- pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the LTM4655.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on pads, unless they are capped or plated over.
- For each channel, use a separate S_{VOUTn}^- copper plane for components connected to signal pins. Connect SV_{OUTn}^- to V_{OUTn}^- directly under the module.
- For parallel applications, connect the respective V_{OUTn}^+, V_{OUTn}^-, V_{OSNSn}^+, RUN*n*, ISET*n*a, COMP*n*a, PGOOD*n* and IMON*n*a pins, accordingly (see Figure 45).
- Bring out test points on the signal pins for monitoring.

Figure 44 gives a good example of the recommended LTM4655 layout.

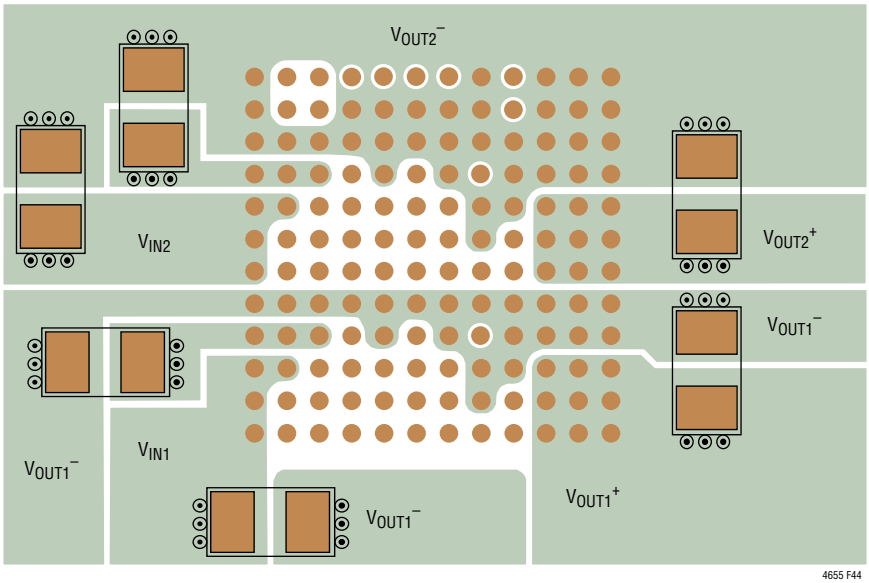
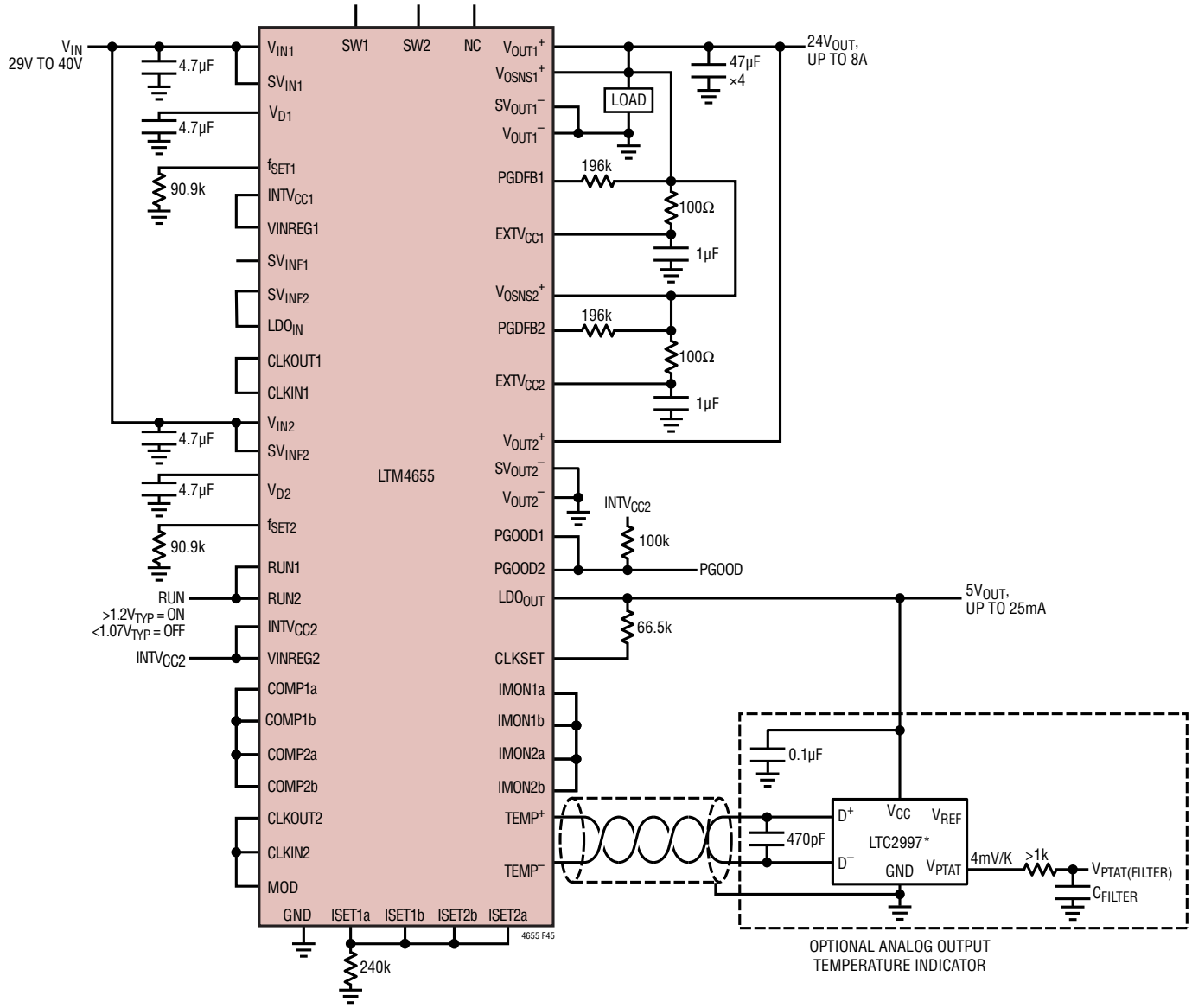


Figure 44. Recommended PCB Layout, Package Top View

TYPICAL APPLICATIONS



* PLACE 470pF DIRECTLY ACROSS THE LTC2997'S D^+/D^- PINS.
ROUTE $TEMP^+/TEMP^-$ DIFFERENTIALLY TO D^+/D^- AND PROTECT FROM NOISE WITH GROUND SHIELDING.
TERMINATE (CONNECT) THE D^+/D^- GROUND SHIELD AT THE LTC2997 GND PIN, ONLY.
FOR BEST V_{PTAT} PERFORMANCE, THE V_{CC} PIN OF THE LTC2997 MUST BE LOCALLY BYPASSED AND QUIET.
SEE LTC2997 DATA SHEET AND APRIL 2017 LT JOURNAL TECHNICAL ARTICLES.

Figure 45. Single 8A, 24V Output DC/DC µModule Regulator with Optional Analog Temperature Indicator

TYPICAL APPLICATIONS

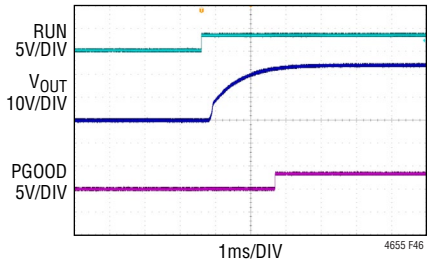


Figure 46. Start-Up Waveforms at $36V_{IN}$, Figure 45 Circuit

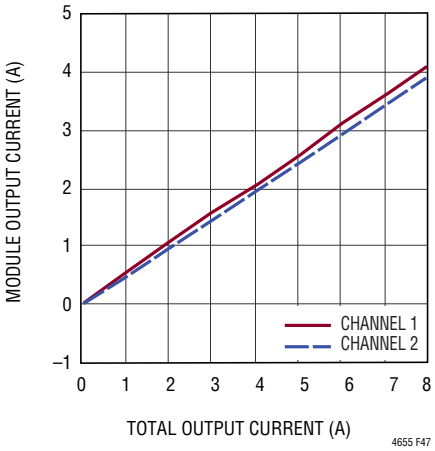
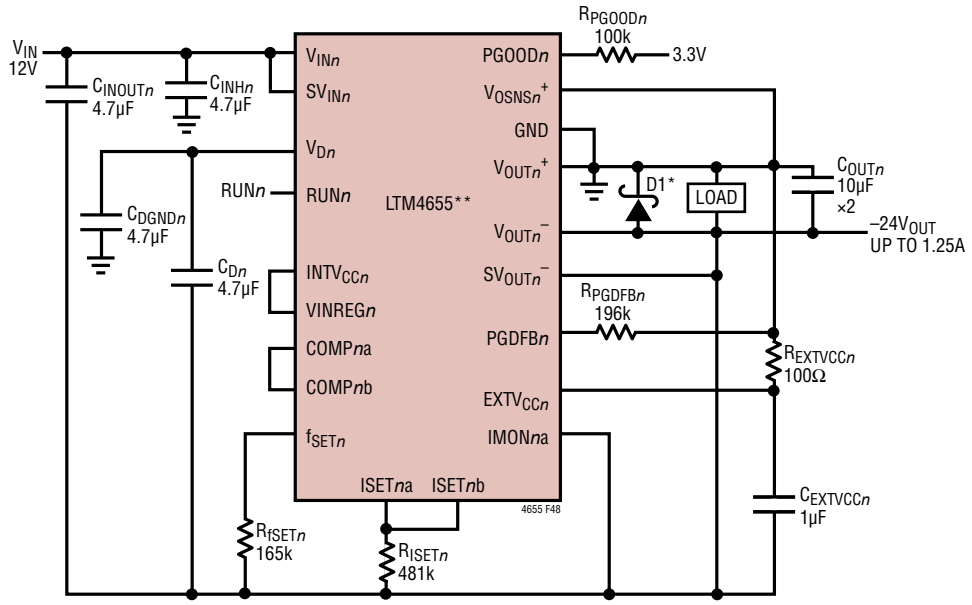


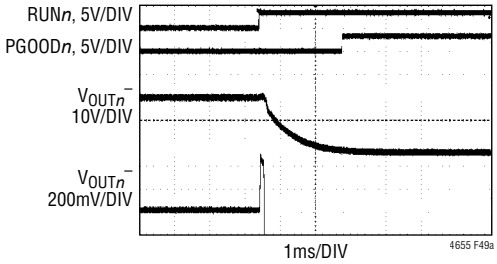
Figure 47. Current Sharing Performance of LTM4655 Channels in Figure 45 Circuit

TYPICAL APPLICATIONS

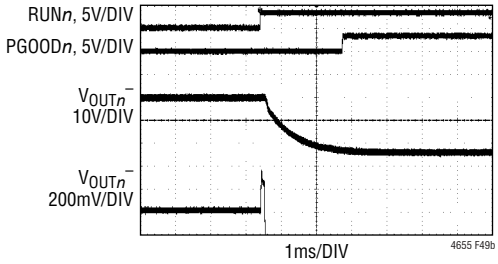


*D1 OPTIONAL (SEE EFFECT IN FIGURE 49): CENTRAL SEMICONDUCTOR P/N CMMSH1-40L
**ONE CHANNEL SHOWN. PINS NOT USED AND NOT SHOWN IN THIS CIRCUIT: NC, SV_{INFn}, IMON*n*b, LDO_{IN}, LDO_{OUT}, CLKSET, MOD, CLKOUT*n*, CLKIN*n*, $TEMP^+$, $TEMP^-$

Figure 48. 1.25A, –24V Output DC/DC µModule Regulator



(a) Start-up Performance with D1 Not Installed. V_{OUTn}^- Reverse-Polarity at Start-Up Transiently Reaches 500mV



(b) Start-up Performance with D1 Installed. V_{OUTn}^- Reverse-Polarity at Start-Up is Transiently Limited to 360mV

Figure 49. Start-Up Waveforms at $12V_{IN}$, Figure 48 Circuit

TYPICAL APPLICATIONS

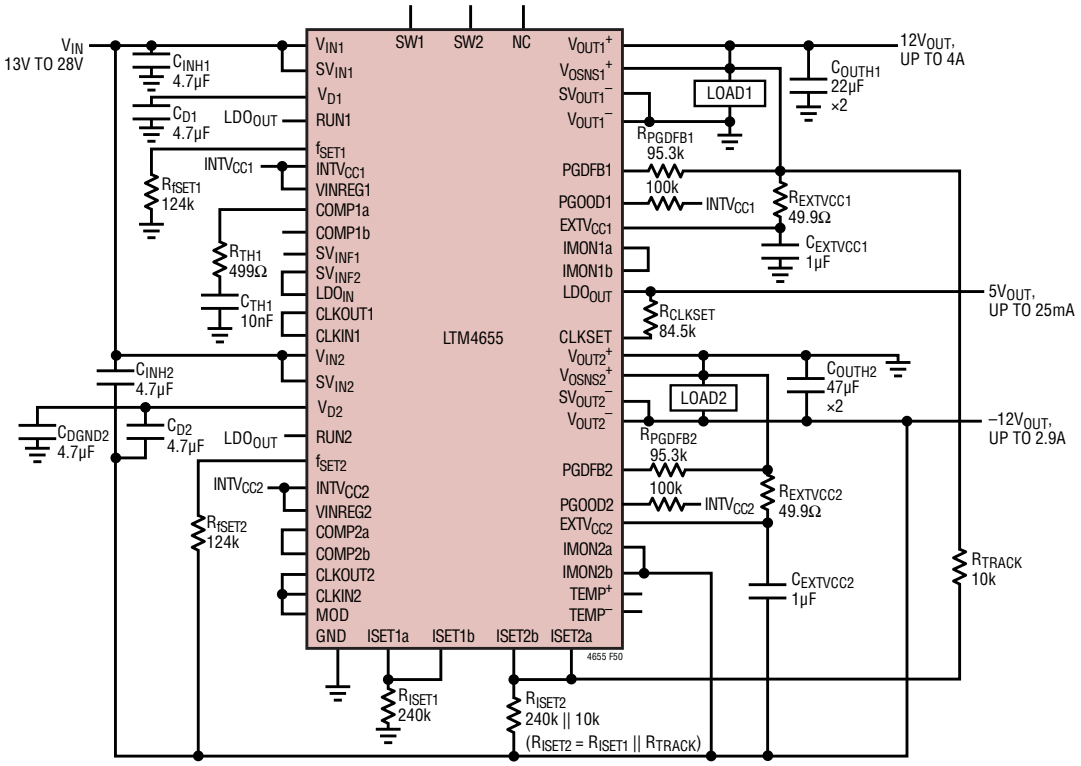


Figure 50. Concurrent ±12V Output DC/DC µModule Regulator

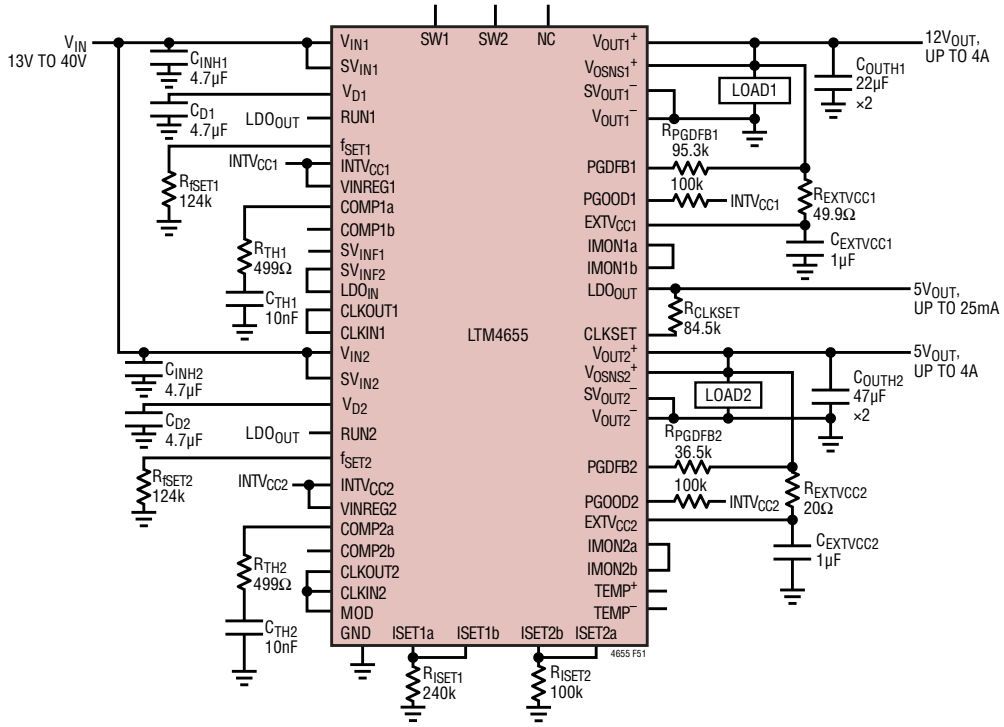
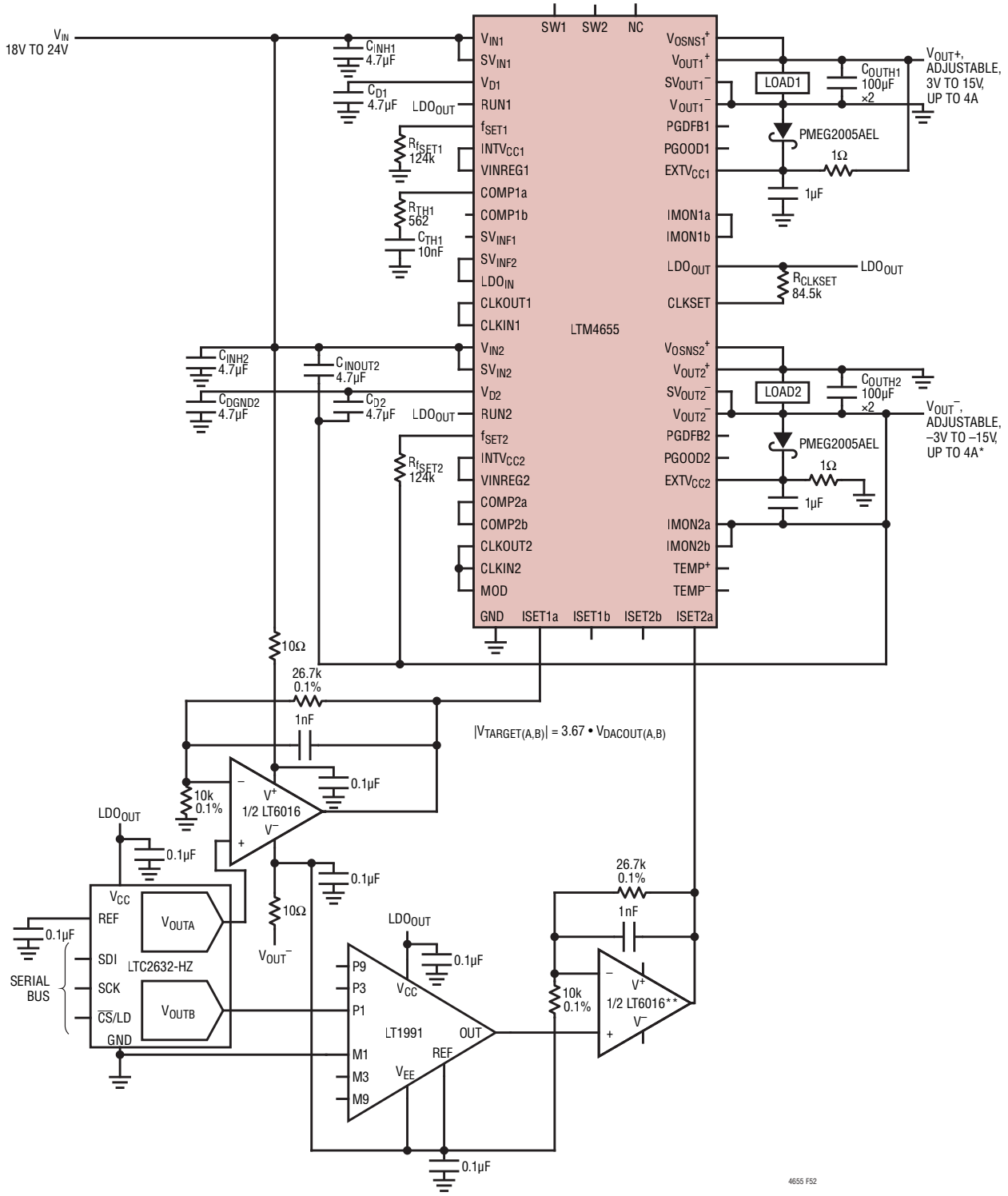


Figure 51. Dual 4A, 12V and 5V Output DC/DC µModule Regulator

TYPICAL APPLICATIONS



*SEE TABLE 6 AND APPLICATIONS INFORMATION SECTION FOR NEGATIVE OUTPUT CURRENT CAPABILITY
**BOTH HALVES OF LT6016 ON SAME SUPPLY

Figure 52. A DAC-Controlled Bipolar-Output Programmable Power Supply

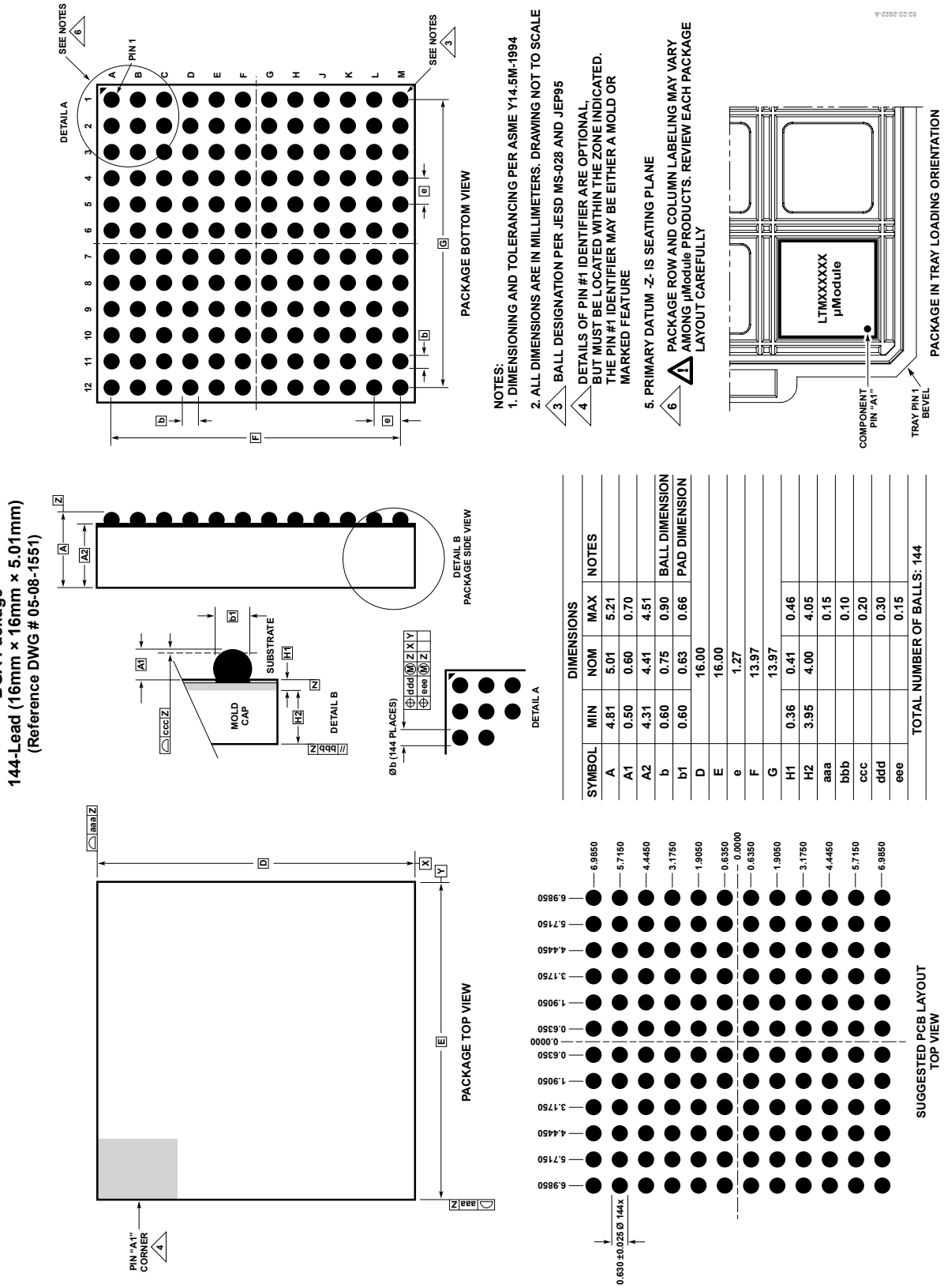
PACKAGE DESCRIPTION

Table 13. LTM4655 Component BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{IN1}	B1	CLKIN1	C1	IMON1b	D1	PGOOD1	E1	COMP1b	F1	ISET1b
A2	V_{IN1}	B2	CLKOUT1	C2	IMON1a	D2	PGDFB1	E2	COMP1a	F2	ISET1a
A3	V_{IN1}	B3	V_{IN1}	C3	SV_{IN1}	D3	VINREG1	E3	f_{SET1}	F3	$EXTV_{CC1}$
A4	V_{D1}	B4	V_{D1}	C4	V_{D1}	D4	GND	E4	SV_{OUT1}^-	F4	RUN1
A5	V_{OUT1}^-	B5	V_{OUT1}^-	C5	V_{OUT1}^-	D5	V_{OUT1}^-	E5	V_{OUT1}^-	F5	V_{OUT1}^-
A6	V_{IN2}	B6	CLKIN2	C6	IMON2b	D6	PGOOD2	E6	COMP2b	F6	ISET2b
A7	V_{IN2}	B7	CLKOUT2	C7	IMON2a	D7	PGDFB2	E7	COMP2a	F7	ISET2a
A8	V_{IN2}	B8	V_{IN2}	C8	SV_{IN2}	D8	VINREG2	E8	f_{SET2}	F8	$EXTV_{CC2}$
A9	V_{D2}	B9	V_{D2}	C9	V_{D2}	D9	GND	E9	SV_{OUT2}^-	F9	RUN2
A10	V_{OUT2}^-	B10	V_{OUT2}^-	C10	V_{OUT2}^-	D10	V_{OUT2}^-	E10	V_{OUT2}^-	F10	V_{OUT2}^-
A11	V_{OUT2}^-	B11	SV_{INF1}	C11	SV_{INF2}	D11	V_{OUT2}^-	E11	V_{OUT2}^-	F11	V_{OUT2}^-
A12	V_{OUT2}^-	B12	LDO_{IN}	C12	CLKOUT2	D12	GND	E12	MOD	F12	CLKSET

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	V_{OSNS1}^+	H1	V_{OSNS1}^+	J1	NC	K1	V_{OUT1}^+	L1	V_{OUT1}^+	M1	V_{OUT1}^+
G2	SV_{OUT1}^-	H2	SV_{OUT1}^-	J2	NC	K2	V_{OUT1}^+	L2	V_{OUT1}^+	M2	V_{OUT1}^+
G3	$INTV_{CC1}$	H3	V_{OUT1}^-	J3	V_{OUT1}^-	K3	V_{OUT1}^+	L3	V_{OUT1}^+	M3	V_{OUT1}^+
G4	V_{OUT1}^-	H4	SW1	J4	V_{OUT1}^-	K4	V_{OUT1}^-	L4	V_{OUT1}^-	M4	V_{OUT1}^-
G5	V_{OUT1}^-	H5	V_{OUT1}^-	J5	V_{OUT1}^-	K5	V_{OUT1}^-	L5	V_{OUT1}^-	M5	V_{OUT1}^-
G6	V_{OSNS2}^+	H6	V_{OSNS2}^+	J6	$TEMP^+$	K6	V_{OUT2}^+	L6	V_{OUT2}^+	M6	V_{OUT2}^+
G7	SV_{OUT2}^-	H7	SV_{OUT2}^-	J7	$TEMP^-$	K7	V_{OUT2}^+	L7	V_{OUT2}^+	M7	V_{OUT2}^+
G8	$INTV_{CC2}$	H8	V_{OUT2}^-	J8	V_{OUT2}^-	K8	V_{OUT2}^+	L8	V_{OUT2}^+	M8	V_{OUT2}^+
G9	V_{OUT2}^-	H9	SW2	J9	V_{OUT2}^-	K9	V_{OUT2}^-	L9	V_{OUT2}^-	M9	V_{OUT2}^-
G10	V_{OUT2}^-	H10	V_{OUT2}^-	J10	V_{OUT2}^-	K10	V_{OUT2}^-	L10	V_{OUT2}^-	M10	V_{OUT2}^-
G11	V_{OUT2}^-	H11	V_{OUT2}^-	J11	NC	K11	V_{OUT2}^-	L11	V_{OUT2}^-	M11	V_{OUT2}^-
G12	LDO_{OUT}	H12	V_{OUT2}^-	J12	NC	K12	V_{OUT2}^-	L12	V_{OUT2}^-	M12	V_{OUT2}^-

PACKAGE DESCRIPTION



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.81	5.01	5.21	
A1	0.50	0.60	0.70	
A2	4.31	4.41	4.51	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		16.00		
E		16.00		
e		1.27		
F		13.97		
G		13.97		
H1	0.36	0.41	0.46	
H2	3.95	4.00	4.05	
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 144				

Rev. B

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/22	Reordered pin names according to pin number instead of function.	14-20
		Corrected SSFM acronym typo.	15
		Corrected CLKSET-supported switching frequency range and corresponding resistor-setting values.	19
		Corrected SW pin typo.	22
		Corrected pin name typos to indicate italic “n” subscript suffix, where missing.	23
		Clarified supported positive output voltage range.	25
		Fixed Equation 5 typo.	26
		Corrected numerical reference to Loop Compensation tables.	29
		Fixed typo referencing f_{SW}.	34
B	03/22	Amended POD.	54
		Added ink marking statement to package photos.	56

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