A 7-Bit Current DAC with PMBus Interface

FEATURES

- **±0.8% I_{DAC} Positive Output Current Accuracy (Over Temp)**
- **±1.5% I_{DAC} Negative Output Current Accuracy (Over Temp)**
- **PMBus/I²C Compliant Serial Interface**
- **Input Voltage Range: 2.5V to 5.5V**
- **High Impedance at IDAC Output When Disabled**
- **Wide IDAC Operation Voltage (0.4V to 2.0V)**
- 7-Bit Programmable DAC Output Current for DC/DC V_{OUT} Control
- Wide Range IDAC Output Current: ±16µA to ±256µA
- Programmable Slew Rate: 500ns ~ 3ms per Bit
- Available in a 10-Lead (3mm × 2mm) DFN Package

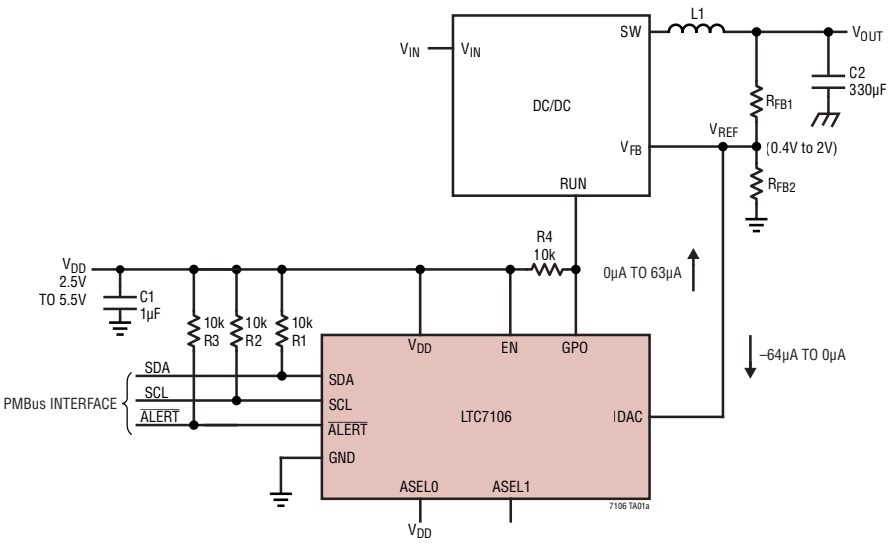
APPLICATIONS

- General Purpose Power Systems
- Telecom Systems
- Industrial Applications

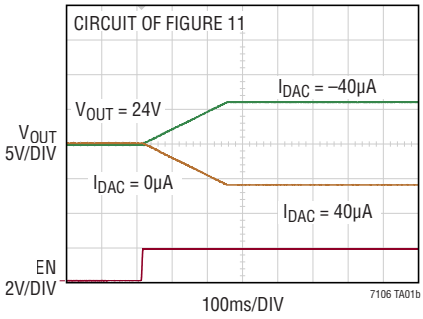
DESCRIPTION

The LTC®7106 is a precision, PMBus controlled, bidirectional current digital-to-analog converter that adjusts the output voltage of any conventional V_{FB} referenced regulator. The LTC7106 can work with the vast majority of power management controllers or regulators to enable digital control of the output voltage. Internal power-on reset circuitry keeps the DAC output current at zero (high impedance IDAC) until a valid write takes place. Features include a range bit for easy interfacing to almost any impedance resistor divider, and an open-drain GPO output for controlling the Run or Enable pin of the DC/DC regulator. For most applications, the current DAC error is significantly attenuated with proper design. See more detail about V_{OUT} accuracy in the Applications Information section of this data sheet. The LTC7106 is supported by the ADI LTpowerPlay® development tool with graphical user interface (GUI).

TYPICAL APPLICATION



Margin High and Margin Low

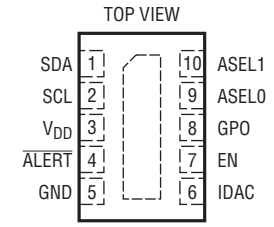


ABSOLUTE MAXIMUM RATINGS

(Note 1)

All Pins Except GND ..... –0.3V to 6.0V
Operating Junction Temperature Range... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DDB PACKAGE
10-LEAD (3mm × 2mm) PLASTIC DFN
θ_{JA} = 55°C/W, θ_{JC} = 16.8°C/W

ORDER INFORMATION

http://www.linear.com/product/LTC7106#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7106EDDB#PBF	LTC7106EDDB#TRPBF	LHCG	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LTC7106IDDB#PBF	LTC7106IDDB#TRPBF	LHCG	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{DD} = 3.3V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{DD}	Power Supply				2.5		5.5	V
I_Q	Supply Quiescent Current	EN High				700	1400	µA
$I_{SHUTDOWN}$	Supply Quiescent Current	EN = 0V				800		µA
V_{UVLO_R}	Undervoltage Rising Threshold	V_{DD} Rising				2.35		V
V_{UVLO_F}	Undervoltage Falling Threshold	V_{DD} Falling				2.15		V
V_{EN_R}	Enable Rising Threshold	V_{EN} Rising					1.35	V
V_{EN_F}	Enable Falling Threshold	V_{EN} Falling			0.8			V
IDAC_OUT								
I_{DAC}	Accuracy	Full Scale Positive $0.4 \le V_{IDAC} \le 2V$ (Note 3)	Range = Normal	●	62.5	63	63.5	µA
			Range = Low	●	15.5	15.75	16.0	µA
			Range = High	●	246.7	252.00	255.3	µA
		Full Scale Negative $0.4 \le V_{IDAC} \le 2V$ (Note 3)	Range = Normal (0°C to 85°C)		–64.64	–64	–63.36	µA
			Range = Normal	●	–64.96	–64	–63.04	µA
			Range = Low	●	–16.36	–16	–15.64	µA
			Range = High	●	–262.50	–256	–249.50	µA
LSB		$0.4 \le V_{IDAC} \le 2V$	Range = Normal			1		µA
			Range = Low			0.25		µA
			Range = High			4		µA
INL		$0.4 \le V_{IDAC} \le 2V$	Range = Normal		–1		1	LSB
			Range = Low		–1.5		1.5	LSB
			Range = High		–1.6		1.6	LSB
DNL		$0.4 \le V_{IDAC} \le 2V$	Range = Normal		–0.3		0.3	LSB
			Range = Low		–0.5		0.5	LSB
			Range = High		–0.8		0.8	LSB
IHZ	High-Z Current	$0.4 \le V_{IDAC} \le 2V$	V_{EN} = 0	●			20	nA
Digital Input: SDA, SCL								
V_{IH}							1.4	V
V_{IL}					0.8			V
C_{PIN}	Input Capacitance						10	pF
Open-Drain Outputs: ALERTB, GPO, SDA								
V_{OL}	Output Low Voltage	I_{SINK} = 3mA					0.4	V

PMBus INTERFACE TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{DD} = 3.3V, unless otherwise specified.

SYMBOL	PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
f_{SCL}	Serial Bus Operating Frequency			10		400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition			1.3			µs
t_{HD_SDA}	Hold Time After (Repeated) Start Condition			0.6			µs
t_{SU_SDA}	Repeated Start Condition Setup Time			0.6			µs
t_{SU_STO}	Stop Condition Setup Time			0.6			µs
$t_{HD\_DAT(OUT)}$	Data Hold Time			300		900	ns
$t_{HD\_DAT(IN)}$	Input Data Hold Time			0			ns
t_{SU_DAT}	Data Setup Time			100			ns
t_{LOW}	Clock Low Period			1.3		10000	µs
t_{HIGH}	Clock High Period			0.6			µs
$t_{TIMEOUT\_SMB}$	Stuck PMBus Timer				30		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7106 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7106E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7106I is guaranteed over the –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

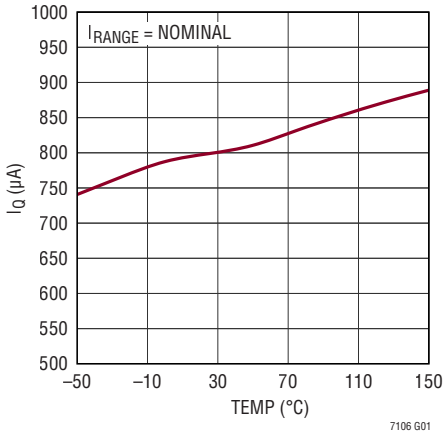
$$T_J = T_A + (P_D \bullet 55°C/W).$$

Note 3: IDAC is a bidirectional current DAC, controlled by 2's complementary logic. Under the setting of Range = Normal, I_{DAC} = 63µA for Code = 0111111 provides the maximum source current and I_{DAC} = –64µA for Code = 1000000 provides the maximum sink current. Max sink current generates the Highest V_{OUT}, while Max source current generates the lowest V_{OUT}. See the Operation section for more details.

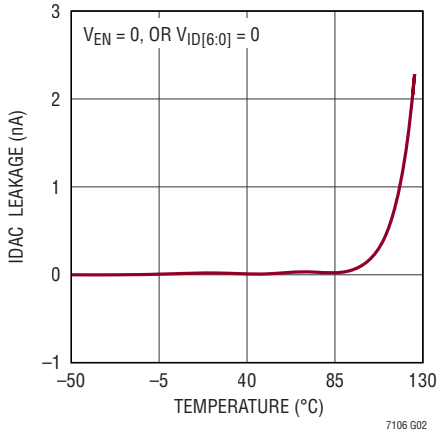
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 3.3V, V_{IDAC} = 1.0V, Range = Normal unless otherwise noted.

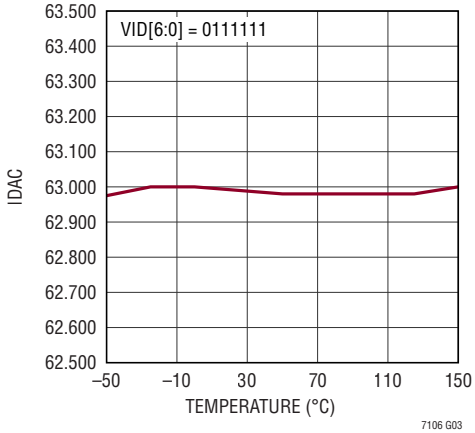
Quiescent Current vs Temperature



IDAC Leakage Current vs Temperature



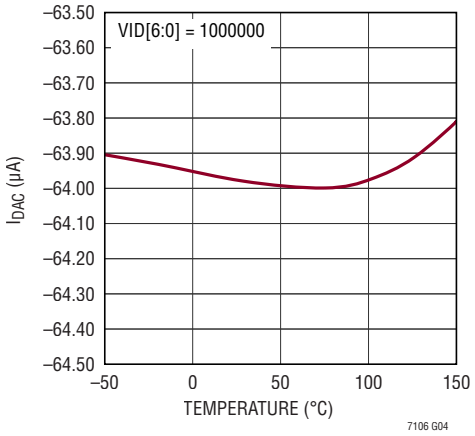
PIDAC Full-Scale vs Temperature



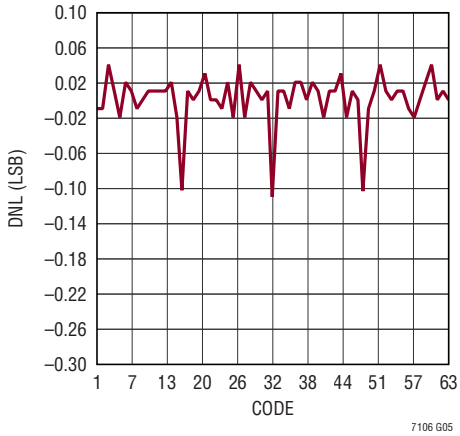
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 3.3V, Range = Normal unless otherwise noted.

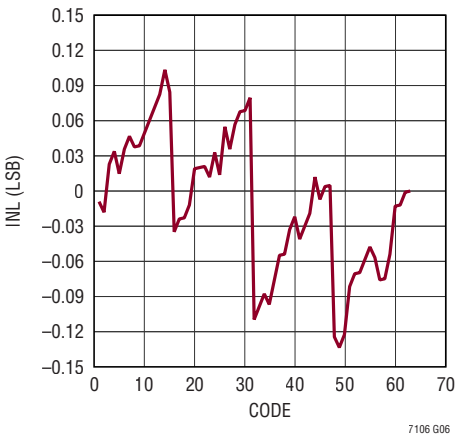
NIDAC vs Temperature



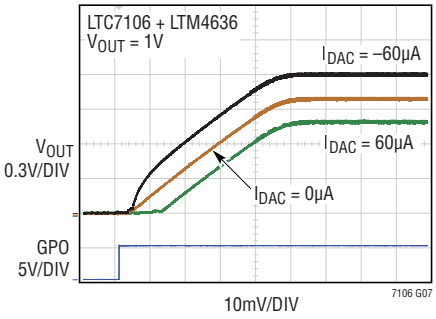
Differential Nonlinearity



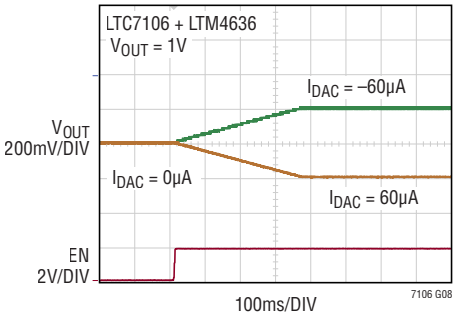
Integral Nonlinearity



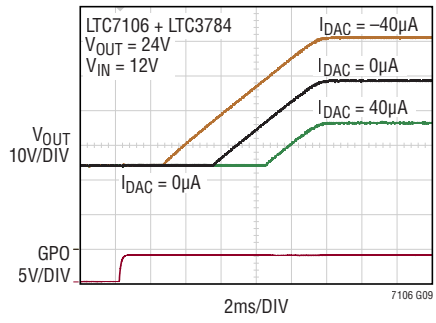
Buck Start-Up with IDAC



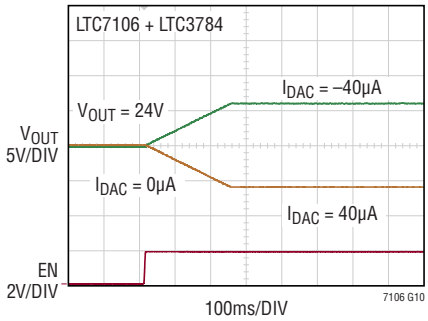
Margin High and Margin Low



Boost Start-Up with IDAC



Margin High and Margin Low



PIN FUNCTIONS

V_{DD} (Pin 3): Input Supply. Bypass this pin to GND with a capacitor (0.1µF to 1µF).

IDAC (Pin 6): Bidirectional Current DAC Output.

EN (Pin 7): Chip Enable Pin. Current DAC output is in Hi-Z state when EN is Grounded. Do not leave EN floating.

SDA (Pin 1): Serial Bus Data Input and Open-Drain Output. A pull-up resistor to V_{DD} is required in the application.

SCL (Pin 2): Serial Bus Clock Input.

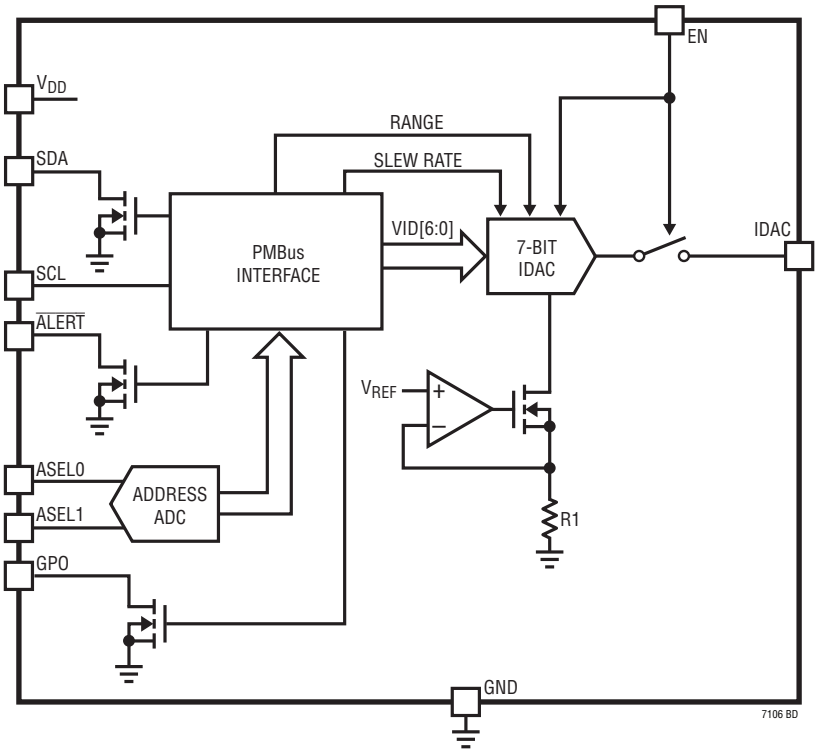
GPO (Pin 8): Open-Drain Digital Output. A pull-up resistor to V_{DD} is required.

$\overline{\text{ALERT}}$ (Pin 4): Open-Drain Digital Output. A pull-up resistor to V_{DD} is required.

ASEL1/ASEL0 (Pins 10, 9): Serial Bus Address Select Inputs. Each pin has three states (V_{DD}, FLOATING and GND); these two pins provide 9 addresses.

GND (Pin 5): Ground.

BLOCK DIAGRAM



OPERATION

The LTC7106 is a PMBus controlled 7-bit D/A converter current source. Through its PMBus interface, the LTC7106 receives a 7-bit DAC code and converts this value to a bidirectional analog output current through the pin IDAC. By connecting IDAC to the feedback node of a voltage regulator, I_{DAC} can change the output voltage of the regulator with the equation:

$$V_{OUT} = V_{REF} \bullet (1 + R_{FB1}/R_{FB2}) – I_{DAC} \bullet R_{FB1}$$

where V_{REF} is the reference voltage of the voltage regulator. R_{FB1} and R_{FB2} are the resistor divider for the voltage regulator. I_{DAC} is the programmed bidirectional current shown in Table 2.

A typical application diagram is shown on the front page. Therefore, the traditional pure analog designed oriented PWM controller can be controlled by a PMBus interface.

This illustrates the flexibility of the LTC7106 providing a PMBus interface to conventional analog DC/DC converters.

CHIP ENABLE (EN PIN)

The LTC7106 is activated by the EN pin. It turns on/off the device with threshold of 1.2V. When EN is low (<1.2V), IDAC is in high impedance (Hi-Z).

However, PMBus interface is still active when EN is low which means users can program the device and readback the internal register's value. The device will execute the commands of MFR_IOUT_COMMAND, MFR_IOUT_MARGIN_HIGH, MFR_IOUT_MARGIN_LOW after EN goes high.

SLEW RATE CONTROL

To prevent abrupt changes in the D/A output current and subsequently the output voltage of the DC/DC regulator, an internal digital programmable slew rate control is included. The slew rate range can be programmed with a 6-bit register from 0.5µs/step to 3.58ms/step with a default value of 3.58ms/step.

CURRENT RANGE SETTING AND D/A PROGRAMMING

The LTC7106 is a 7-bit bidirectional current DAC with a 1µA LSB as its default setting. The MSB determines the current direction. When MSB is 0, I_{DAC} is sourcing current (reducing V_{OUT}), which is positive current flowing out of the pin, and when MSB is 1, I_{DAC} is sinking current (increasing V_{OUT}), which is negative current flowing into the pin. The LTC7106 also provides range high and range low options through its digital interface to change the LSB value to 4µA expanding the output current range and subsequently widening the programmable output voltage range. Alternately for higher resolution, the low range is provided with a LSB of 0.25µA. Users have additional flexibility of choosing the resistor divider ratio and resistor values to meet the output specification target. However, the design is most accurate using the nominal range which is the recommended setting. Table 1 lists the output current range and Table 2 lists the detailed DAC codes vs I_{DAC} current.

Table 1. Output Current Range

Range	LSB (µA)	I_{MIN} (µA)	I_{MAX} (µA)
Nominal	1	–64	63
Range High	4	–256	252
Range Low	0.25	–16	15.75

OPERATION

Table 2. IDAC Current and Corresponding DAC Codes

DAC CODE							I_{DAC} (µA)		
[6]	[5]	[4]	[3]	[2]	[1]	[0]	NOMINAL	RANGE HIGH	RANGE LOW
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1	4	0.25
0	0	0	0	0	1	0	2	8	0.5
0	0	0	0	0	1	1	3	12	0.75
0	0	0	0	1	0	0	4	16	1
0	0	0	0	1	0	1	5	20	1.25
0	0	0	0	1	1	0	6	24	1.5
0	0	0	0	1	1	1	7	28	1.75
0	0	0	1	0	0	0	8	32	2
0	0	0	1	0	0	1	9	36	2.25
0	0	0	1	0	1	0	10	40	2.5
0	0	0	1	0	1	1	11	44	2.75
0	0	0	1	1	0	0	12	48	3
0	0	0	1	1	0	1	13	52	3.25
0	0	0	1	1	1	0	14	56	3.5
0	0	0	1	1	1	1	15	60	3.75
0	0	1	0	0	0	0	16	64	4
0	0	1	0	0	0	1	17	68	4.25
0	0	1	0	0	1	0	18	72	4.5
0	0	1	0	0	1	1	19	76	4.75
0	0	1	0	1	0	0	20	80	5
0	0	1	0	1	0	1	21	84	5.25
0	0	1	0	1	1	0	22	88	5.5
0	0	1	0	1	1	1	23	92	5.75
0	0	1	1	0	0	0	24	96	6
0	0	1	1	0	0	1	25	100	6.25
0	0	1	1	0	1	0	26	104	6.5
0	0	1	1	0	1	1	27	108	6.75
0	0	1	1	1	0	0	28	112	7
0	0	1	1	1	0	1	29	116	7.25
0	0	1	1	1	1	0	30	120	7.5
0	0	1	1	1	1	1	31	124	7.75
0	1	0	0	0	0	0	32	128	8
0	1	0	0	0	0	1	33	132	8.25
0	1	0	0	0	1	0	34	136	8.5
0	1	0	0	0	1	1	35	140	8.75
0	1	0	0	1	0	0	36	144	9
0	1	0	0	1	0	1	37	148	9.25
0	1	0	0	1	1	0	38	152	9.5
0	1	0	0	1	1	1	39	156	9.75
0	1	0	1	0	0	0	40	160	10
0	1	0	1	0	0	1	41	164	10.25
0	1	0	1	0	1	0	42	168	10.5
0	1	0	1	0	1	1	43	172	10.75
0	1	0	1	1	0	0	44	176	11
0	1	0	1	1	0	1	45	180	11.25
0	1	0	1	1	1	0	46	184	11.5
0	1	0	1	1	1	1	47	188	11.75
0	1	1	0	0	0	0	48	192	12
0	1	1	0	0	0	1	49	196	12.25
0	1	1	0	0	1	0	50	200	12.5
0	1	1	0	0	1	1	51	204	12.75
0	1	1	0	1	0	0	52	208	13
0	1	1	0	1	0	1	53	212	13.25
0	1	1	0	1	1	0	54	216	13.5
0	1	1	0	1	1	1	55	220	13.75
0	1	1	1	0	0	0	56	224	14
0	1	1	1	0	0	1	57	228	14.25
0	1	1	1	0	1	0	58	232	14.5
0	1	1	1	0	1	1	59	236	14.75
0	1	1	1	1	0	0	60	240	15
0	1	1	1	1	0	1	61	244	15.25
0	1	1	1	1	1	0	62	248	15.5
0	1	1	1	1	1	1	63	252	15.75
1	0	0	0	0	0	0	–64	–256	–16
1	0	0	0	0	0	1	–63	–252	–15.75
1	0	0	0	0	1	0	–62	–248	–15.5
1	0	0	0	0	1	1	–61	–244	–15.25
1	0	0	0	1	0	0	–60	–240	–15
1	0	0	0	1	0	1	–59	–236	–14.75
1	0	0	0	1	1	0	–58	–232	–14.5
1	0	0	0	1	1	1	–57	–228	–14.25
1	0	0	1	0	0	0	–56	–224	–14
1	0	0	1	0	0	1	–55	–220	–13.75
1	0	0	1	0	1	0	–54	–216	–13.5
1	0	0	1	0	1	1	–53	–212	–13.25

OPERATION

Table 2. IDAC Current and Corresponding DAC Codes (Continued)

DAC CODE							I_{DAC} (µA)		
[6]	[5]	[4]	[3]	[2]	[1]	[0]	NOMINAL	RANGE HIGH	RANGE LOW
1	0	0	1	1	0	0	–52	–208	–13
1	0	0	1	1	0	1	–51	–204	–12.75
1	0	0	1	1	1	0	–50	–200	–12.5
1	0	0	1	1	1	1	–49	–196	–12.25
1	0	1	0	0	0	0	–48	–192	–12
1	0	1	0	0	0	1	–47	–188	–11.75
1	0	1	0	0	1	0	–46	–184	–11.5
1	0	1	0	0	1	1	–45	–180	–11.25
1	0	1	0	1	0	0	–44	–176	–11
1	0	1	0	1	0	1	–43	–172	–10.75
1	0	1	0	1	1	0	–42	–168	–10.5
1	0	1	0	1	1	1	–41	–164	–10.25
1	0	1	1	0	0	0	–40	–160	–10
1	0	1	1	0	0	1	–39	–156	–9.75
1	0	1	1	0	1	0	–38	–152	–9.5
1	0	1	1	0	1	1	–37	–148	–9.25
1	0	1	1	1	0	0	–36	–144	–9
1	0	1	1	1	0	1	–35	–140	–8.75
1	0	1	1	1	1	0	–34	–136	–8.5
1	0	1	1	1	1	1	–33	–132	–8.25
1	1	0	0	0	0	0	–32	–128	–8
1	1	0	0	0	0	1	–31	–124	–7.75
1	1	0	0	0	1	0	–30	–120	–7.5
1	1	0	0	0	1	1	–29	–116	–7.25
1	1	0	0	1	0	0	–28	–112	–7
1	1	0	0	1	0	1	–27	–108	–6.75
1	1	0	0	1	1	0	–26	–104	–6.5
1	1	0	0	1	1	1	–25	–100	–6.25
1	1	0	1	0	0	0	–24	–96	–6
1	1	0	1	0	0	1	–23	–92	–5.75
1	1	0	1	0	1	0	–22	–88	–5.5
1	1	0	1	0	1	1	–21	–84	–5.25
1	1	0	1	1	0	0	–20	–80	–5
1	1	0	1	1	0	1	–19	–76	–4.75
1	1	0	1	1	1	0	–18	–72	–4.5
1	1	0	1	1	1	1	–17	–68	–4.25
1	1	1	0	0	0	0	–16	–64	–4
1	1	1	0	0	0	1	–15	–60	–3.75
1	1	1	0	0	1	0	–14	–56	–3.5
1	1	1	0	0	1	1	–13	–52	–3.25
1	1	1	0	1	0	0	–12	–48	–3
1	1	1	0	1	0	1	–11	–44	–2.75
1	1	1	0	1	1	0	–10	–40	–2.5
1	1	1	0	1	1	1	–9	–36	–2.25
1	1	1	1	0	0	0	–8	–32	–2
1	1	1	1	0	0	1	–7	–28	–1.75
1	1	1	1	0	1	0	–6	–24	–1.5
1	1	1	1	0	1	1	–5	–20	–1.25
1	1	1	1	1	0	0	–4	–16	–1
1	1	1	1	1	0	1	–3	–12	–0.75
1	1	1	1	1	1	0	–2	–8	–0.5
1	1	1	1	1	1	1	–1	–4	–0.25

OPERATION

GPO

GPO is a general purpose open-drain output pin, which can be set by PMBus command. It is designed to turn on/off the DC/DC regulator by connecting GPO to the RUN pin of the regulator. Once GPO is set high, it stays high even if the EN pin goes low as long as the device is not power cycled.

ADDRESS

The PMBus address is selected by ASEL0 and ASEL1 pins. Each pin has three states: high, low and floating. The possible PMBus addresses are shown in Table 3.

Table 3. Address Selection

ASEL1	ASEL0	PMBus ADDRESS
GND	GND	2A
GND	V_{DD}	2C
GND	FLOAT	2E
V_{DD}	GND	4A
V_{DD}	V_{DD}	4C
V_{DD}	FLOAT	4E
FLOAT	GND	6A
FLOAT	V_{DD}	6C
FLOAT	FLOAT	6E

PMBus SERIAL INTERFACE

The LTC7106 serial interface is a PMBus-compliant slave device and can operate at any frequency between 10kHz and 400kHz. In addition the LTC7106 always responds to the global broadcast address of 0x5A or 0x5B (7-bit). The serial interface supports the following protocols defined in the PMBus specifications: 1) send command, 2) write byte, 3) group, 4) read byte and 5) read word. The PMBus write operations are not acted upon until a complete valid message is received by the LTC7106 including the STOP bit.

Communication Failure

Attempts to access unsupported commands or writing invalid data to supported commands will result in a CML fault. The CML bit is set in the STATUS_BYTE command and the $\overline{\text{ALERT}}$ pin is pulled low.

Device Addressing

The LTC7106 offers four different types of addressing over the PMBus interface, specifically: 1) global, 2) device, 3) rail addressing and 4) alert response address (ARA).

Global addressing provides a means of the PMBus master to address all LTC7106 devices on the bus. The LTC7106 global addresses are fixed 0x5A or 0x5B (7 bit) or 0xB4 or 0xB6 (8 bit) and cannot be disabled.

Device addressing provides the standard means of the PMBus master communicating with a single instance of a LTC7106. The value of the device address is set by the ASEL0/ASEL1 configuration pins. Rail addressing provides a means of the PMBus master addressing a set of channels connected to the same output rail, simultaneously. This is similar to global addressing, however, the PMBus address can be dynamically assigned by using the MFR_RAIL_ADDRESS command. It is recommended that rail addressing should be limited to command write operations.

All four means of PMBus addressing require the user to employ disciplined planning to avoid addressing conflicts.

Fault Status

The STATUS_BYTE and $\overline{\text{ALERT}}$ pin provide fault status information of the LTC7106 to the host.

Bus Timeout Failure

The LTC7106 implements a timeout feature to avoid hanging the serial interface. The data packet timer begins at the first START event before the device address write byte. Data packet information must be completed within 25ms or the LTC7106 will tri-state the bus and ignore the given data packet. Data packet information includes the device address byte write, command byte, repeat start event (if a read operation), device address byte read (if a read operation), and all data bytes.

The user is encouraged to use as high a clock rate as possible to maintain efficient data packet transfer between all devices sharing the serial bus interface. The LTC7106 supports the full PMBus frequency range from 10kHz to 400kHz.

OPERATION

Similarity Between PMBus, SMBus and I²C 2-Wire Interface

The PMBus 2-wire interface is an incremental extension of the SMBus. SMBus is built upon I²C with some minor differences in timing, DC parameters and protocol. The PMBus/SMBus protocols are more robust than simple I²C byte commands because PMBus/SMBus provide timeouts to prevent bus hangs and valid operation commands. In general, a master device that can be configured for I²C communication can be used for PMBus communication with little or no change to hardware or firmware. Repeat start (restart) is not supported by all I²C controllers but is required for SMBus/PMBus reads. If a general purpose I²C controller is used, check that repeat start is supported.

For a description of the minor extensions and exceptions PMBus makes to SMBus, refer to PMBus Specification Part 1, Revision 1.1: Paragraph 5: Transport.

For a description of the differences between SMBus and I²C, refer to System Management Bus (SMBus) Specification Version 2.0: Appendix B—Differences Between SMBus and I²C.

PMBus SERIAL INTERFACE

The LTC7106 communicates with a host (master) using the standard PMBus serial bus interface. The Timing Diagram, Figure 1, shows the timing relationship of the signals on the bus. The two-bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTC7106 is a slave device. The master can communicate with the LTC7106 using the following formats:

- Master Transmitter, Slave Receiver
- Master Receiver, Slave Transmitter

The following PMBus protocols are supported:

- Write Byte, Send Byte
- Read Byte, Read Word
- Alert Response Address

Figure 3 through Figure 6 illustrate the aforementioned PMBus protocols. All transactions support GCP (group command protocol).

Figure 2 is a key to the protocol diagrams in this section.

A value shown below a field in the following figures is a mandatory value for that field.

The data formats implemented by PMBus are:

- Master transmitter transmits to slave receiver. The transfer direction in this case is not changed.
- Master reads slave immediately after the first byte. At the moment of the first acknowledgment (provided by the slave receiver) the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter.
- Combined format. During a change of direction within a transfer, the master repeats both a start condition and the slave address but with the R/$\overline{W}$ bit reversed. In this case, the master receiver terminates the transfer by generating a NACK on the last byte of the transfer and a STOP condition.

Examples of these formats are shown in Figure 4 and Figure 5.

OPERATION

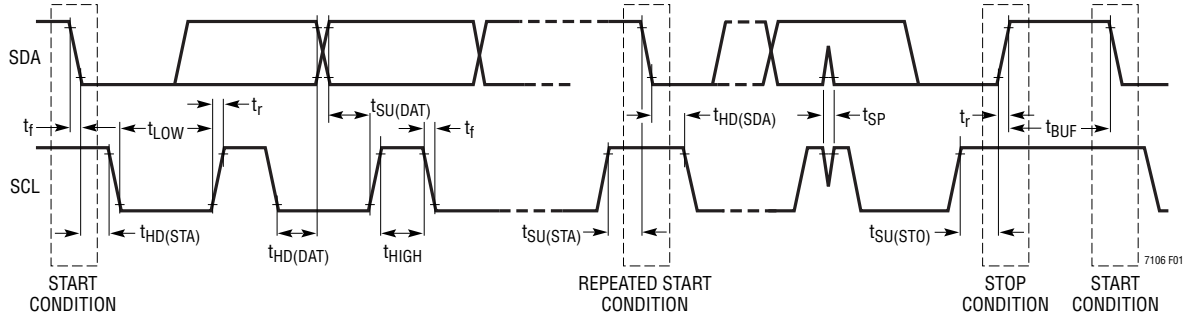
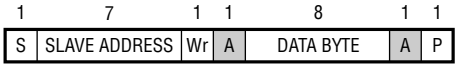


Figure 1. Timing Diagram



S	START CONDITION
Sr	REPEATED START CONDITION
Rd	READ (BIT VALUE OF 1)
Wr	WRITE (BIT VALUE OF 0)
x	SHOWN UNDER A FIELD INDICATES THAT THAT FIELD IS REQUIRED TO HAVE THE VALUE OF x
A	ACKNOWLEDGE (THIS BIT POSITION MAY BE 0 FOR AN ACK OR 1 FOR A NACK)
P	STOP CONDITION
PEC	PACKET ERROR CODE
☐	MASTER TO SLAVE
▒	SLAVE TO MASTER
...	CONTINUATION OF PROTOCOL

7106 F02

Figure 2. PMBus Packet Protocol Diagram Element Key

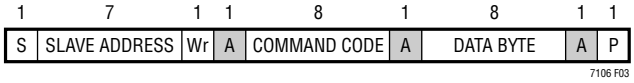


Figure 3. Write Byte Protocol

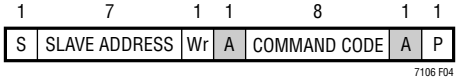


Figure 4. Send Byte Protocol

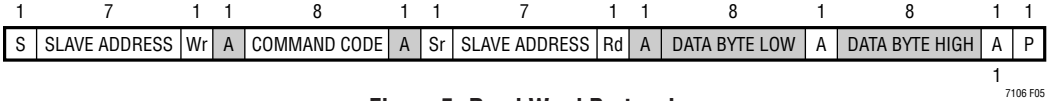


Figure 5. Read Word Protocol

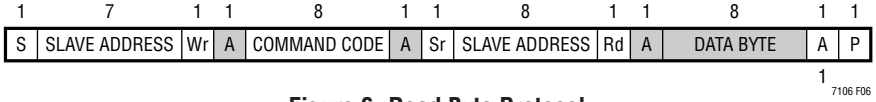


Figure 6. Read Byte Protocol

REGISTER COMMAND DETAILS

Table 4. LTC7106 Supported PMBus Commands

PMBus CODE (8 BITS)	R/W TYPE	COMMAND NAME	DESCRIPTION
0x01	R/W	OPERATION	Default is On: [7:0] = 0x80
0x78	R/W	STATUS_BYTE	Read Fault Status: CML, Write 1 to Reset
0x98	Read	PMBUS_REVISION	Read PMBus Revision = 0x22 for Rev 1.2
0xE2	R/W	MFR_CHIP_CTRL	[7:4] – Reserved: [7:0] = 0x00 Default [0] = GPO EN, [1] = Reserved, [2] = Write Protect, [3] = Timeout Status
0xE4	R/W	MFR_DAC_CTRL	[7:6] = Current Step Control, [5:0] = DAC Slew Rate Control
0xE5	R/W	MFR_IOUT_MARGIN_HIGH	Same Format as MFR_IOUT_COMMAND
0xE6	R/W	MFR_IOUT_MAX	Clamped Value that DAC Cannot Exceed. Default 7-Bit Value of 0x00 = Source Current Only
0xE7	Read	MFR_SPECIAL_ID	MFR Special ID for LTC7106 = 0x8080
0xE8	R/W	MFR_IOUT_COMMAND	I_{OUT} Margining Command (see Table 5) [5:0] Step Value, Source: [6] = 0, Sink: [6] = 1
0xED	R/W	MFR_IOUT_MARGIN LOW	Same Format as MFR_IOUT_COMMAND
0xFA	R/W	MFR_RAIL_ADDRESS	Set Common PMBus Address [6:0], [7] = 0 Enable, [7] = 1 Disable
0xFD	Write	MFR_RESET	Reset PMBus Interface to Power-On State Write Data is Ignored; 0, 1, 2 Bytes

MFR_IOUT_COMMAND

The DAC output current command is formatted as a 7-bit 2's complement value. When the operation register is set to 0x80, DAC takes the value stored in this register. Setting bit[6] to 0 sources the current from the IC and bit[6] to 1 sinks the current into the IC. Default value for this register is 0x00. The valid range of values are from 0x40 to 0x3F.

Do not attempt to write values outside of this range or undesired behavior may result. Writes to this register are inhibited when the WPB, bit [2] in MFR_CHIP_CTRL, is set high.

MFR_IOUT_MARGIN_HIGH

DAC margining register with the same format and rules as MFR_IOUT_COMMAND. The DAC value will take the value stored in this register when the operation register is set to margin high, 0xA8.

MFR_IOUT_MARGIN_LOW

DAC margining register with the same format and rules as MFR_IOUT_COMMAND. The DAC value will take the value stored in this register when the operation register is set to margin low, 0x98.

MFR_IOUT_MAX

Clamping value that DAC cannot exceed. The format is a 7-bit 2's complement value, the same as the margin registers. Therefore, the DAC value cannot be a smaller 2's complement value than what is stored in this register.

The 7-bit default value is 0x00 = cannot sink current. I_{OUT} cannot be set to a higher value unless this value is changed to a negative number, bit [7] = 1.

Setting this register to 0x40 allows the LTC7106 to sink the maximum current with no clamping.

REGISTER COMMAND DETAILS

MFR_CHIP_CTRL

This register is for general chip control and status. Please refer to Table 7 for each bit description.

Bits **Description**

[7:4] Reserved

[3] Timeout Status:

0 = No PMBus Timeout Occurred

1 = A Timeout Occurred

Writing a 1 to this bit will clear this bit

[2] Write Protect for Margin Registers

0 = Write Allowed

1 = Writes Inhibited

[1] Reserved

[0] GPO, General Purpose Output

0 = GPO Pulls Open Drain to GND

1 = Hi-Z on GPO

MFR_DAC_CTRL

8-bit register to control the I_{DAC} LSB current value and the timer count for the slew rate control. Default value = 0x40.

Bits **Description**

[7:6] Selector Range for I_{DAC} Step Current:

b'00 = 0.25µA/Step, Range Low

b'01 = 1.0µA/Step, Nominal

b'10 = 4.0µA/Step, Range High

b'11 = Reserved

[5:0] Selector for Time in µs/Step

Default Value 0x00 = Max = 3584µs/Step

See Table 6 for Allowable Values

Only a power cycle, POR, will reset this register to prevent unwanted immediate current changes in IDAC. MFR_RESET will not reset this register.

In addition, IDAC must be at 0x00 to change the current range selector to prevent unwanted large swings in I_{DAC} current. The time step selector, bits [5:0], can be changed at any time.

Table 5. Programmable Delay Per Current Step

Slew Rate Timer Clock (µs/Step)					
[5:0]		[5:0]		[5:0]	
0 0 0 0 0 0	= 3584	0 1 0 0 0 0	= 16	1 0 0 0 0 0	= 256
0 0 0 0 0 1	= 0.5	0 1 0 0 0 1	= 20	1 0 0 0 0 1	= 320
0 0 0 0 1 0	= 1.0	0 1 0 0 1 0	= 24	1 0 0 0 1 0	= 384
0 0 0 0 1 1	= 1.5	0 1 0 0 1 1	= 28	1 0 0 0 1 1	= 448
0 0 0 1 0 0	= 2.0	0 1 0 1 0 0	= 32	1 0 0 1 0 0	= 512
0 0 0 1 0 1	= 2.5	0 1 0 1 0 1	= 40	1 0 0 1 0 1	= 640
0 0 0 1 1 0	= 3.0	0 1 0 1 1 0	= 48	1 0 0 1 1 0	= 768
0 0 0 1 1 1	= 3.5	0 1 0 1 1 1	= 56	1 0 0 1 1 1	= 896
0 0 1 0 0 0	= 4.0	0 1 1 0 0 0	= 64	1 0 1 0 0 0	= 1280*
0 0 1 0 0 1	= 5.0	0 1 1 0 0 1	= 80	1 0 1 0 0 1	= 1280
0 0 1 0 1 0	= 6.0	0 1 1 0 1 0	= 96	1 0 1 0 1 0	= 1536
0 0 1 0 1 1	= 7.0	0 1 1 0 1 1	= 112	1 0 1 0 1 1	= 1792
0 0 1 1 0 0	= 8.0	0 1 1 1 0 0	= 128	1 0 1 1 0 0	= 2560*
0 0 1 1 0 1	= 10	0 1 1 1 0 1	= 160	1 0 1 1 0 1	= 2560
0 0 1 1 1 0	= 12	0 1 1 1 1 0	= 192	1 0 1 1 1 0	= 3584*
0 0 1 1 1 1	= 14	0 1 1 1 1 1	= 224	1 0 1 1 1 1	= 3584

* Duplicate Encoding

PMBus COMMAND DETAILS

MFR_RESET

This command provides a means by which the user can perform a reset of the LTC7106. All latched faults ($\overline{\text{ALERT}}$ and status register) and register contents will be reset to a power-on condition by this command. V_{OUT} will remain in regulation but may change due to the reset of the margin registers.

This write-only command accepts zero, one, or two data bytes but ignores them.

MFR_RAIL_ADDRESS

The MFR_RAIL_ADDRESS command allows all devices to share a common address, such as all devices attached to a single power supply rail. The desired 7-bit address value is written to the 7 bits of the data byte.

The MSB (bit B7) must be set low to enable communication using the MFR_RAIL_ADDRESS address. Setting this bit disables this address. The default for this register is 0x80.

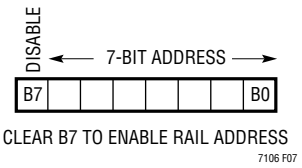


Figure 7. MFR_RAIL_ADDRESS Data Byte

The user should only perform command writes to this address. If a read is performed from this address and the rail devices do not respond with EXACTLY the same value, the LTC7106 will detect bus contention and abort its read command with no CML or ALERTB set.

This command accepts one or two data bytes but the second is ignored.

OPERATION

The OPERATION command is used to turn the unit on/off and for margining the output voltage.

The ON bit is automatically reset to ON after a master shutdown (EN), power cycle, or MFR_RESET command.

The MARGIN_LOW/HIGH bits command the I_{OUT} reference to the offset value stored in either the MFR_IOUT_MARGIN_HIGH or MFR_IOUT_MARGIN_LOW.

This command has one data byte. It will accept one or two but ignores the second byte.

Table 6. Supported OPERATION Command Register Values

ACTION	VALUE
Turn Off Immediately	0x00
Turn On	0x80
Margin Low	0x98
Margin High	0xA8

PMBus_REVISION

The PMBUS_REVISION command indicates the revision of the PMBus to which the device is compliant. The LTC7106 is PMBus Version 1.2 compliant in both Part I and Part II.

This read-only command has one data byte and will return 0x22.

MFR_SPECIAL_ID

The 16-bit word representing a unique identification for LTpowerPlay.

This read-only command has 2 data bytes and is set to 0x8080.

PMBus COMMAND DETAILS

STATUS_BYTE

The STATUS_BYTE command returns one byte of information with a summary of the unit's fault condition.

See Table 7 for a list of the status bits that are supported and the conditions in which each bit is set. Certain bits when set in the STATUS_BYTE also cause the $\overline{\text{ALERT}}$ pin to be asserted.

Writing a "1" to a particular bit in the status byte will attempt to reset that fault in the status byte and the $\overline{\text{ALERT}}$ pin. If the fault is still present the status byte bit and $\overline{\text{ALERT}}$ will remain asserted. If the $\overline{\text{ALERT}}$ has previously been cleared by an ARA message, the $\overline{\text{ALERT}}$ will be re-asserted. If the fault is no longer present, the $\overline{\text{ALERT}}$ pin will be de-asserted and the fault bit in the status byte will be cleared.

All bits in the status byte are also cleared by toggling the RUN_MSTR pin or the ON bit in OPERATION. The bit will immediately be set again if the fault remains.

Table 7. Status Byte Bit Descriptions and Conditions

BIT	DESCRIPTION	CONDITION	SET ALERT?	CLEARABLE BY WRITING '1' TO BIT?
0 (LSB)	None of the Above	MFR_VOUT_MAX Register Exceeded	No	Yes
1	Communication Failure	(See Note 1)	Yes	Yes
2	Temperature Fault	Not Implemented		
3	V_{IN} Undervoltage Fault	Not Implemented		
4	Output Overcurrent Fault	Not Implemented		
5	Output Overvoltage Fault	Not Implemented		
6	OFF	Not Implemented		
7	Busy	Not Implemented		

Note 1: Communication failure is one of following faults: host sends too few bits, host reads too few bits, host writes too few bytes, improper R/W bit set, unsupported command code, attempt to write to a read-only command. See PMBus Specification v1.2, Part II, Sections 10.8 and 10.9 for more information.

APPLICATIONS INFORMATION

I_{DAC} ACCURACY

The LTC7106 provides three ranges of I_{DAC} output current. However, only nominal range (LSB = ±1µA) is optimized with the highest accuracy. It is recommended that users design the resistor divider using the nominal range of the IDAC setting.

TWO'S COMPLEMENTARY CODE

VID [6:0] of the LTC7106 is in the format of two's complementary. From Table 2, it is easy to program the register once the desired output current is known. For example, if output current is 20µA, then set VID [6:0] = 0010100. If the output current is –20µA, then set VID [6:0] = 1101100 for the nominal I_{DAC} setting.

V_{OUT} ACCURACY

When I_{DAC} = 0, define:

$$V_{OUT0} = V_{REF}\left[1+\frac{R_{FB1}}{R_{FB2}}\right] \quad (1)$$

Referring to Figure 8, the output voltage is set according to:

$$V_{OUT} = V_{REF}\left[1+\frac{R_{FB1}}{R_{FB2}}\right] - I_{DAC} \bullet R_{FB1} \quad (2)$$

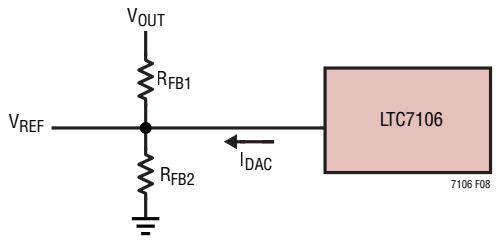


Figure 8. Setting the Output Voltage Using the LTC7106

Define ΔV_{OUT} as the V_{OUT} error caused by the I_{DAC} error ΔI_{DAC}, then we can derive the following equation from equation (1) and (2):

$$\frac{\Delta V_{OUT}}{V_{OUT}} = \left(\frac{\Delta I_{DAC} / I_{DAC}}{Ratio - 1}\right) \quad (3)$$

Where:

$$Ratio = \frac{V_{OUT0}}{I_{DAC} \bullet R_{FB1}} \quad (4)$$

It is clear that when Ratio < 0 or Ratio ≥ 2, the V_{OUT} error can be attenuated from the I_{DAC} error:

$$\left|\frac{\Delta V_{OUT}}{V_{OUT}}\right| \le \left|\frac{\Delta I_{DAC}}{I_{DAC}}\right| \quad (5)$$

In the case of margin high, I_{DAC} < 0 so Ratio < 0. Therefore, the V_{OUT} error is always smaller than the I_{DAC} error by a factor of:

$$\frac{V_{OUT0}}{I_{DAC} \bullet R_{FB1}} - 1 \quad (6)$$

In the case of margin low, I_{DAC} > 0. So the V_{OUT} error will only be attenuated when:

$$Ratio = \frac{V_{OUT0}}{I_{DAC} \bullet R_{FB1}} > 2$$

$$\text{or} \quad I_{DAC} \bullet R_{FB1} < \frac{V_{OUT0}}{2} \quad (7)$$

In other words, as long as V_{OUT} is margining low within 50% of the V_{OUT} default value, V_{OUT0}, the V_{OUT} error won't be larger than the I_{DAC} error.

DESIGN EXAMPLES

The LTC7106 can work with almost all the power management controllers or regulators. Figure 9, Figure 10 and Figure 11 show three design examples using the LTC7106 to control the output voltage with a monolithic buck regulator, an µModule® and a boost controller.

APPLICATIONS INFORMATION

Case One

Assume that the LTC7150S, a monolithic buck regulator, provides a 1.5V output and requires to margin low V_{OUT} from 1.5V to 1.0V (see Figure 9). The V_{FB} is 0.6V and the voltage dividers are external. In order to achieve the best accuracy of the LTC7106, it is recommended to design I_{DAC} in nominal range. Also within certain current range (nominal, high or low), the larger the absolute I_{DAC} current amplitude is, the better accuracy the LTC7106 can achieve. So it is easy to choose R_{TOP} = 10kΩ and R_{BOT} = 6.65kΩ. Then I_{DAC} = (1.5V – 1.0V)/10kΩ = + 50µA. Choose MFR_CONTROL [6:5] = 00 (Range = Nominal) to set I_{DAC} LSB =1µA.

By looking in Table 2, choose DAC [6:0] = 0110010 to set the I_{DAC} = +50µA, which will margin V_{OUT} from 1.5V to 1.0V.

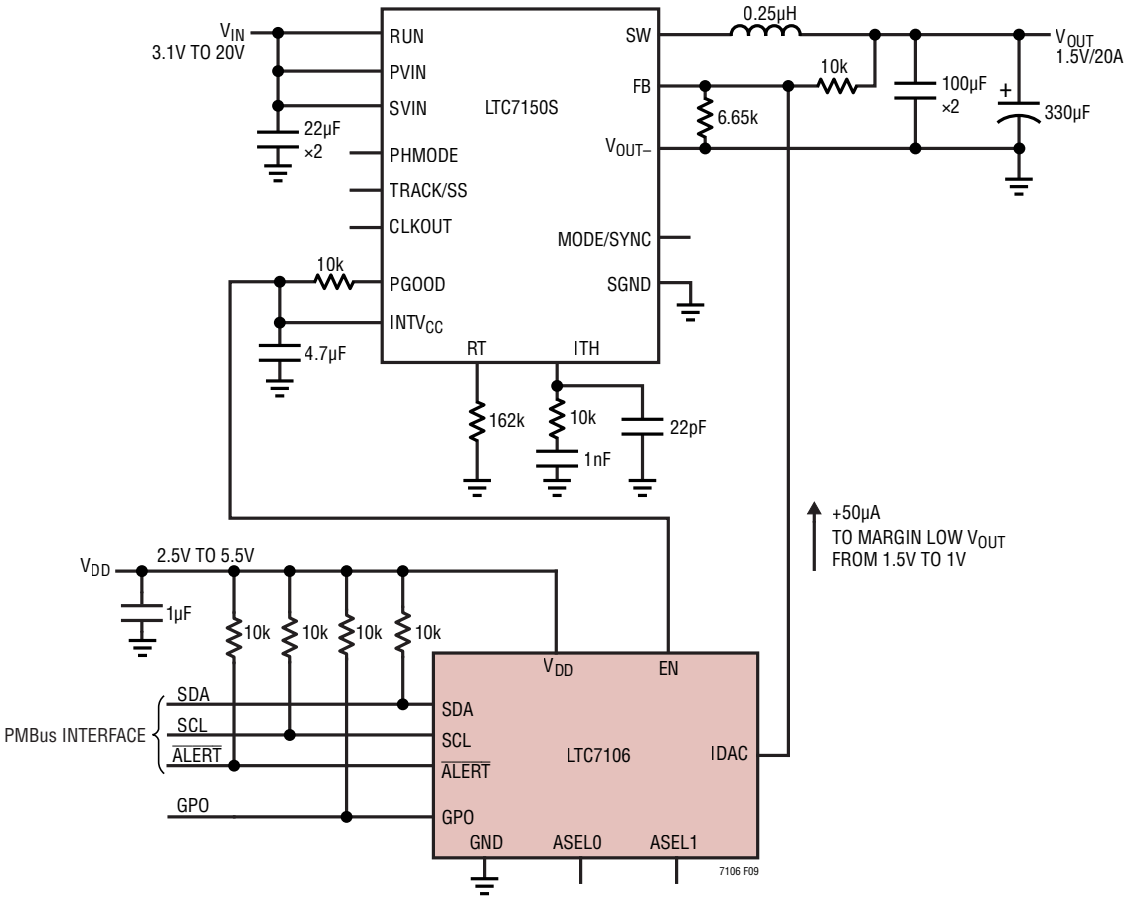


Figure 9. Using the LTC7106 to Margin Low Monolithic Buck Regulator LTC7150S Providing 1.5V to 1.0V at 20A

APPLICATIONS INFORMATION

Case Two

In this case, the µModule LTM4636 provides a 1.2V output and requires to margin high V_{OUT} from 1.2V to 2.0V (see Figure 10). The V_{FB} of the LTM4636 is again 0.6V. However, the top voltage divider is internal (R_{TOP} = 4.99kΩ), so the R_{BOT} is also fixed at 4.99kΩ. Then I_{DAC} = (1.2V – 2.0V)/ 4.99kΩ = –160µA.

So we have to choose MFR_CONTROL [6:5] = 10 (Range = High) to set I_{DAC} LSB = 4µA.

From Table 3, choose DAC[6:0] = 1011000 to set the I_{DAC} = –160µA, which will margin V_{OUT} from 1.2V to 2.0V.

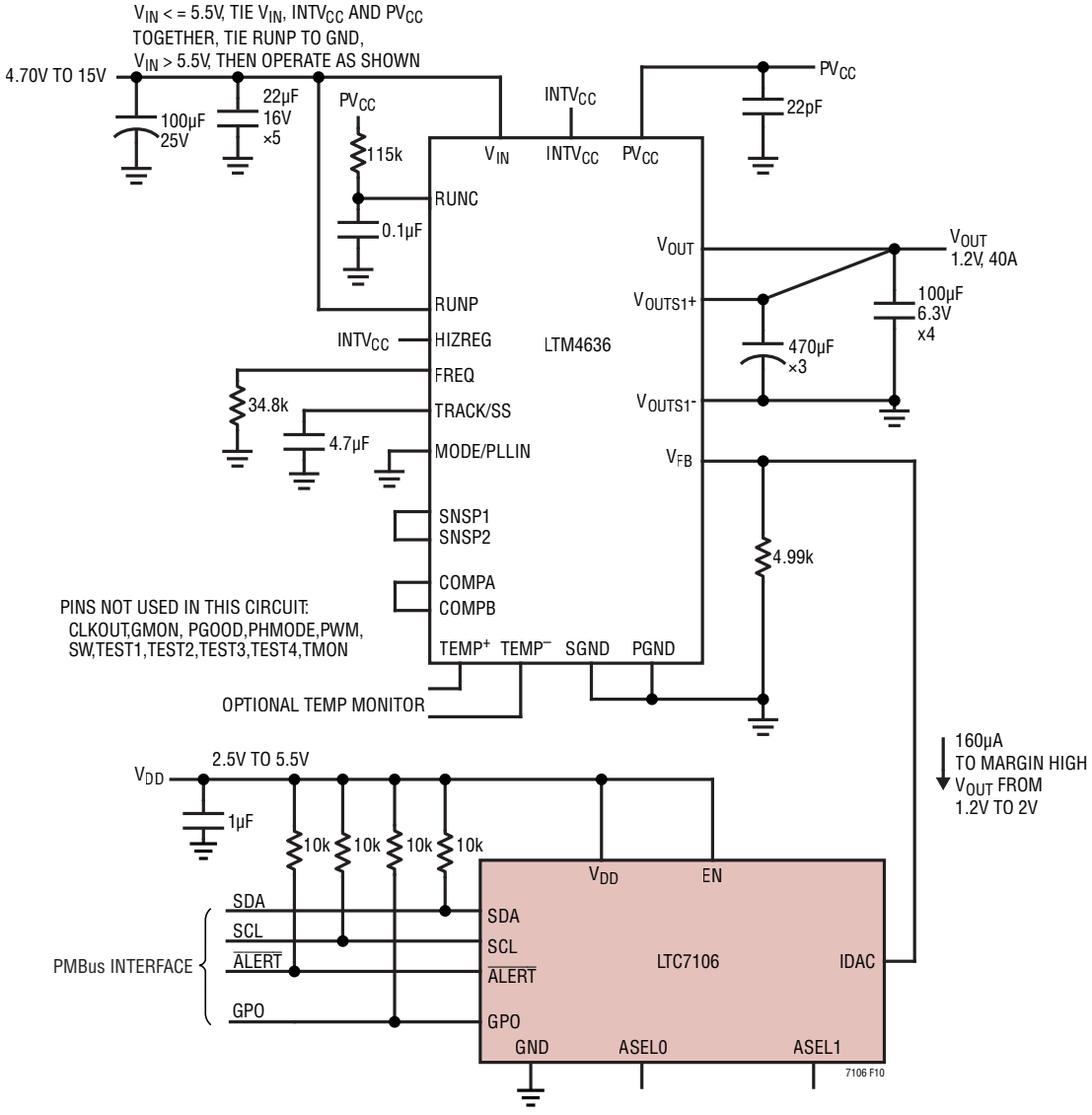


Figure 10. Using the LTC7106 to Margin High µModule LTM4636 Providing 1.2V to 2.0V at 40A

APPLICATIONS INFORMATION

Case Three

The LTC7106 can also work with boost converters. In this case, the LTC3784, a synchronous boost controller, provides a 2-phase 28V/10A output and requires to control V_{OUT} from 28V to 18V (see Figure 11). The VFB is 1.2V and the voltage dividers are external. Based on the same design criteria in Case One, we can choose R_{TOP} = 200kΩ and R_{BOT} = 8.97kΩ for the best accuracy. Then I_{DAC} = (28V – 18V)/200kΩ = +50µA. Choose MFR_CONTROL [6:5] = 00 (Range Nominal) to set I_{DAC} LSB = 1µA. By looking in Table 2, choose DAC[6:0] = 0001110 to set the I_{DAC} = +50µA, which will margin V_{OUT} from 28V to 18V.

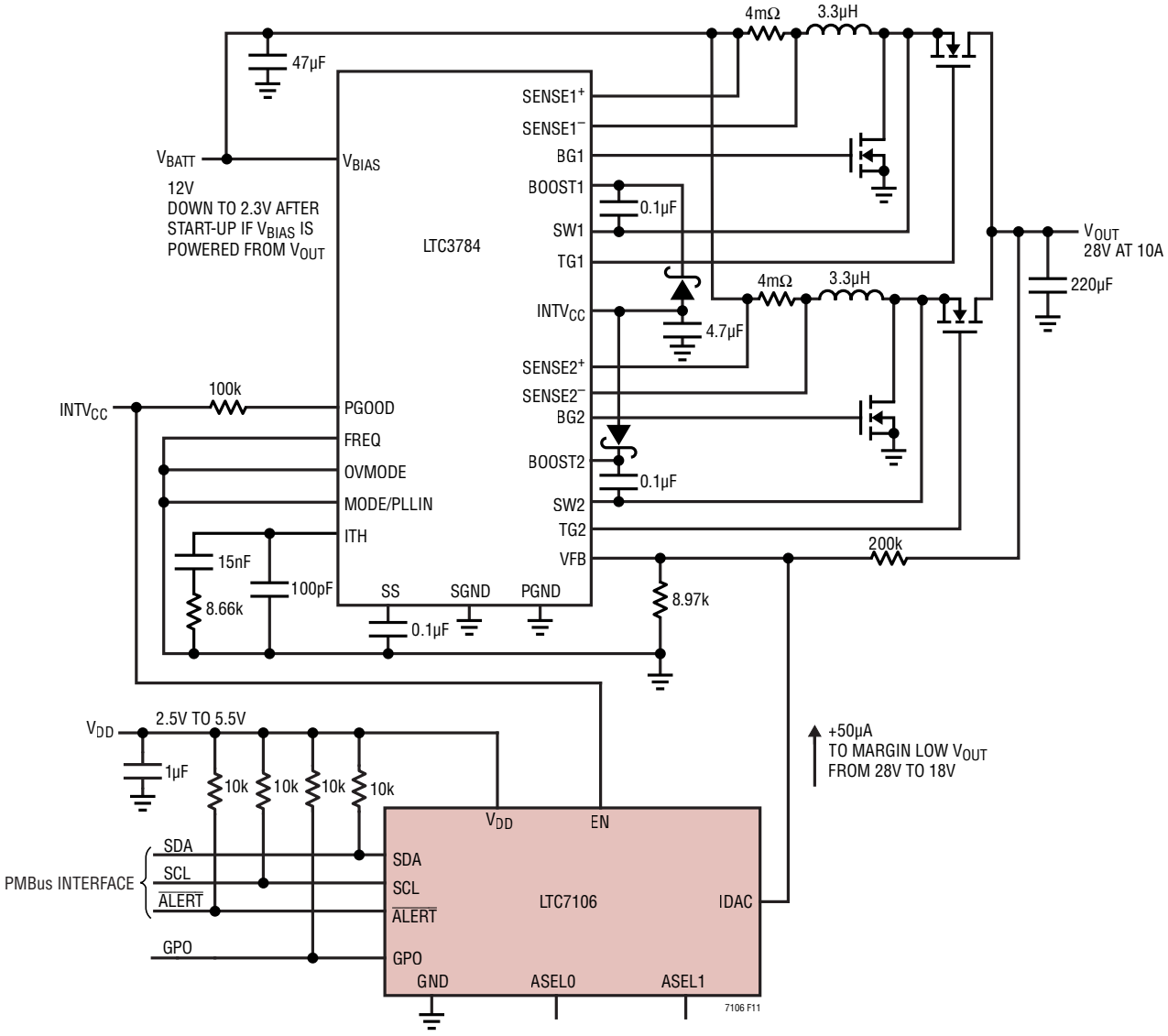
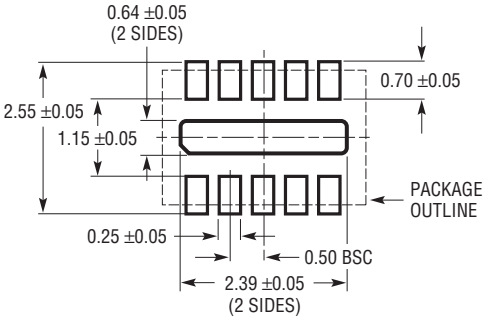


Figure 11. Using the LTC7106 with a Boost Controller to Vary V_{OUT} from 28V to 18V

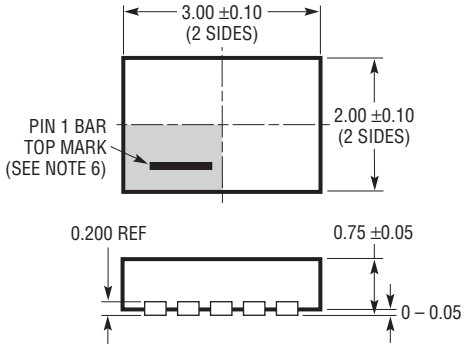
PACKAGE DESCRIPTION

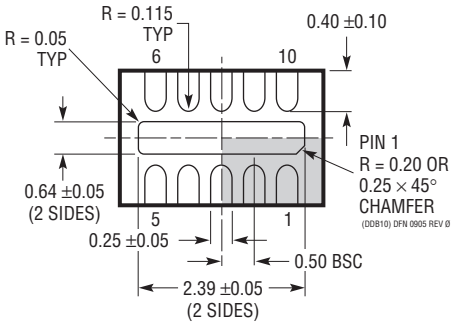
Please refer to http://www.linear.com/product/LTC7106#packaging for the most recent package drawings.

DDB Package
10-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1722 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/18	Clarified MFG_RAIL_ADDRESS and MFG_SPECIAL_ID paragraphs Changed from “Status Word” to “Status Byte”	15 16