Dual Output, 6-Phase, Multiphase Current Mode Synchronous Controller with Current Monitoring

FEATURES

- **Sub-Milliohm DCR Sensing or DrMOS with Current Sense Improves Efficiency**
- **Operates with Power Blocks, DrMOS or External Gate Drivers and MOSFETs**
- **±0.5% Total Output Voltage Accuracy**
- **Flexible Phase Configuration**
- **Dual Output Current Monitoring**
- **$t_{ON(MIN)}$ = 40ns, Capable of Very Low Duty Cycles at High Frequency**
- Dual Differential Remote Sensing Amplifiers
- Programmable Frequency Range of 250kHz to 1.2MHz
- V_{IN} Range Is Not Limited by IC
- V_{CC} Range: 4.5V to 5.5V
- V_{OUT} Range: 0.5V to 2.0V
- 48 Lead (5mm × 6mm) GQFN for LTC7852
- 36 Lead (4mm × 5mm) QFN for LTC7852-1

APPLICATIONS

- Computer Systems
- Telecom and Datacom Systems
- DC Power Distribution Systems

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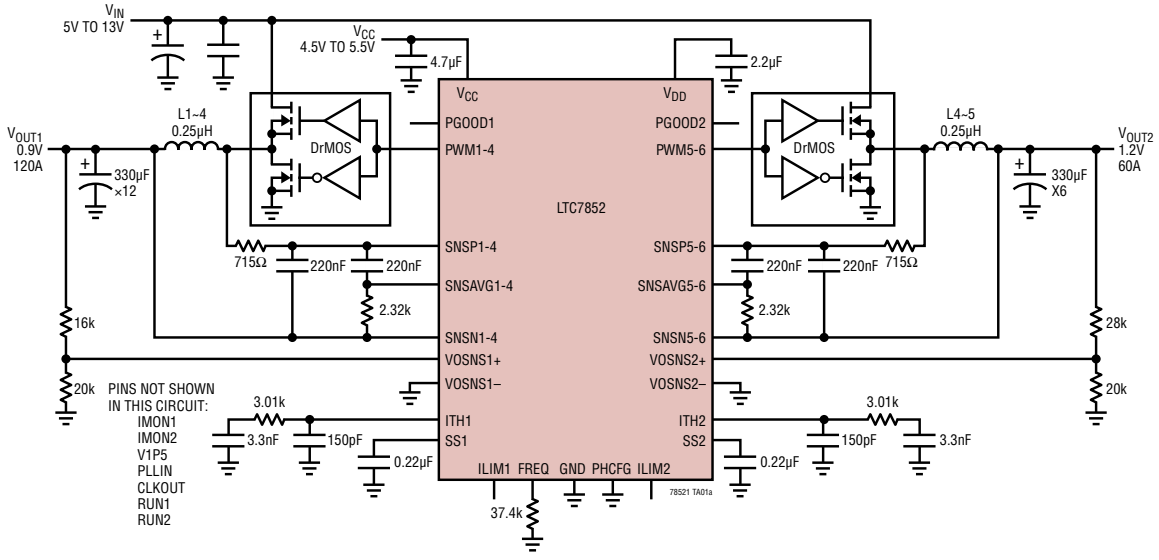
DESCRIPTION

The LTC®7852/LTC7852-1 is a six-phase, dual output current mode synchronous step-down switching regulator controller that works in conjunction with external power train devices such as DrMOS, power blocks or discrete N-channel MOSFETs and associated gate drivers. Its flexible design enables 1-, 2-, 3-, 4-, 5-, and 6-phase configurations. The LTC7852 offers a unique feature that enhances the signal-to-noise ratio of the current sense signal, allowing the use of inductors with very low DC winding resistances for maximum efficiency. The controller achieves a minimum on-time of just 40ns, permitting the use of high switching frequency at high step-down ratios. 8-, 10- or 12 phases with two ICs can be paralleled for very high current requirements up to 400A.

The remote sense differential amplifiers and a precise reference provide accurate output voltages between 0.5V and 2.0V. The input voltage is not limited by the controller. Hiccup mode protection from output shorts or overcurrent minimizes the thermal dissipation.

The LTC7852-1 is designed specifically for DrMOS with an internal current sense signal.

TYPICAL APPLICATION



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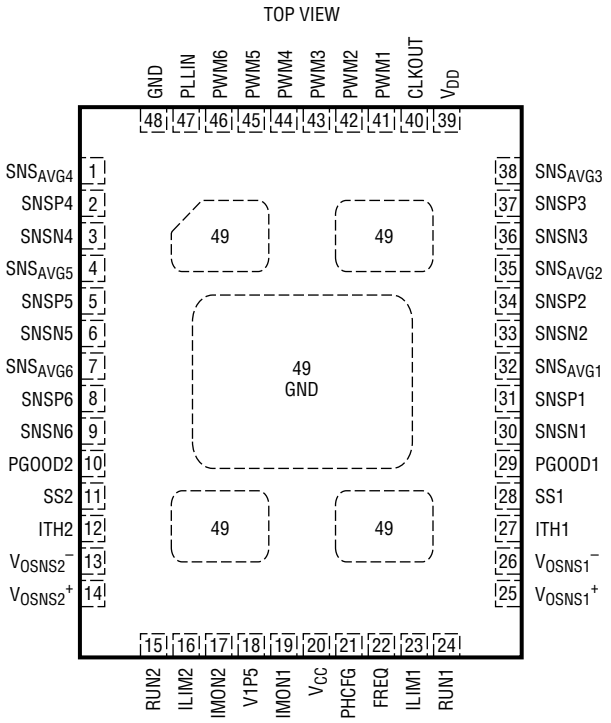
ABSOLUTE MAXIMUM RATINGS (Note 1)

RUN1,2, PGOOD1,2, V_{CC} Voltage ..... –0.3V to 6V
SNSN, SNS_{AVG} (LTC7852 Only),
SNSP .....–0.3V to (V_{CC} + 0.3V)
All Other Pin Voltages .....–0.3V to (V_{CC} + 0.3V)
Operating Junction Temperature Range... –40° to 125°C
Storage Temperature Range ..... –65°C to 150°C

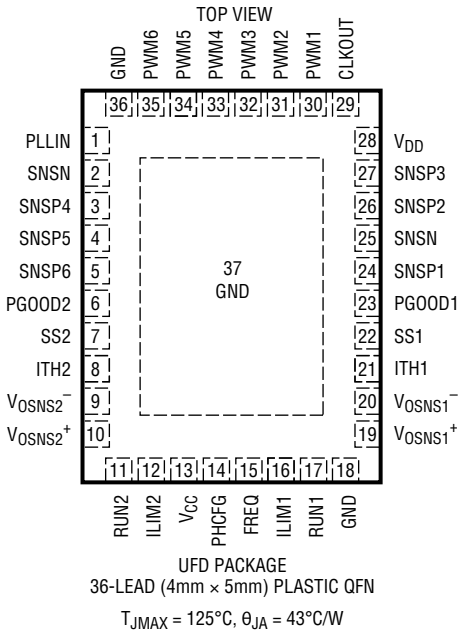
PIN CONFIGURATION

LTC7852



RHE PACKAGE
48-LEAD (5mm × 6mm) PLASTIC GQFN
T_{JMAX} = 125°C, θ_{JA} = 30°C/W

LTC7852-1



UFD PACKAGE
36-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7852ERHE#PBF	LTC7852ERHE#TRPBF	7852	48-LEAD (5mm x 6mm) Plastic GQFN	–40°C to 125°C
LTC7852IRHE#PBF	LTC7852IRHE#TRPBF	7852	48-LEAD (5mm x 6mm) Plastic GQFN	–40°C to 125°C
LTC7852EUFD-1#PBF	LTC7852EUFD-1#TRPBF	78521	36-LEAD (4mm x 5mm) Plastic QFN	–40°C to 125°C
LTC7852IUFD-1#PBF	LTC7852IUFD-1#TRPBF	78521	36-LEAD (4mm x 5mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{RUN} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} Minimum	Bias Supply Input					4.5	V
V_{OUT}	Output Voltage Range	LTC7852 Only (Note 2)	●			2.0	V
V_{OSNS}^+	Regulated Feedback Voltage	ITH = 1.2V (Note 4) –40°C to 125°C 0°C to 85°C	 ● ●	 496 498	 500 500	 504 502	 mV mV
I_{OSNS}^+	Feedback Current					–100	nA
$V_{REFLNREG}$	Reference Voltage Line Reg.	V_{CC} = 4.5V to 5.5V				0.1	%
$V_{LOADREG}$	Output Voltage Load Regulation	ΔI_{TH} = 0.7V to 1.2V ΔI_{TH} = 1.2V to 1.6V	● ●		0.01 0.01	0.1 0.1	% %
$g_{m1,2}$	Transconductance Amplifier g_m	I_{TH} =1.7V, Sink/Source 10µA			2.75		mmho
f_{0dB}	Differential Amplifier Unity-Gain Crossover Frequency	(Note 5)			4		MHz
V_{OVL}	Feedback Overvoltage Lockout	Measured at V_{OSNS}^+	●	5	7.5	10	%
I_Q	Input DC Supply Current Normal Mode Shutdown	 V_{RUN} = 0V			 15 1.2		 mA mA
UVLO	Undervoltage Lockout	V_{VCC} Falling		3.6	4.0	4.3	V
$UVLO_{HYS}$	UVLO Hysteresis				200		mV
I_{SNSAVG}	Sense Pin Bias Currents	V_{SNSAVG} = 1.0V LTC7852 Only	●			±30	nA
I_{SNSP}	Sense Pin Bias Currents	LTC7852 SNSP = 1.0V LTC7852-1 SNSP = 1.5V	●			±50	nA
I_{SS}	Soft-Start Charge Current	V_{SS} = 0V		–4.5	–5	–5.5	µA
V_{SNSN}	Sense Pin Bias Voltage	–3mA < I_{SNSN} < 3mA LTC7852-1 Only			1.5		V
A_{VT_SNS}	Total Sense Signal Gain to Current Comparator	LTC7852 Only			5		V/V
V_{RUN}	RUN Pin ON Threshold	V_{RUN} Rising	●	1.1	1.22	1.34	V
V_{RUN_HYS}	RUN Pin ON Hysteresis				140		mV
I_{RUN}	RUN Pin Pull-Up Current RUN < ON Threshold RUN > ON Threshold	 RUN < 1.1V RUN > 1.34V			 –1.3 –7.7		 µA µA
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	LTC7852 I_{TH} = 2.2V, V_{SNSN} =1.0V V_{SNSAVG} = V_{SNSN} I_{LIM} = 0V I_{LIM} = 1/4V_{CC} I_{LIM} = Float I_{LIM} = 3/4V_{CC} I_{LIM} = V_{CC}	 ● ● ● ● ●	 9 14 19 24 28.5	 10 15 20 25 30	 11 16 21 26 31.5	 mV mV mV mV mV
		LTC7852-1 I_{TH} = 2.2V I_{LIM} = 0V I_{LIM} = 1/4Vcc I_{LIM} = Float I_{LIM} = 3/4V_{CC} I_{LIM} = V_{CC}	 ● ● ● ● ●	 45 70 95 120 142.5	 50 75 100 125 150	 55 80 105 130 157.5	 mV mV mV mV mV
$V_{ØMIS}$ Standard Deviation of	Phase to Phase Current Sensed Voltage Mismatching	I_{LIM} = Float, PHCFG = Float I_{TH} = 2.2V			0.5		mV
$t_{ON(MIN)}$	Minimum On-Time	(Note 6)			40		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{RUN} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Good							
$V_{PGOOD(ON)}$	PGOOD Pull Down Resistance					200	Ω
$I_{PGOOD(OFF)}$	PGOOD Leakage Current	V_{PGOOD} = 5V				2	µA
t_{PGOOD}	V_{PGOOD} High to Low Delay				45		µs
V_{PGD}	PGOOD Trip Level	V_{FB} with Respect to Set Output Voltage V_{FB} Ramping Up V_{FB} Ramping Down		 5 –5	 7.5 –7.5	 10 –10	 % %
$V_{PG1(HYST)}$	PGOOD Trip Level Hysteresis				15		mV
Oscillator and Phase-Locked Loop							
f_{OSC}	Oscillator Frequency	R_{FREQ} = 30.1kΩ R_{FREQ} = 47.5kΩ R_{FREQ} = 54.9kΩ R_{FREQ} = 75.0kΩ		215 550 675 0.875	250 600 750 1.05	285 650 825 1.225	kHz kHz kHz MHz
	Sync. Freq. Range		●	0.25		1.2	MHz
I_{FREQ}	FREQ Pin Output Current	V_{FREQ} = 0.8V		–18.5	20	–21.5	µA
R_{PLLIN}	PLLIN Input Resistance				200		kΩ
V_{PLLIN}	PLLIN Input Threshold	V_{PLLIN} Rising V_{PLLIN} Falling			2 1.2		V V
V_{CLKOUT}	Low Output Voltage High Output Voltage	I_{LOAD} = 500µA I_{LOAD} = –500µA			0.2 5		V V
V_{DD} Output							
V_{DD}	Internal V_{DD} Voltage				3.3		V
PWM Outputs							
PWM	PWM Output High Voltage	I_{LOAD} = –500µA	●	3.1	3.3	3.5	V
	PWM Output Low Voltage	I_{LOAD} = 500µA	●			0.5	V
	PWM Output Current in Hi-Z State	PWM = 0V PWM = 3.3V				–1 1	µA µA
IMON Outputs (LTC7852 Only)							
V1P5	1.5V Regulator Output Voltage	V_{SNS} = 0, –3mA < I_{V1P5} < 3mA	●	1.4	1.5	1.6	V
IMON	IMON Output Voltage	V_{SNS} = V_{SNSMAX}, I_{LIM} = Float	●	V1P5 +142.5	V1P5 +150	V1P5 +157.5	mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7852/LTC7852-1 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7852E/LTC7852-1E is guaranteed to meet performance specifications from 0°C to 85°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7852I/LTC7852-1I is guaranteed to meet performance specifications over the full –40°C to 125°C operating junction temperature range. The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the package thermal impedance and other environmental factors.

T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the following formula:

LTC7852RHE: $T_J = T_A + (P_D \bullet 30°C/W)$
LTC7852UFD-1: $T_J = T_A + (P_D \bullet 43°C/W)$

Note 3: Output voltage range of LTC7852-1 is determined by the DrMOS.

Note 4: The LTC7852/LTC7852-1 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}.

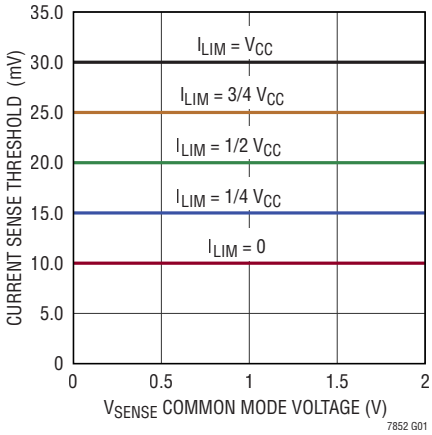
Note 5: Guaranteed by design.

Note 6: The minimum on-time condition is specified for an inductor peak-to-peak ripple current >40% of I_{MAX} (See Minimum On-Time Considerations in the Applications Information section).

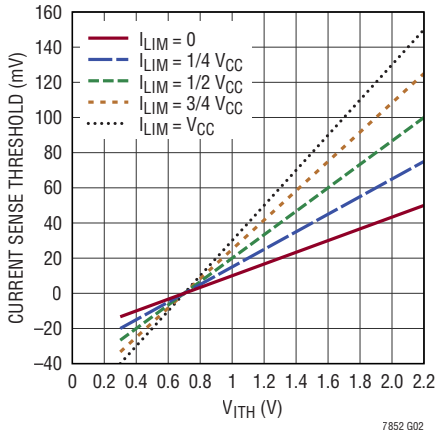
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V unless otherwise noted.

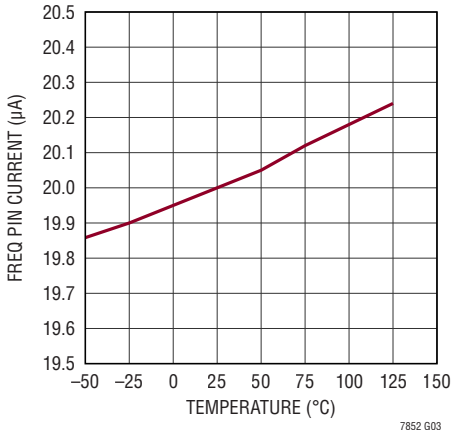
Maximum Current Sense Threshold vs Common Mode Voltage



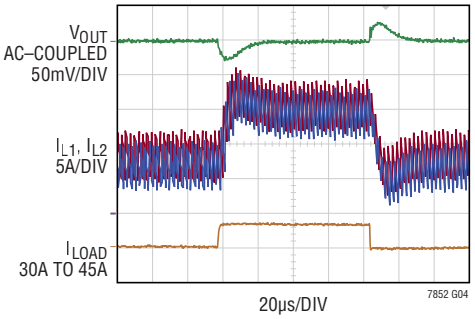
Current Sense Threshold vs I_{TH} Voltage



FREQ Pin Source Current vs Temperature

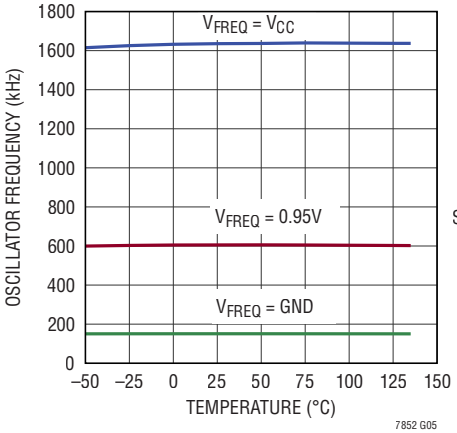


Load Step

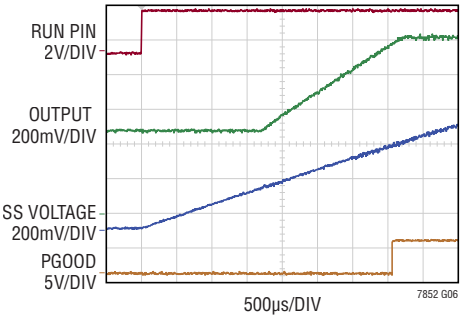


V_{IN} = 12V
V_{OUT} = 1V
f_{SW} = 400kHz
L = 0.25µH

Oscillator Frequency vs Temperature



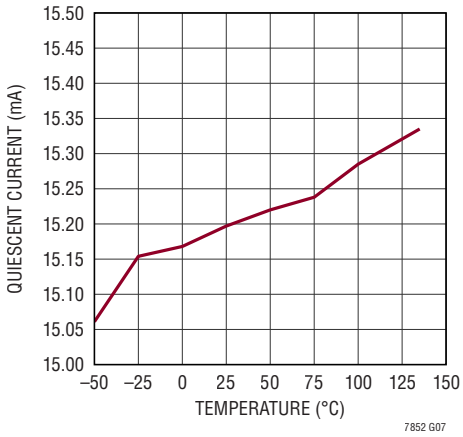
Prebias Startup at 0.5V



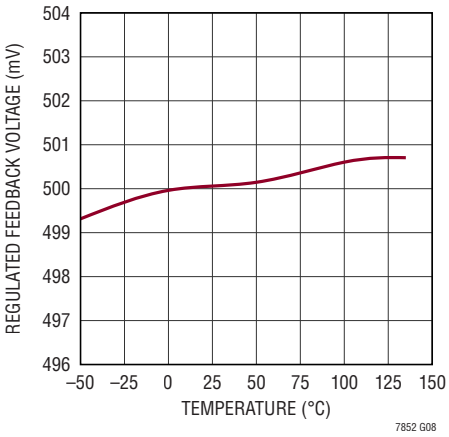
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V unless otherwise noted.

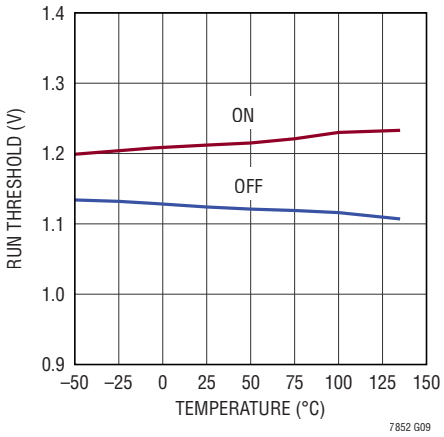
Quiescent Current vs Temperature



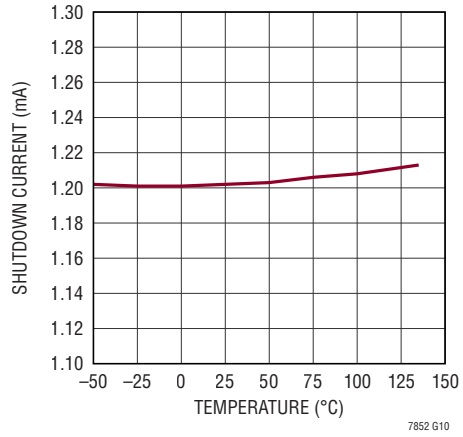
Regulated Feedback Voltage vs Temperature



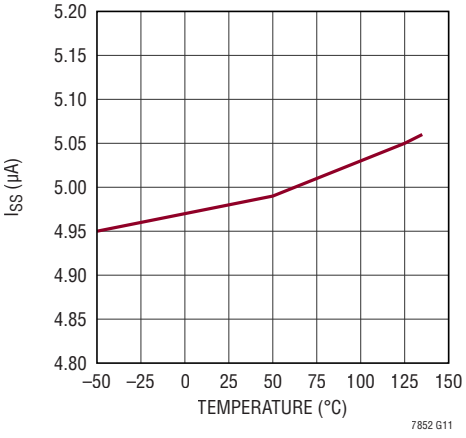
RUN Threshold vs Temperature



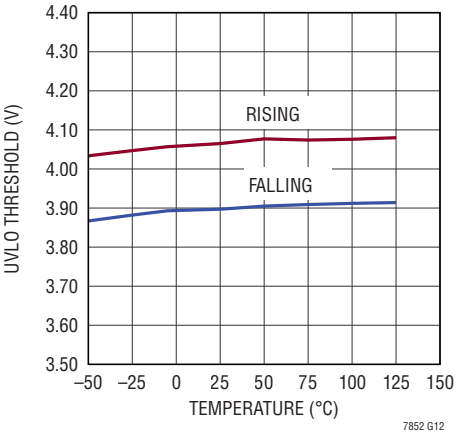
Shutdown Current vs Temperature



SS Pull-Up Current vs Temperature



Undervoltage Lockout Threshold (V_{CC}) vs Temperature



PIN FUNCTIONS (GQFN/QFN, LTC7852/LTC7852-1)

V1P5 (Pin 18, LTC7852 Only): Internally Generated 1.5V Voltage Regulator Output Pin. Bypass this pin to SGND with a low ESR 2.2µF capacitor.

IMON1, IMON2 (Pins 19, 17, LTC7852 Only): Output Current Monitors. The differential voltage between each IMON pin and the V1P5 pin provides a linear indication of output current from the corresponding channel.

V_{CC} (Pin 20/Pin 13): External 5V Input. The control circuits are powered from this voltage. Bypass this pin to GND with a capacitor (0.1µF to 1µF ceramic) in close proximity to the chip.

PHCFG (Pin 21/Pin 14): Phase Configuration Pin. This pin selects the phases powering output 1 and output 2.

FREQ (Pin 22/Pin 15): Frequency Set/Select Pin. A resistor between this pin and SGND sets the switching frequency. This pin sources 20µA.

ILIM1, ILIM2 (Pins 23, 16/Pins 16, 12): Current Comparator Sense Voltage Limit Selection Pin.

RUN1, RUN2 (Pins 24, 15/Pins 17, 11): Enable Control Inputs. A voltage above 1.22V turns on the IC. There is a 1µA pull-up current on this pin. Once the RUN pin rises above the 1.22V threshold, the pull-up increases to 7.7µA.

V_{OSNS1}^+, V_{OSNS2}^+ (Pins 25, 14/Pins 19, 10): Remote Sense Differential Amplifier Non-Inverting inputs. Connect to feedback divider center tap with the divider across the output load. The remote sense differential amplifier's output is internally connected to the error amplifier's inverting input.

V_{OSNS1}^-, V_{OSNS2}^- (Pins 26, 13/Pins 20, 9): Remote Sense Differential Amplifier Inverting Inputs. Connect to sense ground at the output load.

ITH1, ITH2 (Pins 27, 12/Pins 21, 8): Current Control Thresholds and Error Amplifier Compensation Points. The current comparator's threshold increases with the ITH control voltage.

SS1, SS2 (Pins 28, 11/Pins 22, 7): Soft-Start Inputs. The voltage ramp rate at this pin sets the voltage ramp rate of the output. A capacitor to ground programs soft-start. This pin has a 5µA pull-up current. The minimum required soft-start capacitor is 22nF.

PGOOD1, PGOOD2 (Pins 29, 10/Pins 23, 6): Power Good Indicator Outputs. Open drain output that pulls to ground when output voltage is not in regulation.

SNSN1, SNSN2, SNSN3, SNSN4, SNSN5, SNSN6 (Pins 30, 33, 36, 3, 6, 9, LTC7852 Only): Second Negative Current Sense Comparator Inputs. This input senses the signal from the output inductor's DCR with a filter bandwidth of five times the inductor's L/DCR value when low DCR current sensing is enabled.

SNSP1, SNSP2, SNSP3, SNSP4, SNSP5, SNSP6 (Pins 31, 34, 37, 2, 5, 8 /Pins 24, 26, 27, 3, 4, 5): Positive Current Sense Comparator Inputs.

SNS_{AVG1}, SNS_{AVG2}, SNS_{AVG3}, SNS_{AVG4}, SNS_{AVG5}, SNS_{AVG6} (Pins 32, 35, 38, 1, 4, 7, LTC7852 Only): First Negative Current Sense Comparator Inputs. This input senses the signal from the output inductor's DCR with a filter which has a bandwidth at 3/5 of the inductor's L/DCR value. Tie to V_{CC} for DCR sensing with DCR >1mΩ or DrMOS current sensing.

SNSN (Pins 2, 25, LTC7852-1 Only): Internal 1.5V Voltage Regulator Output.

V_{DD} (Pin 39/Pin 28): Internally Generated 3.3V Power Supply Output Pin. Bypass this pin to SGND with a low ESR 2.2µF capacitor. Do not load this pin with external current. PWM output HIGH voltage equals to V_{DD} voltage. If a PWM HIGH voltage between 3.3V and V_{CC} voltage is desirable, it is allowed to bias this pin with external source at the desirable voltage.

CLKOUT (Pin 40/Pin 29): Clock Output Pin.

PWM1, PWM2, PWM3, PMW4, PWM5, PWM6 (Pins 41, 42, 43, 44, 45, 46/Pins 30, 31, 32, 33, 34, 35): (Top) Gate Signal Outputs. This signal goes to the PWM or top gate input of the external gate driver or integrated driver MOSFET or Power Block. This is a three-state compatible output. PWM output HIGH voltage equals to Vdd pin voltage.

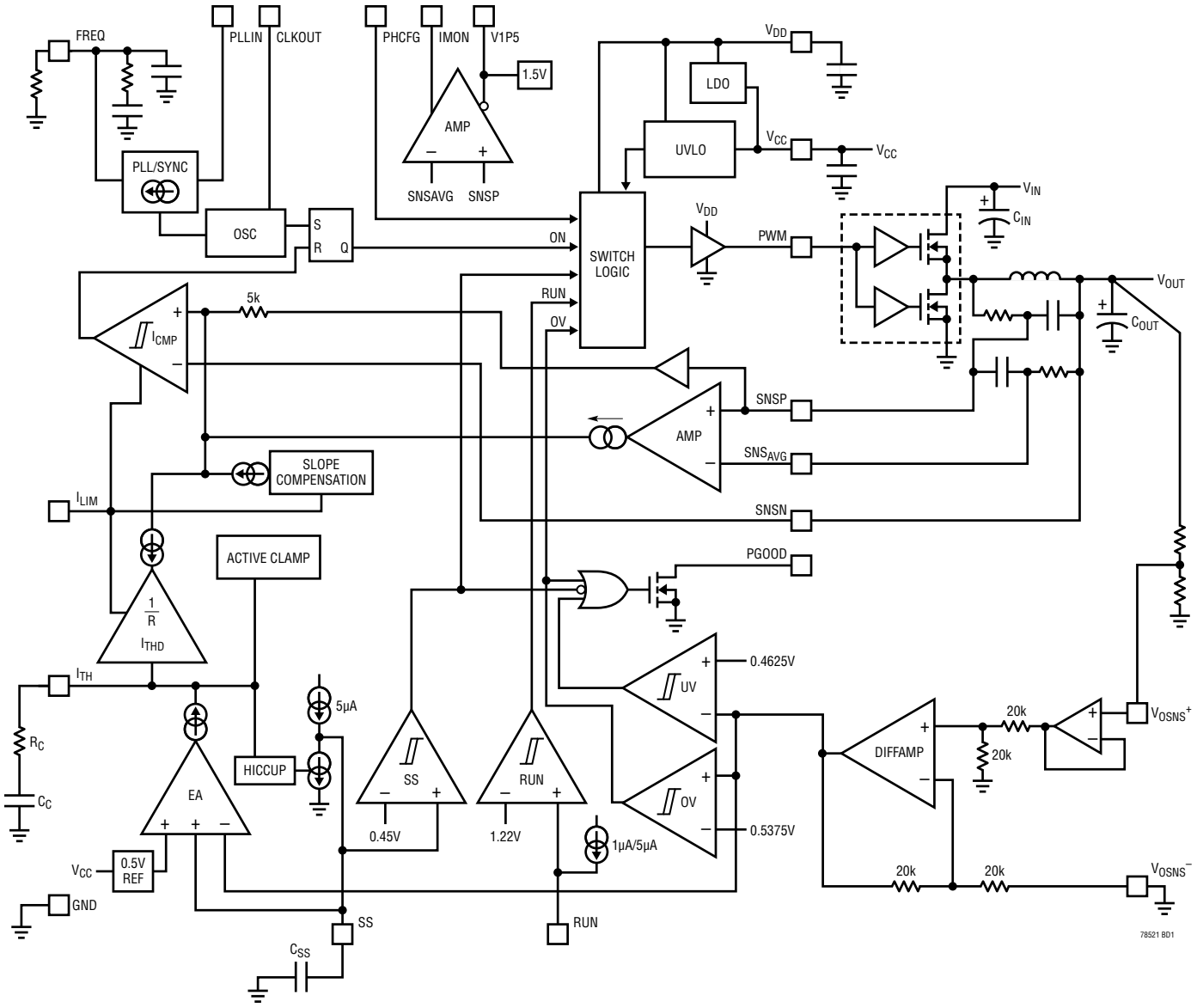
PLLIN (Pin 47/Pin 1): External Synchronization Input to Phase Detector Pin. A clock on the pin will synchronize the internal oscillator with the clock on this pin. The PLL compensation network is integrated into the IC.

GND (Pin 48/Pin 36): Ground. All small-signal components and compensation components should be connected here. The exposed pad must be soldered to the PCB for rated thermal performance.

Exposed pad (Pin 49/Pin 37): Ground.

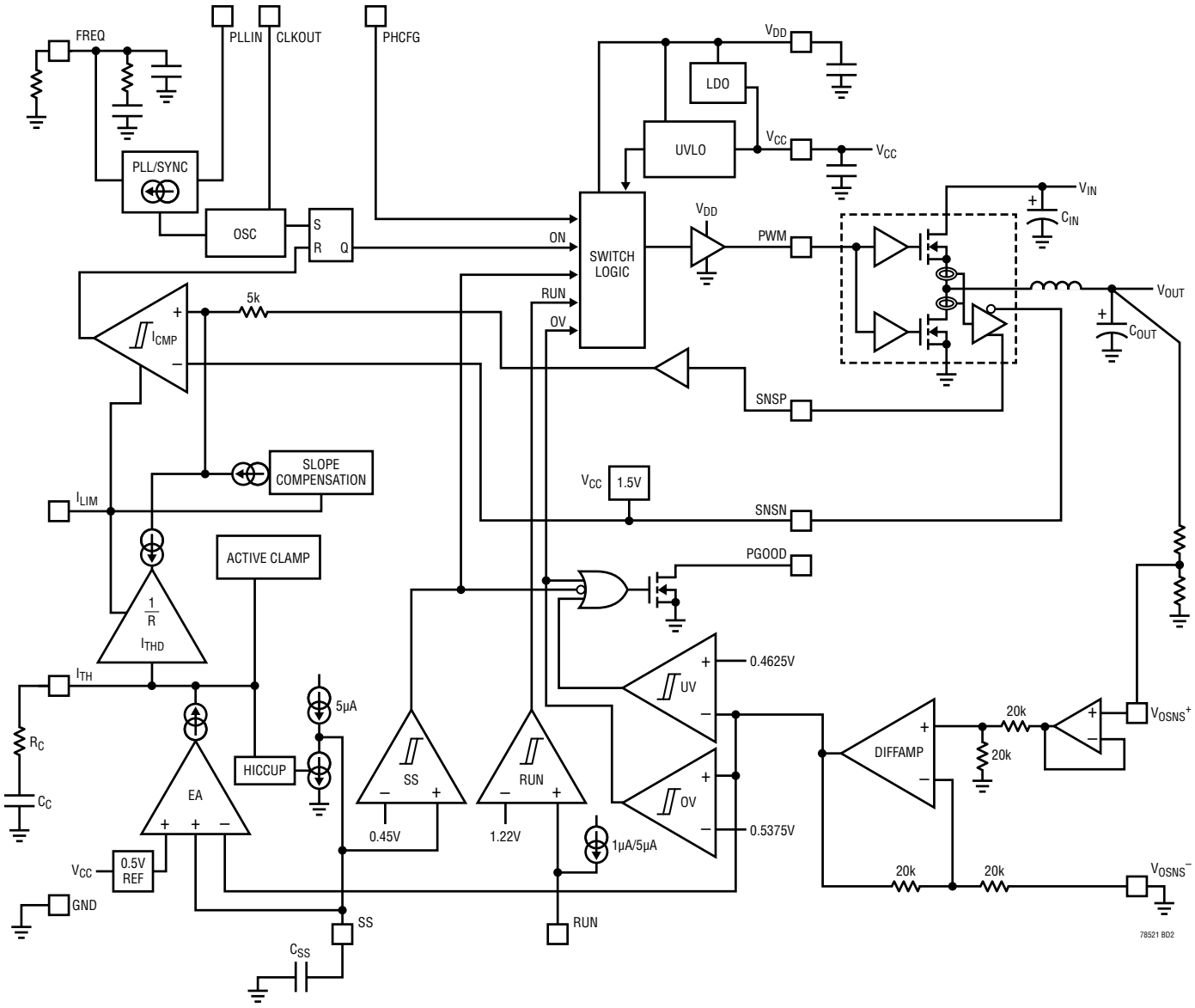
FUNCTIONAL BLOCK DIAGRAMS

LTC7852



FUNCTIONAL BLOCK DIAGRAMS

LTC7852-1



OPERATION

Main Control Loop

The LTC7852/LTC7852-1 uses an LTC proprietary current sensing, current mode step-down architecture. During normal operation, the top MOSFET is turned on every cycle when the oscillator sets the RS latch, and turned off when the main current comparator, I_{CMP}, resets the RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier, EA. The remote sense amplifier (diffamp) produces a signal equal to the differential voltage sensed across the output capacitor divided down by the feedback divider and re-references it to the local IC ground. The error amplifier receives this feedback signal and compares it to the internal 0.5V reference. When the load current increases, it causes a slight decrease in the V_{OSNS}^+ pin voltage relative to the 0.5V reference, which in turn causes the ITH voltage to increase until the inductor's average current equals the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on until the beginning of the next cycle. The inductor current is allowed to reverse at light loads or under large transient conditions.

The main control loop is shut down by pulling the RUN pin low. Releasing RUN allows an internal 1.3µA current source to pull up the RUN pin. When the RUN pin reaches 1.22V, the main control loop is enabled and the IC is powered up. When the RUN pin is low, all functions are kept in a controlled state.

Sensing Signal of Very Low DCR (LTC7852)

The LTC7852 employs a unique architecture to enhance the signal-to-noise ratio, enabling it to operate with a small sense signal of a very low value inductor DCR, 1mΩ or less. This improves power efficiency, and reduces jitter due to the switching noise which could corrupt the signal. The LTC7852 can sense a DCR value as low as 0.2mΩ with careful PCB layout. Each phase has two negative sense pins, SNSN and SNS_{AVG}, which share the positive sense pin SNSP. These sense pins acquire signals and internally processes them for a 14dB signal-to-noise ratio improvement. In the meantime, the current limit threshold is still a function of the inductor peak current and its DCR value, and can be accurately set from 10mV to 30mV in 5mV steps with the ILIM pin. The filter across the inductor should have a time constant R1 • C1 equal to 1/5 of the time constant of the output inductor L/DCR. The filter at SNS_{AVG} should have a bandwidth of three times larger than SNSP R1 • C1.

Driver MOSFET (DrMOS) Current Sensing (LTC7852-1)

The LTC7852-1 is dedicated for converters using DrMOS current sensing. The SNSN pins are connected to an internal 1.5V voltage regulator with current sinking and sourcing capability. It serves as a common mode bias for all the DrMOSs' current sensing differential signals.

Shutdown and Start-Up (RUN and SS Pins)

The LTC7852/LTC7852-1 can be shut down using the RUN pin. Pulling the RUN pin below 1.14V shuts down the main control loop for the controller and most internal circuits. Releasing the RUN pin allows an internal 1.3µA current to pull up the pin and enable the controller. Alternatively, the RUN pin may be externally pulled up or driven directly by logic. Be careful not to exceed the absolute maximum rating of 6V on this pin. The start-up of the controller's output voltage, V_{OUT}, is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 0.5V internal reference, the LTC7852/LTC7852-1 regulates the V_{OSNS}^+ voltage to the SS pin voltage instead of the 0.5V reference. This allows the SS pin to be used to program a soft-start by connecting an external capacitor from the SS pin to GND. The minimum required SS capacitor is 22nF. An internal 5µA pull-up current charges this capacitor, creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 0.5V (and beyond), the output voltage, V_{OUT}, rises smoothly from its pre-biased value to its final set value. Certain applications can result in the start-up of the converter into a non-zero load voltage, where residual charge is stored on the output capacitor at the onset of converter switching. In order to prevent the output from discharging under these conditions, the bottom MOSFET is disabled until soft-start is greater than V_{OSNS}^+.

OPERATION

When the RUN pin is pulled low to disable the controller, or when V_{CC} drops below its undervoltage lockout threshold of 4.0V, the SS pin is pulled low by an internal MOSFET. When in undervoltage lockout, the controller is disabled and the external MOSFETs are held off.

Frequency Selection and Phase-Locked Loop (FREQ and PLLIN Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. If the PLLIN pin is not being driven by an external clock source, the FREQ pin can be used to program the controller's operating frequency from 250kHz to 1.2MHz. There is a precision 20µA current flowing out of the FREQ pin so that the user can program the controller's switching frequency with a single resistor to GND. A curve is provided in the Applications Information section showing the relationship between the voltage on the FREQ pin and switching frequency. A phase-locked loop (PLL) is available on the LTC7852/LTC7852-1 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN pin. The PLL loop filter network is integrated inside the LTC7852/LTC7852-1. The phase-locked loop is capable of locking to any frequency within the range of 250kHz to 1.2MHz. The frequency setting resistor should always be present to set the controller's initial switching frequency before locking to the external clock.

Multiphase Operation

LTC7852/LTC7852-1 provides flexible phase configurations for dual high current outputs. When PHCFG is either grounded, floated or tied to $INTV_{CC}$, the controller is in 4+2 mode, 3+3 mode and 5+1 mode, respectively. In order to minimize the input and output voltage ripple and increase the power conversion efficiency, the multi-phase PWM signals are evenly interleaved. Table 1 shows the detailed information. A 6-phase single output converter can be configured by floating the PHCFG pin, while externally connecting the ITHs, V_{OSNS}^+s, V_{OSNS}^-s, RUNs, I_{LIM}s and SS pins, respectively.

Multichip Operation

For output loads that demand high current, multiple LTC7852/LTC7852-1s can be daisy chained to run out of phase to provide more output current without increasing input and output voltage ripple. The ITH, V_{OSNS}^+, V_{OSNS}^-, I_{LIM} and SS pins of one phase should be tied to the corresponding pins of the other phases.

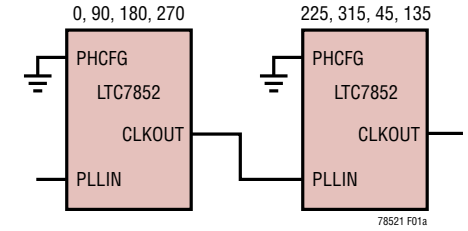
The PLLIN pin allows the LTC7852/LTC7852-1 to synchronize to the CLKOUT signal of another LTC7852/LTC7852-1, or other external clock source. For the LTC7852/LTC7852-1 synchronized to PLLIN clock signal, the rising edge of PWM1 is lined up with the rising edge of the PLLIN clock. The CLKOUT signal can be connected to the PLLIN pin of the following LTC7852/LTC7852-1 stage to line up both the frequency and the phase of the entire system. In 3+3 mode, the phase difference between PH1 and CLKOUT is 90°. In this mode, a total of 12 phases can be daisy chained to run simultaneously out-of-phase with respect to each other. In 4+2 mode, the phase difference between PH1 and CLKOUT is 225°. With two ICs in this mode, an 8 phase interleaving power stage could be configured. In 5+1 mode, difference between PH1 and CLKOUT is 252°. With two ICs in this mode a 10 phase interleaving power stage could be configured.

Table 1.

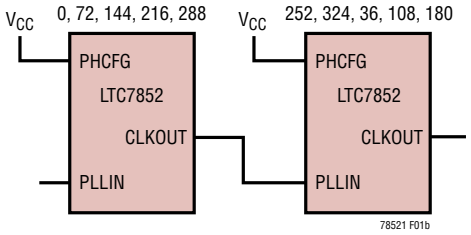
	OUTPUT 1			OUTPUT 2			
3+3 Mode	0°	120°	240°	60°	180°	300°	90°
4+2 Mode	0°	90°	180°	270°	45°	225°	225°
5+1 Mode	0°	72°	144°	216°	288°	252°	252°
6 Phase Mode	0°	120°	240°	60°	180°	300°	90°
	PH1	PH2	PH3	PH4	PH5	PH6	CLKOUT

Figure 1 shows the connections necessary for 8-, 10- or 12-phase operation.

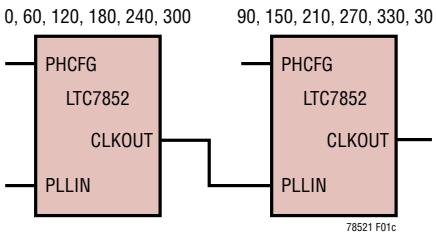
OPERATION



(a) 8-Phase Configuration



(b) 10-Phase Configuration



(c) 12-Phase Configuration

Figure 1. Phase Operations

Sensing the Output Voltage with a Differential Amplifier

The LTC7852/LTC7852-1 includes two low offset, high input impedance, unity-gain, high bandwidth differential amplifiers for applications that require true remote sensing. Sensing the load across the load capacitors directly benefits regulation in high current, low voltage applications, where board interconnection losses can be a significant portion of the total error budget. Connect V_{OSNS}^+ to the center tap of the feedback divider across the output load, and V_{OSNS}^- to the load ground. See Figure 2. The LTC7852/LTC7852-1 differential amplifier is configured for unity gain, meaning that the difference between V_{OSNS}^+ and V_{OSNS}^- is translated to its output, relative to GND. The differential amplifier's output is internally connected to the error amplifier inverting input. Care should be taken to route the V_{OSNS}^+ and V_{OSNS}^- PCB traces parallel to each other all the way to the remote sensing points on the board. In addition, avoid routing these sensitive traces near any high speed switching nodes in the circuit. Ideally, the V_{OSNS}^+ and V_{OSNS}^- traces should be shielded by a low impedance ground plane to maintain signal integrity.

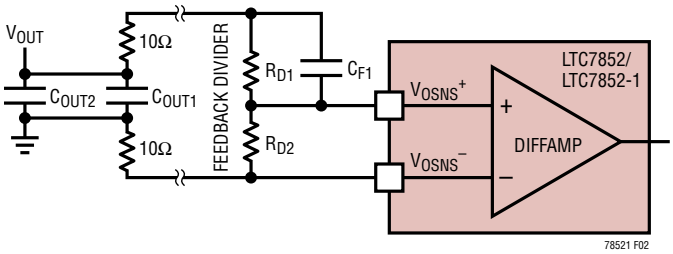


Figure 2. Differential Amplifier Connection

Power Good (PGOOD Pin)

The PGOOD pin is connected to the open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the V_{OSNS}^+ pin voltage is not within ±10% of the 0.5V reference voltage. The PGOOD pin is also pulled low when the RUN pin is below 1.14V or when the LTC7852/LTC7852-1 is in the soft-start phase. When the V_{OSNS}^+ pin voltage is within the ±5% regulation window, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source of up to 6V. The PGOOD pin will flag power good immediately when the V_{OSNS}^+ pin is within the regulation window. However, there is an internal 45µs power-bad mask delay when the V_{OSNS}^+ goes out of the window.

There is an independent PGOOD pin for each channel. For single output configuration, the two PGOOD pins can be tied together.

OPERATION

Output Overvoltage Protection

An overvoltage comparator, OV, guards against transient overshoots (>10%) as well as other more serious conditions that may overvoltage the output. In such cases, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Undervoltage Lockout

The LTC7852/LTC7852-1 has two functions that help protect the controller in case of undervoltage conditions. A precision UVLO comparator constantly monitors the V_{CC} voltage to ensure that an adequate PWM voltage is present. It locks out the switching action when V_{CC} is below 4.0V during ramping up. To prevent oscillation when there is a disturbance on the V_{CC}, the UVLO comparator has 200mV of precision hysteresis.

The RUN pin can be configured to detect an undervoltage condition of the power stage input voltage as needed. Because the RUN pin has a precision turn-on reference of 1.22V, one can use a resistor divider across the input voltage to turn on the IC when input voltage is high enough. An extra 4µA of current flows out of the RUN pin once the RUN pin voltage passes 1.22V. The RUN comparator itself has about 80mV of hysteresis. One can program additional hysteresis for the RUN comparator by adjusting the values of the resistive divider. Always set the power stage input voltage undervoltage detection threshold higher than the controller UVLO threshold so that the LTC7852/LTC7852-1 is enabled after the power stage.

Load Current Monitoring

The LTC7852's I_{MON} pins outputs a voltage proportional to the load current of the corresponding channel. I_{MON} is referred to the regulated 1.5V common mode voltage at the V1P5 pin. A decoupling capacitor might be placed between I_{MON} and V1P5 for noise decoupling. Please note that the I_{MON} pin is not a low impedance signal source. Minimize the leakage current of circuitry connecting to this pin for best accuracy. The linear transfer function from load current to the I_{MON} signal is:

$$V_{IMON} = 150mV/V_{ILIM} \bullet \Sigma(V_{SNSAVG})/N_{PH}$$

where:

N_{PH}: number of paralleled phases

V_{ILIM}: maximum sense voltage of the selected ILIM level

V_{SNSAVG}: differential sense voltage between SNSP and SNS_{AVG} of each phase

For a 6-phase single output converter, tie the I_{MON1} and I_{MON2} together; this signal represents the total current of six phases.

APPLICATIONS INFORMATION

The Typical Application on the first page of this data sheet is a basic LTC7852 application circuit. The LTC7852 is designed and optimized for use with a very low DCR value by utilizing a novel approach to reduce the noise sensitivity of the sensing signal by a factor of 14dB. DCR sensing is popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, as the DCR value drops below 1mΩ, the signal-to-noise ratio is low and current sensing is difficult. LTC7852 uses an LTC proprietary technique to solve this issue. In general, external component selection is driven by the load requirement, and begins with the DCR and inductor value. Next, power MOSFETs are selected. Finally, input and output capacitors are selected.

LTC7852-1 is designed for use with DrMOS with a current sensing signal. With DrMOS current sensing, the inductor DCR value does not impact the current sensing/current sharing accuracy, and the maximum current limit could be continuously programmed by external sensing circuitry.

Current Limit Programming

The ILIM pin is a 5-level logic input which sets the maximum current limit of the controller. When ILIM is either grounded, floated or tied to V_{CC}, the typical value for the maximum current sense threshold will be 10mV, 20mV or 30mV, respectively. Set ILIM to one-fourth V_{CC} or three-fourths V_{CC} for maximum current sense thresholds of 15mV and 25mV respectively. Please note that the ILIM pin has an internal 500k pull-down to GND and a 500k pull-up to V_{CC}. For the best current limit accuracy, use the highest setting that is applicable to the output requirements.

SNSP, SNSN and SNS_{AVG} (LTC7852 only) Pins

The SNSP and SNSN pins are the inputs to the current comparators, while the SNSP and SNS_{AVG} pins are the input of an internal amplifier. The differential signal across SNSP and SNS_{AVG} is an averaged value of the signal across SNSP and SNSN. The operating input voltage range is 0V to 2V for all three sense pins. All the sense pins that are connected to the current comparator or the amplifier are high impedance with input bias currents of less than 1µA. The SNSN should be connected directly to V_{OUT}. The SNSP pin connects to the filter that has a R1•C1 time constant equal to one-fifth the L/DCR of the inductor. The SNS_{AVG} pin is connected to the second filter with a time constant three times that of R1•C1. Therefore, the switching ripple at SNS_{AVG} is attenuated. Do not float these pins during normal operation. Filter components, especially capacitors, must be placed close to the LTC7852/LTC7852-1, and the sense lines should run close together to a Kelvin connection underneath the current sense element (Figure 3). The LTC7852 is designed to be used with a very low DCR value to sense inductor current, requiring proper care, during layout of the sense lines. Otherwise, the parasitic resistance, capacitance and inductance will degrade the current sense signal integrity, making the programmed current limit unpredictable. As shown in Figure 4, resistor R1 is placed close to the output inductor and R2, C1, C2 are placed close to the IC pins to prevent noise coupling to the sense signal.

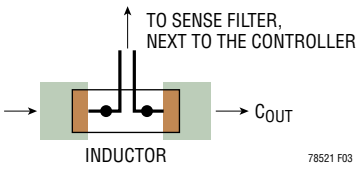


Figure 3. Sense Lines Placement with Inductor DCR

The LTC7852 could also be used like any typical current mode controller by disabling the SNS_{AVG} pin, tying it to V_{CC}. An R_{SENSE} resistor or a RC filter can be used to sense the output inductor signal and connects to the SNSP pin. If the RC filter is used, its time constant, R•C, should be equal to the L/DCR time constant of the output inductor.

Inductor DCR Sensing

The LTC7852 is specifically designed for high load current applications requiring the highest possible efficiency; it is capable of sensing the signal of an inductor DCR in the sub milliohm range (Figure 4). The DCR is the DC winding resistance of the inductor's copper, which is often less than 1mΩ for high current inductors. In high current and low output voltage applications, a conduction loss of a high DCR or a sense resistor will cause a significant reduction in power efficiency. For a specific output requirement,choose the inductor with the DCR that satisfies the maximum desirable sense voltage, and uses the relationship of the

APPLICATIONS INFORMATION

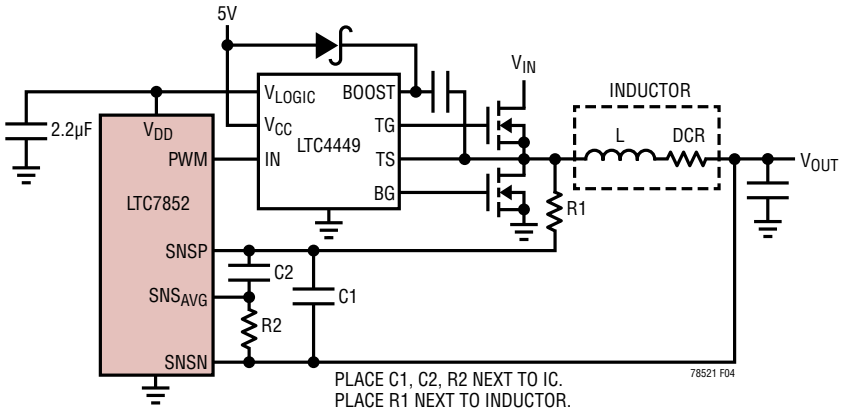


Figure 4. Inductor DCR Current Sensing

sense pin filters to output inductor characteristics as depicted below.

$$DCR = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

$$L/DCR = 5 \bullet R1 \bullet C1 = 1.6 \bullet R2 \bullet C2$$

where:

$V_{SENSE(MAX)}$: Maximum sense voltage for a given I_{LIM} threshold

I_{MAX}: Maximum load current

ΔI_L: Inductor ripple current

L, DCR: Output inductor characteristics

R1 • C1: Filter time constant of the SNSN pin

R2 • C2: Filter time constant of the SNS_{AVG} pin

Typically, C1 and C2 are selected in the range of 0.047µF to 0.47µF. If C1 and C2 are chosen to be 220nF, and an inductor of 250nH with 0.32mΩ DCR is selected, R1 and R2 will be 715Ω and 2.21k respectively.

There will be some power loss in R1 that relates to the duty cycle, and will be the most in continuous mode at the maximum input voltage:

$$P_{LOSS}(R1) = \frac{(V_{IN(MAX)} - V_{OUT}) \bullet V_{OUT}}{R1}$$

Ensure that R1 has a power rating higher than this value. However, DCR sensing eliminates the conduction loss of a sense resistor; it will provide a better efficiency at heavy loads. To maintain a good signal-to-noise ratio for the current sense signal, using a minimum ΔV_{SENSE} of 2mV for duty cycles less than 40% is desirable. The actual ripple voltage will be determined by the following equation:

$$\Delta V_{SENSE} = \frac{V_{OUT}}{V_{IN}} \bullet \frac{V_{IN} - V_{OUT}}{R_1 C_1 \bullet f_{OSE}}$$

DrMOS Current Sensing

The LTC7852-1 is designed to work with DrMOS which has built-in current sensing. The SNSN pins are regulated at 1.5V and a 2.2µF ~10µF low ESR ceramic decoupling capacitor to ground is required.

Soft-Start

The LTC7852/LTC7852-1 has the ability to soft-start by itself. A capacitor may be connected to its SS. The controller is in the shutdown state if its RUN pin voltage is below 1.22V. Its SS pin is actively pulled to ground in this shutdown state. If the RUN pin voltage is above 1.22V, the controller powers up. A soft-start current of 5µA then starts to charge the SS soft-start capacitor. Note that soft-start is achieved not by limiting the maximum output current of the controller but by controlling the output ramp voltage according to the ramp rate on the SS pin. The soft-start range is defined to be the voltage range from 0V to 0.5V on the SS pin. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = 0.5V \bullet \frac{C_{SS}}{5\mu A}$$

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When SS is rising from 0V to 0.4V, the controller disables the bottom MOSFET until ITH rises above 0.8V so that it always starts in discontinuous mode. After SS > 0.4V, the controller is in forced continuous mode, ensuring a clean PGOOD signal.

Pre-Biased Output Start-Up

There may be situations that require the power supply to start up with a pre-bias on the output capacitors. In this case, it is desirable to start up without discharging that output pre-bias. The LTC7852/LTC7852-1 can safely power up into a pre-biased output without discharging it. The LTC7852/LTC7852-1 accomplishes this by disabling both the top and bottom MOSFETs until the SS pin voltage and the internal soft-start voltage are above the V_{OSNS}^+ pin voltage. When V_{OSNS}^+ is higher than SS or the internal soft-start voltage, the error amp output is railed low. The control loop would like to turn the bottom MOSFET on, which would discharge the output. Disabling both top and bottom MOSFETs prevents the pre-biased output voltage from being discharged. When SS and the internal soft-start both cross 500mV or V_{OSNS}^+, whichever is lower, the top MOSFET is enabled. The bottom MOSFET is enabled later on after ITH rises above 800mV. If the pre-bias is higher than the OV threshold, the bottom gate is turned on immediately to pull the output back into the regulation window.

Fault Conditions: Current Limit

The LTC7852/LTC7852-1's current limiting is not disabled during soft-start. Under short-circuit conditions with very low duty cycles, the LTC7852/LTC7852-1 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short circuit ripple current is determined by the minimum on-time $t_{ON(MIN)}$ of the LTC7852/LTC7852-1(≈40ns with power stage), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \bullet \frac{V_{IN}}{L}$$

The resulting short-circuit current is:

$$I_{SC} = \left(\frac{V_{SENSE(MAX)}}{R_{SENSE}} - \frac{1}{2} \Delta I_{L(SC)}\right)$$

Overcurrent Fault Recovery

When the output of the power supply is loaded beyond its preset current limit, the regulated output voltage may collapse depending on the load. The output may be shorted to ground through a very low impedance path or it may be a resistive short, in which case the output will collapse partially, until the load current equals the preset current limit. The controller will continue to source current into the short for 32 switching periods. The amount of current sourced depends on the ILIM pin setting. If the overcurrent fault still exists after 32 switching periods, the controller enters hiccup mode. The ITH pin will be pulled to ground by an internal MOSFET, and therefore both the MOSFETs are off. The SS soft-start capacitor will be discharged by a 2.5µA current. When the SS reaches to ground, the ITH is released and the circuit retries to soft-start, as described in the section Shutdown and Start-Up. The hiccup overcurrent protection is not disabled during soft-start period.The sleep time is estimated by:

$$t_{SLEEP} = C_{SS}\left(\frac{2.7V}{I_{SS}} + \frac{3.3V}{2.5\mu A}\right)$$

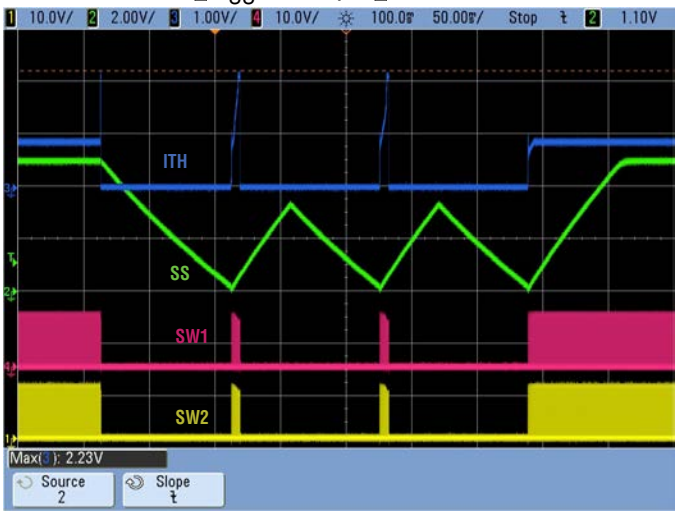

Figure 5. Hiccup Mode Overcurrent Protection and Recovery

If the short is removed before the 32 switching period timer expires, the output soft recovers using the internal soft-start, thus reducing output overshoot. In the absence of this feature, the output capacitors would have been charged at current limit, and in applications with minimal output capacitance this may have resulted in output overshoot.

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Inductor Value Calculation

Given the desired input and output voltages, the inductor value and operating frequency, f_{OSC}, directly determine the inductor's peak-to-peak ripple current:

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN}}\left(\frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet L}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor. A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet I_{RIPPLE}} \bullet \frac{V_{OUT}}{V_{IN}}$$

Inductor Core Selection

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

PWM Pins

The PWM pins are three-state compatible outputs, designed to drive MOSFET drivers and DrMOSs which do not represent a heavy capacitive load. An external resistor divider may be used to set the voltage to mid-rail while in the high impedance state.

Power MOSFET and Schottky Diode (Optional) Selection

At least two external power MOSFETs need to be selected: One N-channel MOSFET for the top (main) switch and one or more N-channel MOSFET(s) for the bottom (synchronous) switch. The number, type and on-resistance of all MOSFETs selected take into account the voltage step-down ratio as well as the actual position (main or synchronous) in which the MOSFET will be used. A much smaller and much lower input capacitance MOSFET should be used for the top MOSFET in applications that have an output voltage that is less than one-third of the input voltage. In applications where $V_{IN} >> V_{OUT}$, the top MOSFETs' on-resistance is normally less important for overall efficiency than its input capacitance at operating frequencies above 300kHz. MOSFET manufacturers have designed special purpose devices that provide reasonably low on-resistance with significantly reduced input capacitance for the main switch application in switching regulators.

The peak-to-peak MOSFET gate drive levels are set by the bias voltage of the driver, requiring the use of logic-level threshold MOSFETs in most applications. Pay close attention to the BVDSS specification for the MOSFETs as well; many of the logic-level MOSFETs are limited to 30V or less. Selection criteria for the power MOSFETs include the on-resistance, $R_{DS(ON)}$, input capacitance, input voltage and maximum output current. MOSFET input capacitance is a combination of several components but can be taken from the typical gate charge curve included on most data sheets (Figure 6). The curve is generated by forcing a constant input current into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time.

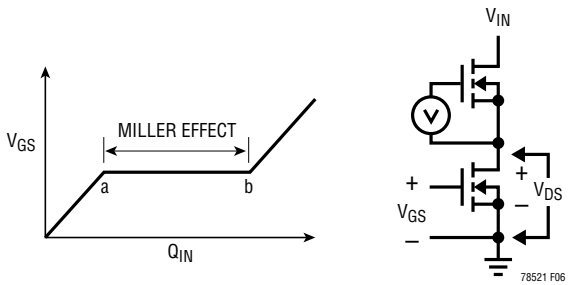

Figure 6. Gate Charge Characteristic

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The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain drops the voltage across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given V_{DS} drain voltage, but can be adjusted for different V_{DS} voltages by multiplying the ratio of the application V_{DS} to the curve specified V_{DS} values. A way to estimate the C_{MILLER} term is to take the change in gate charge from points a and b on a manufacturer's data sheet and divide by the stated V_{DS} voltage specified. C_{MILLER} is the most important selection criterion for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets. C_{RSS} and C_{OS} are specified sometimes but definitions of these parameters are not included. When the controller is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

The power dissipation for the main and synchronous MOSFETs at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet \left(\frac{1}{V_{INTVCC} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right)\bullet f$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$, RDR is the effective top driver resistance (approximately 2Ω at $V_{GS} = V_{MILLER}$), V_{IN} is the drain potential and the change in drain potential in the particular application. $V_{TH(MIN)}$ is the data sheet specified typical gate threshold voltage specified in the power MOSFET data sheet at the specified drain current. C_{MILLER} is the calculated capacitance using the gate charge curve from the MOSFET data sheet and the technique described.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which peak at the highest input voltage. For $V_{IN} < 20V$, the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

An optional Schottky diode across the synchronous MOSFET conducts during the dead time between the conduction of the two large power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead time and requiring a reverse-recovery period which could cost as much as several percent in efficiency. A 2A to 8A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition loss due to their larger junction capacitance.

MOSFET Driver Selection

Gate driver ICs, DrMOSs and power blocks with an interface compatible with the LTC7852/LTC7852-1's three-state PWM outputs can be used. Always enable the power stage first, before the LTC7852/LTC7852-1 is enabled.

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C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \simeq \frac{I_{MAX}}{V_{IN}}\left(V_{OUT}\right)\left(V_{IN} - V_{OUT}\right)^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life.

This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC7852/LTC7852-1, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question. Ceramic capacitors are becoming very popular for small designs but several cautions should be observed. X7R, X5R and Y5V are examples of a few of the ceramic materials used as the dielectric layer, and these different dielectrics have very different effect on the capacitance value due to the voltage and temperature conditions applied. Physically, if the capacitance value changes due to applied voltage change, there is a concomitant piezo effect which results in radiating sound! A load that draws varying current at an audible rate may cause an attendant varying input voltage on a ceramic capacitor, resulting in an audible signal. A secondary issue relates to the energy flowing back into a ceramic capacitor whose capacitance value is being reduced by the increasing charge. The voltage can increase at a considerably higher rate than the constant current being supplied because the capacitance value is decreasing as the voltage is increasing! Nevertheless, ceramic capacitors, when properly selected and used, can provide the lowest overall loss due to their extremely low ESR. A small (0.1µF to 1µF) bypass capacitor, C_{IN}, between the chip V_{IN} pin and ground, placed close to the LTC7852/LTC7852-1, is also suggested. A 2.2Ω to 10Ω resistor placed between C_{IN} and V_{IN} pin provides further isolation. The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically once the ESR requirement is satisfied the capacitance is adequate for filtering. The steady-state output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \simeq \Delta I_{RIPPLE}\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_{RIPPLE} = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_{RIPPLE} increases with input voltage. The output ripple will be less than 50mV at maximum V_{IN} with $\Delta I_{RIPPLE} = 0.4I_{OUT(MAX)}$ assuming:

C_{OUT} required $ESR < N \bullet R_{SENSE}$

and

$$C_{OUT} > \frac{1}{(8f)(R_{SENSE})}$$

The emergence of very low ESR capacitors in small, surface mount packages makes very small physical implementations possible. The ability to externally compensate the switching regulator loop using the ITH pin allows a much wider selection of output capacitor types. The impedance characteristic of each capacitor type is significantly different than an ideal capacitor and therefore requires accurate modeling or bench evaluation during design. Manufacturers such as Nichicon, Nippon Chemi-Con and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitors available from Sanyo and the Panasonic SP surface mount types have a good ESR • size product.

Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. Ceramic capacitors from AVX, Taiyo Yuden, Murata and TDK offer high capacitance value and very low ESR, especially applicable for low output voltage applications.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available

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in surface mount configurations. New special polymer surface mount capacitors offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent choices are the AVX TPS, AVX TPSV, the KEMET T510 series of surface mount tantalums or the Panasonic SP series of surface mount special polymer capacitors available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo POSCAP, Sanyo OS-CON, Nichicon PL series and Sprague 595D series. Consult the manufacturers for other specific recommendations.

Differential Amplifier

The LTC7852/LTC7852-1 has true remote voltage sense capability. The sense connections should be returned from the load, back to the differential amplifier's inputs through a common, tightly coupled pair of PC traces. The differential amplifier rejects common mode signals capacitively or inductively radiated into the feedback PC traces as well as ground loop disturbances. The LTC7852/LTC7852-1 diffamp has high input impedance on V_{OSNS}^+ pin. The output of the diffamp connects to the inverting input of the error amplifier internally.

Setting Output Voltage

The LTC7852/LTC7852-1 output voltage is set by an external feedback resistive divider carefully placed across the output, as shown in Figure 2. The regulated output voltage is determined by:

$$V_{OUT} = 0.5V \bullet \left(1 + \frac{R_{D1}}{R_{D2}}\right)$$

To improve the frequency response, a feedforward capacitor, C_{F1}, may be used. Great care should be taken to route the V_{OSNS}^+ line away from noise sources, such as the inductor or the SW line. To minimize the effect of the voltage drop caused by high current flowing through board conductance; connect V_{OSNS}^- and V_{OSNS}^+ sense lines close to the ground and the load output respectively.

V_{DD} and V1P5 LDO

The LTC7852/LTC7852-1 features a true PMOS LDO that supplies power to V_{DD} and V1P5 from the V_{CC} supply. The V_{DD} and V1P5 must be bypassed to ground with a minimum of 2.2µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the V_{DD} and GND pins is highly recommended. Please do not load the LDO with an external circuit at the V_{DD} pin. V_{DD} must be within approximately 7% of its targeted value before the RUN pin is released. In addition, when V1P5 is approximately 20% below its regulated value, the controller is kept in shutdown.

Phase-Locked Loop and Frequency Synchronization

The LTC7852/LTC7852-1 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the turn-on of the top MOSFET to be locked to the rising edge of an external clock signal applied to the PLLIN pin. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. There is a precision 20µA current flowing out of the FREQ pin. This allows the user to use a single resistor to GND to set the switching frequency when no external clock is applied to the PLLIN pin. Do not program the FREQ pin voltage below 0.57V. The internal switch between the FREQ pin and the integrated PLL filter network is on, allowing the filter network to be pre-charged at the same voltage as of the FREQ pin. The relationship between the voltage on the FREQ pin and operating frequency is shown in Figure 7 and specified in the Electrical Characteristics table. If an external clock is detected on the PLLIN pin, the internal switch mentioned above turns off and isolates the influence of the FREQ pin. Note that the LTC7852/LTC7852-1 can only be synchronized to an external clock whose frequency is within range of the LTC7852/LTC7852-1's internal VCO. Do not synchronize to a clock below 250kHz. A simplified block diagram is shown in Figure 8.

APPLICATIONS INFORMATION

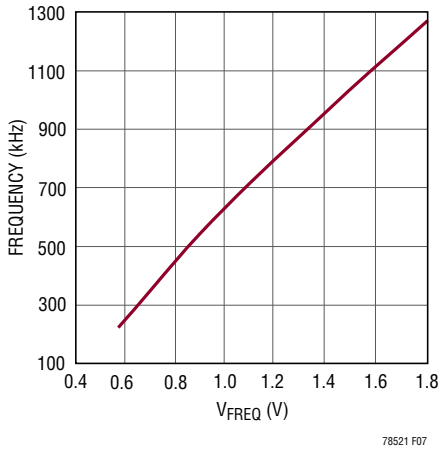

Figure 7. Relationship Between Oscillator Frequency and Voltage at the FREQ Pin

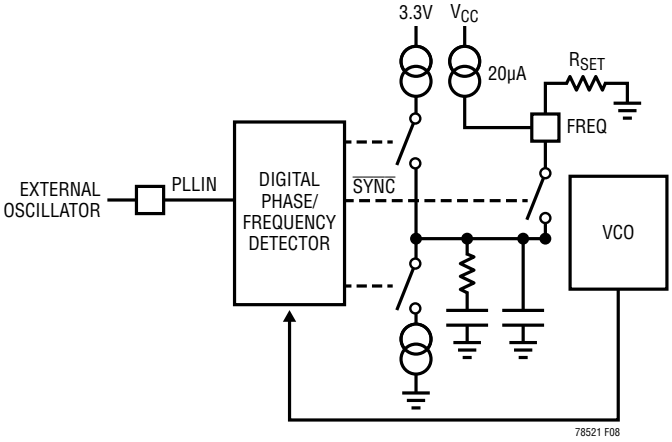

Figure 8. Phase-Locked Loop Block Diagram

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the filter network. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the filter network. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the filter network is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor CLP holds the voltage. Typically, the external clock (on the PLLIN pin) input high threshold is 1.6V, while the input low threshold is 1V.

Using the CLKOUT and PHCFG Pins in Multiphase Applications

The LTC7852/LTC7852-1 features CLKOUT and PHCFG pins that allow multiple LTC7852/LTC7852-1 ICs to be daisy chained together in multiphase applications. The clock output signal on the CLKOUT pin can be used to synchronize additional ICs in a 8-, 10- or 12-phase power supply solution feeding a single high current output, or even several outputs from the same input supply.

The PHCFG pin is used to adjust the phase relationship between six channels, as well as the phase relationship between channel 1 and CLKOUT. The phases are calculated relative to zero degrees, defined as the rising edge of PWM1. Refer to the Applications Information section for more details on how to create multiphase applications.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC7852/LTC7852-1 is capable of turning on the top MOSFET. It is determined by internal timing delays, power stage timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the voltage ripple and current ripple will increase.

The minimum on-time for the LTC7852/LTC7852-1 is approximately 40ns, with good PCB layout, minimum 30% inductor current ripple and at least 2mV ripple on the current sense signal. The minimum on-time can be affected by PCB switching noise in the voltage and current loop. As the peak sense voltage decreases the minimum on time gradually increases This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

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Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC7852/LTC7852-1 circuits: 1) IC V_{CC} current, 2) MOSFET driver current, 3) I^2R losses, 4) topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics table. V_{IN} current typically results in a small (<0.1%) loss.
2. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from the driver supply to ground. The resulting dQ/dt is a current out of the driver supply that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.
3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor and current sense resistor. In continuous mode, the average output current flows through L and R_{SENSE}, but is chopped between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 10mΩ, R_L = 10mΩ, R_{SENSE} = 5mΩ, then the total resistance is 25mΩ. This results in losses ranging from 2% to 8% as the output current increases from 3A to 15A for a 5V output, or a 3% to 12% loss for a 3.3V output.

   Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!
4. Transition losses apply only to the topside MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

   Transition Loss = $(1.7)\ V_{IN}^2 \bullet I_{O(MAX)} \bullet C_{RSS} \bullet f$

   Other hidden losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these system level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. Other losses including Schottky conduction losses during dead time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \bullet$ ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the ITH pin not only allows optimization of control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step,

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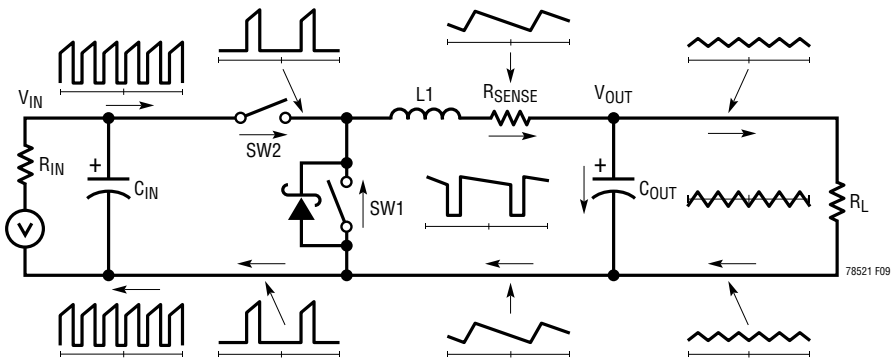
rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in the Typical Application circuit will provide an adequate starting point for most applications. The ITH series RC-CC filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing RC and the bandwidth of the loop will be increased by decreasing CC. If RC is increased by the same factor that CC is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 9. Check the following in the PC layout:

1. The V_{CC}, V_{DD}, V1P5 decoupling capacitor should be placed immediately adjacent to the IC between the V_{CC} pin and GND plane. A 1µF ceramic capacitor of the X7R or X5R type is small enough to fit very close to the IC. An additional 4.7µF to 10µF of ceramic, tantalum or other very low ESR capacitance is recommended in order to keep the internal IC supply quiet.
2. Place the feedback divider between the + and – terminals of C_{OUT}. Route V_{OSNS}^+ and V_{OSNS}^- with minimum PC trace spacing from the IC to the feedback divider.
3. Are the SNS_{AVG}, SNSP and SNSN printed circuit traces routed together with minimum PC trace spacing? The filter capacitors between SNS_{AVG}, SNSP and SNSN should be as close as possible to the pins of the IC.
4. Do the (+) plates of C_{IN} connect to the drain of the topside MOSFET as closely as possible? This capacitor provides the pulsed current to the MOSFET.
5. Keep the switching nodes away from sensitive small signal nodes (SNSP, SNS_{AVG}, SNSN, V_{OSNS}^+, V_{OSNS}^-). Ideally the PWM and switch nodes printed circuit traces should be routed away and separated from the IC and especially the quiet side of the IC. Separate the high dv/ dt traces from sensitive small-signal nodes with ground traces or ground planes.
6. Use a low impedance source such as a logic gate to drive the PLLIN pin and keep the lead as short as possible.

APPLICATIONS INFORMATION



BOLD LINES INDICATE HIGH, SWITCHING CURRENTS. KEEP LINES TO A MINIMUM LENGTH.

Figure 9. Branch Current Waveforms

7. The 47pF to 330pF ceramic capacitor between the ITH pin and signal ground should be placed as close as possible to the IC. Figure 9 illustrates all branch currents in a switching regulator. It becomes very clear after studying the current waveforms why it is critical to keep the high switching current paths to a small physical size. High electric and magnetic fields will radiate from these loops just as radio stations transmit signals. The output capacitor ground should return to the negative terminal of the input capacitor and not share a common ground path with any switched current paths. The left half of the circuit gives rise to the noise generated by a switching regulator. The ground terminations of the synchronous MOSFET and Schottky diode should return to the bottom plate(s) of the input capacitor(s) with a short isolated PC trace since very high switched currents are present. External OPTI-LOOP® compensation allows overcompensation for PC layouts which are not optimized but this is not the recommended design procedure.

8. Are the signal and power grounds kept separate? The IC ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The V_{OSNS}^+ and ITH traces should be as short as possible. The path formed by the top N-channel MOSFET, Schottky diode and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.

9. Use a modified “star ground” technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the GND pin of the IC.

Design Example

A design example of a 6-phase high current regulator is shown in Figure 10. Assume V_{IN} = 12V(nominal), V_{IN} = 20V(maximum), V_{OUT} = 1.0V, I_{MAX} = 200A, and f = 400kHz.

The regulated output voltage is determined by:

$$V_{OUT} = 0.5V \bullet \left(1 + \frac{R_{D1}}{R_{D2}}\right)$$

Using a 20k 1% resistor from the V_{FB} node to ground, the top feedback resistor is 20k. The frequency is set by biasing the FREQ pin to 0.75V (see Figure 7).

The inductance value is based on a 30% maximum ripple current assumption (10A per phase). The highest value of ripple current occurs at the maximum input voltage:

$$L = \frac{V_{OUT}}{f \bullet I_{L(MAX)}} \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

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This design will require 0.23µH. The Wurth 744301025, 0.25µH inductor is chosen. At the nominal input voltage (12V), the ripple current will be:

$$\Delta I_{L(NOM)} = \frac{V_{OUT}}{f \bullet L}\left(1 - \frac{V_{OUT}}{V_{IN(NOM)}}\right)$$

It will have 9.2A (28%) ripple. The peak inductor current will be the maximum DC value plus one-half the ripple current, or 38A per phase.

The minimum on-time occurs at the maximum V_{IN}, and should not be less than 100ns (includes margin):

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)} f} = \frac{1.0V}{20V(400kHz)} = 124ns$$

DCR sensing is used in this circuit. If C1 and C2 are chosen to be 220nF, based on the chosen 0.25µH inductor with 0.32mΩ DCR, R1 and R2 can be calculated as:

$R1 = L/DCR \bullet C1 \bullet 5 = 710\Omega$

$R2 = L/DCR \bullet C2 \bullet 1.6 = 2.22k$

Choose R1 = 715Ω and R2 = 2.32k.

The maximum DCR of the inductor is 0.34mΩ. The $V_{SENSE(MAX)}$ is calculated as:

$V_{SENSE(MAX)} = I_{PEAK} \bullet DCRMAX = 12mV$

The current limit is chosen to be 15mV.

The power dissipation on the topside MOSFET can be easily estimated. Choosing an Infineon BSC050NE2LS MOSFET results in: $R_{DS(ON)}$ = 7.1mΩ (max), V_{MILLER} = 2.8V, $C_{MILLER} \cong$ 108pF. At maximum input voltage with T_J (estimated) = 75°C.

$$P_{MAIN} = \frac{1.0V}{20V}(33.3A)^2[1+(0.005)(75°C - 25°C)] \bullet (0.0071\Omega) + (20V)^2\left(\frac{33.3A}{2}\right)(2\Omega)(108pF) \bullet \left(\frac{1}{5V - 2.8V} + \frac{1}{2.8V}\right)(400kHz)$$

$$= 492mW + 467mW$$

$$= 959mW / phase$$

An Infineon BSC010NE2LS, $R_{DS(ON)}$ = 1.3mΩ (Max), is chosen for the bottom FET. The resulting power loss is:

$$P_{SYNC} = \frac{20V - 1.0V}{20V}(33.3A)^2 \bullet [1+(0.005) \bullet (75° - 25°C)] \bullet 0.0013\Omega$$

$$P_{SYNC} = 1.7W / Phase$$

C_{IN} is chosen for an equivalent RMS current rating of at least 13.7A. C_{OUT} is chosen with an equivalent ESR of 4.5mΩ for low output ripple. The output ripple is continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$V_{ORIPPLE} = R_{ESR}(\Delta I_L) = 0.0045\Omega \bullet 10A = 45mV_{P-P}$

Further reductions in output voltage ripple can be made by placing a 100µF ceramic capacitor across C_{OUT}.

TYPICAL APPLICATIONS

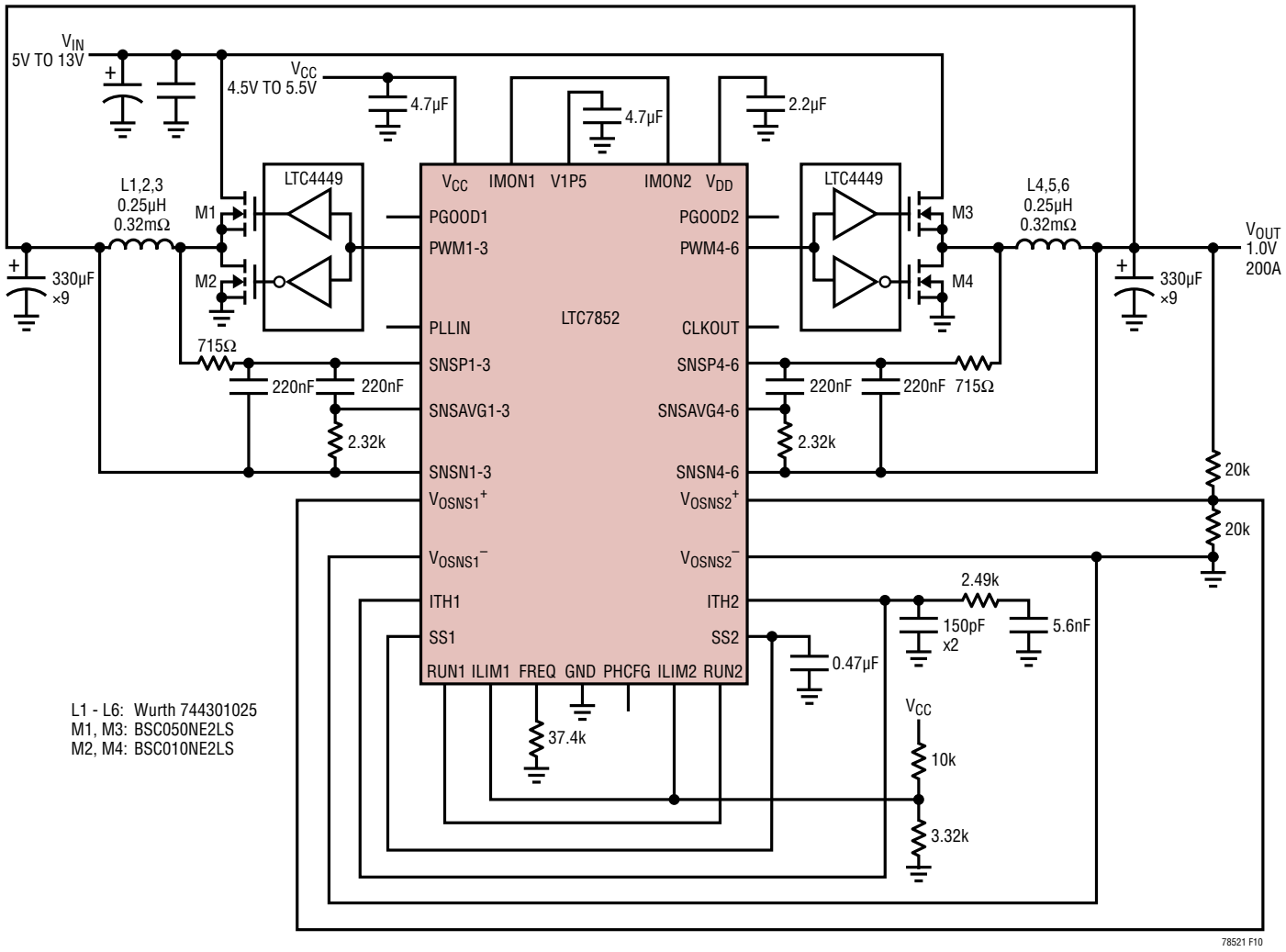


Figure 10. Single Output 6-Phase 1V/200A LTC7852 Converter with Discrete Drivers and MOSFETs

TYPICAL APPLICATIONS

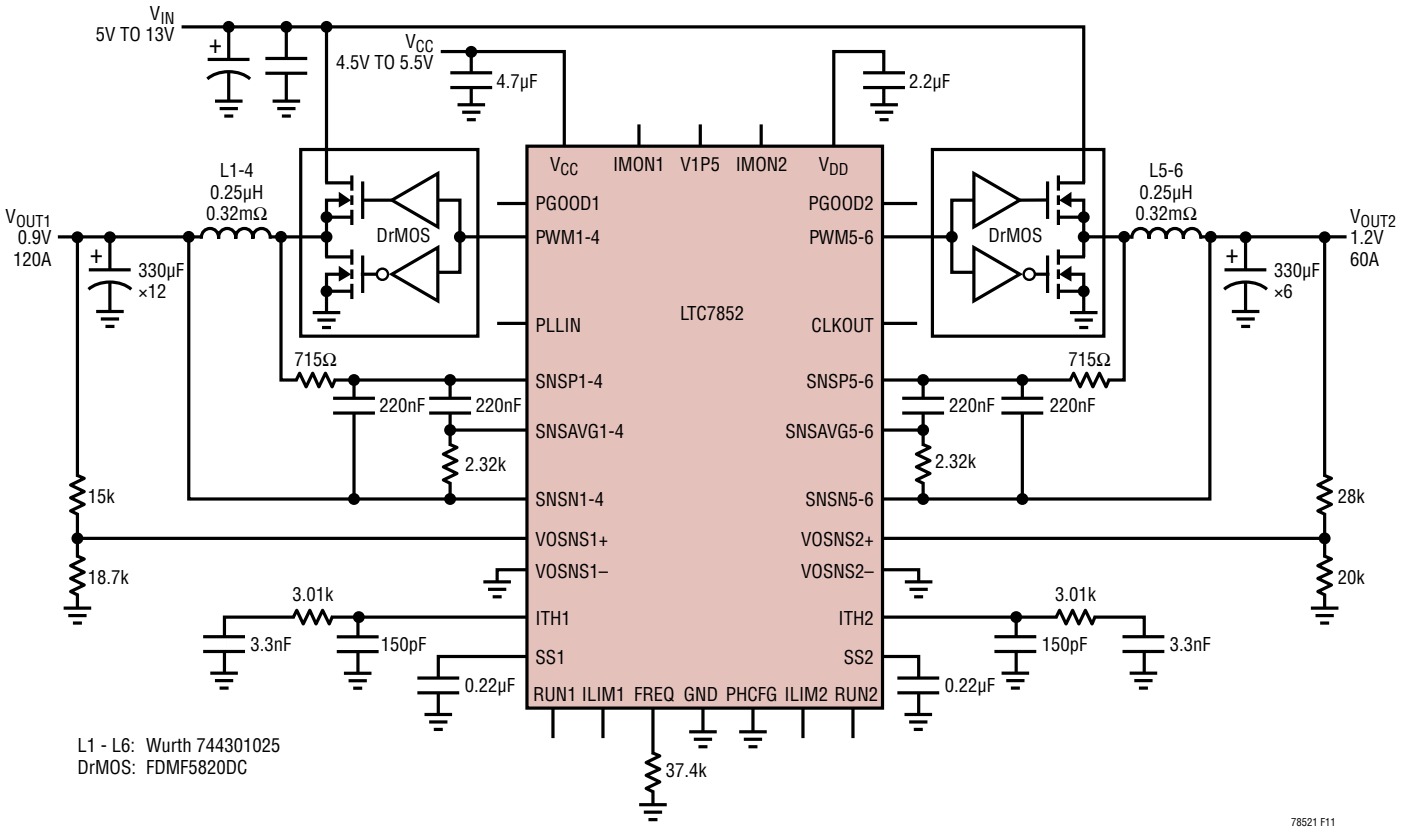
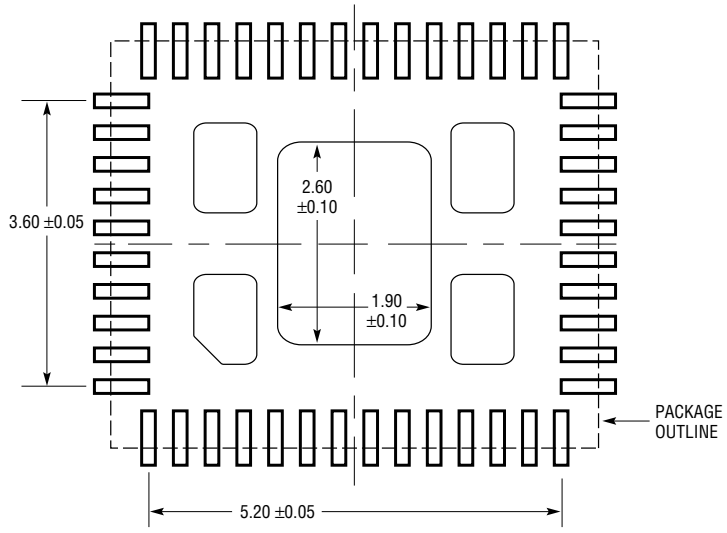


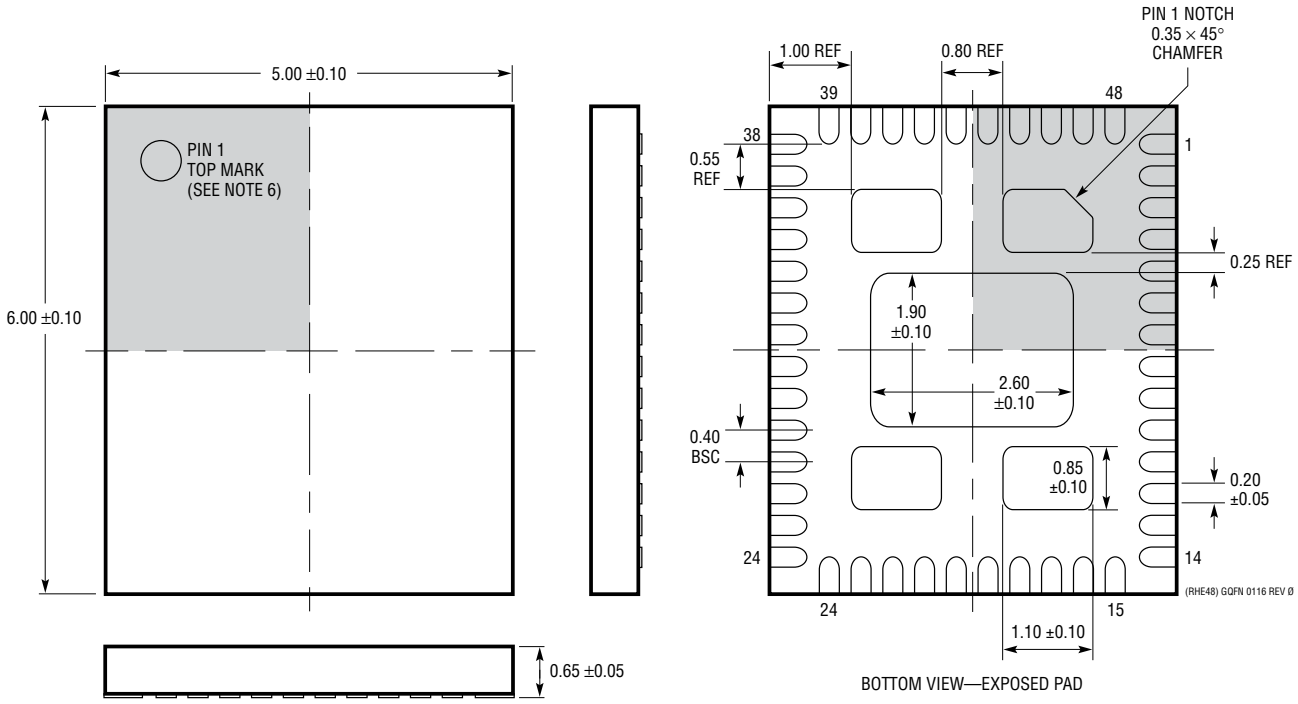
Figure 11. Dual Output 4-Phase 0.9V/120A and 2-Phase 1.2V/60A LTC7852 Converter with DRMOS

PACKAGE DESCRIPTION

RHE Package
48-Lead Plastic GQFN (5mm × 6mm)
(Reference LTC DWG # 05-08-1527 Rev Ø)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

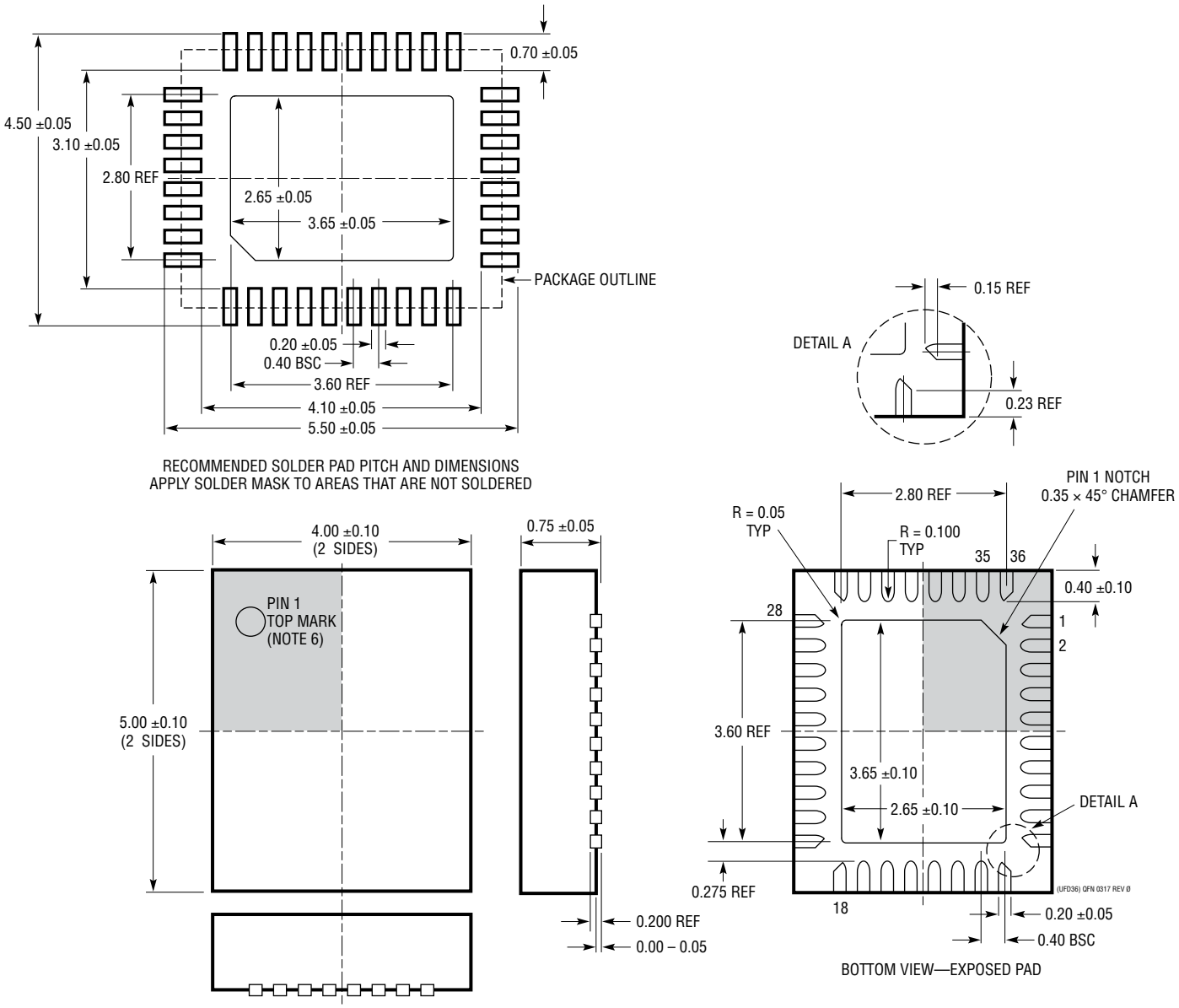


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.25mm ON ANY SIDE
5. EXPOSED PAD SHALL BE Pd Ni Au PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

UFD Package
36-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1575 Rev Ø)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/19	Changed RUN Pin Note to 5µA	8
		Changed Main Control Loop and Shutdown/Start-up Current to 1.3µA	28
B	01/21	Added Pad Labels	3

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