Micropower Octal 8-Bit and 10-Bit DACs

FEATURES

- **Tiny: 8 DACs in the Board Space of an SO-8**
- **Micropower: 56µA per DAC Plus 1µA Sleep Mode for Extended Battery Life**
- Pin Compatible 8-Bit LTC1665 and 10-Bit LTC1660
- Wide 2.7V to 5.5V Supply Range
- **Rail-to-Rail Voltage Outputs Drive 1000pF**
- Reference Range Includes Supply for Ratiometric 0V-to-V_{CC} Output
- **Reference Input Impedance is Constant—Eliminates External Buffer**

APPLICATIONS

- Mobile Communications
- Remote Industrial Devices
- Automatic Calibration for Manufacturing
- Portable Battery-Powered Instruments
- Trim/Adjust Applications

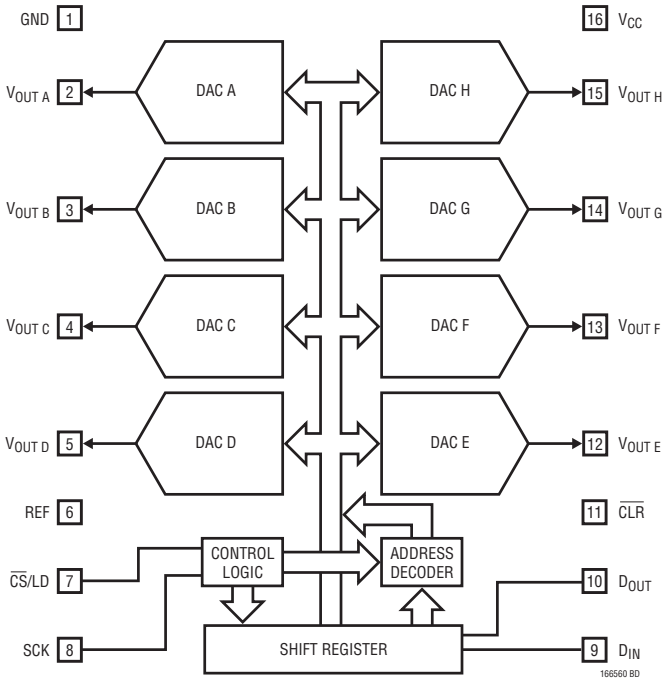
DESCRIPTION

The 8-bit LTC®1665 and 10-bit LTC1660 integrate eight accurate, serially addressable digital-to-analog converters (DACs) in tiny 16-pin narrow SSOP packages. Each buffered DAC draws just 56µA total supply current, yet is capable of supplying DC output currents in excess of 5mA and reliably driving capacitive loads to 1000pF. Sleep mode further reduces total supply current to 1µA.

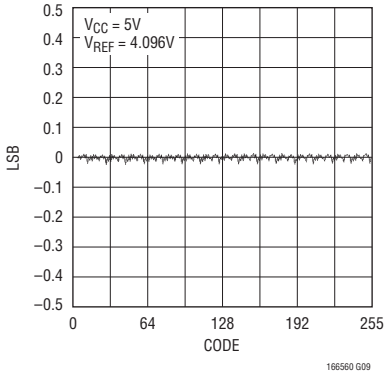
Linear Technology's proprietary, inherently monotonic voltage interpolation architecture provides excellent linearity while allowing for an exceptionally small external form factor.

Ultralow supply current, power-saving Sleep mode and extremely compact size make the LTC1665 and LTC1660 ideal for battery-powered applications, while their ease of use, high performance and wide supply range make them excellent choices as general purpose converters.

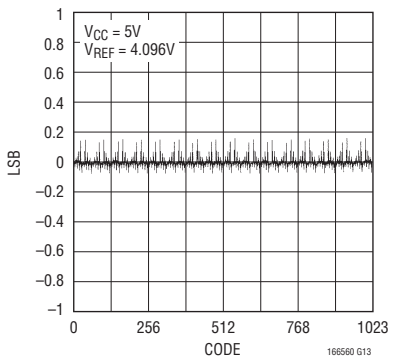
BLOCK DIAGRAM



LTC1665 Differential Nonlinearity (DNL)



LTC1660 Differential Nonlinearity (DNL)

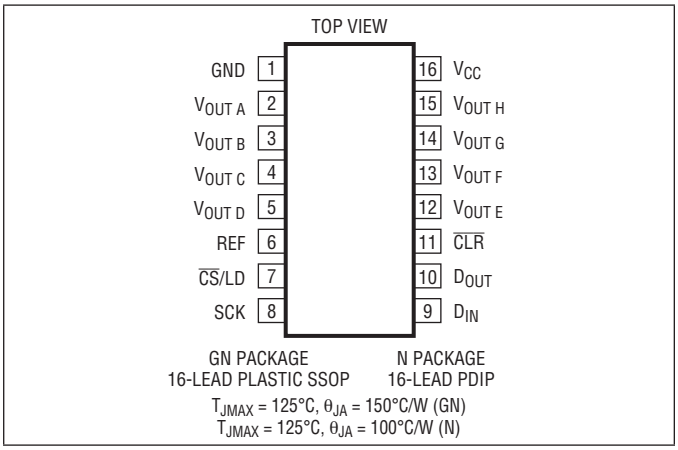


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} to GND ..... –0.2V to 7.5V
Logic Inputs to GND ..... –0.2V to 7.5V
$V_{OUT\ A}$, $V_{OUT\ B}$, $V_{OUT\ H}$,
REF to GND .....–0.2V to (V_{CC} + 0.2V)
Maximum Junction Temperature ..... 125°C
Operating Temperature Range
LTC1665C/LTC1660C..... 0°C to 70°C
LTC1665I/LTC1660I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1665CGN#PBF	LTC1665CGN#PBF	1665	16-Lead Plastic SSOP	0°C to 70°C
LTC1665IGN#PBF	LTC1665IGN#PBF	1665I	16-Lead Plastic SSOP	–40°C to 85°C
LTC1660CGN#PBF	LTC1660CGN#PBF	1660	16-Lead Plastic SSOP	0°C to 70°C
LTC1660IGN#PBF	LTC1660IGN#PBF	1660I	16-Lead Plastic SSOP	–40°C to 85°C
LTC1665CN#PBF	LTC1665CN#PBF	LTC1665CN	16-Lead Plastic PDIP	0°C to 70°C
LTC1665IN#PBF	LTC1665IN#PBF	LTC1665IN	16-Lead Plastic PDIP	–40°C to 85°C
LTC1660CN#PBF	LTC1660CN#PBF	LTC1660CN	16-Lead Plastic PDIP	0°C to 70°C
LTC1660IN#PBF	LTC1660IN#PBF	LTC1660IN	16-Lead Plastic PDIP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, $V_{REF} \le V_{CC}$, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1665 MIN	LTC1665 TYP	LTC1665 MAX	LTC1660 MIN	LTC1660 TYP	LTC1660 MAX	UNITS
Accuracy										
	Resolution		●	8			10			Bits
	Monotonicity	$V_{REF} \le V_{CC}$ – 0.1V (Note 2)	●	8			10			Bits
DNL	Differential Nonlinearity	$V_{REF} \le V_{CC}$ – 0.1V (Note 2)	●		±0.1	±0.5		±0.2	±0.75	LSB
INL	Integral Nonlinearity	$V_{REF} \le V_{CC}$ – 0.1V (Note 2)	●		±0.2	±1.0		±0.6	±2.5	LSB
V_{OS}	Offset Error	(Note 7)	●		±10	±30		±10	±30	mV
	V_{OS} Temperature Coefficient		●		±15			±15		µV/°C
FSE	Full-Scale Error	V_{CC} = 5V, V_{REF} = 4.096V	●		±1	±4		±3	±15	LSB
	Full-Scale Error Temperature Coefficient		●		±30			±30		µV/°C
PSR	Power Supply Rejection	V_{REF} = 2.5V			0.045			0.18		LSB/V

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, $V_{REF} \le V_{CC}$, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Input							
	Input Voltage Range		●	0		V_{CC}	V
	Resistance	Not in Sleep Mode	●	35	65		kΩ
	Capacitance	(Note 6)			15		pF
I_{REF}	Reference Current	Sleep Mode	●		0.001	1	µA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.7		5.5	V
I_{CC}	Supply Current	V_{CC} = 5V (Note 3) V_{CC} = 3V (Note 3) Sleep Mode (Note 3)	● ● ●		450 340 1	730 530 3	µA µA µA
DC Performance							
	Short-Circuit Current Low	V_{OUT} = 0V, V_{CC} = 5.5V, V_{REF} = 5.1V, Code = Full Scale	●	10	30	100	mA
	Short-Circuit Current High	V_{OUT} = V_{CC} = 5.5V, V_{REF} = 5.1V, Code = 0	●	10	27	120	mA
AC Performance							
	Voltage Output Slew Rate	Rising (Notes 4, 5) Falling (Notes 4, 5)			0.60 0.25		V/µs V/µs
	Voltage Output Settling Time	To ±0.5LSB (Notes 4, 5)			30		µs
	Capacitive Load Driving				1000		pF
Digital I/O							
V_{IH}	Digital Input High Voltage	V_{CC} = 2.7V to 5.5V V_{CC} = 2.7V to 3.6V	● ●	2.4 2.0			V V
V_{IL}	Digital Input Low Voltage	V_{CC} = 4.5V to 5.5V V_{CC} = 2.7V to 5.5V	● ●			0.8 0.6	V V
V_{OH}	Digital Output High Voltage	I_{OUT} = –1mA, D_{OUT} Only	●	V_{CC} – 1			V
V_{OL}	Digital Output Low Voltage	I_{OUT} = 1mA, D_{OUT} Only	●			0.4	V
I_{LK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±10	µA
C_{IN}	Digital Input Capacitance	(Note 6)	●			10	pF

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (See Figure 1)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} = 4.5V to 5.5V							
t_1	D_{IN} Valid to SCK Setup		●	40			ns
t_2	D_{IN} Valid to SCK Hold		●	0			ns
t_3	SCK High Time	(Note 6)	●	30			ns
t_4	SCK Low Time	(Note 6)	●	30			ns
t_5	$\overline{CS}$/LD Pulse Width	(Note 6)	●	80			ns
t_6	LSB SCK High to $\overline{CS}$/LD High	(Note 6)	●	30			ns
t_7	$\overline{CS}$/LD Low to SCK High	(Note 6)	●	80			ns
t_8	D_{OUT} Propagation Delay	C_{LOAD} = 15pF (Note 6)	●	5		80	ns
t_9	SCK Low to $\overline{CS}$/LD Low	(Note 6)	●	20			ns
t_{10}	$\overline{CLR}$ Pulse Width	(Note 6)	●	100			ns
t_{11}	$\overline{CS}$/LD High to SCK Positive Edge	(Note 6)	●	30			ns
	SCK Frequency	Continuous Square Wave (Note 6) Continuous 23% Duty Cycle Pulse (Note 6) Gated Square Wave (Note 6)	● ● ●			5.00 7.69 16.7	MHz MHz MHz
V_{CC} = 2.7V to 5.5V							
t_1	D_{IN} Valid to SCK Setup	(Note 6)	●	60			ns
t_2	D_{IN} Valid to SCK Hold	(Note 6)	●	0			ns
t_3	SCK High Time	(Note 6)	●	50			ns
t_4	SCK Low Time	(Note 6)	●	50			ns
t_5	$\overline{CS}$/LD Pulse Width	(Note 6)	●	100			ns
t_6	LSB SCK High to $\overline{CS}$/LD High	(Note 6)	●	50			ns
t_7	$\overline{CS}$/LD Low to SCK High	(Note 6)	●	100			ns
t_8	D_{OUT} Propagation Delay	C_{LOAD} = 15pF (Note 6)	●	5		150	ns
t_9	SCK Low to $\overline{CS}$/LD Low	(Note 6)	●	30			ns
t_{10}	$\overline{CLR}$ Pulse Width	(Note 6)	●	120			ns
t_{11}	$\overline{CS}$/LD High to SCK Positive Edge	(Note 6)	●	30			ns
	SCK Frequency	Continuous Square Wave (Note 6) Continuous 28% Duty Cycle Pulse Gated Square Wave	● ● ●			3.85 5.55 10	MHz MHz MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Nonlinearity and monotonicity are defined from code 4 to code 255 for the LTC1665 and from code 20 to code 1023 for the LTC1660. See Applications Information.

Note 3: Digital inputs at 0V or V_{CC}.

Note 4: Load is 10kΩ in parallel with 100pF.

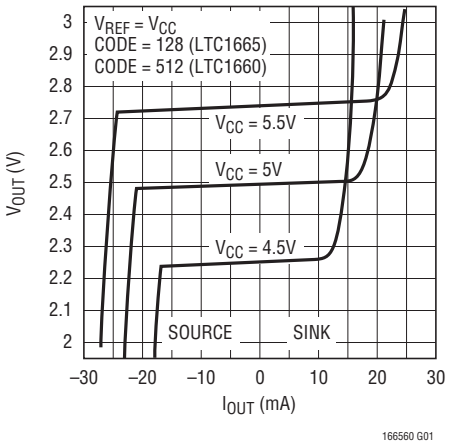
Note 5: V_{CC} = V_{REF} = 5V. DAC switched between $0.1V_{FS}$ and $0.9V_{FS}$, i.e., codes 26 and 230 for the LTC1665 or codes 102 and 922 for the LTC1660.

Note 6: Guaranteed by design and not production tested.

Note 7: Measured at code 4 for the LTC1665 and code 20 for the LTC1660.

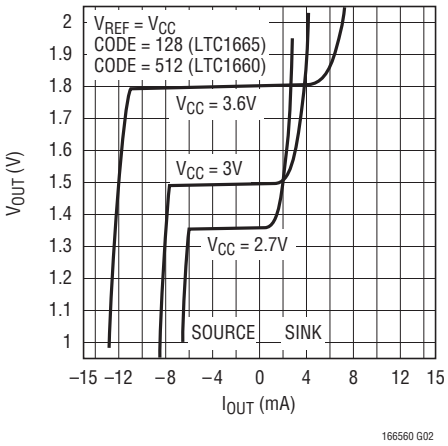
TYPICAL PERFORMANCE CHARACTERISTICS (LTC1665/LTC1660)

Midscale Output Voltage vs Load Current



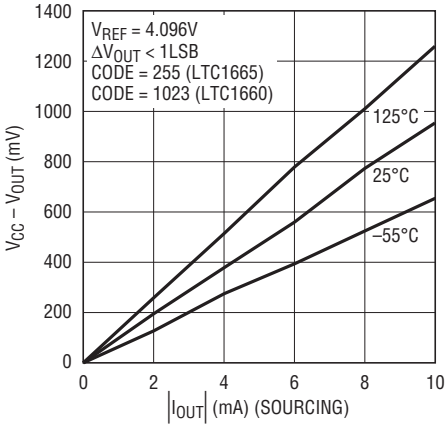
166560 G01

Midscale Output Voltage vs Load Current



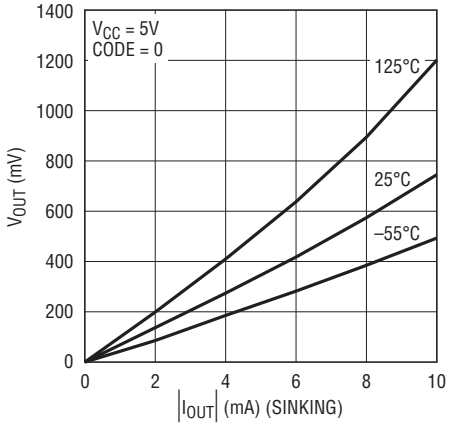
166560 G02

Minimum Supply Headroom vs Load Current (Output Sourcing)



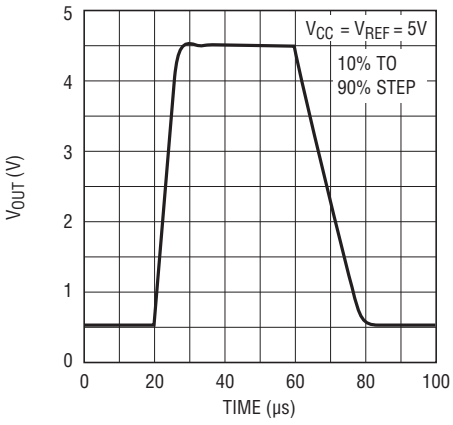
166560 G03

Minimum V_{OUT} vs Load Current (Output Sinking)



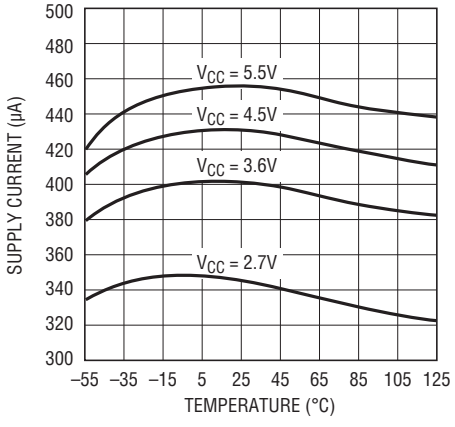
166560 G04

Large-Signal Step Response



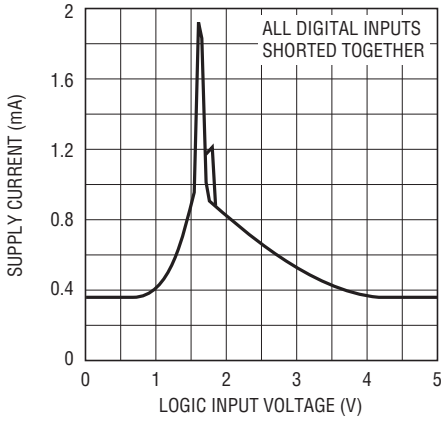
166560 G05

Supply Current vs Temperature



166560 G06

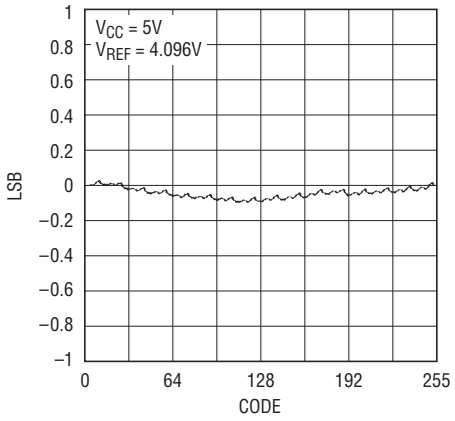
Supply Current vs Logic Input Voltage



166560 G07

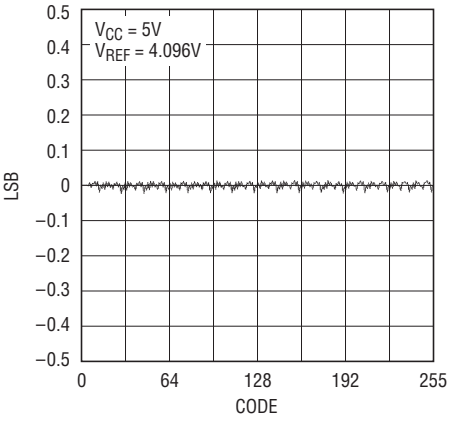
TYPICAL PERFORMANCE CHARACTERISTICS (LTC1665)

Integral Nonlinearity (INL)



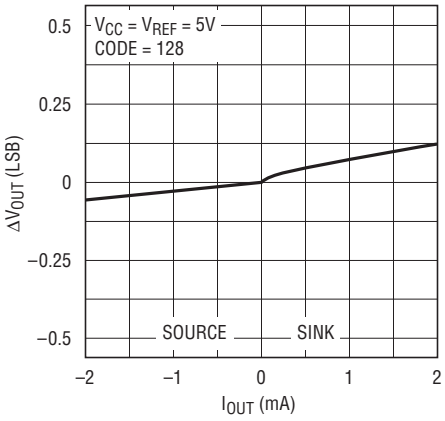
1665/60 G08

Differential Nonlinearity (DNL)



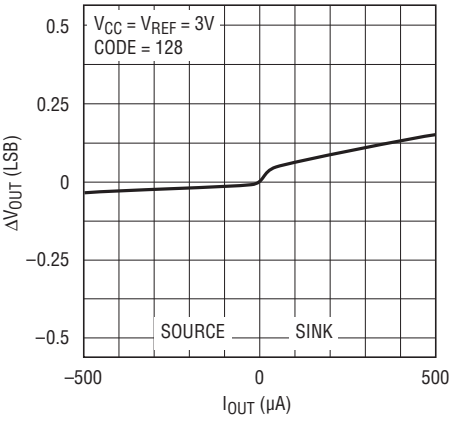
166560 G09

Load Regulation vs Output Current



166560 G10

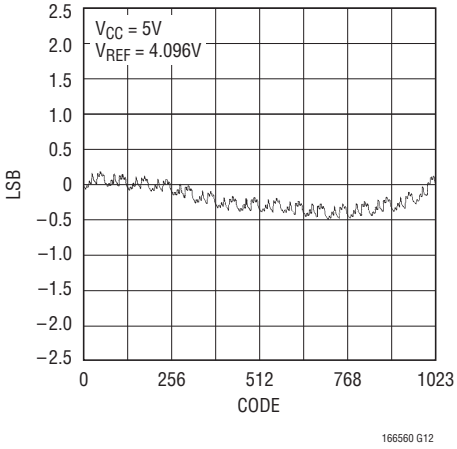
Load Regulation vs Output Current



166560 G11

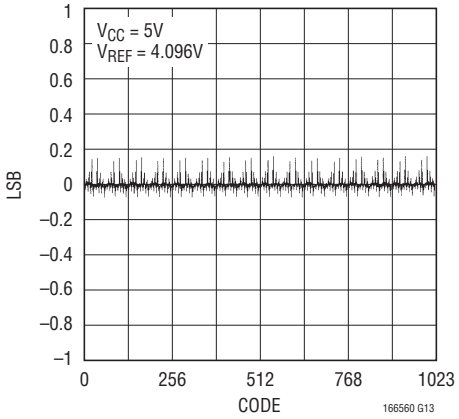
TYPICAL PERFORMANCE CHARACTERISTICS (LTC1660)

Integral Nonlinearity (INL)



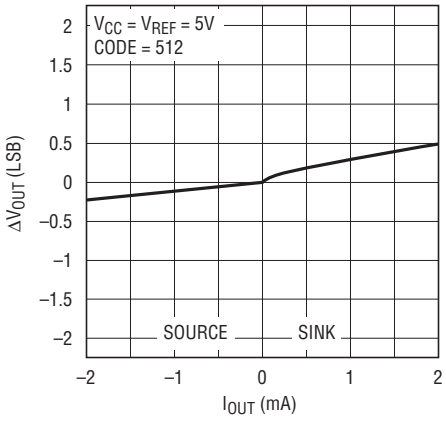
166560 G12

Differential Nonlinearity (DNL)



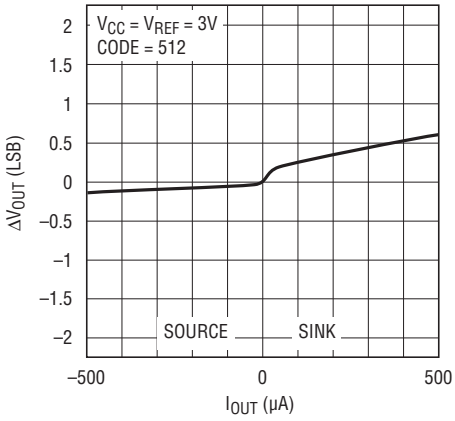
166560 G13

Load Regulation vs Output Current



166560 G14

Load Regulation vs Output Current



166560 G15

PIN FUNCTIONS (LTC1665/LTC1660)

GND (Pin 1): System Ground.

$V_{OUT\ A}$ to $V_{OUT\ H}$ (Pins 2-5 and 12-15): DAC Analog Voltage Outputs. The output range is

$$0 \text{ to } \left(\frac{255}{256}\right) V_{REF} \text{ for the LTC1665}$$

$$0 \text{ to } \left(\frac{1023}{1024}\right) V_{REF} \text{ for the LTC1660}$$

REF (Pin 6): Reference Voltage Input. $0V \le V_{REF} \le V_{CC}$.

$\overline{CS}$/LD (Pin 7): Serial Interface Chip Select/Load Input. When $\overline{CS}$/LD is low, SCK is enabled for shifting data on D_{IN} into the register. When $\overline{CS}$/LD is pulled high, SCK is disabled and data is loaded from the shift register into the specified DAC register(s), updating the analog output(s). CMOS and TTL compatible.

SCK (Pin 8): Serial Interface Clock Input. CMOS and TTL compatible.

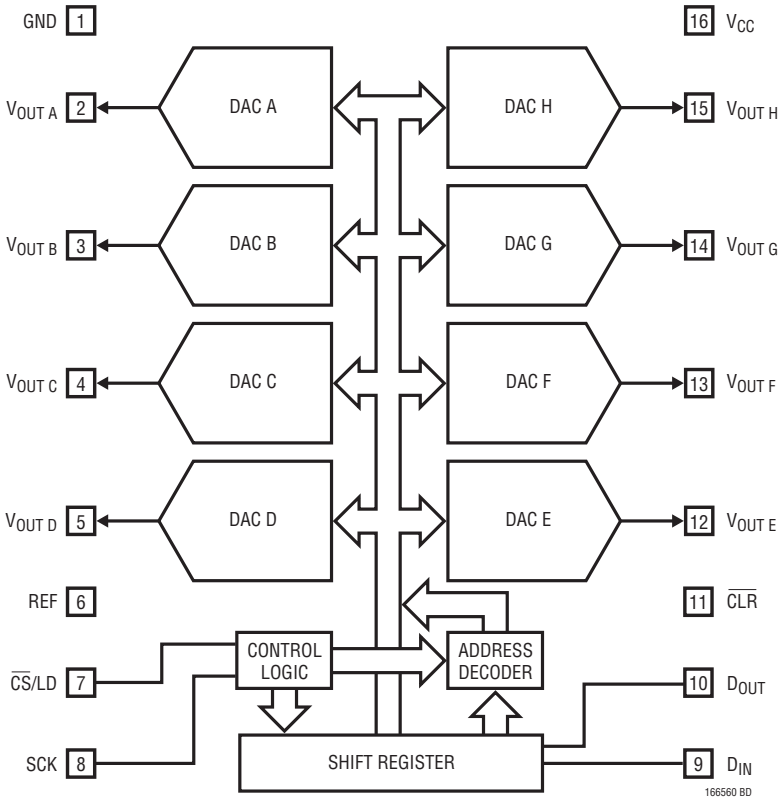
D_{IN} (Pin 9): Serial Interface Data Input. Data on the D_{IN} pin is shifted into the 16-bit register on the rising edge of SCK. CMOS and TTL compatible.

D_{OUT} (Pin 10): Serial Interface Data Output. Data appears on D_{OUT} 16 positive SCK edges after being applied to D_{IN}. May be tied to D_{IN} of another LTC1665/LTC1660 for daisy-chain operation. CMOS and TTL compatible.

$\overline{CLR}$ (Pin 11): Asynchronous Clear Input. All internal shift and DAC registers are cleared to zero at the falling edge of the $\overline{CLR}$ signal, forcing the analog outputs to zero scale. CMOS and TTL compatible.

V_{CC} (Pin 16): Supply Voltage Input. $2.7V \le V_{CC} \le 5.5V$.

BLOCK DIAGRAM



TIMING DIAGRAM

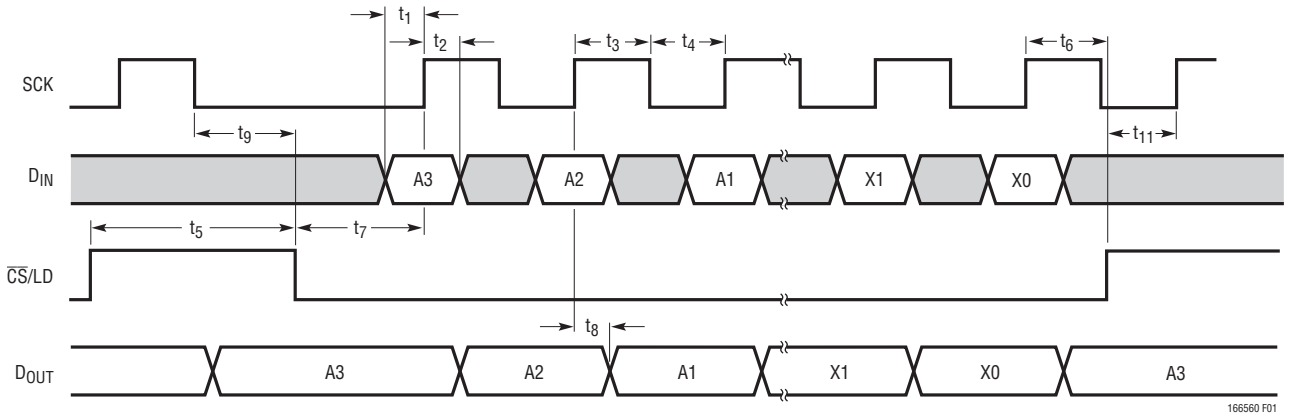


Figure 1

OPERATION

Transfer Function

The transfer function is:

$$V_{OUT(IDEAL)} = \left(\frac{k}{256}\right) V_{REF} \text{ for the LTC1665}$$

$$V_{OUT(IDEAL)} = \left(\frac{k}{1024}\right) V_{REF} \text{ for the LTC1660}$$

where k is the decimal equivalent of the binary DAC input code and V_{REF} is the voltage at REF (Pin 6).

Power-On Reset

The LTC1665 clears the outputs to zero scale when power is first applied, making system initialization consistent and repeatable.

Power Supply Sequencing

The voltage at REF (Pin 6) should be kept within the range $-0.2V \le V_{REF} \le V_{CC} + 0.2V$ (see Absolute Maximum Ratings). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at V_{CC} (Pin 16) is in transition.

Serial Interface

Referring to Figure 2a (2b): With $\overline{CS}$/LD held low, data on the D_{IN} input is shifted into the 16-bit shift register on the positive edge of SCK. The 4-bit DAC address, A3-A0, is loaded first (see Table 2), then the 8-bit (10-bit) input code, D7-D0 (D9-D0), ordered MSB-to-LSB in each case. Four (two) don't-care bits, X3-X0 (X1-X0), are loaded last. When the full 16-bit input word has been shifted in, $\overline{CS}$/LD is pulled high, loading the DAC register with the word and causing the addressed DAC output(s) to update. The clock is disabled internally when $\overline{CS}$/LD is high. Note: SCK must be low before $\overline{CS}$/LD is pulled low.

The buffered serial output of the shift register is available on the D_{OUT} pin, which swings from GND to V_{CC}. Data appears on D_{OUT} 16 positive SCK edges after being applied to D_{IN}.

Multiple LTC1665/LTC1660's can be controlled from a single 3-wire serial port (i.e., SCK, D_{IN} and $\overline{CS}$/LD) by using the included "daisy-chain" facility. A series of *m* chips is configured by connecting each D_{OUT} (except the last) to D_{IN} of the next chip, forming a single 16*m*-bit shift register. The SCK and $\overline{CS}$/LD signals are common to all chips in the chain. In use, $\overline{CS}$/LD is held low while *m* 16-bit words are clocked to D_{IN} of the first chip; $\overline{CS}$/LD is then pulled high, updating all of them simultaneously.

OPERATION

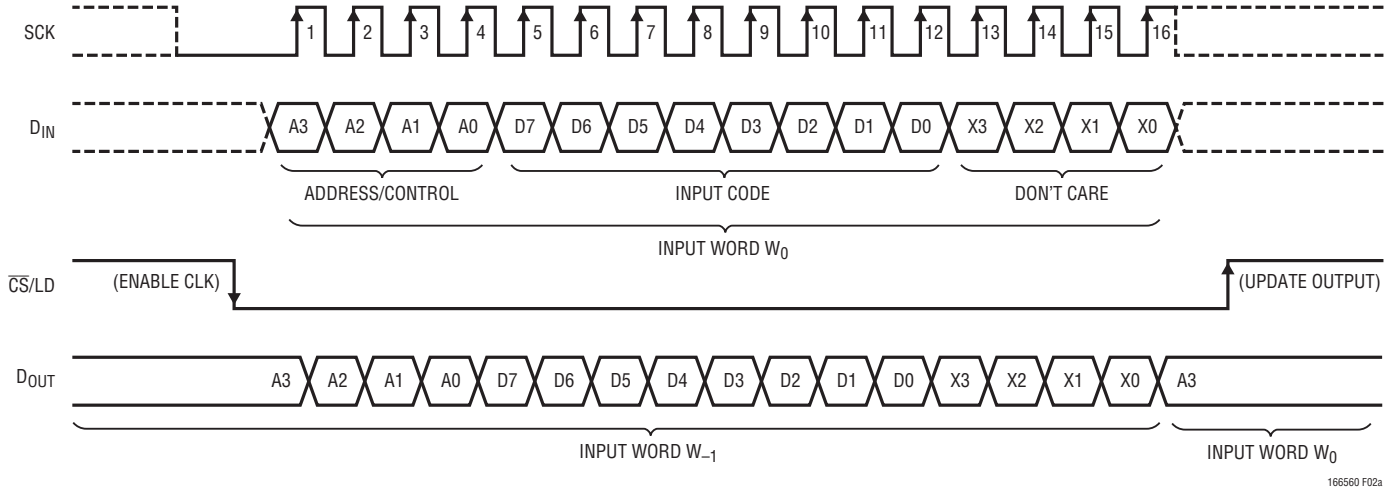


Figure 2a. LTC1665 Register Loading Sequence

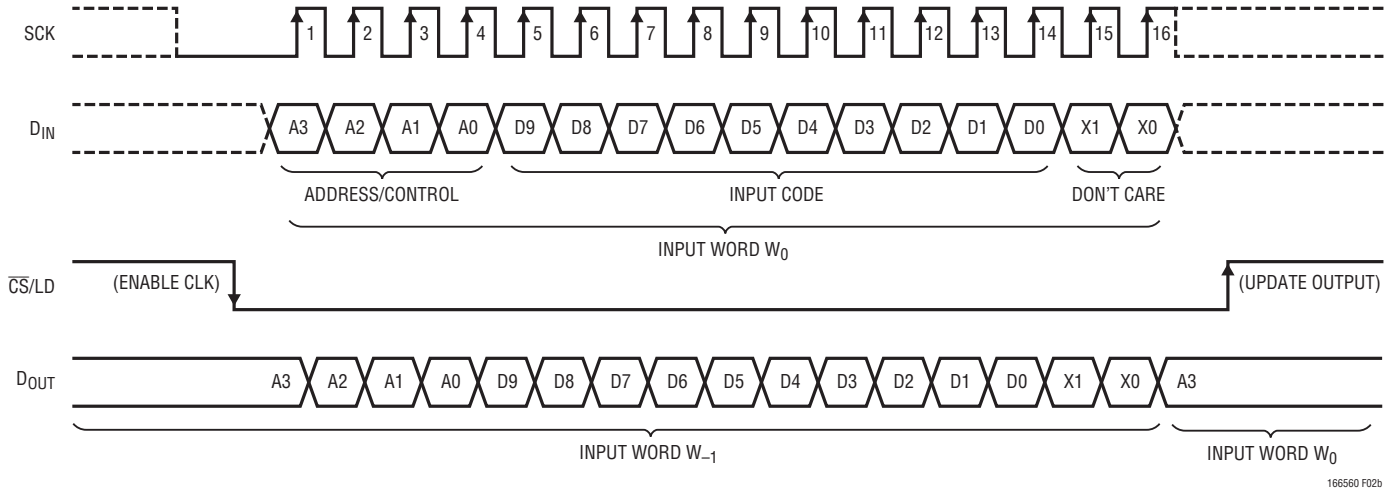


Figure 2b. LTC1660 Register Loading Sequence

Table 1a. LTC1665 Input Word

A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	X3	X2	X1	X0
ADDRESS/CONTROL				INPUT CODE								DON'T CARE			

Table 1b. LTC1660 Input Word

A3	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X1	X0
ADDRESS/CONTROL				INPUT CODE										DON'T CARE	

Sleep Mode

DAC address 1110_b is reserved for the special Sleep instruction (see Table 2). In this mode, the digital interface stays active while the analog circuits are disabled; static power consumption is thus virtually eliminated. The reference input and analog outputs are set in a high impedance state and all DAC settings are retained in memory so that when Sleep mode is exited, the outputs of DACs not updated by the Wake command are restored to their last active state.

OPERATION

Table 2. DAC Address/Control Functions

ADDRESS/CONTROL					
A3	**A2**	**A1**	**A0**	**DAC STATUS**	**SLEEP STATUS**
0	0	0	0	No Change	Wake
0	0	0	1	Load DAC A	Wake
0	0	1	0	Load DAC B	Wake
0	0	1	1	Load DAC C	Wake
0	1	0	0	Load DAC D	Wake
0	1	0	1	Load DAC E	Wake
0	1	1	0	Load DAC F	Wake
0	1	1	1	Load DAC G	Wake
1	0	0	0	Load DAC H	Wake
1	0	0	1	No Change	Wake
1	0	1	0	No Change	Wake
1	0	1	1	No Change	Wake
1	1	0	0	No Change	Wake
1	1	0	1	No Change	Wake
1	**1**	**1**	**0**	**No Change**	**Sleep**
1	1	1	1	Load **ALL** DACs with Same 8/10-Bit Code	Wake

Sleep mode is initiated by performing a load sequence to address 1110_b (the DAC input word D7-D0 [D9-D0] is ignored). Once in Sleep mode, a load sequence to any other address (including "No Change" addresses 0000_b and $1001\text{-}1101_b$) causes the LTC1665/LTC1660 to Wake. It is possible to keep one or more chips of a daisy chain in continuous Sleep mode by giving the Sleep instruction to these chips each time the active chips in the chain are updated.

Voltage Outputs

Each of the eight rail-to-rail output amplifiers contained in these parts can source or sink up to 5mA. The outputs swing to within a few millivolts of either supply rail when unloaded and have an equivalent output resistance of 85Ω when driving a load to the rails. The output amplifiers are stable driving capacitive loads up to 1000pF.

A small resistor placed in series with the output can be used to achieve stability for any load capacitance. A 1µF load can be successfully driven by inserting a 20Ω resistor; a 2.2µF load needs only a 10Ω resistor. In either case, larger values of resistance, capacitance or both may be safely substituted for the values given.

Rail-to-Rail Output Considerations

In any rail-to-rail output voltage DAC, the output is limited to voltages within the supply range.

If the DAC offset is negative, the output for the lowest codes limits at 0V as shown in Figure 3b.

Similarly, limiting can occur near full scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 3c. No full-scale limiting can occur if V_{REF} is less than V_{CC} – FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

OPERATION

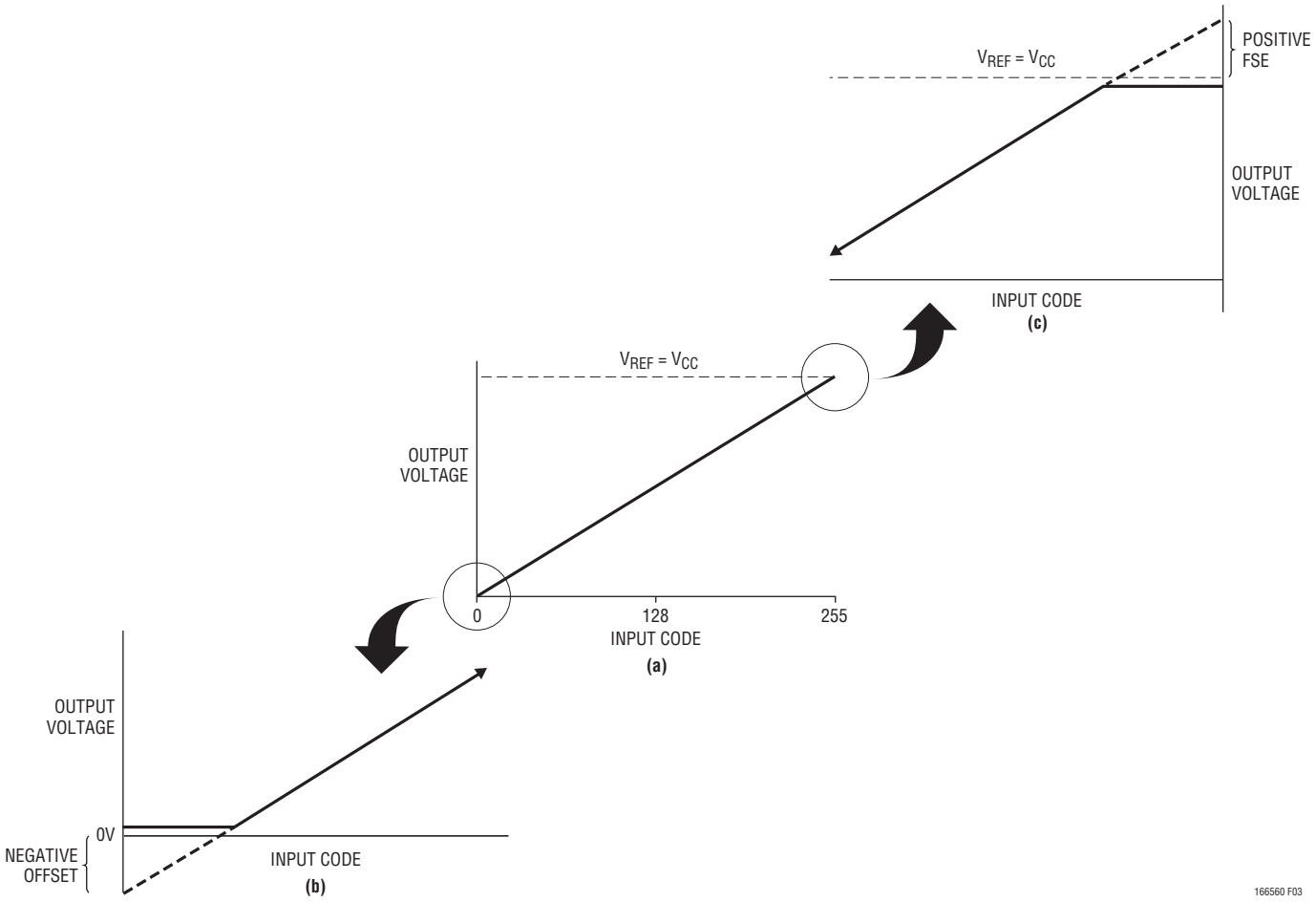
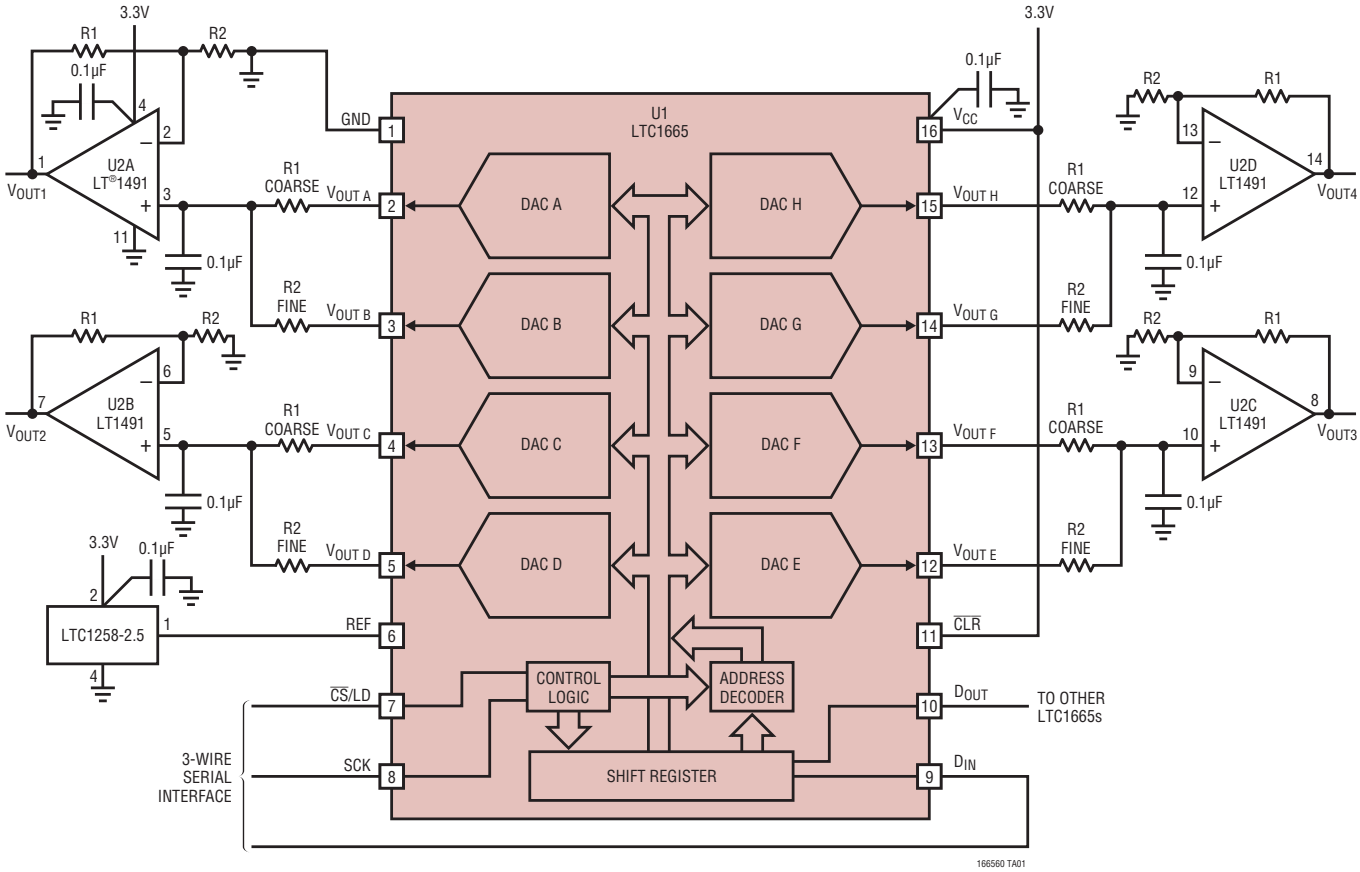


Figure 3. Effects of Rail-to-Rail Operation On a DAC Transfer Curve. (a) Overall Transfer Function (b) Effect of Negative Offset for Codes Near Zero Scale (c) Effect of Positive Full-Scale Error for Input Codes Near Full Scale When $V_{REF} = V_{CC}$

TYPICAL APPLICATIONS

A Low Power Quad Trim Circuit with Coarse/Fine Adjustment



R2 >> R1

$V_{OUT\ 1} = V_{OUT\ A} + \left(\frac{R1}{R2}\right) V_{OUT\ B}$

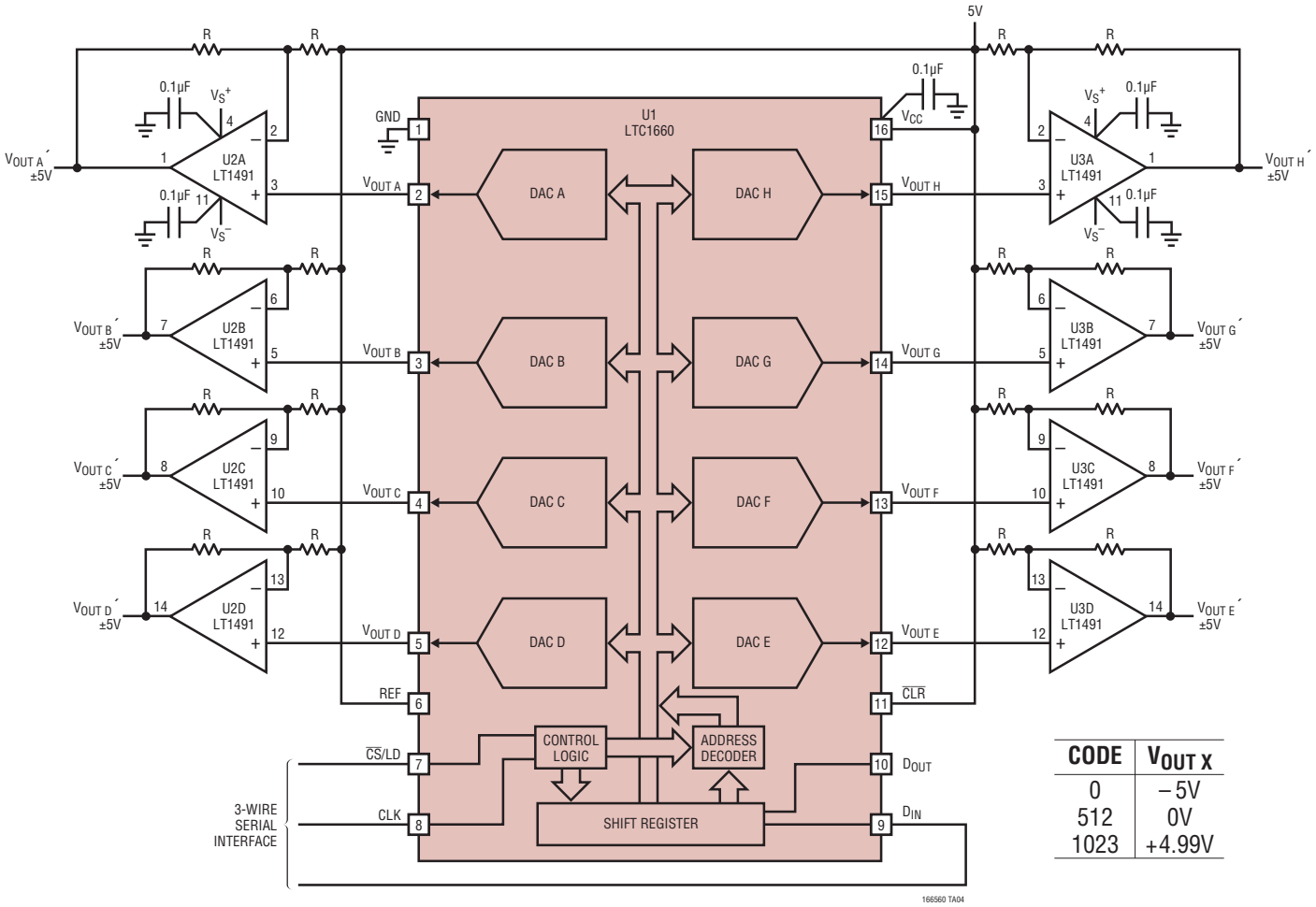
Similarly $V_{OUT\ 2}$, $V_{OUT\ 3}$, $V_{OUT\ 4}$

Example: For R1 = 110Ω and R2 = 11k,

$V_{OUT\ 1} = V_{OUT\ A} + 0.01\ V_{OUT\ B}$

TYPICAL APPLICATIONS

An 8-Channel Bipolar Output Voltage Circuit Configuration

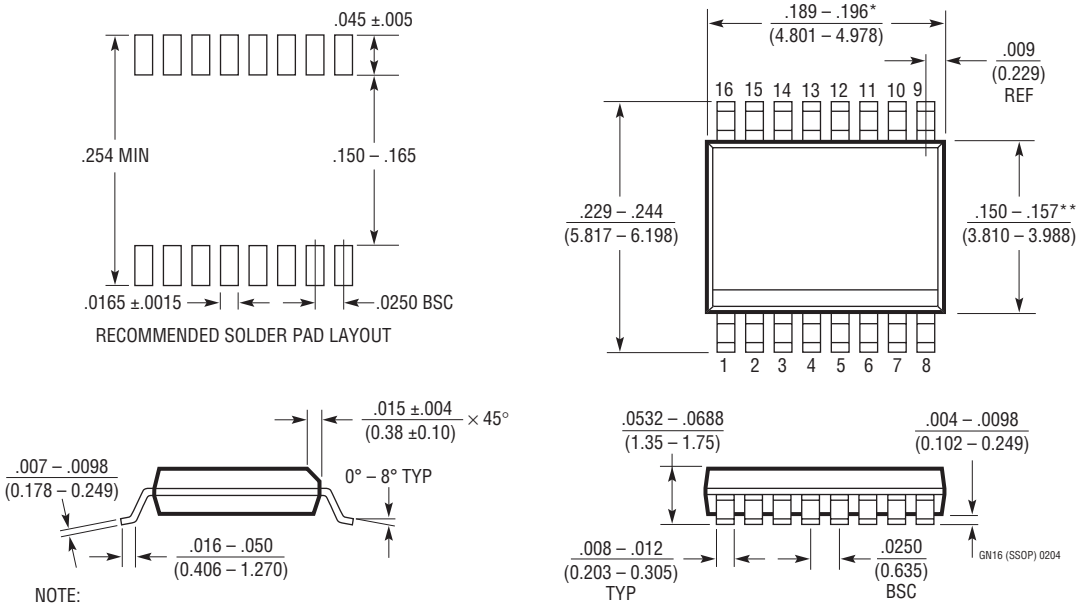


CODE	V_{OUT} X
0	–5V
512	0V
1023	+4.99V

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG #05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

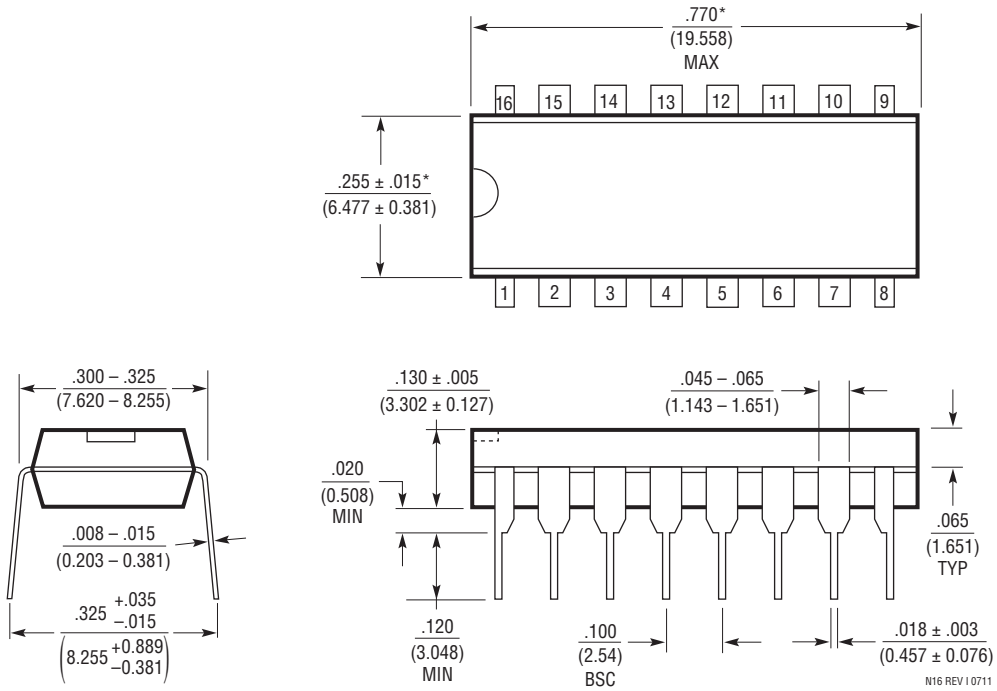
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

N Package
16-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510 Rev I)



NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	1/12	Removed Typical values in Timing Characteristics	3, 4