Low Quiescent Current Ideal Diode Controller

FEATURES

- **Reduces Power Dissipation by Replacing a Power Schottky Diode**
- **Low Quiescent Current: 5µA Operating**
- **Wide Operating Voltage Range: 2.5V to 80V**
- **Reverse Supply Protection to –28V**
- **No TVS Input Clamps Required**
- High Side External N-Channel MOSFET Drive
- Drives Back-to-Back MOSFETs for Inrush Control and Load Switching
- Shutdown Input for ON/OFF Control
- Fast Reverse Current Turn-Off within 1.5µs
- 8-Lead MSOP and 3mm × 3mm DFN Packages

APPLICATIONS

- Automotive Battery Protection
- Redundant Power Supplies
- Portable Instrumentation
- Solar Powered Systems
- Energy Harvesting Applications
- Supply Holdup

DESCRIPTION

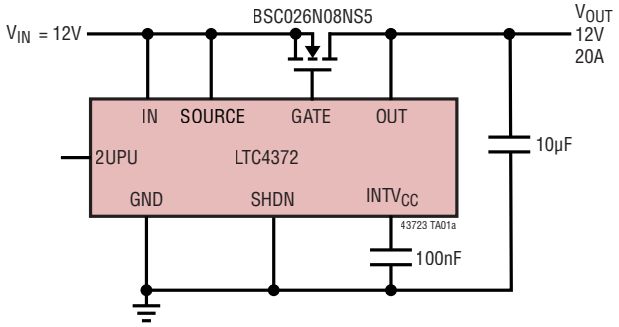
The LTC®4372/LTC4373 are positive high voltage ideal diode controllers that drive an external N-channel MOSFET to replace a Schottky diode. They control the forward voltage drop across the MOSFET to ensure current delivery or current transfer from one path to the other even at light loads.

A 5µA operating current achieves high efficiency for intermittent load applications or always-on backup power supplies. If a power source fails or is shorted, a fast turn-off minimizes reverse current transients. The LTC4372/LTC4373 control back-to-back N-channel MOSFETs for inrush current control and load switching.

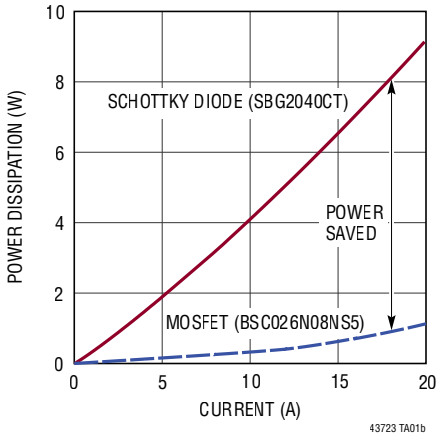
The LTC4372's SHDN pin keeps the MOSFET off and reduces the quiescent current to 3.5µA. The LTC4373 has a UV pin for undervoltage monitoring while the $\overline{\text{UVOUT}}$ pin provides hysteresis adjustment and status information. During undervoltage, the back-to-back MOSFETs are cut off and quiescent current reduces to 0.5µA.

TYPICAL APPLICATION

12V, 20A Reverse Battery Protection



Power Dissipation vs Load Current



ABSOLUTE MAXIMUM RATINGS

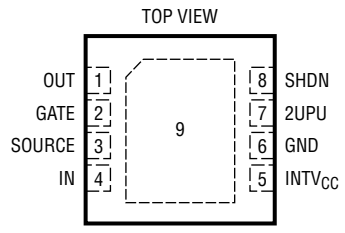
(Notes 1, 2)

IN, SOURCE .....–28V to 100V
OUT.....–2V to 100V
IN – OUT .....–100V to 100V
IN – SOURCE .....–1V to 100V
SOURCE – OUT.....–100V to 100V
GATE – SOURCE (Note 3) ..... –0.3V to 10V
SHDN, UV, 2UPU, $\overline{\text{UVOUT}}$..... –0.3V to 100V
$INTV_{CC}$ ..... –0.3V to 6V

Operating Ambient Temperature Range
LTC4372C, LTC4373C..... 0°C to 70°C
LTC4372I, LTC4373I .....–40°C to 85°C
LTC4372H, LTC4373H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 Sec)
MSOP Package .....300°C

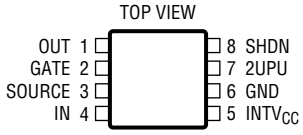
PIN CONFIGURATION

LTC4372



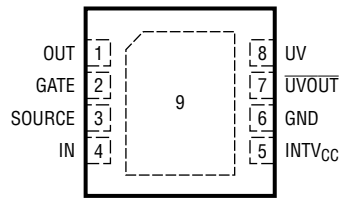
DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 9) PCB CONNECTION TO GND IS OPTIONAL

LTC4372



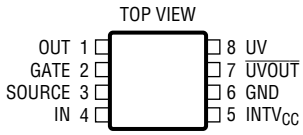
MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 163°C/W

LTC4373



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 9) PCB CONNECTION TO GND IS OPTIONAL

LTC4373



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 163°C/W

ORDER INFORMATION

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4372CDD#PBF	LTC4372CDD#TRPBF	LHGR	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4372IDD#PBF	LTC4372IDD#TRPBF	LHGR	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4372HDD#PBF	LTC4372HDD#TRPBF	LHGR	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4372CMS8#PBF	LTC4372CMS8#TRPBF	LTHGS	8-Lead Plastic MSOP	0°C to 70°C
LTC4372IMS8#PBF	LTC4372IMS8#TRPBF	LTHGS	8-Lead Plastic MSOP	–40°C to 85°C
LTC4372HMS8#PBF	LTC4372HMS8#TRPBF	LTHGS	8-Lead Plastic MSOP	–40°C to 125°C
LTC4373CDD#PBF	LTC4373CDD#TRPBF	LHMQ	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4373IDD#PBF	LTC4373IDD#TRPBF	LHMQ	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4373HDD#PBF	LTC4373HDD#TRPBF	LHMQ	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4373CMS8#PBF	LTC4373CMS8#TRPBF	LTHMR	8-Lead Plastic MSOP	0°C to 70°C
LTC4373IMS8#PBF	LTC4373IMS8#TRPBF	LTHMR	8-Lead Plastic MSOP	–40°C to 85°C
LTC4373HMS8#PBF	LTC4373HMS8#TRPBF	LTHMR	8-Lead Plastic MSOP	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges.
Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. IN = SOURCE =12V, SHDN = 0V, UV = 2V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Voltage Range		●	2.5		80	V
$V_{IN(UVL)}$	Input Supply Undervoltage Lockout	IN Rising	●	1.9	2.1	2.45	V
$\Delta V_{IN(HYST)}$	Input Supply Undervoltage Lockout Hysteresis				80		mV
V_{INTVCC}	Internal Regulator Voltage	I_{INTVCC} = 0 to –10µA	●	2.5	3.5	4.5	V
I_Q	Total Supply Current $I_Q = I_{IN} + I_{SOURCE} + I_{OUT}$	Diode Control: I_{GATE} = –0.1µA Single or Back-to-Back MOSFETs (Note 4) (C-Grade, I-Grade) (H-Grade) Shutdown: SHDN = 2V, UV = 0V Single MOSFET Back-to-Back MOSFETs Reverse Current: ΔV_{SD} = –0.1V, IN = 12V Single MOSFET Back-to-Back MOSFETs	 ● ● ● ● ● ●	 	 5 5 3.5 0.5 20 10	 10 20 10 2.5 30 20	 µA µA µA µA µA µA
I_{OUT}	OUT Current	IN – OUT = 4V IN – OUT = –4V	● ●		–0.5 1.8	–10 5	µA µA
I_{NEG}	IN + SOURCE Current During Reverse Battery	IN = SOURCE = –24V, OUT = 24V	●		–1	–5	mA
$I_{OUT(NEG)}$	OUT Current During Reverse Battery	IN = SOURCE = –24V, OUT = 24V	●		0.3	0.5	mA
$\Delta V_{SD(T)}$	Source-Drain Threshold (IN-OUT)	Low to High. Activates $I_{GATE(UP)}$	●	20	30	45	mV
$\Delta V_{GATE(H)}$	Maximum GATE Drive (GATE-SOURCE)	IN ≤ 5V, ΔV_{SD} = 0.1V, I_{GATE} = 0, –1µA IN > 5V, ΔV_{SD} = 0.1V, I_{GATE} = 0, –1µA	● ●	4.5 10	6.5 11.7	10 16	V V
$I_{GATE(UP)}$	GATE Pull-Up Current	GATE = IN, ΔV_{SD} = 0.1V	●	–15	–20	–25	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. IN = SOURCE =12V, SHDN = 0V, UV = 2V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{GATE(DOWN)}$	GATE Pull-Down Current	Shutdown: SHDN = 2V, UV = 0V, ΔV_{GATE} = 5V	●	0.5	1	3	mA
		Reverse Current: ΔV_{SD} = –0.1V, ΔV_{GATE} = 5V	●	70	130	230	mA
		Reverse Battery: IN = SOURCE = –7V, GATE = –3V	●	70	130	230	mA
$V_{GATE(NEG)}$	GND-GATE clamp	I_{GATE} = 10mA (Note 3)	●	–28	–32	–35	V
$V_{SOURCE(TH)}$	Reverse SOURCE Threshold for GATE Off	GATE = 0V (Note 5)	●	–0.9	–1.8	–2.7	V
t_{OFF}	Gate Turn-Off Delay Time	ΔV_{SD} = Step 0.1V to –0.8V, C_{GATE} = 0pF, ΔV_{GATE} <1V	●		0.5	1.5	µs
t_{ON}	Gate Turn-On Delay Time	IN = 12V, SOURCE = OUT = 0V, ΔV_{GATE} > 4.5V, C_{GATE} = 0pF, SHDN = 2V to 0V, UV = 0V to 1.25V	●	100	500	1200	µs
LTC4372							
I_{2UPU}	2UPU Pull-Up Current		●	–1	–2	–3	µA
V_{SHDN}	SHDN Threshold	SHDN Falling	●	1	1.2	1.4	V
$V_{SHDN(HYST)}$	SHDN Threshold Hysteresis		●	2	15	40	mV
I_{SHDN}	SHDN Leakage Current	SHDN = 1.2V	●		±1	±50	nA
LTC4373							
V_{UV}	UV Threshold	UV Falling	●	1.174	1.191	1.208	V
$V_{UV(HYST)}$	UV Threshold Hysteresis		●	2	15	40	mV
$I_{UV(LK)}$	UV Leakage Current	UV = 1.2V	●		±1	±50	nA
$I_{\overline{UVOUT}(LK)}$	$\overline{UVOUT}$ Leakage Current	UV = 2V, $\overline{UVOUT}$ = 1.2V					
		(C-Grade, I-Grade)	●		±1	±50	nA
		(H-Grade)	●		±1	±200	nA
$R_{UVOUT\#}$	$\overline{UVOUT}$ Output Low Resistance	I = 2mA	●		140	500	Ω
t_{UV}	Under Voltage Detect to $\overline{UVOUT}$ Assert Low	UV = Step 1.25V to 1.1V	●	10	50	300	µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 3: An internal clamp limits the GATE pin to a minimum of 10V above SOURCE or 100V above GND. A second internal clamp limits the GATE pin to a minimum of 28V below GND. Driving this pin to voltages beyond the clamp may damage the device.

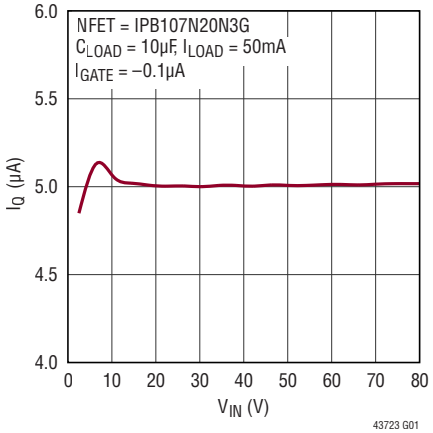
Note 4: When testing the single MOSFET configuration, IN is connected to SOURCE. When testing the back-to-back MOSFET configuration, SOURCE is left unconnected.

Note 5: SOURCE ≤ –1.8V triggers a 130mA pull-down current from GATE to SOURCE. An internal clamp limits the GATE pin to a minimum of 28V below GND. Driving SOURCE to voltages beyond the clamp may damage the device.

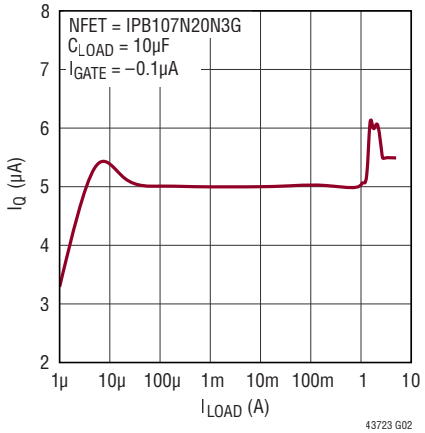
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. IN = SOURCE = 12V, SHDN = 0V, UV = 2V unless otherwise noted.

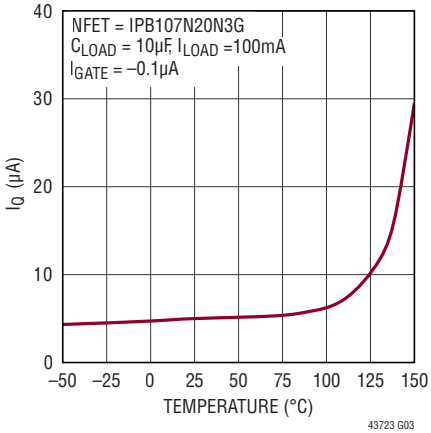
Total Supply Current vs V_{IN}



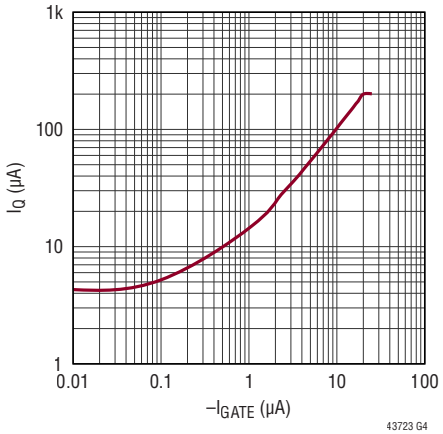
Total Supply Current vs Load Current



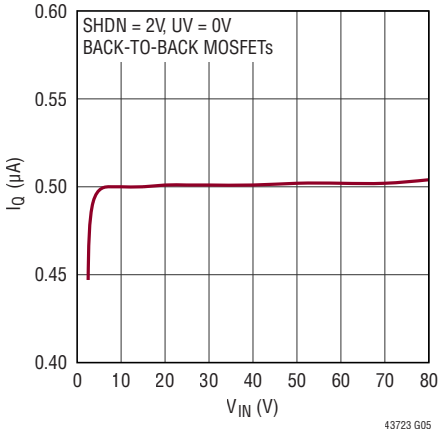
Total Supply Current vs Temperature



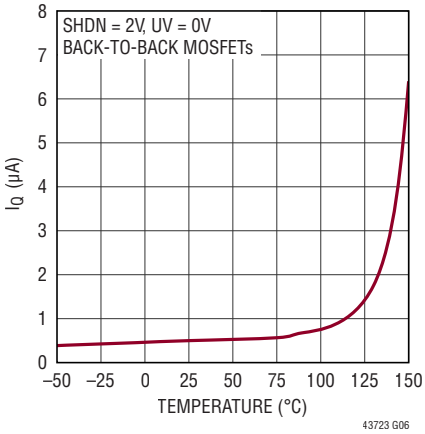
Total Supply Current vs GATE Leakage



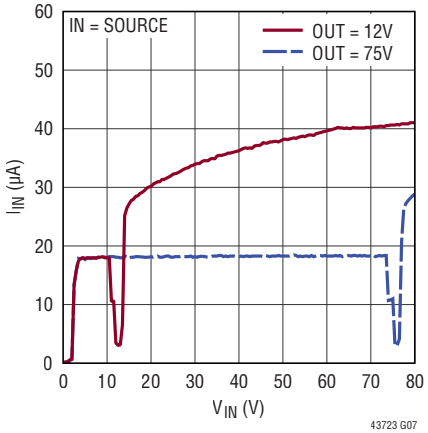
Total Supply Current (Shutdown) vs V_{IN}



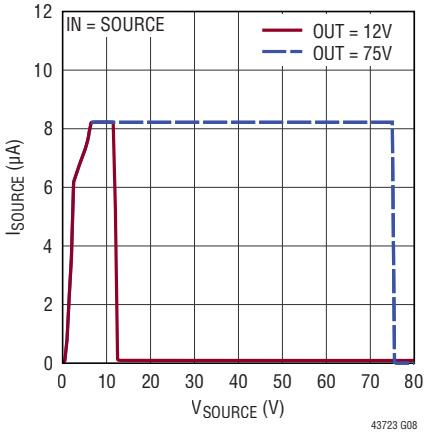
Total Supply Current (Shutdown) vs Temperature



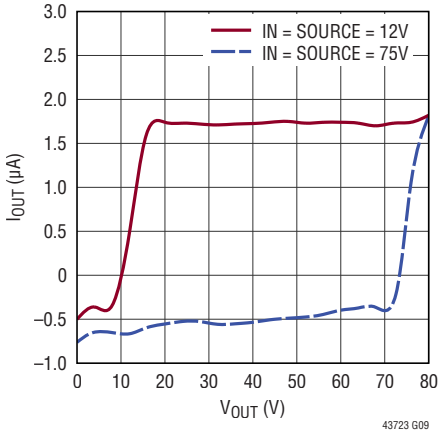
IN Current



SOURCE Current



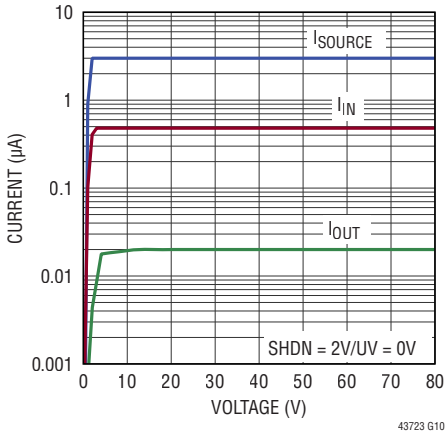
OUT Current



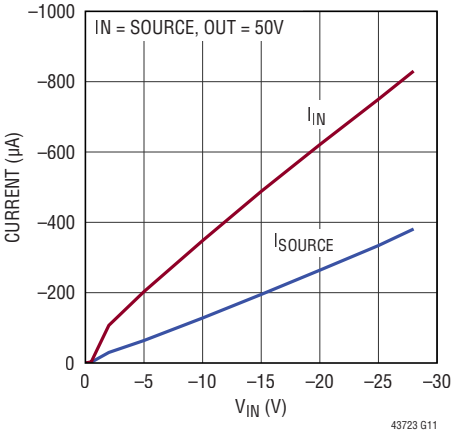
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. IN = SOURCE = 12V, SHDN = 0V, UV = 2V unless otherwise noted.

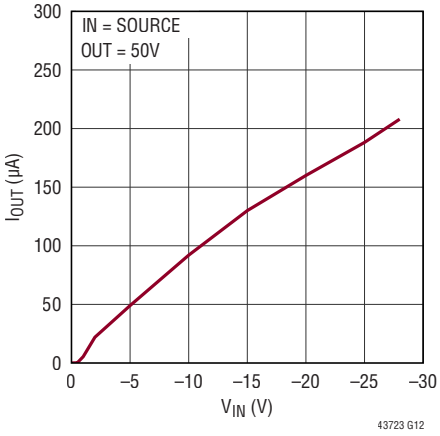
Pin Current at Shutdown



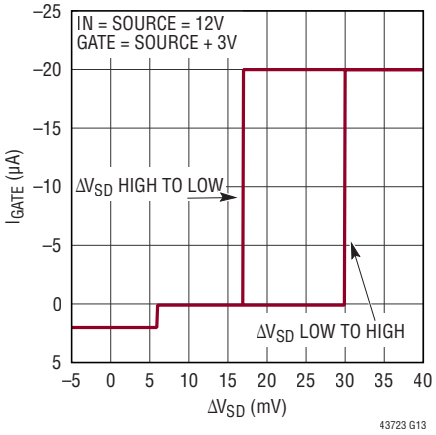
Pin Current at Negative Input



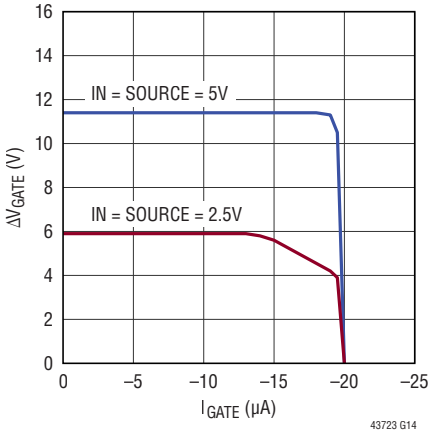
OUT Current at Negative Input



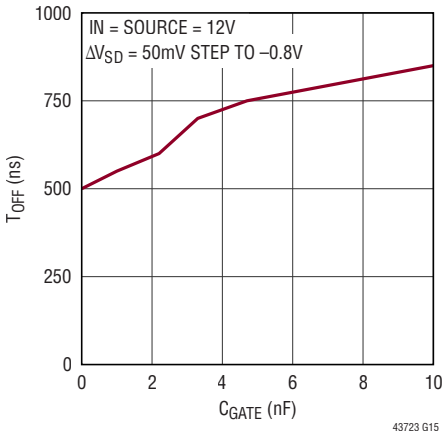
GATE Current vs Forward Voltage Drop



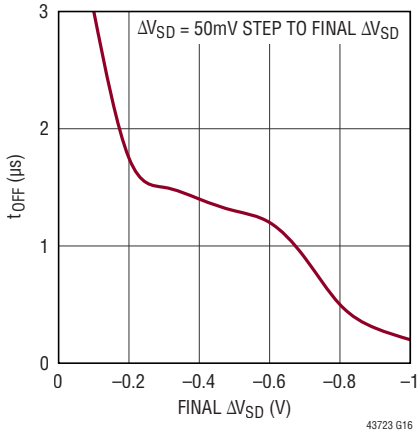
ΔV_{GATE} (Average) vs GATE Leakage



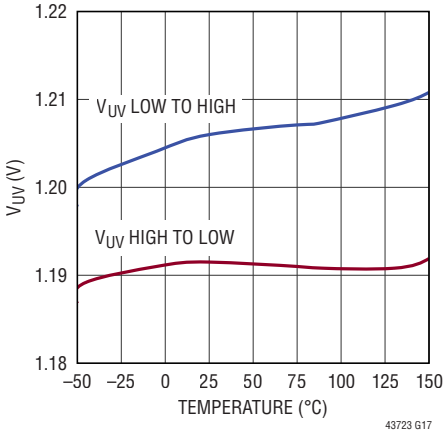
GATE Turn-Off Time vs GATE Capacitance



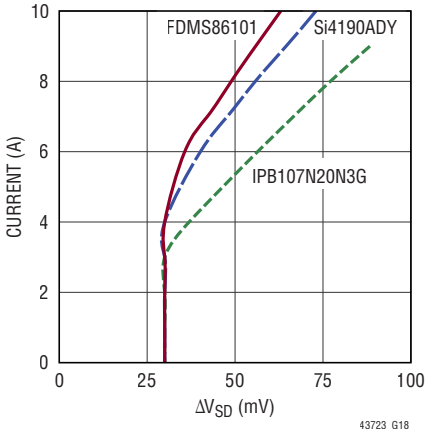
GATE Turn-Off Time vs Forward Overdrive



UV Threshold vs Temperature



Load Current vs V_{FWD}



PIN FUNCTIONS

Exposed Pad (DD Package Only) : Exposed pad may be left open or connected to device ground.

GATE: MOSFET Gate Drive Output. The LTC4372/LTC4373 control the gate of the MOSFET to maintain the voltage drop between 0mV to 30mV using a pulsed control method. If reverse current flows, a fast pull-down circuit connects GATE to SOURCE within 0.5µs, turning off the MOSFET.

GND: Device Ground.

IN: Voltage Sense and Supply Voltage. IN is the anode of the ideal diode. The voltage sensed at this pin is used to control the MOSFET gate for forward voltage regulation and reverse current turn-off. The positive supply input ranges from 2.5V to 80V for normal operation. It can go below GND by up to 28V during a reverse battery condition without damaging the part.

$INTV_{CC}$: Internal 3V Supply Decoupling Output. Connect a 0.1µF or larger capacitor to this pin. An external load of less than 10µA can be connected at this pin.

OUT: MOSFET Drain Voltage Sense. OUT is the cathode of the ideal diode and the common output when multiple LTC4372/LTC4373's are configured as an ideal diode-OR. It connects to the drain of the N-channel MOSFET. The voltage sensed at this pin is used to control the MOSFET gate for forward voltage regulation and reverse current turn-off. OUT is used as the supply to hold the MOSFET off when IN is not available (below UVLO). Connect a 10µF or larger capacitor to this pin.

SHDN (LTC4372): Shutdown Control Input. The LTC4372 can be shut down to a low current mode by pulling SHDN above 1.215V. Connect to GND if unused.

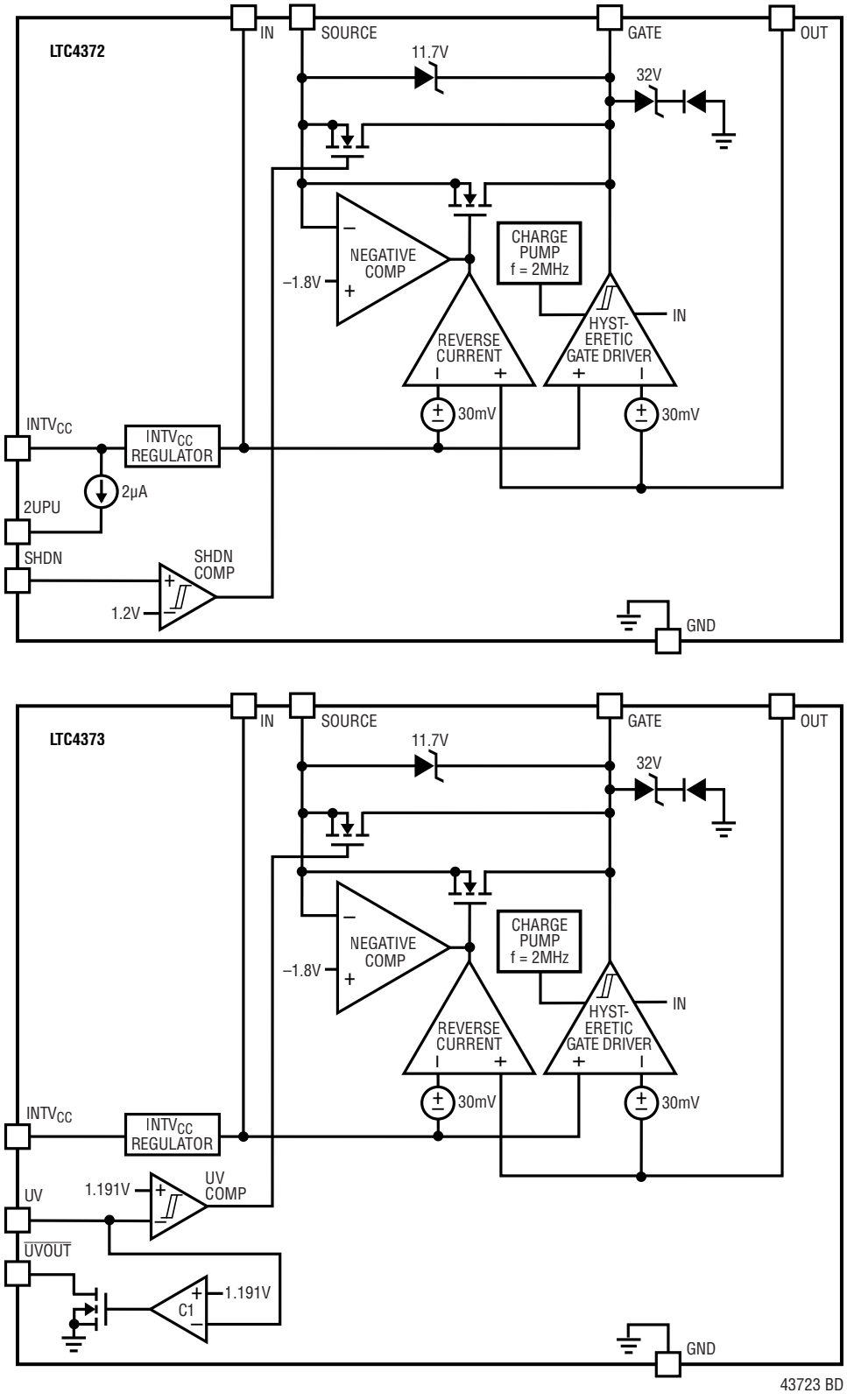
SOURCE: MOSFET Source Connection. SOURCE is the return path of the GATE fast pull-down. Connect this pin as close as possible to the source of the external N-channel MOSFET.

2UPU (LTC4372): 2µA Pull-Up Output. This pin has a 2µA pull-up to $INTV_{CC}$. It can be connected to SHDN to facilitate on/off control of the LTC4372 by a microcontroller's open-drain output. If unused, leave open or connect to $INTV_{CC}$.

$\overline{UVOUT}$ (LTC4373): UV Status Output. Open Drain output that pulls low when UV goes below 1.191V (V_{UV}) and goes high impedance when UV exceeds 1.191V. $\overline{UVOUT}$ can be used to adjust hysteresis for the UV monitor. This pin may be left open or connected to GND if unused.

UV (LTC4373): Undervoltage Detection Input. The LTC4373 goes into a low current shutdown mode when UV is below 1.191V. Connect to $INTV_{CC}$ if unused.

BLOCK DIAGRAM



OPERATION

Blocking diodes are commonly placed in series with supply inputs for ORing redundant supplies and protecting against supply reversal. The LTC4372/LTC4373 replace the diodes such as in portable equipment and automotive applications with N-channel MOSFETs acting as ideal diodes. The forward voltage drop reduces as shown in Figure 1, a feature that is readily appreciated at low input voltages where headroom is tight.

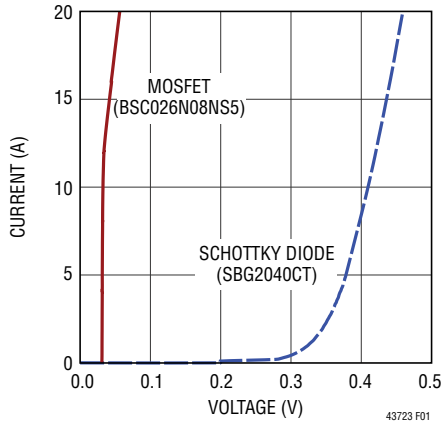


Figure 1. Forward Voltage Drop Comparison Between MOSFET and Schottky Diode

As a result of this lower forward voltage drop, there is a dramatic reduction in power loss achieved in a practical application as shown in the Typical Application curve on Page 1. This represents significant savings in board area by greatly reducing heat sinking requirements of the pass device. In addition to these two desirable properties, the LTC4372/LTC4373 feature a low operating current (5µA) and shutdown current (0.5µA). This increases efficiency in applications where the ideal diode is used for intermittent loads or always on standby channels, making the LTC4372/LTC4373 suitable for battery powered applications in the portable instrumentation, automotive and renewable energy fields.

The source of the external MOSFET is connected to IN and SOURCE while its drain is connected to OUT. The LTC4372/LTC4373 control the gate of the MOSFET to regulate the voltage drop across the pass transistor to less than 30mV.

In the event of a rapid drop in input voltage, such as an input short-circuit fault or negative-going voltage spike, reverse current temporarily flows through the MOSFET. This current is provided by any load capacitance and by other supplies or batteries that feed the output in diode-OR applications. The reverse current comparator quickly responds to this condition by turning the MOSFET off in 500ns. This fast turn-off prevents the reverse current from ramping up to a damaging level, thus minimizing the disturbance to the output bus.

IN, SOURCE and GATE are protected against reverse inputs of up to –28V. The negative comparator detects negative input potentials at SOURCE and quickly connects GATE to SOURCE, turning off the MOSFET and isolating the load from the negative input.

For the LTC4372, driving SHDN high pulls the MOSFET gate down to SOURCE with a 1mA pull-down. I_Q reduces to 0.5µA for a back-to-back MOSFET configuration and GATE is held low with a 3µA pull-down to GND. When SHDN goes low, the LTC4372 ramps GATE up to turn on the external MOSFET. 2UPU has a 2µA pull-up to $INTV_{CC}$ which can be connected to SHDN to facilitate on/off control by a microcontroller's open-drain output.

The LTC4373 can monitor the input voltage via an external resistive voltage divider to UV. When UV goes below 1.191V, GATE pulls down to SOURCE with a 1mA pull-down and $\overline{UVOUT}$ pulls low. I_Q reduces to 0.5µA for a back-to-back MOSFET configuration and GATE is held low with a 3µA pull down to GND. When UV recovers above $V_{UV} + V_{UV(HYST)}$, the LTC4373 ramps GATE up to turn on the external MOSFET. An optional resistor can be connected between UV and $\overline{UVOUT}$ to configure an external hysteresis to override $V_{UV(HYST)}$.

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The LTC4372/LTC4373 operate from 2.5V to 80V and withstands an absolute maximum range of –28V to 100V without damage. In automotive applications the LTC4372/LTC4373 can operate through load dump, cold crank and two-battery jump starts, and survive reverse battery connections while protecting the load.

A 12V/20A ideal diode application is shown in Figure 2. The following sections cover power-on, ideal diode operation, shutdown and various faults that the LTC4372/LTC4373 detect and act upon.

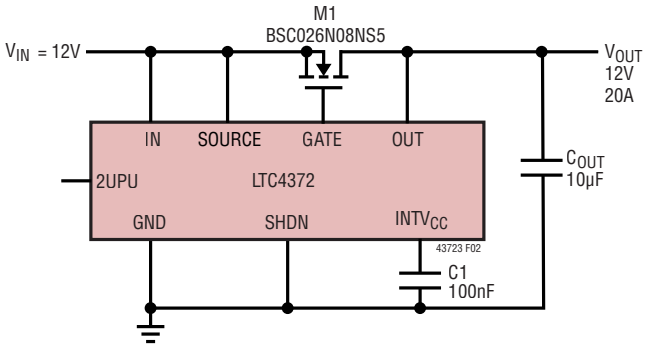

Figure 2. 12V/20A Ideal Diode with Reverse Input Protection

Power-On and Ideal Diode Operation

When power is applied, the initial load current flows through the body diode of the MOSFET M1. When IN exceeds the UVLO level of 2.1V and SHDN is low or UV is high, the LTC4372/LTC4373 begin operation. An internal charge pump asserts a 20µA pull-up on GATE to enhance the MOSFET. To achieve a low supply current, the LTC4372/LTC4373 employ a pulsed control style of operation where the internal charge pump is not always on. Instead, the charge pump periodically wakes up to recharge GATE after it droops from leakage to keep $\Delta V_{SD} \leq 30mV$. This pulsed control creates a voltage ripple at OUT even with a stable DC load. The amplitude of this ripple is dependent on gate leakage, GATE capacitance, the load condition and the size of the bypass capacitance at OUT. At low load or no-load condition, this ripple can increase to $30mV_{PK-PK}$. Figure 3 shows a typical OUT ripple at an ultralight I_{LOAD} of 1µA for the circuit shown in Figure 2.

With a moderate DC load, the ripple amplitude is about 10mVpk-pk. Figure 4 shows a typical OUT ripple at a moderate I_{LOAD} of 2A for the circuit shown in Figure 2.

Figure 5 shows a typical OUT ripple at an I_{LOAD} of 16A for the circuit shown in Figure 2.

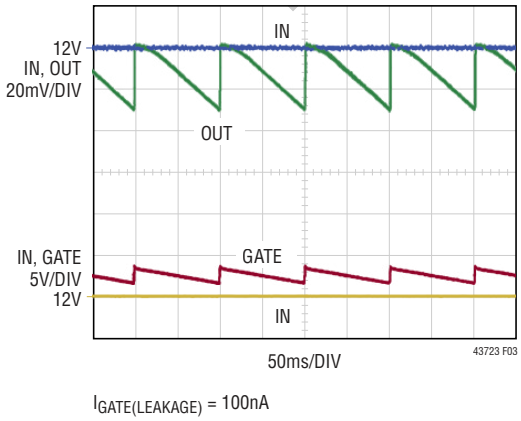

Figure 3. Regulating ΔV_{SD} at Low I_{LOAD} = 1µA

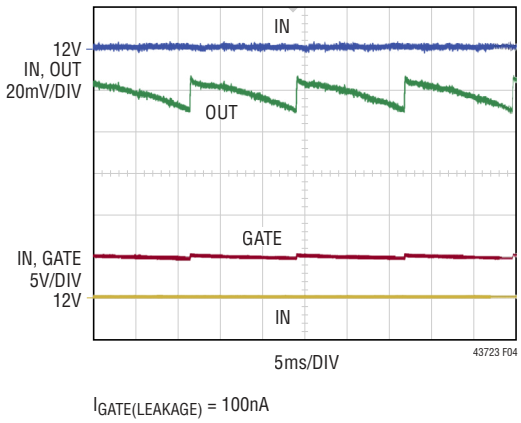

Figure 4. Regulating ΔV_{SD} at Moderate I_{LOAD} = 2A

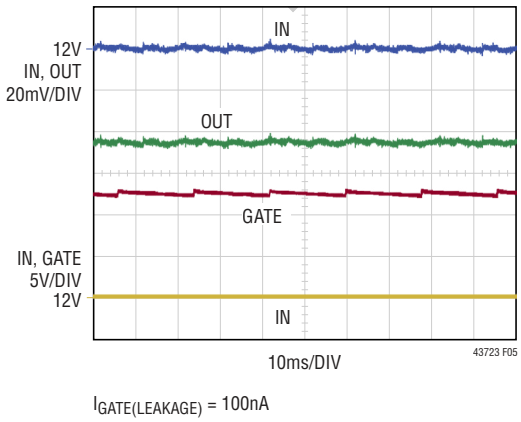

Figure 5. Regulating ΔV_{GATE} at High I_{LOAD} = 16A

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As the load current increases, GATE is driven higher and higher until a point is reached where ΔV_{GATE} reaches the maximum overdrive that the internal charge pump is capable of ($\Delta V_{GATE(H)}$) but ΔV_{SD} is still above 30mV. In this situation, the internal charge pump will periodically turn on to recharge GATE as needed to keep ΔV_{GATE} between $\Delta V_{GATE(H)}$ and $\Delta V_{GATE(H)}$ – 0.7V. ΔV_{SD} is then equal to $R_{DS(ON)} \bullet I_{LOAD}$. There is now insignificant ripple on OUT as the 0.7Vpk-pk ripple on ΔV_{GATE} has little effect on the MOSFET R_{ON}.

Achieving Low Average I_Q

To lower average I_Q in diode control mode when GATE is high, the LTC4372/LTC4373 operate by turning on the charge pump periodically. When in charge pump sleep mode, the I_Q is 3.5µA. Once the charge pump is turned on to deliver a current pulse to GATE, I_Q goes up to 300µA. The average I_Q will depend on how often the charge pump is turned on and this is affected by GATE leakage, GATE capacitance, OUT bypass capacitance and I_{LOAD}. To achieve the lowest possible average I_Q, minimize GATE leakage and ensure that GATE has a moderate capacitance (>1nF). If the C_{GS} of the MOSFET does not already exceed this, add a 1nF capacitor between GATE and SOURCE. C_{LOAD} may be placed nearer to the load but an OUT bypass capacitance of at least 10µF low ESR and ESL electrolytic or ceramic is required close to the drain pin of MOSFET M1 (see Figure 6a). Average I_Q for Diode Control mode can be estimated by Equation 1.

$$\text{AVERAGE}\, I_Q = 3.5 + \frac{I_{GATE(LEAKAGE)}}{I_{GATE(UP)}} \bullet 300\mu A \qquad (1)$$

The Typical Performance Characteristics section shows relationship of I_Q with $I_{GATE(LEAKAGE)}$ and I_{LOAD}.

MOSFET Selection

The LTC4372/LTC4373 drive N-channel MOSFETs to conduct the load current. The important characteristics of the MOSFET are the gate threshold voltage $V_{GS(TH)}$, the maximum drain-source voltage BV_{DSS} and on-resistance $R_{DS(ON)}$.

Gate drive is compatible with 4.5V logic-level MOSFETs over the entire operating range of 2.5V to 80V. In applications with supply voltages above 5V, standard 10V threshold MOSFETs may be used. An internal clamp limits the gate drive to 16V maximum between GATE and SOURCE.

The maximum allowable drain-source voltage, BV_{DSS}, must be higher than the power supply voltage. If the input is grounded, the full supply voltage will appear across the MOSFET. If a reverse battery is possible and the output is held up by a charged capacitor, battery or power supply, then the sum of the input and output voltages will appear across the MOSFET and BV_{DSS} must be higher than $V_{OUT}+|V_{IN}|$.

The MOSFET's on-resistance, $R_{DS(ON)}$, directly affects the forward voltage drop and power dissipation during a heavy load. Desired forward voltage drop (V_{FWD}) should be less than that of a diode for reduced power dissipation; 50mV is a good starting point. Since the LTC4372/LTC4373 drop at least 30mV across the MOSFET, a very low $R_{DS(ON)}$ may be wasted. Choose a MOSFET using Equation 2.

$$R_{DS(ON)} < \frac{V_{FWD}}{I_{LOAD}} \qquad (2)$$

The resulting power dissipation is shown in Equation 3.

$$P_d = I_{LOAD}^2 \bullet R_{DS(ON)} \qquad (3)$$

Input Short-Circuit Faults

Input short-circuits that cause reverse current to flow can occur in many ways. Some examples include PCB traces getting accidentally shorted or bypass capacitors in the upstream power supply failing shorted. The LTC4372/LTC4373 utilize the external MOSFETs to add rugged input short-circuit protection without using large TVS clamps or capacitors.

Figure 6a models a low impedance input short with a switch. When the short-circuit switch closes, reverse current builds up in L_{IN}, L_{OUT} and M1 in the direction shown. The LTC4372/LTC4373 detect the reverse current quickly and activate the internal 130mA GATE to SOURCE pulldown current to turn M1 off. The reverse current build up

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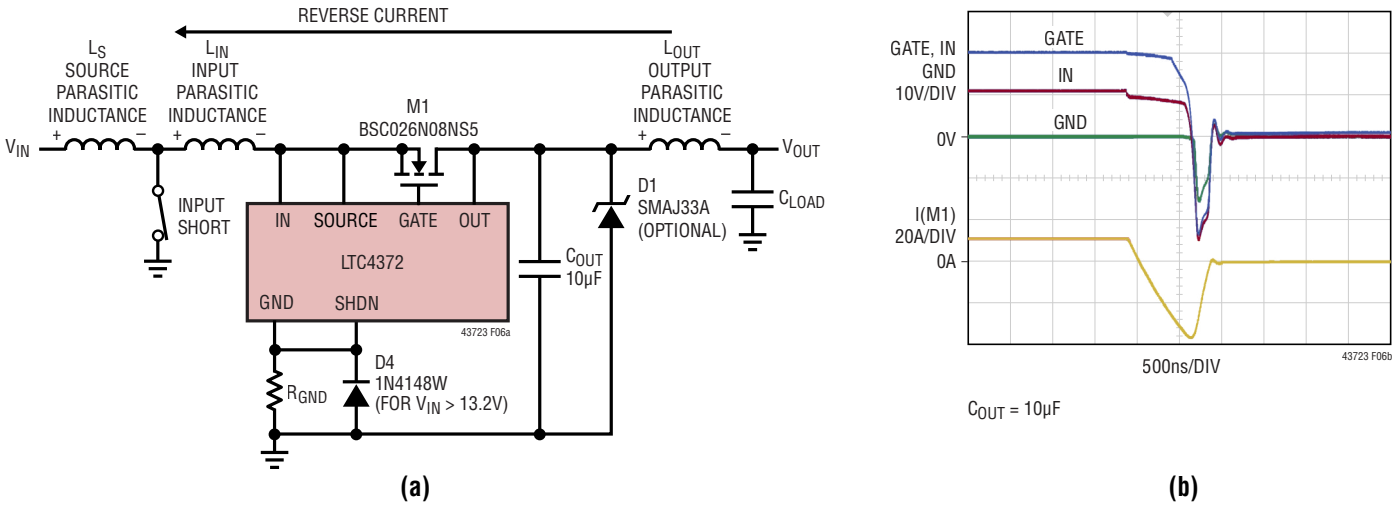

Figure 6. Reverse Recovery Produces Inductive Spikes at IN, SOURCE and OUT. The Polarity of Inductive Spike is Shown Across Parasitic Inductances

in L_{IN} and L_{OUT} is interrupted and this causes IN to spike negative and OUT to spike positive. At OUT, C_{OUT} clamps the positive going spike caused by L_{OUT} and commutates $I(L_{OUT})$ to zero. At IN, the internal GND – GATE clamp asserts and holds GATE to 32V below GND, this causes M1 to turn back on as IN/SOURCE undershoots below GATE. The current in L_{IN} is diverted by M1 to C_{OUT} and safely commutates to zero as shown in the short-circuit transient of Figure 6b. If these transients cause too large of a ΔV at OUT, increase the capacitance of C_{OUT} or add a TVS D1.

If a low source resistance power supply drives V_{IN}, large currents can build up in L_S during the short-circuit. When the short-circuit goes away, $I(L_S)$ can cause IN and SOURCE to spike positive until it is held by M1 body diode to C_{OUT}. This fast slew rate at SOURCE can cause a large shoot-through current to flow into the part from SOURCE to GND potentially causing damage. Adding an external R_{GND} will limit this current to a safe level.

For applications where IN ≤ 13.2V, a 0805 size 100Ω for R_{GND} is sufficient. For applications where IN > 13.2V, a larger value R_{GND}, 1k, is necessary. To keep GND from going too negative when the GND – GATE clamp turns on, a fast recovery diode like the 1N4148W is placed in parallel with the 1k R_{GND}.

For back-to-back MOSFET applications where SOURCE is not driven by V_{IN}, R_{GND} is not needed. R_{GND} can also be omitted for a single MOSFET application driven by a power supply with a large source impedance. V_{IN} collapses during the short-circuit and cannot build up current in L_S. SOURCE will not see fast slew rates when the short-circuit goes away.

Using the external MOSFETs to commutate the parasitic inductor currents during an input short-circuit is feasible with input voltages up to 33V. This ensures that during the transient, the IN – OUT Absolute Maximum Voltage of ±100V is not exceeded. During the short-circuit transient, the MOSFET V_{DS} sees $|V_{GND}|+|V_{GATE(NEG)}|+V_{TH(M1)}+V_{OUT}$. Choose the MOSFET BV_{DSS} accordingly. For other techniques to protect the LTC4372/LTC4373 during input short-circuits see the Design Examples section.

Reverse Input Protection

Negative voltages at IN can also occur if a battery is plugged in backwards or a negative supply is inadvertently connected. Figure 7 shows the waveforms when the application circuit in Figure 2 is hot plugged to –24V. Due to the parasitic inductance in between input and IN/SOURCE, the voltages at the pins can ring significantly below –24V. Similar to the input short-circuit situation, the GND – GATE clamp causes M1 to divert the current in the parasitic inductances to C_{OUT}. The GND – GATE clamp limits the maximum DC negative voltage that the Figure 2 application can handle to –28V.

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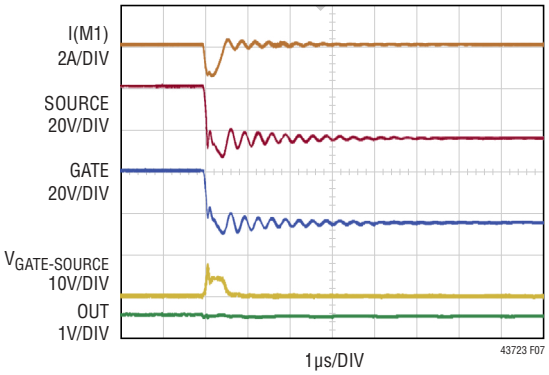


Figure 7. LTC4372/LTC4373 Handling Reverse Input

Paralleling Supplies

Multiple LTC4372/LTC4373's can be used to combine the outputs of two or more supplies for redundancy or for droop sharing, as shown in Figure 8. For redundant supplies, the supply with the highest output voltage sources most or all of the load current. Figure 9a and Figure 9b show the load transition between the two redundant power supplies.

Depending on INA and INB's supply impedances, slew rates and the transient response of the LTC4372/LTC4373, a transient reverse current might flow into lower

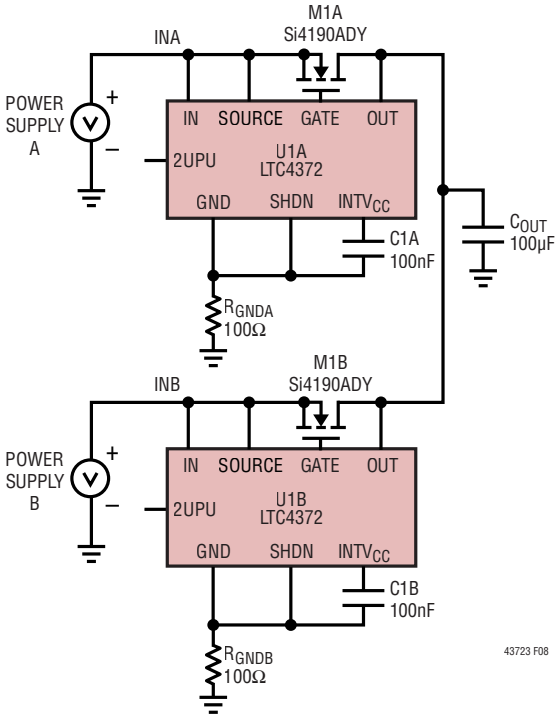
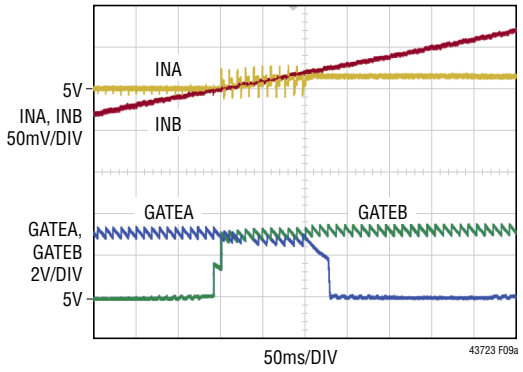
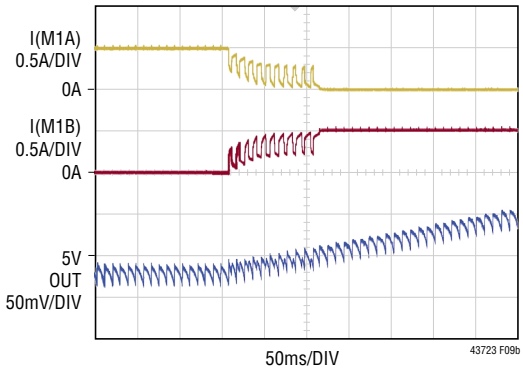


Figure 8. Redundant Power Supplies



(a)



$I_{GATEA(LEAKAGE)} = I_{GATEB(LEAKAGE)} = 100nA$

(b)

Figure 9. Load Transition of Redundant Power Supplies

supply (INA) from the supply ramping higher (INB). The reverse current may cause INA to rise, with the amount of voltage rise dependent on the input supply's impedance. The safest course of action is to use capacitors on the input supply whose voltage rating is higher than the highest voltage in the system, or to consider protecting these capacitors with a TVS, for example.

If the higher supply's input is shorted to ground while delivering load current, the flow of current temporarily reverses and flows backwards through the higher supply's MOSFET. The LTC4372/LTC4372 sense this reverse current and activate a fast pull-down to quickly turn off the MOSFET.

If all the load current was supplied by the channel that suffered the short, the output will fall until the body diode of the next MOSFET conducts. Meanwhile, the LTC4372/LTC4372 charge the MOSFET gate with 20µA until the forward drop

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is reduced to 30mV. If this supply was sharing load current at the time of the fault, its associated ORing MOSFET was already servoed to less than 30mV drop. In this case, the LTC4372/LTC4372 will simply drive the MOSFET gate higher to maintain a drop of 30mV at full load.

Load sharing can be accomplished if both power supply output voltages and source impedances are nearly equal. The 30mV regulation technique allows load sharing between outputs. The degree of sharing is a function of MOSFET $R_{DS(ON)}$, the source impedance of the supplies and their initial output voltages.

Using the LTC4372's SHDN and 2UPU

When SHDN goes high, the LTC4372 enters shutdown and asserts a 1mA pull-down between GATE and SOURCE to turn off the external MOSFET. It also turns off most of the internal circuitry, reducing I_{IN} to 0.5µA. GATE is held low with a 3µA pull-down to GND. If IN and SOURCE are connected together, I_Q = 3.0µA + 0.5µA = 3.5µA.

Shutting down the part does not interrupt forward current flow as a path is still present through M1's body diode. A second MOSFET may be added to block the forward path (see Figure 10). In this case, GATE and SOURCE are pulled to GND during shutdown. The 3µA pull-down on GATE is pinched off and I_Q = 0.5µA. With back-to-back MOSFETs, SHDN serves as an on/off control for the forward path, as well as enabling the diode function. When SHDN is driven low, the LTC4372 exits shutdown and re-enters ideal diode operation.

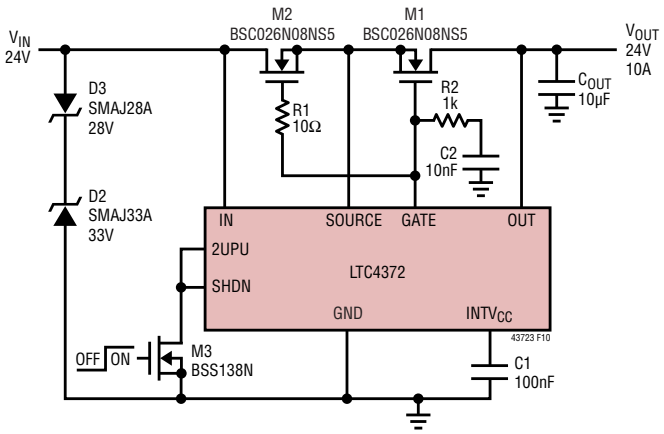

Figure 10. 24V Load Switch and Ideal Diode with Inrush Control and Reverse Input Protection

If SHDN is not needed, connect it to GND. SHDN may be driven with a 3.3V or 5V logic signal. It can also be driven with an open-drain or collector output with SHDN tied to 2UPU. 2UPU provides an internal pull up current of 2µA to $INTV_{CC}$. For higher pull-up currents, connect a resistor from SHDN to $INTV_{CC}$ (capable of supplying up to 10µA) or IN.

Load Switching and Inrush Control

By adding a second MOSFET as shown in Figure 10, the LTC4372/LTC4373 can be used to control power flow in the forward direction while retaining ideal diode behavior in the reverse direction. The body diodes of M1 and M2 prohibit current flow when the MOSFETs are off. M1 serves as the ideal diode while M2 acts as a switch to control forward power flow. ON/OFF control is provided by SHDN or UV. C2 and R2 may be added to further reduce inrush current. While C2 and R2 may be omitted if soft starting is not needed. R1 is necessary to prevent MOSFET parasitic oscillations and must be placed close to M2.

When SHDN is driven low or UV driven high and ΔV_{DS} > 30mV, GATE sources 20µA and gradually charges C2, pulling up both MOSFET gates. M2 operates as a source follower as shown in Equation 4.

$$I_{INRUSH} = \frac{C_{OUT}}{C2} \bullet 20\mu A \quad (4)$$

If $\Delta V_{DS} \leq$ 30mV, the LTC4372/LTC4373 stay activated but holds M1 and M2 off until the input exceeds the output by 30mV. In this way normal diode behavior of the circuit is preserved, but with soft starting when the diode turns on.

When SHDN is driven high or UV driven low, GATE pulls the MOSFET gates down quickly to SOURCE with a 1mA pull-down. Both forward and reverse paths are cut off and I_Q is reduced to 0.5µA.

Configuring LTC4373's UV and $\overline{UVOUT}$ for Voltage Monitoring

With back-to-back MOSFETs, the LTC4373 can implement voltage monitoring at IN. Connect a resistive voltage divider between IN and ground to bias UV. UV has a high to low threshold of 1.191V with 15mV of hysteresis. The UV hysteresis is around 1.3% referred to V_{UV}.

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When UV ramps high to low, the LTC4373 enters undervoltage mode and asserts a 1mA pull-down between GATE and SOURCE to turn off the external MOSFETs. It also turns off most of the internal circuitry, reducing I_Q to 0.5µA. When UV ramps low to high, the LTC4373 exits undervoltage mode and goes back into ideal diode operation.

Figure 11 demonstrates how UV can be used to monitor IN. For the UV pin, the maximum input leakage current is 50nA. For a maximum error of 1% due to leakage currents, the resistive voltage divider current I_{RVD} should be at least 100 times the sum of the leakage currents, or 5µA. The IN Undervoltage threshold (V_{H2L}) is used to calculate the value of R4, R5 and Undervoltage Recovery threshold (V_{L2H}) as shown in Equation 5.

$$V_{H2L} = V_{UV} \bullet \frac{R4+R5}{R4}$$
$$V_{L2H} = \left(V_{UV} + V_{UV(HYST)}\right) \bullet \frac{R4+R5}{R4} \quad (5)$$

For applications that require a higher and more accurate hysteresis, $\overline{UVOUT}$ can be used to program an external hysteresis to override the default hysteresis. Comparator C1 in the Block Diagram controls an internal 140Ω switch pulling down on $\overline{UVOUT}$. When UV ramps below 1.191V and trips C1, the switch pulls $\overline{UVOUT}$ low. When UV ramps above 1.191V and un-trips C1, the switch turns off and $\overline{UVOUT}$ goes high impedance. By connecting R6 between UV and $\overline{UVOUT}$, R4 and R5 implements V_{H2L} and V_{L2H}.

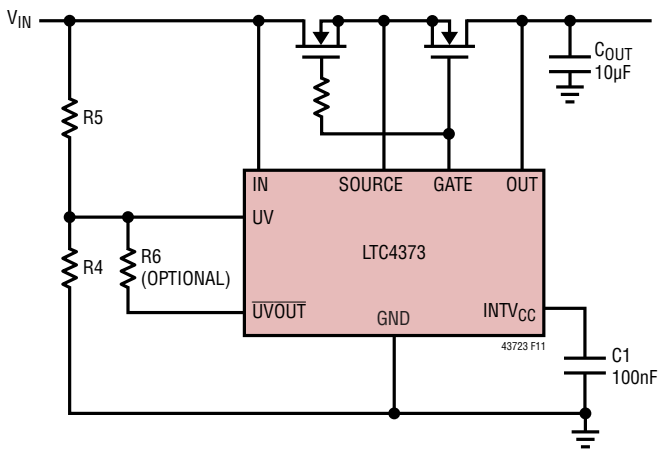

Figure 11. Configuration for Monitoring IN

Obtain R4 and R5 from Equation 5 and calculate R6 using Equation 6.

$$V_{H2L} = V_{UV} \bullet \frac{R4+R5}{R4}$$
$$V_{L2H} = V_{UV} \bullet \frac{R5+Rpa}{Rpa} \quad (6)$$
$$\text{where } Rpa = R4 \,//\, R6 = \frac{R4 \bullet R6}{R4+R6}$$

As long as the external hysteresis to be implemented exceeds 5% of V_{H2L}, Equation 6 can disregard the default UV hysteresis without affecting accuracy.

With $\overline{UVOUT}$ connected to the resistive voltage divider, the leakage current error needs to be re-visited. For the $\overline{UVOUT}$ pin, the maximum input leakage current below 85°C is 50nA. While IN ramps high to low, the resistive voltage divider sees the leakage currents from both UV and $\overline{UVOUT}$. This gives a total of 100nA of leakage currents. With 5µA through R4 and R5, this will add 2% inaccuracy to V_{H2L}. While IN ramps low to high, $\overline{UVOUT}$ is pulled low. The resistive voltage divider sees only the 50nA of leakage current from UV. With 5µA through R4 and R5, this will add 1% inaccuracy to V_{L2H}. To lower the leakage current error, increase I_{RVD}.

Layout Considerations

Connect IN, SOURCE and OUT as close as possible to the MOSFET source and drain pins. Keep the drain and source traces to the MOSFET wide and short to minimize resistive losses as shown in Figure 12. Place C_{OUT} close to the drain pin of MOSFET and keep the trace from LTC4372/LTC4373 GATE pin to MOSFET gate short and thin to minimize parasitic inductance and capacitance. This practice will reduce the chance of MOSFET parasitic oscillations. Place any surge suppressors and necessary transient protection components close to the LTC4372/LTC4373 using short lead lengths.

For the DFN package, pin spacing may be a concern at voltages greater than 30V. Check creepage and clearance guidelines to determine if this is an issue. To increase the effective pin spacing between high voltage and ground pins, leave the exposed pad connection open. Use no-clean flux to minimize PCB contamination.

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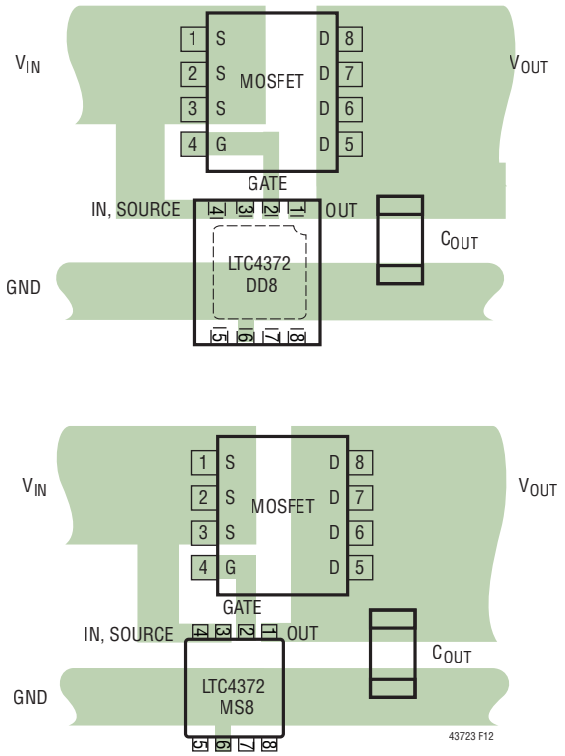

Figure 12. Layout, MS8 and DD8 Package

Design Examples

The following design example demonstrates the considerations involved in selecting components for a 12V system with 20A maximum load current (see Figure 2). First, choose the N-channel MOSFET. The 80V BSC026N08NS5 with $R_{DS(ON)}$ = 2.6mΩ(max) offers a good solution. The maximum voltage drop across is:

ΔV_{SD} = 20A • 2.6mΩ = 52mV

The maximum power dissipation in the MOSFET is:

P = 20A • 52mV = 1.04W

During input short-circuit voltage transients, using the GND – GATE clamp to hold GATE should keep IN, SOURCE, GATE and OUT within their Absolute Maximum Ratings. If there is a problem with SOURCE to GND shoot through current during input short-circuits, add a R_{GND} of 100Ω.

Figure 13 shows a high voltage application. For the 48V system, using the GND – GATE clamp to hold GATE during input short-circuit voltage transients can exceed IN – OUT's –100V absolute maximum voltage. D2 is added between IN and ground to clamp IN and SOURCE when they spike negative. During the input short-circuit transient, D2 diverts the reverse recovery current in the input parasitic inductances to ground while C_{OUT} does the same for the output parasitic inductances. The 100V, FDMS86101 with $R_{DS(ON)}$ = 8mΩ(max) can handle both the 5A load current as well as the input short-circuit voltage transients.

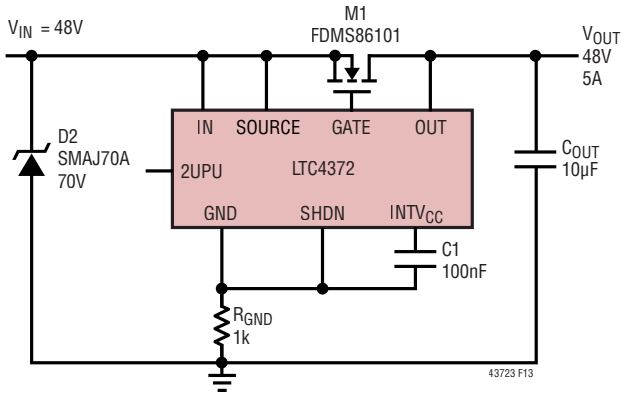

Figure 13. 48V Ideal Diode without Reverse Input Protection

Figure 14 shows a high voltage application with reverse battery protection. To handle a potential worst-case situation of –48V at the input side and 48V at the output side, the BV_{DSS} of the external MOSFET must be greater than 48V + 48V = 96V with allowance. Choose the 200V, IPB107N20N3G in the TO-263 package with $R_{DS(ON)}$ = 10.7mΩ(max).

When IN is –48V and OUTPUT is 48V, D3 breaks down and clamps IN – GND at about –6V. The MOSFET is held off and isolates the load from the negative input. D1 and R7 clamps OUT – GND to about 70V. The combination of D1, D2, D3 and R7 clamps IN – OUT to about 76V.

During an input short-circuit, M1 drain spikes positive and IN spikes negative. D2, D3 and D4 commutates the reverse recovery current in the input parasitic inductances while C_{OUT} does the same for the output parasitic inductances. D1, D2, D3, D4, R7 and R8 clamp IN, SOURCE, OUT and GND to within their Absolute Maximum Ratings.

During normal ideal diode operation with GATE high, D4, C3 and C4 help to handle I_Q pulsating between 300µA (charging GATE) and 3.5µA (charge pump sleep mode) while D1, D2 and D3 draw no current.

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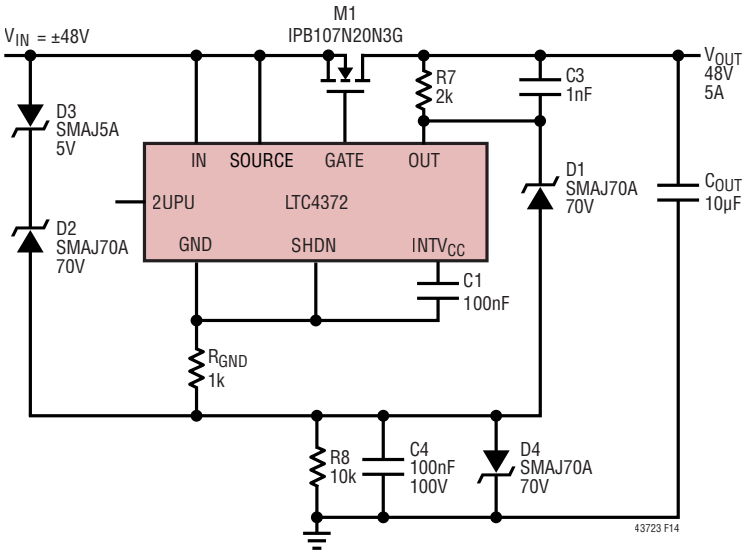

Figure 14. 48V Ideal Diode with Reverse Input Protection

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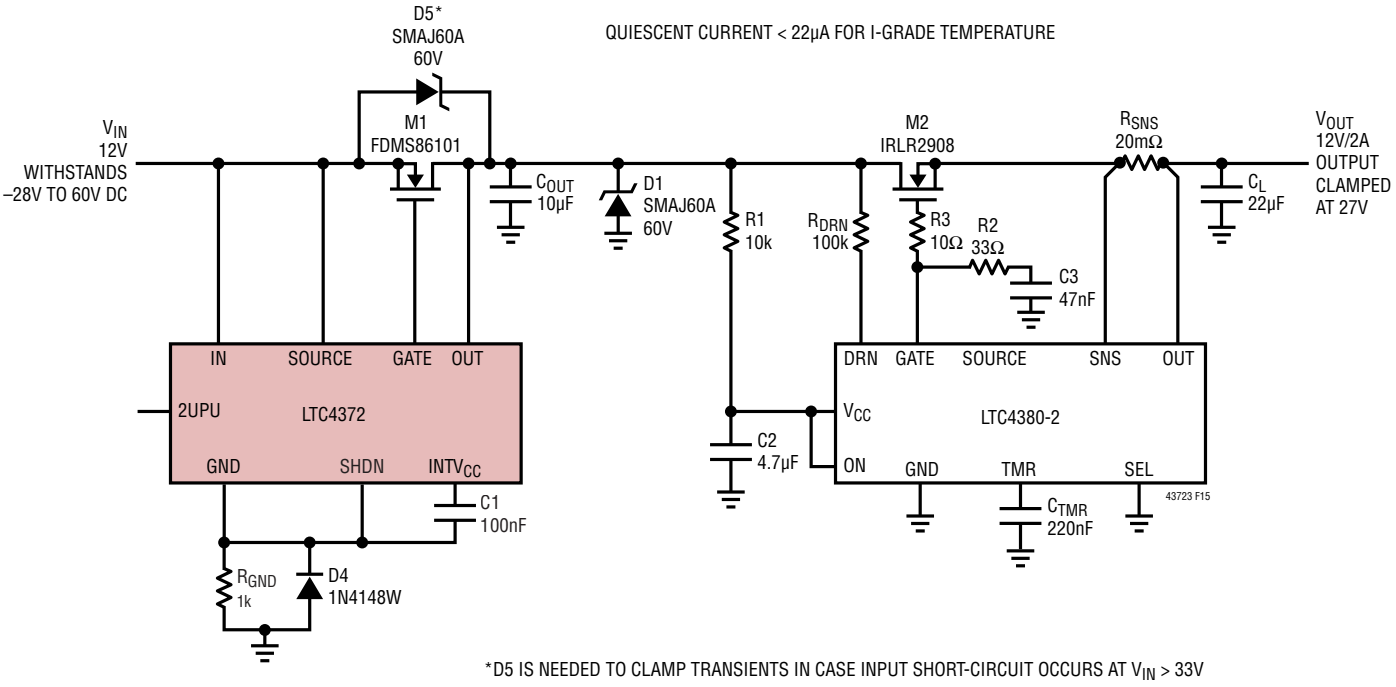


Figure 15. Micropower 12V Surge Stopper with Ideal Diode

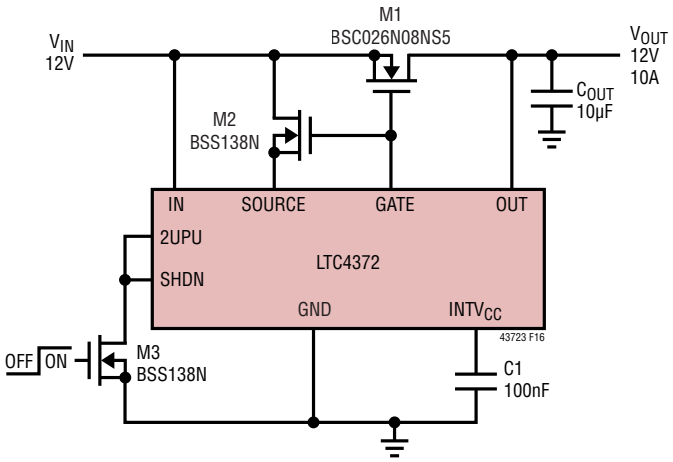
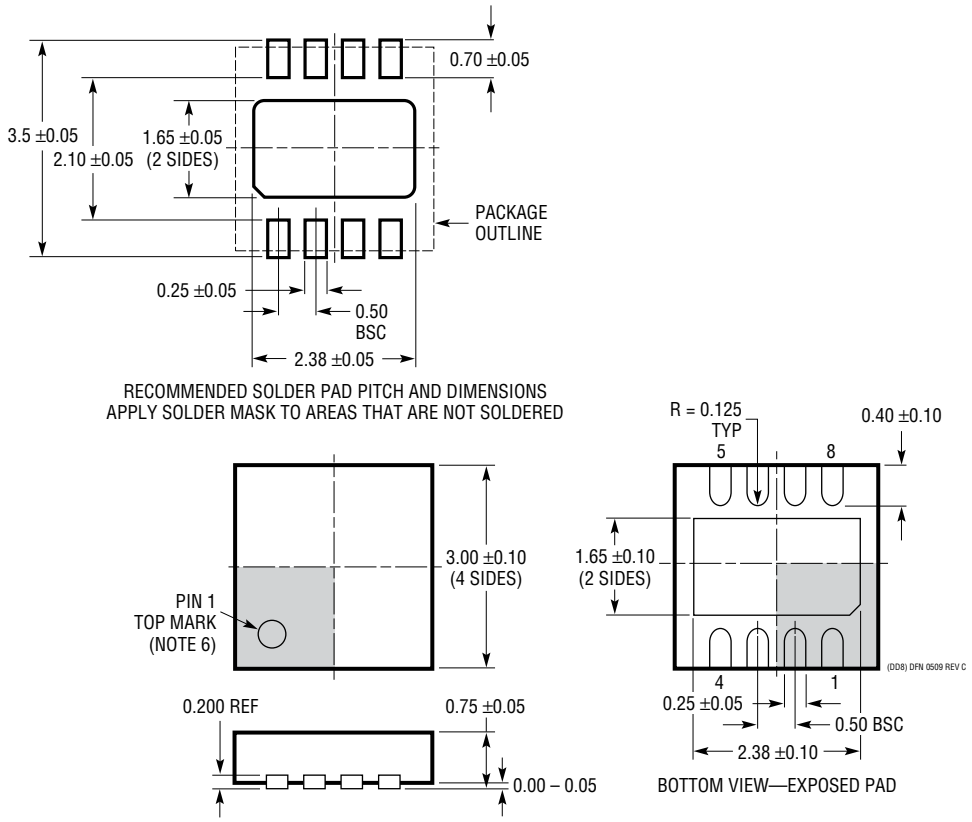


Figure 16. 12V Ideal Diode with Shutdown I_{CC} of 0.5µA (Nominal)

PACKAGE DESCRIPTION

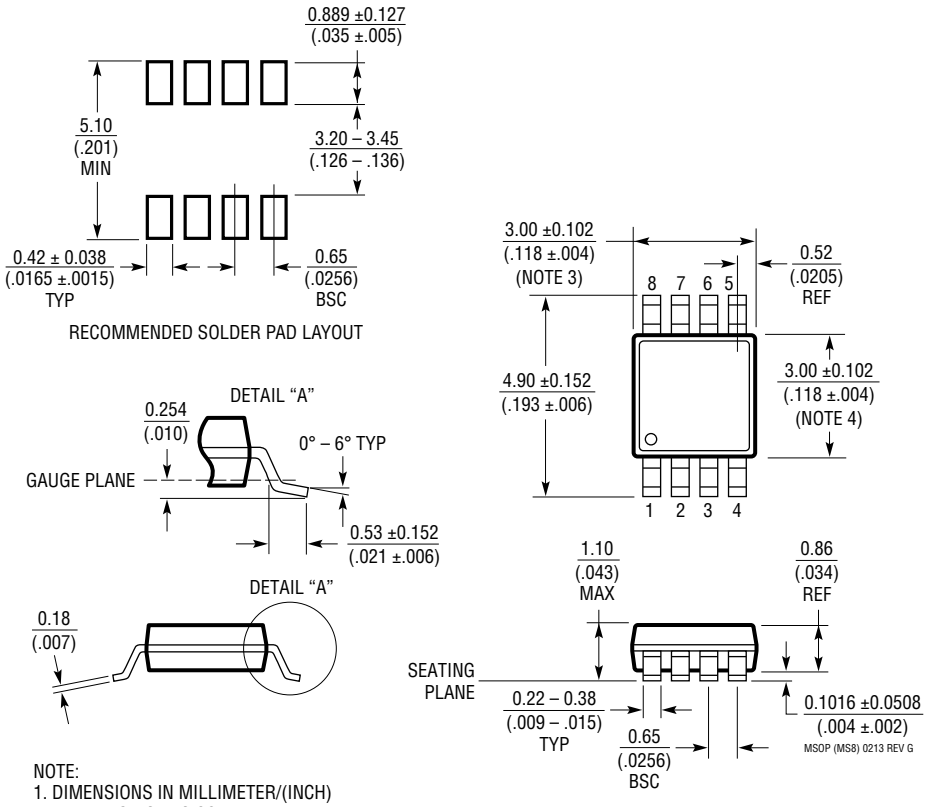
DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/21	Revised bullets and SHDN pin description.	1
		Revised Paralleling Supplies section.	13
		Revised Equations 5 and 6.	15
		Added new application.	18