42V, 5A/8A Peak Synchronous Step-Down Silent Switcher with 2.5µA Quiescent Current

FEATURES

- **Silent Switcher® Architecture**
  - **Ultralow EMI Emissions**
  - **Spread Spectrum Frequency Modulation**
- **High Efficiency at High Frequency**
  - **Up to 96% Efficiency at 1MHz, $12V_{IN}$ to $5V_{OUT}$**
  - **Up to 95% Efficiency at 2MHz, $12V_{IN}$ to $5V_{OUT}$**
- **Wide Input Voltage Range: 3.4V to 42V**
- **5A Maximum Continuous, 8A Peak Transient Output**
- **Ultralow Quiescent Current Burst Mode® Operation**
  - **2.5µA I_Q Regulating $12V_{IN}$ to $3.3V_{OUT}$**
  - **Output Ripple < $10mV_{P-P}$**
- **Fast Minimum Switch On-Time: 30ns**
- **Low Dropout Under All Conditions: 100mV at 1A**
- **Available in Fixed 3.3V Output**
- **Forced Continuous Mode**
- Safely Tolerates High Reverse Current
- Adjustable and Synchronizable: 200kHz to 3MHz
- Peak Current Mode Operation
- Output Soft-Start and Tracking
- Small 18-Lead 3mm × 4mm Side Solderable QFN with Improved Solder Joint Reliability
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Automotive and Industrial Supplies
- General Purpose Step-Down

DESCRIPTION

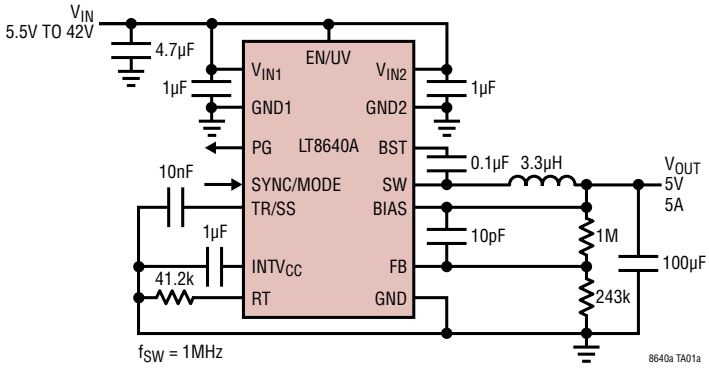
The LT®8640A step-down regulator features Silent Switcher architecture designed to minimize EMI emissions while delivering high efficiency at frequencies up to 3MHz. An ultralow 2.5µA quiescent current—with the output in full regulation—enables applications requiring highest efficiency at very small load currents.

The LT8640A allows high V_{IN} to low V_{OUT} conversion at high frequency with a fast minimum top switch on-time of 30ns. The SYNC/MODE pin selects between Burst Mode operation, spread spectrum mode, synchronization to an external clock, and forced continuous mode.

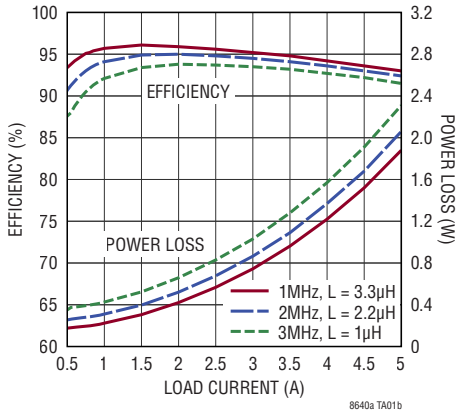
	PACKAGE	SYNC/ MODE ≠ 0	V_C COMP	150°C GRADE	INTERNAL CAPS	OUTPUT (PEAK)
LT8640A	QFN	FCM	Internal	Yes	No	5A (8A)
LT8640	QFN	Pulse-Skipping	Internal	Yes	No	5A (7A)
LT8640-1	QFN	FCM	Internal	Yes	No	5A (7A)
LT8640S	LQFN	FCM	Internal	No	Yes	6A (7A)
LT8643S	LQFN	FCM	External	No	Yes	6A (7A)
LT8640S-2	LQFN	FCM	Internal	Yes	No	6A (7A)
LT8643S-2	LQFN	FCM	External	Yes	No	6A (7A)

TYPICAL APPLICATION

5V 5A Step-Down Converter



$12V_{IN}$ to $5V_{OUT}$ Efficiency



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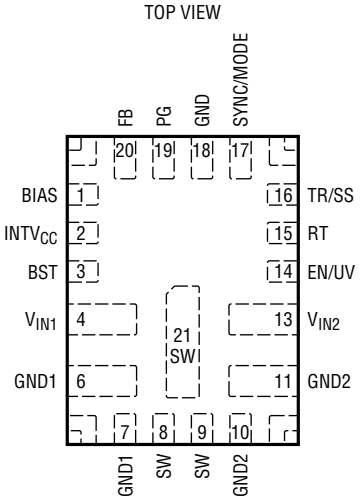
ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN}, EN/UV, PG.....42V
BIAS.....25V
FB, TR/SS 4V
SYNC/MODE, V_{OUT} Voltage 6V

Operating Junction Temperature Range (Note 2)
LT8640AJ .....–40°C to 150°C
Storage Temperature Range .....–65 to 150°C

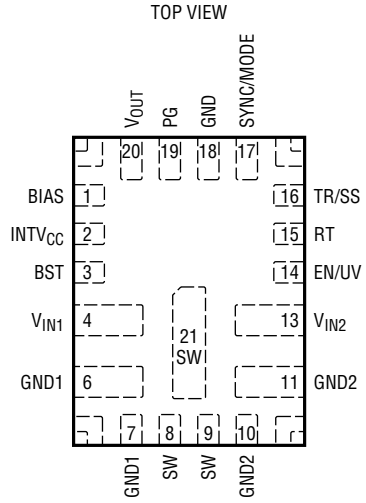
PIN CONFIGURATION

LT8640A



UDCM PACKAGE
18-LEAD (3mm × 4mm) PLASTIC QFN
DEMO BOARD: θ_{JA} = 29°C/W, ψ_{JT} = 0.5°C/W
JEDEC BOARD: θ_{JCtop} = 39.5°C/W, $\theta_{JCbottom}$ = 5.4°C/W (Note 3)
EXPOSED PAD (PIN 21) IS SW, SHOULD BE SOLDERED TO PCB
NOTE: PINS 5 AND 12 ARE REMOVED. CONFIGURATION DOES **NOT** MATCH JEDEC 20-LEAD PACKAGE OUTLINE

LT8640A-3.3



UDCM PACKAGE
18-LEAD (3mm × 4mm) PLASTIC QFN
DEMO BOARD: θ_{JA} = 29°C/W, ψ_{JT} = 0.5°C/W
JEDEC BOARD: θ_{JCtop} = 39.5°C/W, $\theta_{JCbottom}$ = 5.4°C/W (Note 3)
EXPOSED PAD (PIN 21) IS SW, SHOULD BE SOLDERED TO PCB
NOTE: PINS 5 AND 12 ARE REMOVED. CONFIGURATION DOES **NOT** MATCH JEDEC 20-LEAD PACKAGE OUTLINE

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8640AJUDCM#PBF	LT8640AJUDCM#TRPBF	LHNK	18-Lead (3mm × 4mm) Plastic Side Solderable QFN	–40°C to 150°C
LT8640AJUDCM-3.3#PBF	LT8640AJUDCM-3.3#TRPBF	LHQQ	18-Lead (3mm × 4mm) Plastic Side Solderable QFN	–40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LT8640AJUDCM#WPBF	LT8640AJUDCM#WTRPBF	LHNK	18-Lead (3mm × 4mm) Plastic Side Solderable QFN	–40°C to 150°C
LT8640AJUDCM-3.3#WPBF	LT8640AJUDCM-3.3#WTRPBF	LHQQ	18-Lead (3mm × 4mm) Plastic Side Solderable QFN	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		●		2.9	3.4	V
V_{IN} Quiescent Current In Shutdown	$V_{EN/UV}$ = 0V, V_{IN} = 12V	 ●		0.75 0.75	3 10	µA µA
V_{IN} Quiescent Current In Sleep	$V_{EN/UV}$ = 2V, Not Switching, V_{SYNC} = 0V, V_{IN} = 6V	 ●		1.7 1.7	4 10	µA µA
LT8640A Feedback Reference Voltage	V_{IN} = 6V, I_{LOAD} = 0.5A V_{IN} = 6V, I_{LOAD} = 0.5A	 ●	0.964 0.958	0.970 0.970	0.976 0.982	V V
LT8640A-3.3 Output Reference Voltage	V_{IN} = 6V, I_{LOAD} = 0.5A V_{IN} = 6V, I_{LOAD} = 0.5A	 ●	3.28 3.25	3.3 3.3	3.32 3.35	V V
Reference Voltage Line Regulation	V_{IN} = 4.0V to 36V	●		0.004	0.02	%/V
LT8640A Feedback Pin Input Current	V_{FB} = 1V		–20		20	nA
BIAS Pin Current Consumption	V_{BIAS} = 3.3V, f_{SW} = 2MHz			11		mA
Minimum On-Time	I_{LOAD} = 1.5A, SYNC = 0V I_{LOAD} = 1.5A, SYNC = 2V	● ●		35 30	50 50	ns ns
Minimum Off-Time				80	110	ns
Oscillator Frequency	R_T = 221k R_T = 60.4k R_T = 18.2k	● ● ●	180 665 1.8	210 700 1.95	240 735 2.1	kHz kHz MHz
Top Power NMOS On-Resistance	I_{SW} = 1A			67		mΩ
Top Power NMOS Current Limit		●	9	12	15	A
Bottom Power NMOS On-Resistance	V_{INTVCC} = 3.4V, I_{SW} = 1A			28		mΩ
SW Leakage Current	V_{IN} = 42V, V_{SW} = 0V, 42V		–3		3	µA
EN/UV Pin Threshold	EN/UV Rising	●	0.94	1.0	1.06	V
EN/UV Pin Hysteresis				40		mV
EN/UV Pin Current	$V_{EN/UV}$ = 2V		–20		20	nA
PG Upper Threshold Offset from V_{FB} or V_{OUT}	V_{FB} or V_{OUT} Falling	●	5	7.5	10.25	%
PG Lower Threshold Offset from V_{FB} or V_{OUT}	V_{FB} or V_{OUT} Rising	●	–10.75	–8	–5.25	%
PG Hysteresis				0.3		%
PG Leakage	V_{PG} = 3.3V		–40		40	nA
PG Pull-Down Resistance	V_{PG} = 0.1V	●		700	2000	Ω
SYNC/MODE Threshold	SYNC/MODE DC and Clock Low Level Voltage SYNC/MODE Clock High Level Voltage SYNC/MODE DC High Level Voltage	● ● ●	0.7 2.2		 1.5 2.9	V V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Spread Spectrum Modulation Frequency Range	R_T = 60.4k, V_{SYNC} = 3.3V			22		%
Spread Spectrum Modulation Frequency	V_{SYNC} = 3.3V			3		kHz
TR/SS Source Current		●	1.2	1.9	2.6	µA
TR/SS Pull-Down Resistance	Fault Condition, TR/SS = 0.1V			200		Ω
V_{IN} to Disable Forced Continuous Mode	V_{IN} Rising		35	37	39	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8640AJ is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (PD, in Watts) according to the formula:

$$T_J = T_A + (PD \bullet \theta_{JA})$$

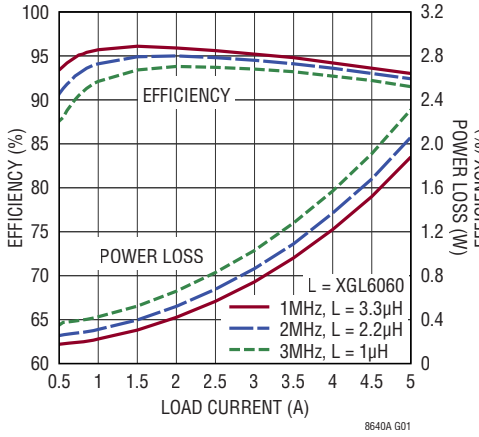
where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: JEDEC board θ values are determined per JESD51 conditions. Demo board θ values are obtained with demo board. See Applications Information section for information on improving the thermal resistance and for actual temperature measurements of a demo board in typical operating conditions.

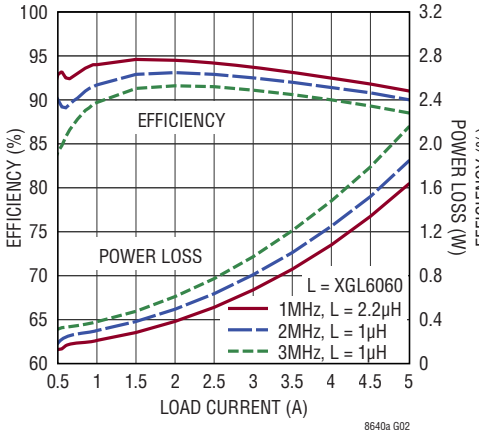
Note 4: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

TYPICAL PERFORMANCE CHARACTERISTICS

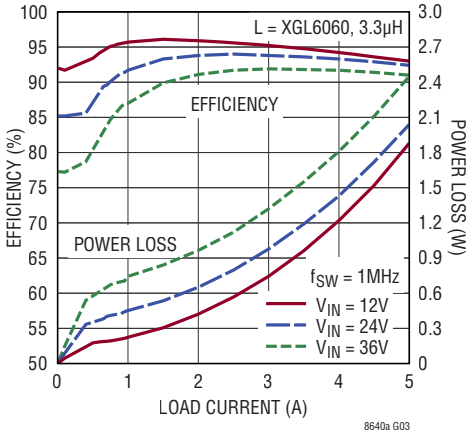
$12V_{IN}$ to $5V_{OUT}$ Efficiency vs Frequency



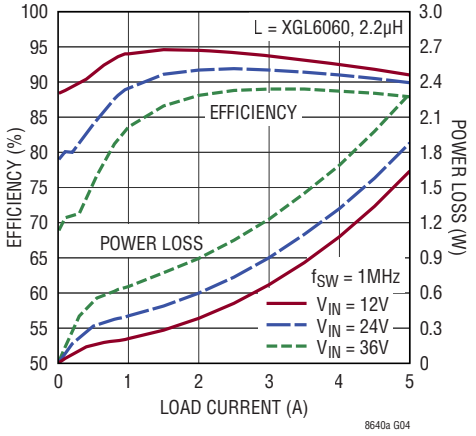
$12V_{IN}$ to $3.3V_{OUT}$ Efficiency vs Frequency



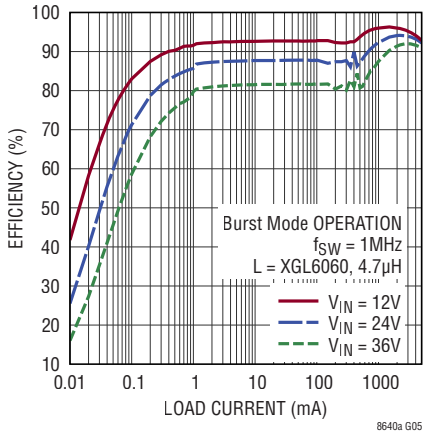
Efficiency at $5V_{OUT}$



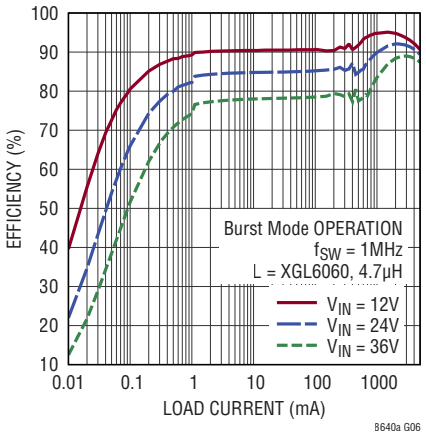
Efficiency at $3.3V_{OUT}$



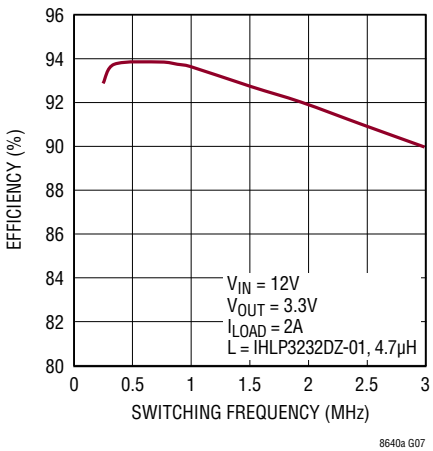
Low Load Efficiency at $5V_{OUT}$



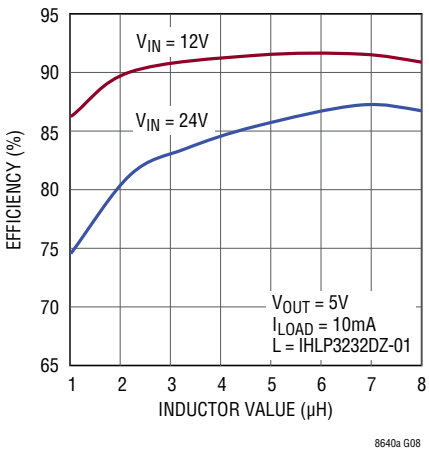
Low Load Efficiency at $3.3V_{OUT}$



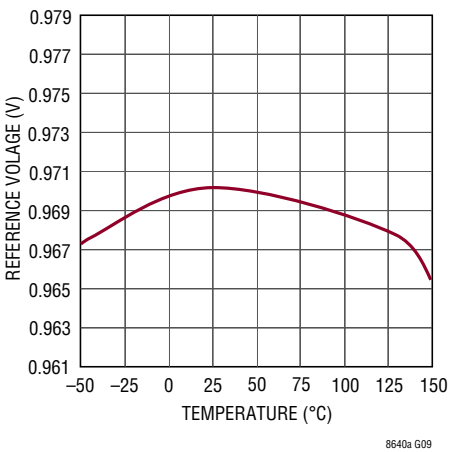
Efficiency vs Frequency



Burst Mode Operation Efficiency vs Inductor Value

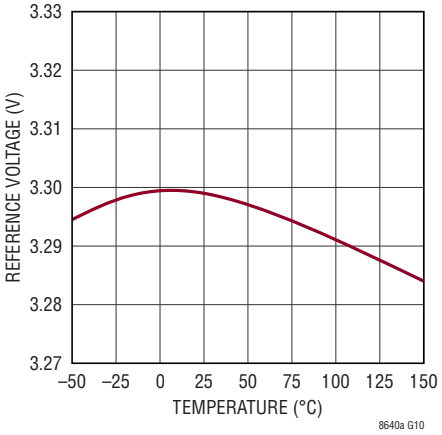


LT8640A Feedback Reference Voltage

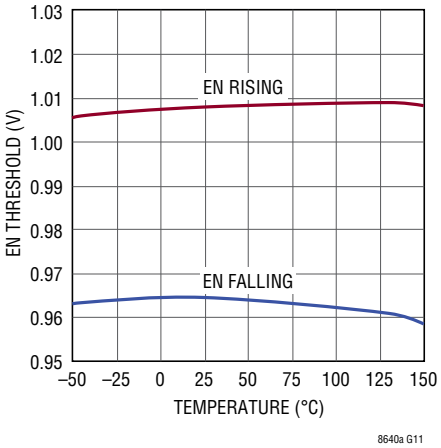


TYPICAL PERFORMANCE CHARACTERISTICS

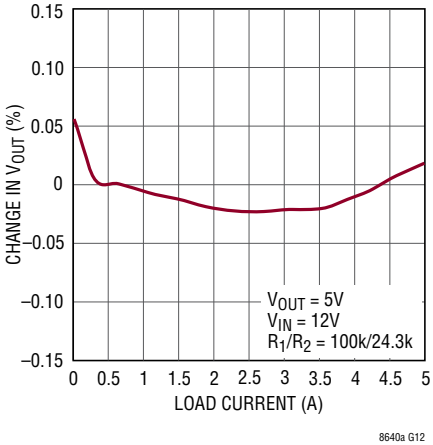
LT8640A-3.3 Output Reference Voltage



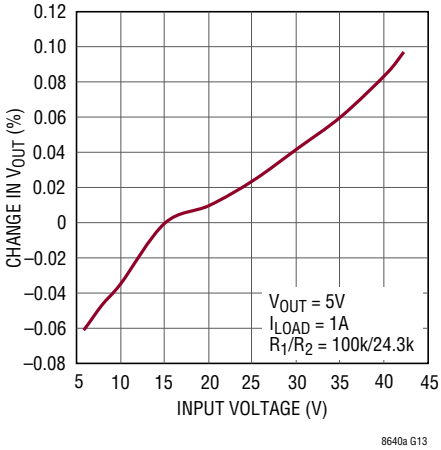
EN Pin Thresholds



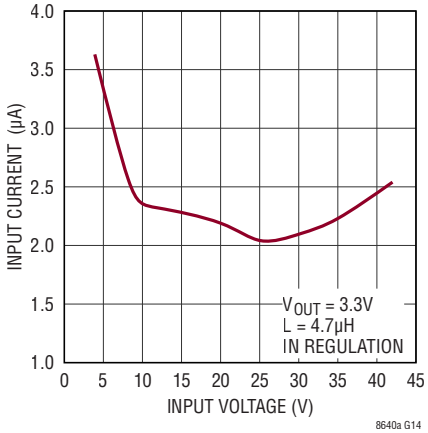
Load Regulation



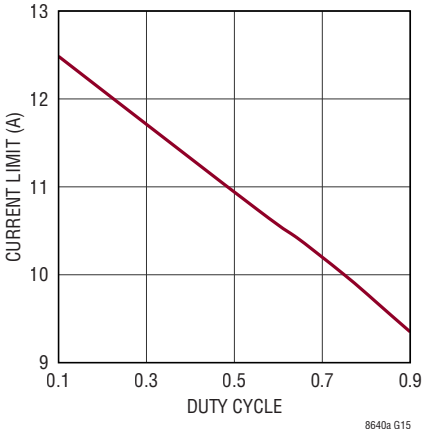
Line Regulation



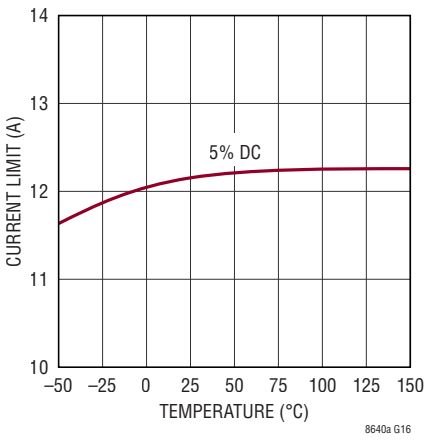
LT8640A No-Load Supply Current



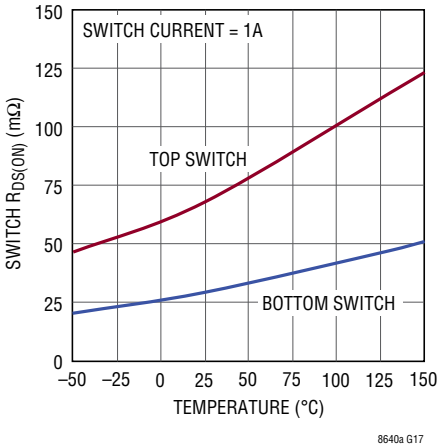
Top FET Current Limit vs Duty Cycle



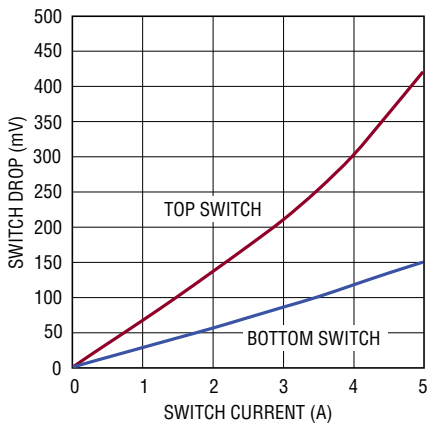
Top FET Current Limit



Switch $R_{DS(ON)}$ vs Temperature



Switch Drop vs Switch Current



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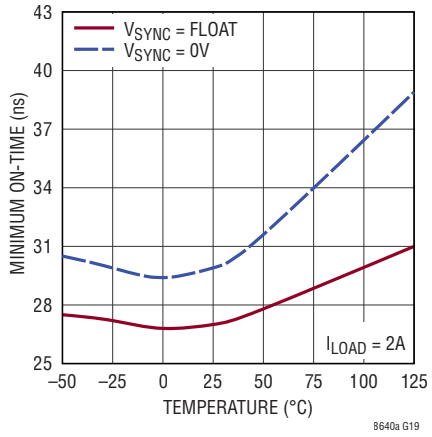
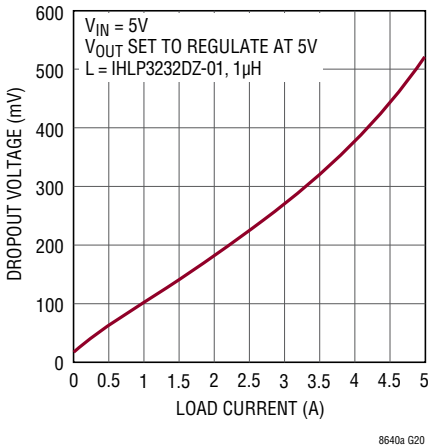
TYPICAL PERFORMANCE CHARACTERISTICS

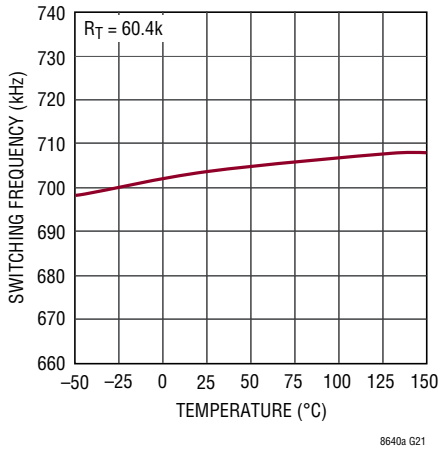
Minimum On-Time



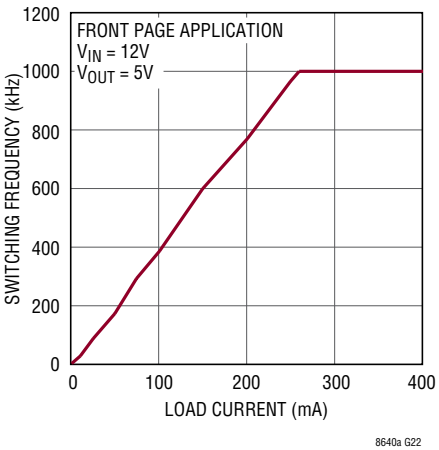
Dropout Voltage



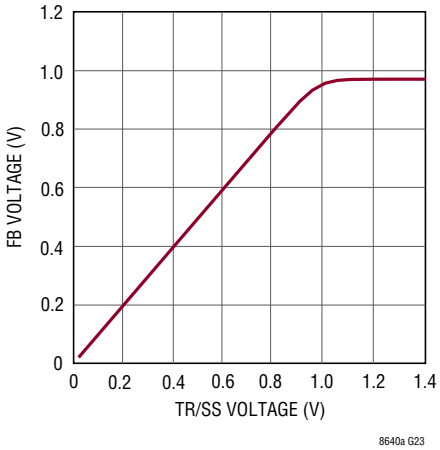
Switching Frequency



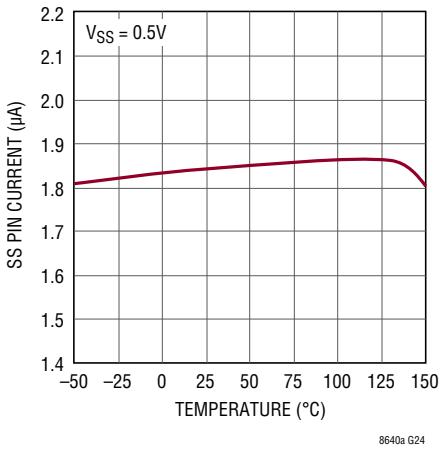
Burst Frequency



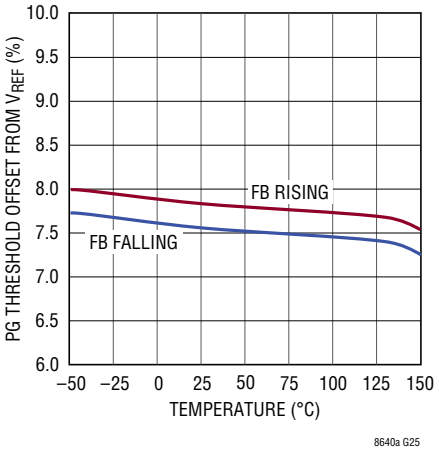
Soft-Start Tracking



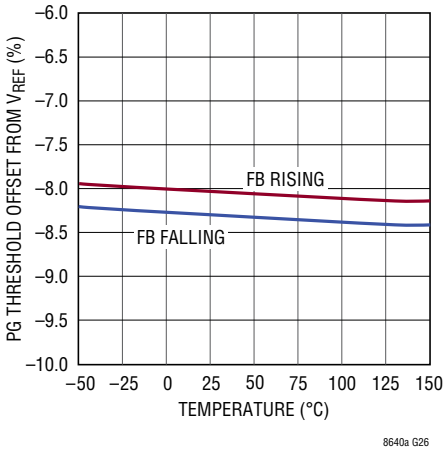
Soft-Start Current



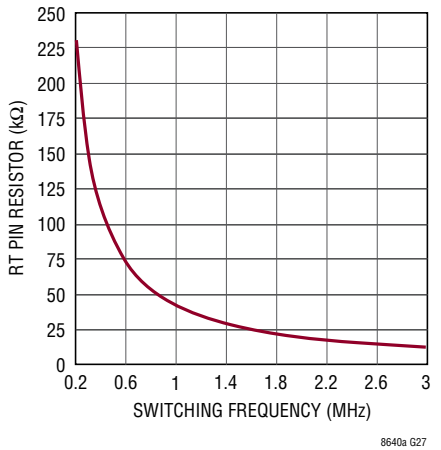
PG Thresholds Above V_{REF}



PG Thresholds Below V_{REF}

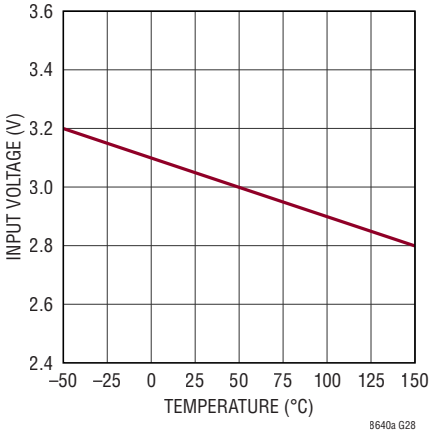


RT Programmed Switching Frequency

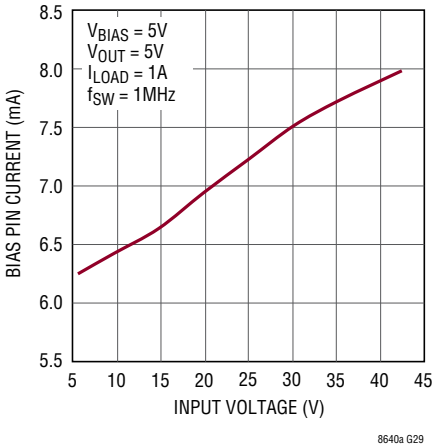


TYPICAL PERFORMANCE CHARACTERISTICS

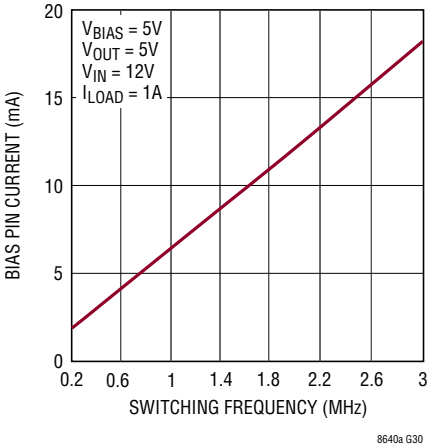
Minimum Input Voltage



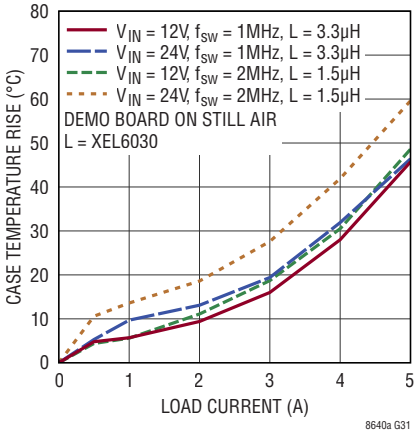
Bias Pin Current



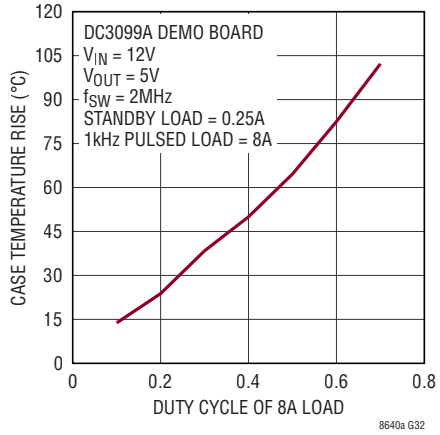
Bias Pin Current



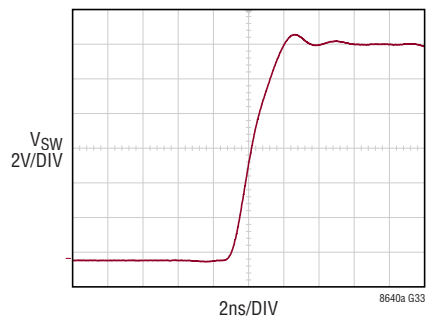
Case Temperature Rise



Case Temperature Rise vs 8A Pulsed Load

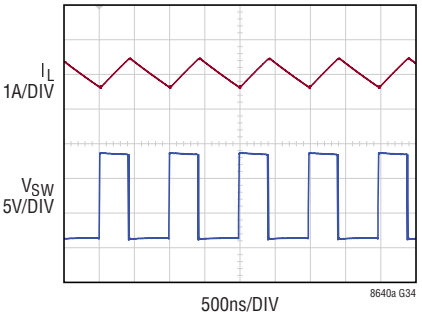


Switching Rising Edge



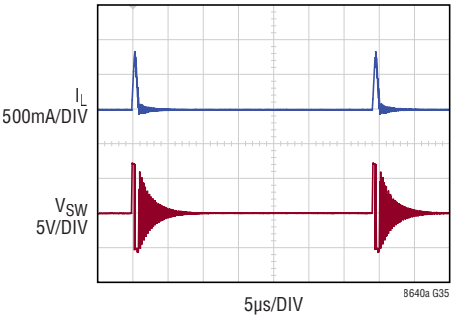
VIN = 12V
ILOAD = 2A

Switching Waveforms, Full Frequency Continuous Operation



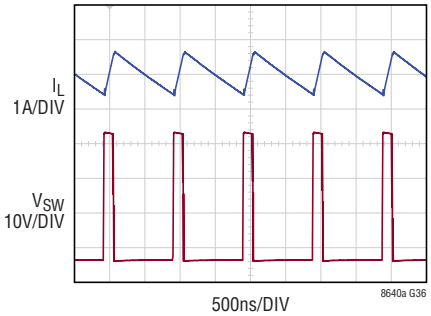
FRONT PAGE APPLICATION
12VIN TO 5VOUT AT 1A

Switching Waveforms, Burst Mode Operation



FRONT PAGE APPLICATION
12VIN TO 5VOUT AT 10mA
VSYNC = 0V

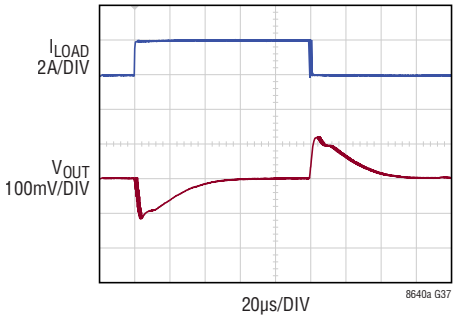
Switching Waveforms



FRONT PAGE APPLICATION
36VIN TO 5VOUT AT 1A

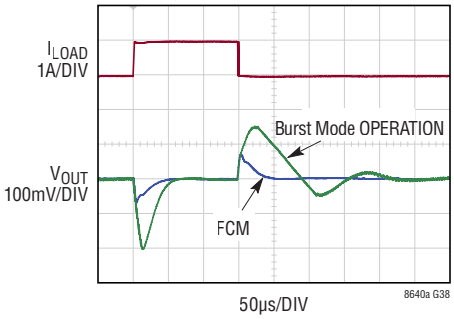
TYPICAL PERFORMANCE CHARACTERISTICS

Transient Response; Load Current Stepped from 2A to 4A



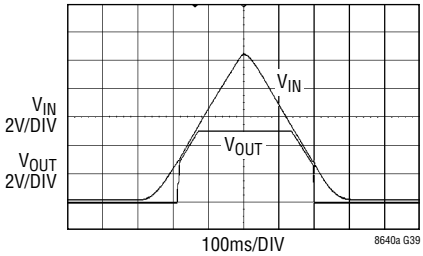
FRONT PAGE APPLICATION
2A TO 4A TRANSIENT
$12V_{IN}$, $5V_{OUT}$, f_{SW} = 2MHz
C_{OUT} = 100µF, C_{LEAD} = 10pF

Transient Response; Load Current Stepped from 100mA to 1.1A



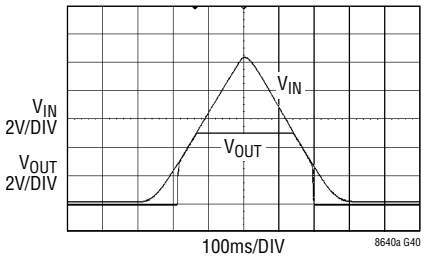
FRONT PAGE APPLICATION
100mA TO 1.1A TRANSIENT
$12V_{IN}$, $5V_{OUT}$, f_{SW} = 1MHz
C_{OUT} = 100µF

Start-Up Dropout Performance



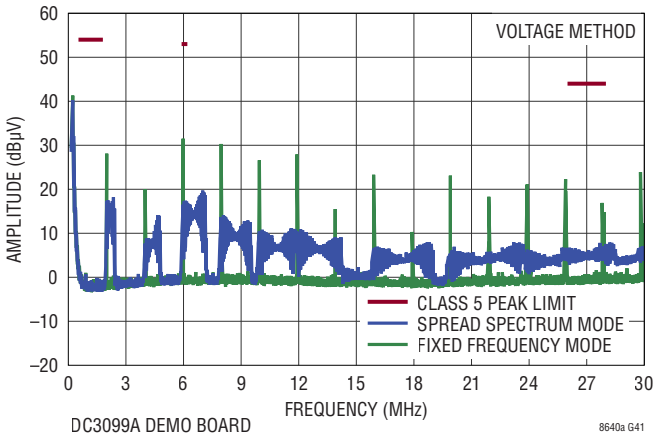
2.5Ω LOAD
(2A IN REGULATION)

Start-Up Dropout Performance



20Ω LOAD
(250mA IN REGULATION)

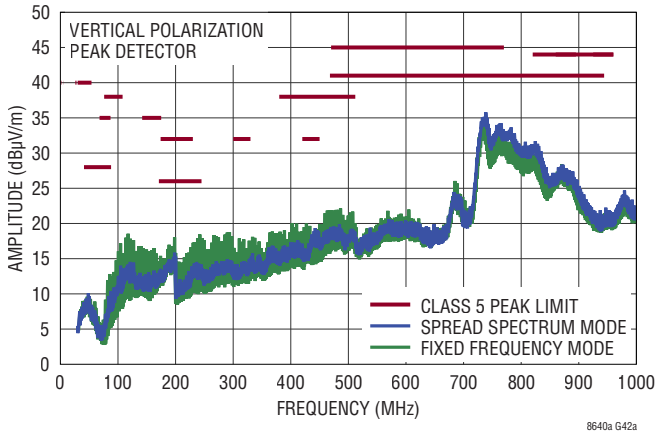
Conducted EMI Performance (CISPR25 Conducted Emission Test with Class 5 Peak Limits)

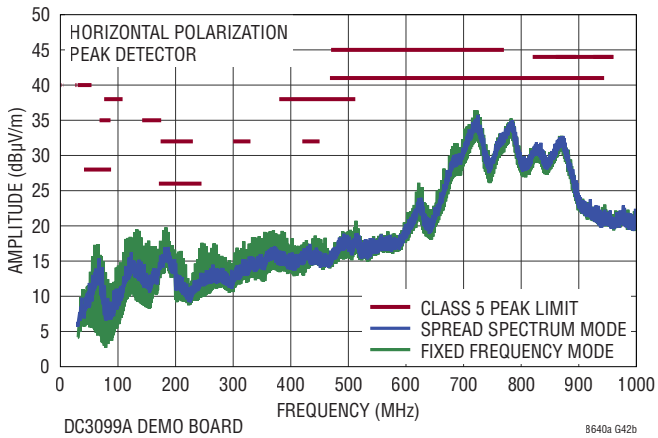


DC3099A DEMO BOARD
(WITH EMI FILTER INSTALLED)
12V INPUT TO 5V OUTPUT AT 5A, f_{SW} = 2MHz

TYPICAL PERFORMANCE CHARACTERISTICS

Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Peak Limits)





DC3099A DEMO BOARD
(WITH EMI FILTER INSTALLED)
12V INPUT TO 5V OUTPUT AT 5A, f_{SW} = 2MHz

PIN FUNCTIONS

BIAS (Pin 1): The internal regulator will draw current from BIAS instead of V_{IN} when BIAS is tied to a voltage higher than 3.1V. For output voltages of 3.3V to 25V this pin should be tied to V_{OUT}. If this pin is tied to a supply other than V_{OUT} use a 1µF local bypass capacitor on this pin. If no supply is available, tie to GND.

$INTV_{CC}$ (Pin 2): Internal 3.4V Regulator Bypass Pin. The internal power drivers and control circuits are powered from this voltage. $INTV_{CC}$ maximum output current is 20mA. Do not load the $INTV_{CC}$ pin with external circuitry. $INTV_{CC}$ current will be supplied from BIAS if BIAS > 3.1V, otherwise current will be drawn from V_{IN}. Voltage on $INTV_{CC}$ will vary between 2.8V and 3.4V when BIAS is between 3.0V and 3.6V. Decouple this pin to power ground with at least a 1µF low ESR ceramic capacitor placed close to the IC.

BST (Pin 3): This pin is used to provide a drive voltage, higher than the input voltage, to the topside power switch. Place a 0.1µF boost capacitor as close as possible to the IC.

V_{IN1} (Pin 4): The LT8640A requires two 1µF small input bypass capacitors. One 1µF capacitor should be placed between V_{IN1} and GND1. A second 1µF capacitor should be placed between V_{IN2} and GND2. These capacitors must be placed as close as possible to the LT8640A. A third larger capacitor of 2.2µF or more should be placed close to the LT8640A with the positive terminal connected to V_{IN1} and V_{IN2}, and the negative terminal connected to ground. See Applications Information section for sample layout.

GND1 (6, 7): Power Switch Ground. These pins are the return path of the internal bottom side power switch and must be tied together. Place the negative terminal of the input capacitor as close to the GND1 pins as possible. Also be sure to tie GND1 to the ground plane. See the Applications Information section for sample layout.

SW (Pins 8, 9): The SW pins are the outputs of the internal power switches. Tie these pins together and connect them to the inductor and boost capacitor. This node should be kept small on the PCB for good performance and low EMI.

GND2 (10, 11): Power Switch Ground. These pins are the return path of the internal bottom side power switch and must be tied together. Place the negative terminal of the input capacitor as close to the GND2 pins as possible. Also be sure to tie GND2 to the ground plane. See the Applications Information section for sample layout.

V_{IN2} (Pin 13): The LT8640A requires two 1µF small input bypass capacitors. One 1µF capacitor should be placed between V_{IN1} and GND1. A second 1µF capacitor should be placed between V_{IN2} and GND2. These capacitors must be placed as close as possible to the LT8640A. A third larger capacitor of 2.2µF or more should be placed close to the LT8640A with the positive terminal connected to V_{IN1} and V_{IN2}, and the negative terminal connected to ground. See the Applications Information section for sample layout.

EN/UV (Pin 14): The LT8640A is shut down when this pin is low and active when this pin is high. The hysteretic threshold voltage is 1.00V going up and 0.96V going down. Tie to V_{IN} if the shutdown feature is not used. An external resistor divider from V_{IN} can be used to program a V_{IN} threshold below which the LT8640A will shut down.

RT (Pin 15): A resistor is tied between RT and ground to set the switching frequency.

TR/SS (Pin 16): Output Tracking and Soft-Start Pin. This pin allows user control of output voltage ramp rate during start-up. A TR/SS voltage below 0.97V forces the LT8640A to regulate the FB pin to equal the TR/SS pin voltage. In the LT8640A-3.3 fixed output voltage option, the output voltage will track the TR/SS pin voltage based on the 3.3/0.97 factor set by the internal feedback resistor divider. When TR/SS is above 0.97V, the tracking function is disabled and the internal reference resumes control of the error amplifier. An internal 1.9µA pull-up current from $INTV_{CC}$ on this pin allows a capacitor to program output voltage slew rate. This pin is pulled to ground with an internal 200Ω MOSFET during shutdown and fault conditions; use a series resistor if driving from a low impedance output. This pin may be left floating if the tracking function is not needed.

SYNC/MODE (Pin 17): This pin programs four different operating modes: 1) Burst Mode operation. Tie this pin to ground for Burst Mode operation at low output loads—this will result in ultralow quiescent current. 2) Forced Continuous mode (FCM). This mode offers fast transient

PIN FUNCTIONS

response and full frequency operation over a wide load range. Float this pin for FCM. When floating, pin leakage currents should be <1µA. 3) Spread spectrum mode. Tie this pin high to $INTV_{CC}$ (~3.4V) or an external supply of 3V to 4V for forced continuous mode with spread-spectrum modulation. 4) Synchronization mode. Drive this pin with a clock source to synchronize to an external frequency. During synchronization the part will operate in forced continuous mode.

GND (Pins 18): LT8640A Ground Pin. Connect this pin to system ground and to the ground plane.

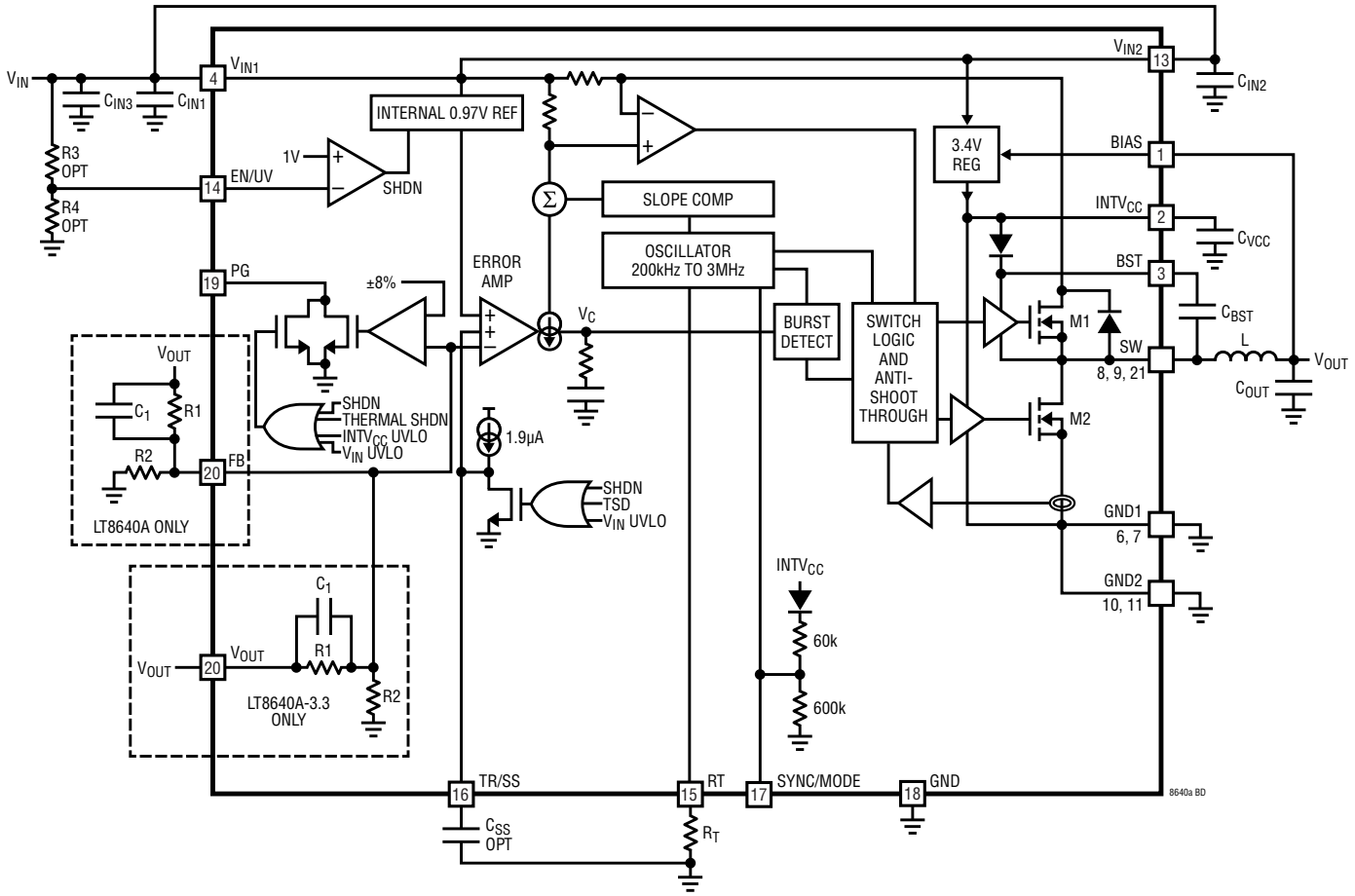
PG (Pin 19): The PG pin is the open-drain output of an internal comparator. PG remains low until the FB pin is within ±8% of the final regulation voltage, and there are no fault conditions. PG is valid when V_{IN} is above 3.4V, regardless of EN/UV pin state.

FB (Pin 20, LT8640A Only): The LT8640A regulates the FB pin to 0.970V. Connect the feedback resistor divider tap to this pin. Also, connect a phase lead capacitor between FB and V_{OUT}. Typically, this capacitor is 4.7pF to 22pF.

V_{OUT} (Pin 20, LT8640A-3.3 Only): The LT8640A-3.3 regulates the V_{OUT} pin to 3.3V. This pin connects a 11.33MΩ internal feedback that programs the fixed output.

SW (Exposed Pad Pin 21): The exposed pads should be connected and soldered to the SW trace for good thermal performance. If necessary due to manufacturing limitations Pin 21 may be left disconnected, however thermal performance will be degraded.

BLOCK DIAGRAM



OPERATION

The LT8640A is a monolithic, constant frequency, current mode step-down DC/DC converter. An oscillator, with frequency set using a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by the voltage on the internal VC node. The error amplifier servos the VC node by comparing the voltage on the V_{FB} pin with an internal 0.97V reference. When the load current increases it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the VC voltage until the average inductor current matches the new load current. The LT8640A-3.3 fixed output part uses the V_{OUT} pin and an internal resistor divider to generate an internal FB node. When the top power switch turns off, the synchronous power switch turns on until the next clock cycle begins or inductor current falls to zero. If overload conditions result in more than 9A flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

If the EN/UV pin is low, the LT8640A is shut down and draws 1µA from the input. When the EN/UV pin is above 1V, the switching regulator will become active.

To optimize efficiency at light loads, the LT8640A operates in Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 1.7µA. In a typical application, 2.5µA will be consumed from the input supply when regulating with no load. The SYNC/MODE pin is tied low to use Burst Mode operation and can be floated to use forced continuous mode (FCM). If a clock is applied to the SYNC/MODE pin, the part will synchronize to an external clock frequency and operate in FCM.

The LT8640A can operate in forced continuous mode (FCM) for fast transient response and full frequency operation over a wide load range. When in FCM the oscillator operates continuously and positive SW transitions are aligned to the clock. Negative inductor current is allowed. The LT8640A can sink current from the output and return this charge to the input in this mode, improving load step transient response.

To improve EMI, the LT8640A can operate in spread spectrum mode. This feature varies the clock with a triangular frequency modulation of +20%. For example, if the LT8640A's frequency is programmed to switch at 2MHz, spread spectrum mode will modulate the oscillator between 2MHz and 2.4MHz. The SYNC/MODE pin should be tied high to $INTV_{CC}$ (~3.4V) or an external supply of 3V to 4V to enable spread spectrum modulation with forced continuous mode.

To improve efficiency across all loads, supply current to internal circuitry can be sourced from the BIAS pin when biased at 3.1V or above. Else, the internal circuitry will draw current from V_{IN}. The BIAS pin should be connected to V_{OUT} if the LT8640A output is programmed at 3.3V to 25V.

Comparators monitoring the FB pin voltage will pull the PG pin low if the output voltage varies more than ±8% (typical) from the set point, or if a fault condition is present.

The oscillator reduces the LT8640A's operating frequency when the voltage at the FB pin is low, or the voltage at the V_{OUT} pin is low on the LT8640A-3.3 fixed voltage option. This frequency foldback helps to control the inductor current when the output voltage is lower than the programmed value which occurs during start-up or overcurrent conditions. When a clock is applied to the SYNC/MODE pin, the SYNC/MODE pin is floated, or held DC high, the frequency foldback is disabled and the switching frequency will slow down only during overcurrent conditions.

APPLICATIONS INFORMATION

Low EMI PCB Layout

The LT8640A is specifically designed to minimize EMI emissions and also to maximize efficiency when switching at high frequencies. For optimal performance the LT8640A requires the use of multiple V_{IN} bypass capacitors.

Two small 1µF capacitors should be placed as close as possible to the LT8640A: One capacitor should be tied to V_{IN1}/GND1; a second capacitor should be tied to V_{IN2}/GND2. A third capacitor with a larger value, 2.2µF or higher, should be placed near V_{IN1} or V_{IN2}.

See Figure 1 for a recommended PCB layout.

For more detail and PCB design files refer to the Demo Board guide for the LT8640A.

Note that large, switched currents flow in the LT8640A V_{IN1}, V_{IN2}, GND1, and GND2 pins and the input capacitors (C_{IN1}, C_{IN2}). The loops formed by the input capacitors should be as small as possible by placing the capacitors adjacent to the $V_{IN1/2}$ and GND1/2 pins. Capacitors with small case size such as 0603 are optimal due to lowest parasitic inductance.

The input capacitors, along with the inductor and output capacitors, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BOOST nodes should be as small as possible. Finally, keep the FB and RT nodes small so that the ground traces will shield them from the SW and BOOST nodes.

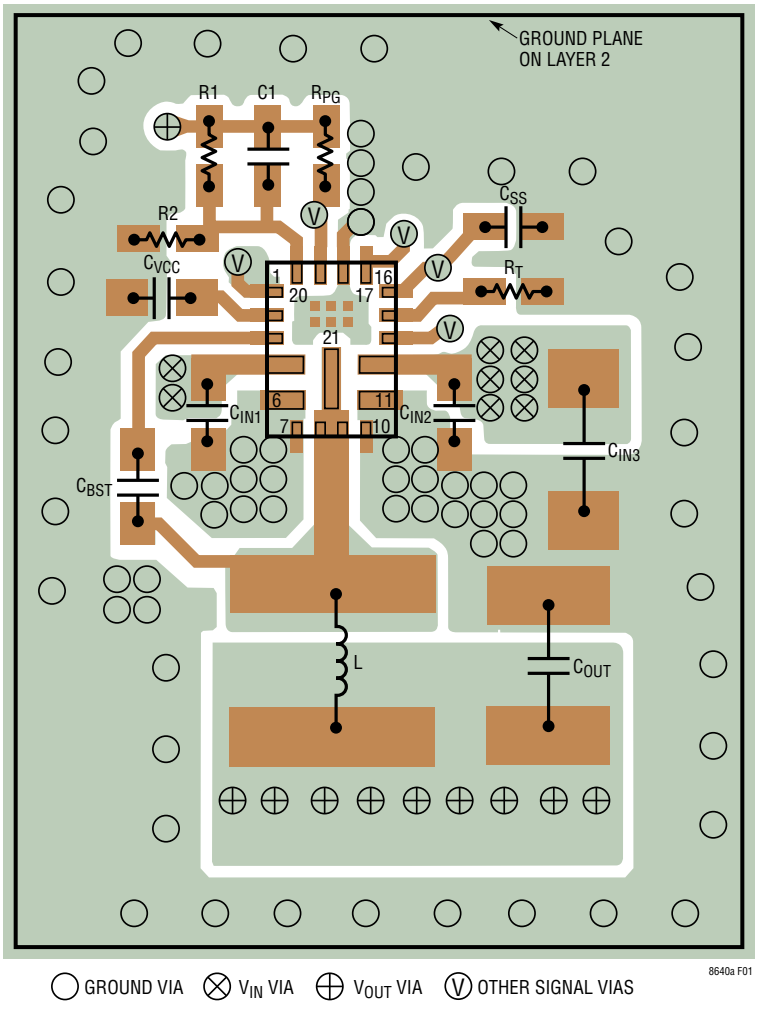


Figure 1. Recommended PCB Layout for the LT8640A

APPLICATIONS INFORMATION

The exposed pad on the bottom of the package should be soldered to SW to reduce thermal resistance to ambient. To keep thermal resistance low, extend the ground plane from GND1 and GND2 as much as possible, and add thermal vias to additional ground planes within the circuit board and on the bottom side.

Burst Mode Operation

To enhance efficiency at light loads, the LT8640A operates in low ripple Burst Mode operation, which keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and minimizing output voltage ripple. In Burst Mode operation the LT8640A delivers single small pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode the LT8640A consumes 1.7µA.

As the output load decreases, the frequency of single current pulses decreases (see Figure 2) and the percentage of time the LT8640A is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. By maximizing the time between pulses, the converter quiescent current approaches 2.5µA for a typical application when there is no output load. Therefore, to optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current.

In order to achieve higher light load efficiency, more energy must be delivered to the output during the single small pulses in Burst Mode operation such that the LT8640A can stay in sleep mode longer between each pulse. This can be achieved by using a larger value inductor (i.e., 4.7µH), and should be considered independent of switching frequency when choosing an inductor. For example, while a lower inductor value would typically be used for a high switching frequency application, if high light load efficiency is desired, a higher inductor value should be chosen. See curve in Typical Performance Characteristics.

While in Burst Mode operation the current limit of the top switch is approximately 900mA (as shown in Figure 3), resulting in low output voltage ripple. Increasing the output capacitance will decrease output ripple proportionally. As load ramps upward from zero the switching frequency will increase but only up to the switching frequency programmed by the resistor at the RT pin as shown in Figure 2.

The output load at which the LT8640A reaches the programmed frequency varies based on input voltage, output voltage and inductor choice. To select low ripple Burst Mode operation, tie the SYNC/MODE pin below 0.4V (this can be ground or a logic low output).

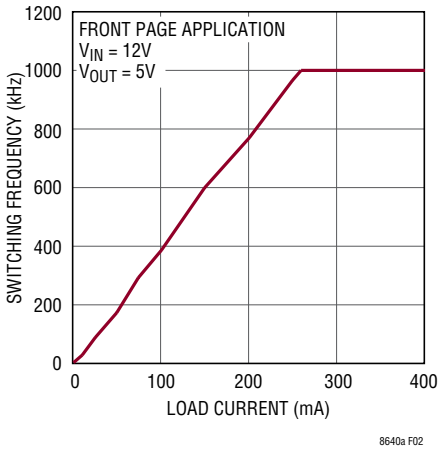


Figure 2. SW Frequency vs Load Information in Burst Mode Operation

APPLICATIONS INFORMATION

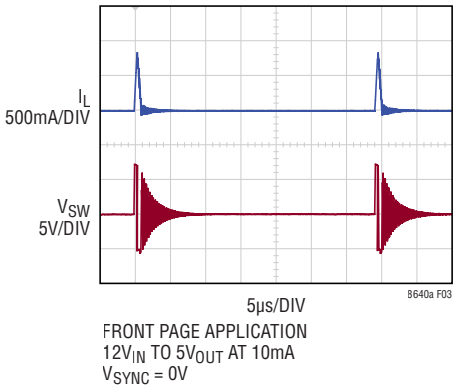


Figure 3. Burst Mode Operation

Forced Continuous Mode

The LT8640A can operate in forced continuous mode (FCM) for fast transient response and full frequency operation over a wide load range. When in FCM, the oscillator operates continuously and positive SW transitions are aligned to the clock. Negative inductor current is allowed at light loads or under large transient conditions. The LT8640A can sink current from the output and return this charge to the input in this mode, improving load step transient response (see Figure 4). At light loads, FCM operation is less efficient than Burst Mode operation, but may be desirable in applications where it is necessary to keep switching harmonics out of the signal band. FCM must be used if the output is required to sink current. To enable FCM, float the SYNC/MODE pin. Leakage current on this pin should be <1µA. See Block Diagram for internal pull-up and pull-down resistance.

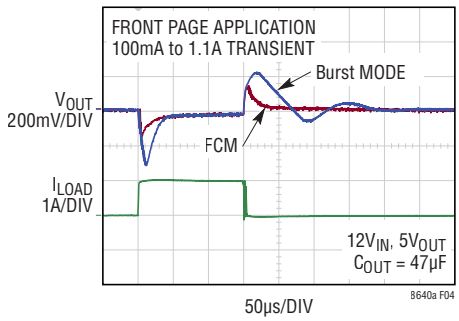


Figure 4. Load Step Transient Response with and without Forced Continuous Mode

FCM is disabled if the V_{IN} pin is held above 37V or if the FB pin is held greater than 8% above the feedback reference voltage. FCM is also disabled during soft-start until the soft-start capacitor is fully charged. When FCM is disabled in these ways, negative inductor current is not allowed and the LT8640A operates in pulse-skipping mode.

Spread Spectrum Mode

The LT8640A features spread spectrum operation to further reduce EMI emissions. To enable spread spectrum operation, the SYNC/MODE pin should be tied high to $INTV_{CC}$ (~3.4V) or an external supply of 3V to 4V. In this mode, triangular frequency modulation is used to vary the switching frequency between the value programmed by RT to approximately 20% higher than that value. The modulation frequency is approximately 3kHz. For example, when the LT8640A is programmed to 2MHz, the frequency will vary from 2MHz to 2.4MHz at a 3kHz rate. When spread spectrum operation is selected, Burst Mode operation is disabled, and the part will run in forced continuous mode.

Synchronization

To synchronize the LT8640A oscillator to an external frequency, connect a square wave to the SYNC/MODE pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 1.5V (up to 6V) with a minimum on-time and off-time of 50ns.

The LT8640A will not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead will run forced continuous mode to maintain regulation. The LT8640A may be synchronized over a 200kHz to 3MHz range. The RT resistor should be chosen to set the LT8640A switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the RT should be selected for 500kHz. The slope compensation is set by the RT value, while the minimum slope compensation required to avoid subharmonic oscillations is established by the inductor size, input voltage and output voltage. Since the synchronization frequency will not change the slopes of the inductor current waveform, if the inductor is large enough to avoid subharmonic oscillations at the

APPLICATIONS INFORMATION

frequency set by RT, then the slope compensation will be sufficient for all synchronization frequencies.

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to Equation 1.

$$R1 = R2\left(\frac{V_{OUT}}{0.970V} - 1\right) \quad (1)$$

Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy.

If low input quiescent current and good light-load efficiency are desired, use large resistor values for the FB resistor divider. The current flowing in the divider acts as a load current, and will increase the no-load input current to the converter, which is approximately given by Equation 2.

$$I_Q = 1.7\mu A + \left(\frac{V_{OUT}}{R1+R2}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{1}{n}\right) \quad (2)$$

where 1.7µA is the quiescent current of the LT8640A and the second term is the current in the feedback divider reflected to the input of the buck operating at its light load efficiency n. For a 3.3V application with R1 = 1M and R2 = 412k, the feedback divider draws 2.3µA. With V_{IN} = 12V and n = 80%, this adds 0.8µA to the 1.7µA quiescent current resulting in 2.5µA no-load current from the 12V supply. Note that this equation implies that the no-load current is a function of V_{IN}; this is plotted in the Typical Performance Characteristics section.

When using large FB resistors, a 4.7pF to 22pF phase-lead capacitor should be connected from V_{OUT} to FB.

The fixed output versions of the LT8640A have the feedback resistor network and phase lead capacitor integrated within the part. The FB pin is replaced with a V_{OUT} pin for these regulators. The V_{OUT} pin can be connected directly to the inductor and output capacitor. The LT8640A-3.3 regulates to 3.3V and has a total of 11.33MΩ of internal feedback divider resistance from the V_{OUT} pin to ground.

Setting the Switching Frequency

The LT8640A uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 3MHz by using a resistor tied from the RT pin to ground. A table showing the necessary R_T value for a desired switching frequency is in Table 1.

The R_T resistor required for a desired switching frequency can be calculated using Equation 3.

$$R_T = \frac{46.5}{f_{SW}} - 5.2 \quad (3)$$

where R_T is in kΩ and f_{SW} is the desired switching frequency in MHz.

Table 1. SW Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.2	232
0.3	150
0.4	110
0.5	88.7
0.6	71.5
0.7	60.4
0.8	52.3
1.0	41.2
1.2	33.2
1.4	28.0
1.6	23.7
1.8	20.5
2.0	17.8
2.2	15.8
3.0	10.7

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency and a smaller input voltage range.

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The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated with Equation 4.

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)}\left(V_{IN} - V_{SW(TOP)} + V_{SW(BOT)}\right)} \quad (4)$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.4V, ~0.15V, respectively at maximum load) and $t_{ON(MIN)}$ is the minimum top switch on-time (see the Electrical Characteristics). This equation shows that a slower switching frequency is necessary to accommodate a high V_{IN}/V_{OUT} ratio.

For transient operation, V_{IN} may go as high as the absolute maximum rating of 42V regardless of the R_T value, however the LT8640A will reduce switching frequency as necessary to maintain control of inductor current to assure safe operation. Note that in FCM operation, V_{OUT} may increase by up to 8% while V_{IN} is greater than what's allowed in Equation 4.

The LT8640A is capable of a maximum duty cycle of approximately 99%, and the V_{IN}-to-V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch. In this mode the LT8640A skips switch cycles, resulting in a lower switching frequency than programmed by RT. The maximum on-time of the top switch is approximately 14µs.

For applications that cannot allow deviation from the programmed switching frequency at low V_{IN}/V_{OUT} ratios use Equation 5 to set switching frequency:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{SW(BOT)}}{1 - f_{SW} \bullet t_{OFF(MIN)}} - V_{SW(BOT)} + V_{SW(TOP)} \quad (5)$$

where $V_{IN(MIN)}$ is the minimum input voltage without skipped cycles, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.4V, ~0.15V, respectively at maximum load), f_{SW} is the switching frequency (set by R_T), and $t_{OFF(MIN)}$ is the minimum switch off-time. Note that higher switching frequency will increase the minimum input voltage below which cycles will be dropped to achieve higher duty cycle.

Inductor Selection and Maximum Output Current

The LT8640A is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. During overload or short-circuit conditions the LT8640A safely tolerates operation with a saturated inductor through the use of a high speed peak-current mode architecture.

A good first choice for the inductor value is given by Equation 6.

$$L = \left(\frac{V_{OUT} + V_{SW(BOT)}}{f_{SW}}\right) \bullet 0.7 \quad (6)$$

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, $V_{SW(BOT)}$ is the bottom switch drop (~0.15V) and L is the inductor value in µH.

To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus 1/2 of in inductor ripple current (Equation 7).

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L \quad (7)$$

where ΔI_L is the inductor ripple current as calculated in Equation 9 and $I_{LOAD(MAX)}$ is the maximum output load for a given application.

As a quick example, an application requiring 3A output should use an inductor with an RMS rating of greater than 3A and an I_{SAT} of greater than 4A. During long duration overload or short-circuit conditions, the inductor RMS rating requirement is greater to avoid overheating of the inductor. To keep the efficiency high, the series resistance (DCR) should be less than 0.02Ω, and the core material should be intended for high frequency applications.

The LT8640A limits the peak switch current in order to protect the switches and the system from overload faults. The top switch current limit (I_{LIM}) is 12A at low duty cycles and decreases linearly to 9.5A at DC = 0.8. The inductor value must then be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is

APPLICATIONS INFORMATION

a function of the switch current limit (I_{LIM}) and the ripple current (Equation 8).

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2} \quad (8)$$

The peak-to-peak ripple current in the inductor can be calculated Equation 9.

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (9)$$

where f_{SW} is the switching frequency of the LT8640A, and L is the value of the inductor. Therefore, the maximum output current that the LT8640A will deliver depends on the switch current limit, the inductor value, and the input and output voltages. The inductor value may have to be increased if the inductor ripple current does not allow sufficient maximum output current ($I_{OUT(MAX)}$) given the switching frequency, and maximum input voltage used in the desired application.

In order to achieve higher light load efficiency, more energy must be delivered to the output during the single small pulses in Burst Mode operation such that the LT8640A can stay in sleep mode longer between each pulse. This can be achieved by using a larger value inductor (i.e., 4.7µH), and should be considered independent of switching frequency when choosing an inductor. For example, while a lower inductor value would typically be used for a high switching frequency application, if high light load efficiency is desired, a higher inductor value should be chosen. See curve in Typical Performance Characteristics.

The optimum inductor for a given application may differ from the one indicated by this design guide. A larger value inductor provides a higher maximum load current and reduces the output voltage ripple. For applications requiring smaller load currents, the value of the inductor may be lower and the LT8640A may operate with higher ripple current. This allows use of a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. Be aware that low inductance may result in discontinuous mode operation, which further reduces maximum load current.

For more information about maximum output current and discontinuous operation, see ADI's Application Note 44.

For duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid subharmonic oscillation (See Equation 10). See Application Note 19 for more details.

$$L_{MIN} = \frac{V_{IN}(2 \bullet DC - 1)}{4 \bullet f_{SW}} \quad (10)$$

where DC is the duty cycle ratio (V_{OUT}/V_{IN}) and f_{SW} is the switching frequency.

Input Capacitors

The V_{IN} of the LT8640A should be bypassed with at least three ceramic capacitors for best performance. Two small ceramic capacitors of 1µF should be placed close to the part; one at the V_{IN1}/GND1 pins and a second at V_{IN2}/GND2 pins. These capacitors should be 0402 or 0603 in size. For automotive applications requiring 2 series input capacitors, two small 0402 or 0603 may be placed at each side of the LT8640A near the V_{IN1}/GND1 and V_{IN2}/GND2 pins.

A third, larger ceramic capacitor of 2.2µF or larger should be placed close to V_{IN1} or V_{IN2}. See Low EMI PCB Layout section for more detail. X7R or X5R capacitors are recommended for best performance across temperature and input voltage variations.

Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT8640A circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8640A's voltage rating. This situation is easily avoided (see ADI Application Note 88).

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by

APPLICATIONS INFORMATION

the LT8640A to produce the DC output. In this role it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT8640A's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. For good starting values, see the Typical Applications section.

Use X5R or X7R types. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value output capacitor and the addition of a feedforward capacitor placed between V_{OUT} and FB. Increasing the output capacitance will also decrease the output voltage ripple. A lower value of output capacitor can be used to save space and cost but transient performance will suffer and may cause loop instability. See the Typical Applications in this data sheet for suggested capacitor values.

When choosing a capacitor, special attention should be given to the data sheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

Ceramic Capacitors

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8640A due to their piezoelectric nature. When in Burst Mode operation, the LT8640A's switching frequency depends on the load current, and at very light loads the LT8640A can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT8640A operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output. Low noise ceramic capacitors are also available.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LT8640A. As previously mentioned, a ceramic input capacitor combined with trace or cable inductance forms a high quality (underdamped) tank circuit. If the LT8640A circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8640A's rating. This situation is easily avoided (see ADI Note 88).

Enable Pin

The LT8640A is in shutdown when the EN pin is low and active when the pin is high. The rising threshold of the EN comparator is 1.0V, with 40mV of hysteresis. The EN pin can be tied to V_{IN} if the shutdown feature is not used, or tied to a logic level if shutdown control is required.

Adding a resistor divider from V_{IN} to EN programs the LT8640A to regulate the output only when V_{IN} is above a desired voltage (see the Block Diagram). Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. This threshold can be adjusted by setting the values R3 and R4 such that they satisfy Equation 11.

$$V_{IN(EN)} = \left(\frac{R3}{R4} + 1\right) \bullet 1.0V \qquad (11)$$

where the LT8640A will remain off until V_{IN} is above $V_{IN(EN)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $V_{IN(EN)}$.

When operating in Burst Mode operation for light load currents, the current through the $V_{IN(EN)}$ resistor network can easily be greater than the supply current consumed by the LT8640A. Therefore, the $V_{IN(EN)}$ resistors should be large to minimize their effect on efficiency at low loads.

$INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces the 3.4V supply from V_{IN} that powers the drivers and the internal bias circuitry. The $INTV_{CC}$ can supply enough current for the LT8640A's circuitry and must be bypassed to ground with a minimum of 1µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. To

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improve efficiency the internal LDO can also draw current from the BIAS pin when the BIAS pin is at 3.1V or higher. Typically the BIAS pin can be tied to the output of the LT8640A, or can be tied to an external supply of 3.3V or above. If BIAS is connected to a supply other than V_{OUT}, be sure to bypass with a local ceramic capacitor. If the BIAS pin is below 3.0V, the internal LDO will consume current from V_{IN}. Applications with high input voltage and high switching frequency where the internal LDO pulls current from V_{IN} will increase die temperature because of the higher power dissipation across the LDO. Do not connect an external load to the $INTV_{CC}$ pin.

Output Voltage Tracking and Soft-Start

The LT8640A allows the user to program its output voltage ramp rate by means of the TR/SS pin. An internal 1.9µA pulls up the TR/SS pin to $INTV_{CC}$. Putting an external capacitor on TR/SS enables soft starting the output to prevent current surge on the input supply. During the soft-start ramp the output voltage will proportionally track the TR/SS pin voltage. For output tracking applications, TR/SS can be externally driven by another voltage source. From 0V to 0.97V, the TR/SS voltage will override the internal 0.97V reference input to the error amplifier, thus regulating the FB pin voltage to that of TR/SS pin. In the LT8640A-3.3 fixed output voltage option, the output voltage will track the TR/SS pin voltage based on the 3.3/0.97 factor set by the internal feedback resistor divider. When TR/SS is above 0.97V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage. The TR/SS pin may be left floating if the function is not needed.

An active pull-down circuit is connected to the TR/SS pin which will discharge the external soft-start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the EN/UV pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

Output Power Good

When the LT8640A's output voltage is within the ±8% window of the regulation point, the output voltage is considered good and the open-drain PG pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal pull-down device will pull the PG pin low. To prevent glitching both the upper and lower thresholds include 0.3% of hysteresis. PG is valid when V_{IN} is above 3.4V.

The PG pin is also actively pulled low during several fault conditions: EN/UV pin is below 1V, $INTV_{CC}$ has fallen too low, V_{IN} is too low, or thermal shutdown.

Shorted and Reversed Input Protection

The LT8640A will tolerate a shorted output. Several features are used for protection during output short-circuit and brownout conditions. The first is the switching frequency will be folded back while the output is lower than the set point to maintain inductor current control.

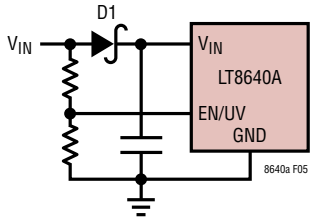

Figure 5. Reverse V_{IN} Protection

Second, the bottom switch current is monitored such that if inductor current is beyond safe levels switching of the top switch will be delayed until such time as the inductor current falls to safe levels.

Frequency foldback behavior depends on the state of the SYNC pin: If the SYNC pin is low the switching frequency will slow while the output voltage is lower than the programmed level. If the SYNC pin is connected to a clock source, floated or tied high, the LT8640A will stay at the programmed frequency without foldback and only slow switching if the inductor current exceeds safe levels.

There is another situation to consider in systems where the output will be held high when the input to the LT8640A is absent. This may occur in battery charging applications or in battery-backup systems where a battery or some other supply is diode ORed with the LT8640A's output. If the V_{IN} pin is allowed to float and the EN pin is held high (either by a logic signal or because it is tied to V_{IN}), then the

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LT8640A's internal circuitry will pull its quiescent current through its SW pin. This is acceptable if the system can tolerate several µA in this state. If the EN pin is grounded the SW pin current will drop to near 1µA. However, if the V_{IN} pin is grounded while the output is held high, regardless of EN, parasitic body diodes inside the LT8640A can pull current from the output through the SW pin and the V_{IN} pin. Figure 5 shows a connection of the V_{IN} and EN/UV pins that will allow the LT8640A to run only when the input voltage is present and that protects against a shorted or reversed input.

Thermal Considerations and Peak Output Current

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT8640A. The ground pins on the bottom of the package should be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT8640A. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LT8640A can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The die temperature is calculated by multiplying the LT8640A power dissipation by the thermal resistance from junction to ambient.

The internal overtemperature protection monitors the junction temperature of the LT8640A. If the junction temperature reaches approximately 170°C, the LT8640A will stop switching and indicate a fault condition until the temperature drops about 10°C cooler.

Temperature rise of the LT8640A is worst when operating at high load, high V_{IN}, and high switching frequency. If the case temperature is too high for a given application, then either V_{IN}, switching frequency, or load current can be decreased to reduce the temperature to an acceptable level. Figure 6 shows examples of how case temperature rise can be managed by reducing V_{IN}, switching frequency, or load.

The LT8640A's internal power switches are capable of safely delivering up to 8A of peak output current. However, due to thermal limits, the package can only handle 8A loads for short periods of time. This time is determined by how quickly the case temperature approaches the maximum junction rating. Figure 6 shows an example of how case temperature rise changes with the duty cycle of a 1kHz pulsed 8A load.

The LT8640A's top switch current limit decreases with higher duty cycle operation for slope compensation. This also limits the peak output current the LT8640A can deliver for a given application. See curve in Typical Performance Characteristics.

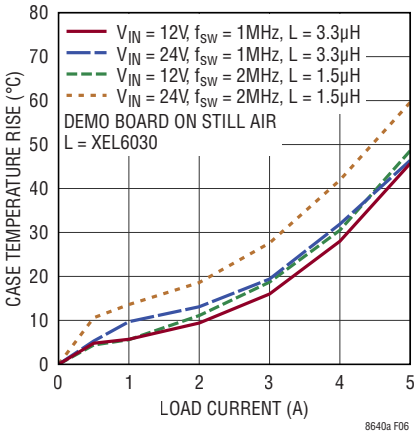


Figure 6. Case Temperature Rise

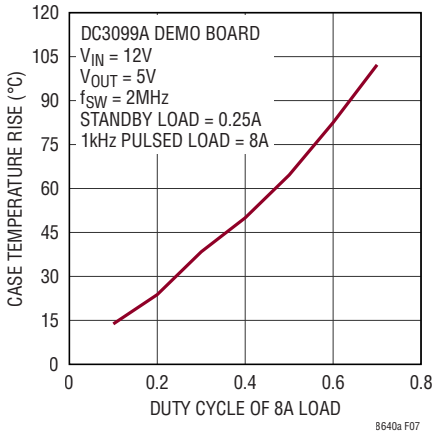
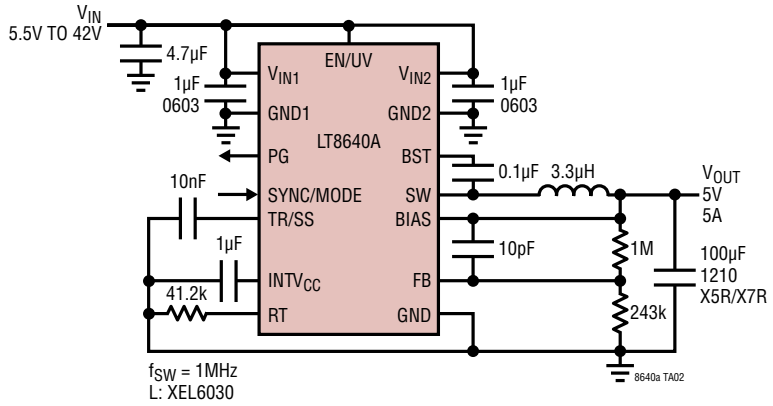


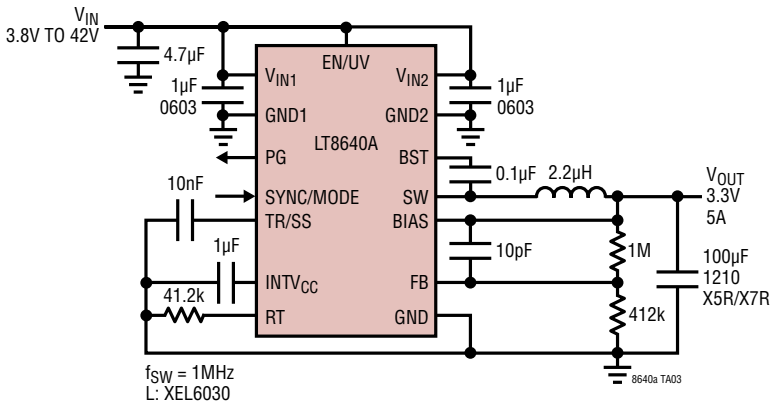
Figure 7. Case Temperature Rise vs 8A Pulsed Load

TYPICAL APPLICATIONS

1MHz 5V 5A Step-Down Converter

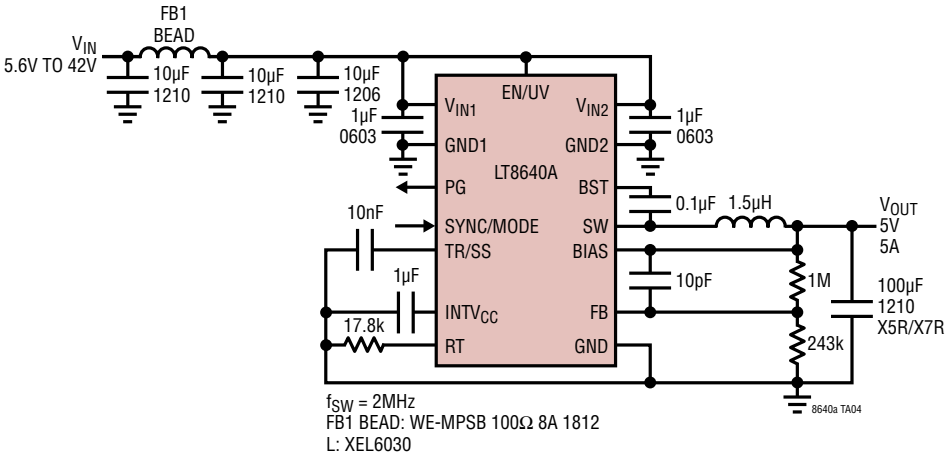


1MHz 3.3V, 5A Step-Down Converter

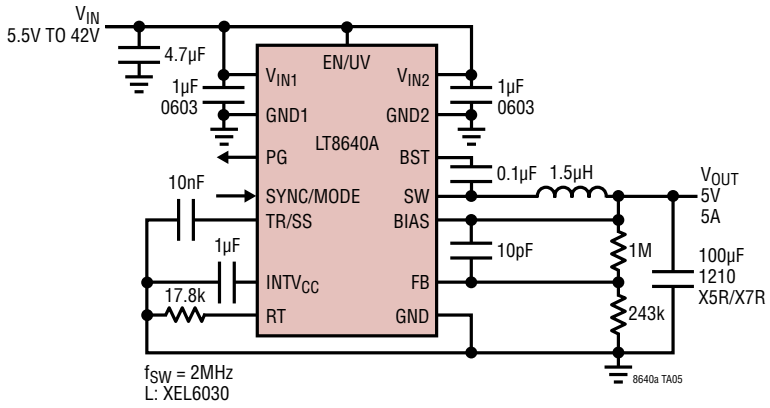


TYPICAL APPLICATIONS

Ultralow EMI 5V, 5A Step-Down Converter

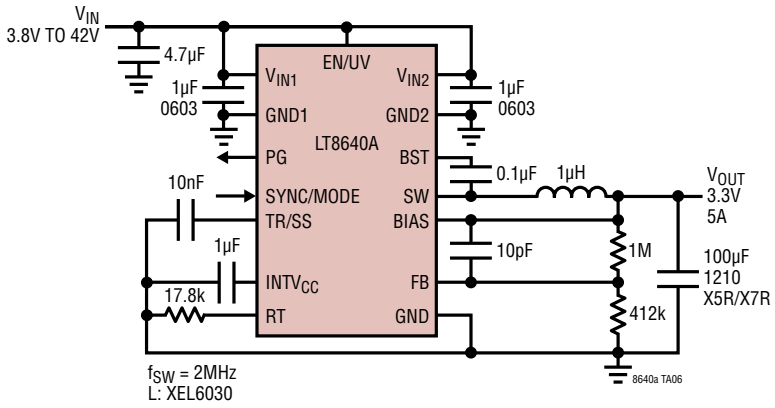


2MHz 5V, 5A Step-Down Converter

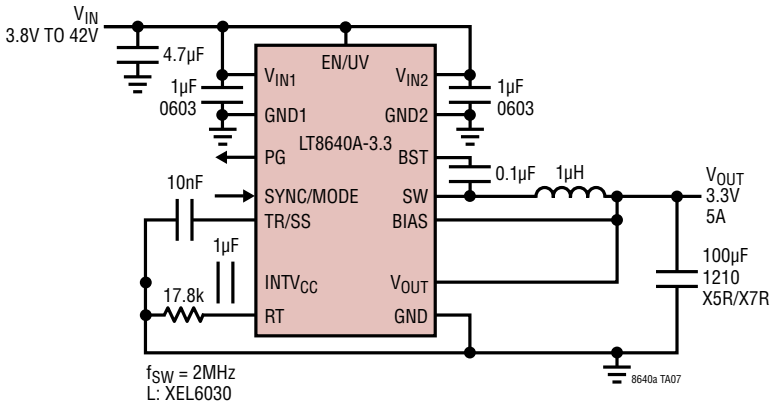


TYPICAL APPLICATIONS

2MHz 3.3V, 5A Step-Down Converter

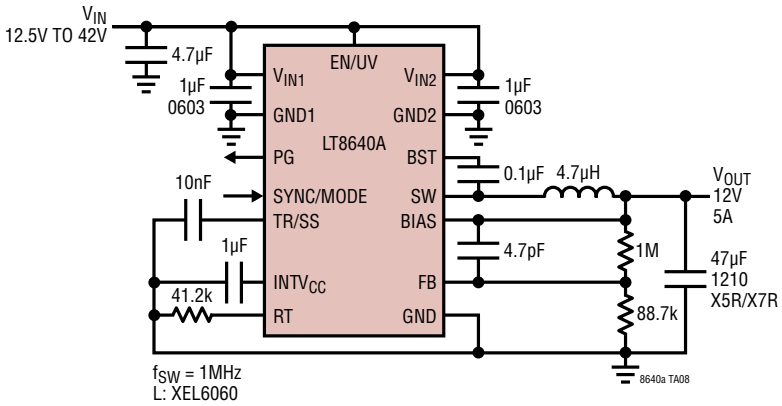


LT8640A-3.3 2MHz 3.3V, 5A Step-Down Converter



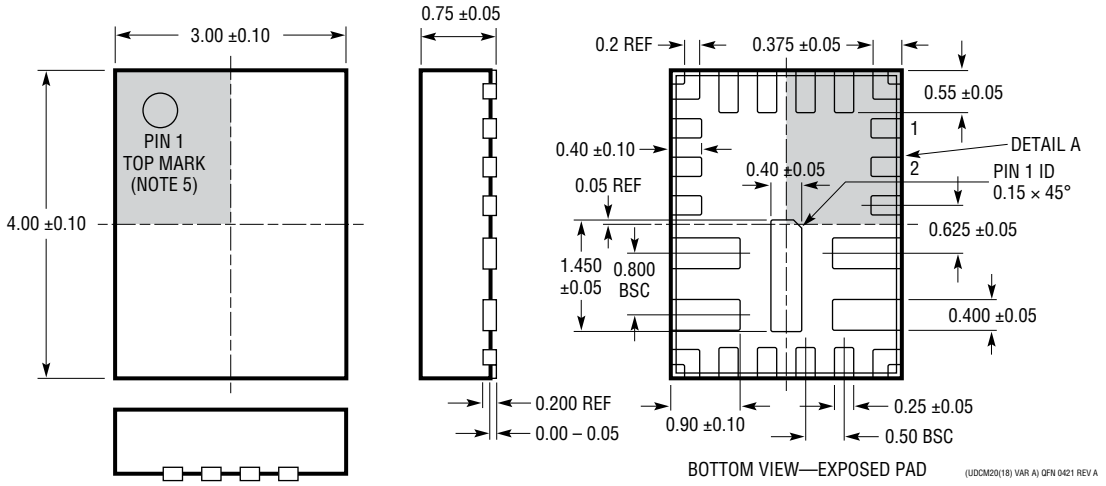
TYPICAL APPLICATIONS

12V, 5A Step-Down Converter

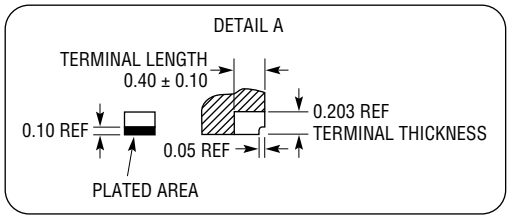


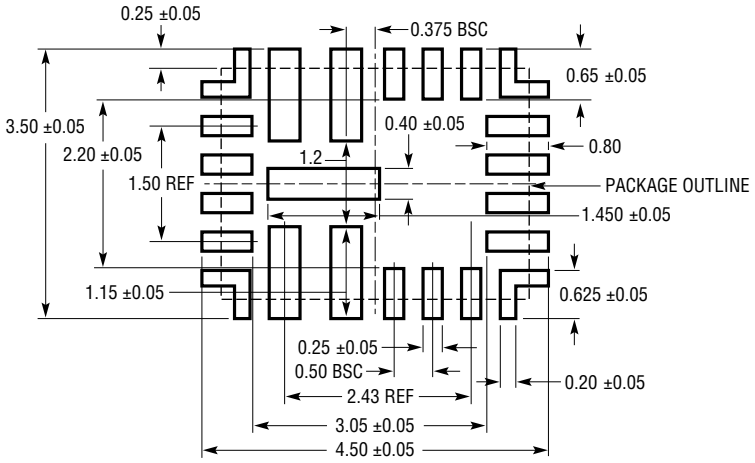
PACKAGE DESCRIPTION

UDCM Package
20(18)-Lead Plastic Side Wettable QFN (3mm × 4mm)
(Reference LTC DWG # 05-08-7030 Rev A)
Exposed Pad Variation AA



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE





RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED