Wide Operating Range, No R_{SENSE}™ Step-Down Controller for DDR/QDR Memory Termination

FEATURES

- **V_{OUT} = 1/2 V_{IN} (Supply Splitter)**
- **Adjustable and Symmetrical Sink/Source Current Limit up to 20A**
- **±0.65% Output Voltage Accuracy**
- **Up to 97% Efficiency**
- **No Sense Resistor Required**
- **Ultrafast Transient Response**
- **True Current Mode Control**
- **2% to 90% Duty Cycle at 200kHz**
- **$t_{ON(MIN)} \leq$ 100ns**
- **Stable with Ceramic C_{OUT}**
- Dual N-Channel MOSFET Synchronous Drive
- Power Good Output Voltage Monitor
- Wide V_{CC} Range: 4V to 36V
- Adjustable Switching Frequency up to 1.5MHz
- Output Overvoltage Protection
- Optional Short-Circuit Shutdown Timer
- Available in a 16-Pin Narrow SSOP Package

APPLICATIONS

- Bus Termination: DDR and QDR Memory, SSTL, HSTL, ...
- Notebook Computers, Desktop Servers
- Tracking Power Supply

DESCRIPTION

The LTC®3717 is a synchronous step-down switching regulator controller for double data rate (DDR) and Quad Data Rate™ (QDR™) memory termination. The controller uses a valley current control architecture to deliver very low duty cycles without requiring a sense resistor. Operating frequency is selected by an external resistor and is compensated for variations in V_{IN}.

Forced continuous operation reduces noise and RF interference. Output voltage is internally set to half of V_{REF}, which is user programmable.

Fault protection is provided by an output overvoltage comparator and optional short-circuit shutdown timer. Soft-start capability for supply sequencing is accomplished using an external timing capacitor. The regulator current limit level is symmetrical and user programmable. Wide supply range allows operation from 4V to 36V at the V_{CC} input.

TYPICAL APPLICATION

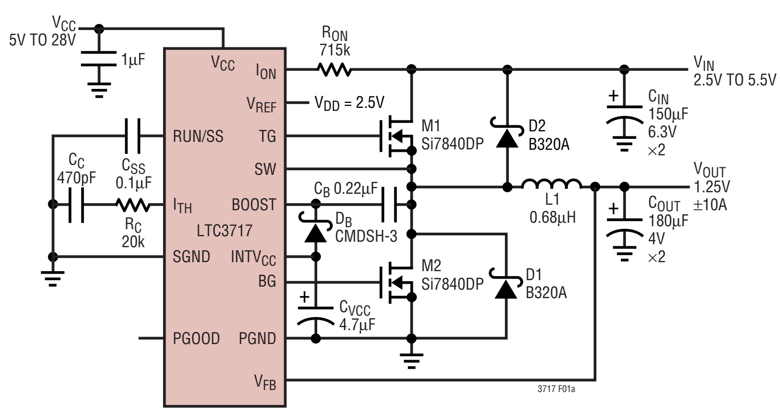
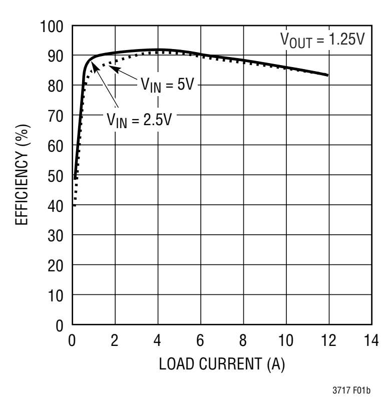


Figure 1. High Efficiency DDR Memory Termination Supply

Efficiency vs Load Current

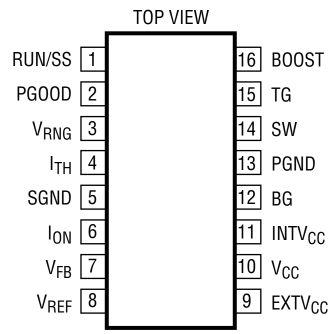


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{CC}, I_{ON}) .... 36V to –0.3V
Boosted Topside Driver Supply Voltage
(BOOST) .... 42V to –0.3V
SW Voltage .... 36V to –5V
$EXTV_{CC}$, (BOOST – SW), RUN/SS,
PGOOD Voltages .... 7V to –0.3V
V_{REF}, V_{RNG} Voltages .... ($INTV_{CC}$ + 0.3V) to –0.3V
I_{TH}, V_{FB} Voltages .... 2.7V to –0.3V
TG, BG, $INTV_{CC}$, $EXTV_{CC}$ Peak Currents 2A
TG, BG, $INTV_{CC}$, $EXTV_{CC}$ RMS Currents 50mA
Operating Ambient Temperature
Range (Note 4) .... –40°C to 85°C
Junction Temperature (Note 2) .... 125°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/ W

ORDER PART NUMBER
LTC3717EGN
GN PART MARKING
3717

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 15V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
I_Q	Input DC Supply Current Normal Shutdown Supply Current	 $V_{RUN/SS}$ = 0V			 1000 15	 2000 30	 µA µA
V_{FB}	Feedback Voltage Accuracy	I_{TH} = 1.2V (Note 3), V_{REF} = 2.4V		–0.65		0.65	%
$\Delta V_{FB(LINEREG)}$	Feedback Voltage Line Regulation	V_{CC}= 4V to 36V, I_{TH} = 1.2V (Note 3)			0.002		%/V
$\Delta V_{FB(LOADREG)}$	Feedback Voltage Load Regulation	I_{TH} = 0.5V to 1.9V (Note 3)	●		–0.05	–0.3	%
$g_{m(EA)}$	Error Amplifier Transconductance	I_{TH} = 1.2V (Note 3)		0.93	1.13	1.33	mS
t_{ON}	On-Time	I_{ON} = 30µA I_{ON} = 60µA		186 95	233 115	280 135	ns ns
$t_{ON(MIN)}$	Minimum On-Time	I_{ON} = 180µA			50	100	ns
$t_{OFF(MIN)}$	Minimum Off-Time	I_{ON} = 30µA			300	400	ns
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold (Source) V_{PGND} – V_{SW}	V_{RNG} = 1V, V_{FB} = $V_{REF/2}$ – 50mV V_{RNG} = 0V, V_{FB} = $V_{REF/2}$ – 50mV V_{RNG} = $INTV_{CC}$, V_{FB} = $V_{REF/2}$ – 50mV	● ● ●	108 76 148	135 95 185	162 114 222	mV mV mV
$V_{SENSE(MIN)}$	Minimum Current Sense Threshold (Sink) V_{PGND} – V_{SW}	V_{RNG} = 1V, V_{FB} = $V_{REF/2}$ + 50mV V_{RNG} = 0V, V_{FB} = $V_{REF/2}$ + 50mV V_{RNG} = $INTV_{CC}$, V_{FB} = $V_{REF/2}$ + 50mV	● ● ●	–140 –97 –200	–165 –115 –235	–190 –133 –270	mV mV mV
$\Delta V_{FB(OV)}$	Output Overvoltage Fault Threshold			8	10	12	%
$\Delta V_{FB(UV)}$	Output Undervoltage Fault Threshold				–25		%
$V_{RUN/SS(ON)}$	RUN Pin Start Threshold		●	0.8	1.5	2	V
$V_{RUN/SS(LE)}$	RUN Pin Latchoff Enable Threshold	RUN/SS Pin Rising			4	4.5	V
$V_{RUN/SS(LT)}$	RUN Pin Latchoff Threshold	RUN/SS Pin Falling			3.5	4.2	V
$I_{RUN/SS(C)}$	Soft-Start Charge Current			–0.5	–1.2	–3	µA
$I_{RUN/SS(D)}$	Soft-Start Discharge Current			0.8	1.8	3	µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 15V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{CC(UVLO)}$	Undervoltage Lockout Threshold	V_{CC} Falling	●		3.4	3.9	V
$V_{CC(UVLOR)}$	Undervoltage Lockout Threshold	V_{CC} Rising	●		3.5	4	V
TG R_{UP}	TG Driver Pull-Up On Resistance	TG High			2	3	Ω
TG R_{DOWN}	TG Driver Pull-Down On Resistance	TG Low			2	3	Ω
BG R_{UP}	BG Driver Pull-Up On Resistance	BG High			3	4	Ω
BG R_{DOWN}	BG Driver Pull-Down On Resistance	BG Low			1	2	Ω
TG t_r	TG Rise Time	C_{LOAD} = 3300pF			20		ns
TG t_f	TG Fall Time	C_{LOAD} = 3300pF			20		ns
BG t_r	BG Rise Time	C_{LOAD} = 3300pF			20		ns
BG t_f	BG Fall Time	C_{LOAD} = 3300pF			20		ns
Internal V_{CC} Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{CC} < 30V, V_{EXTVCC} = 4V	●	4.7	5	5.3	V
$\Delta V_{LDO(LOADREG)}$	Internal V_{CC} Load Regulation	I_{CC} = 0mA to 20mA, V_{EXTVCC} = 4V			–0.1	±2	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	I_{CC} = 20mA, V_{EXTVCC} Rising	●	4.5	4.7		V
ΔV_{EXTVCC}	$EXTV_{CC}$ Switch Drop Voltage	I_{CC} = 20mA, V_{EXTVCC} = 5V			150	300	mV
$\Delta V_{EXTVCC(HYS)}$	$EXTV_{CC}$ Switchover Hysteresis				200		mV
PGOOD Output							
ΔV_{FBH}	PGOOD Upper Threshold	V_{FB} Rising (0% = 1/3 V_{REF})		8	10	12	%
ΔV_{FBL}	PGOOD Lower Threshold	V_{FB} Falling (0% = 1/3 V_{REF})		–8	–10	–12	%
$\Delta V_{FB(HYS)}$	PGOOD Hysteresis	V_{FB} Returning (0% = 1/3 V_{REF})			1	2	%
V_{PGL}	PGOOD Low Voltage	I_{PGOOD} = 5mA			0.15	0.4	V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D as follows:

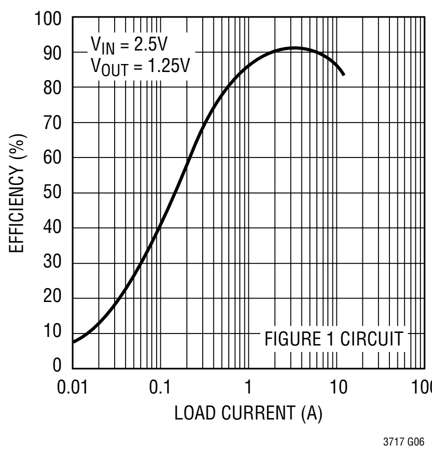
LTC3717EGN: $T_J = T_A + (P_D \bullet 130°C/W)$

Note 3: The LTC3717 is tested in a feedback loop that adjusts V_{FB} to achieve a specified error amplifier output voltage (I_{TH}).

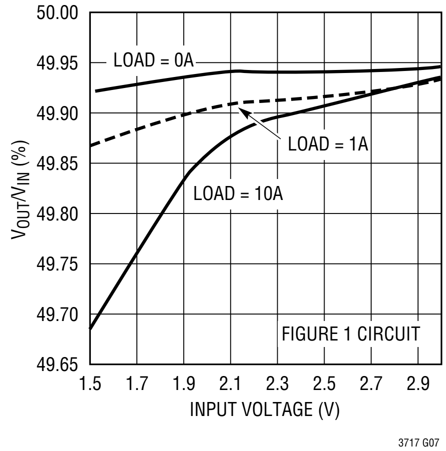
Note 4: The LTC3717E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

TYPICAL PERFORMANCE CHARACTERISTICS

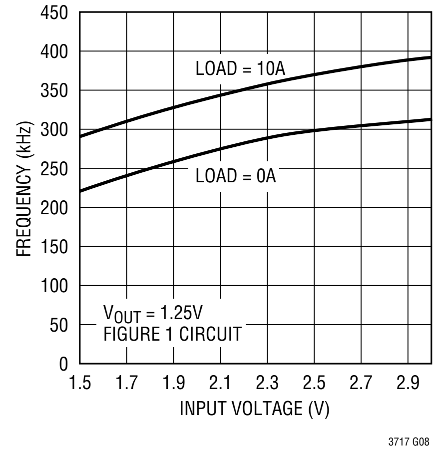
Efficiency vs Load Current



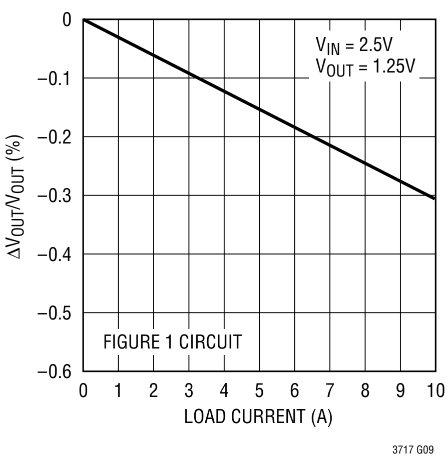
V_{OUT}/V_{IN} Tracking Ratio vs Input Voltage



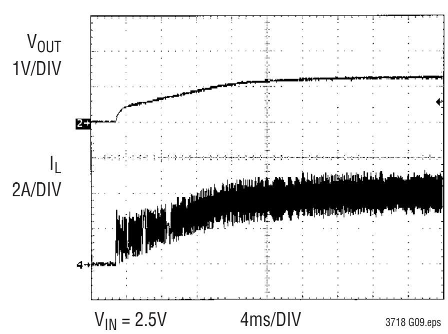
Frequency vs Input Voltage



Load Regulation

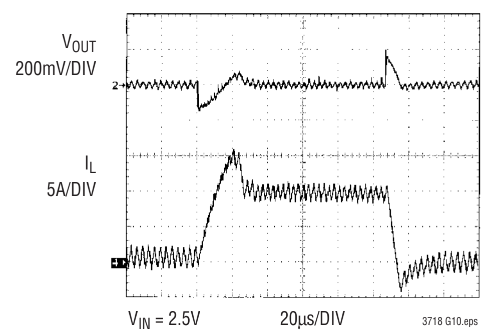


Start-Up Response



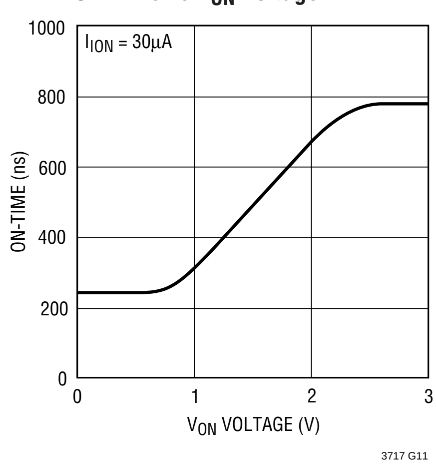
V_{IN} = 2.5V
V_{OUT} = 1.25V
LOAD = 0.2Ω
FIGURE 1 CIRCUIT

Load-Step Transient

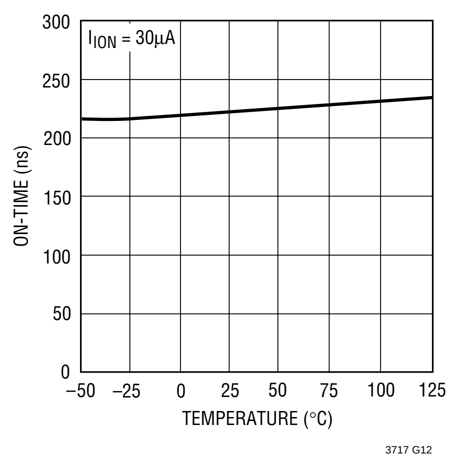


V_{IN} = 2.5V
V_{OUT} = 1.25V
LOAD = 500mA TO 10A STEP
FIGURE 1 CIRCUIT

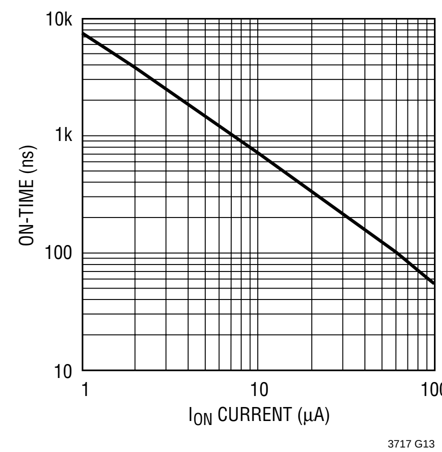
On-Time vs V_{ON} Voltage



On-Time vs Temperature

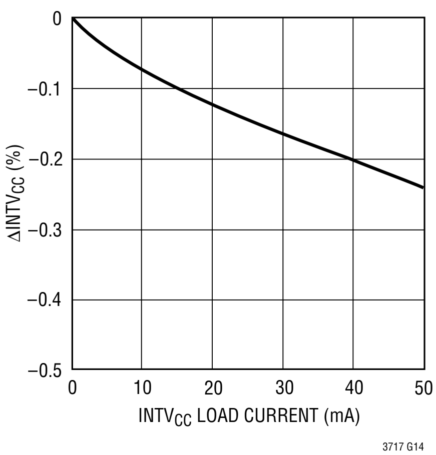


On-Time vs I_{ON} Current

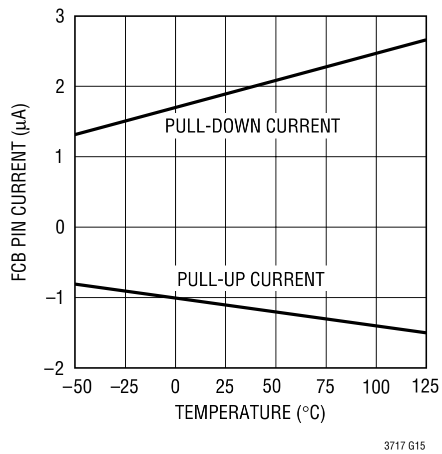


TYPICAL PERFORMANCE CHARACTERISTICS

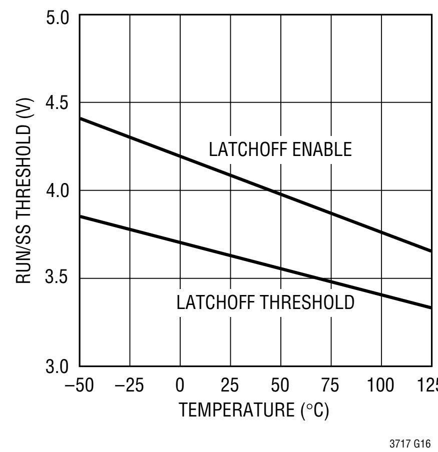
$INTV_{CC}$ Load Regulation



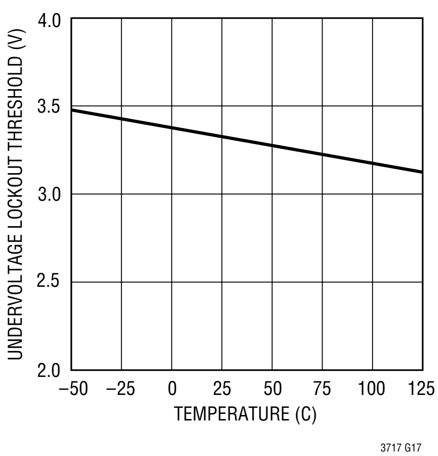
RUN/SS Latchoff Thresholds vs Temperature



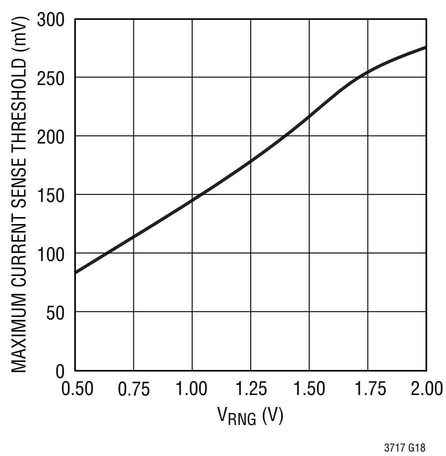
RUN/SS Latchoff Thresholds vs Temperature



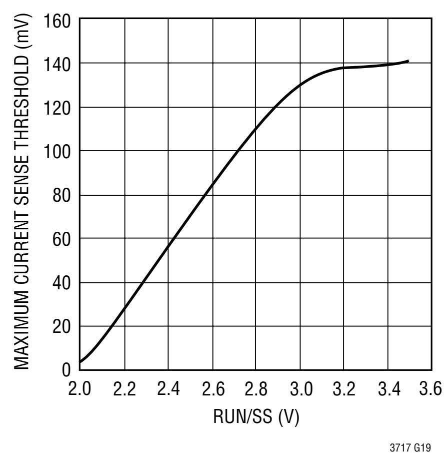
Undervoltage Lockout Threshold vs Temperature



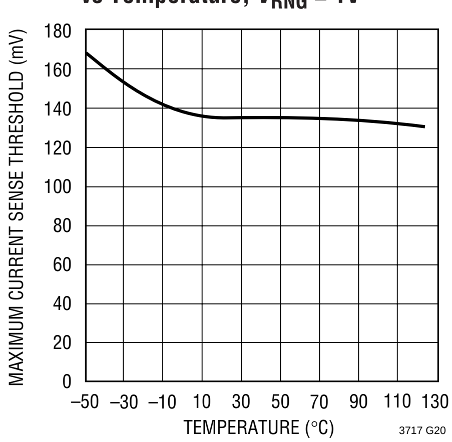
Maximum Current Sense Threshold vs V_{RNG} Voltage



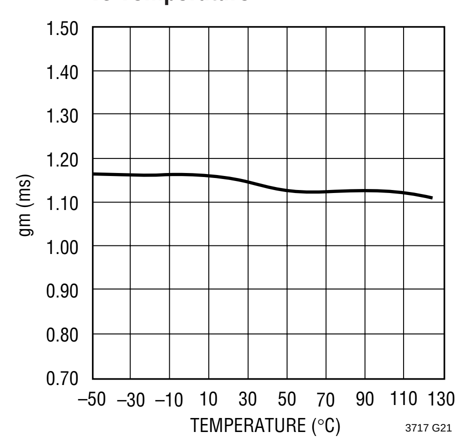
Maximum Current Sense Threshold vs RUN/SS Voltage, V_{RNG} = 1V



Maximum Current Sense Threshold vs Temperature, V_{RNG} = 1V



Error Amplifier gm vs Temperature



PIN FUNCTIONS

RUN/SS (Pin 1): Run Control and Soft-Start Input. A capacitor to ground at this pin sets the ramp time to full output current (approximately 3s/μF) and the time delay for overcurrent latchoff (see Applications Information). Forcing this pin below 0.8V shuts down the device.

PGOOD (Pin 2): Power Good Output. Open drain logic output that is pulled to ground when the output voltage is not within ±10% of the regulation point.

V_{RNG} (Pin 3): Sense Voltage Range Input. The voltage at this pin is ten times the nominal sense voltage at maximum output current and can be set from 0.5V to 2V by a resistive divider from $INTV_{CC}$. The nominal sense voltage defaults to 70mV when this pin is tied to ground, 140mV when tied to $INTV_{CC}$.

I_{TH} (Pin 4): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V with 0.8V corresponding to zero sense voltage (zero current).

SGND (Pin 5): Signal Ground. All small-signal components and compensation components should connect to this ground, which in turn connects to PGND at one point.

I_{ON} (Pin 6): On-Time Current Input. Tie a resistor from V_{IN} to this pin to set the one-shot timer current and thereby set the switching frequency.

V_{FB} (Pin 7): Error Amplifier Feedback Input. This pin connects to V_{OUT} and divides its voltage to 2/3 • V_{FB} through precision internal resistors before it is applied to the input of the error amplifier. Do not apply more than 1.5V on V_{FB}. For higher output voltages, attach an external resistor R2 (1/2 • R1 at V_{REF}) from V_{OUT} to V_{FB}.

V_{REF} (Pin 8): Positive Input of Internal Error Amplifier. This pin connects to an external reference and divides its voltage to 1/3 V_{REF} through precision internal resisters before it is applied to the positive input of the error amplifier. Reference voltage for output voltage, power good threshold, and short-circuit shutdown threshold. Do not apply more than 3V on V_{REF}. If higher voltages are used, connect an external resistor (R1 ≥ 160k) from voltage reference to V_{REF}.

$EXTV_{CC}$ (Pin 9): External V_{CC} Input. When $EXTV_{CC}$ exceeds 4.7V, an internal switch connects this pin to $INTV_{CC}$ and shuts down the internal regulator so that controller and gate drive power is drawn from $EXTV_{CC}$. Do not exceed 7V at this pin and ensure that $EXTV_{CC} < V_{CC}$.

V_{CC} (Pin 10): Bias Input Supply. 4V to 36V operating range. Decouple this pin to PGND with an RC filter (1Ω, 0.1μF).

$INTV_{CC}$ (Pin 11): Internal 5V Regulator Output. The driver and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum of 4.7μF low ESR tantalum or ceramic capacitor.

BG (Pin 12): Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFET between ground and $INTV_{CC}$.

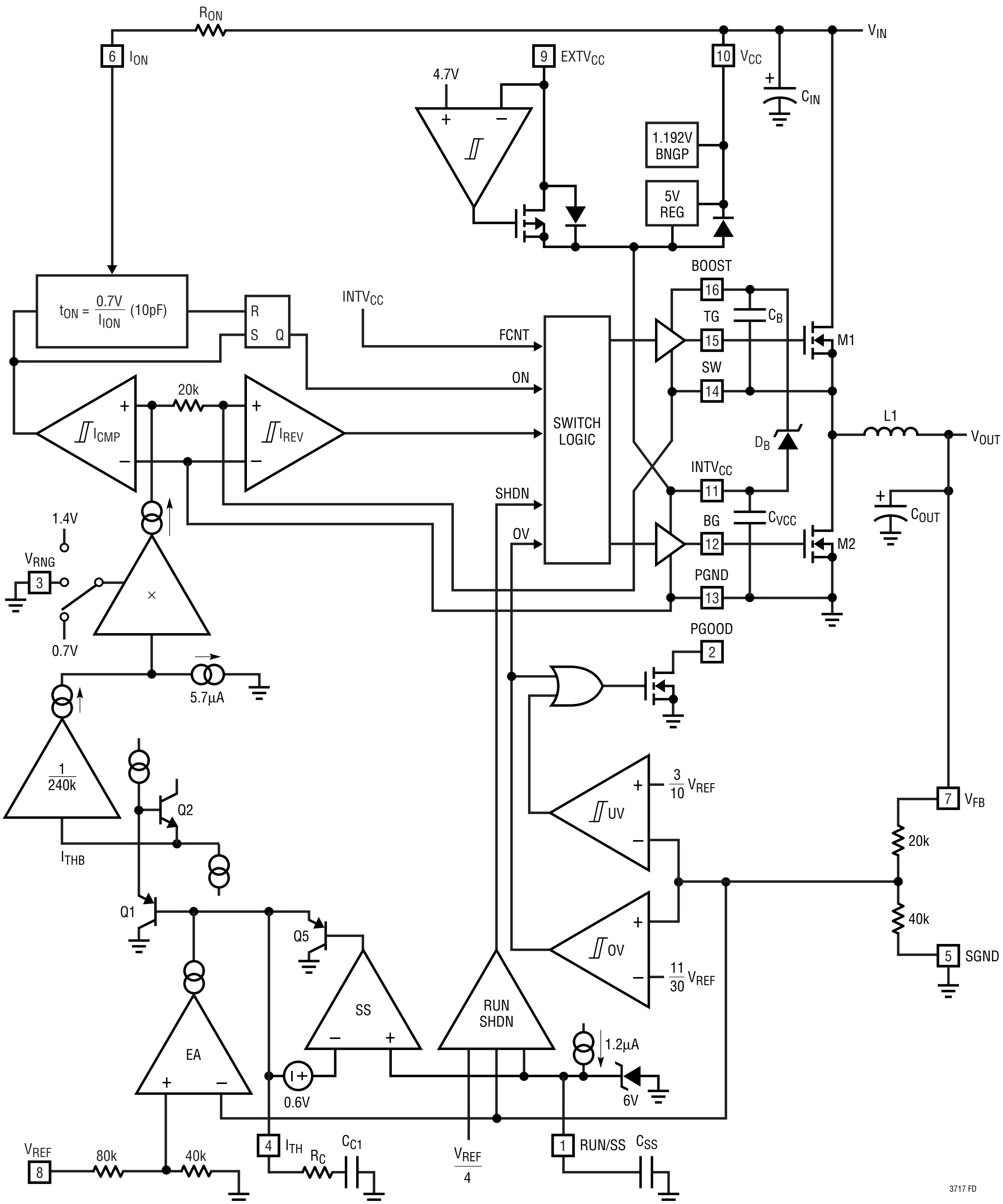
PGND (Pin 13): Power Ground. Connect this pin closely to the source of the bottom N-channel MOSFET, the (–) terminal of C_{VCC} and the (–) terminal of C_{IN}.

SW (Pin 14): Switch Node. The (–) terminal of the bootstrap capacitor C_B connects here. This pin swings from a diode voltage drop below ground up to a diode voltage drop above V_{IN}.

TG (Pin 15): Top Gate Drive. Drives the top N-channel MOSFET with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage SW.

BOOST (Pin 16): Boosted Floating Driver Supply. The (+) terminal of the bootstrap capacitor C_B connects here. This pin swings from a diode voltage drop below $INTV_{CC}$ up to V_{IN} + $INTV_{CC}$.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC3717 is a current mode controller for DC/DC step-down converters. In normal operation, the top MOSFET is turned on for a fixed interval determined by a one-shot timer OST. When the top MOSFET is turned off, the bottom MOSFET is turned on until the current comparator I_{CMP} trips, restarting the one-shot timer and initiating the next cycle. Inductor current is determined by sensing the voltage between the PGND and SW pins using the bottom MOSFET on-resistance . The voltage on the I_{TH} pin sets the comparator threshold corresponding to inductor valley current. The error amplifier EA adjusts this I_{TH} voltage by comparing 2/3 of the feedback signal V_{FB} from the output voltage with a reference equal to 1/3 of the V_{REF} voltage. If the load current increases, it causes a drop in the feedback voltage relative to the reference. The I_{TH} voltage then rises until the average inductor current again matches the load current. As a result in normal DDR operation V_{OUT} is equal to 1/2 of the V_{REF} voltage.

The operating frequency is determined implicitly by the top MOSFET on-time and the duty cycle required to maintain regulation. The one-shot timer generates an on-time that is proportional to the ideal duty cycle, thus holding frequency approximately constant with changes in V_{IN}. The nominal frequency can be adjusted with an external resistor R_{ON}.

Overvoltage and undervoltage comparators OV and UV pull the PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point. Furthermore, in an overvoltage condition, M1 is turned off and M2 is turned on and held on until the overvoltage condition clears.

Pulling the RUN/SS pin low forces the controller into its shutdown state, turning off both M1 and M2. Releasing the pin allows an internal 1.2μA current source to charge up an external soft-start capacitor C_{SS}. When this voltage reaches 1.5V, the controller turns on and begins switching, but with the I_{TH} voltage clamped at approximately 0.6V below the RUN/SS voltage. As C_{SS} continues to charge, the soft-start current limit is removed.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most of the internal controller circuitry is derived from the $INTV_{CC}$ pin. The top MOSFET driver is powered from a floating bootstrap capacitor C_B. This capacitor is recharged from $INTV_{CC}$ through an external Schottky diode D_B when the top MOSFET is turned off. When the $EXTV_{CC}$ pin is grounded, an internal 5V low dropout regulator supplies the $INTV_{CC}$ power from V_{CC}. If $EXTV_{CC}$ rises above 4.7V, the internal regulator is turned off, and an internal switch connects $EXTV_{CC}$ to $INTV_{CC}$. This allows a high efficiency source connected to $EXTV_{CC}$, such as an external 5V supply or a secondary output from the converter, to provide the $INTV_{CC}$ power. Voltages up to 7V can be applied to $EXTV_{CC}$ for additional gate drive. If the V_{CC} voltage is low and $INTV_{CC}$ drops below 3.4V, undervoltage lockout circuitry prevents the power switches from turning on.

APPLICATIONS INFORMATION

The basic LTC3717 application circuit is shown in Figure 1. External component selection is primarily determined by the maximum load current and begins with the selection of the sense resistance and power MOSFET switches. The LTC3717 uses the on-resistance of the synchronous power MOSFET for determining the inductor current. The desired amount of ripple current and operating frequency largely determines the inductor value. Finally, C_{IN} is selected for its ability to handle the large RMS current into the converter and C_{OUT} is chosen with low enough ESR to meet the output voltage ripple and transient specification.

Maximum Sense Voltage and V_{RNG} Pin

Inductor current is determined by measuring the voltage across a sense resistance that appears between the PGND and SW pins. The maximum sense voltage is set by the voltage applied to the V_{RNG} pin and is equal to approximately $(0.13)V_{RNG}$ for sourcing current and $(0.17)V_{RNG}$ for sinking current. The current mode control loop will not allow the inductor current valleys to exceed $(0.13)V_{RNG}/R_{SENSE}$ for sourcing and $(0.17)V_{RNG}/R_{SENSE}$ for sinking. In practice, one should allow some margin for variations in

APPLICATIONS INFORMATION

the LTC3717 and external component values and a good guide for selecting the sense resistance is:

$$R_{SENSE} = \frac{V_{RNG}}{10 \bullet I_{OUT(MAX)}}$$

An external resistive divider from $INTV_{CC}$ can be used to set the voltage of the V_{RNG} pin between 0.5V and 2V resulting in nominal sense voltages of 50mV to 200mV. Additionally, the V_{RNG} pin can be tied to SGND or $INTV_{CC}$ in which case the nominal sense voltage defaults to 70mV or 140mV, respectively. The maximum allowed sense voltage is about 1.3 times this nominal value for positive output current and 1.7 times the nominal value for negative output current.

Power MOSFET Selection

The LTC3717 requires two external N-channel power MOSFETs, one for the top (main) switch and one for the bottom (synchronous) switch. Important parameters for the power MOSFETs are the breakdown voltage $V_{(BR)DSS}$, threshold voltage $V_{(GS)TH}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and maximum current $I_{DS(MAX)}$.

The gate drive voltage is set by the 5V $INTV_{CC}$ supply. Consequently, logic-level threshold MOSFETs must be used in LTC3717 applications. If the input voltage is expected to drop below 5V, then sub-logic level threshold MOSFETs should be considered.

When the bottom MOSFET is used as the current sense element, particular attention must be paid to its on-resistance. MOSFET on-resistance is typically specified with a maximum value $R_{DS(ON)(MAX)}$ at 25°C. In this case, additional margin is required to accommodate the rise in MOSFET on-resistance with temperature:

$$R_{DS(ON)(MAX)} = \frac{R_{SENSE}}{\rho_T}$$

The ρ_T term is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically about 0.4%/°C as shown in Figure 2. For a maximum junction temperature of 100°C, using a value ρ_T = 1.3 is reasonable.

The power dissipated by the top and bottom MOSFETs strongly depends upon their respective duty cycles and the load current. During LTC3717's normal operation, the duty cycles for the MOSFETs are:

$$D_{TOP} = \frac{V_{OUT}}{V_{IN}}$$

$$D_{BOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The resulting power dissipation in the MOSFETs at maximum output current are:

$$P_{TOP} = D_{TOP}\, I_{OUT(MAX)}^2\, \rho_{T(TOP)}\, R_{DS(ON)(MAX)} + k\, V_{IN}^2\, I_{OUT(MAX)}\, C_{RSS}\, f$$

$$P_{BOT} = D_{BOT}\, I_{OUT(MAX)}^2\, \rho_{T(BOT)}\, R_{DS(ON)(MAX)}$$

Both MOSFETs have I^2R losses and the top MOSFET includes an additional term for transition losses, which are largest at high input voltages. The constant $k = 1.7A^{-1}$ can be used to estimate the amount of transition loss. The bottom MOSFET losses are greatest when the bottom duty cycle is near 100%, during a short-circuit or at high input voltage.

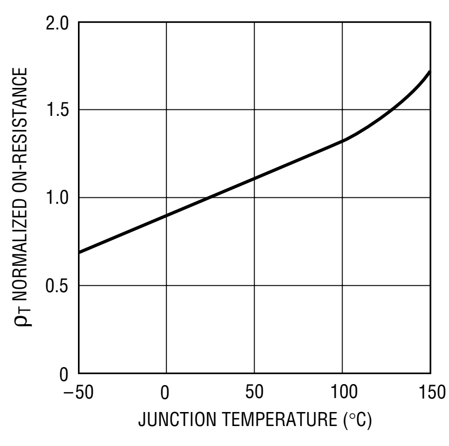


Figure 2. $R_{DS(ON)}$ vs. Temperature

Operating Frequency

The choice of operating frequency is a tradeoff between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses but requires larger inductance and/or capacitance in order to maintain low output ripple voltage.

The operating frequency of LTC3717 applications is determined implicitly by the one-shot timer that controls the

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on-time t_{ON} of the top MOSFET switch. The on-time is set by the current into the I_{ON} pin according to:

$$t_{ON} = \frac{(0.7V)}{I_{ION}}(10pF)$$

Tying a resistor R_{ON} from V_{IN} to the I_{ON} pin yields an on-time inversely proportional to V_{IN}. For a step-down converter, this results in approximately constant frequency operation as the input supply varies:

$$f = \frac{V_{OUT}}{(0.7V)\,R_{ON}(10pF)}\,[H_Z]$$

Because the voltage at the I_{ON} pin is about 0.7V, the current into this pin is not exactly inversely proportional to V_{IN}, especially in applications with lower input voltages. A more exact equation taking in account the 0.7V drop on the I_{ON} pin is:

$$f = \frac{V_{OUT}(V_{IN} - 0.7V)}{(0.7V)\,R_{ON}(10pF)V_{IN}}\,[H_Z]$$

To correct for this error, an additional resistor R_{ON2} connected from the I_{ON} pin to the 5V $INTV_{CC}$ supply will further stabilize the frequency.

$$R_{ON2} = \frac{5V}{0.7V}R_{ON}$$

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \left(\frac{V_{OUT}}{f\,L}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a tradeoff between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. The largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f\,\Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Panasonic, Coiltronics, Coilcraft and Toko.

Schottky Diode D1 Selection

The Schottky diode D1 shown in Figure 1 conducts during the dead time between the conduction of the power MOSFET switches. It is intended to prevent the body diode of the bottom MOSFET from turning on and storing charge during the dead time, which can cause a modest (about 1%) efficiency loss. The diode can be rated for about one half to one fifth of the full load current since it is on for only a fraction of the duty cycle. In order for the diode to be effective, the inductance between it and the bottom MOSFET must be as small as possible, mandating that these components be placed adjacently. The diode can be omitted if the efficiency loss is tolerable.

C_{IN} and C_{OUT} Selection

The input capacitance C_{IN} is required to filter the square wave current at the drain of the top MOSFET. Use a low ESR capacitor sized to handle the maximum RMS current.

$$I_{RMS} \cong I_{OUT(MAX)}\frac{V_{OUT}}{V_{IN}}\sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple

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current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to derate the capacitor.

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The output ripple ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} \le \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

Since ΔI_L increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications providing that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. When used as input capacitors, care must be taken to ensure that ringing from inrush currents and switching does not pose an overvoltage hazard to the power switches and controller. To dampen input voltage transients, add a small 5μF to 50μF aluminum electrolytic capacitor with an ESR in the range of 0.5Ω to 2Ω. High performance through-hole capacitors may also be used, but an additional ceramic capacitor in parallel is recommended to reduce the effect of their lead inductance.

Top MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor C_B connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. This capacitor is charged through diode D_B from $INTV_{CC}$ when the switch node is low. When the top MOSFET turns on, the switch node rises to V_{IN} and the BOOST pin rises to approximately $V_{IN} + INTV_{CC}$. The boost capacitor needs to store about 100 times the gate charge required by the top MOSFET. In most applications 0.1μF to 0.47μF, X5R or X7R dielectric capacitor is adequate.

Fault Condition: Current Limit

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the LTC3717, the maximum sense voltage is controlled by the voltage on the V_{RNG} pin. With valley current control, the maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current. The corresponding output current limits are:

$$I_{LIMIT}\,POSITIVE = \frac{V_{SNS(MAX)}}{R_{DS(ON)}\ \rho_T} + \frac{1}{2}\Delta I_L$$

$$I_{LIMIT}\,NEGATIVE = \frac{V_{SNS(MIN)}}{R_{DS(ON)}\ \rho_T} - \frac{1}{2}\Delta I_L$$

The current limit value should be checked to ensure that $I_{LIMIT(MIN)} > I_{OUT(MAX)}$. The minimum value of current limit generally occurs with the largest V_{IN} at the highest ambient temperature, conditions that cause the largest power loss in the converter. Note that it is important to check for self-consistency between the assumed MOSFET junction temperature and the resulting value of I_{LIMIT} which heats the MOSFET switches.

Caution should be used when setting the current limit based upon the $R_{DS(ON)}$ of the MOSFETs. The maximum current limit is determined by the minimum MOSFET on-resistance. Data sheets typically specify nominal and maximum values for $R_{DS(ON)}$, but not a minimum. A reasonable assumption is that the minimum $R_{DS(ON)}$ lies the same amount below the typical value as the maximum lies above it. Consult the MOSFET manufacturer for further guidelines.

Minimum Off-time and Dropout Operation

The minimum off-time $t_{OFF(MIN)}$ is the smallest amount of

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time that the LTC3717 is capable of turning on the bottom MOSFET, tripping the current comparator and turning the MOSFET back off. This time is generally about 300ns. The minimum off-time limit imposes a maximum duty cycle of $t_{ON}/(t_{ON} + t_{OFF(MIN)})$. If the maximum duty cycle is reached, due to a dropping input voltage for example, then the output will drop out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = V_{OUT}\frac{t_{ON} + t_{OFF(MIN)}}{t_{ON}}$$

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces the 5V supply that powers the drivers and internal circuitry within the LTC3717. The $INTV_{CC}$ pin can supply up to 50mA RMS and must be bypassed to ground with a minimum of 4.7µF tantalum or other low ESR capacitor. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate drivers. Applications using large MOSFETs with a high input voltage and high frequency of operation may cause the LTC3717 to exceed its maximum junction temperature rating or RMS current rating. Most of the supply current drives the MOSFET gates unless an external $EXTV_{CC}$ source is used. In continuous mode operation, this current is $I_{GATECHG} = f(Q_{g(TOP)} + Q_{g(BOT)})$. The junction temperature can be estimated from the equations given in Note 2 of the Electrical Characteristics. For example, the LTC3717CGN is limited to less than 14mA from a 30V supply:

$$T_J = 70°C + (14mA)(30V)(130°C/W) = 125°C$$

For larger currents, consider using an external supply with the $EXTV_{CC}$ pin.

$EXTV_{CC}$ Connection

The $EXTV_{CC}$ pin can be used to provide MOSFET gate drive and control power from the output or another external source during normal operation. Whenever the $EXTV_{CC}$ pin is above 4.7V the internal 5V regulator is shut off and an internal 50mA P-channel switch connects the $EXTV_{CC}$ pin to $INTV_{CC}$. $INTV_{CC}$ power is supplied from $EXTV_{CC}$ until this pin drops below 4.5V. Do not apply more than 7V to the $EXTV_{CC}$ pin and ensure that $EXTV_{CC} \le V_{CC}$. The following list summarizes the possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. $INTV_{CC}$ is always powered from the internal 5V regulator.

2. $EXTV_{CC}$ connected to an external supply. A high efficiency supply compatible with the MOSFET gate drive requirements (typically 5V) can improve overall efficiency.

3. $EXTV_{CC}$ connected to an output derived boost network. The low voltage output can be boosted using a charge pump or flyback winding to greater than 4.7V. The system will start-up using the internal linear regulator until the boosted output supply is available.

External Gate Drive Buffers

The LTC3717 drivers are adequate for driving up to about 60nC into MOSFET switches with RMS currents of 50mA. Applications with larger MOSFET switches or operating at frequencies requiring greater RMS currents will benefit from using external gate drive buffers such as the LTC1693. Alternately, the external buffer circuit shown in Figure 4 can be used. Note that the bipolar devices reduce the signal swing at the MOSFET gate, and benefit from an increased $EXTV_{CC}$ voltage of about 6V.

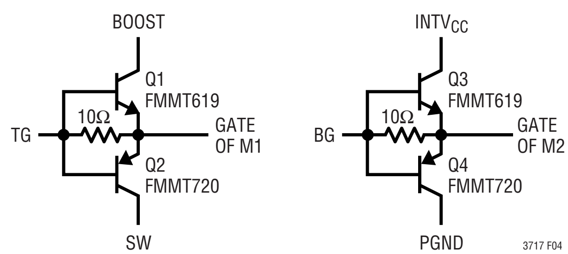

Figure 4. Optional External Gate Driver

Soft-Start and Latchoff with the RUN/SS Pin

The RUN/SS pin provides a means to shut down the LTC3717 as well as a timer for soft-start and overcurrent latchoff. Pulling the RUN/SS pin below 0.8V puts the LTC3717 into a low quiescent current shutdown (I_Q < 30µA). Releasing the pin allows an internal 1.2µA current source to charge up the external timing capacitor C_{SS}. If RUN/SS has been pulled all the way to ground, there is a delay before starting of about:

$$t_{DELAY} = \frac{1.5V}{1.2\mu A}C_{SS} = (1.3s/\mu F)C_{SS}$$

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When the voltage on RUN/SS reaches 1.5V, the LTC3717 begins operating with a clamp on I_{TH} of approximately 0.9V. As the RUN/SS voltage rises to 3V, the clamp on I_{TH} is raised until its full 2.4V range is available. This takes an additional 1.3s/μF. The pin can be driven from logic as shown in Figure 5. Diode D1 reduces the start delay while allowing C_{SS} to charge up slowly for the soft-start function.

After the controller has been started and given adequate time to charge up the output capacitor, C_{SS} is used as a short-circuit timer. After the RUN/SS pin charges above 4V, if the output voltage falls below 75% of its regulated value, then a short-circuit fault is assumed. A 1.8μA current then begins discharging C_{SS}. If the fault condition persists until the RUN/SS pin drops to 3.5V, then the controller turns off both power MOSFETs, shutting down the converter permanently. The RUN/SS pin must be actively pulled down to ground in order to restart operation.

The overcurrent protection timer requires that the soft-start timing capacitor C_{SS} be made large enough to guarantee that the output is in regulation by the time C_{SS} has reached the 4V threshold. In general, this will depend upon the size of the output capacitance, output voltage and load current characteristic. A minimum soft-start capacitor can be estimated from:

$$C_{SS} > C_{OUT}\, V_{OUT}\, R_{SENSE}\, (10^{-4}\ [\mathrm{F/V\ s}])$$

Generally 0.1μF is more than sufficient.

Overcurrent latchoff operation is not always needed or desired. The feature can be overridden by adding a pull-up current greater than 5μA to the RUN/SS pin. The additional current prevents the discharge of C_{SS} during a fault and also shortens the soft-start period. Using a resistor to V_{IN} as shown in Figure 5a is simple, but slightly increases shutdown current. Connecting a resistor to $INTV_{CC}$ as shown in Figure 5b eliminates the additional shutdown current, but requires a diode to isolate C_{SS}. Any pull-up network must be able to pull RUN/SS above the 4.5V maximum threshold that arms the latchoff circuit and overcome the 4μA maximum discharge current.

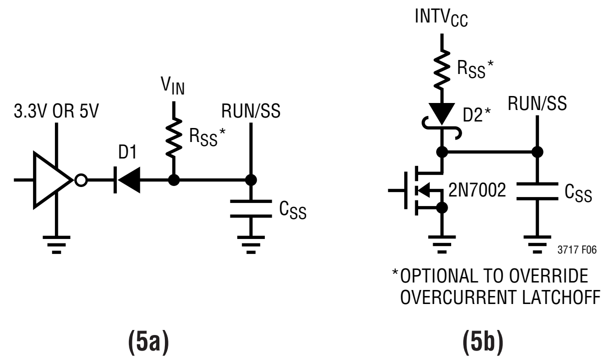

Figure 5. RUN/SS Pin Interfacing with Latchoff Defeated

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LTC3717 circuits:

1. DC I^2R losses. These arise from the resistances of the MOSFETs, inductor and PC board traces and cause the efficiency to drop at high output currents. In continuous mode the average output current flows through L, but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and the board traces to obtain the DC I^2R loss. For example, if $R_{DS(ON)} = 0.01\Omega$ and $R_L = 0.005\Omega$, the loss will range from 15mW to 1.5W as the output current varies from 1A to 10A.

2. Transition loss. This loss arises from the brief amount of time the top MOSFET spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. The loss is significant at input voltages above 20V and can be estimated from:

$$\text{Transition Loss} \cong (1.7A^{-1})\ V_{IN}^2\ I_{OUT}\ C_{RSS}\ f$$

3. $INTV_{CC}$ current. This is the sum of the MOSFET driver and control currents. This loss can be reduced by supplying $INTV_{CC}$ current through the $EXTV_{CC}$ pin from a high

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efficiency source, such as an output derived boost network or alternate supply if available.

4. C_{IN} loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator. It must have a very low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

Other losses, including C_{OUT} ESR loss, Schottky diode D1 conduction loss during dead time and inductor core loss generally account for less than 2% additional loss.

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. The I_{TH} pin external components shown in Figure 6 will provide adequate compensation for most applications. For a detailed explanation of switching control loop theory see Application Note 76.

Design Example

As a design example, take a supply with the following specifications: $V_{IN} = V_{REF} = 2.5V$, $V_{EXTVCC} = 5V$, $V_{OUT} = 1.25V \pm 5\%$, $I_{OUT(MAX)} = 10A$, f = 250kHz. First, calculate the timing resistor with $V_{ON} = V_{OUT}$:

$$R_{ON} = \frac{1.25V(2.5V - 0.7V)}{(0.7V)(250kHz)(10pF)2.5V} = 514k\Omega$$

and choose the inductor for about 40% ripple current at the maximum V_{IN}:

$$L = \frac{1.25V}{(250kHz)(0.4)(10A)}\left(1 - \frac{1.25V}{2.5V}\right) = 0.63\mu H$$

Selecting a standard value of 0.68μH results in a maximum ripple current of:

$$\Delta I_L = \frac{1.25V}{(250kHz)(0.68\mu H)}\left(1 - \frac{1.25V}{2.5V}\right) = 3.7A$$

Next, choose the synchronous MOSFET switch. Choosing a Si4874 ($R_{DS(ON)}$ = 0.0083Ω (NOM) 0.010Ω (MAX), θ_{JA} = 40°C/W) yields a nominal sense voltage of:

$$V_{SNS(NOM)} = (10A)(1.3)(0.0083\Omega) = 108mV$$

Tying V_{RNG} to 1.1V will set the current sense voltage range for a nominal value of 110mV with current limit occurring at 143mV. To check if the current limit is acceptable, assume a junction temperature of about 40°C above a 70°C ambient with $\rho_{110°C} = 1.4$:

$$I_{LIMIT} \geq \frac{143mV}{(1.4)(0.010\Omega)} + \frac{1}{2}(3.7A) = 12.1A$$

and double check the assumed T_J in the MOSFET:

$$P_{BOT} = \frac{2.5V - 1.25V}{2.5V}(12.1A)^2(1.4)(0.010\Omega) = 1.02W$$

$$T_J = 70°C + (1.02W)(40°C/W) = 111°C$$

Because the top MOSFET is on roughly the same amount of time as the bottom MOSFET, the same Si4874 can be used as the synchronous MOSFET.

The junction temperatures will be significantly less at nominal current, but this analysis shows that careful attention to heat sinking will be necessary in this circuit.

C_{IN} is chosen for an RMS current rating of about 5A at 85°C. The output capacitors are chosen for a low ESR of 0.013Ω to minimize output voltage changes due to inductor ripple current and load steps. For current sinking applications where current flows back to the input through the top transistor, output capacitors with a similar amount of bulk C and ESR should be placed on the input as well.

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(This is typically the case, since V_{IN} is derived from another DC/DC converter.) The ripple voltage will be only:

$$\Delta V_{OUT(RIPPLE)} = \Delta I_{L(MAX)} (ESR) = (4A)(0.013\Omega) = 52mV$$

However, a 0A to 10A load step will cause an output change of up to:

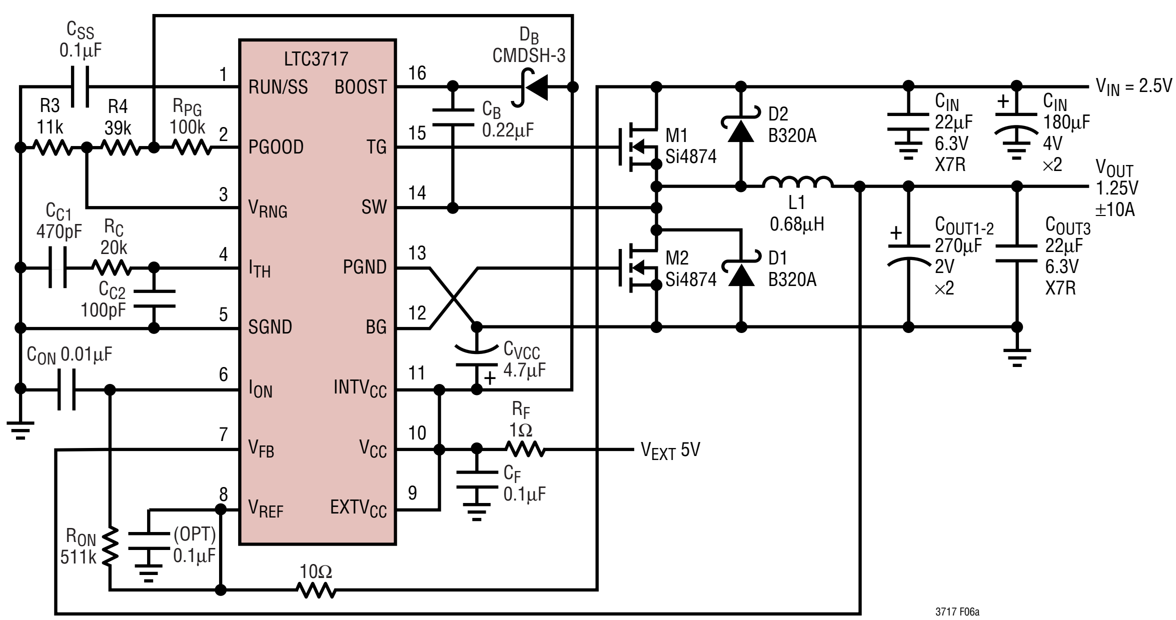
$$\Delta V_{OUT(STEP)} = \Delta I_{LOAD} (ESR) = (10A)(0.013\Omega) = 130mV$$

An optional 22µF ceramic output capacitor is included to minimize the effect of ESL in the output ripple. The complete circuit is shown in Figure 6.

PC Board Layout Checklist

When laying out a PC board follow one of the two suggested approaches. The simple PC board layout requires a dedicated ground plane layer. Also, for higher currents, it is recommended to use a multilayer board to help with heat sinking power components.

- The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.
- Place C_{IN}, C_{OUT}, MOSFETs, D1 and inductor all in one compact area. It may help to have some components on the bottom side of the board.
- Place LTC3717 chip with pins 9 to 16 facing the power components. Keep the components connected to pins 1 to 8 close to LTC3717 (noise sensitive components).
- Use an immediate via to connect the components to ground plane including SGND and PGND of LTC3717. Use several bigger vias for power components.
- Use compact plane for switch node (SW) to improve cooling of the MOSFETs and to keep EMI down.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.



CIN, COUT1-2: CORNELL DUBILIER ESRE181E04B
L1: SUMIDA CEP125-0R68MC-H

Figure 6. Design Example: 1.25V/±10A at 250kHz

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- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power component. You can connect the copper areas to any DC net (V_{IN}, V_{OUT}, GND or to any other DC rail in your system).

When laying out a printed circuit board, without a ground plane, use the following checklist to ensure proper operation of the controller. These items are also illustrated in Figure 7.

- Segregate the signal and power grounds. All small signal components should return to the SGND pin at one point which is then tied to the PGND pin close to the source of M2.
- Place M2 as close to the controller as possible, keeping the PGND, BG and SW traces short.
- Connect the input capacitor(s) C_{IN} close to the power MOSFETs. This capacitor carries the MOSFET AC current.
- Keep the high dV/dT SW, BOOST and TG nodes away from sensitive small-signal nodes.
- Connect the $INTV_{CC}$ decoupling capacitor C_{VCC} closely to the $INTV_{CC}$ and PGND pins.
- Connect the top driver boost capacitor C_B closely to the BOOST and SW pins.
- Connect the V_{CC} pin decoupling capacitor C_F closely to the V_{CC} and PGND pins.

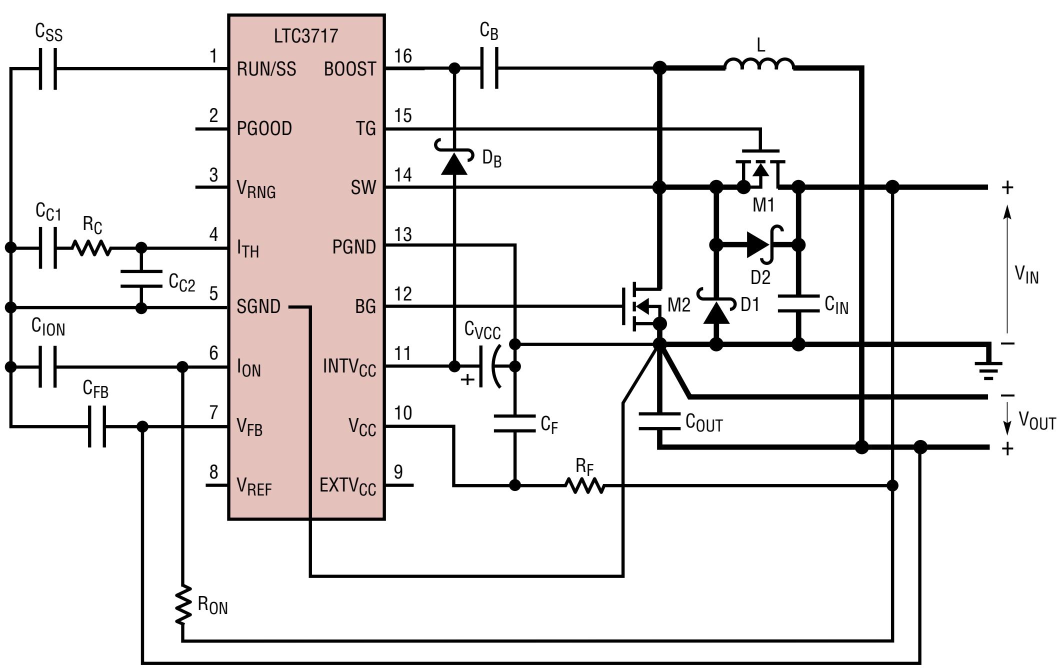
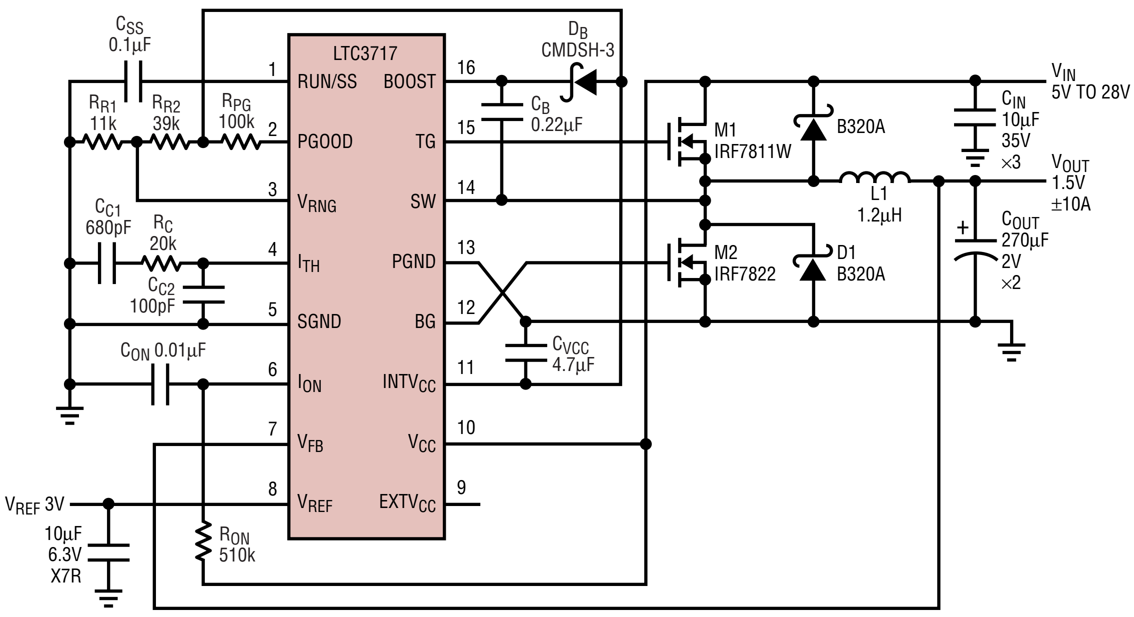


Figure 7. LTC3717 Layout Diagram

TYPICAL APPLICATIONS

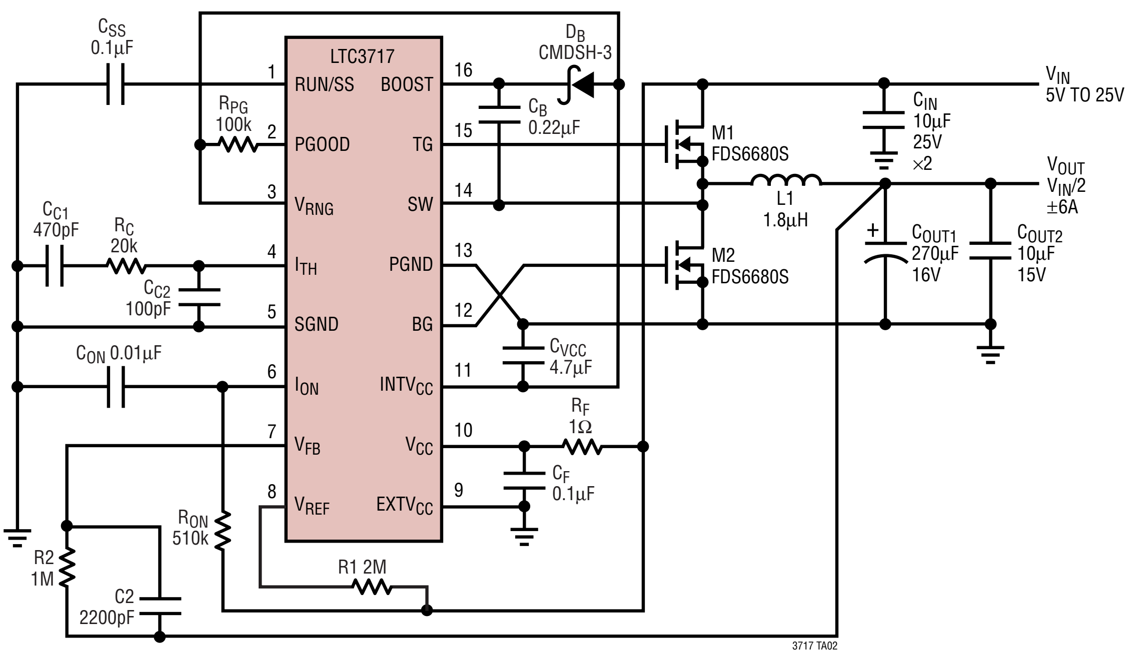
1.5V/±10A at 300kHz from 5V to 28V Input



C_{OUT}: CORNELL DUBILIER ESRE271M02B

TYPICAL APPLICATIONS

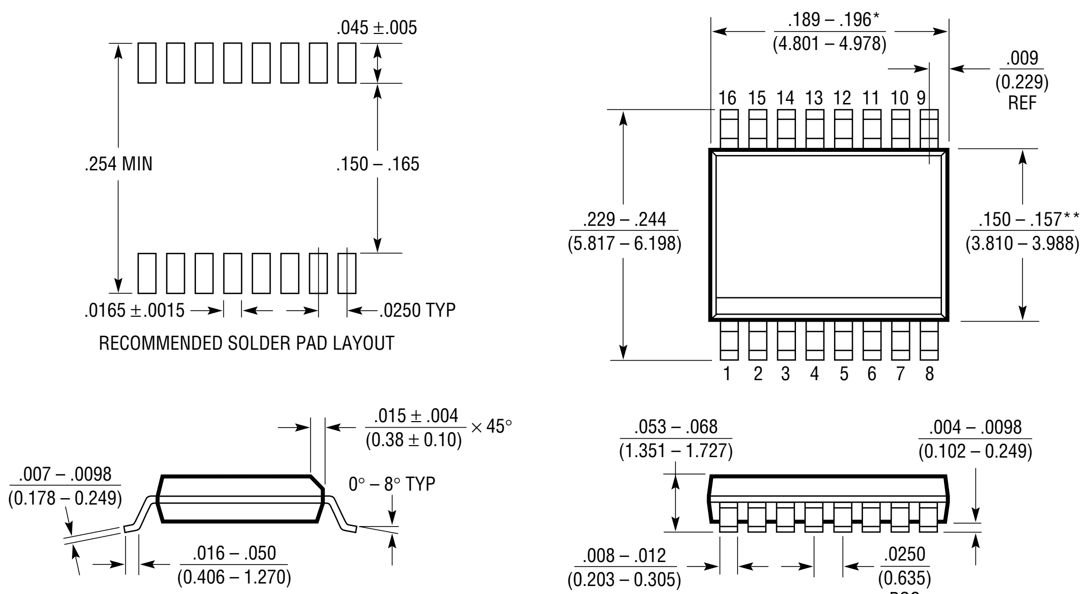
High Voltage Half (V_{IN}) Power Supply



C_{IN}: TAIYO YUDEN TMK432BJ106MM
C_{OUT1}: SANYO, OS-CON 16SP270
C_{OUT2}: TAIYO YUDEN JMK316BJ106ML
L1: TOKO 919AS-1R8N

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0502