Photoflash Capacitor Chargers with Automatic Refresh

FEATURES

- **Charges 220µF to 320V in 3.7 Seconds from 5V (LT3420)**
- **Charges 100µF to 320V in 3.5 Seconds from 5V (LT3420-1)**
- **Charges Any Size Photoflash Capacitor**
- **Supports Operation from Two AA Cells or Any Supply from 1.8V to 16V**
- **Controlled Peak Switch Current: 1.4A (LT3420) 1.0A (LT3420-1)**
- **Controlled Input Current: 840mA (LT3420) 450mA (LT3420-1)**
- **Uses Standard Transformers**
- **Efficient Flyback Operation (>75% Typical)**
- Adjustable Output
- Automatic Refresh
- Charge Complete Indicator
- No High Voltage Zener Diode Required
- No Output Voltage Divider Required
- Small 10-Lead MSOP Package
- Small 10-Lead (3mm × 3mm) DFN Package

APPLICATIONS

- Digital Camera Flash Unit
- Film Camera Flash Unit
- High Voltage Power Supplies

DESCRIPTION

The LT®3420/LT3420-1 charge high voltage photoflash capacitors quickly and efficiently. Designed for use in both digital and film cameras, these devices use a flyback topology to achieve efficiencies up to four times better than competing flash modules. A unique adaptive off-time control algorithm* maintains current-limited continuous mode transformer operation throughout the entire charge cycle, eliminating the high inrush current often found in modules.

The LT3420/LT3420-1 output voltage sensing scheme* monitors the flyback voltage to indirectly regulate the output voltage, eliminating an output resistor divider or discrete zener diode. This feature allows the capacitor to be held at a fully charged state without excessive power consumption. Automatic refresh (which can be defeated) allows the capacitor to remain charged while consuming an average input current of about 2mA, at a user-defined refresh rate. A logic high on the CHARGE pin initiates charging, while the DONE pin signals that the capacitor is fully charged.

The LT3420/LT3420-1 are available in 10-Lead MSOP and (3mm × 3mm) DFN packages.

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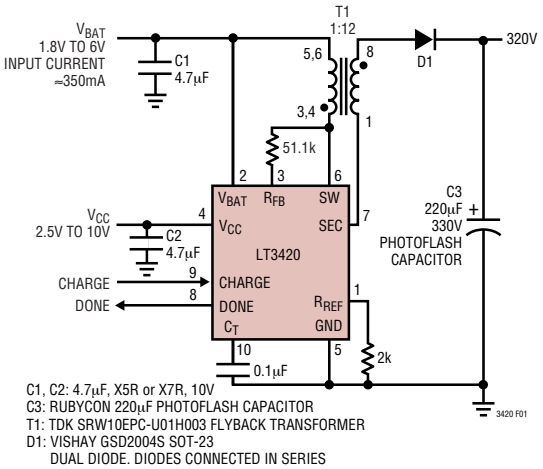
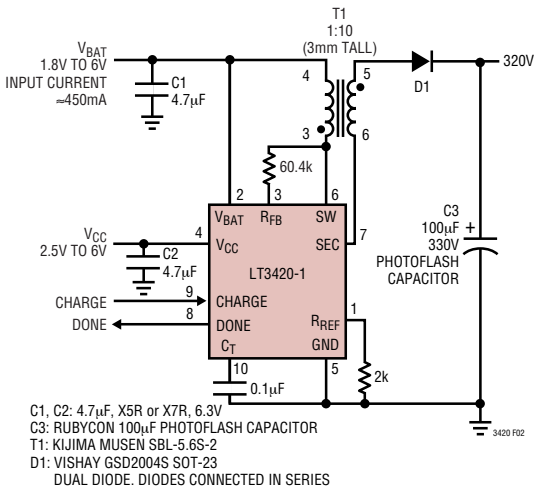
TYPICAL APPLICATION



C1, C2: 4.7µF, X5R or X7R, 10V
C3: RUBYCON 220µF PHOTOFLASH CAPACITOR
T1: TDK SRW10EPC-U01H003 FLYBACK TRANSFORMER
D1: VISHAY GSD2004S SOT-23
DUAL DIODE. DIODES CONNECTED IN SERIES

DANGER HIGH VOLTAGE OPERATION BY HIGH VOLTAGE TRAINED PERSONNEL ONLY

Figure 1. High Charge Rate LT3420 Photoflash Circuit



C1, C2: 4.7µF, X5R or X7R, 6.3V
C3: RUBYCON 100µF PHOTOFLASH CAPACITOR
T1: KIJIMA MUSEN SBL-5.6S-2
D1: VISHAY GSD2004S SOT-23
DUAL DIODE. DIODES CONNECTED IN SERIES

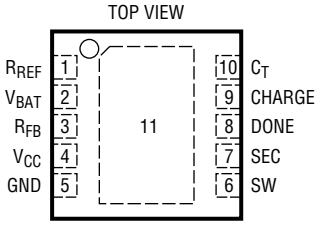
Figure 2. Small Size LT3420-1 Photoflash Circuit

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} Voltage 16V
V_{BAT} Voltage 16V
SW Voltage (Note 2)
LT3420 ..... 38V
LT3420-1 ..... 50V
SEC Current ..... ±200mA
R_{FB} Current ..... ±3mA
R_{REF} Voltage 2.5V
CHARGE Voltage 16V
CT Voltage 1.5V
DONE Voltage 16V
Current into DONE Pin ..... ±1mA
Maximum Junction Temperature ..... 125°C
Operating Ambient Temperature Range
(Note 3) ..... –40°C to 85°C
Storage Temperature Range ..... –40°C to 125°C
Lead Temperature (Soldering, 10 sec)
(For MS Package only) ..... 300°C

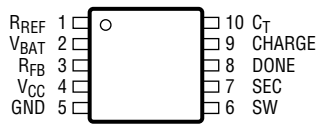
PACKAGE/ORDER INFORMATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 3°C/W
EXPOSED PAD IS GND (PIN 11)
AND MUST BE SOLDERED TO PCB

ORDER PART NUMBER
LT3420EDD LT3420EDD-1
DD PART MARKING
LBJW LBJX



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 100°C/W, θ_{JC} = 45°C/W
(4-LAYER BOARD)

ORDER PART NUMBER
LT3420EMS LT3420EMS-1
MS PART MARKING
LTYH LTAJG

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = V_{BAT} = 3.3V, V_{CHARGE} = V_{CC} unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operating Voltage, V_{CC}		●		2.2	2.5	V
Maximum Operating Voltage, V_{CC}					16	V
V_{CC} UVLO Hysteresis				40		mV
Minimum V_{BAT} Voltage				1.6	1.8	V
Maximum V_{BAT} Voltage					16	V
V_{BAT} UVLO Hysteresis				275		mV
R_{REF} Threshold Voltage		 ●	0.98 0.975	1.00	1.02 1.025	V V
R_{REF} Pin Bias Current	V_{RREF} = 0V, Switching V_{RFB} = V_{BAT} – 0.2V (Note 4)			2	4	µA
Quiescent Current	V_{RREF} = 1.1V, Not Switching			90	130	µA
Quiescent Current in Shutdown	V_{CHARGE} = 0V, V_{IN} = 3.3V			0.01	1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = V_{BAT} = 3.3V, V_{CHARGE} = V_{CC} unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Primary Side Current Limit	LT3420 (Note 5) LT3420-1 (Note 5)		1.20 0.75	1.4 0.9	1.60 1.05	A A
Secondary Side Current Limit	LT3420 (Note 5) LT3420-1 (Note 5)		20 5	40 15	50 25	mA mA
Leakage Blanking Pulse Width	LT3420 LT3420-1			200 0		ns ns
Refresh Timer Charge/Discharge Current	V_{CT} = 0.75V		1.5	2.5	3.5	µA
Refresh Timer Upper Threshold			0.9	1.0	1.1	V
Refresh Timer Lower Threshold			0.45	0.5	0.55	V
Switch V_{CESAT}	LT3420, SW = 1A (Note 5) LT3420-1, SW = 0.5A (Note 5)			220 130	340 230	mV mV
Switch Leakage Current	V_{SW} = 38V (LT3420), V_{SW} = 50V (LT3420-1)			0.01	1	µA
CHARGE Input Voltage High			1.5			V
CHARGE Input Voltage Low					0.2	V
CHARGE Pin Bias Current	V_{CHARGE} = 3V V_{CHARGE} = 0V			4.5 0.01	15 0.1	µA µA
DONE Output Signal High	100k from V_{CC} to DONE			3.3		V
DONE Output Signal Low	33µA into DONE Pin			100	200	mV

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Rated breakdown with LT3420 in power delivery mode and power switch off.

Note 3: The LT3420/LT3420-1 are guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

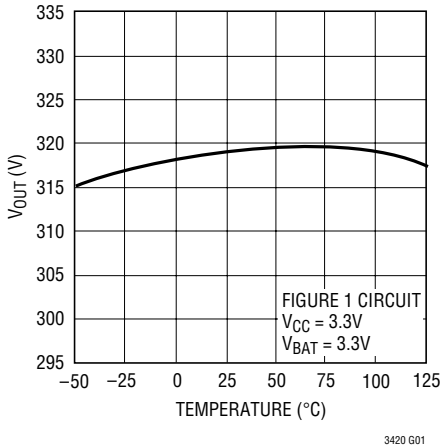
Note 4: Bias current flows out of R_{FB} pin.

Note 5: Current limit and V_{CESAT} guaranteed by design and/or correlation to static test for DD package.

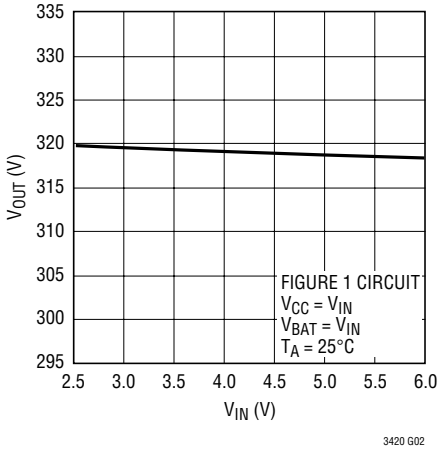
TYPICAL PERFORMANCE CHARACTERISTICS

Graphs apply to both the LT3420 and LT3420-1 unless otherwise noted.

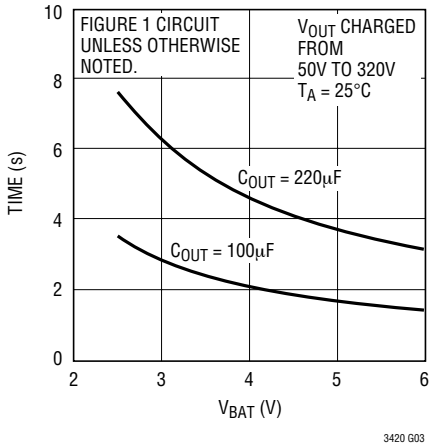
Output Voltage in Refresh Mode, LT3420



Output Voltage in Refresh Mode, LT3420



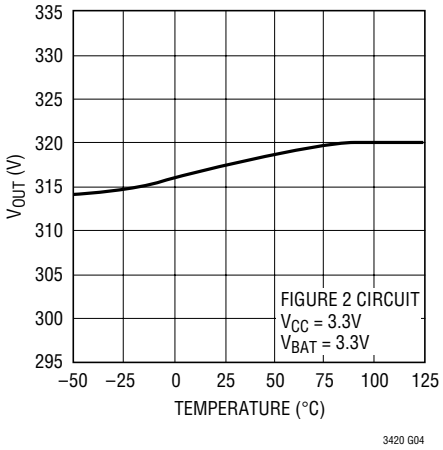
Charge Time, LT3420



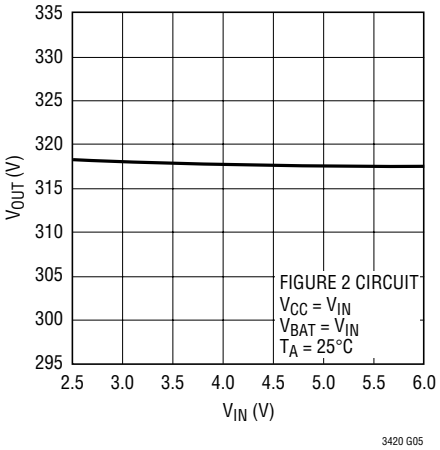
TYPICAL PERFORMANCE CHARACTERISTICS

Graphs apply to both the LT3420 and LT3420-1 unless otherwise noted.

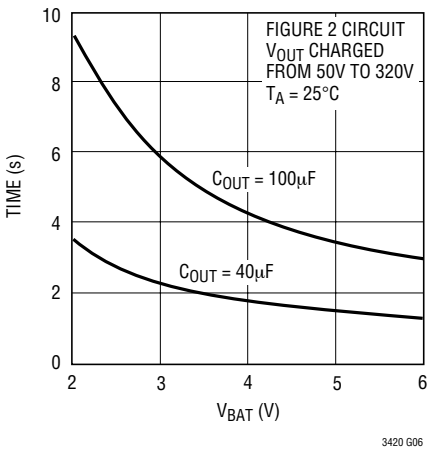
Output Voltage in Refresh Mode, LT3420-1



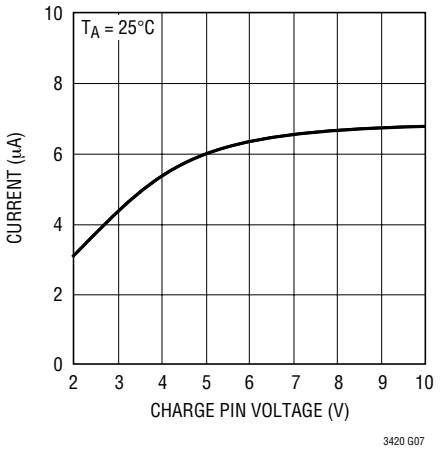
Output Voltage in Refresh Mode, LT3420-1



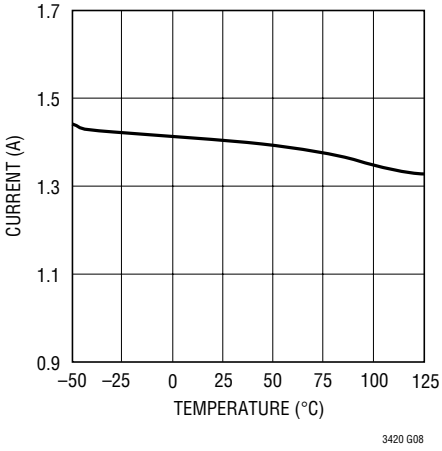
Charge Time, LT3420-1



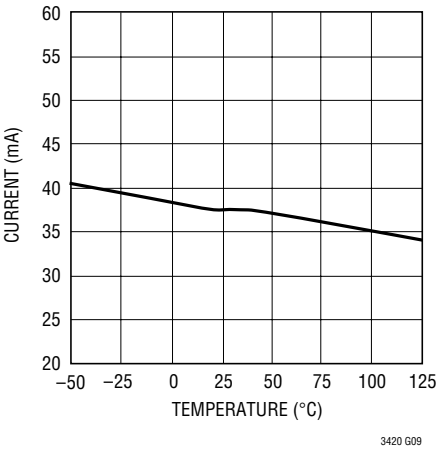
Charge Pin Input Current



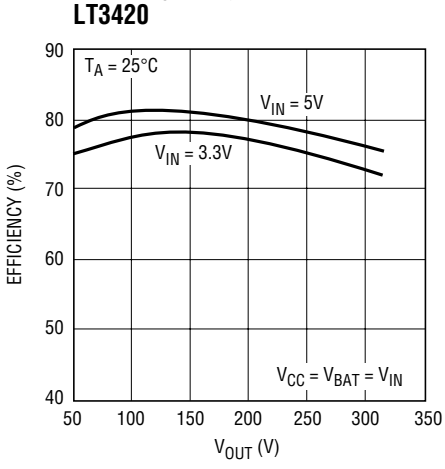
Primary Current Limit, LT3420



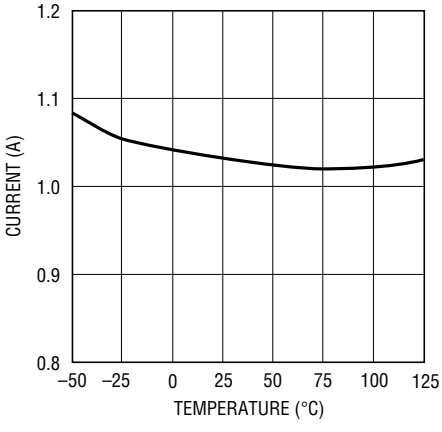
Secondary Current Limit, LT3420



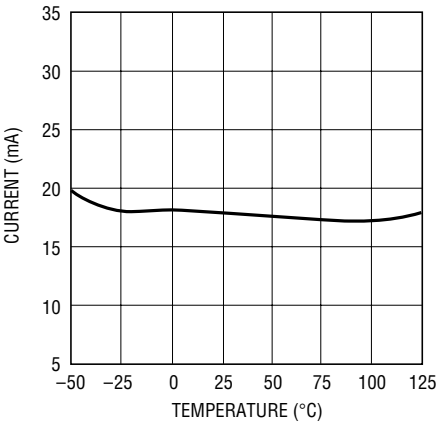
Efficiency of Figure 1 Circuit, LT3420



Primary Current Limit, LT3420-1



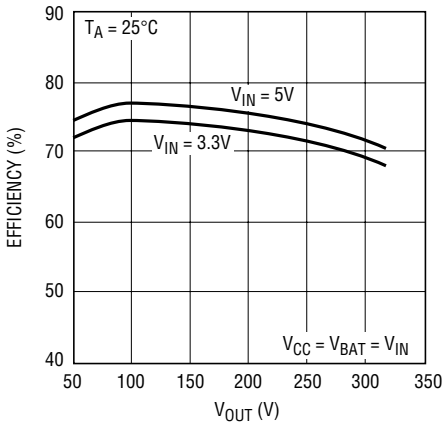
Secondary Current Limit, LT3420-1



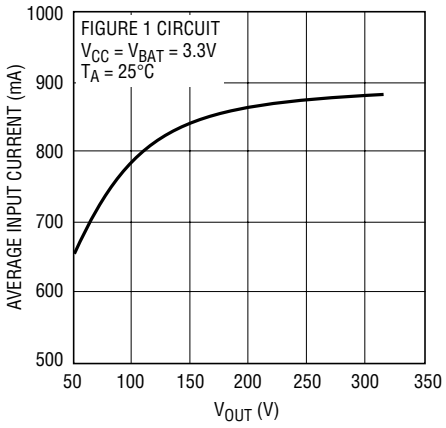
TYPICAL PERFORMANCE CHARACTERISTICS

Graphs apply to both the LT3420 and LT3420-1 unless otherwise noted.

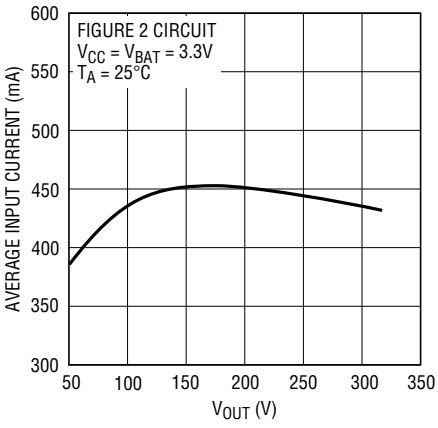
Efficiency for Figure 2 Circuit, LT3420-1



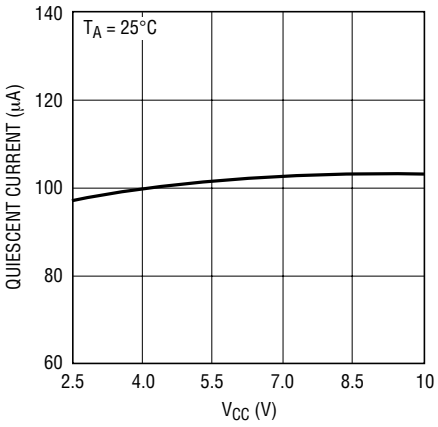
Input Current, LT3420



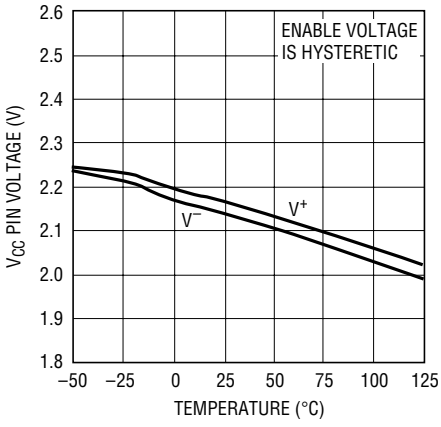
Input Current, LT3420-1



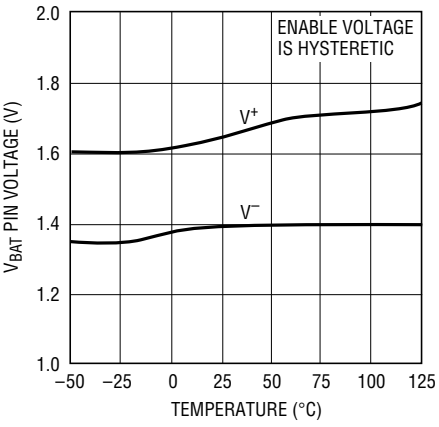
Quiescent Current in Refresh Mode



V_{CC} Minimum Operating Voltage



V_{BAT} Minimum Operating Voltage



PIN FUNCTIONS

R_{REF} (Pin 1): Reference Resistor Pin. Place a resistor (R2) from the R_{REF} pin to GND. 2k is recommended.

V_{BAT} (Pin 2): Battery Voltage Input. This pin should be connected to the power supply or battery, which supplies power to transformer T1. Must be locally bypassed.

R_{FB} (Pin 3): Feedback Resistor Pin. Place a resistor (R1) from the SW pin to the R_{FB} pin. Set R1 according to the following formula:

$$R1 = \frac{R2}{N^2}\left[(1.4 \bullet R_{SEC}) + N(V_{OUT} + 2V_D)\right] \text{ (LT3420)}$$

$$R1 = \frac{R2}{N^2}\left[(R_{SEC}) + N(V_{OUT} + 2V_D)\right] \text{ (LT3420-1)}$$

V_{OUT} : Desired Output Voltage

N: Transformer Turns Ratio

R_{SEC}: Transformer Secondary Resistance

V_D: Diode Forward Voltage Drop

R2: Resistor from the R_{REF} Pin to GND. 2k is a Typical Choice

V_{CC} (Pin 4): Input Supply Pin. Must be locally bypassed with a 4.7µF or larger ceramic capacitor.

GND (Pin 5): Ground. Tie directly to local ground plane.

SW (Pin 6): Switch Pin. This is the collector of the internal NPN power switch. Minimize the metal trace area connected to this pin to minimize EMI.

SEC (Pin 7): Transformer Secondary Pin. Tie one end of the transformer secondary to this pin. Take care to use the correct phasing of the transformer (Refer to Figures 1 and 2).

DONE (Pin 8): Done Output Pin. Open collector NPN output. DONE is pulled low whenever the chip is delivering power to the output and goes high when power delivery stops.

CHARGE (Pin 9): Charge Pin. Drive CHARGE high (1.5V or more) to commence charging of the output capacitor. Drive to 0.2V or less to put the part in shutdown mode.

C_T (Pin 10): Refresh Timer Capacitor Pin. Place a capacitor from the C_T pin to GND to set the refresh timer sample rate according to the following formula:

$C_T = 2.5 \bullet 10^{-6} \bullet t_{REFRESH}$

$t_{REFRESH}$: Desired Refresh Period in Seconds.

EXPOSED PAD (Pin 11) (DD Package only): GND. Must be soldered to local ground plane on PCB.

BLOCK DIAGRAMS

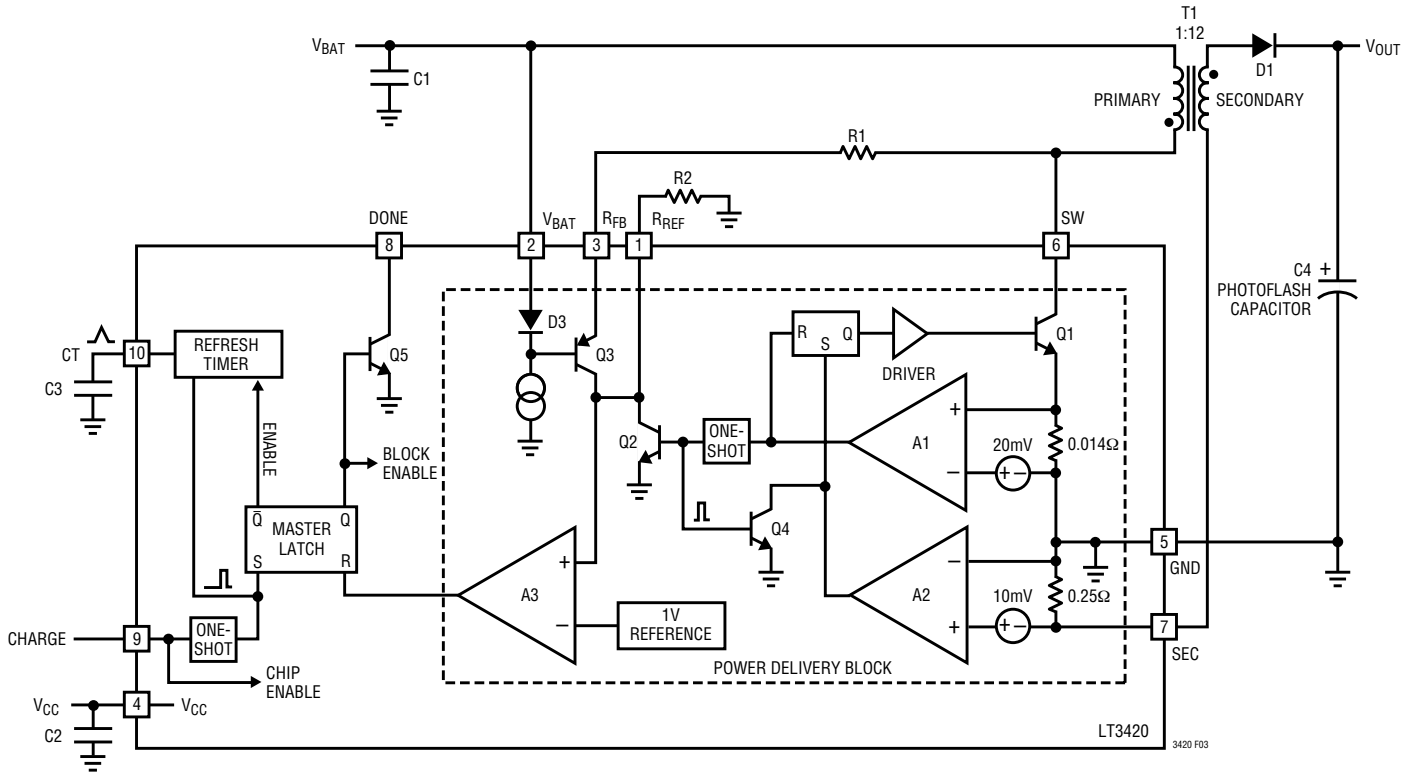


Figure 3. Block Diagram, LT3420

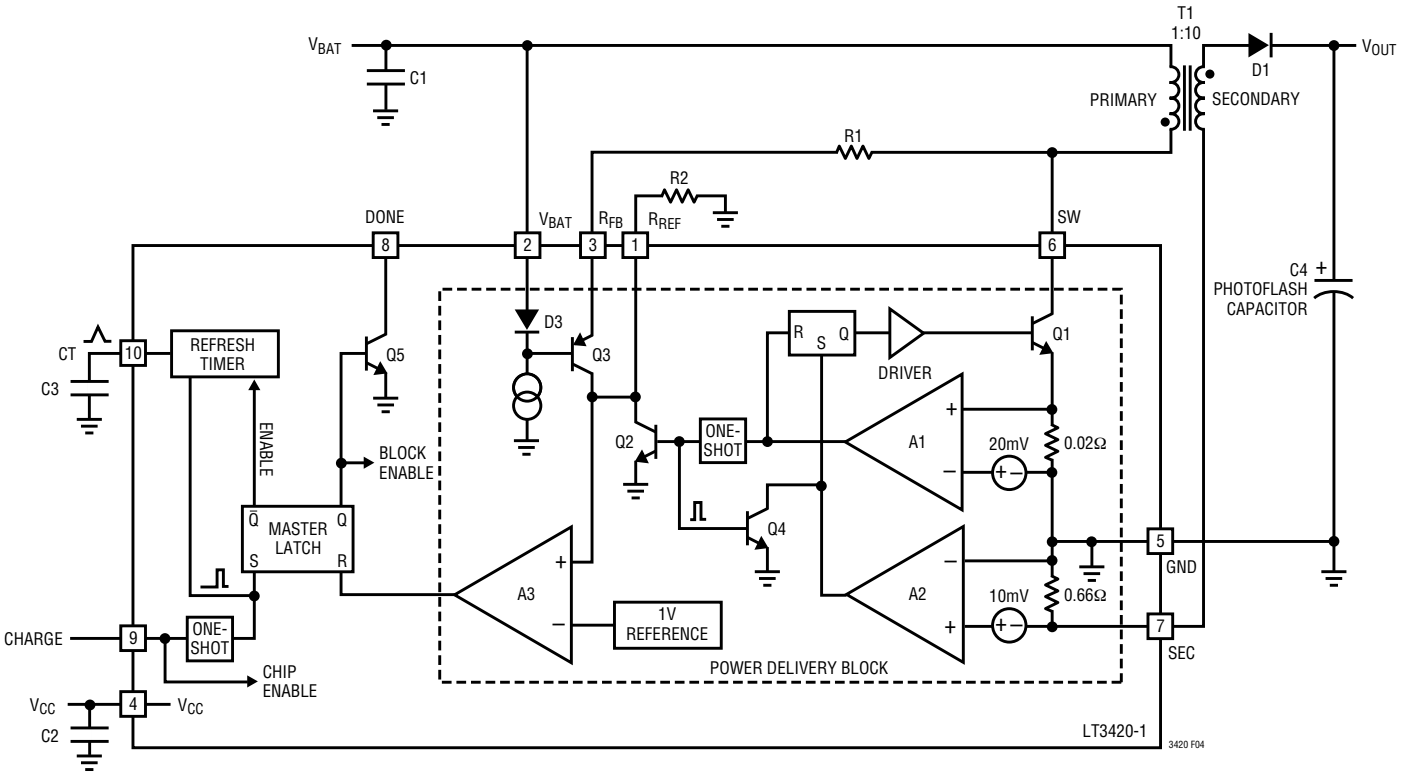


Figure 4. Block Diagram, LT3420-1

OPERATION

Overview

The following text focuses on the operation of the LT3420. The operation of the LT3420-1 is nearly identical with the differences discussed at the end of this section.

The LT3420 uses an adaptive on-time/off-time control scheme to provide excellent efficiency and precise control of switching currents. Please refer to Figure 3 for the following overview of the part's operation. At any given instant, the master latch determines which mode the LT3420 is in: "charging" or "refresh". In charging mode, the circuitry enclosed by the smaller dashed box is enabled, providing power to charge photoflash capacitor C1. The output voltage is monitored via the flyback pulse on the primary of the transformer. When the target output voltage is reached, the charging mode is terminated and the part enters the refresh mode. In refresh mode, the power delivery block is disabled, reducing quiescent current, while the refresh timer is enabled. The refresh timer simply generates a user programmable delay, after which the part reenters the charging mode. Once in the charging mode, the LT3420 will again provide power to the output until the target voltage is reached. Figure 5 is an oscillograph photo showing both the initial charging of the photoflash capacitor and the subsequent refresh action. The upper waveform is the output voltage. The middle waveform is the voltage on the C_T pin. The lower waveform shows the input current. The mode of the part is indicated below the photo.

The user can defeat the refresh timer and force the part into charging mode by toggling the CHARGE pin (high→low→high). The low to high transition on the CHARGE pin fires a one-shot that sets the master latch, putting the part in charging mode. Bringing CHARGE low puts the part in shutdown. The refresh timer can be programmed to wait indefinitely by simply grounding the C_T pin. In this configuration, the LT3420 will only reenter the charging mode by toggling the CHARGE pin.

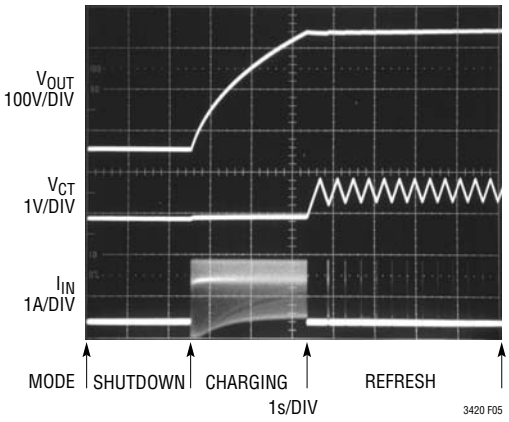


Figure 5. Demonstrating 3 Operating Modes of LT3420: Shutdown, Charging and Refresh of Photoflash Capacitor

Power Delivery Block

The power delivery block consists of all circuitry enclosed by the smaller dashed box in Figure 3. This circuit block contains all elements needed for charging and output voltage detection. To better understand the circuit operation, follow the subsequent description of one cycle of operation and refer to Figure 6. Assume that initially there is no current in the primary or secondary of the transformer, so the output of comparator A1 is low, while that of A2 is high (note the small offset voltages at the inputs of A1 and A2). The SR latch is thus set and the power NPN switch, Q1, is turned on. Current increases linearly in the primary of the transformer at a rate determined by the V_{BAT} voltage and the primary inductance of the transformer. As the current builds up, the voltage across the 14mΩ resistor increases. When this voltage exceeds the 20mV offset voltage of A1, the output of A1 goes high, resetting the SR latch and turning off Q1. The current needed to reset the latch is approximately 1.4A (~20mV/14mΩ).

When Q1 turns off, the secondary side current quickly jumps from zero current to the primary side current divided by N (the turns ratio of transformer T1). In this example, the peak secondary current is 116mA (1.4A/12). Diode D1 now conducts, providing power to the output. Since a positive voltage exists across the secondary winding of the transformer, the secondary current decreases linearly at a rate determined by the secondary inductance and the output voltage (neglecting the diode voltage drop). When the secondary side current drops below 40mA (10mV/0.25Ω), the output of A2 goes high, setting the SR latch and turning on Q1. The initial primary current is simply the minimum secondary current times N, in this case 0.48A (40mA • 12) . Q1 will now remain on until the primary current again reaches 1.4A. This cycle of operation repeats itself, automatically adjusting the On and Off times

OPERATION

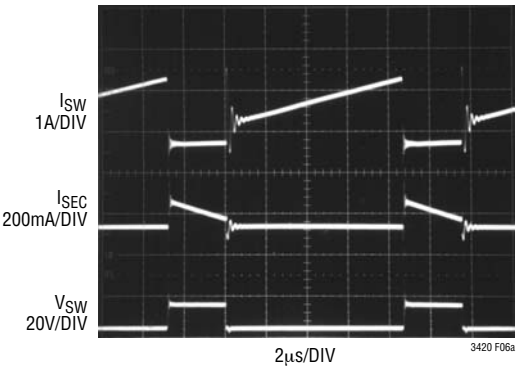


Figure 6a. Switching Waveforms with V_{OUT} = 100V, V_{CC} = V_{BAT} = 3.3V

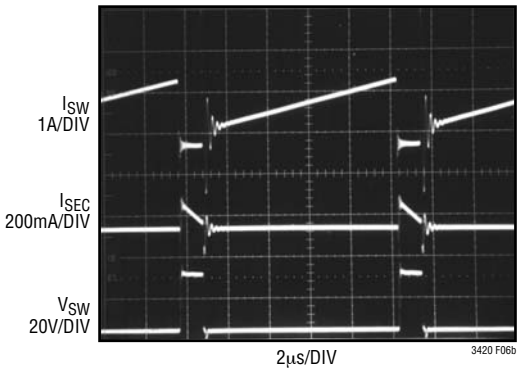


Figure 6b. Switching Waveforms with V_{OUT} = 300V, V_{CC} = V_{BAT} = 3.3V

of Q1 so that the peak current of Q1 is 1.4A and the minimum secondary current is 40mA (typical values).

The previously described charging cycle must be halted when the output voltage reaches the desired value. The LT3420 monitors the output voltage via the flyback pulse on the SW pin. When Q1 turns off, the secondary side conducts current turning on diode D1. Since the diode is conducting and the SEC pin is at nearly ground, the voltage across the secondary is nearly equal to V_{OUT}. The voltage across the primary is therefore close to V_{OUT}/N. A current proportional to V_{OUT}/N flows through R1 and into the R_{FB} pin. The current flows out of the R_{REF} pin through a resistor creating a ground referred voltage. When this voltage exceeds an internal 1V reference voltage, the output of comparator A3 goes high which resets the master latch. The Q output of the master latch goes low, disabling the entire power delivery block and enabling the refresh timer.

Leakage Spike Blanking

Another function of the LT3420 is leakage spike blanking when the power switch, Q1, turns off. Right after Q1 turns off, a one-shot turns on Q2 for 200ns (typ). With Q2 on, comparator A3 is disabled. This function may prevent A3 from false tripping on the leakage inductance spike on the SW pin. In practice, the PNP transistor Q3 filters out the leakage spike.

Refresh Timer

When the refresh timer is enabled, a 2.5µA current source is switched on, charging up the external timing capacitor, C3, from its initial voltage towards 1V. When the voltage on C3 reaches 1V, the polarity of the current source changes and 2.5µA discharges C3. When the voltage on C3 reaches 0.5V, the refresh timer sends a set pulse to the master latch, which puts the LT3420 into the charging mode.

Interface/Control

The CHARGE pin serves two functions. The first is to enable or shutdown the part depending on the level of the pin (high = enable, low = shutdown). The second is to force the part into the charging mode (low→high transition). The LT3420 also has a DONE pin, which signals whether or not the part is done charging the photoflash capacitor. The DONE pin is an open collector NPN switch (Q5) so an external pull-up resistor is needed. Whenever the part is in charging mode, DONE will be low. DONE will go high when the charging mode is complete. Both the CHARGE and DONE pins can be easily interfaced to a microprocessor in a digital or film camera.

LT3420-1 Differences

The LT3420-1 has different primary and secondary current limit levels. The primary current limit level of the LT3420-1 is 1A (typ) and the secondary current limit is 15mA (typ). The LT3420-1 has no leakage spike blanking which causes no problems since the PNP transistor, Q3, provides adequate filtering. Finally, the breakdown voltage of the SW pin of the LT3420-1 is higher at 50V.

APPLICATIONS INFORMATION

COMPONENT SELECTION

Choosing the Right Transformer

The flyback transformer plays a key role in any LT3420/LT3420-1 application. A poorly designed transformer can result in inefficient operation. Linear Technology Corporation has worked with a number of transformer manufacturers to develop specific transformers for use with the LT3420/LT3420-1. These predesigned transformers are sufficient for a large majority of the applications that may be encountered. In some cases, the reader may choose to design his own transformer or may simply be curious about the issues involved in designing the transformer. The following is a brief discussion of the issues relating to transformer design.

Transformer Turns Ratio

The turns ratio for the transformer, N, should be high enough so that the absolute maximum voltage rating for the NPN power switch is not exceeded. When the power switch turns off, the voltage on the collector of the switch (SW Pin) will "fly" up to the output voltage divided by N plus the battery voltage (neglecting the voltage drop across the rectifying diodes). **This voltage should not exceed the 38V (LT3420) or 50V (LT3420-1) breakdown rating of the power switch.**

Choose the minimum N by the following formula.

$$N_{MIN} \geq \frac{V_{OUT}}{38 - V_{BAT}} \quad (LT3420)$$

$$N_{MIN} \geq \frac{V_{OUT}}{50 - V_{BAT}} \quad (LT3420 - 1)$$

For an LT3420 design, a 5V battery voltage and a 330V output results in a N_{MIN} of 10 so a turns ratio of 10 or greater should be used.

Transformer Primary Inductance

A flyback transformer needs to store substantial amounts of energy in the core during each switching cycle. The transformer, therefore, will generally require an air gap. The use of an air gap in the core makes the energy storage ability, or inductance, much more stable with temperature and variations in the core material. Most core manufacturers will supply standard sizes of air gaps with a given type of core, resulting in different A_L values. A_L is the inductance of a particular core per square turns of winding. To get a certain inductance, simply divide the desired inductance by the A_L value and take the square root of the result to find the number of turns needed on the primary of the transformer.

The LT3420/LT3420-1 detect the output voltage via the flyback pulse on the SW pin. Since this can only occur while the power switch is off, an important criteria is that the value of the primary inductance of the transformer be larger than a certain minimum value. **The switch off time should be 500ns or larger for the LT3420 and 350ns or larger for the LT3420-1.** The minimum inductance can be calculated with the following formula:

$$L_{PRI} \geq \frac{500 \bullet 10^{-9} \bullet V_{OUT}}{N \bullet (1.4 - 0.04N)} \quad (LT3420)$$

$$L_{PRI} \geq \frac{350 \bullet 10^{-9} \bullet V_{OUT}}{N \bullet (1.0 - 0.015N)} \quad (LT3420 - 1)$$

V_{OUT}: Target Output Voltage

N: Transformer Turns Ratio

Transformer Leakage Inductance

The leakage inductance of the transformer must be carefully minimized for both proper and efficient operation of the part. The DC voltage rating of the SW pin on the LT3420 is 38V while on the LT3420-1 it is 50V. These ratings are for DC blocking voltages only and additional precautions

APPLICATIONS INFORMATION

must be taken into account for the dynamic blocking voltage capabilities of the LT3420/LT3420-1. The dynamic blocking voltage capability of both parts is 38V.

Table 1 summarizes the various breakdown voltages of the SW pin for both parts.

Table 1. SW Pin Voltage Ratings

PART	SW PIN DC RATING	SW PIN DYNAMIC RATING
LT3420	38V	38V
LT3420-1	50V	38V

Figure 7 shows what to examine in a new transformer design to determine if the specifications for the SW pin are met.

The first leakage inductance spike labeled "A" must not exceed the dynamic rating of the SW pin. If it does exceed the rating, then the transformer leakage inductance must be lowered. The flyback waveform after the initial spike labeled "B" must not exceed the DC rating of the SW pin. If it does exceed the rating, then the turns ratio of the transformer must be lowered. In measuring the voltage on the SW pin, care must be taken in minimizing the ground loop of the voltage probe. Careless probing will result in inaccurate readings.

Note also the magnitude of the initial current spike in the primary of the transformer labeled "C" when the power switch turns on. If the leakage inductance is lowered to a very low level, the internal capacitances of the transformer will be high. This will result in the initial spike of current in the primary becoming excessively high. The level of "C" should be kept to 4A or less in a typical design for both the LT3420 and LT3420-1. Please note that by inserting a loop of wire in the primary to measure the primary current, the leakage inductance of the primary will be made artificially high. This may result in erroneous voltage measurements on the SW pin.

The measurements shown in Figure 7 should be made with both V_{OUT} and V_{BAT} at the maximum levels for the given application. This results in the highest voltage and current stress on the SW pin.

Transformer Secondary Capacitance

The total capacitance of the secondary should be minimized for both efficient and proper operation of the LT3420/LT3420-1. Since the secondary of the transformer undergoes large voltage swings (approaching $600V_{P-P}$), any capacitance on the secondary can severely affect the

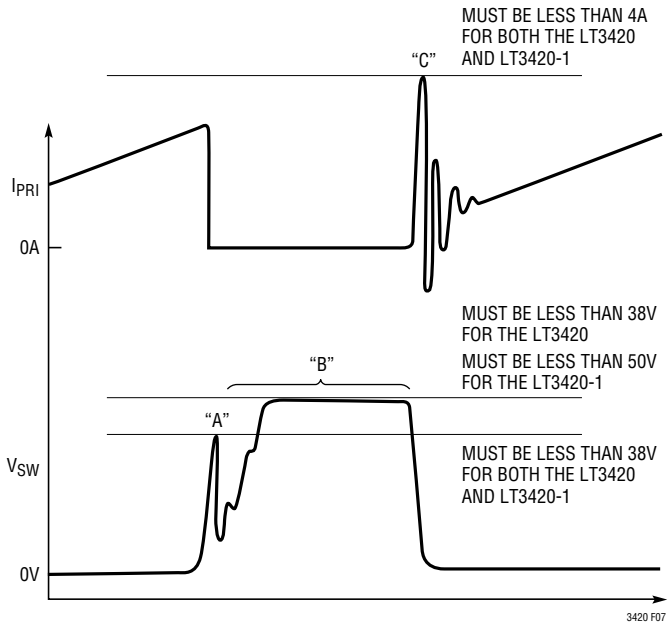


Figure 7. New Transformer Design Check (Not to Scale)

APPLICATIONS INFORMATION

efficiency of the circuit. In addition, the effective capacitance on the primary is largely dominated by the actual secondary capacitance. This is simply a result of any secondary capacitance being multiplied by N^2 when reflected to the primary. Since N is generally 10 or higher, a small capacitance of 10pF on the secondary is 100 times larger, or 1.0nF, on the primary. This capacitance forms a resonant circuit with the primary leakage inductance of the transformer. As such, both the primary leakage inductance and secondary side capacitance should be minimized.

Table 2 shows various predesigned transformers along with relevant parameters. Contact the individual transformer manufacturer for additional information or customization.

Table 2a. Predesigned Transformers, LT3420

PART	TURNS RATIO	L (µH)	SIZE LxWxH (mm)	VENDOR
SRW10EPC -U01H003	1:12	24	10.9x10.8x5.2	TDK (847) 803-6100 www.components.tdk.com
6375-T108	1:12	15	10.8x9.5x3.6	Sumida (847) 956-0666 www.sumida.com
SBL-6.4	1:12	17.5	10.3x6.4x5.2	Kijima Musen 852-2489-8266 kijimahk@netvigator.com

Table 2b. Predesigned Transformers, LT3420-1

PART	TURNS RATIO	L (µH)	SIZE LxWxH (mm)	VENDOR
SBL-5.6S-2	1:10	15	5.6x8.5x3.0	Kijima Musen 852-2489-8266 kijimahk@netvigator.com
LDT565630T -002	1:10.2	14.5	5.8x5.8x3.0	TDK (847) 803-6100 www.components.tdk.com

DIODE SELECTION

The rectifying diode(s) should be low capacitance type with sufficient reverse voltage and forward current ratings. The peak reverse voltage that the diode(s) will see is approximately:

$$V_{PK-R} \approx \left(V_{OUT} + (N \bullet V_{BAT})\right) \bullet 1.65$$

The peak current of the diode is simply:

$$I_{PK-SEC} = \frac{1.4A}{N} \quad (LT3420)$$

$$I_{PK-SEC} = \frac{1.0A}{N} \quad (LT3420-1)$$

For the circuit of Figure 1 with V_{BAT} of 3.3V, V_{PK-R} is 590V and I_{PK-SEC} is 116mA. Table 3 shows various diodes that can work with the LT3420/LT3420-1. These are chosen for low capacitance and high reverse blocking voltage. Use the appropriate number of diodes to achieve the necessary reverse breakdown voltage.

Table 3

PART	MAX REVERSE VOLTAGE (V)	CAPACITANCE (pF)	VENDOR
GSD2004S (Dual diode)	2x300	5	Vishay (402) 563-6866 www.vishay.com
BAS21 (Single diode)	250	1.5	Philips Semiconductor (800) 234-7381 www.philips.com
MMBD3004S	2x300	5	Diodes Inc. (805) 446-4800 www.diodes.com

APPLICATIONS INFORMATION

CAPACITOR SELECTION

The V_{BAT} and V_{CC} decoupling capacitors should be multilayer ceramic type with X5R or X7R dielectric. This insures adequate decoupling across wide ambient temperature ranges. A good quality ceramic capacitor is also recommended for the timing capacitor on the C_T pin. Avoid Y5V or Z5U dielectrics.

Selectively Disabling the LT3420/LT3420-1

The LT3420/LT3420-1 can be disabled at any time, even during the charge phase. This may be useful when a digital camera enters a sensitive data acquisition phase. Figure 8 illustrates this feature. Midway through the charge cycle, the CHARGE pin is brought low, which disables the part. After the sensitive data operation is complete, the CHARGE pin is brought high and the charging operation continues.

Measuring Efficiency

Measuring the efficiency of a circuit designed to charge large capacitive loads is a difficult issue, particularly with photoflash capacitors. The ideal way to measure the efficiency of a capacitor charging circuit would be to find the energy delivered to the output capacitor ($0.5 \bullet C \bullet V^2$) and divide it by the total input energy. This method does not work well here because photoflash capacitors are far from ideal. Among other things, they have relatively high leakage currents, large amounts of dielectric absorption, and significant voltage coefficients. A much more accurate, and easier, method is to measure the efficiency as a function of the output voltage. In place of the photoflash capacitor, use a smaller, high quality capacitor, reducing errors associated with the non-ideal photoflash capacitor. Using an adjustable load, the output voltage can be set anywhere between ground and the maximum output voltage. The efficiency is measured as the output power ($V_{OUT} \bullet I_{OUT}$) divided by the input power ($V_{IN} \bullet I_{IN}$). This method also provides a good means to compare various charging circuits since it removes the variability of the photoflash capacitor from the measurement. The total efficiency of the circuit, charging an ideal capacitor, would be the time average of the given efficiency curve, over time as V_{OUT} changes.

Adjustable Input Current

With many types of modern batteries, the maximum allowable current that can be drawn from the battery is limited. This is generally accomplished by active circuitry or a polyfuse. Different parts of a digital camera may require high currents during certain phases of operation and very little at other times. A photoflash charging circuit should be able to adapt to these varying currents by drawing more current when the rest of the camera is drawing less, and vice-versa. This helps to reduce the charge time of the photoflash capacitor, while avoiding the

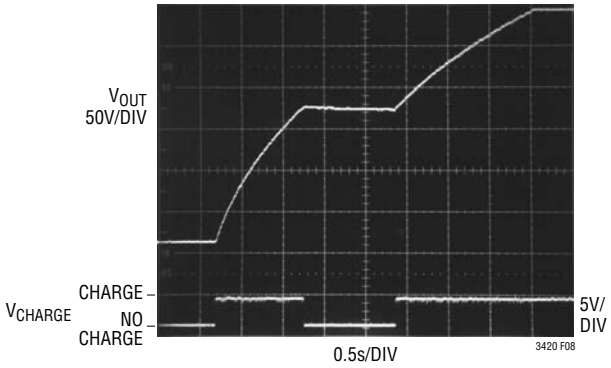


Figure 8. Halting the Charge Cycle at Any Time

APPLICATIONS INFORMATION

risk of drawing too much current from the battery. The input current to the LT3420/LT3420-1 circuit can be adjusted by driving the CHARGE pin with a PWM (pulse width modulation) signal. The microprocessor can adjust the duty cycle of the PWM signal to achieve the desired level of input current. Many schemes exist to achieve this function. Once the target output voltage is reached, the PWM signal should be halted to avoid overcharging the photoflash capacitor, since the signal at the CHARGE pin overrides the refresh timer.

A simple method to achieve adjustable input current is shown in Figure 9. The PWM signal has a frequency of 1kHz. When ON is logic high, the circuit is enabled and the CHARGE pin is driven by the PWM signal. When the target output voltage is reached, DONE goes high while CHARGE is also high. The output of A1 goes high, which forces CHARGE high regardless of the PWM signal. The part is now in the Refresh mode. Once the refresh period is over, the DONE pin goes low, allowing the PWM signal to drive the CHARGE pin once again. This function can be easily implemented in a microcontroller. Figure 10 shows the input current for the LT3420 and LT3420-1 as the duty cycle of the PWM signal is varied.

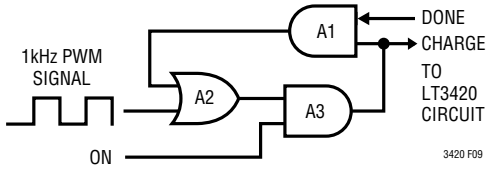


Figure 9. Simple Logic for Adjustable Input Current

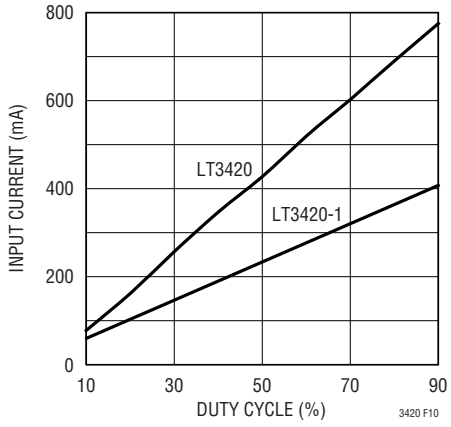


Figure 10. Input Current as Duty Cycle is Varied

APPLICATIONS INFORMATION

BOARD LAYOUT

The high voltage operation of the LT3420/LT3420-1 demands careful attention to board layout. You will not get advertised performance with careless layout. Figures 11 and 12 show the recommended component placement. Keep the area for the high voltage end of the secondary as small as possible. Note the larger than minimum spacing for all high voltage nodes. This is necessary to meet the breakdown specifications for the circuit board. If the Photoflash capacitor is placed far from the LT3420/LT3420-1 circuit, place a small (20nF-50nF) ceramic capacitor with sufficient voltage rating close to the part. This insures adequate bypassing. Remember that **LETHAL VOLTAGES ARE PRESENT** in this circuit. Use caution when working with the circuit.

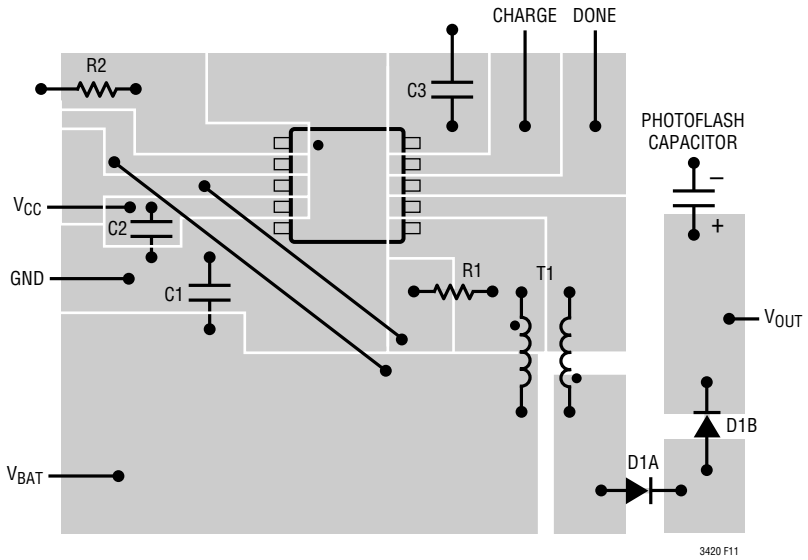


Figure 11. Suggested Layout (MS10 Package)

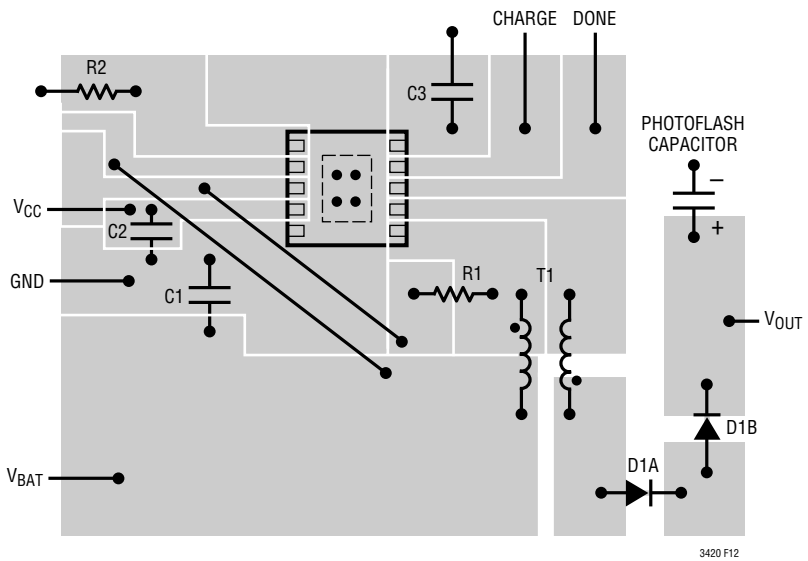
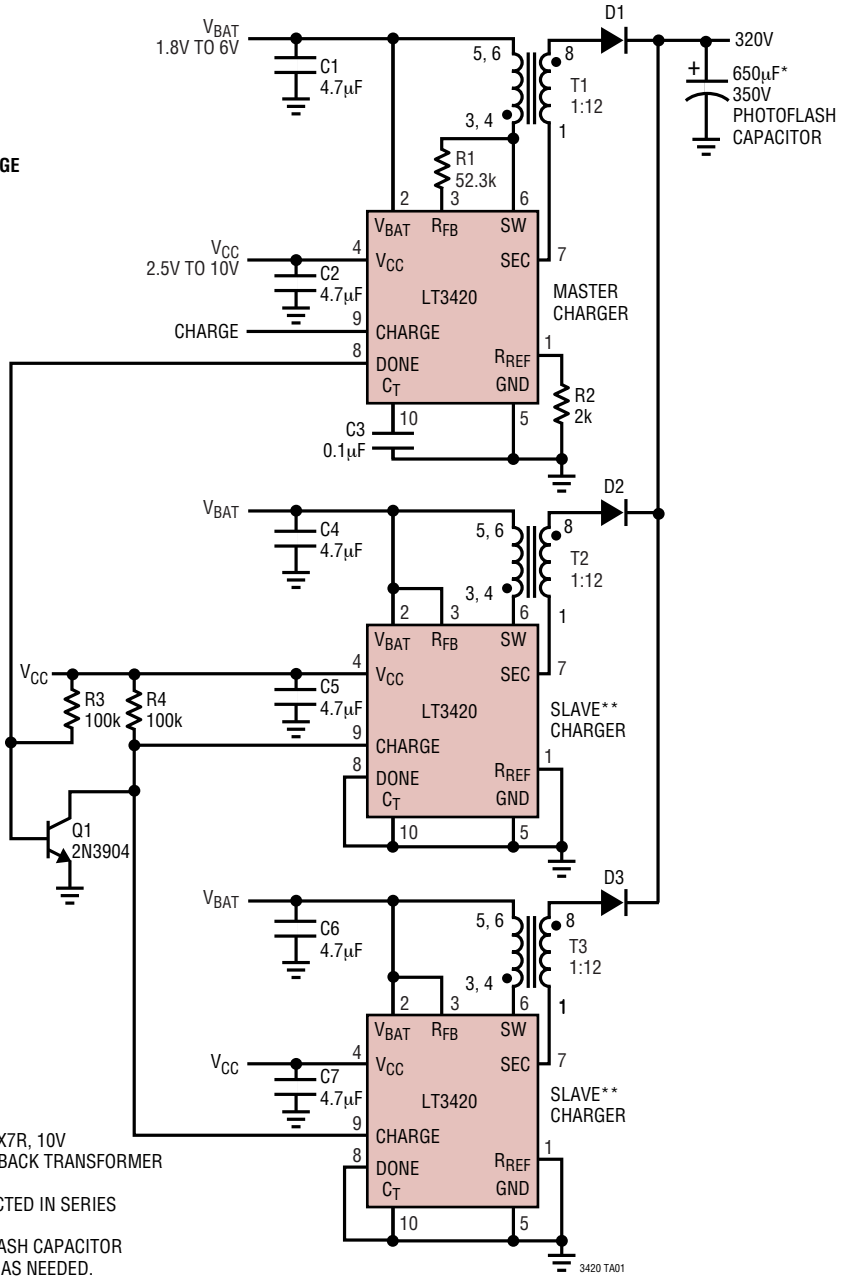


Figure 12. Suggested Layout (DD Package)

TYPICAL APPLICATIONS

Professional Charger uses Multiple LT3420 Circuits in Parallel to Charge Large Photoflash Capacitors Quickly

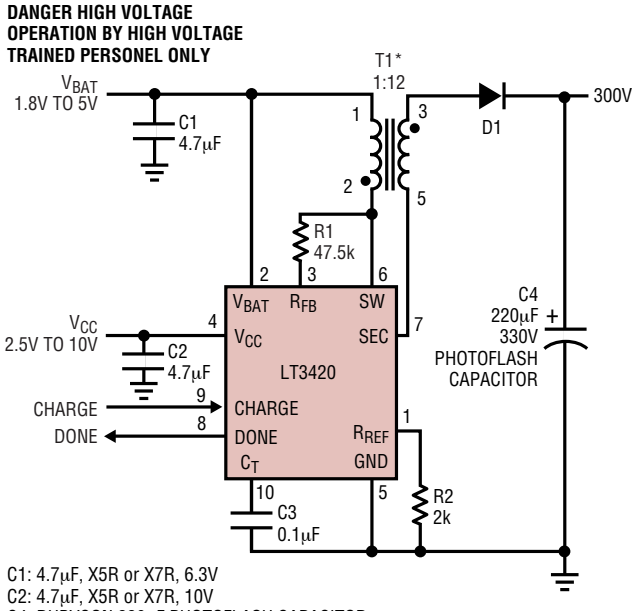
DANGER HIGH VOLTAGE
OPERATION BY HIGH VOLTAGE
TRAINED PERSONEL ONLY



C1, C2, C4, C5, C6, C7: 4.7µF, X5R or X7R, 10V
T1-T3: TDK SRW10EPC-U01H003 FLYBACK TRANSFORMER
D1-D3: VISHAY GSD2004S SOT-23
DUAL DIODE. DIODES CONNECTED IN SERIES
Q1: 2N3904 OR EQUIVALENT
* CAN CHARGE ANY SIZE PHOTOFLASH CAPACITOR
** USE AS MANY SLAVE CHARGERS AS NEEDED.

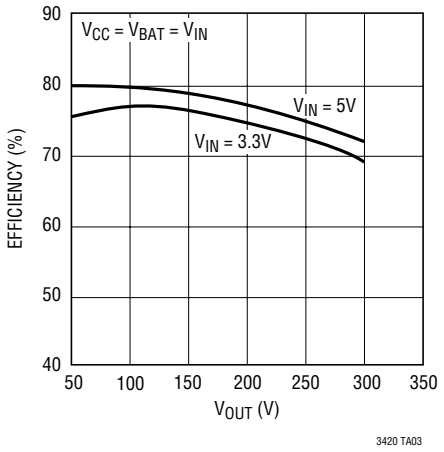
TYPICAL APPLICATIONS

LT3420 Photoflash Charging Circuit Uses Small Transformer



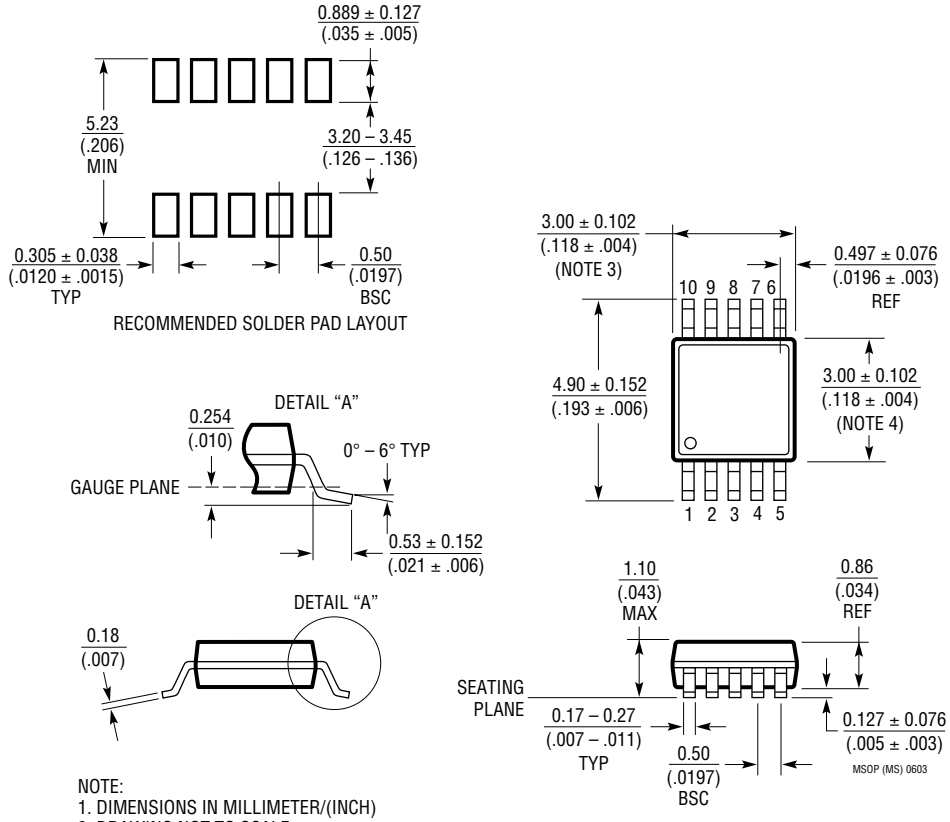
C1: 4.7µF, X5R or X7R, 6.3V
C2: 4.7µF, X5R or X7R, 10V
C4: RUBYCON 220µF PHOTOFLASH CAPACITOR
D1: VISHAY GSD2004S SOT-23
DUAL DIODE. DIODES CONNECTED IN SERIES
T1: KIJIMA MUSEN SBL-6.4
* MAXIMUM AMBIENT TEMPERATURE OF 60°C DICTATED BY TRANSFORMER

Efficiency



PACKAGE DESCRIPTION

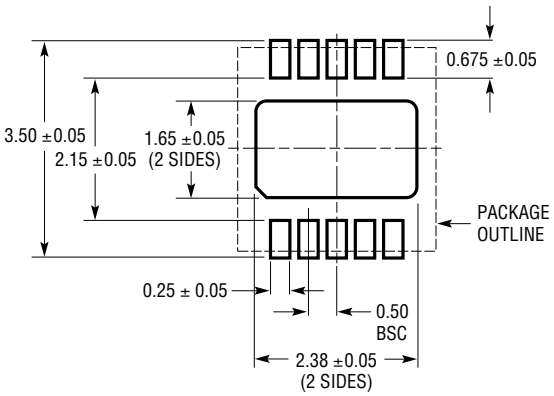
MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



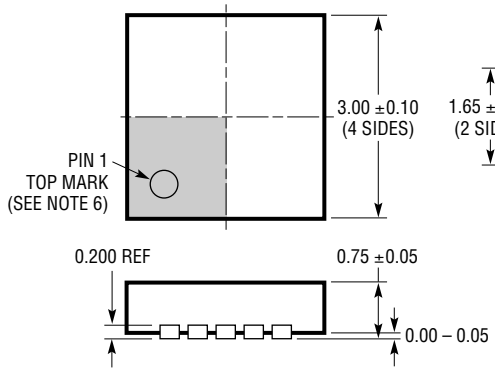
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

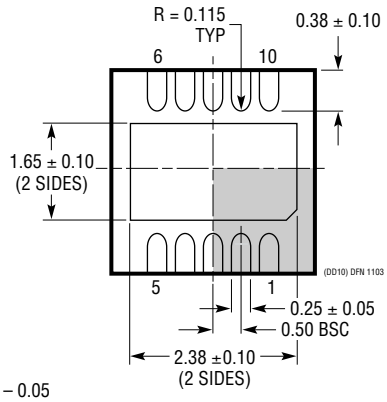
PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.