Constant Frequency Step-Down DC/DC Controller with LDO Regulator

FEATURES

- **Dual Output Regulator in Tiny 10-Pin MSOP**
- **High Efficiency: Up to 94%**
- **Wide V_{IN} Range: 2.65V to 9.8V**
- **Constant Frequency 550kHz Operation**
- **150mA LDO Regulator with Current Limit and Thermal Shutdown Protection**
- High Output Currents Easily Achieved
- Burst Mode® Operation at Light Load
- Low Dropout: 100% Duty Cycle
- Current Mode Operation for Excellent Line and Load Transient Response
- 0.8V Reference Allows Low Output Voltages
- Low Quiescent Current: 260µA Total
- Shutdown Mode Draws Only 10µA Supply Current
- Common Power Good Output for Both Supplies

APPLICATIONS

- Notebook Computers
- Portable Instruments
- One or Two Li-Ion Battery-Powered Applications

DESCRIPTION

The LTC®3700 is a constant frequency current mode step-down (buck) DC/DC controller with excellent AC and DC load and line regulation. The on-chip 150mA low dropout (LDO) linear regulator can be powered from the buck controller's input supply, its own independent input supply or the buck regulator's output. The buck controller incorporates an undervoltage lockout feature that shuts down the controller when the input voltage falls below 2.1V.

The buck regulator provides a ±2.5% output voltage accuracy. It consumes only 210µA of quiescent current in normal operation with the LDO consuming an additional 50µA. In shutdown, a mere 10µA (combined) is consumed.

For applications where efficiency is a prime consideration, the buck controller is configured for Burst Mode operation which enhances efficiency at low output current. To further maximize the life of a battery source, the external P-channel MOSFET is turned on continuously in dropout (100% duty cycle). High constant operating frequency of 550kHz allows the use of a small external inductor.

The LDO is protected by both current limit and thermal shutdown circuits.

The LTC3700 is available in a tiny 10-pin MSOP.

TYPICAL APPLICATION

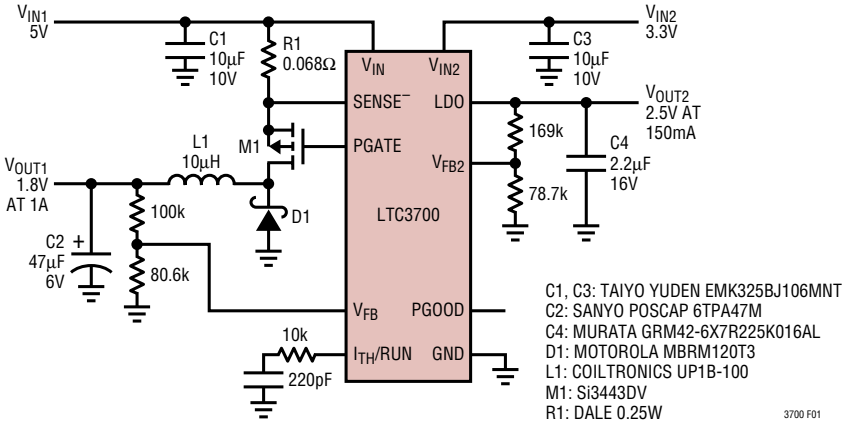
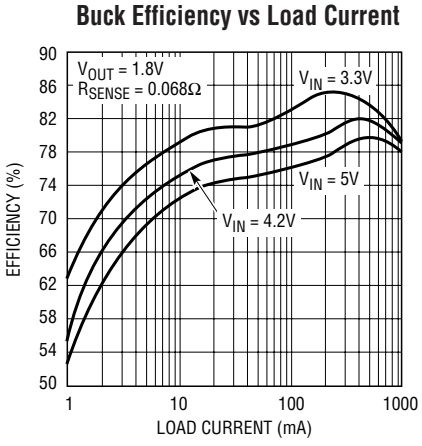


Figure 1. High Efficiency 5V to 1.8V/1A Buck with 3.3V to 2.5V/150mA LDO

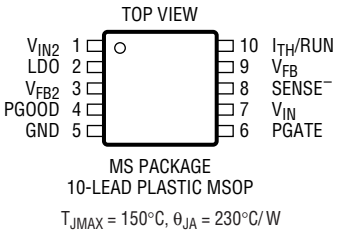


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Buck Input Supply Voltage (V_{IN}) .....–0.3V to 10V
SENSE$^-$, PGATE Voltages .....–0.3V to (V_{IN} + 0.3V)
V_{FB}, I_{TH}/RUN Voltages .....–0.3V to 2.4V
PGATE Peak Output Current (<10µs) 1A
LDO Input Supply Voltage (V_{IN2}) .....–0.3V to 6V
LDO, V_{FB2} Voltages ..... –0.3V to (V_{IN2} + 0.3V)
PGOOD Voltage .....–0.3V to 10V
LDO Peak Output Current (< 10µs) 500mA
Storage Ambient Temperature Range ... –65°C to 150°C
Operating Temperature Range (Note 2) ... –40°C to 85°C
Junction Temperature (Note 3) ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 230°C/ W

ORDER PART NUMBER
LTC3700EMS
MS PART MARKING
LTXN

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{IN2} = 4.2V unless otherwise specified. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Buck DC/DC Controller						
Input DC Supply Current	Typicals at V_{IN} = 4.2V (Note 4)					
Normal Operation	2.65V ≤ V_{IN} ≤ 9.8V			210	340	µA
Sleep Mode	2.65V ≤ V_{IN} ≤ 9.8V			200	330	µA
Shutdown	2.65V ≤ V_{IN} ≤ 9.8V, V_{ITH} /RUN = 0V			10	30	µA
UVLO	V_{IN} < UVLO Threshold			10	30	µA
Undervoltage Lockout Threshold	V_{IN} Falling	●	1.90	2.10	2.60	V
	V_{IN} Rising	●	2.00	2.20	2.65	V
Shutdown Threshold (at I_{TH} /RUN)		●	0.15	0.30	0.45	V
Start-Up Current Source	V_{ITH} /RUN = 0V		0.25	0.5	0.85	µA
Regulated Feedback Voltage	(Note 5), 0°C to 70°C	●	0.780	0.800	0.820	V
	(Note 5), –40°C to 85°C	●	0.770	0.800	0.830	V
Output Voltage Line Regulation	2.65V ≤ V_{IN} ≤ 9.8V (Note 5)			0.1		mV/V
Output Voltage Load Regulation	I_{TH} /RUN Sinking 5µA (Note 5)			4		mV/µA
	I_{TH} /RUN Sourcing 5µA (Note 5)			4		mV/µA
V_{FB} Input Current	(Note 5)			10	50	nA
Overvoltage Protect Threshold	Measured at V_{FB}		0.820	0.860	0.910	V
Overvoltage Protect Hysteresis				20		mV
Oscillator Frequency	V_{FB} = 0.8V		500	550	650	kHz
	V_{FB} = 0V			110		kHz
Gate Drive Rise Time	C_{LOAD} = 3000pF			40		ns
Gate Drive Fall Time	C_{LOAD} = 3000pF			40		ns
Peak Current Sense Voltage	(Note 6)			120		mV
Peak Current Sense Voltage in Burst Mode				30		mV

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{IN2} = 4.2V unless otherwise specified. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LDO Regulator						
V_{IN2} Input Voltage			2.4		6	V
Input DC Supply Current	Typicals at V_{IN2} = 4.2V					
Normal Operation with Buck Enabled	2.4V ≤ V_{IN2} ≤ 6V			50	100	µA
Normal Operation with Buck Undervoltage	2.4V ≤ V_{IN2} ≤ 6V			100	150	µA
Shutdown with Buck Enabled	2.4V ≤ V_{IN2} ≤ 6V, $V_{ITH/RUN}$ = 0V			0	1	µA
Shutdown with Buck Undervoltage	2.4V ≤ V_{IN2} ≤ 6V, $V_{ITH/RUN}$ = 0V			8	24	µA
Regulated Feedback Voltage	0°C ≤ T_A ≤ 70°C, I_{LDO} = 1mA	●	0.780	0.800	0.830	V
	–40°C ≤ T_A ≤ 85°C, I_{LDO} = 1mA	●	0.765	0.800	0.835	V
Output Voltage Line Regulation	(Unity-Gain Feedback)					
With Buck Enabled	2.65V ≤ V_{IN} ≤ 9.8V			0.05		mV/V
With Buck Enabled	2.4V ≤ V_{IN2} ≤ 6V, I_{LDO} = 1mA			4		mV/V
With Buck Undervoltage	2.4V ≤ V_{IN2} ≤ 6V, I_{LDO} = 1mA			4		mV/V
Output Voltage Load Regulation	1mA ≤ I_{LOAD} ≤ 150mA			0.06	0.12	mV/mA
V_{FB2} Input Current				0	10	nA
LDO Short-Circuit Current	V_{LDO} = 0V		150	200		mA
LDO Dropout	V_{IN2} = 3.3V, I_{LDO} = 150mA			270		mV
	V_{IN2} = 6V, I_{LDO} = 150mA			170		mV
Overtemperature Trip Point	(Note 7)			150		°C
Overtemperature Hysteresis	(Note 7)			5		°C
PGOOD						
Feedback Voltage PGOOD Threshold	(Note 8)					
PGOOD High-to-Low	V_{FB} or V_{FB2} Falling		–12	–7.5		%
	V_{FB} or V_{FB2} Rising			7.5	12	%
PGOOD Low-to-High	V_{FB} or V_{FB2} Rising		–10	–5.0		%
	V_{FB} or V_{FB2} Falling			5.0	10	%
PGOOD On-Resistance	$V_{ITH/RUN}$ = 0V, V_{IN} = V_{IN2} = 4.2V, V_{PGOOD} = 100mV			135	180	Ω

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC3700 is guaranteed to meet specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$T_J = T_A + (P_D \bullet \theta_{JA}°C/W)$

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 5: The LTC3700 is tested in a feedback loop that servos V_{FB} to the output of the error amplifier.

Note 6: Peak current sense voltage is reduced dependent on duty cycle to a percentage of value as given in Figure 2.

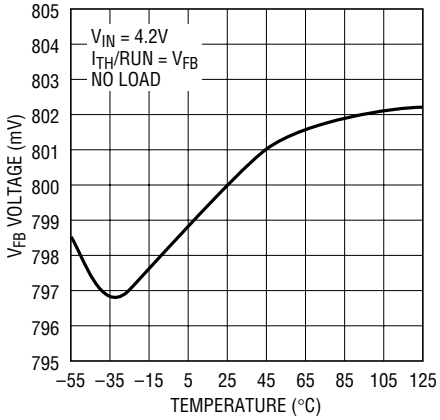
Note 7: Guaranteed by design; not tested in production.

Note 8: PGOOD values are expressed as a percentage difference from the respective "Regulated Feedback Voltage" as given in the table.

TYPICAL PERFORMANCE CHARACTERISTICS

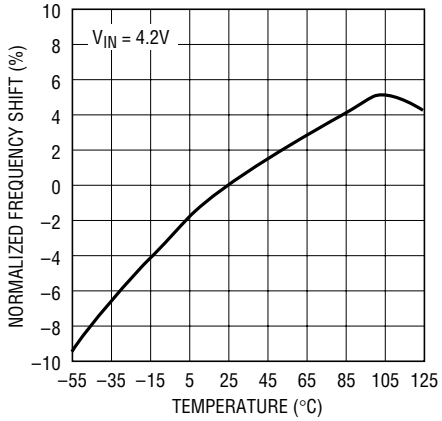
BUCK DC/DC CONTROLLER

V_{FB} Voltage vs Temperature



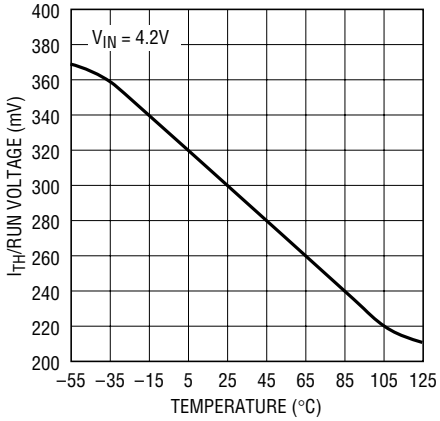
3700 G01

Normalized Oscillator Frequency vs Temperature



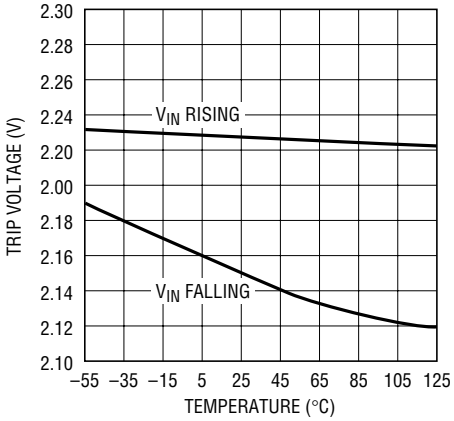
3700 G02

Shutdown Threshold vs Temperature



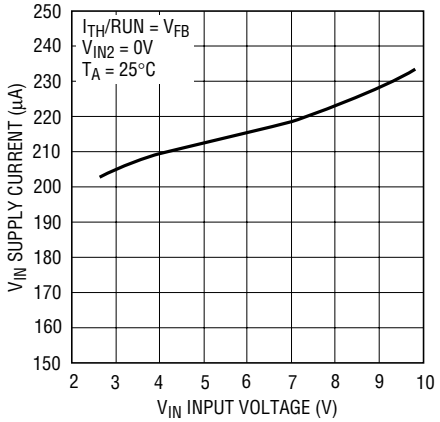
3700 G04

Undervoltage Lockout Trip Voltage vs Temperature



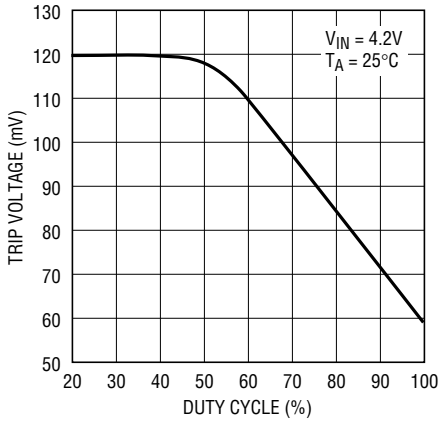
3700 G03

Buck Supply Current vs Input Voltage



3700 G10

Maximum (V_{IN} – SENSE$^-$) Voltage vs Duty Cycle

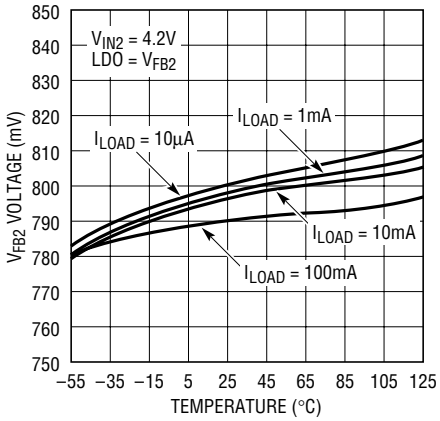


3700 G05

TYPICAL PERFORMANCE CHARACTERISTICS

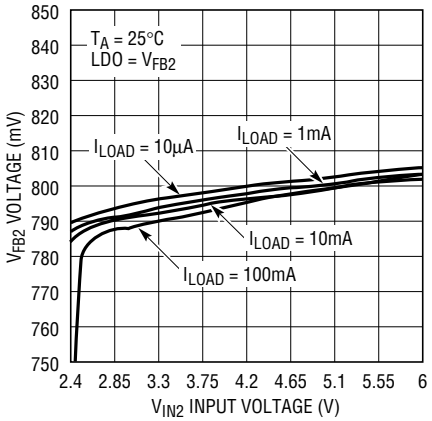
LDO REGULATOR

V_{FB2} Voltage vs Temperature



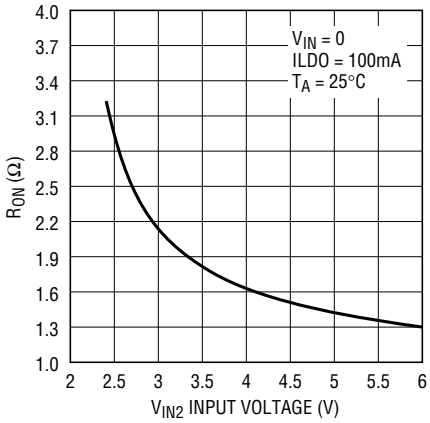
3700 G06

LDO Line Regulation (V_{FB2} Voltage vs Supply)



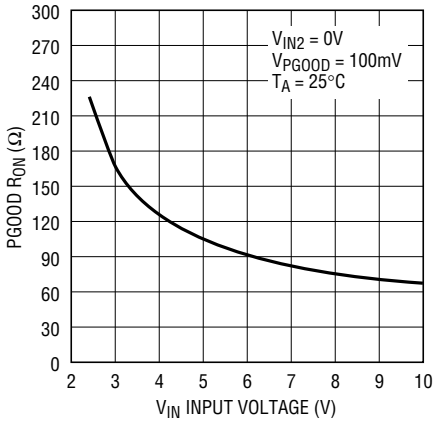
3700 G07

LDO Pass FET R_{ON} vs Input Voltage



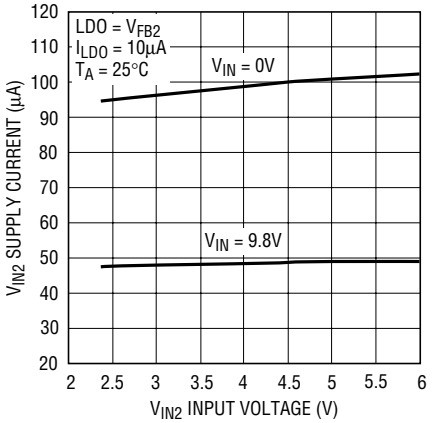
3700 G08

PGOOD R_{ON} vs Input Voltage



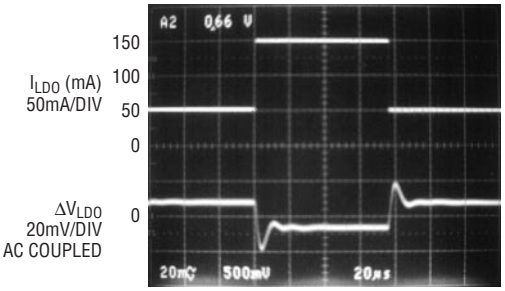
3700 G09

LDO Supply Current vs Input Voltage



3700 G11

Load Transient Response



TA = 25°C
VIN2 = 3.3V
VLDO = 2.5V
CLDO = 10µF

20µs/DIV

3700 G12

PIN FUNCTIONS

V_{IN2} (Pin 1): LDO Input Supply Pin. Must be closely decoupled to GND (Pin 5).

LDO (Pin 2): LDO Output Pin. Must be closely decoupled to GND (Pin 5) with a low ESR ceramic capacitor ≥2.2µF.

V_{FB2} (Pin 3): LDO Feedback Voltage. Receives the feedback voltage from an external resistor divider between LDO (Pin 2) and GND (Pin 5).

PGOOD (Pin 4): Open-Drain Power Good Output. This pin will pull to ground if either voltage output of the buck or the LDO [sensed at V_{FB} (Pin 9) and V_{FB2} (Pin 3), respectively] is out of range. When both voltage outputs are valid, this pin will go to a high impedance state.

GND (Pin 5): Common Ground Pin for Both Buck and LDO.

PGATE (Pin 6): Gate Drive for Buck's External P-Channel MOSFET. This pin swings from 0V to V_{IN}.

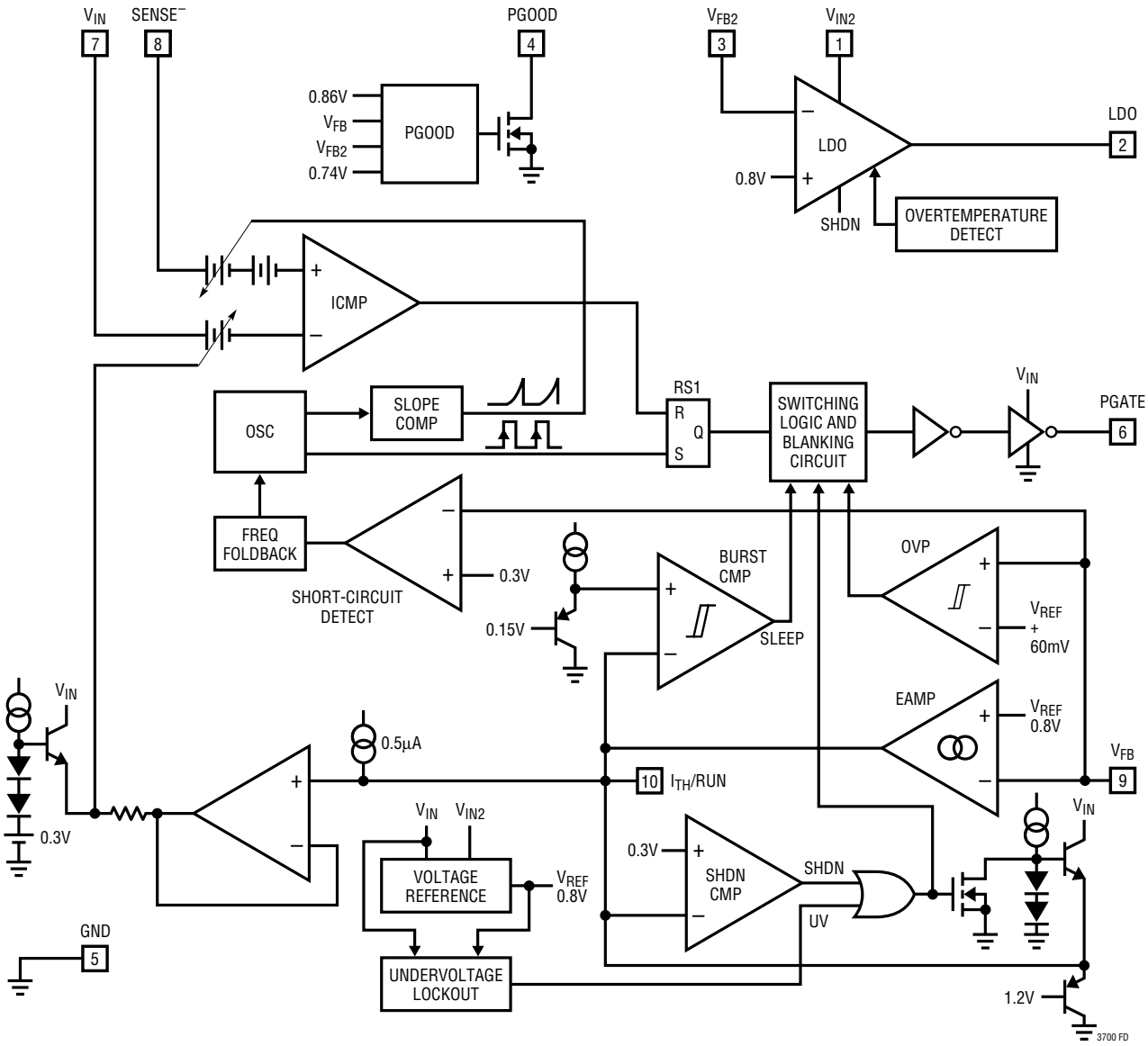
V_{IN} (Pin 7): Buck Input Supply Pin. Must be closely decoupled to GND (Pin 5).

$SENSE^-$ (Pin 8): The Negative Input to the Current Comparator of the Buck. Monitors switch current of external P-Channel MOSFET.

V_{FB} (Pin 9): Buck Feedback Voltage. Receives the feedback voltage from an external resistor divider between buck output and GND (Pin 5).

I_{TH}/RUN (Pin 10): This pin performs two functions. It serves as the error amplifier compensation point for the buck, as well as a common run control input for both the buck and the LDO. The current comparator threshold of the buck increases with this voltage. Nominal voltage range for this pin is 0.7V to 1.9V. Forcing this pin below 0.3V causes both the buck and the LDO to be shut down. In shutdown all functions are disabled, the PGATE pin is held high and the LDO output will go to a high impedance state.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop (Buck Controller)

The LTC3700 is a constant frequency current mode switching regulator. During normal operation, the external P-channel power MOSFET is turned on each cycle when the oscillator sets the RS latch (RS1) and turned off when the current comparator (ICMP) resets the latch. The peak inductor current at which ICMP resets the RS latch is controlled by the voltage on the I_{TH}/RUN pin, which is the output of the error amplifier EAMP. An external resistive divider connected between V_{OUT} and ground allows the EAMP to receive an output feedback voltage V_{FB}. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.8V reference, which in turn causes the I_{TH}/RUN voltage to increase until the average inductor current matches the new load current.

The main control loop is shut down by pulling the I_{TH}/RUN pin low. Releasing I_{TH}/RUN allows an internal 0.5µA current source to charge up the external compensation network. When the I_{TH}/RUN pin reaches 0.3V, the main control loop is enabled with the I_{TH}/RUN voltage then pulled up to its zero current level of approximately 0.7V. As the external compensation network continues to charge up, the corresponding output current trip level follows, allowing normal operation.

Comparator OVP guards against transient overshoots >7.5% by turning off the external P-channel power MOSFET and keeping it off until the fault is removed.

Burst Mode Operation

The buck enters Burst Mode operation at low load currents. In this mode, the peak current of the inductor is set as if V_{ITH}/RUN = 1V (at low duty cycles) even though the voltage at the I_{TH}/RUN pin is at a lower value. If the inductor's average current is greater than the load requirement, the voltage at the I_{TH}/RUN pin will drop. When the I_{TH}/RUN voltage goes below 0.85V, the sleep signal goes high, turning off the external MOSFET. The sleep signal goes low when the I_{TH}/RUN voltage goes above 0.925V and the buck resumes normal operation. The next oscillator cycle will turn the external MOSFET on and the switching cycle repeats.

Dropout Operation

When the input supply voltage decreases towards the output voltage, the rate of change of inductor current during the ON cycle decreases. This reduction means that the external P-channel MOSFET will remain on for more than one oscillator cycle since the inductor current has not ramped up to the threshold set by EAMP. Further reduction in input supply voltage will eventually cause the P-channel MOSFET to be turned on 100%, i.e., DC. The output voltage will then be determined by the input voltage minus the voltage drop across the MOSFET, the sense resistor and the inductor.

Undervoltage Lockout

To prevent operation of the P-channel MOSFET below safe input voltage levels, an undervoltage lockout is incorporated into the buck input supply. When the input supply voltage drops below approximately 2.1V, the P-channel MOSFET and all circuitry is turned off except the undervoltage block, which draws only several microamperes.

Short-Circuit Protection

When the output is shorted to ground, the frequency of the oscillator will be reduced to about 110kHz. This lower frequency allows the inductor current to safely discharge, thereby preventing current runaway. The oscillator's frequency will gradually increase to its designed rate when the feedback voltage again approaches 0.8V.

Overvoltage Protection

As a further protection, the overvoltage comparator in the buck will turn the external MOSFET off when the feedback voltage has risen 7.5% above the reference voltage of 0.8V. This comparator has a typical hysteresis of 20mV.

Slope Compensation and Inductor's Peak Current

The inductor's peak current is determined by:

$$I_{PK} = \frac{V_{ITH} - 0.7}{10(R_{SENSE})}$$

OPERATION (Refer to Functional Diagram)

when the buck is operating below 40% duty cycle. However, once the duty cycle exceeds 40%, slope compensation begins and effectively reduces the peak inductor current. The amount of reduction is given by the curves in Figure 2.

Soft-Start

An internal default soft-start circuit is employed at power up and/or when coming out of shutdown. The soft-start circuit works by internally clamping the voltage at the I_{TH}/RUN pin to the corresponding zero-current level and gradually raising the clamp voltage such that the minimum time required for the programmed switch current to reach its maximum is approximately 0.5msec. After the soft-start circuit has timed out, it is disabled until the part is put in shutdown again or the input supply is cycled.

LDO Regulator

The 150mA low dropout (LDO) regulator on the LTC3700 employs an internal P-channel MOSFET pass device between its input supply (V_{IN2}) and the LDO output pin. The pass FET has an on-resistance of approximately 1.5Ω (with V_{IN2} = 4.2V) with a strong dependence on input supply voltage. The dropout voltage is simply the FET on-resistance multiplied by the load current when in dropout.

The LDO is protected by both current limit and thermal shutdown circuits. Current limit is set such that the output voltage will start dropping out when the load current reaches approximately 200mA. With a short-circuited LDO output, the device will limit the sourced current to approximately 225mA. The thermal shutdown circuit has a typical trip point of 150°C with a typical hysteresis of 5°C. In thermal shutdown, the LDO pass device is turned off.

Frequency compensation of the LDO is accomplished by forcing the dominant pole at the output. For stability, a low ESR ceramic capacitor ≥2.2µF is required from LDO to GND. For improved transient response, particularly at heavy loads, it is recommended to use the largest value of capacitor available in the same size considered.

Both the buck and the LDO share the same internally generated bandgap reference voltage for their feedback reference. When both input supplies are present, the internal reference is powered by the buck input supply (V_{IN}). For this reason, line regulation for the LDO output is specified both with respect to V_{IN} and V_{IN2} if the buck is present and with respect only to V_{IN2} if the buck is disabled. The same is true for V_{IN2} supply current, which will be higher when the buck is disabled by the current draw of the internal reference.

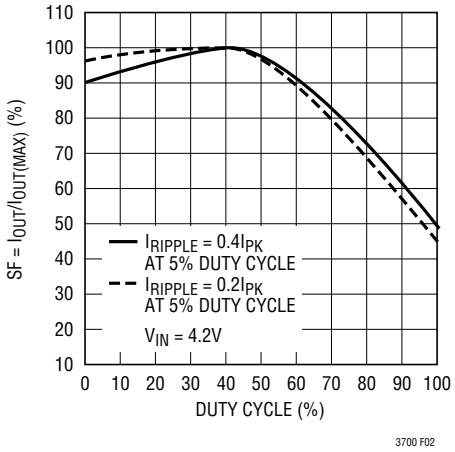


Figure 2. Maximum Output Current vs Duty Cycle

APPLICATIONS INFORMATION

The basic LTC3700 application circuit is shown in Figure 1. External component selection for the buck is driven by the load requirement and begins with the selection of L1 and R_{SENSE} (= R1). Next, the power MOSFET, M1 and the output diode D1 are selected followed by C_{IN} (= C1) and C_{OUT} (= C2).

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. With the current comparator monitoring the voltage developed across R_{SENSE}, the threshold of the comparator determines the inductor's peak current. The output current the buck can provide is given by:

$$I_{OUT} = \frac{0.12}{R_{SENSE}} - \frac{I_{RIPPLE}}{2}$$

where I_{RIPPLE} is the inductor peak-to-peak ripple current (see Inductor Value Calculation section).

A reasonable starting point for setting ripple current is $I_{RIPPLE} = (0.4)(I_{OUT})$. Rearranging the above equation, it becomes:

$$R_{SENSE} = \frac{1}{(10)(I_{OUT})} \text{ for Duty Cycle } < 40\%$$

However, for operation that is above 40% duty cycle, slope compensation effect has to be taken into consideration to select the appropriate value to provide the required amount of current. Using Figure 2, the value of R_{SENSE} is:

$$R_{SENSE} = \frac{SF}{(10)(I_{OUT})(100)}$$

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies permit the use of a smaller inductor for the same amount of inductor ripple current. However, this is at the expense of efficiency due to an increase in MOSFET gate charge losses.

The inductance value also has a direct effect on ripple current. The ripple current, I_{RIPPLE}, decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}. The inductor's peak-to-peak ripple current is given by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{f(L)}\left(\frac{V_{OUT} + V_D}{V_{IN} + V_D}\right)$$

where f is the operating frequency. Accepting larger values of I_{RIPPLE} allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $I_{RIPPLE} = 0.4(I_{OUT(MAX)})$. Remember, the maximum I_{RIPPLE} occurs at the maximum input voltage.

APPLICATIONS INFORMATION

In Burst Mode operation on the LTC3700, the ripple current is normally set such that the inductor current is continuous during the burst periods. Therefore, the peak-to-peak ripple current must not exceed:

$$I_{RIPPLE} \leq \frac{0.03}{R_{SENSE}}$$

This implies a minimum inductance of:

$$L_{MIN} = \frac{V_{IN} - V_{OUT}}{f\left(\frac{0.03}{R_{SENSE}}\right)}\left(\frac{V_{OUT} + V_D}{V_{IN} + V_D}\right)$$

(Use $V_{IN(MAX)} = V_{IN}$)

A smaller value than L_{MIN} could be used in the circuit; however, the inductor current will not be continuous during burst periods.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new designs for surface mount that do not increase the height significantly are available.

Power MOSFET Selection

An external P-channel power MOSFET must be selected for use with the LTC3700. The main selection criteria for the power MOSFET are the threshold voltage $V_{GS(TH)}$ and the "on" resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and total gate charge.

Since the LTC3700 is designed for operation down to low input voltages, a sublogic level threshold MOSFET ($R_{DS(ON)}$ guaranteed at V_{GS} = 2.5V) is required for applications that work close to this voltage. When these MOSFETs are used, make sure that the input supply to the buck is less than the absolute maximum V_{GS} rating, typically 8V.

The required minimum $R_{DS(ON)}$ of the MOSFET is governed by its allowable power dissipation. For applications that may operate the LTC3700 in dropout, i.e., 100% duty cycle, at its worst case the required $R_{DS(ON)}$ is given by:

$$R_{DS(ON)_{DC=100\%}} = \frac{P_P}{\left(I_{OUT(MAX)}\right)^2\left(1+\delta p\right)}$$

where P_P is the allowable power dissipation and δp is the temperature dependency of $R_{DS(ON)}$. (1 + δp) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but δp = 0.005/°C can be used as an approximation for low voltage MOSFETs.

Kool Mμ is a registered trademark of Magnetics, Inc.

APPLICATIONS INFORMATION

In applications where the maximum duty cycle is less than 100% and the buck is in continuous mode, the $R_{DS(ON)}$ is governed by:

$$R_{DS(ON)} \cong \frac{P_P}{(DC)I_{OUT}^2(1+\delta p)}$$

where DC is the maximum operating duty cycle of the buck.

Output Diode Selection

The catch diode carries load current during the off-time. The average diode current is therefore dependent on the P-channel switch duty cycle. At high input voltages the diode conducts most of the time. As V_{IN} approaches V_{OUT} the diode conducts only a small fraction of the time. The most stressful condition for the diode is when the output is short-circuited. Under this condition the diode must safely handle I_{PEAK} at close to 100% duty cycle. Therefore, it is important to adequately specify the diode peak current and average power dissipation so as not to exceed the diode ratings.

Under normal load conditions, the average current conducted by the diode is:

$$I_D = \left(\frac{V_{IN} - V_{OUT}}{V_{IN} + V_D}\right) I_{OUT}$$

The allowable forward voltage drop in the diode is calculated from the maximum short-circuit current as:

$$V_F \approx \frac{P_D}{I_{SC(MAX)}}$$

where P_D is the allowable power dissipation and will be determined by efficiency and/or thermal requirements.

A fast switching diode must also be used to optimize efficiency. Schottky diodes are a good choice for low forward drop and fast switching times. Remember to keep lead length short and observe proper grounding (see Board Layout Checklist) to avoid ringing and increased dissipation.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle $(V_{OUT} + V_D)/(V_{IN} + V_D)$. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx I_{MAX} \frac{\left[V_{OUT}(V_{IN} - V_{OUT})\right]^{1/2}}{V_{IN}}$$

This formula has a maximum value at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet the size or height requirements in the design. Due to the high operating frequency of the LTC3700, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

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The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE}\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR (size) product of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS, AVX TPSV and KEMET T510 series of surface mount tantalum, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON, Nichicon PL series and Panasonic SP.

Low Supply Voltage Operation

Although the LTC3700 can function down to 2.1V (typ), the maximum allowable output current is reduced when V_{IN} decreases below 3V. Figure 3 shows the amount of change as the supply is reduced down to 2.2V. Also shown in Figure 3 is the effect of V_{IN} on V_{REF} as V_{IN} goes below 2.3V.

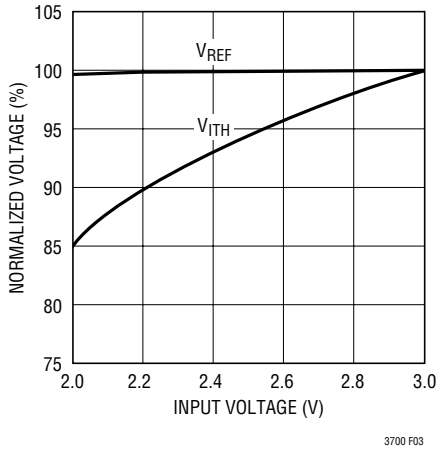


Figure 3. Line Regulation of V_{REF} and V_{ITH}

APPLICATIONS INFORMATION

Setting Output Voltage (Buck Controller)

The buck develops a 0.8V reference voltage between the feedback (Pin 9) terminal and ground (see Figure 4). By selecting resistor R1, a constant current is caused to flow through R1 and R2 to set the overall output voltage. The regulated output voltage is determined by:

$$V_{OUT1} = 0.8\left(1+\frac{R2}{R1}\right)$$

For most applications, an 80k resistor is suggested for R1. To prevent stray pickup, locate resistors R1 and R2 close to LTC3700.

Foldback Current Limiting

As described in the Output Diode Selection, the worst-case dissipation occurs with a short-circuited output when the diode conducts the current limit value almost continuously. To prevent excessive heating in the diode, foldback current limiting can be added to reduce the current in proportion to the severity of the fault.

Foldback current limiting is implemented by adding diodes D_{FB1} and D_{FB2} between the output and the I_{TH}/RUN pin as shown in Figure 5. In a hard short (V_{OUT} = 0V), the current will be reduced to approximately 50% of the maximum output current.

Setting Output Voltage (LDO Regulator)

The LDO develops a 0.8V reference voltage between V_{FB2} (Pin 3) and ground (see Figure 6), similar to the buck controller. The regulated output voltage V_{OUT2} is given by:

$$V_{OUT2} = 0.8\left(1+\frac{R4}{R3}\right)$$

For most applications, an 80k resistor is suggested for R3. To prevent stray pickup, locate resistors R3 and R4 close to LTC3700.

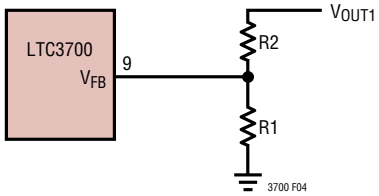


Figure 4. Setting Output Voltage (Buck Controller)

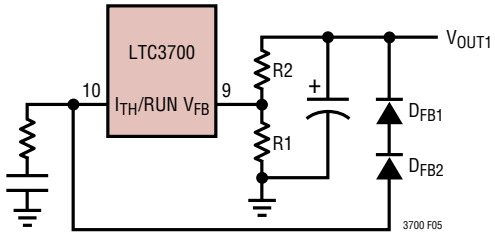


Figure 5. Foldback Current Limiting

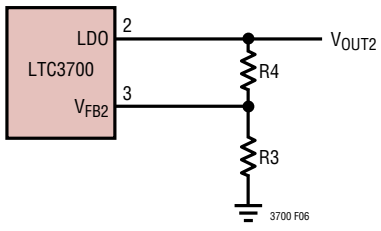
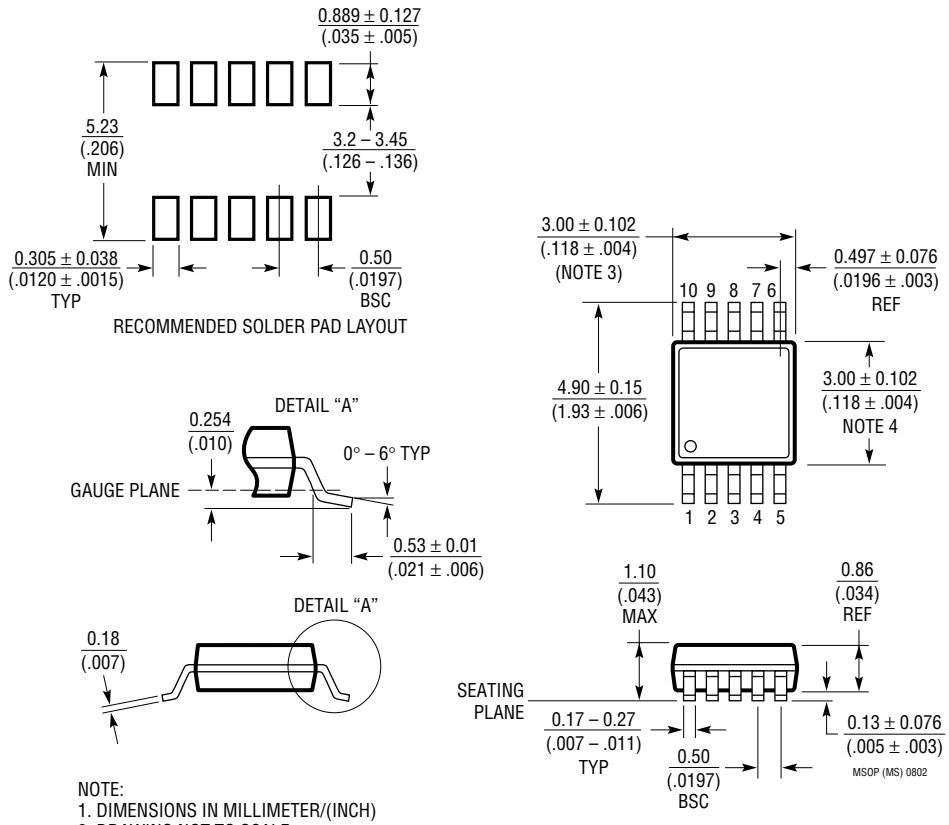


Figure 6. Setting Output Voltage (LDO Regulator)

PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX