Wide Input Range, No R_{SENSE}™ Positive-to-Negative DC/DC Controller

FEATURES

- **High Efficiency Operation (No Sense Resistor Required)**
- **Wide Input Voltage Range: 2.5V to 36V**
- **Current Mode Control Provides Excellent Transient Response**
- **High Maximum Duty Cycle (Typ 92%)**
- **±1% Internal Voltage Reference**
- **±2% RUN Pin Threshold with 100mV Hysteresis**
- Micropower Shutdown: I_Q = 10µA
- Programmable Switching Frequency (50kHz to 1MHz) with One External Resistor
- Synchronizable to an External Clock Up to 1.3 × f_{OSC}
- User-Controlled Pulse Skip or Burst Mode® Operation
- Internal 5.2V Low Dropout Voltage Regulator
- Capable of Operating with a Sense Resistor for High Output Voltage Applications (V_{DS} >36V)
- Small 10-Lead MSOP Package

APPLICATIONS

- SLIC Power Supplies
- Telecom Power Supplies
- Portable Electronic Equipment
- Cable and DSL Modems
- Router Supplies

DESCRIPTION

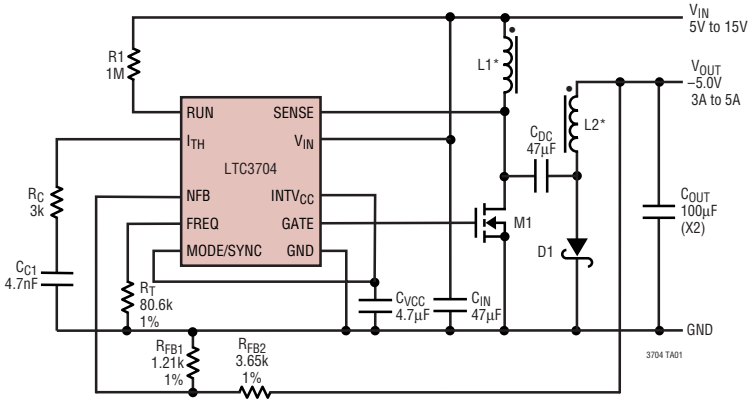
The LTC®3704 is a wide input range, current mode, positive-to-negative DC/DC controller that drives an N-channel power MOSFET and requires very few external components. Intended for low to high power applications, it eliminates the need for a current sense resistor by utilizing the power MOSFET's on-resistance, thereby maximizing efficiency.

The IC's operating frequency can be set with an external resistor over a 50kHz to 1MHz range, and can be synchronized to an external clock using the MODE/SYNC pin. Burst Mode operation at light loads, a low minimum operating supply voltage of 2.5V and a low shutdown quiescent current of 10µA make the LTC3704 ideally suited for battery-operated systems.

For applications requiring constant frequency operation, the Burst Mode operation feature can be defeated using the MODE/SYNC pin. Higher than 36V switch voltage applications are possible with the LTC3704 by connecting the SENSE pin to a resistor in the source of the power MOSFET.

The LTC3704 is available in the 10-lead MSOP package.

TYPICAL APPLICATION



CIN, CDC : TDK C5750X5R1C476M
COUT: TDK C5750X5R0J107M
CVCC: TAIYO YUDEN LMK316BJ475ML

D1: MBRD835L (ON SEMICONDUCTOR)
L1, L2: BH ELECTRONICS BH510-1009
M1: Si4884 (SILICONIX/VISHAY)

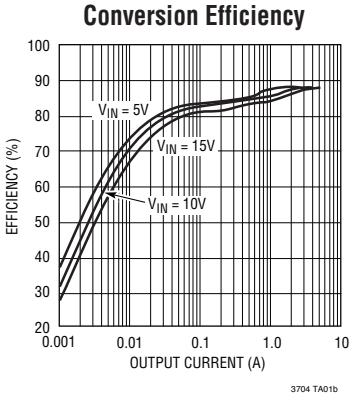


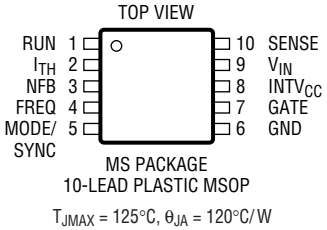
Figure 1. High Efficiency Positive to Negative Supply

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage ..... –0.3V to 36V
$INTV_{CC}$ Voltage ..... –0.3V to 7V
$INTV_{CC}$ Output Current 50mA
GATE Voltage ..... –0.3V to V_{INTVCC} + 0.3V
I_{TH} Voltage ..... –0.3V to 2.7V
NFB Voltage ..... –2.7V to 2.7V
RUN, MODE/SYNC Voltages ..... –0.3V to 7V
FREQ Voltage ..... –0.3V to 1.5V
SENSE Pin Voltage ..... –0.3V to 36V
Operating Temperature Range (Note 2) .. –40°C to 85°C
  LTC3704E ..... –40°C to 85°C
  LTC3704I ..... –40°C to 125°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 120°C/W

ORDER PART NUMBER	MS PART MARKING
LTC3704EMS LTC3704IMS	LTYT LTCFW

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{INTVCC} = 5V, V_{RUN} = 1.5V, R_T = 80k, $V_{MODE/SYNC}$ = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
$V_{IN(MIN)}$	Minimum Input Voltage			2.5			V
I_Q	Input Voltage Supply Current Continuous Mode Burst Mode Operation, No Load Shutdown Mode	(V_{INTVCC} = Open, No Switching) (Note 4) $V_{MODE/SYNC}$ = 5V, V_{ITH} = 0.75V $V_{MODE/SYNC}$ = 0V, V_{ITH} = 0V (Note 5) V_{RUN} = 0V			 550 250 10	 1000 500 20	 µA µA µA
V_{RUN}^+	Rising RUN Input Threshold Voltage	V_{INTVCC} = Open			1.348		V
V_{RUN}^-	Falling RUN Input Threshold Voltage	V_{INTVCC} = Open	 ●	1.223 1.198	1.248	1.273 1.298	V V
$V_{RUN(HYST)}$	RUN Pin Input Threshold Hysteresis			50	100	150	mV
I_{RUN}	RUN Input Current				1	100	nA
V_{NFB}	Negative Feedback Voltage	V_{ITH} = 0.4V (Note 5) V_{ITH} = 0.4V (Note 5) V_{ITH} = 0.4V (I-Grade) (Notes 2 and 5)	 ● ●	–1.218 –1.212 –1.205	–1.230	–1.242 –1.248 –1.255	V V V
I_{NFB}	NFB Pin Input Current				7.5	15	µA
$\frac{\Delta V_{NFB}}{\Delta V_{IN}}$	Line Regulation	2.5V ≤ V_{IN} ≤ 30V			0.002	0.02	%/V
$\frac{\Delta V_{NFB}}{\Delta V_{ITH}}$	Load Regulation	$V_{MODE/SYNC}$ = 0V, V_{ITH} = 0.5V to 0.90V (Note 5)	●	–1	–0.1		%
g_m	Error Amplifier Transconductance	I_{TH} Pin Load = ±5µA (Note 5)			650		µmho
$V_{ITH(BURST)}$	Burst Mode Operation I_{TH} Pin Voltage	Falling I_{TH} Voltage			0.17		V
$V_{SENSE(MAX)}$	Maximum Current Sense Input Threshold	Duty Cycle < 20%		120	150	180	mV
$I_{SENSE(ON)}$	SENSE Pin Current (GATE High)	V_{SENSE} = 0V			40	75	µA
$I_{SENSE(OFF)}$	SENSE Pin Current (GATE Low)	V_{SENSE} = 30V			0.1	5	µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{INTVCC} = 5V, V_{RUN} = 1.5V, R_{FREQ} = 80k, $V_{MODE/SYNC}$ = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator							
f_{OSC}	Oscillator Frequency	R_{FREQ} = 80k		250	300	350	kHz
	Oscillator Frequency Range			50		1000	kHz
D_{MAX}	Maximum Duty Cycle			87	92	97	%
f_{SYNC}/f_{OSC}	Recommended Maximum Synchronized Frequency Ratio	f_{OSC} = 300kHz (Note 6)			1.25	1.30	
$t_{SYNC(MIN)}$	MODE/SYNC Minimum Input Pulse Width	V_{SYNC} = 0V to 5V			25		ns
$t_{SYNC(MAX)}$	MODE/SYNC Maximum Input Pulse Width	V_{SYNC} = 0V to 5V			$0.8/f_{OSC}$		ns
$V_{IL(MODE)}$	Low Level MODE/SYNC Input Voltage					0.3	V
$V_{IH(MODE)}$	High Level MODE/SYNC Input Voltage			1.2			V
$R_{MODE/SYNC}$	MODE/SYNC Input Pull-Down Resistance				50		kΩ
V_{FREQ}	Nominal FREQ Pin Voltage				0.62		V
Low Dropout Regulator							
V_{INTVCC}	$INTV_{CC}$ Regulator Output Voltage	V_{IN} = 7.5V		5.0	5.2	5.4	V
$\frac{\Delta V_{INTVCC}}{\Delta V_{IN1}}$	$INTV_{CC}$ Regulator Line Regulation	7.5V ≤ V_{IN} ≤ 15V			8	25	mV
$\frac{\Delta V_{INTVCC}}{\Delta V_{IN2}}$	$INTV_{CC}$ Regulator Line Regulation	15V ≤ V_{IN} ≤ 30V			70	200	mV
$V_{LDO(LOAD)}$	$INTV_{CC}$ Load Regulation	V_{IN} = 7.5V, 0 ≤ I_{INTVCC} ≤ 20mA		–2	–0.2		%
$V_{DROPOUT}$	$INTV_{CC}$ Regulator Dropout Voltage	V_{INTVCC} = Open, $INTV_{CC}$ Load = 20mA			280		mV
I_{INTVCC}	Bootstrap Mode $INTV_{CC}$ Supply Current in Shutdown	RUN = 0V, SENSE = 5V			10	20	µA
GATE Driver							
t_r	GATE Driver Output Rise Time	C_L = 3300pF (Note 7)			17	100	ns
t_f	GATE Driver Output Fall Time	C_L = 3300pF (Note 7)			8	100	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliabilty and lifetime.

Note 2: The LTC3704E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3704I is guaranteed over the full –40°C to 125°C operating temperature range.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$T_J = T_A + (P_D \bullet 120°C/W)$

Note 4: The dynamic input supply current is higher due to power MOSFET gate charging ($Q_G \bullet f_{OSC}$). See Applications Information.

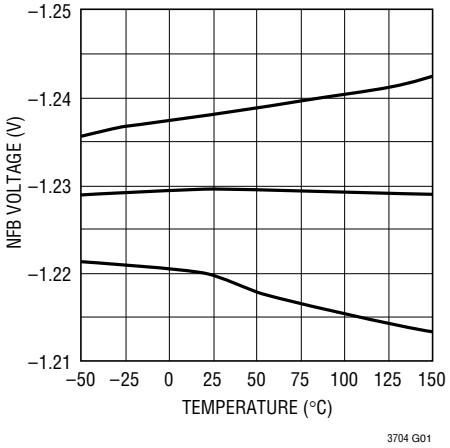
Note 5: The LTC3704 is tested in a feedback loop that servos V_{NFB} to the reference voltage with the I_{TH} pin forced to a voltage between 0V and 1.4V (the no load to full load operating voltage range for the I_{TH} pin is 0.3V to 1.23V).

Note 6: In a synchronized application, the internal slope compensation gain is increased by 25%. Synchronizing to a significantly higher ratio will reduce the effective amount of slope compensation, which could result in subharmonic oscillation for duty cycles greater than 50%.

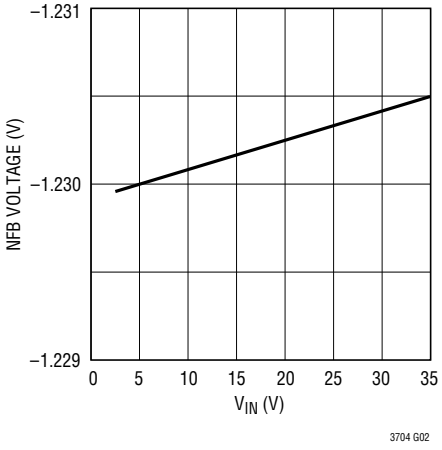
Note 7: Rise and fall times are measured at 10% and 90% levels.

TYPICAL PERFORMANCE CHARACTERISTICS

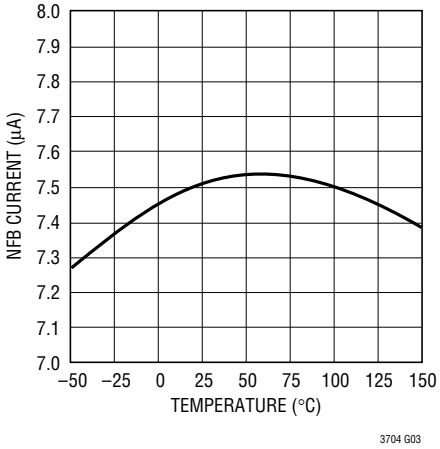
NFB Voltage vs Temp



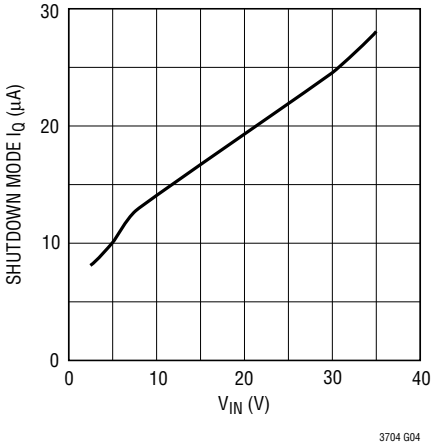
NFB Voltage Line Regulation



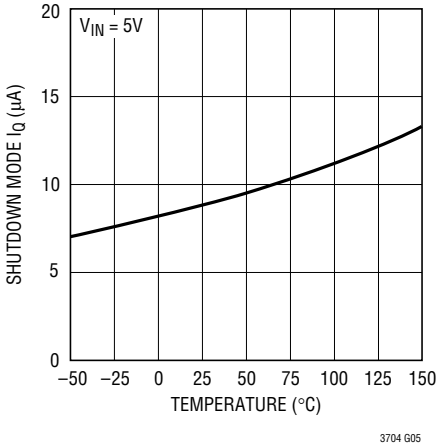
NFB Pin Current vs Temperature



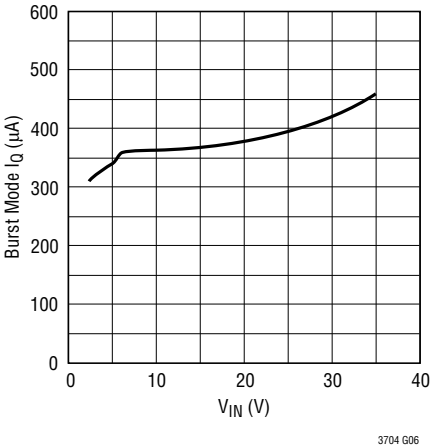
Shutdown Mode I_Q vs V_{IN}



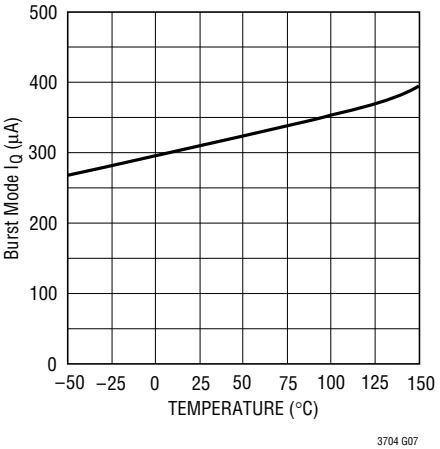
Shutdown Mode I_Q vs Temperature



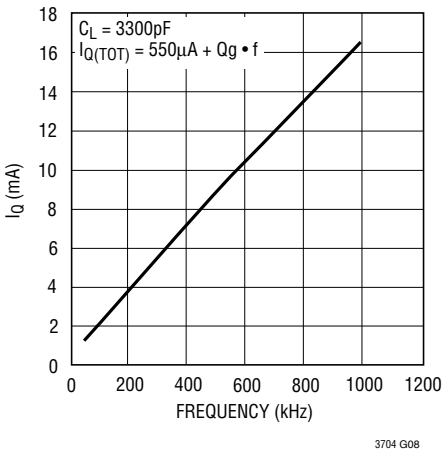
Burst Mode I_Q vs V_{IN}



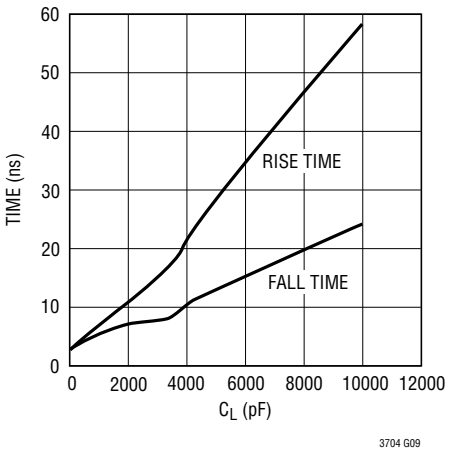
Burst Mode I_Q vs Temperature



Dynamic I_Q vs Frequency

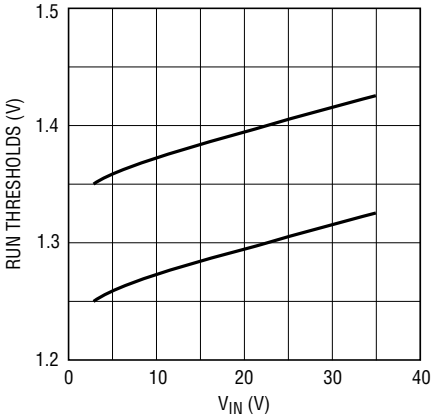


Gate Drive Rise and Fall Time vs C_L



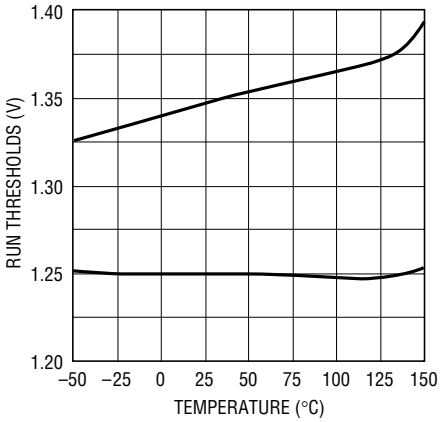
TYPICAL PERFORMANCE CHARACTERISTICS

RUN Thresholds vs V_{IN}



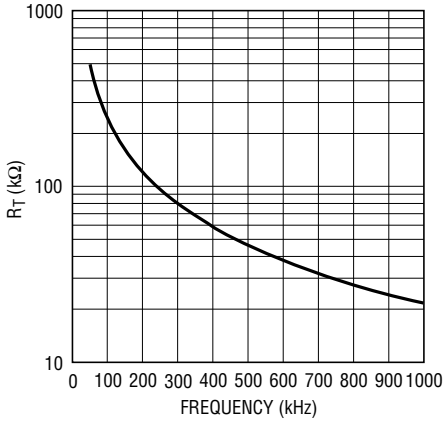
3704 G10

RUN Thresholds vs Temperature



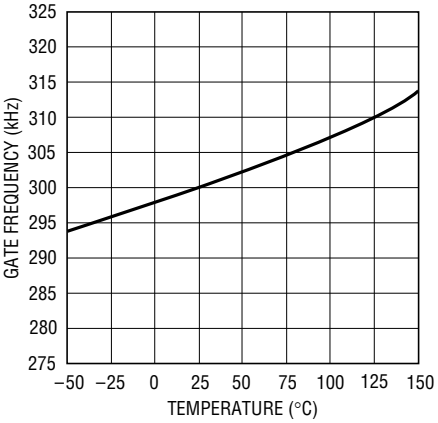
3704 G11

R_T vs Frequency



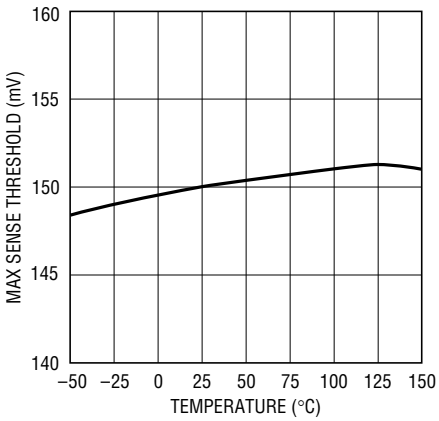
3704 G12

Frequency vs Temperature



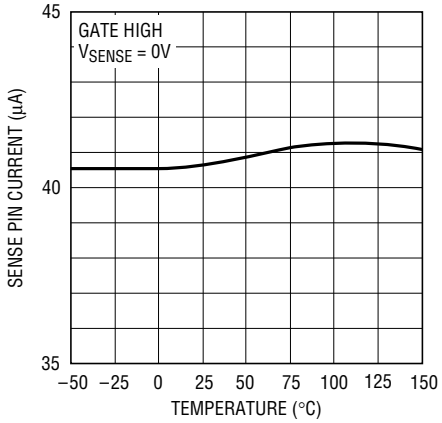
3704 G13

Maximum Sense Threshold vs Temperature



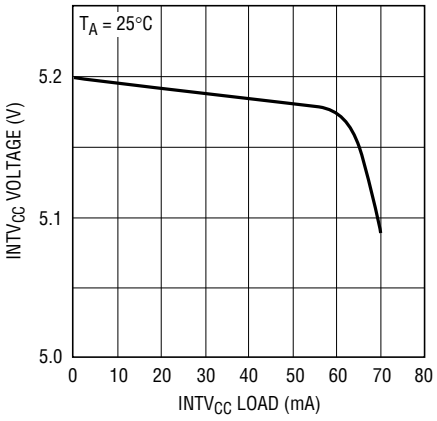
3704 G14

SENSE Pin Current vs Temperature



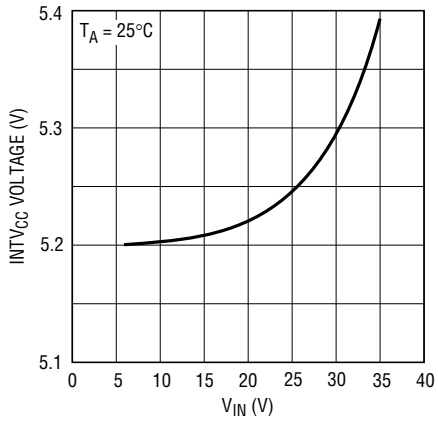
3704 G15

$INTV_{CC}$ Load Regulation



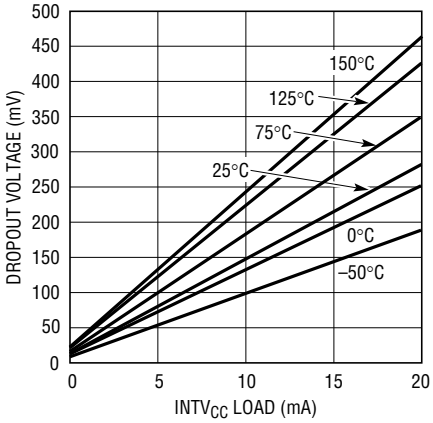
3704 G16

$INTV_{CC}$ Line Regulation



3704 G17

$INTV_{CC}$ Dropout Voltage vs Current, Temperature



3704 G18

PIN FUNCTIONS

RUN (Pin 1): The RUN pin provides the user with an accurate means for sensing the input voltage and programming the start-up threshold for the converter. The falling RUN pin threshold is nominally 1.248V and the comparator has 100mV of hysteresis for noise immunity. When the RUN pin is below this input threshold, the IC is shut down and the V_{IN} supply current is kept to a low value (typ 10μA). The Absolute Maximum Rating for the voltage on this pin is 7V.

I_{TH} (Pin 2): Error Amplifier Compensation Pin. The current comparator input threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 1.40V.

NFB (Pin 3): Receives the feedback voltage from the external resistor divider across the output. Nominal voltage for this pin in regulation is –1.230V.

FREQ (Pin 4): A resistor from the FREQ pin to ground programs the operating frequency of the chip. The nominal voltage at the FREQ pin is 0.62V.

MODE/SYNC (Pin 5): This input controls the operating mode of the converter and allows for synchronizing the operating frequency to an external clock. If the MODE/SYNC pin is connected to ground, Burst Mode operation is enabled. If the MODE/SYNC pin is connected to $INTV_{CC}$, or if an external logic-level synchronization signal is applied to this input, Burst Mode operation is disabled and the IC operates in a continuous mode.

GND (Pin 6): Ground Pin.

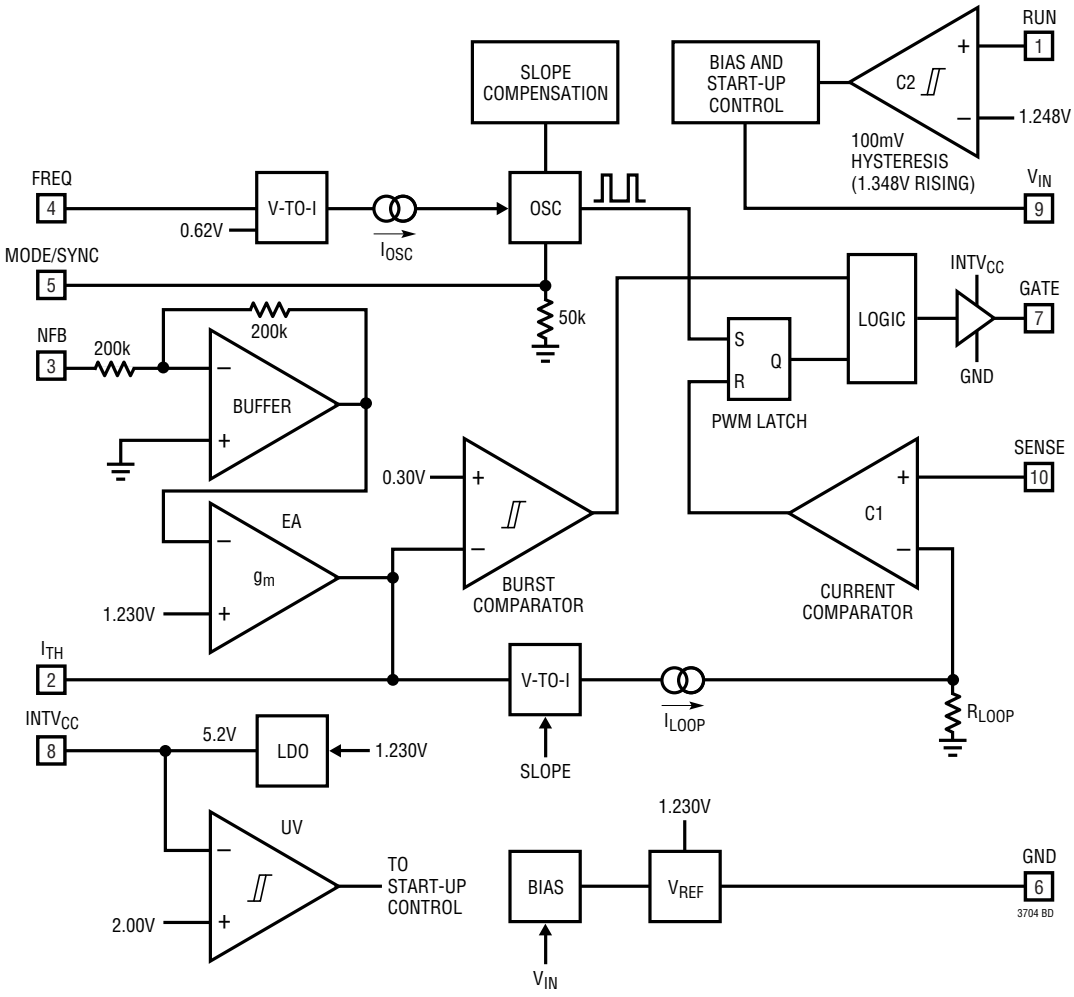
GATE (Pin 7): Gate Driver Output.

$INTV_{CC}$ (Pin 8): The Internal 5.20V Regulator Output. The gate driver and control circuits are powered from this voltage. Decouple this pin locally to the IC ground with a minimum of 4.7μF low ESR tantalum or ceramic capacitor.

V_{IN} (Pin 9): Main Supply Pin. Must be closely decoupled to ground.

SENSE (Pin 10): The Current Sense Input for the Control Loop. Connect this pin to the drain of the power MOSFET for V_{DS} sensing and highest efficiency. Alternatively, the SENSE pin may be connected to a resistor in the source of the power MOSFET. Internal leading edge blanking is provided for both sensing methods.

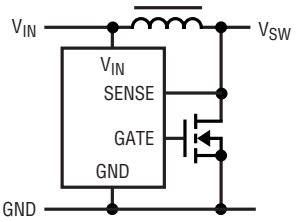
BLOCK DIAGRAM



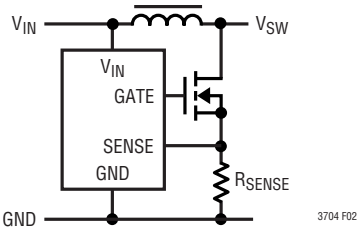
OPERATION

Main Control Loop

The LTC3704 is a constant frequency, current mode controller for DC/DC positive-to-negative converter applications. The LTC3704 is distinguished from conventional current mode controllers because the current control loop can be closed by sensing the voltage drop across the power MOSFET switch instead of across a discrete sense resistor, as shown in Figure 2. This sensing technique improves efficiency, increases power density, and reduces the cost of the overall solution.



2a. SENSE Pin Connection for Maximum Efficiency (V_{SW} < 36V)



2b. SENSE Pin Connection for Precise Control of Peak I_{IN}/I_{OUT} or for V_{SW} > 36V

Figure 2. Using the SENSE Pin On the LTC3704

For circuit operation, please refer to the Block Diagram of the IC and Figure 1. In normal operation, the power MOSFET is turned on when the oscillator sets the PWM latch and is turned off when the current comparator C1 resets the latch. The divided-down output voltage is compared to an internal 1.230V reference by the error amplifier EA, which outputs an error signal at the I_{TH} pin. The voltage on the I_{TH} pin sets the current comparator C1 input threshold. When the load current increases, a fall in the NFB voltage relative to the reference voltage causes the I_{TH} pin to rise, which causes the current comparator C1 to trip at a higher peak inductor current value. The average inductor current will therefore rise until it equals the load current, thereby maintaining output regulation.

The nominal operating frequency of the LTC3704 is programmed using a resistor from the FREQ pin to ground and can be controlled over a 50kHz to 1000kHz range. In addition, the internal oscillator can be synchronized to an external clock applied to the MODE/SYNC pin and can be locked to a frequency between 100% and 130% of its nominal value. When the MODE/SYNC pin is left open, it is pulled low by an internal 50k resistor and Burst Mode operation is enabled. If this pin is taken above 2V or an external clock is applied, Burst Mode operation is disabled and the IC operates in continuous mode. With no load (or an extremely light load), the controller will skip pulses in order to maintain regulation and prevent excessive output ripple.

The RUN pin controls whether the IC is enabled or is in a low current shutdown state. A micropower 1.248V reference and comparator C2 allow the user to program the supply voltage at which the IC turns on and off (comparator C2 has 100mV of hysteresis for noise immunity). With the RUN pin below 1.248V, the chip is off and the input supply current is typically only 10μA.

The LTC3704 can be used either by sensing the voltage drop across the power MOSFET or by connecting the SENSE pin to a conventional shunt resistor in the source of the power MOSFET, as shown in Figure 2. Sensing the voltage across the power MOSFET maximizes converter efficiency and minimizes the component count, but limits the output voltage to the maximum rating for this pin (36V). By connecting the SENSE pin to a resistor in the source of the power MOSFET, the user is able to program output voltages significantly greater than the 36V maximum input voltage rating for the IC.

Programming the Operating Mode

For applications where maximizing the efficiency at very light loads (e.g., <100μA) is a high priority, Burst Mode operation should be applied (i.e., the MODE/SYNC pin should be connected to ground). In applications where fixed frequency operation is more critical than low current efficiency, or where the lowest output ripple is desired, pulse-skip mode operation should be used and the MODE/SYNC pin should be connected to the $INTV_{CC}$ pin. This allows discontinuous conduction mode (DCM) operation down to near the limit defined by the chip's

OPERATION

minimum on-time (about 175ns). Below this output current level, the converter will begin to skip cycles in order to maintain output regulation. Figures 3 and 4 show the light load switching waveforms for Burst Mode and Pulse-Skip Mode operation for the converter in Figure 1.

Burst Mode Operation

Burst Mode operation is selected by leaving the MODE/SYNC pin unconnected or by connecting it to ground. In normal operation, the range on the I_{TH} pin corresponding to no load to full load is 0.30V to 1.2V. In Burst Mode operation, if the error amplifier EA drives the I_{TH} voltage below 0.525V, the buffered I_{TH} input to the current comparator C1 will be clamped at 0.525V (which corresponds to 25% of maximum load current). The inductor current peak is then held at approximately 30mV divided by the power MOSFET $R_{DS(ON)}$. If the I_{TH} pin drops below 0.30V, the Burst Mode comparator B1 will turn off the power MOSFET and scale back the quiescent current of the IC to 250μA (sleep mode). In this condition, the load current will be supplied by the output capacitor until the I_{TH} voltage rises above the 50mV hysteresis of the burst comparator. At light loads, short bursts of switching (where the average inductor current is 25% of its maximum value) followed by long periods of sleep will be observed, thereby greatly improving converter efficiency. Oscilloscope waveforms illustrating Burst Mode operation are shown in Figure 3.

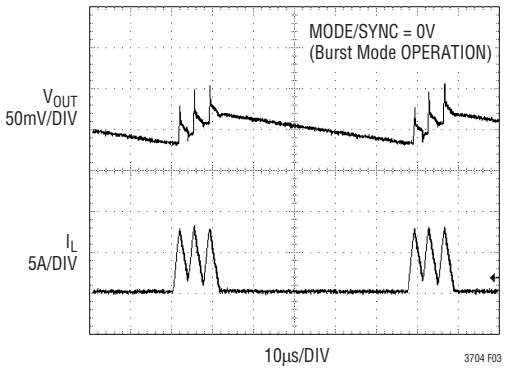


Figure 3. LTC3704 Burst Mode Operation (MODE/SYNC = 0V) at Low Output Current

Pulse-Skip Mode Operation

With the MODE/SYNC pin tied to a DC voltage above 1.2V, Burst Mode operation is disabled. The internal, 0.525V buffered I_{TH} burst clamp is removed, allowing the I_{TH} pin to directly control the current comparator from no load to full load. With no load, the I_{TH} pin is driven below 0.30V, the power MOSFET is turned off and sleep mode is invoked. Oscilloscope waveforms illustrating this mode of operation are shown in Figure 4.

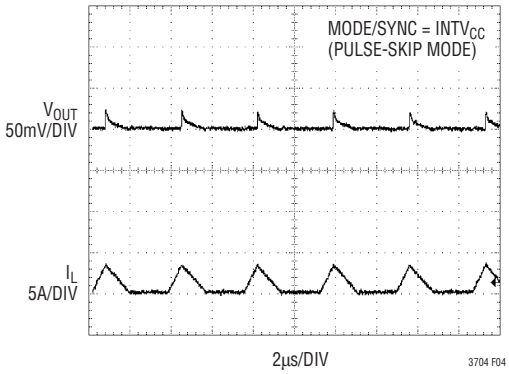


Figure 4. LTC3704 Low Output Current Operation with Burst Mode Operation Disabled (MODE/SYNC = $INTV_{CC}$)

When an external clock signal drives the MODE/SYNC pin at a rate faster than the chip's internal oscillator, the oscillator will synchronize to it. In this synchronized mode, Burst Mode operation is disabled. The constant frequency associated with synchronized operation provides a more controlled noise spectrum from the converter, at the expense of overall system efficiency of light loads.

When the oscillator's internal logic circuitry detects a synchronizing signal on the MODE/SYNC pin, the internal oscillator ramp is terminated early and the slope compensation is increased by approximately 30%. As a result, in applications requiring synchronization, it is recommended that the nominal operating frequency of the IC be programmed to be about 75% of the external clock frequency. Attempting to synchronize to too high an external frequency (above $1.3f_O$) can result in inadequate slope compensation and possible subharmonic oscillation (or jitter).

The external clock signal must exceed 2V for at least 25ns, and should have a maximum duty cycle of 80%, as shown in Figure 5. The MOSFET turn on will synchronize to the rising edge of the external clock signal.

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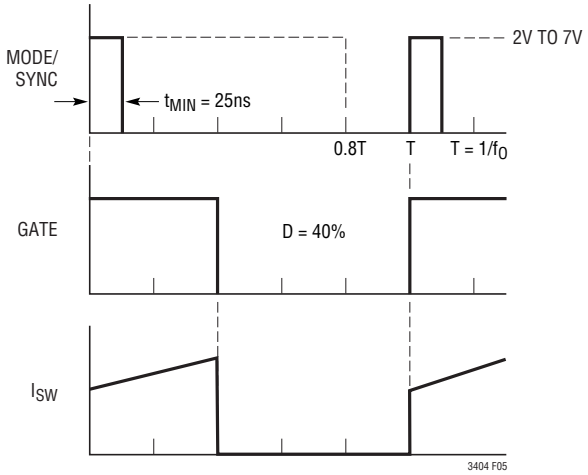

Figure 5. MODE/SYNC Clock Input and Switching Waveforms for Synchronized Operation

Programming the Operating Frequency

The choice of operating frequency and inductor value is a tradeoff between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET and diode switching losses. However, lower frequency operation requires more inductance for a given amount of load current.

The LTC3704 uses a constant frequency architecture that can be programmed over a 50kHz to 1000kHz range with a single external resistor from the FREQ pin to ground, as shown in Figure 1. The nominal voltage on the FREQ pin is 0.6V, and the current that flows into the FREQ pin is used to charge and discharge an internal oscillator capacitor. A graph for selecting the value of R_T for a given operating frequency is shown in Figure 6.

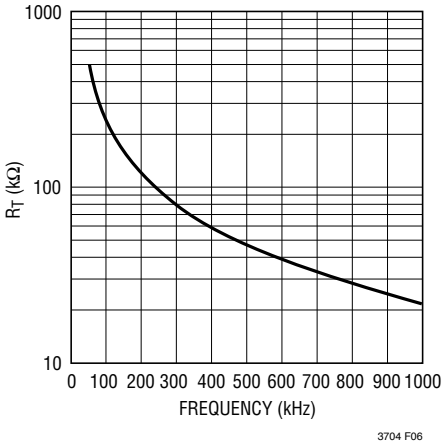

Figure 6. Timing Resistor (R_T) Value

$INTV_{CC}$ Regulator Bypassing and Operation

An internal, P-channel low dropout voltage regulator produces the 5.2V supply which powers the gate driver and logic circuitry within the LTC3704, as shown in Figure 7. The $INTV_{CC}$ regulator can supply up to 50mA and must be bypassed to ground immediately adjacent to the IC pins with a minimum of 4.7µF tantalum or ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate driver.

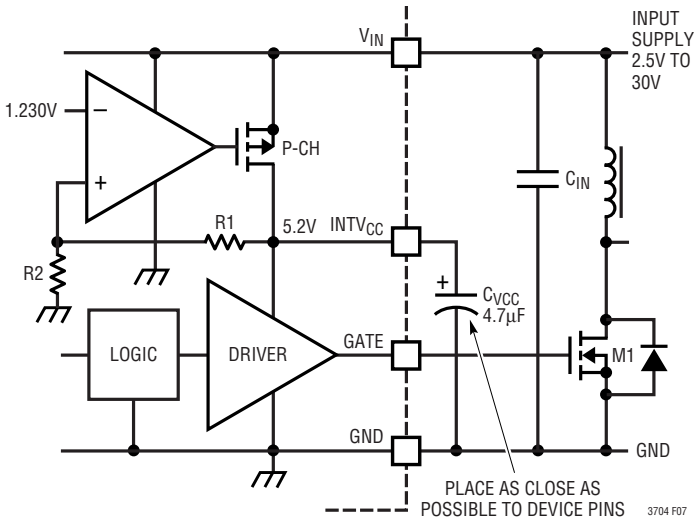

Figure 7. Bypassing the LDO Regulator and Gate Driver Supply

For input voltages that don't exceed 7V (the absolute maximum rating for this pin), the internal low dropout regulator in the LTC3704 is redundant and the $INTV_{CC}$ pin can be shorted directly to the V_{IN} pin. With the $INTV_{CC}$ pin shorted to V_{IN}, however, the divider that programs the regulated $INTV_{CC}$ voltage will draw 10µA of current from the input supply, even in shutdown mode. For applications that require the lowest shutdown mode input supply current, do not connect the $INTV_{CC}$ pin to V_{IN}. Regardless of whether the $INTV_{CC}$ pin is shorted to V_{IN} or not, **it is always necessary to have the driver circuitry bypassed with a 4.7µF tantalum or low ESR ceramic capacitor to ground immediately adjacent to the $INTV_{CC}$ and GND pins.**

In an actual application, most of the IC supply current is used to drive the gate capacitance of the power MOSFET. As a result, high input voltage applications in which a large power MOSFET is being driven at high frequencies can

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cause the LTC3704 to exceed its maximum junction temperature rating. The junction temperature can be estimated using the following equations:

$I_{Q(TOT)} \approx I_Q + f \bullet Q_G$

$P_{IC} = V_{IN} \bullet (I_Q + f \bullet Q_G)$

$T_J = T_A + P_{IC} \bullet R_{TH(JA)}$

The total quiescent current $I_{Q(TOT)}$ consists of the static supply current (I_Q) and the current required to charge and discharge the gate of the power MOSFET. The 10-pin MSOP package has a thermal resistance of $R_{TH(JA)}$ = 120°C/W.

As an example, consider a power supply with V_{IN} = 5V and $V_{SW(MAX)}$ = 12V. The switching frequency is 500kHz, and the maximum ambient temperature is 70°C. The power MOSFET chosen is the IRF7805, which has a maximum $R_{DS(ON)}$ of 11mΩ (at room temperature) and a maximum total gate charge of 37nC (the temperature coefficient of the gate charge is low).

$I_{Q(TOT)}$ = 600µA + 37nC • 500kHz = 19.1mA

P_{IC} = 5V • 19.1mA = 95mW

T_J = 70°C + 120°C/W • 95mW = 81.4°C

This demonstrates how significant the gate charge current can be when compared to the static quiescent current in the IC.

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked when operating in a continuous mode at high V_{IN}. A tradeoff between the operating frequency and the size of the power MOSFET may need to be made in order to maintain a reliable IC junction temperature. Prior to lowering the operating frequency, however, be sure to check with power MOSFET manufacturers for their latest-and-greatest low Q_G, low $R_{DS(ON)}$ devices. Power MOSFET manufacturing technologies are continually improving, with newer and better performance devices being introduced almost yearly.

Output Voltage Programming

The output voltage is set by a resistor divider according to the following formula:

$$V_O = V_{REF} \bullet \left(1 + \frac{R2}{R1}\right) + I_{NFB} \bullet R2$$

where V_{REF} = –1.230V, and I_{NFB} is the current which flows out of the NFB pin (I_{NFB} = –7.5µA). In order to properly dimension R2, including the effect of the NFB pin current, the following formula can be used:

$$R2 = \frac{V_{OUT} - V_{REF}}{\left(\frac{V_{REF}}{R1} + I_{NFB}\right)}$$

The nominal 7.5µA current which flows out of the NFB pin has a production tolerance of approximately ±2.5µA, so an output divider current of 500µA (R1 = 2.49k) results in a 0.5% uncertainty in the output voltage. For low power applications where the output voltage tolerance is less important, efficiency can be increased by increasing the value of R1.

Programming Turn-On and Turn-Off Thresholds with the RUN Pin

The LTC3704 contains an independent, micropower voltage reference and comparator detection circuit that remains active even when the device is shut down, as shown in Figure 8. This allows users to accurately program an input voltage at which the converter will turn on and off. The falling threshold voltage on the RUN pin is equal to the internal reference voltage of 1.248V. The comparator has 100mV of hysteresis to increase noise immunity.

The turn-on and turn-off input voltage thresholds are programmed using a resistor divider according to the following formulas:

$$V_{IN(OFF)} = 1.248V \bullet \left(1 + \frac{R2}{R1}\right)$$

$$V_{IN(ON)} = 1.348V \bullet \left(1 + \frac{R2}{R1}\right)$$

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The resistor R1 is typically chosen to be less than 1M.

For applications where the RUN pin is only to be used as a logic input, the user should be aware of the 7V Absolute Maximum Rating for this pin! The RUN pin can be connected to the input voltage through an external 1M resistor, as shown in Figure 8c, for "always on" operation.

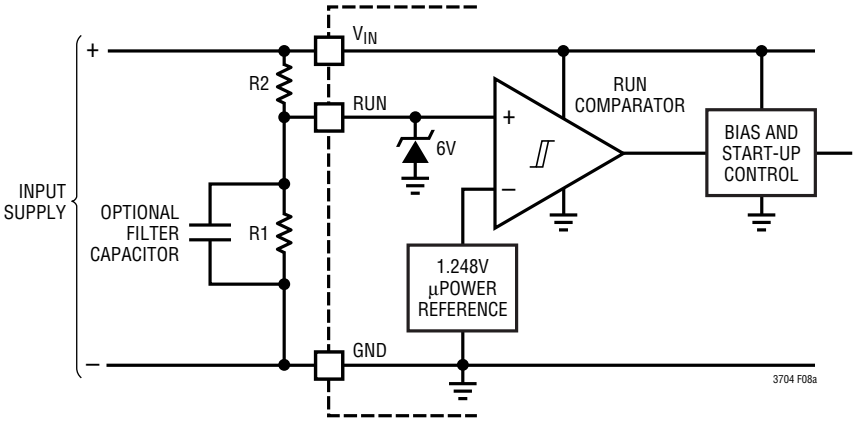

Figure 8a. Programming the Turn-On and Turn-Off Thresholds Using the RUN Pin

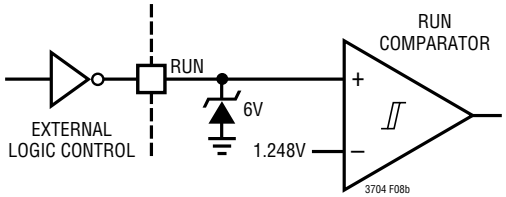

Figure 8b. On/Off Control Using External Logic

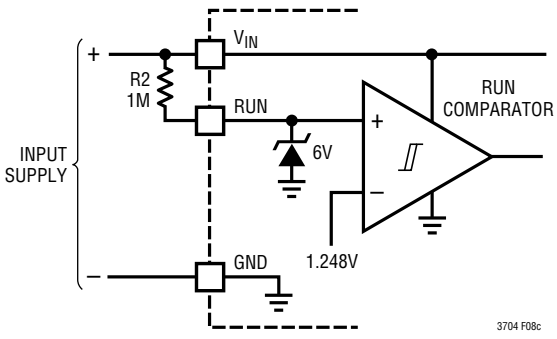

Figure 8c. External Pull-Up Resistor On RUN Pin for "Always On" Operation

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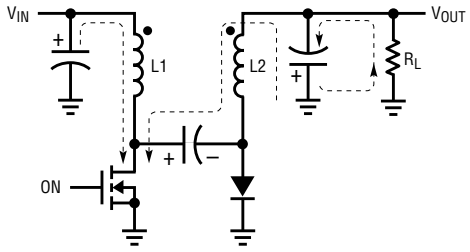
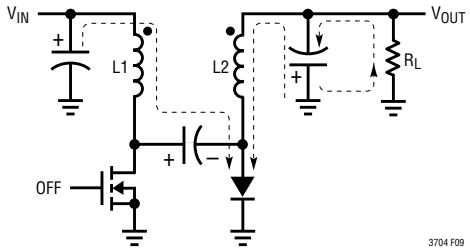
Applications Circuits

A simple positive-to-negative application circuit for the LTC3704 is shown in Figure 1. The basic operation of this circuit is shown in Figure 9. During the on-time the inductor currents flow through the switch, and during the off-time these currents flow through the output diode. The use of inductors in series with both the input and output results in continuous currents in these capacitors, resulting in low input and output noise. Discontinuous currents flow in the switch, the coupling capacitor, and the diode.



a) Current Flow During The Switch On-Time



b) Current Flow During The Switch Off-Time

Figure 9. Positive-to-Negative Converter Operation

Duty Cycle Considerations

For the positive-to-negative converter shown in Figure 1, the duty cycle of the main switch in CCM is:

$$D = \frac{V_O}{V_O - V_{IN}}$$

where V_O is a negative number. The maximum output voltage for this converter (in CCM) is:

$$V_{O(MAX)} = V_{IN(MIN)} \bullet \frac{D_{MAX}}{1 - D_{MAX}}$$

The maximum duty cycle capability of the LTC3704 is typically 92%.

Peak and Average Input and Switch Currents

The control loop in the LTC3704 is measuring the peak switch current (either by using the $R_{DS(ON)}$ of the power MOSFET or by using a sense resistor in the MOSFET source), so the output current needs to be reflected back to the switch in order to dimension the power MOSFET and inductors properly. Based on the fact that, ideally, the input power is equal to the output power, the maximum average input current is:

$$I_{IN(MAX)} = -I_{O(MAX)} \bullet \frac{D_{MAX}}{1 - D_{MAX}}$$

where $I_{O(MAX)}$ is a negative number. The peak input current is:

$$I_{IN(PEAK)} = -\left(1 + \frac{\chi}{2}\right) \bullet I_{O(MAX)} \bullet \frac{D_{MAX}}{1 - D_{MAX}}$$

In a positive-to-negative converter, however, the switch current is equal to $I_{IN} + I_O$, so the maximum average switch current is:

$$I_{SW(MAX)} = -I_{O(MAX)} \bullet \frac{1}{1 - D_{MAX}}$$

and the peak switch current is:

$$I_{SW(PEAK)} = -\left(1 + \frac{\chi}{2}\right) \bullet I_{O(MAX)} \bullet \frac{1}{1 - D_{MAX}}$$

The maximum duty cycle, D_{MAX}, should be calculated at minimum V_{IN}.

Ripple Current ΔI_L and the 'χ' Factor

The constant 'χ' in the equation above represents the percentage peak-to-peak total ripple current in the inductor, relative to its maximum value. For example, if 30% ripple current is chosen, then χ = 0.30, and the peak current is 15% greater than the average.

For a current mode converter operating in CCM, slope compensation must be added for duty cycles above 50% in order to avoid subharmonic oscillation. For the LTC3704, this ramp compensation is internal. Having an internally fixed ramp compensation waveform, however, does place some constraints on the value of the inductor and the operating frequency. If too large an inductor is used, the resulting current ramp (ΔI_L) will be small relative to the

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internal ramp compensation (at duty cycles above 50%), and the converter operation will approach voltage mode (ramp compensation reduces the gain of the current loop). If too small an inductor is used, but the converter is still operating in CCM (near critical conduction mode), the internal ramp compensation may be inadequate to prevent subharmonic oscillation. To ensure good current mode gain and avoid subharmonic oscillation, it is recommended that the ripple current in the inductor fall in the range of 20% to 40% of the maximum average switch current. For example, if the maximum average switch current is 1A, choose a ΔI_L between 0.2A and 0.4A, and a value 'χ' between 0.2 and 0.4.

Inductor Selection

Selecting inductors for a positive-to-negative converter is slightly more complicated than for a single-inductor topology like a buck or boost. The use of separate, uncoupled inductors can reduce the size of the solution, at the expense of input and output ripple. Using a coupled inductor complicates the design procedure, but can result in significantly lower input and/or output ripple. It will also reduce the number of components that the purchasing department has to keep track of.

Regardless of the design goals, however, the inductor selection process is an iterative one. The best recommendation is to use the equations as a guideline, and then to build a solution and measure the circuit's performance. If the measured performance deviates from the design guidelines, substitute a bigger (or smaller) inductor, as appropriate, and repeat the measurements. In addition, do your best to minimize layout parasitics, which can have a significant effect on circuit performance.

The inductor currents for a positive-to-negative converter are calculated at full load current and minimum input voltage. The peak inductor currents can be significantly higher than the output current, especially with smaller inductors and lighter loads. The following formulae assume uncoupled inductors and CCM operation.

$$I_{L1(PEAK)} = -\left(1+\frac{\chi}{2}\right)\bullet I_{O(MAX)}\bullet\frac{D_{MAX}}{1-D_{MAX}}$$

$$I_{L2(PEAK)} = -\left(1+\frac{\chi}{2}\right)\bullet I_{O(MAX)}$$

where "χ" represents the percentage of ripple current. In a positive-to-negative converter, however, the switch current is the sum of the two inductor currents. Therefore,

$$I_{SW(PEAK)} = -\left(1+\frac{\chi}{2}\right)\bullet I_{O(MAX)}\bullet\frac{1}{1-D_{MAX}}$$

Since the control loop is looking at the switch current, and since the internal slope compensation is acting on this switch current, the ripple current percentage should be between 20% and 40% of the maximum average current at $V_{IN(MIN)}$ and $I_{O(MAX)}$. This corresponds to a value of "χ" in the equations above between 0.20 and 0.40. Expressing this ripple current as a function of the output current results in the following equation for calculating the inductor value:

$$L1 = L2 = \frac{V_{IN(MIN)}}{\Delta I_{SW}\bullet f}\bullet D_{MAX}$$

where:

$$\Delta I_{SW} = -\chi\bullet I_{O(MAX)}\bullet\frac{1}{1-D_{MAX}}$$

By using a coupled inductor with a 1:1 turns ratio, the value of inductance in the equation above can be replaced by 2L due to mutual inductance. Doing this maintains the same total ripple current and energy storage in the inductor. Substituting 2L yields the following equation for 1:1 coupled inductors:

$$L1 = L2 = \frac{V_{IN(MIN)}}{2\bullet\Delta I_L\bullet f}\bullet D_{MAX}$$

For the case of uncoupled inductors, choose minimum saturation currents based on the peak currents outlined in

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the initial equations for $I_{L1(PEAK)}$ and $I_{L2(PEAK)}$. If a coupled inductor is used, make sure that the minimum saturation current for the parallel configuration exceeds the maximum switch current, or:

$$I_{LSAT(MIN)} \geq -\left(1+\frac{\chi}{2}\right)\bullet I_{O(MAX)} \bullet \frac{1}{1-D_{MAX}}$$

The saturation current rating should be checked at minimum input voltage (which results in the highest average inductor current) and maximum load current.

Operating in Discontinuous Mode

Discontinuous mode operation occurs when the load current is low enough to allow the inductor current to run out during the off-time of the switch, as shown in Figure 10. Once the inductor current is near zero, the switch and diode capacitances resonate with the inductance to form damped ringing at 1MHz to 10MHz. If the off-time is long enough, the drain voltage will settle to the input voltage.

Depending on the input voltage and the residual energy in the inductor, this ringing can cause the drain of the power MOSFET to go below ground where it is clamped by the body diode. This ringing is not harmful to the IC and it has not been shown to contribute significantly to EMI. Any attempt to damp it with a snubber will degrade the efficiency.

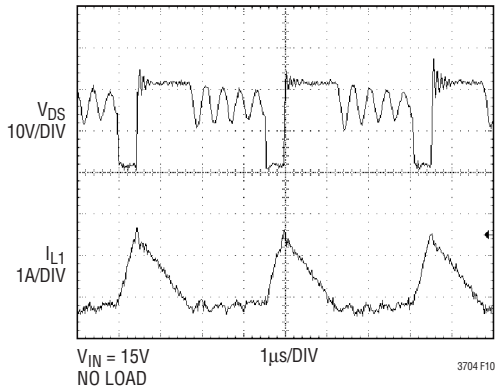

Figure 10. Discontinuous Mode Waveforms (MODE/SYNC = INTV$_{CC}$, Pulse-Skip Mode) for the Circuit in Figure 1.

Power MOSFET or Sense Resistor Selection

If the maximum voltage on the drain of the power MOSFET (which is $V_{IN(MAX)} + V_{OUT}$, plus any transients) is less than 36V then the circuit can take advantage of the LTC3704's No R_{SENSE} technology in order to improve efficiency and eliminate the sense resistor. For higher switch voltages the SENSE pin should be connected to a resistor in the source of the power MOSFET, as shown in Figure 2. Internal leading-edge blanking is provided in the LTC3704 to eliminate the need for filtering components on the SENSE pin.

In both positive-to-negative and flyback converters the maximum switch current is equal to the input current plus the output current. As a result, the peak switch current is:

$$I_{SW(PEAK)} = -\left(1+\frac{\chi}{2}\right)\bullet I_{O(MAX)} \bullet \frac{1}{1-D_{MAX}}$$

where $I_{O(MAX)}$ is a negative number.

During the switch on-time, the control circuit limits the maximum voltage drop across the power MOSFET to 150mV (at low duty cycles). The peak switch current is therefore limited to 150mV/$R_{DS(ON)}$. The relationship between the maximum load current, the duty cycle and the $R_{DS(ON)}$ of the power MOSFET is:

$$R_{DS(ON)} \leq \frac{V_{SENSE(MAX)}}{I_{SW(PEAK)}}$$

or

$$R_{DS(ON)} \leq V_{SENSE(MAX)} \bullet \frac{D_{MAX}-1}{\left(1+\frac{\chi}{2}\right)\bullet I_{O(MAX)} \bullet \rho_T}$$

again, where $I_{O(MAX)}$ is a negative number. The $V_{SENSE(MAX)}$ term is typically 150mV at low duty cycle, and is reduced to about 100mV at a duty cycle of 92% due to slope compensation, as shown in Figure 11. The ρ_T term accounts for the temperature coefficient of the $R_{DS(ON)}$ of the MOSFET, which is typically 0.4%/°C. Figure 12 illustrates the variation of $R_{DS(ON)}$ over temperature for a typical power MOSFET (normalized for simplicity).

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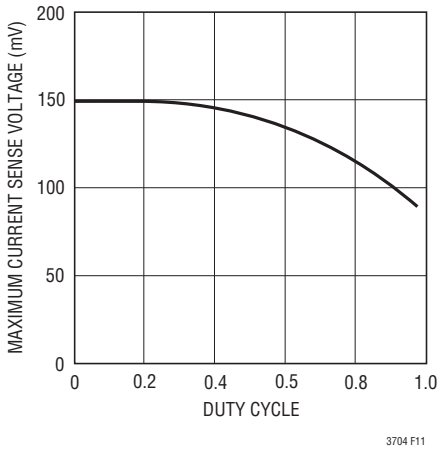

Figure 11. Maximum SENSE Threshold Voltage vs Duty Cycle

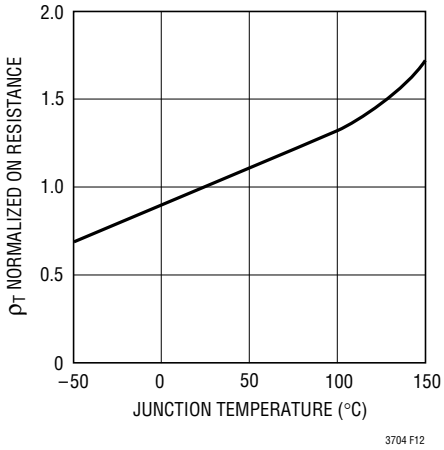

Figure 12. Normalized $R_{DS(ON)}$ vs Temperature

Another method of choosing which power MOSFET to use is to check the maximum output current for a given $R_{DS(ON)}$, since MOSFET on-resistances are generally available in discrete values.

$$I_{O(MAX)} = -V_{SENSE(MAX)} \bullet \frac{1-D_{MAX}}{\left(1+\frac{\chi}{2}\right)\bullet R_{DS(ON)} \bullet \rho_T}$$

For the case where a conventional sense resistor is used,

$$R_{SENSE} = V_{SENSE(MAX)} \bullet \frac{D_{MAX}-1}{\left(1+\frac{\chi}{2}\right)\bullet I_{O(MAX)}}$$

Sense resistors are generally low TC and are available with different ranges of tolerance depending on price. The power dissipated in the sense resistor is:

$$P_{SENSE} = I_{SW(PEAK)}^{2} \bullet R_{SENSE} \bullet D_{MAX}$$

Calculating Power MOSFET Switching and Conduction Losses and Junction Temperatures

In order to calculate the junction temperature of the power MOSFET, the power dissipated by the device must be known. This power dissipation is a function of the duty cycle, the load current and the junction temperature itself (due to the positive temperature coefficient of its $R_{DS(ON)}$).

As a result, some iterative calculation is normally required to determine a reasonably accurate value. Since the controller is using the MOSFET as both a switching and a sensing element, care should be taken to ensure that the converter is capable of delivering the required load current over all operating conditions (line voltage and temperature), and for the worst-case specifications for $V_{SENSE(MAX)}$ and the $R_{DS(ON)}$ of the MOSFET listed in the manufacturer's data sheet.

The power dissipated by the MOSFET in a positive-to-negative converter is:

$$P_{FET} = \left(\frac{-I_{O(MAX)}}{1-D_{MAX}}\right)^{2} \bullet R_{DS(ON)} \bullet D_{MAX} \bullet \rho_T + k \bullet (V_{IN} - V_O)^{1.85} \bullet \frac{I_{O(MAX)}}{1-D_{MAX}} \bullet C_{RSS} \bullet f$$

where $I_{O(MAX)}$ and V_O are negative numbers.

The first term in the equation above represents the I^2R losses in the device, and the second term, the switching losses. The constant, k = 1.7, is an empirical factor inversely related to the gate drive current and has the dimension of 1/current.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P_{FET} \bullet R_{TH(JA)}$$

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The $R_{TH(JA)}$ to be used in this equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature ($R_{TH(CA)}$). This value of T_J can then be compared to the original, assumed value used in the iterative calculation process.

Output Diode Selection

To maximize efficiency, a fast switching diode with low forward drop and low reverse leakage is desired. The output diode in a positive-to-negative converter conducts current during the switch off-time. The peak reverse voltage that the diode must withstand is equal to $V_{IN(MAX)} – V_O$. The average forward current in normal operation is equal to the output current, and the peak current is equal to the peak inductor current.

$$I_{D(PEAK)} = -\left(1+\frac{\chi}{2}\right)\bullet I_{O(MAX)}\frac{1}{1-D_{MAX}}$$

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in this equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the board to the ambient temperature in the enclosure.

Remember to keep the diode lead lengths short and to observe proper switch-node layout (see Board Layout Checklist) to avoid excessive ringing and increased dissipation.

Selecting the DC Coupling Capacitor

The voltage on the coupling capacitor in a positive-to-negative converter is $V_{IN(MAX)} – V_O$, plus any additional ΔV due to the ripple currents in the inductors. Generally, the DC coupling capacitor is dimensioned based on the high RMS ripple which flows in it, as shown in Figure 13.

The minimum RMS current rating of this capacitor must exceed:

$$I_{RMS(CAP)} = -I_{O(MAX)} \bullet \sqrt{\frac{D_{MAX}}{1-D_{MAX}}}$$

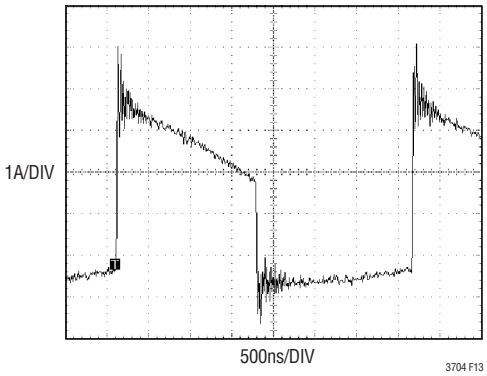

Figure 13. Ripple Current in the DC Coupling Capacitor

A low ESR and ESL, X5R- or X7R-type ceramic capacitor is recommended here.

Selecting the Output Capacitor

The output ripple voltage appears as a triangular waveform riding on V_O, due to the ripple current of L2 (the DC component of the current in L2 equals the output current). This ripple current flows through the ESR and bulk capacitance of the output capacitor to produce the overall ripple voltage on this node. Using the off-time to calculate this ripple current results in the following equation for ΔI_{L2}:

$$\Delta I_{L2} = -\frac{1-D_{MAX}}{f}\bullet\frac{V_O}{L2}$$

where V_O is a negative number. The output ripple voltage is therefore:

$$\Delta V_{O(P-P)} = \frac{1-D_{MAX}}{f}\bullet\frac{V_O}{L2}\left[-ESR-\frac{1}{8\bullet f\bullet C_O}\right]$$

The ESR can be minimized by using high quality, X5R- or X7R-dielectric ceramic capacitor in parallel with a larger value tantalum or aluminum electrolytic bulk capacitor. Depending upon the application, it may be that the ceramic capacitor alone will be sufficient.

The RMS ripple current rating of the output capacitor needs to be greater than:

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$$I_{RMS(COUT)} \geq \sqrt{\frac{1}{12} \bullet \frac{(1-D_{MAX})}{f} \bullet \frac{V_O}{L2}}$$

It should be noted that these equations assume no coupling between the inductors. If the inductors are wound on the same core, the ripple currents at the input and output can be tuned to very low values, and so the equations above would be extremely conservative. It is highly recommended that the user experiment in the lab with the same magnetics and capacitors which will be used in production.

Note that the ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be placed in parallel to meet size or height requirements in the design.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest product of ESR and size of any aluminum electrolytic, at a somewhat higher price.

In surface mount applications, multiple capacitors may have to be placed in parallel in order to meet the ESR or RMS current handling requirements of the application.

Table 1. Recommended Component Manufacturers

VENDOR	COMPONENTS	TELEPHONE	WEB ADDRESS
AVX	Capacitors	(207) 282-5111	avxcorp.com
BH Electronics	Inductors, Transformers	(952) 894-9590	bhelectronics.com
Coilcraft	Inductors	(847) 639-6400	coilcraft.com
Coiltronics	Inductors	(407) 241-7876	coiltronics.com
Diodes, Inc	Diodes	(805) 446-4800	diodes.com
Fairchild	MOSFETs	(408) 822-2126	fairchildsemi.com
General Semiconductor	Diodes	(516) 847-3000	generalsemiconductor.com
International Rectifier	MOSFETs, Diodes	(310) 322-3331	irf.com
IRC	Sense Resistors	(361) 992-7900	irctt.com
Kemet	Tantalum Capacitors	(408) 986-0424	kemet.com
Magnetics Inc	Toroid Cores	(800) 245-3984	mag-inc.com
Microsemi	Diodes	(617) 926-0404	microsemi.com
Murata-Erie	Inductors, Capacitors	(770) 436-1300	murata.co.jp
Nichicon	Capacitors	(847) 843-7500	nichicon.com
On Semiconductor	Diodes	(602) 244-6600	onsemi.com
Panasonic	Capacitors	(714) 373-7334	panasonic.com
Sanyo	Capacitors	(619) 661-6835	sanyo.co.jp
Sumida	Inductors	(847) 956-0667	sumida.com
Taiyo Yuden	Capacitors	(408) 573-4150	t-yuden.com
TDK	Capacitors, Inductors	(562) 596-1212	component.tdk.com
Thermalloy	Heat Sinks	(972) 243-4321	aavidthermalloy.com
Tokin	Capacitors	(408) 432-8020	tokin.com
Toko	Inductors	(847) 699-3430	tokoam.com
United Chemicon	Capacitors	(847) 696-2000	chemi-com.com
Vishay/Dale	Resistors	(605) 665-9301	vishay.com
Vishay/Siliconix	MOSFETs	(800) 554-5565	vishay.com
Vishay/Sprague	Capacitors	(207) 324-4140	vishay.com
Zetex	Small-Signal Discretes	(631) 543-7100	zetex.com

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Aluminum electrolytic and dry tantalum capacitors are both available in surface mount packages. In the case of tantalum, it is critical that the capacitors have been surge tested for use in switching power supplies. An excellent choice is AVX TPS series of surface mount tantalum. Also, ceramic capacitors are now available with extremely low ESR, ESL and high ripple current ratings.

Input Capacitor Selection

The input voltage source impedance determines the size of the input capacitor, which is typically in the range of 10µF to 100µF. A low ESR capacitor is recommended, although it is not as critical as for the output capacitor.

The RMS input capacitor ripple current for a positive-to-negative converter is:

$$I_{RMS(CIN)} = \sqrt{\frac{1}{12}} \bullet \frac{V_{IN(MIN)}}{L1 \bullet f} \bullet D_{MAX}$$

Please note that the input capacitor can see a very high surge current when a battery is suddenly connected to the input of the converter and solid tantalum capacitors can fail catastrophically under these conditions. **Be sure to specify surge-tested capacitors!**

Burst Mode Operation and Considerations

The choice of MOSFET $R_{DS(ON)}$ and inductor value also determines the load current at which the LTC3704 enters Burst Mode operation. When bursting, the controller clamps the peak inductor current to approximately:

$$I_{BURST(PEAK)} = \frac{30mV}{R_{DS(ON)}}$$

which represents about 20% of the maximum 150mV SENSE pin voltage. The corresponding average current depends upon the amount of ripple current. Lower inductor values (higher ΔI_L) will reduce the load current at which Burst Mode operations begins, since it is the peak current that is being clamped.

The output voltage ripple can increase during Burst Mode operation if ΔI_L is substantially less than I_{BURST}. This can occur if the input voltage is very low or if a very large inductor is chosen. At high duty cycles, a skipped cycle causes the inductor current to quickly decay to zero. However, because ΔI_L is small, it takes multiple cycles for the current to ramp back up to $I_{BURST(PEAK)}$. During this inductor charging interval, the output capacitor must supply the load current and a significant droop in the output voltage can occur. Generally, it is a good idea to choose a value of inductor ΔI_L between 20% and 40% of $I_{IN(MAX)}$. The alternative is to either increase the value of the output capacitor or disable Burst Mode operation using the MODE/SYNC pin.

Burst Mode operation can be defeated by connecting the MODE/SYNC pin to a high logic-level voltage (either with a control input or by connecting this pin to $INTV_{CC}$). In this mode, the burst clamp is removed, and the chip can operate at constant frequency from continuous conduction mode (CCM) at full load, down into deep discontinuous conduction mode (DCM) at light load. Prior to skipping pulses at very light load (i.e., <5-10% of full load), the controller will operate with a minimum switch on-time in DCM. Pulse skipping prevents a loss of control of the output at very light loads and reduces output voltage ripple.

Checking Transient Response

The regulator loop response can be verified by looking at the load transient response. Switching regulators generally take several cycles to respond to an instantaneous step in resistive load current. When the load step occurs, V_O immediately shifts by an amount equal to $(\Delta I_{LOAD})(ESR)$, and then C_O begins to charge or discharge (depending on the direction of the load step) as shown in Figure 14. The

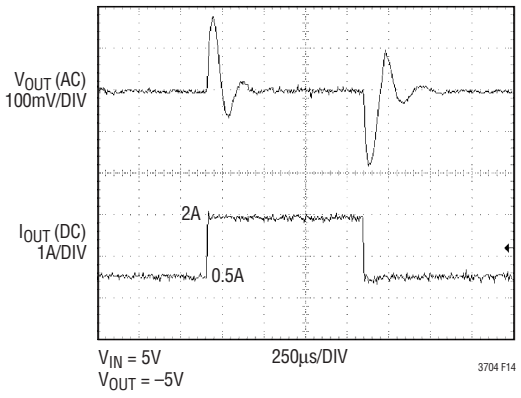

Figure 14. Load Step Response for the Circuit in Figure 1.

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regulator feedback loop acts on the resulting error amp output signal to return V_O to its steady-state value. During this recovery time, V_O can be monitored for overshoot or ringing that would indicate a stability problem.

A second, more severe transient can occur when connecting loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_O, causing a nearly instantaneous drop in V_O. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive in order to limit the inrush current di/dt to the load.

Design Example: A 5V to 15V Input, –5V at 2A Output Positive-to-Negative Converter

The design example presented here will be for the circuit shown in Figure 1. The input voltage range is 5V to 15V, and the output is -5V. The maximum load current is 2A at an input voltage of 5V (3A peak), and 3A at an input voltage of 15V (5A peak).

1. The maximum duty cycle of the main switch is:

$$D_{MAX} = \frac{V_{OUT}}{V_{OUT} - V_{IN(MIN)}} = \frac{-5}{-10} = 50\%$$

2. Pulse-Skip operation is chosen, so the MODE/SYNC pin is connected to the $INTV_{CC}$ pin.

3. The operating frequency is chosen to be 300kHz to reduce the size of the inductors. From Figure 5, the resistor from the FREQ pin to ground is 80.6k.

4. A total inductor ripple current of 40% of the maximum is chosen, so the inductor ripple current is:

$$\Delta I_{L1} = -\chi \bullet I_{O(MAX)} \bullet \frac{D_{MAX}}{1 - D_{MAX}}$$

$$\Delta I_{L1} = 0.4 \bullet 2.0 \bullet \frac{0.5}{1 - 0.5} = 0.8A$$

For a standard 1:1 coupled inductor, the inductance is therefore:

$$L1 = L2 = \frac{V_{IN(MIN)}}{2 \bullet \Delta I_{L1} \bullet f} \bullet D_{MAX}$$

$$= \frac{5}{2 \bullet 0.8 \bullet 300k} \bullet 0.5 = 5.2\mu H$$

The minimum saturation current for this inductor is:

$$I_{LSAT(MIN)} \geq -\left(1 + \frac{\chi}{2}\right) \bullet I_{O(MAX)} \bullet \frac{1}{1 - D_{MAX}}$$

$$= 1.2 \bullet 2.0 \bullet \frac{1}{1 - 0.5} = 4.8A$$

The inductor chosen is a BH Electronics part # 510-1009, which has an open circuit parallel inductance of 4.56µH and a maximum dc current rating of 6.5A.

5. For the power MOSFET,

$$R_{DS(ON)} \leq V_{SENSE(MAX)} \bullet \frac{D_{MAX} - 1}{\left(1 + \frac{\chi}{2}\right) \bullet I_{O(MAX)} \bullet \rho_T}$$

At the maximum duty cycle of 50%, the maximum SENSE pin voltage is reduced to 130mV due to slope compensation, as shown in Figure 11. Assuming a maximum junction temperature of 125°C for the power MOSFET, ρ_T = 1.5, and

$$R_{DS(ON)} \leq 0.130 \bullet \frac{0.5 - 1}{-1.2 \bullet 2.0 \bullet 1.5} = 18.1m\Omega$$

The MOSFET chosen was Siliconix/Vishay's Si4884, which has a maximum $R_{DS(ON)}$ = 16.5mΩ at V_{GS} = 4.5V at 25°C. The minimum BV_{DSS} = 30V and the maximum gate charge is Q_G = 20nC.

6. The output diode must withstand a reverse voltage of $V_{IN(MAX)} - V_O$ = 20V and a continuous current of $I_{O(MAX)}$ = 5.0A (peak output current at V_{IN} = 15V). The peak current in the diode is:

$$I_{D(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet I_{O(MAX)} = 6A$$

The power dissipated in this diode at full load is:

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$$P_D = I_{O(MAX)} \bullet V_F$$

Assuming a maximum junction temperature of 125°C and a forward voltage of approximately 0.33V at 3A (the maximum output current at V_{IN} = 15V), this diode will dissipate 1W at full load. The diode selected was the MBRD835L from On Semiconductor, packaged in a D-Pak.

7. The DC coupling capacitor must be capable of handling an RMS current of:

$$I_{D(PEAK)} = -I_{O(MAX)} \bullet \sqrt{\frac{D_{MAX}}{1-D_{MAX}}} = 3A$$

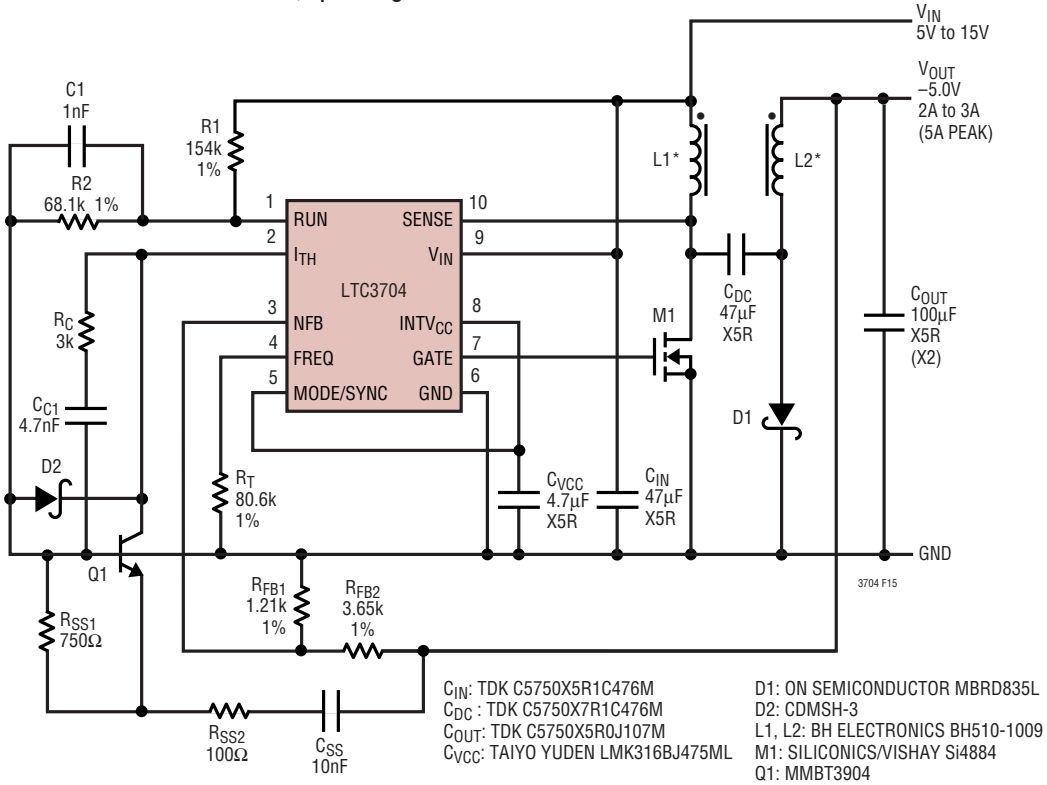

Figure 15. 5V to 15V Input, –5V Output at 2A-3A(5A Peak) Positive-to-Negative Converter with Soft-Start and Undervoltage Lockout.

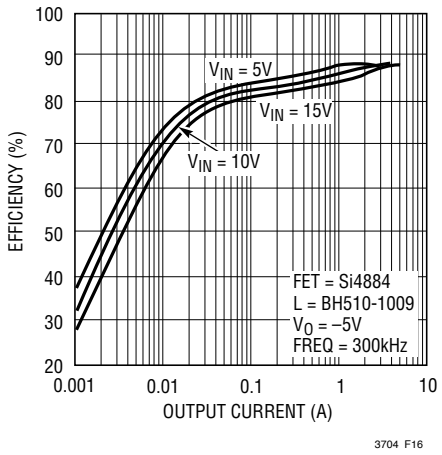

Figure 16. Efficiency vs Output Current

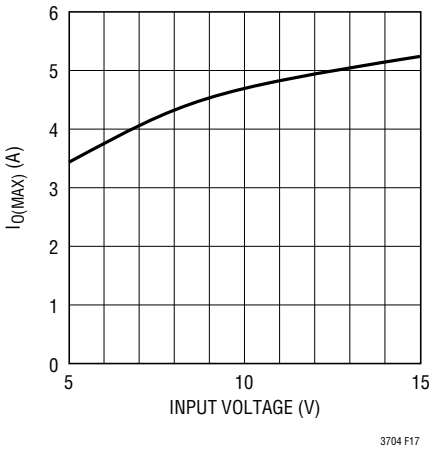

Figure 17. Maximum Output Current vs Input Voltage

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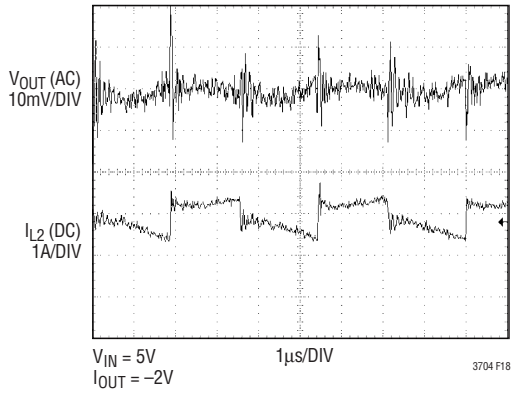

Figure 18. Output Ripple Voltage and Inductor Current for the Circuit in Figure 15

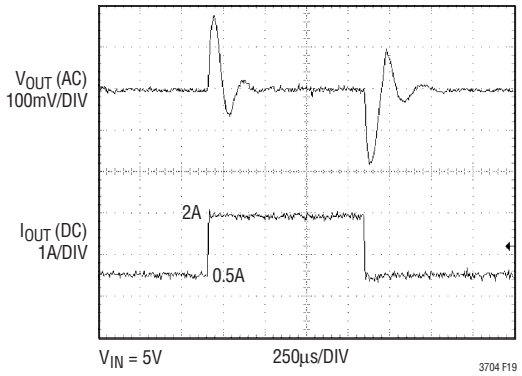

Figure 19. Load Step Response at V_{IN} = 5V for the Circuit in Figure 15

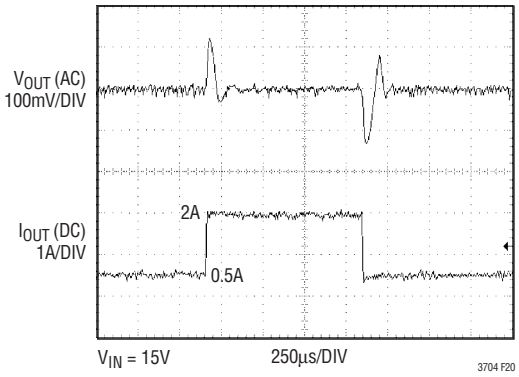

Figure 20. Load Step Response at V_{IN} = 15V for the Circuit in Figure 15

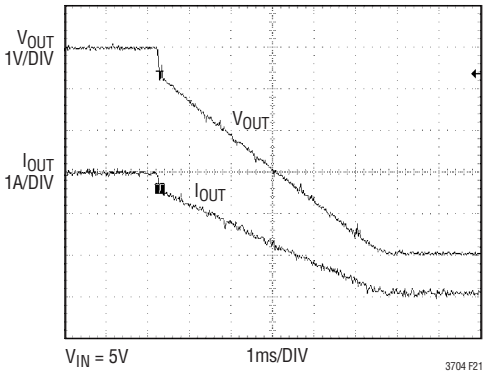

Figure 21. Soft-Start for the Circuit in Figure 15

The capacitor used was a TDK 47µF, 16V X5R-dielectric ceramic (C5750X5R1C476M), mainly because of its low ESR (2.4mΩ) and high RMS current capability.

8. The peak-to-peak output ripple is:

$$\Delta V_{O(P-P)} = \frac{1-D_{MAX}}{f} \bullet \frac{V_O}{L2} \left[-ESR - \frac{1}{8 \bullet f \bullet C_O}\right]$$

As a first try, a TDK 100µF, 6.3V X5R-dielectric ceramic capacitor was chosen (C5750X5R0J107M). This capacitor has a very low 1.6mΩ of ESR. As a result, the peak-to-peak output ripple voltage is:

$$\Delta V_{O(P-P)} = \frac{1-0.5}{300k} \bullet \frac{5.0}{3.5\mu} \left[-0.0016 - \frac{1}{8 \bullet 300k \bullet 100\mu}\right] = 13.7mV$$

This ripple voltage calculation also assumes no coupling between the inductors, making the 13.7mV number very conservative.

Figure 15 illustrates the same basic application shown in Figure 1, with the added features of soft-start and undervoltage lockout on the input supply. Figures 16 through 21 illustrate the measured performance for this converter. The peak efficiency is 87% at a load current of 2A and the peak-to-peak output ripple is less than 10mV. Figures 19 and 20 illustrate the load step response at 5V and 15V input, and Figure 21, the start-up characteristics with a resistive load.

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PC Board Layout Checklist

1. In order to minimize switching noise and improve output load regulation, the GND pin of the LTC3704 should be connected directly to 1) the negative terminal of the INTV$_{CC}$ decoupling capacitor, 2) the negative terminal of the output decoupling capacitors, 3) the source of the power MOSFET or the bottom terminal of the sense resistor, 4) the negative terminal of the input capacitor and 5) at least one via to the ground plane immediately adjacent to Pin 6. The ground trace on the top layer of the PC board should be as wide and short as possible to minimize series resistance and inductance.

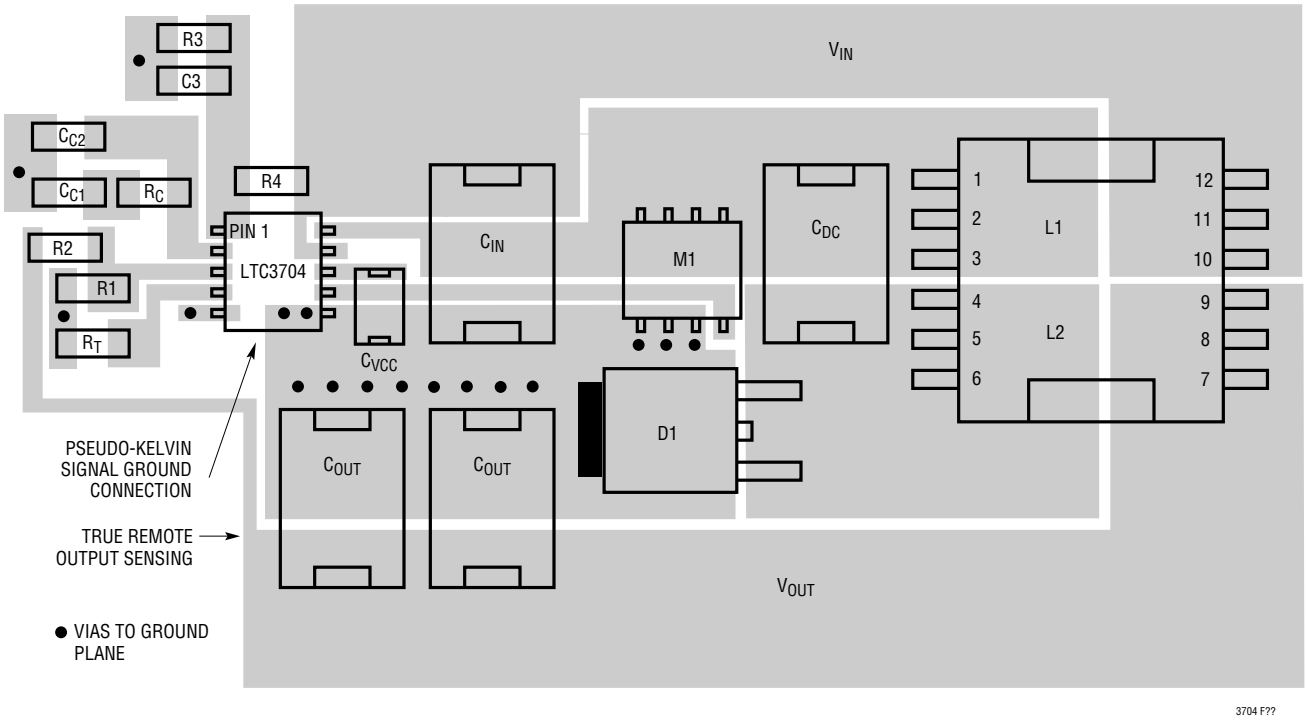
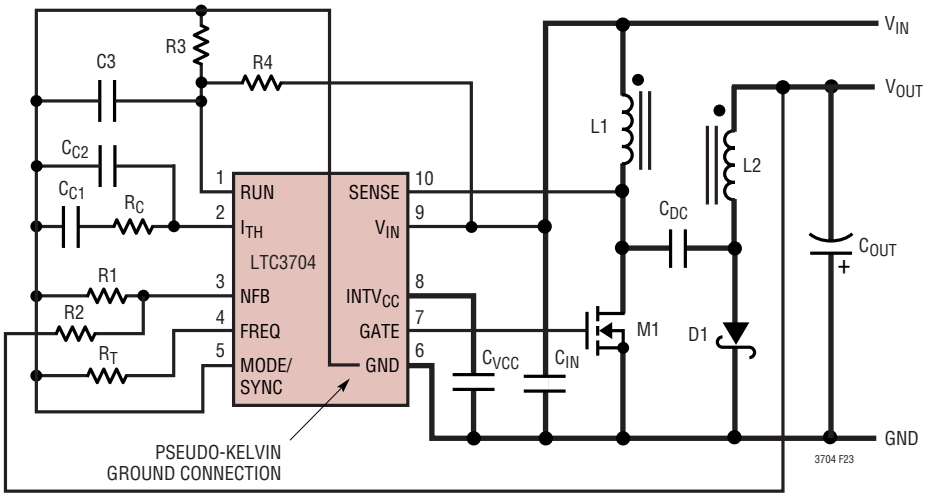


Figure 22. LTC3704 Positive-to-Negative Converter Suggested Layout



BOLD LINES INDICATE HIGH CURRENT PATHS

Figure 23. LTC3704 Positive-to-Negative Converter Layout Diagram

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2. Beware of ground loops in multiple layer PC boards. Try to maintain one central ground node on the board and use the input capacitor to avoid excess input ripple for high output current power supplies. If the ground plane is to be used for high DC currents, choose a path away from the small-signal components.

3. Place the C_{VCC} capacitor immediately adjacent to the $INTV_{CC}$ and GND pins on the IC package. This capacitor carries high di/dt MOSFET gate drive currents. A low ESR X5R-dielectric 4.7µF ceramic capacitor works well here.

4. The high di/dt loop from the drain of the power MOSFET, through the coupling capacitor and back through the diode to ground should be kept as tight as possible to reduce inductive ringing. Excess inductance can cause increased stress on the power MOSFET and increase HF noise on the drain node. It is also important to keep the cathode of the diode as close as possible to the MOSFET source or the bottom of the sense resistor.

5. Check the stress on the power MOSFET by measuring its drain-to-source voltage directly across the device terminals (reference the ground of a single scope probe directly to the source pad on the PC board). Beware of inductive ringing which can exceed the maximum specified voltage rating of the MOSFET. If this ringing cannot be avoided and exceeds the maximum rating of the device, either choose a higher voltage device or specify an avalanche-rated power MOSFET. Not all MOSFETs are created equal (some are more equal than others).

6. Place the small-signal components away from high frequency switching nodes. In the layout shown in Figure 22, all of the small-signal components have been placed on one side of the IC and all of the power components have been placed on the other. This also allows the use of a pseudo-Kelvin connection for the signal ground, where high di/dt gate driver currents flow out of the IC ground pin in one direction (to the bottom plate of the $INTV_{CC}$ decoupling capacitor) and small-signal currents flow in the other direction.

7. If a sense resistor is used in the source of the power MOSFET, minimize the capacitance between the SENSE pin trace and any high frequency switching nodes. The LTC3704 contains an internal leading edge blanking time of approximately 180ns, which should be adequate for most applications.

8. For optimum load regulation and true remote sensing, the top of the output resistor divider should connect independently to the top of the output capacitor (Kelvin connection), staying away from any high dV/dt traces. Place the divider resistors near the LTC3704 in order to keep the high impedance FB node short.

9. For applications with multiple switching power converters connected to the same input supply, make sure that the input filter capacitor for the LTC3704 is not shared with other converters. AC input current from another converter could cause substantial input voltage ripple, and this could interfere with the operation of the LTC3704. A few inches of PC trace or wire ($L \approx 100nH$) between the C_{IN} of the LTC3704 and the actual source V_{IN} should be sufficient to prevent current sharing problems.

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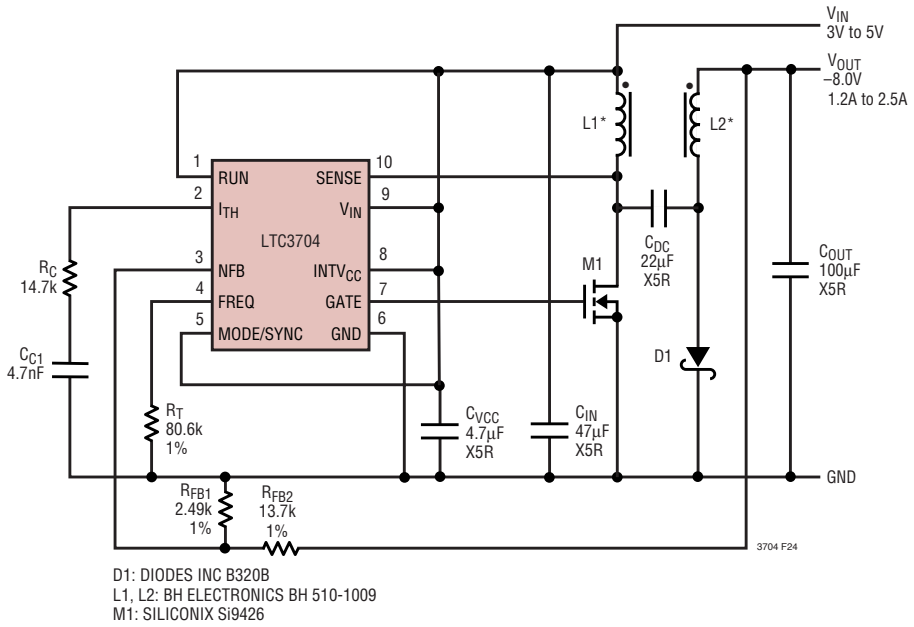

D1: DIODES INC B320B
L1, L2: BH ELECTRONICS BH 510-1009
M1: SILICONIX Si9426

Figure 24. 3V to 5V Input, –8V at 1.2A Output Converter

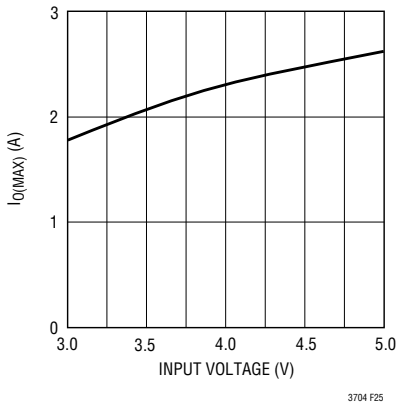

Figure 25. Maximum Output Current vs Input Voltage

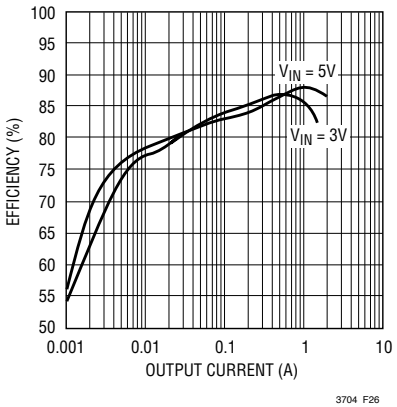

Figure 26. Output Efficiency at 3V and 5V Input

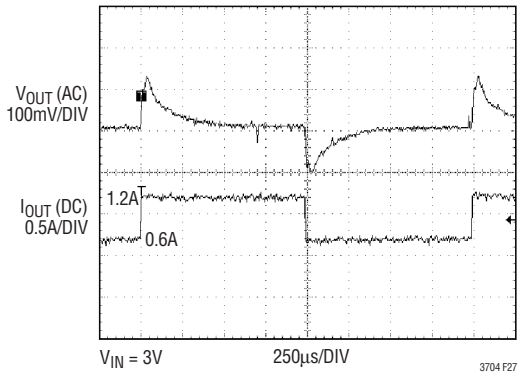

Figure 27. Load Step Response at 3V Input

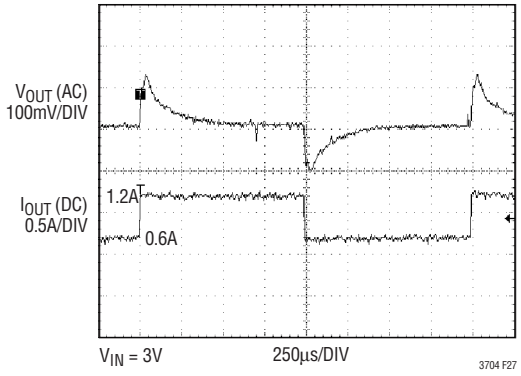

Figure 28.Load Step Response at 5V Input

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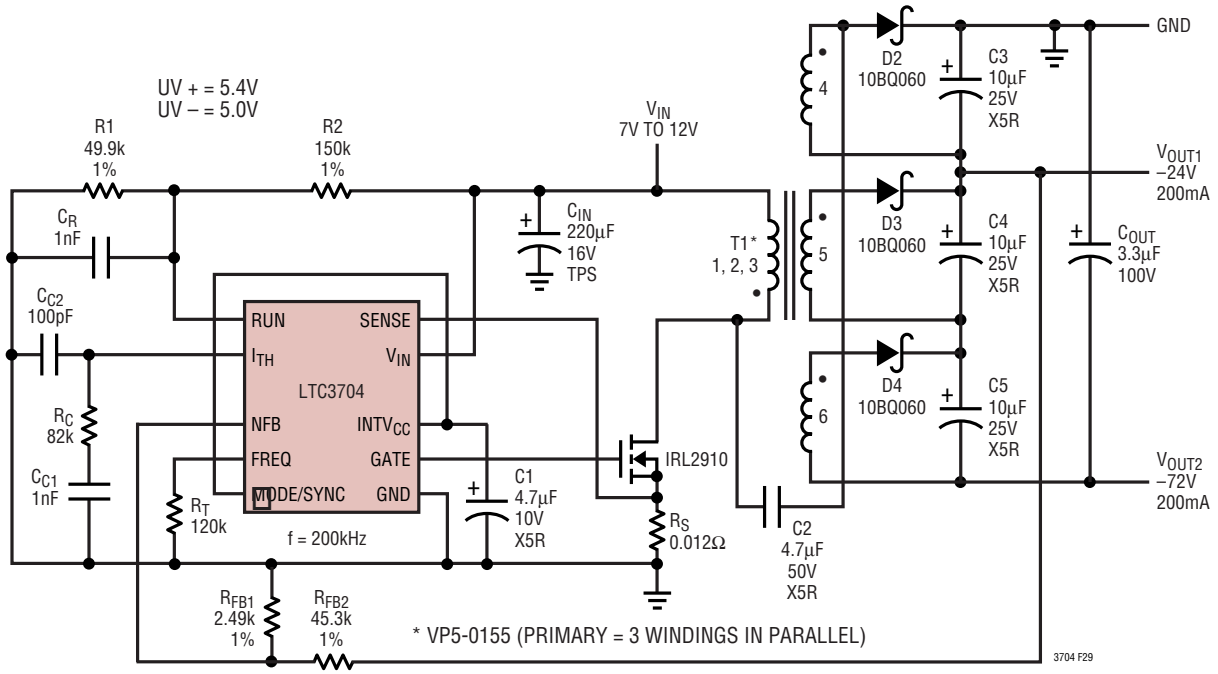
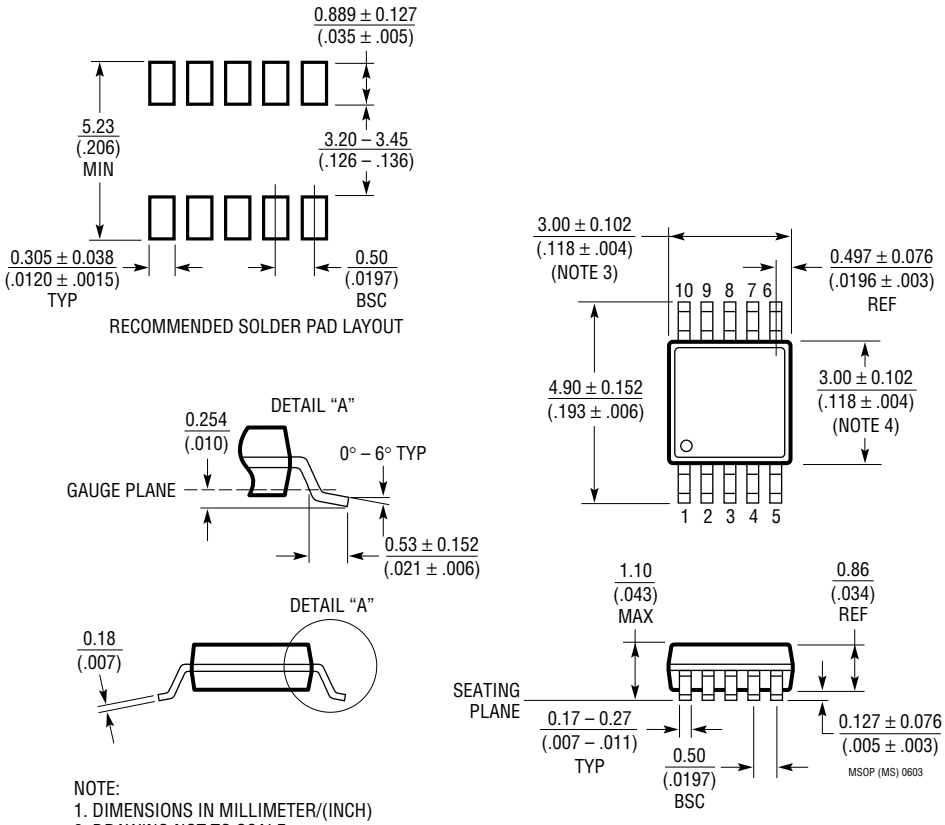


Figure 29. High Power SLIC Supply

PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX