# 3A, 800kHz Step-Up Switching Regulator

## FEATURES

- **Constant 800kHz Switching Frequency**
- **Wide Operating Voltage Range: 3V to 25V**
- **High Efficiency 0.1Ω/3A Switch**
- **1.2V Feedback Reference Voltage**
- **±2% Overall Output Voltage Tolerance**
- Uses Low Profile Surface Mount External Components
- Low Shutdown Current: 11µA
- Synchronizable from 1MHz to 1.4MHz
- Current-Mode Control
- Constant Maximum Switch Current Rating at All Duty Cycles*
- Available in a Small Thermally Enhanced TSSOP-16 Package

## APPLICATIONS

- DSL Modems
- Portable Computers
- Battery-Powered Systems
- Distributed Power

## DESCRIPTION

The LT®3436 is an 800kHz monolithic boost switching regulator. A high efficiency 3A, 0.1Ω switch is included on the die together with all the control circuitry required to complete a high frequency, current-mode switching regulator. Current-mode control provides fast transient response and excellent loop stability.

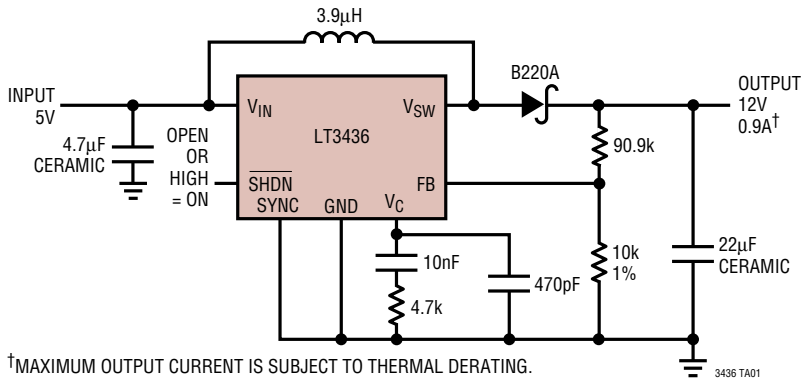
New design techniques achieve high efficiency at high switching frequencies over a wide operating range. A low dropout internal regulator maintains consistent performance over a wide range of inputs from 24V systems to Li-Ion batteries. An operating supply current of 1mA maintains high efficiency, especially at lower output currents. Shutdown reduces quiescent current to 11µA. Maximum switch current remains constant at all duty cycles. Synchronization capability allows an external logic level signal to increase the internal oscillator from 1MHz to 1.4MHz.

Full cycle-by-cycle switch current limit protection and thermal shutdown are provided. High frequency operation allows the reduction of input and output filtering components and permits the use of tiny chip inductors. The LT3436 is available in an exposed pad, 16-pin TSSOP package.



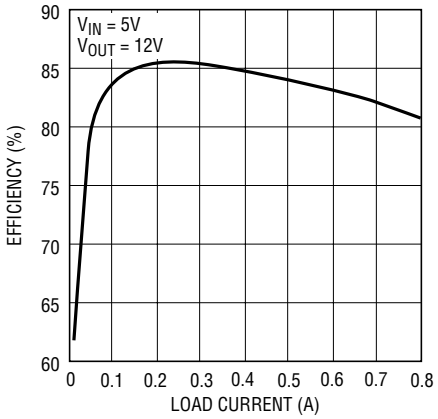
## TYPICAL APPLICATION

**5V to 12V Boost Converter**




†MAXIMUM OUTPUT CURRENT IS SUBJECT TO THERMAL DERATING.

**Efficiency vs Load Current**

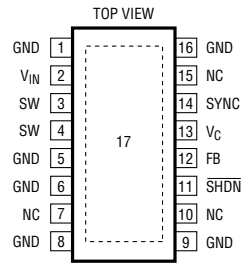


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Input Voltage ..... 25V
Switch Voltage ..... 35V
$\overline{SHDN}$ Pin ..... 25V
FB Pin Current ..... 1mA
SYNC Pin Current ..... 1mA
Operating Junction Temperature Range (Note 2)
LT3436E ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

## PACKAGE/ORDER INFORMATION




FE PACKAGE
16-LEAD PLASTIC TSSOP
EXPOSED PAD IS GND (PIN 17),
MUST BE SOLDERED TO PCB

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 45°C/W,
$\theta_{JC(PAD)}$ = 10°C/W

| ORDER PART NUMBER |
|---|
| LT3436EFE |
| **FE PART MARKING** |
| 3436EFE |

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 15V, $V_C$ = 0.8V, $\overline{SHDN}$, SYNC and switch open unless otherwise noted.**

| PARAMETER | CONDITION | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Recommended Operating Voltage | | ● | 3 | | 25 | V |
| Maximum Switch Current Limit | | ● | 3 | 4 | 6 | A |
| Oscillator Frequency | 3.3V < $V_{IN}$ < 25V | ● | 640 | 800 | 960 | kHz |
| Switch On Voltage Drop | $I_{SW}$ = 3A | ● | | 330 | 550 | mV |
| $V_{IN}$ Undervoltage Lockout | (Note 3) | ● | 2.47 | 2.6 | 2.73 | V |
| $V_{IN}$ Supply Current | $I_{SW}$ = 0A | ● | | 1 | 1.3 | mA |
| $V_{IN}$ Supply Current/$I_{SW}$ | $I_{SW}$ = 3A | | | 15 | | mA/A |
| Shutdown Supply Current | $V_{\overline{SHDN}}$ = 0V, $V_{IN}$ = 25V, $V_{SW}$ = 25V | <br>● | | 11 | 25<br>45 | µA<br>µA |
| Feedback Voltage | 3V < $V_{IN}$ < 25V, 0.4V < $V_C$ < 0.9V | <br>● | 1.182<br>1.176 | 1.2 | 1.218<br>1.224 | V<br>V |
| FB Input Current | | ● | 0 | –0.2 | –0.4 | µA |
| FB to $V_C$ Voltage Gain | 0.4V < $V_C$ < 0.9V | | 150 | 350 | | |
| FB to $V_C$ Transconductance | $\Delta I_{VC}$ = ±10µA | ● | 500 | 850 | 1300 | µMho |
| $V_C$ Pin Source Current | $V_{FB}$ = 1V | ● | –85 | –120 | –165 | µA |
| $V_C$ Pin Sink Current | $V_{FB}$ = 1.4V | ● | 70 | 110 | 165 | µA |
| $V_C$ Pin to Switch Current Transconductance | | | | 4.8 | | A/V |
| $V_C$ Pin Minimum Switching Threshold | Duty Cycle = 0% | | | 0.3 | | V |
| $V_C$ Pin 3A $I_{SW}$ Threshold | | | | 0.9 | | V |
| Maximum Switch Duty Cycle | $V_C$ = 1.2V, $I_{SW}$ = 350mA<br>$V_C$ = 1.2V, $I_{SW}$ = 1A | <br>● | 85<br>80 | 90 | | %<br>% |
| $\overline{SHDN}$ Threshold Voltage | | ● | 1.28 | 1.35 | 1.42 | V |
| $\overline{SHDN}$ Input Current (Shutting Down) | $\overline{SHDN}$ = 60mV Above Threshold | ● | –7 | –10 | –13 | µA |
| $\overline{SHDN}$ Threshold Current Hysteresis | $\overline{SHDN}$ = 100mV Below Threshold | | 4 | 7 | 10 | µA |
| SYNC Threshold Voltage | | | | 1.5 | 2.2 | V |
| SYNC Input Frequency | | | 1 | | 1.4 | MHz |
| SYNC Pin Resistance | $I_{SYNC}$ = 1mA | | | 20 | | kΩ |

## ELECTRICAL CHARACTERISTICS

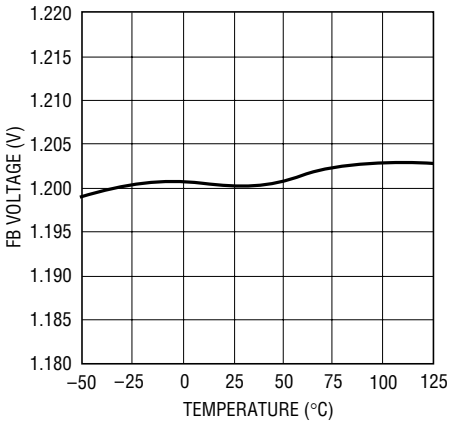
**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** The LT3436E is guaranteed to meet performance specifications from 0°C to 125°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls.

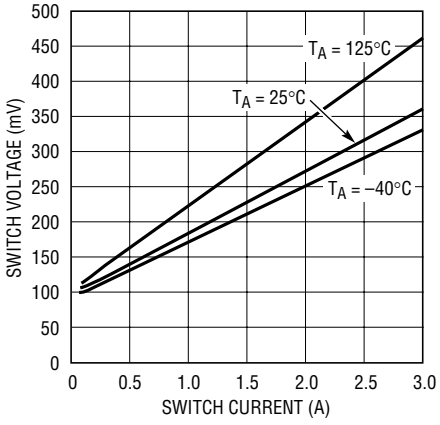
**Note 3:** Minimum input voltage is defined as the voltage where the internal regulator enters lockout. Actual minimum input voltage to maintain a regulated output will depend on output voltage and load current. See Applications Information.

## TYPICAL PERFORMANCE CHARACTERISTICS

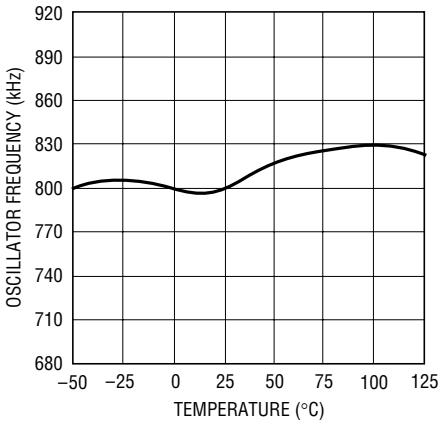
**FB Voltage**



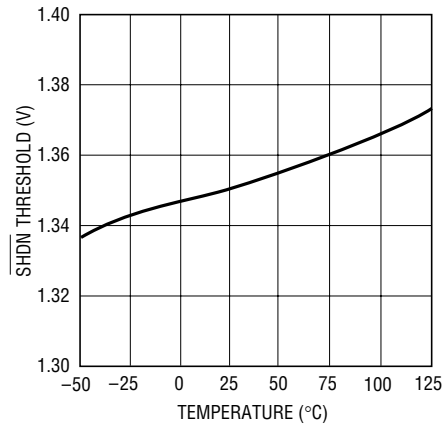

**Switch On Voltage Drop**



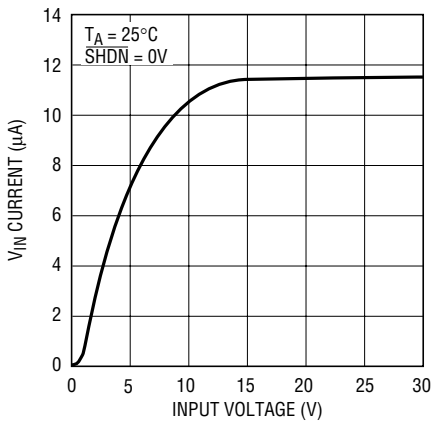

**Oscillator Frequency**



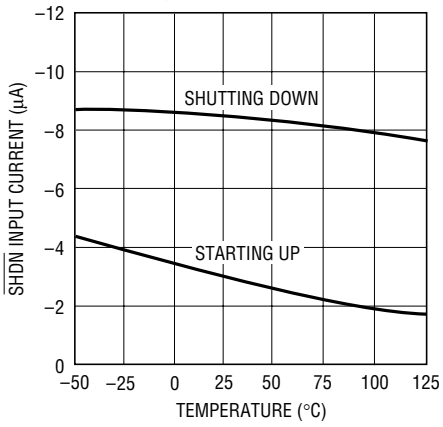

**$\overline{\text{SHDN}}$ Threshold**




**$\overline{\text{SHDN}}$ Supply Current**

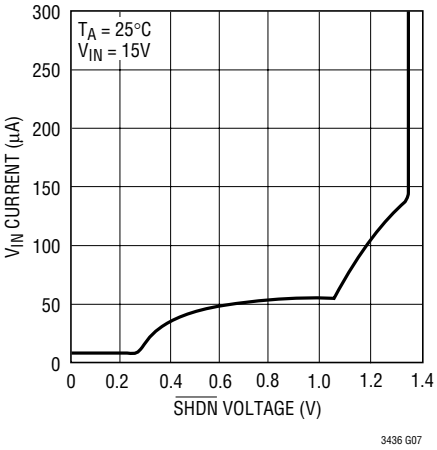



**$\overline{\text{SHDN}}$ Input Current**

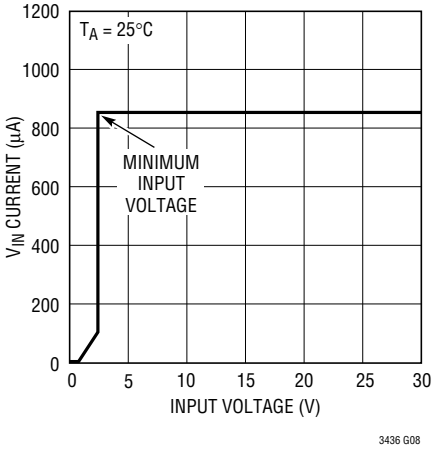


## TYPICAL PERFORMANCE CHARACTERISTICS

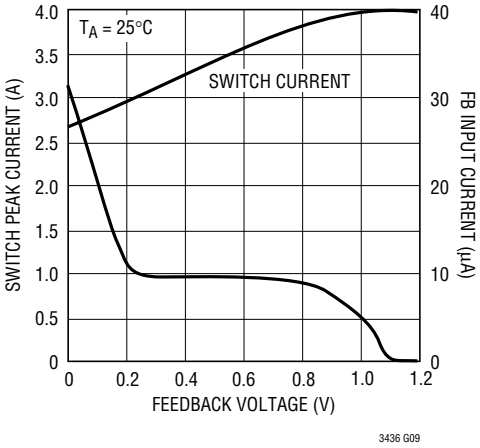
**$\overline{\text{SHDN}}$ Supply Current**




**Input Supply Current**




**Current Limit Foldback**




## PIN FUNCTIONS

**GND (Pins 1, 5, 6, 8, 9, 16, 17):** Short GND pins 1, 5, 6,8, 9, 16 and the exposed pad (pin 17) on the PCB. The GND is the reference for the regulated output, so load regulation will suffer if the "ground" end of the load is not at the same voltage as the GND of the IC. This condition occurs when the load current flows through the metal path between the GND pins and the load ground point. Keep the ground path short between the GND pins and the load and use a ground plane when possible. Keep the path between the input bypass and the GND pins short. The exposed pad should be attached to a large copper area to improve thermal performance.

**$V_{IN}$ (Pin 2):** This pin powers the internal circuitry and internal regulator. Keep the external bypass capacitor close to this pin.

**SW (Pins 3, 4):** The switch pin is the collector of the on-chip power NPN switch and has large currents flowing through it. Keep the traces to the switching components as short as possible to minimize radiation and voltage spikes.

**$\overline{\text{SHDN}}$ (Pin 11):** The shutdown pin is used to turn off the regulator and to reduce input drain current to a few microamperes. The 1.35V threshold can function as an accurate undervoltage lockout (UVLO), preventing the regulator from operating until the input voltage has reached a predetermined level. Float or pull high to put the regulator in the operating mode.

**FB (Pin 12):** The feedback pin is used to set output voltage using an external voltage divider that generates 1.2V at the pin with the desired output voltage. If required, the current limit can be reduced during start up when the FB pin is below 0.5V (see the Current Limit Foldback graph in the Typical Performance Characteristics section). An impedance of less than 5kΩ at the FB pin is needed for this feature to operate.

**$V_C$ (Pin 13):** The $V_C$ pin is the output of the error amplifier and the input of the peak switch current comparator. It is normally used for frequency compensation, but can do double duty as a current clamp or control loop override. This pin sits at about 0.3V for very light loads and 0.9V at maximum load.

**SYNC (Pin 14):** The sync pin is used to synchronize the internal oscillator to an external signal. It is directly logic compatible and can be driven with any signal between 20% and 80% duty cycle. The synchronizing range is equal to *initial* operating frequency, up to 1.4MHz. See Synchronization section in Applications Information for details. When not in use, this pin should be grounded.

## BLOCK DIAGRAM

The LT3436 is a constant frequency, current-mode boost converter. This means that there is an internal clock and two feedback loops that control the duty cycle of the power switch. In addition to the normal error amplifier, there is a current sense amplifier that monitors switch current on a cycle-by-cycle basis. A switch cycle starts with an oscillator pulse which sets the $R_S$ flip-flop to turn the switch on. When switch current reaches a level set by the inverting input of the comparator, the flip-flop is reset and the switch turns off. Output voltage control is obtained by using the output of the error amplifier to set the switch current trip point. This technique means that the error amplifier commands current to be delivered to the output rather than voltage. A voltage fed system will have low phase shift up to the resonant frequency of the inductor and output capacitor, then an abrupt 180° shift will occur. The current fed system will have 90° phase shift at a much lower frequency, but will not have the additional 90° shift until well beyond the LC resonant frequency. This makes it much easier to frequency compensate the feedback loop and also gives much quicker transient response.

A comparator connected to the shutdown pin disables the internal regulator, reducing supply current.

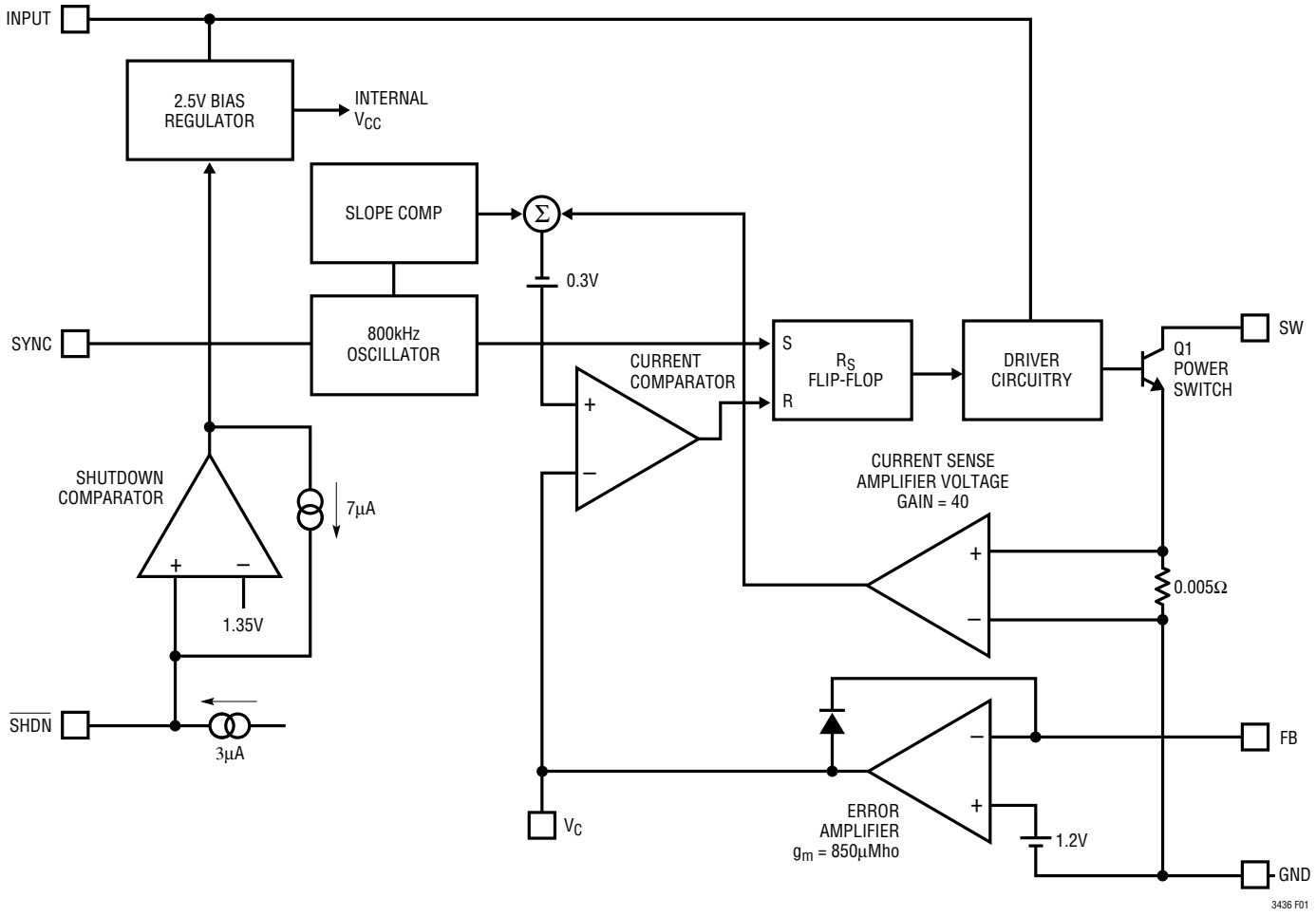



**Figure 1. Block Diagram**

## APPLICATIONS INFORMATION

### FB RESISTOR NETWORK

The suggested resistance (R2) from FB to ground is 10k 1%. This reduces the contribution of FB input bias current to output voltage to less than 0.2%. The formula for the resistor (R1) from $V_{OUT}$ to FB is:

$$R1 = \frac{R2(V_{OUT} - 1.2)}{1.2 - R2(0.2\mu A)}$$

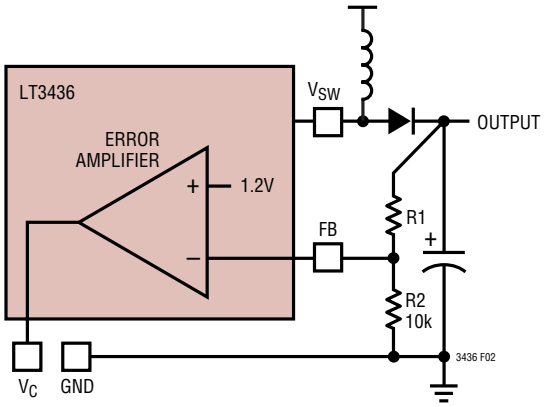



**Figure 2. Feedback Network**

### OUTPUT CAPACITOR

Step-up regulators supply current to the output in pulses. The rise and fall times of these pulses are very fast. The output capacitor is required to reduce the voltage ripple this causes. The RMS ripple current can be calculated from:

$$I_{RIPPLE(RMS)} = I_{OUT}\sqrt{(V_{OUT} - V_{IN}) / V_{IN}}$$

The LT3436 will operate with both ceramic and tantalum output capacitors. Ceramic capacitors are generally chosen for their small size, very low ESR (effective series resistance), and good high frequency operation, reducing output ripple voltage. Their low ESR removes a useful zero in the loop frequency response, common to tantalum capacitors. To compensate for this, the $V_C$ loop compensation pole frequency must typically be reduced by a factor of 10. Typical ceramic output capacitors are in the 4.7µF to 22µF range. Since the absolute value of capacitance defines the pole frequency of the output stage, an X7R or X5R type ceramic, which have good temperature stability, is recommended.

Tantalum capacitors are usually chosen for their bulk capacitance properties, useful in high transient load applications. ESR rather than absolute value defines output ripple at 800kHz. Values in the 22µF to 100µF range are generally needed to minimize ESR and meet ripple current ratings. Care should be taken to ensure the ripple ratings are not exceeded.

**Table 1. Surface Mount Solid Tantalum Capacitor ESR and Ripple Current**

| E Case Size | ESR (Max, Ω) | Ripple Current (A) |
|---|---|---|
| AVX TPS, Sprague 593D | 0.1 to 0.3 | 0.7 to 1.1 |
| **D Case Size** | | |
| AVX TPS, Sprague 593D | 0.1 to 0.3 | 0.7 to 1.1 |
| **C Case Size** | | |
| AVX TPS | 0.2 (typ) | 0.5 (typ) |

### INPUT CAPACITOR

Unlike the output capacitor, RMS ripple current in the input capacitor is normally low enough that ripple current rating is not an issue. The current waveform is triangular, with an RMS value given by:

$$I_{RIPPLE(RMS)} = \frac{0.29(V_{IN})(V_{OUT} - V_{IN})}{(L)(f)(V_{OUT})}$$

At higher switching frequency, the energy storage requirement of the input capacitor is reduced so values in the range of 2.2µF to 10µF are suitable for most applications. Y5V or similar type ceramics can be used since the absolute value of capacitance is less important and has no significant effect on loop stability. If operation is required close to the minimum input voltage required by either the output or the LT3436, a larger value may be necessary. This is to prevent excessive ripple causing dips below the minimum operating voltage resulting in erratic operation.

## APPLICATIONS INFORMATION

### INDUCTOR CHOICE AND MAXIMUM OUTPUT CURRENT

When choosing an inductor, there are 2 conditions that limit the minimum inductance; required output current, and avoidance of subharmonic oscillation. The maximum output current for the LT3436 in a standard boost converter configuration with an infinitely large inductor is:

$$I_{OUT(MAX)} = 3A\frac{V_{IN} \bullet \eta}{V_{OUT}}$$

Where $\eta$ = converter efficiency (typically 0.87 at high current).

As the value of inductance is reduced, ripple current increases and $I_{OUT(MAX)}$ is reduced. The minimum inductance for a required output current is given by:

$$L_{MIN} = \frac{V_{IN}(V_{OUT} - V_{IN})}{2V_{OUT}(f)\left(3 - \frac{(V_{OUT})(I_{OUT})}{V_{IN} \bullet \eta}\right)}$$

The second condition, avoidance of subharmonic oscillation, must be met if the operating duty cycle is greater than 50%. The slope compensation circuit within the LT3436 prevents subharmonic oscillation for inductor ripple currents of up to $1.4A_{P-P}$, defining the minimum inductor value to be:

$$L_{MIN} = \frac{V_{IN}(V_{OUT} - V_{IN})}{1.4V_{OUT}(f)}$$

These conditions define the absolute minimum inductance. However, it is generally recommended that to prevent excessive output noise, and difficulty in obtaining stability, the ripple current is no more than 40% of the average inductor current. Since inductor ripple is:

$$I_{P-P\ RIPPLE} = \frac{V_{IN}(V_{OUT} - V_{IN})}{V_{OUT}(L)(f)}$$

The recommended minimum inductance is:

$$L_{MIN} = \frac{(V_{IN})^2(V_{OUT} - V_{IN})}{0.4(V_{OUT})^2(I_{OUT})(f)}$$

The inductor value may need further adjustment for other factors such as output voltage ripple and filtering requirements. Remember also, inductance can drop significantly with DC current and manufacturing tolerance.

The inductor must have a rating greater than its peak operating current to prevent saturation resulting in efficiency loss. Peak inductor current is given by:

$$I_{LPEAK} = \frac{(V_{OUT})(I_{OUT})}{V_{IN} \bullet \eta} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2V_{OUT}(L)(f)}$$

Also, consideration should be given to the DC resistance of the inductor. Inductor resistance contributes directly to the efficiency losses in the overall converter.

Suitable inductors are available from Coilcraft, Coiltronics, Dale, Sumida, Toko, Murata, Panasonic and other manufactures.

**Table 2**

| PART NUMBER | VALUE (µH) | $I_{SAT(DC)}$ (Amps) | DCR (Ω) | HEIGHT (mm) |
|---|---|---|---|---|
| **Coilcraft** | | | | |
| DO1608C-222 | 2.2 | 2.4 | 0.07 | 2.9 |
| **Sumida** | | | | |
| CDRH3D16-1R5 | 1.5 | 1.6 | 0.043 | 1.8 |
| CDRH4D18-1R0 | 1.0 | 1.7 | 0.035 | 2.0 |
| CDC5D23-2R2 | 2.2 | 2.2 | 0.03 | 2.5 |
| CR43-1R4 | 1.4 | 2.5 | 0.056 | 3.5 |
| CDRH5D28-2R6 | 2.6 | 2.6 | 0.013 | 3.0 |
| CDRH6D38-3R3 | 3.3 | 3.5 | 0.02 | 4.0 |
| CDRH6D28-3R0 | 3.0 | 3.0 | 0.024 | 3.0 |
| **Toko** | | | | |
| (D62F)847FY-2R4M | 2.4 | 2.5 | 0.037 | 2.7 |
| (D73LF)817FY-2R2M | 2.2 | 2.7 | 0.03 | 3.0 |

## APPLICATIONS INFORMATION

### CATCH DIODE

The suggested catch diode (D1) is a B220A Schottky. It is rated at 2A average forward current and 20V reverse voltage. Typical forward voltage is 0.5V at 2A. The diode conducts current only during switch off time. Peak reverse voltage is equal to regulator output voltage. Average forward current in normal operation is equal to output current.

### SHUTDOWN AND UNDERVOLTAGE LOCKOUT

Figure 4 shows how to add undervoltage lockout (UVLO) to the LT3436. Typically, UVLO is used in situations where the input supply is *current limited*, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. UVLO prevents the regulator from operating at source voltages where these problems might occur.

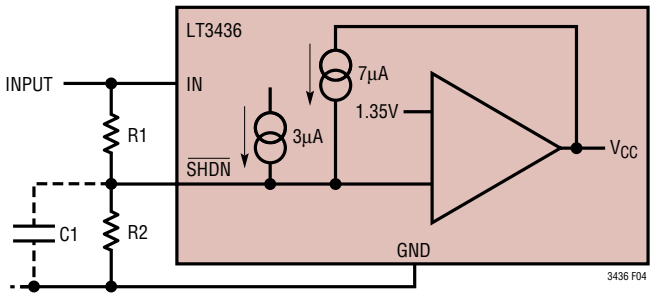



**Figure 4. Undervoltage Lockout**

An internal comparator will force the part into shutdown below the minimum $V_{IN}$ of 2.6V. This feature can be used to prevent excessive discharge of battery-operated systems. If an adjustable UVLO threshold is required, the shutdown pin can be used. The threshold voltage of the shutdown pin comparator is 1.35V. A 3µA internal current source defaults the open pin condition to be operating (see Typical Performance Graphs). Current hysteresis is added above the SHDN threshold. This can be used to set voltage hysteresis of the UVLO using the following:

$$R1 = \frac{V_H - V_L}{7\mu A}$$

$$R2 = \frac{1.35V}{\frac{(V_H - 1.35V)}{R1} + 3\mu A}$$

$V_H$ – Turn-on threshold

$V_L$ – Turn-off threshold

Example: switching should not start until the input is above 4.75V and is to stop if the input falls below 3.75V.

$V_H$ = 4.75V

$V_L$ = 3.75V

$$R1 = \frac{4.75V - 3.75V}{7\mu A} = 143k$$

$$R2 = \frac{1.35V}{\frac{(4.75V - 1.35V)}{143k} + 3\mu A} = 50.4k$$

Keep the connections from the resistors to the $\overline{SHDN}$ pin short and make sure that the interplane or surface capacitance to the switching nodes are minimized. If high resistor values are used, the $\overline{SHDN}$ pin should be bypassed with a 1nF capacitor to prevent coupling problems from the switch node.

# APPLICATIONS INFORMATION

## SYNCHRONIZATION

The SYNC pin, is used to synchronize the internal oscillator to an external signal. The SYNC input must pass from a logic level low, through the maximum synchronization threshold with a duty cycle between 20% and 80%. The input can be driven directly from a logic level output. The synchronizing range is equal to *initial* operating frequency up to 1.4MHz. This means that *minimum* practical sync frequency is equal to the worst-case *high* self-oscillating frequency (960kHz), not the typical operating frequency of 800kHz. Caution should be used when synchronizing above 1.1MHz because at higher sync frequencies the amplitude of the internal slope compensation used to prevent subharmonic switching is reduced. Higher inductor values will tend to eliminate this problem. See Frequency Compensation section for a discussion of an entirely different cause of subharmonic switching before assuming that the cause is insufficient slope compensation. Application Note 19 has more details on the theory of slope compensation.

## LAYOUT CONSIDERATIONS

As with all high frequency switchers, when considering layout, care must be taken to achieve optimal electrical, thermal and noise performance. For maximum efficiency, switch rise and fall times are typically in the nanosecond range. To prevent noise both radiated and conducted, the high speed switching current path, shown in Figure 5, must be kept as short as possible. This is implemented in the suggested layout of Figure 6. Shortening this path will also reduce the parasitic trace inductance of approximately 25nH/inch. At switch off, this parasitic inductance produces a flyback spike across the LT3436 switch. When operating at higher currents and output voltages, with poor layout, this spike can generate voltages across the LT3436 that may exceed its absolute maximum rating. A ground plane should always be used under the switcher circuitry to prevent interplane coupling and overall noise.

The $V_C$ and FB components should be kept as far away as possible from the switch node. The LT3436 pinout has been designed to aid in this. The ground for these components should be separated from the switch current path. Failure to do so will result in poor stability or subharmonic like oscillation.

Board layout also has a significant effect on thermal resistance. The exposed pad is the copper plate that runs under the LT3436 die. This is the best thermal path for heat out of the package. Soldering the pad onto the board will reduce die temperature and increase the power capability of the LT3436. Provide as much copper area as possible around this pad. Adding multiple solder filled feedthroughs under and around the pad to the ground plane will also help. Similar treatment to the catch diode and inductor terminations will reduce any additional heating effects.

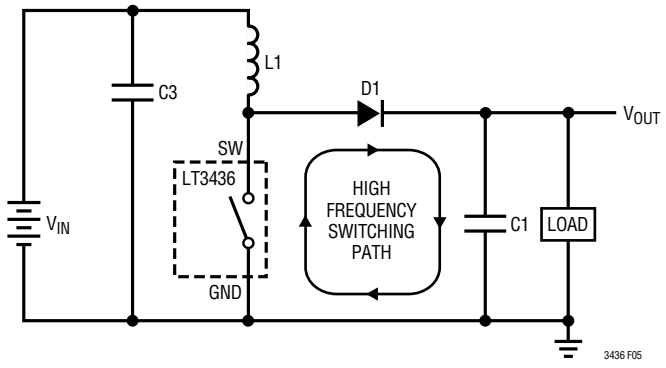
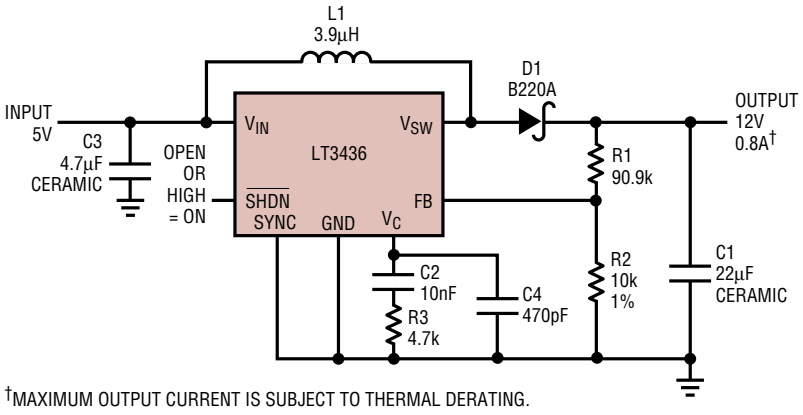



**Figure 5. High Speed Switching Path**

## APPLICATIONS INFORMATION




†MAXIMUM OUTPUT CURRENT IS SUBJECT TO THERMAL DERATING.

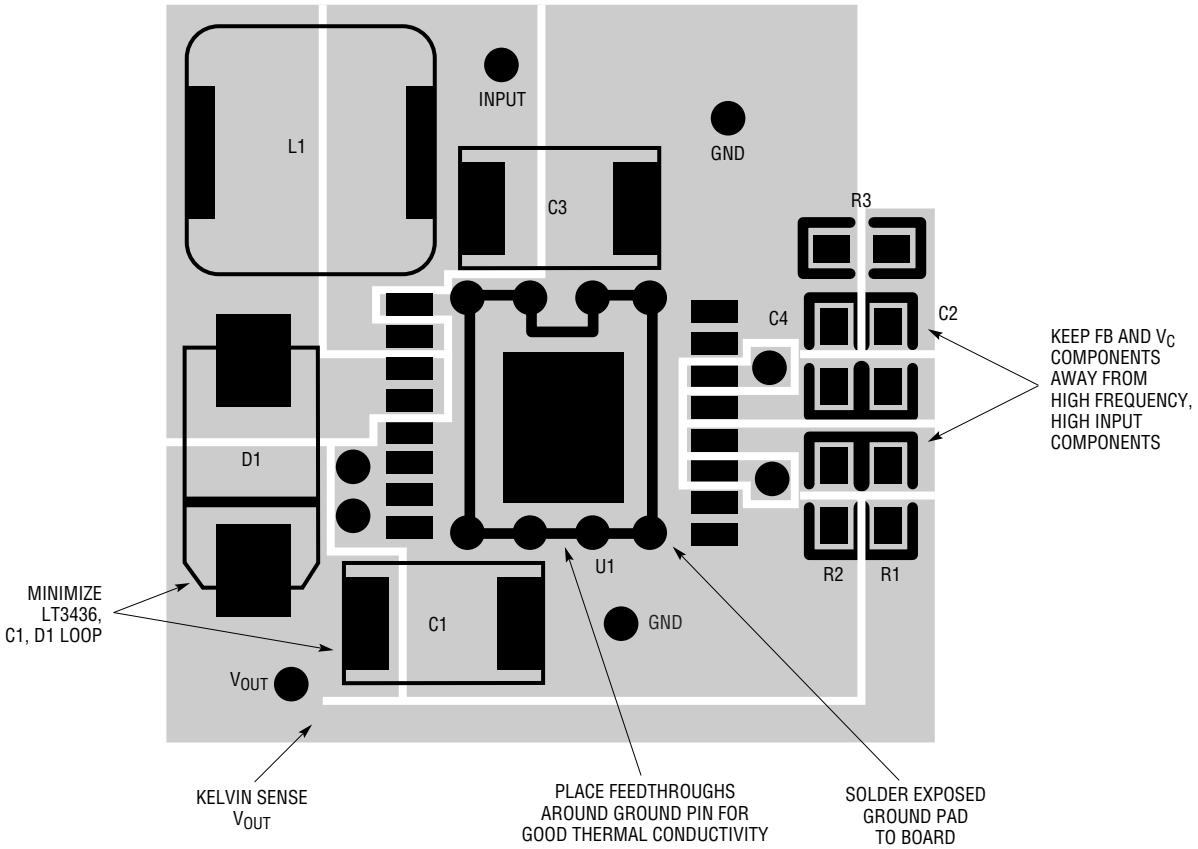



**Figure 6. Typical Application and Suggested Layout (Topside Only Shown)**

## APPLICATIONS INFORMATION

The inductor must have a rating greater than its peak operating current to prevent saturation resulting in efficiency loss. Peak inductor current is given by:

$$I_{LPEAK} = \frac{(V_{OUT})(I_{OUT})}{V_{IN} \bullet \eta} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2V_{OUT}(L)(f)}$$

Also, consideration should be given to the DC resistance of the inductor. Inductor resistance contributes directly to the efficiency losses in the overall converter.

### THERMAL CALCULATIONS

Power dissipation in the LT3436 chip comes from four sources: switch DC loss, switch AC loss, drive current, and input quiescent current. The following formulas show how to calculate each of these losses. These formulas assume continuous mode operation, so they should not be used for calculating efficiency at light load currents.

$$\text{DC, duty cycle} = \frac{(V_{OUT} - V_{IN})}{V_{OUT}}$$

$$I_{SW} = \frac{(V_{OUT})(I_{OUT})}{V_{IN}}$$

Switch loss:

$$P_{SW} = (DC)(I_{SW})^2(R_{SW}) + 17n(I_{SW})(V_{OUT})(f)$$

$V_{IN}$ loss:

$$P_{VIN} = \frac{(V_{IN})(I_{SW})(DC)}{50} + 1mA(V_{IN})$$

$R_{SW}$ = Switch resistance ($\approx$0.16$\Omega$ hot)

Example: $V_{IN}$ = 5V, $V_{OUT}$ = 12V and $I_{OUT}$ = 0.8A

Total power dissipation = 0.34 + 0.31 + 0.11 + 0.005 = 0.77W

Thermal resistance for LT3436 package is influenced by the presence of internal or backside planes. With a full plane under the package, thermal resistance will be about 40°C/W. To calculate die temperature, use the appropriate thermal resistance number and add in worst-case ambient temperature:

$$T_J = T_A + \theta_{JA}(P_{TOT})$$

If a true die temperature is required, a measurement of the SYNC to GND pin resistance can be used. The SYNC pin resistance across temperature must first be calibrated, with no device power, in an oven. The same measurement can then be used in operation to indicate the die temperature.

### FREQUENCY COMPENSATION

Loop frequency compensation is performed on the output of the error amplifier ($V_C$ pin) with a series RC network. The main pole is formed by the series capacitor and the output impedance ($\approx$500k$\Omega$) of the error amplifier. The pole falls in the range of 2Hz to 20Hz. The series resistor creates a "zero" at 1kHz to 5kHz, which improves loop stability and transient response. A second capacitor, typically one-tenth the size of the main compensation capacitor, is sometimes used to reduce the switching frequency ripple on the $V_C$ pin. $V_C$ pin ripple is caused by output voltage ripple attenuated by the output divider and multiplied by the error amplifier. Without the second capacitor, $V_C$ pin ripple is:

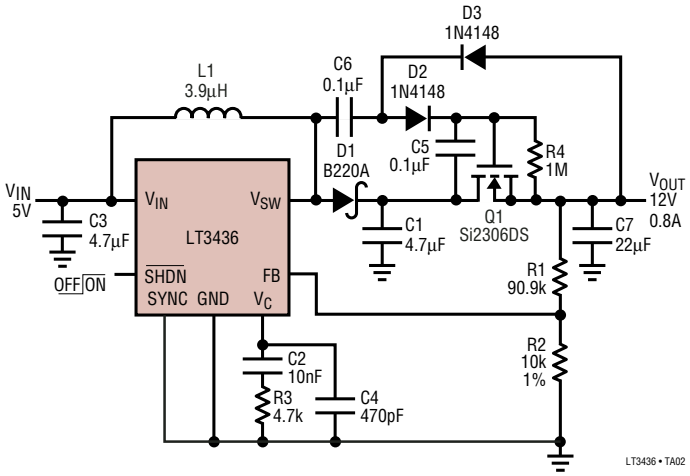
$$V_C \text{ Pin Ripple} = \frac{1.2(V_{RIPPLE})(g_m)(R_C)}{(V_{OUT})}$$

$V_{RIPPLE}$ = Output ripple ($V_{P-P}$)
$g_m$ = Error amplifier transconductance ($\approx$850$\mu$mho)
$R_C$ = Series resistor on $V_C$ pin
$V_{OUT}$ = DC output voltage

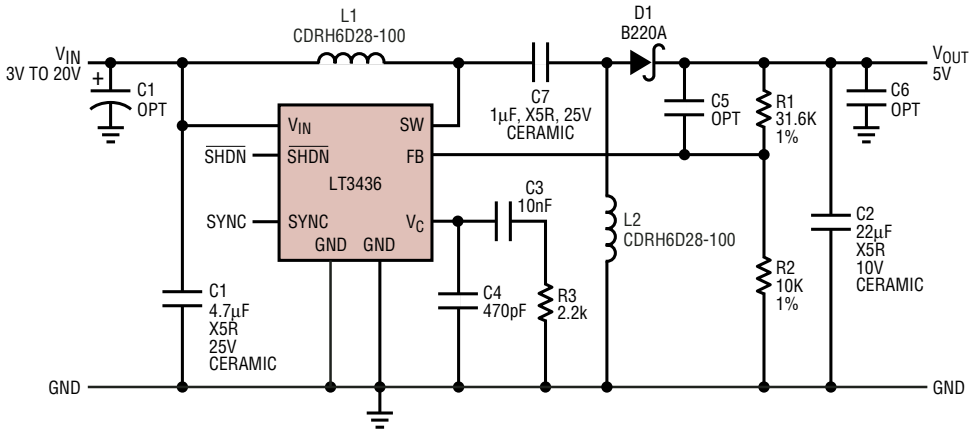
To prevent irregular switching, $V_C$ pin ripple should be kept below 50m$V_{P-P}$. Worst-case $V_C$ pin ripple occurs at maximum output load current and will also be increased if poor quality (high ESR) output capacitors are used. The addition of a 150pF capacitor on the $V_C$ pin reduces switching frequency ripple to only a few millivolts. A low value for $R_C$ will also reduce $V_C$ pin ripple, but loop phase margin may be inadequate.

## TYPICAL APPLICATIONS

### Load Disconnects in Shutdown



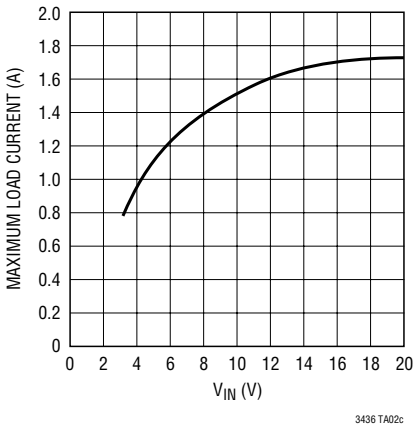

### 3V to 20$V_{IN}$ 5$V_{OUT}$ SEPIC with Either Two Inductors or a Transformer




OPTION: REPLACE L1, L2 WITH TRANSFORMER CTX5-1A, CTX8-1A, CTX10-2A

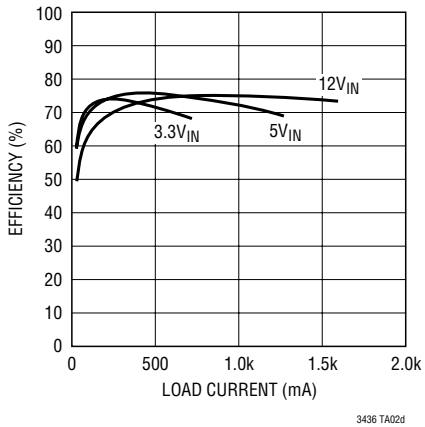
3436 TA02b

### Maximum Load Current Increases with Input Voltage




3436 TA02c

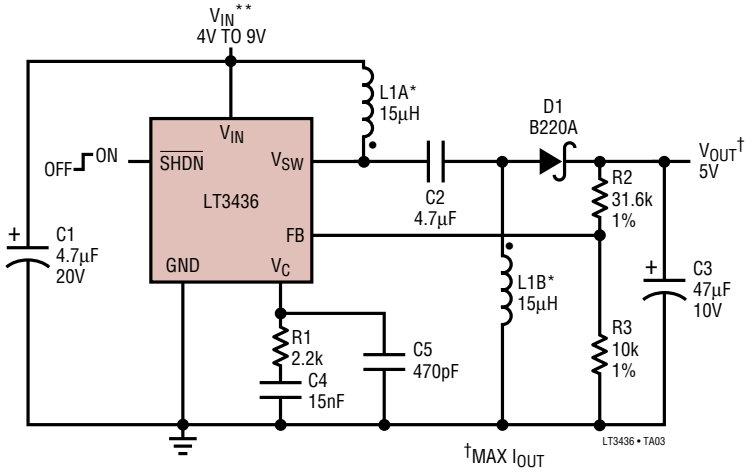
### Efficiency




3436 TA02d

## TYPICAL APPLICATIONS

### 4V-9$V_{IN}$ to 5$V_{OUT}$ SEPIC Converter**



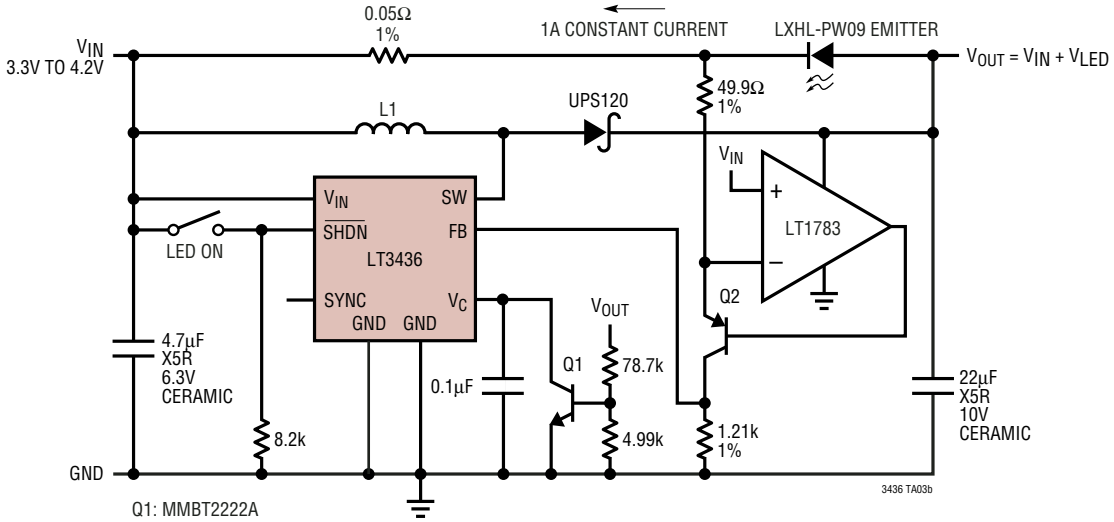

* COILTRONICS CTX15-4

** INPUT VOLTAGE MAY BE GREATER OR LESS THAN OUTPUT VOLTAGE

†MAX $I_{OUT}$

| $I_{OUT}$ | $V_{IN}$ |
|---|---|
| 0.84A | 4V |
| 1.03A | 5V |
| 1.18A | 6V |
| 1.29A | 7V |
| 1.50A | 9V |

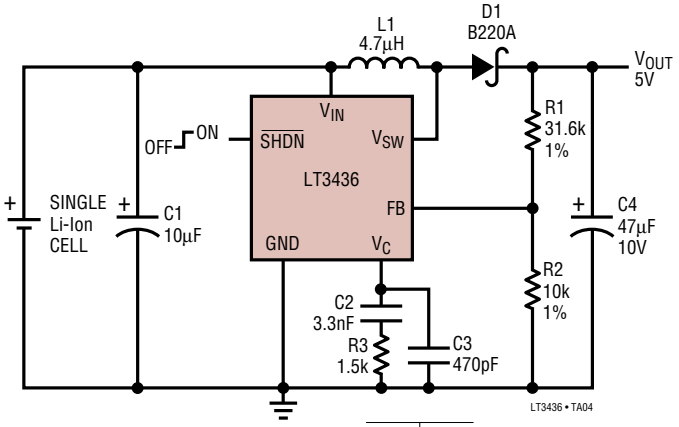
### Boost Converter Drives Luxeon III 1A 3.6V White LED with 70% Efficiency




Q1: MMBT2222A
Q2: FMMT3906
L1: CDRH6D28-3R0

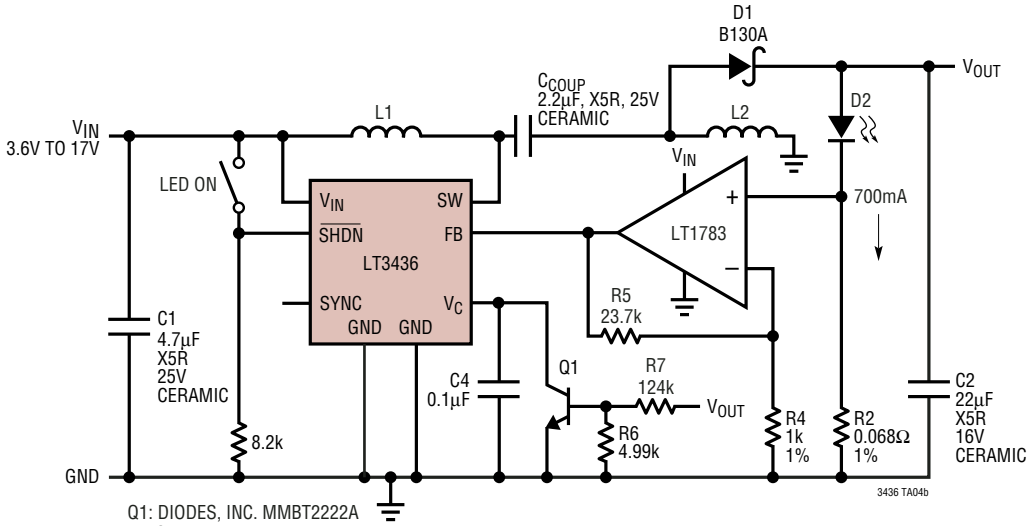
# TYPICAL APPLICATIONS

### Single Li-Ion Cell to 5V




| $I_{OUT}$ | $V_{IN}$ |
|---|---|
| 1.5A | 2.7V |
| 1.86A | 3.3V |
| 2.0A | 3.6V |

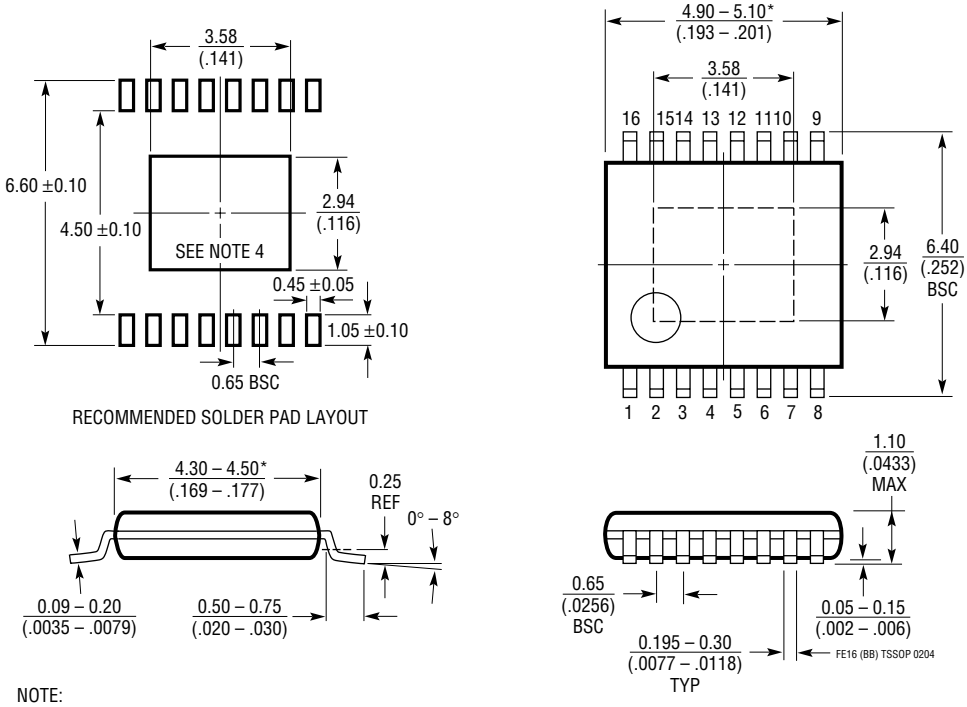
### SEPIC Converter Drives 5W LumiLEDs Luxeon V White LEDs at 70% Efficiency




Q1: DIODES, INC. MMBT2222A
L1: CDRH6D28 10µH 1.7A
L2: CDRH4D28 10µH 1A
D2: LUMILEDS LXHL-PW03 EMITTER OR LXHL-LW6C STAR

# PACKAGE DESCRIPTION

**FE Package**
**16-Lead Plastic TSSOP (4.4mm)**
(Reference LTC DWG # 05-08-1663)
**Exposed Pad Variation BB**




NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE