Low Noise, High Efficiency Charge Pump for White LEDs

FEATURES

- **Low Noise Constant Frequency Operation**
- **25% Less Input Current Than Doubler Charge Pump**
- **High Output Current: Up To 125mA**
- **Small Application Circuit**
- Regulated Output Voltage or Current
- Automatic Soft-Start
- V_{IN} Range: 2.7V to 4.5V
- No Inductors
- 1.5MHz Switching Frequency
- I_{CC} < 1µA in Shutdown
- Available in 10-Pin MSOP and 3mm × 3mm DFN Packages

APPLICATIONS

- White LED Backlighting
- Programmable Boost Current Source

DESCRIPTION

The LTC®3202 is a low noise, constant frequency charge pump DC/DC converter that uses fractional conversion to increase efficiency in white LED applications. The part can be used to produce a regulated voltage or current of up to 125mA from a 2.7V to 4.5V input. Low external parts count (two flying capacitors and two small bypass capacitors at V_{IN} and V_{OUT}) make the LTC3202 ideally suited for small, battery-powered applications.

An internal 2-bit DAC allows LED current to be adjusted for LED brightness control. The LTC3202 also has thermal shutdown protection and can survive a continuous short-circuit from V_{OUT} to GND. Built-in soft-start circuitry prevents excessive inrush current during start-up. High switching frequency enables the use of small external capacitors. A low current shutdown feature disconnects the load from V_{IN} and reduces quiescent current to less than1µA.

The LTC3202 is available in the 10-pin MSOP and 3mm × 3mm DFN packages.

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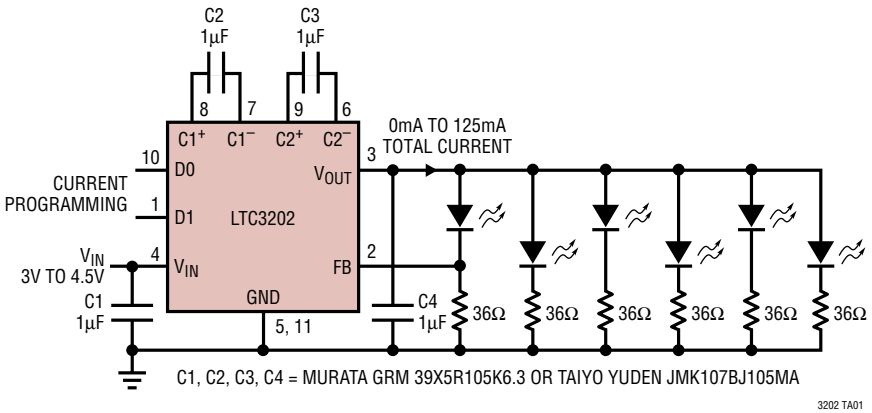
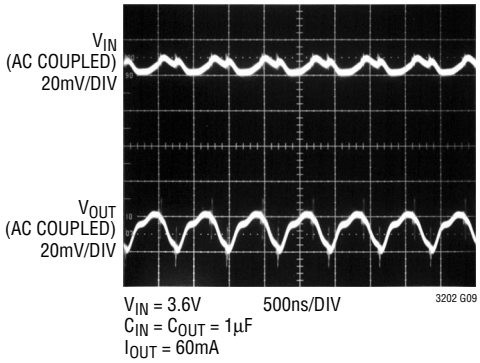
TYPICAL APPLICATION

Programmable White LED Power Supply



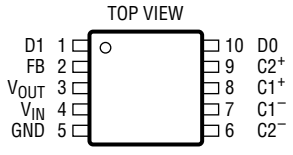
Input and Output Ripple



ABSOLUTE MAXIMUM RATINGS (Note 1)

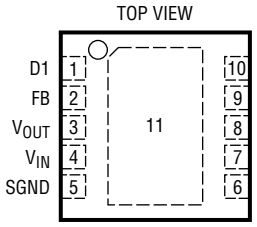
V_{IN}, V_{OUT} to GND .....–0.3V to 6V
D0, D1 .....–0.3V to V_{IN} + 0.3V
V_{OUT} Short-Circuit Duration ..... Indefinite
I_{OUT} (Note 2) 150mA
Operating Temperature Range (Note 3) ...–40°C to 85°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 120°C/W

ORDER PART NUMBER
LTC3202EMS
MS PART MARKING
LTWL



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 44°C/W, θ_{JC} = 3°C/W
EXPOSED PAD IS PGND (PIN 11) MUST BE CONNECTED TO GROUND PLANE

ORDER PART NUMBER
LTC3202EDD
DD PART MARKING
LABB

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Power Supply						
V_{IN} Operating Voltage		●	2.7		4.5	V
I_{CC} Operating Current	I_{OUT} = 0mA, V_{OUT} = 3.6V, V_{IN} = D0 = D1 = 4.5V	●		2.5	5	mA
I_{SHDN} Shutdown Current	V_{OUT} = 0V	●			1	µA
Feedback Pin Set Points						
0.2V Setting Feedback Voltage	D0 = 1, D1 = 0, I_{OUT} = 0mA, V_{IN} = 3.6V	●	188	200	212	mV
0.4V Setting Feedback Voltage	D0 = 0, D1 = 1, I_{OUT} = 0mA, V_{IN} = 3.6V	●	380	400	420	mV
0.6V Setting Feedback Voltage	D0 = 1, D1 = 1, I_{OUT} = 0mA, V_{IN} = 3.6V	●	570	600	630	mV
I_{FB}	V_{FB} = 0.8V	●	–50		50	nA
Charge Pump						
R_{OL} Open Loop Output Impedance $(1.5V_{IN} – V_{OUT})/I_{OUT}$	V_{IN} = 3.3V, V_{OUT} = 4.4V, V_{FB} = 0	●		4.5	6	Ω
V_{OUT} Load Regulation $(\Delta V_{OUT}/\Delta I_{OUT})$	I_{OUT} = 10mA to 90mA, $\Delta V_{FB}/\Delta V_{OUT}$ = 1			0.35		mV/mA
CLK Frequency				1.5		MHz
D0, D1						
High Level Input Voltage (V_{IH})		●	1.3			V
Low Level Input Voltage (V_{IL})		●			0.4	V
Input Current (I_{IH})	D0, D1 = V_{IN}	●	–1		1	µA
Input Current (I_{IL})	D0, D1 = 0V	●	–1		1	µA

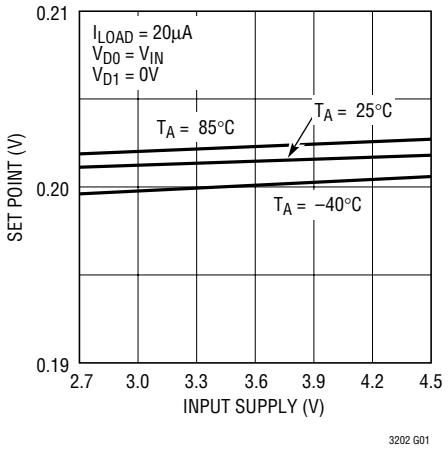
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Based on long-term current density limitations.

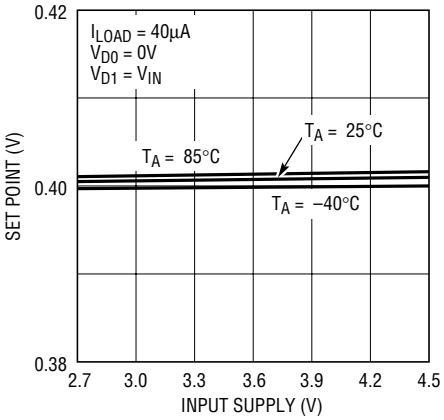
Note 3: The LTC3202E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

TYPICAL PERFORMANCE CHARACTERISTICS

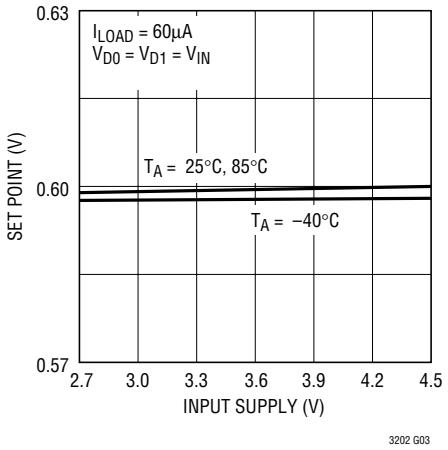
V_{FB} Set Point vs Input Supply (200mV Setting)



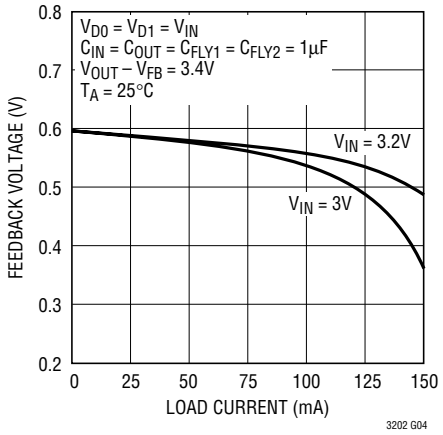
V_{FB} Set Point vs Input Supply (400mV Setting)



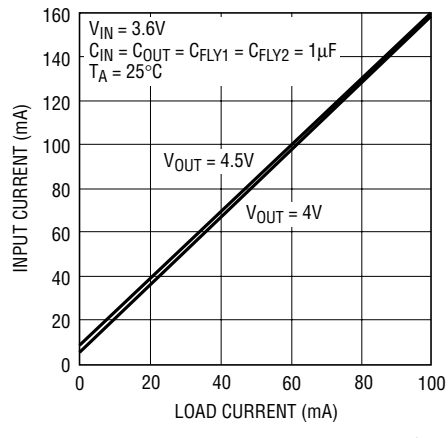
V_{FB} Set Point vs Input Supply (600mV Setting)



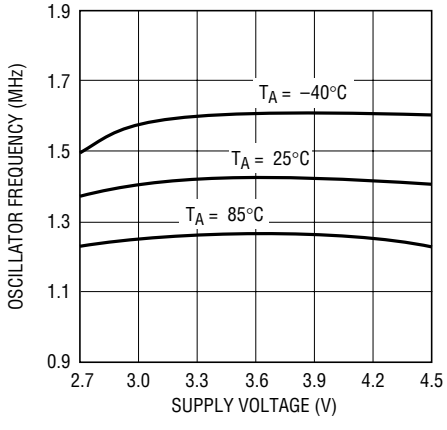
V_{FB} vs Load Current



Input Current vs Load Current

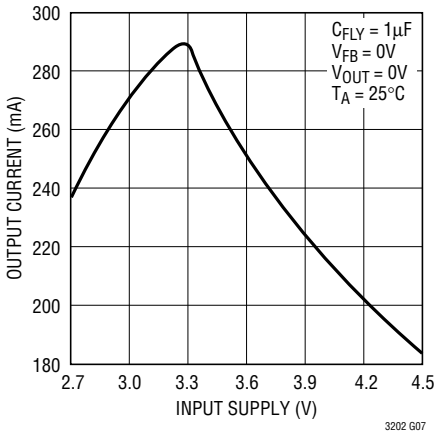


Oscillator Frequency vs Supply Voltage

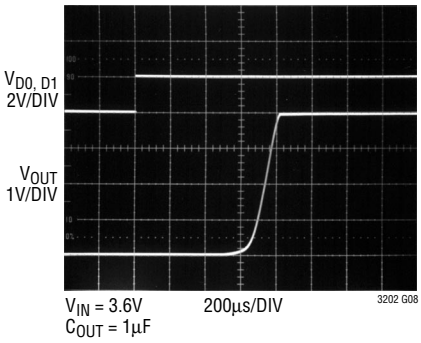


TYPICAL PERFORMANCE CHARACTERISTICS

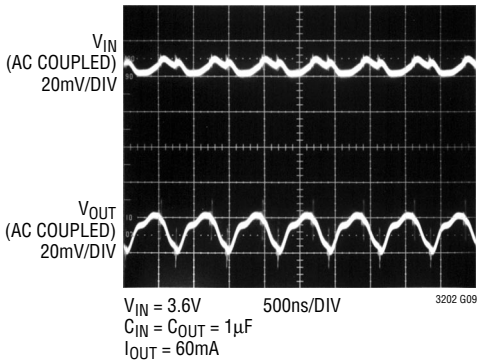
Short-Circuit Current vs Supply Voltage



V_{OUT} Soft-Start Ramp



Input and Output Ripple



PIN FUNCTIONS

D1, D0 (Pin 1, 10): Control Inputs. D0 and D1 determine the set point voltage of the FB pin (see Table 1).

FB (Pin 2): FB is the Feedback Input for the Regulation Control Loop.

V_{OUT} (Pin 3): V_{OUT} is the Output of the Charge Pump. A low impedance 1µF X5R or X7R ceramic capacitor is required from V_{OUT} to GND.

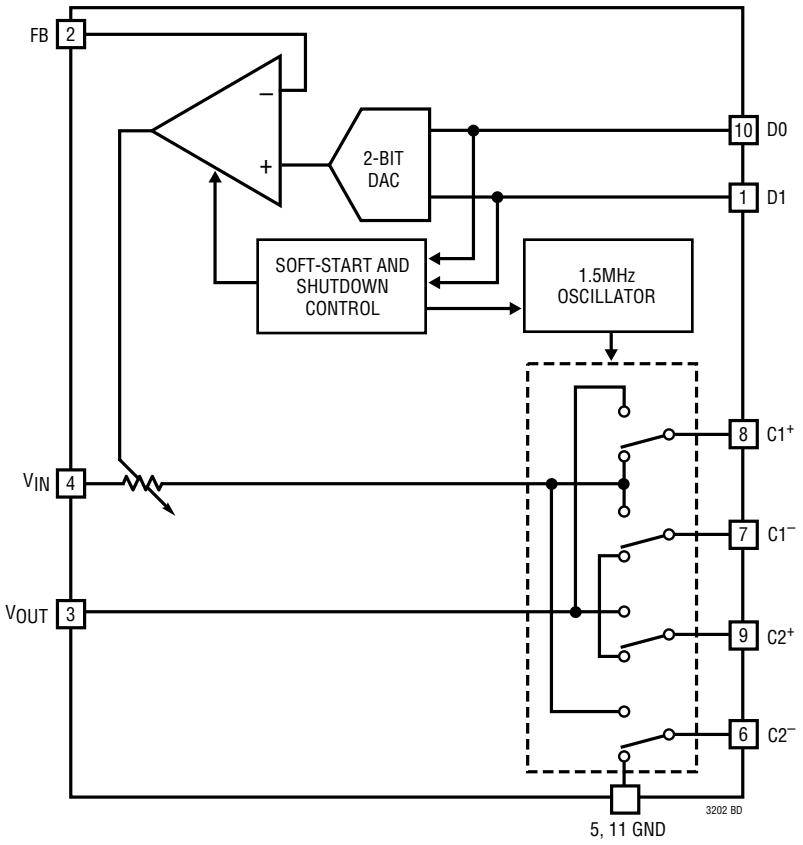
V_{IN} (Pin 4): Input Supply Voltage. V_{IN} should be bypassed with a 1µF to 4.7µF low impedance ceramic capacitor.

GND (Pin 5): Ground for the Charge Pump and Control Circuitry. This pin should be connected directly to a low impedance ground plane.

$C2^-$, $C1^-$, $C1^+$, $C2^+$ (Pin 6, 7, 8, 9): Charge Pump Flying Capacitor Pins. A 1µF X5R or X7R ceramic capacitor should be connected from $C1^+$ to $C1^-$ and from $C2^+$ to $C2^-$.

PGND (Pin 11, Exposed Pad DFN Only): Power Ground for the Charge Pump. This pin must be connected directly to a low impedance ground plane.

SIMPLIFIED BLOCK DIAGRAM



OPERATION (Refer to Simplified Block Diagram)

The LTC3202 uses a fractional conversion switched capacitor charge pump to boost V_{OUT} to as much as 1.5 times the input voltage. A two-phase nonoverlapping clock activates the charge pump switches. On the first phase of the clock the flying capacitors are charged in series from V_{IN}. On the second phase of the clock they are connected in parallel and stacked on top of V_{IN}. This sequence of charging and discharging the flying capacitors continues at a free running frequency of 1.5MHz (typ).

Regulation is achieved by sensing the voltage at the FB pin and modulating the charge pump strength based on the error signal. The control pins, D0 and D1, program the set point of the internal digital-to-analog converter. The regulation loop will increase V_{OUT} until FB comes to balance at the set-point voltage. Table 1 shows the regulation voltage as a function of D0 and D1.

Table 1. Feedback Control Voltage Settings

D1	D0	Feedback Set Point Voltage
0	0	Shutdown
0	1	0.2V
1	0	0.4V
1	1	0.6V

In shutdown mode all circuitry is turned off and the LTC3202 draws only leakage current from the V_{IN} supply. Furthermore, V_{OUT} is disconnected from V_{IN}. The D0 and D1 pins are CMOS inputs with a threshold voltage of approximately 0.8V. The LTC3202 is in shutdown when a logic low is applied to both D0 and D1. Since the D0 and D1 pins are high impedance CMOS inputs they should never be allowed to float. To ensure that their states are defined they must always be driven with valid logic levels.

Shutdown Current

Output voltage detection circuitry will draw a current of 5µA when the LTC3202 is in shutdown. This current will be eliminated when the output voltage (V_{OUT}) is at 0V. To ensure that V_{OUT} is at 0V in shutdown a bleed resistor can be used from V_{OUT} to GND. 10k to 100k is acceptable.

Short-Circuit/Thermal Protection

The LTC3202 has built-in short-circuit current limiting as well as over temperature protection. During short-circuit conditions it will automatically limit its output current to approximately 250mA. At higher temperatures, or if the input voltage is high enough to cause excessive self heating on-chip, thermal shutdown circuitry will shut down the charge pump when the junction temperature exceeds approximately 160°C. It will reenable the charge pump once the junction temperature drops back to approximately 155°C. The LTC3202 will cycle in and out of thermal shutdown indefinitely without latchup or damage until the short-circuit on V_{OUT} is removed.

Soft-Start

To prevent excessive current flow at V_{IN} during start-up, the LTC3202 has built-in soft-start circuitry. Soft-start is achieved by increasing the amount of current available to the output charge storage capacitor linearly over a period of approximately 500µs.

The soft-start feature activates any time an input, D0 or D1, changes state. This will prevent large inrush current during initial start-up as well as when the feedback setting is changed from one value to the next. Note that the set point voltage will drop to zero during the soft-start period. Under heavy load conditions there may be observable droop at V_{OUT} until the soft-start circuit catches up.

Programming the LTC3202 for Voltage or Current

The LTC3202 can be configured to control either a voltage or a current. In white LED applications the LED current is programmed by the ratio of the feedback set point voltage and a sense resistor as shown in Figure 1. The current of the remaining LEDs is controlled by virtue of their similarity to the reference LED and the ballast voltage across the sense resistor.

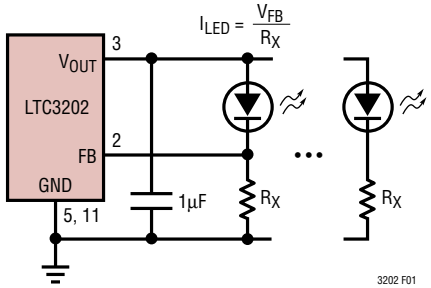


Figure 1. Current Control Mode

OPERATION (Refer to Simplified Block Diagram)

In this configuration the feedback factor ($\Delta V_{FB}/\Delta V_{OUT}$) will be very near unity since the small signal LED impedance will be considerably less than the current setting resistor R_X. Thus, this configuration will have the highest *loop gain* giving it the lowest closed-loop output resistance. Likewise it will also require the largest amount of output capacitance to preserve stability.

For fixed voltage applications, the output voltage can be set by the ratio of two resistors and the feedback control voltage as shown in Figure 2. The output voltage is given by the set point voltage times the gain factor $1 + R_1/R_2$. Note that the closed-loop output resistance will increase in proportion to the loop gain consumed by the resistive divider ratio. For example, if the resistor ratio is 2:1 giving a gain of 3, the closed-loop output resistance will be about 3 times higher than its nominal gain of 1 value. Given that the closed-loop output resistance is about 0.35Ω with a gain of 1, the closed-loop output resistance will be about 1Ω when using a gain of 3.

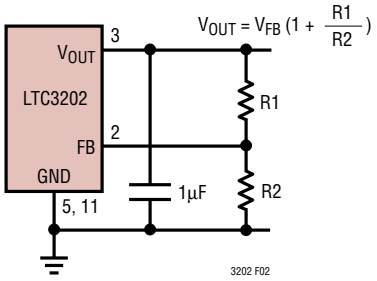


Figure 2. Voltage Control Mode

When using the LTC3202 in voltage control mode, any of the three voltage settings (0.2V, 0.4V or 0.6V) can be used as the set point voltage. For optimum noise performance and lowest closed-loop output resistance the highest voltage setting will likely be the most desirable.

Typical values for total voltage divider resistance can range from several kΩs up to 1MΩ.

Charge Pump Strength

Figure 3 shows how the LTC3202 can be modeled as a Thevenin equivalent circuit to determine the amount of current available from the effective input voltage, $1.5V_{IN}$ and the effective open-loop output resistance, R_{OL}.

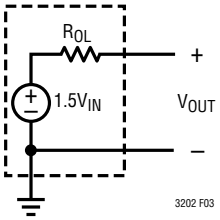


Figure 3. Equivalent Open-Loop Circuit

From Figure 3 the available current is given by:

$$I_{OUT} = \frac{1.5V_{IN} - V_{OUT}}{R_{OL}}$$

Typical values of R_{OL} as a function of temperature are shown in Figure 4.

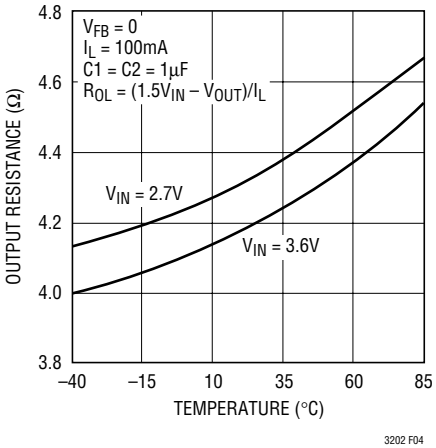


Figure 4. Typical R_{OL} vs Temperature

OPERATION

R_{OL} is dependent on a number of factors including the switching term, $1/(2f_{OSC}\ C_{FLY})$, internal switch resistances and the nonoverlap period of the switching circuit.

However, for a given R_{OL}, the amount of current available will be directly proportional to the *advantage voltage* $1.5V_{IN} – V_{OUT}$. This voltage can typically be quite small. Consider the example of driving white LEDs from a 3.1V supply. If the LED forward voltage is 3.8V and the 0.6V V_{FB} setting is used, the advantage voltage is 3.1V • 1.5V – 3.8V – 0.6V or only 250mV. However if the input voltage is raised to 3.2V the advantage voltage jumps to 400mV—a 60% improvement in available strength! Note that a similar improvement in advantage voltage can be achieved by operating the LTC3202 at a lower voltage setting such as the 0.4V setting.

V_{IN}, V_{OUT} Capacitor Selection

The style and value of capacitors used with the LTC3202 determine several important parameters such as regulator control loop stability, output ripple, charge pump strength and minimum start-up time.

To reduce noise and ripple, it is recommended that low equivalent series resistance (ESR) ceramic capacitors be used for both C_{IN} and C_{OUT}. Tantalum and aluminum capacitors are not recommended because of their high ESR.

The value of C_{OUT} directly controls the amount of output ripple for a given load current. Increasing the size of C_{OUT} will reduce the output ripple at the expense of higher minimum turn-on time and higher start-up current. The peak-to-peak output ripple is approximately given by the expression:

$$V_{RIPPLEP-P} \cong \frac{I_{OUT}}{3f_{OSC} \bullet C_{OUT}}$$

Where f_{OSC} is the LTC3202's oscillator frequency (typically 1.5MHz) and C_{OUT} is the output charge storage capacitor.

Both the style and value of the output capacitor can significantly affect the stability of the LTC3202. As shown in the block diagram, the LTC3202 uses a control loop to adjust the strength of the charge pump to match the current required at the output. The error signal of this loop is stored directly on the output charge storage capacitor. The charge storage capacitor also serves to form the dominant pole for the control loop. To prevent ringing or instability, it is important for the output capacitor to maintain at least 0.6µF of capacitance over all conditions.

Likewise, excessive ESR on the output capacitor will tend to degrade the loop stability of the LTC3202. The closed-loop output resistance of the LTC3202 is designed to be 0.35Ω. For a 100mA load current change, the feedback voltage will change by about 35mV. If the output capacitor has 0.35Ω or more of ESR the closed-loop frequency response will cease to roll-off in a simple one-pole fashion and poor load transient response or instability could result. Multilayer ceramic chip capacitors typically have exceptional ESR performance and combined with a tight board layout should yield very good stability and load transient performance.

As the value of C_{OUT} controls the amount of output ripple, the value of C_{IN} controls the amount of ripple present at the input pin (V_{IN}). The input current to the LTC3202 will be relatively constant while the charge pump is on either the input charging phase or the output charging phase but will drop to zero during the clock nonoverlap times. Since the nonoverlap time is small (~25ns) these missing "notches" will result in only a small perturbation on the input power supply line. Note that a higher ESR capacitor such as tantalum will have higher input noise due to the input current change times the ESR. Therefore ceramic capacitors are again recommended for their exceptional ESR performance.

Further input noise reduction can be achieved by powering the LTC3202 through a very small series inductor as shown in Figure 5. A 10nH inductor will reject the fast current notches, thereby presenting a nearly constant current load to the input power supply. For economy the 10nH inductor can be fabricated on the PC board with about 1cm (0.4") of PC board trace.

OPERATION

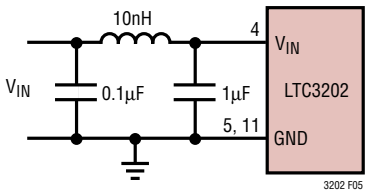


Figure 5. 10nH Inductor Used for Input Noise Reduction

Flying Capacitor Selection

Warning: A polarized capacitor such as tantalum or aluminum should never be used for the flying capacitors since their voltage can reverse upon start-up of the LTC3202. Ceramic capacitors should always be used for the flying capacitors.

The flying capacitor controls the strength of the charge pump. In order to achieve the rated output current it is necessary to have at least 0.7µF of capacitance for each of the flying capacitors.

Capacitors of different materials lose their capacitance with higher temperature and voltage at different rates. For example, a ceramic capacitor made of X7R material will retain most of its capacitance from –40°C to 85°C whereas a Z5U or Y5V style capacitor will lose considerable capacitance over that range. Z5U and Y5V capacitors may also have a very poor voltage coefficient causing them to lose 60% or more of their capacitance when the rated voltage is applied. Therefore, when comparing different capacitors it is often more appropriate to compare the amount of achievable capacitance for a given case size rather than comparing the specified capacitance value. For example, over rated voltage and temperature conditions, a 1µF, 10V, Y5V ceramic capacitor in a 0603 case may not provide any more capacitance than a 0.22µF, 10V, X7R available in the same 0603 case. The capacitor manufacturer's data sheet should be consulted to determine what value of capacitor is needed to ensure minimum capacitances at all temperatures and voltages.

Table 2 shows a list of ceramic capacitor manufacturers and how to contact them:

Table 2 Recommended Capacitor Vendors

AVX	www.avxcorp.com
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay	www.vishay.com

For very light load applications the flying capacitor may be reduced to save space or cost. The theoretical minimum output resistance of a 2:3 fractional charge pump is given by:

$$R_{OL(MIN)} \equiv \frac{1.5V_{IN} - V_{OUT}}{I_{OUT}} = \frac{1}{2f_{OSC}C_{FLY}}$$

Where f_{OSC} is the switching frequency (1.5MHz typ) and C_{FLY} is the value of the flying capacitors. Note that the charge pump will typically be weaker than the theoretical limit due to additional switch resistance, however for very light load applications the above expression can be used as a guideline in determining a starting capacitor value.

Power Efficiency

The power efficiency (η) of the LTC3202 is similar to that of a linear regulator with an effective input voltage of 1.5 times the actual input voltage. This occurs because the input current for a 2:3 fractional charge pump is approximately 1.5 times the load current. In an ideal regulating 2:3 charge pump the power efficiency would be given by:

$$\eta_{IDEAL} \equiv \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet \frac{3}{2} I_{OUT}} = \frac{V_{OUT}}{1.5V_{IN}}$$

At moderate to high output power the switching losses and quiescent current of the LTC3202 are negligible and the expression above is valid. For example with V_{IN} = 3.2V, I_{OUT} = 80mA and V_{OUT} regulating to 4.2V the measured efficiency is 82% which is just under the theoretical 87.5% calculation.

OPERATION

Layout Considerations

Due to its high switching frequency and the transient currents produced by the LTC3202, careful board layout is necessary. A true ground plane and short connections to all capacitors will improve performance and ensure proper regulation under all conditions. Figure 6 shows the recommended layout configurations.

The flying capacitor pins $C1^+$, $C2^+$, $C1^-$ and $C2^-$ will have very high edge rate waveforms. The large dv/dt on these pins can couple energy capacitively to adjacent printed circuit board runs. Magnetic fields can also be generated if the flying capacitors are not close to the LTC3202 (i.e. the loop area is large). To decouple capacitive energy transfer, a Faraday shield may be used. This is a grounded PC trace between the sensitive node and the LTC3202 pins. For a high quality AC ground it should be returned to a solid ground plane that extends all the way to the LTC3202.

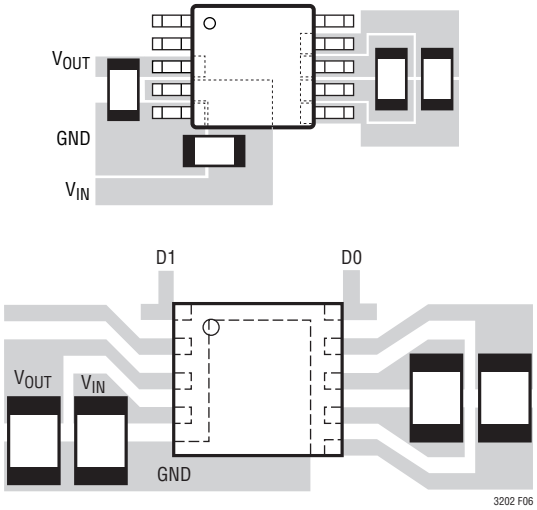


Figure 6. Recommended Layouts

Thermal Management

For higher input voltages and maximum output current there can be substantial power dissipation in the LTC3202. If the junction temperature increases above approximately 160°C the thermal shutdown circuitry will automatically deactivate the output. To reduce the maximum junction temperature, a good thermal connection to the PC board is recommended. Connecting the GND pin (Pin 5 and Pin 11 on the DFN package) to a ground plane, and maintaining a solid ground plane under the device can reduce the thermal resistance of the package and PC board considerably.

Brightness Control Using Pulse Width Modulation

An alternative approach to dimming is to use pulse width modulation rather than the internal digital to analog converter. By connecting both the D0 and D1 pins to a PWM signal, continuous brightness control can be achieved. Frequencies from 100Hz to 500Hz are acceptable with a 1µF to 4.7µF output capacitor.

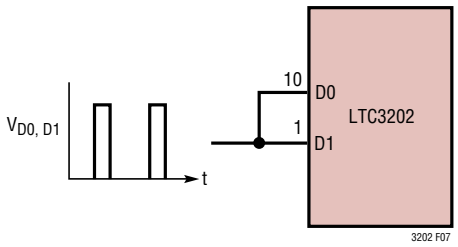
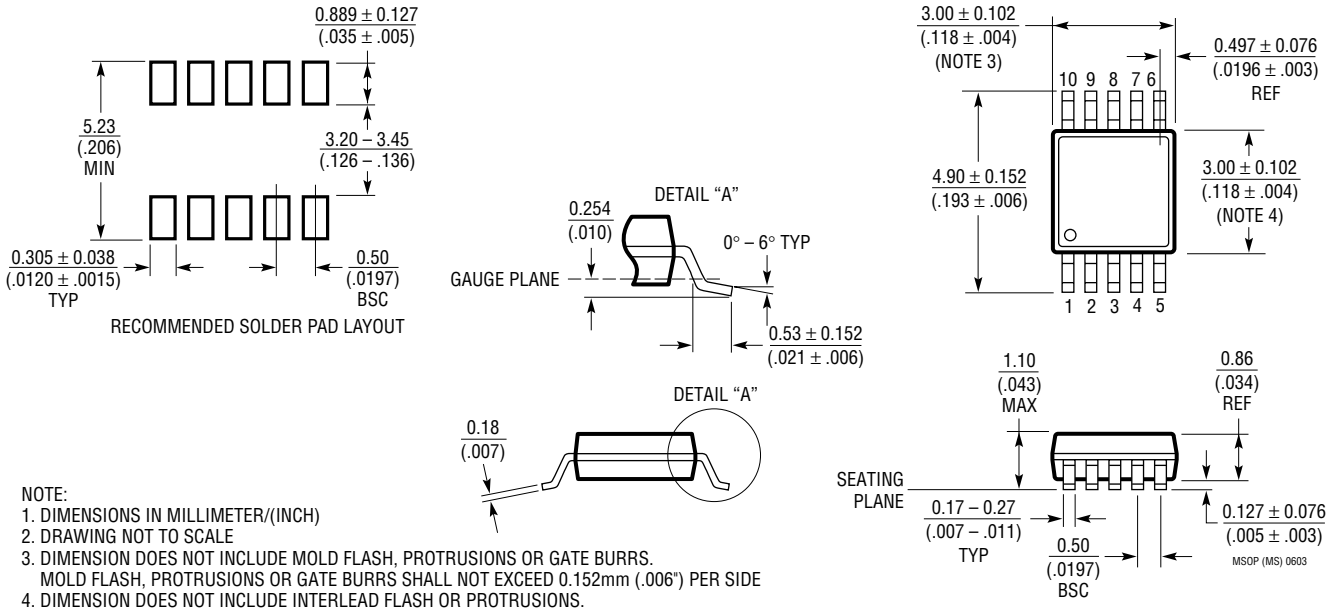


Figure 7. Alternative Brightness Control

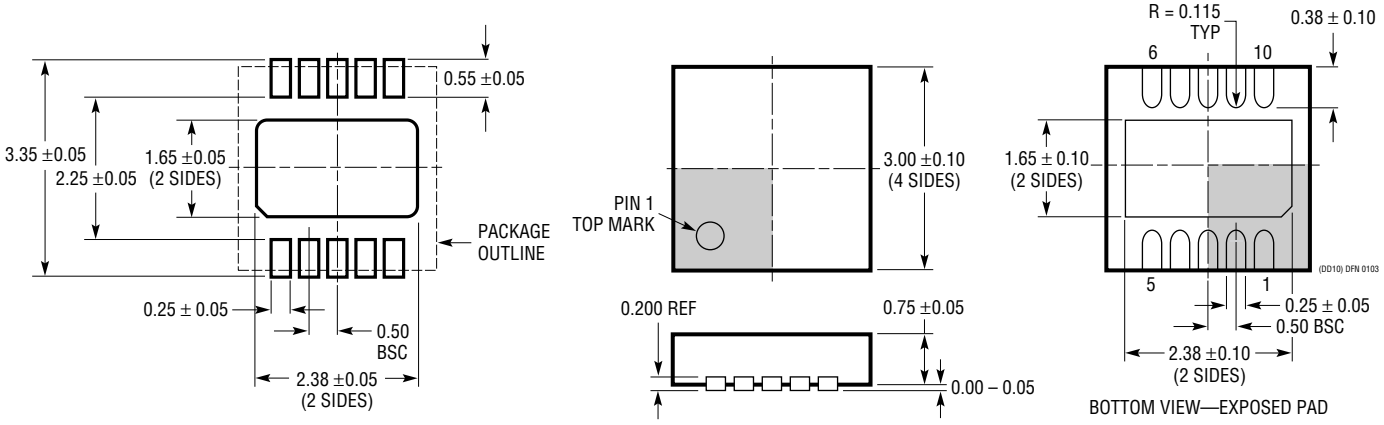
PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2)
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. EXPOSED PAD SHALL BE SOLDER PLATED

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.