Dual 550kHz Synchronous 2-Phase DC/DC Controller with Programmable Up/Down Tracking

FEATURES

- **Wide V_{IN} Range: 3V to 30V Operation with Line Feedforward Compensation**
- **Leading Edge Modulation Architecture for Extremely Low Duty Cycle Operation**
- **Phase-Lockable Fixed Frequency: 330kHz to 750kHz**
- **Two 180° Out-of-Phase Controllers**
- **Fast Programmable Power-Up/-Down Tracking**
- Programmable Current Limit Without External Current Sense Resistor
- Optional Burst Mode® Operation at Light Load
- ±1% 0.6V Voltage Reference
- External N-Channel MOSFET Architecture
- Low Shutdown Current: <100µA
- Overvoltage Protection and PGOOD Flag
- Small 28-Lead SSOP and 32-Lead QFN Packages

APPLICATIONS

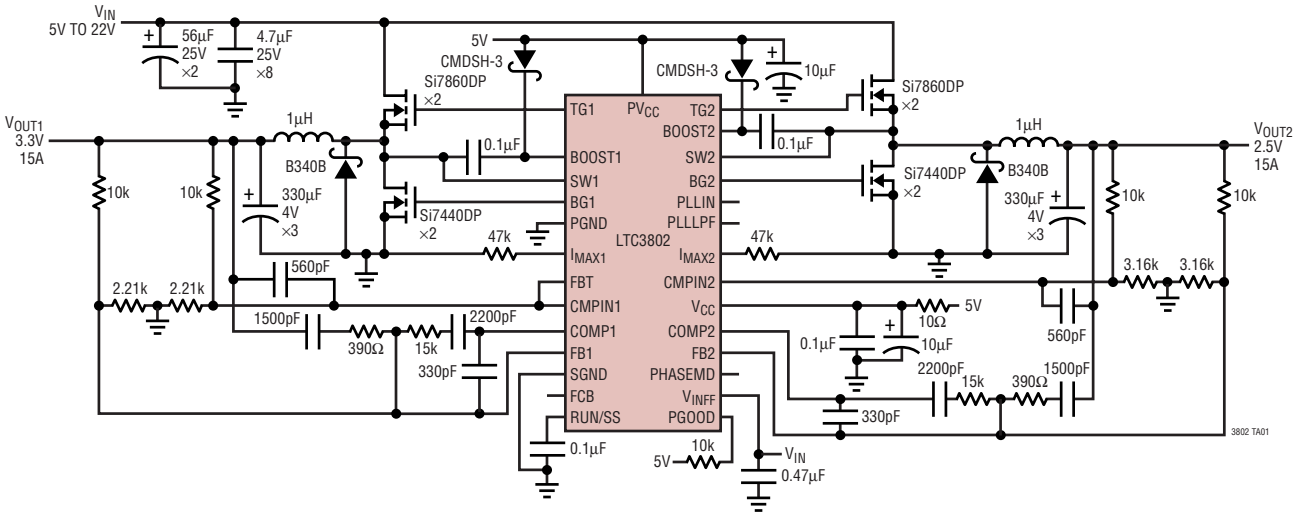
- Notebook and Palmtop Computers
- Portable Instruments
- Battery-Operated Digital Devices
- DC Power Distribution Systems

DESCRIPTION

The LTC®3802 is a dual switching regulator controller optimized for high efficiency step-down conversion from input voltages between 3V to 30V. The controller uses a leading edge modulation scheme to allow extremely low duty cycle operation. The constant frequency voltage mode controller allows a phase-lockable frequency between 330kHz and 750kHz. Power loss and noise due to the ESR of the input capacitors are minimized by operating the two controller output stages 180° out of phase. The synchronous buck architecture automatically shifts to Burst Mode operation as the output load decreases, ensuring maximum efficiency over a wide range of load currents.

The LTC3802 features an onboard, trimmed 0.6V reference and provides better than 1% regulation at the converter outputs. A separate output sense provides real time overvoltage protection and PGOOD sensing. An FBT pin programs the power-up/-down tracking between the two channels to meet various sequencing requirements. A RUN/SS pin provides soft-start and externally programmable current limit protection functions.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage
- V_{CC}, PV_{CC} 7V
- BOOST*n* 37V
- BOOST*n* – SW*n* 7V
- SW*n* ..... –1V to 30V

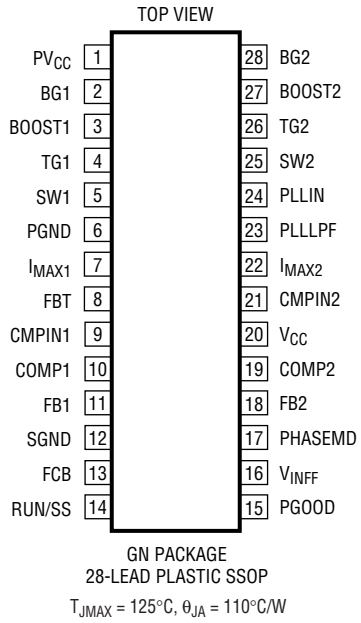
Input Voltage
- V_{INFF} 30V
- FB*n*, CMPIN*n*, FBT, PLLIN, FCB, RUN/SS, PGOOD, PLLLPF, PHASEMD, EXTREF, $I_{MAX}n$ ..... –0.3V to V_{CC} + 0.3V

Extended Commercial Operating Temperature Range (Note 2) .. –40°C to 85°C

Storage Temperature Range
- LTC3802EGN ..... –65°C to 150°C
- LTC3802EUH ..... –65°C to 125°C

Lead Temperature (Soldering, 10 sec)
- LTC3802EGN Only ..... 300°C

PACKAGE/ORDER INFORMATION

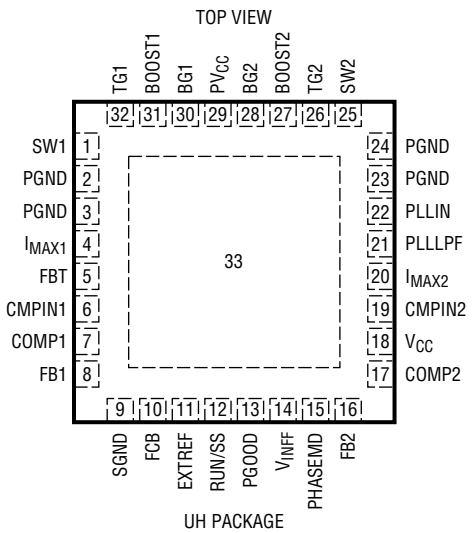


GN PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER

LTC3802EGN



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W

EXPOSED PAD (PIN 33) IS GND MUST BE SOLDERED TO PCB

ORDER PART NUMBER

LTC3802EUH

UH PART MARKING

3802

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range. (Note 3) V_{CC} = PV_{CC} = BOOST = 5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	V_{CC} Supply Voltage		●	3	5	6	V
PV_{CC}	PV_{CC} Supply Voltage	(Note 4)	●		5	6	V
BV_{CC}	BOOST Pin Voltage	V_{BOOST} – V_{SW} (Note 4)	●		5	6	V
V_{UVLO}	Positive Undervoltage Lockout	Measured at V_{CC} Measured at V_{INFF}		2.2 2.2	2.5 2.5	2.8 2.8	V V
I_{VCC}	V_{CC} Supply Current	V_{FB} = V_{COMP} $V_{RUN/SS}$ = 0V, PLLIN Floating	● ●		6.5 100	9 150	mA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range. (Note 3) V_{CC} = PV_{CC} = BOOST = 5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{PVCC}	PV_{CC} Supply Current	V_{FB} = V_{CMPIN} = 0V, No Load $V_{RUN/SS}$ = 0V (Notes 5, 6)			2 1	 10	mA µA
I_{BOOST}	BOOST Pin Current	V_{FB} = V_{CMPIN} = 0V, No Load $V_{RUN/SS}$ = 0V (Notes 5, 6)			1 1	 10	mA µA
Switcher Control Loop							
V_{FB}	Feedback Voltage	V_{EXTREF} = 5V, 0°C ≤ T ≤ 70°C V_{EXTREF} = 5V	 ●	0.594 0.591	0.600 0.600	0.606 0.609	V V
ΔV_{FB}	Feedback Voltage V_{CC} Line Regulation	V_{CC} = 4.5V to 6V			±0.01		%/V
ΔV_{OUT}	Output Voltage Load Regulation	(Note 7)			0.1	±0.2	%
A_{ERR}	Error AMP DC Gain	No Load, V_{EXTREF} = $V_{RUN/SS}$ = V_{CC}	●	70	80		dB
GBW	Error AMP Gain Bandwidth Product	f = 100kHz (Note 7)			10		MHz
I_{COMP}	Error AMP Output Sink/Source Current	$V_{RUN/SS}$ = V_{CC}			±12		mA
I_{FB}	Voltage Feedback Input Current	V_{FB} = 0V to 1V	●			±1	µA
I_{CMPIN}	Comparators Input Current	V_{CMPIN} = 0V to 1V	●			±1	µA
I_{FBT}	FBT Input Current	V_{FBT} = 0V to 1V	●			±1	µA
I_{EXTREF}	EXTREF Input Current	V_{EXTREF} = 0V to 5V	●			±1	µA
V_{EXTREF}	External Reference Not to Affect V_{FB}		●	1			V
A_{LFF}	Δ Drop in Duty Cycle/Δ V_{INFF}	V_{VINFF} = 5V to 30V			2.3		%/V
R_{VINFF}	V_{INFF} Input Resistance				1		MΩ
V_{PGOOD}	Positive Power Good Threshold Negative Power Good Threshold	With Respect to 0.6V With Respect to 0.6V	● ●	5 –5	10 –10	15 –15	% %
V_{OVP}	Overvoltage Threshold	With Respect to V_{FB}		3	5	9	%
V_{BURRS}	(V_{CMPIN} – V_{FB}) to Reset Burst Mode Operation				15 –12		mV mV
V_{SAW}	SAW Before Line Compensation				1.2		V
I_{IMAX}	I_{MAX} Source Current	V_{IMAX} = 1V	 ●	–9.0 –8.5	–10 –10	–11.0 –11.5	µA µA
$I_{LIM(TH)}$	I_{LIM} Comparator Offset V_{IMAX}/I_{LIM} Threshold Hard I_{LIM}/I_{LIM} Threshold	 V_{CMPIN} = 0V	●	–15	0 5 1.5	15	mV V/V V/V
I_{SS}	RUN/SS Source Current RUN/SS Sink/Source Current Ratio RUN/SS Sink Current, I_{LIM} RUN/SS Sink Current, Hard I_{LIM}	V_{CMPIN} = V_{FBT} = 0.6V, $V_{PHASEMD}$ = V_{CC} V_{CMPIN} = V_{FBT} = 0.6V, $V_{PHASEMD}$ = 0V V_{CMPIN} = V_{FBT} = 0.6V V_{CMPIN} = V_{FBT} = 0V	 ●	–5 1.5 1	–7 2 100	–9 2.5	µA µA/µA µA mA
V_{SHDN}	RUN/SS Shutdown Threshold	RUN/SS↑	●	0.4	0.8	1.2	V
LOGIC and PGOOD							
$I_{PHASEMD}$	PHASEMD Pull-Up Current PHASEMD Pull-Down Current	$V_{PHASEMD}$ = 0V $V_{PHASEMD}$ = 5V			–7 2		µA µA
V_{IH}	PLLIN, FCB High Level Input Voltage		●	2.4			V
V_{IL}	PLLIN, FCB Low Level Input Voltage		●			0.8	V
I_{PGOOD}	V_{PGOOD} Leakage Current	Power Good				±1	µA
V_{OLPG}	V_{PGOOD} Output Low Voltage	I_{PGOOD} = 1mA	●		0.1	0.3	V
t_{PGOOD}	V_{PGOOD} Falling Edge Delay V_{PGOOD} Rising Edge Delay	(Note 8) (Note 8)	●	100	150 10		µs µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range. (Note 3) V_{CC} = PV_{CC} = BOOST = 5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switcher Switching Characteristics							
f_{OSC}	Oscillator Frequency	PLLIN Open or V_{PLLIN} = 0V		490	550	610	kHz
		V_{PLLLPF} = 1.2V			550		kHz
		V_{PLLLPF} = 0V		250	330	400	kHz
		V_{PLLLPF} = 2.4V		650	750	850	kHz
R_{PLLIN}	PLLIN Pull-Down Current Source				5		µA
I_{PLLLPF}	Phase Detector Output Current						
	Sourcing Capability	$f_{PLLIN} > f_{OSC}$			–15		µA
	Sinking Capability	$f_{PLLIN} < f_{OSC}$			15		µA
Phase	TG1↓ vs PLLIN↓	PHASEMD Floats			0		Deg
	TG1↓ vs PLLIN↓	$V_{PHASEMD}$ = 5V			90		Deg
	TG2↓ vs PLLIN↓	PHASEMD Floats			180		Deg
	TG2↓ vs PLLIN↓	$V_{PHASEMD}$ = 5V			270		Deg
$V_{PHASEMD}$	Shutdown Threshold		●	1.2	1.7		V
	Floating				2.0		V
	90° Phase Threshold		●	3.5	4.0	4.5	V
DC_{MIN}	Minimum TG Duty Cycle	V_{PLLIN} = 0V	●			0	%
DC_{MAX}	Maximum TG Duty Cycle	V_{PLLIN} = 0V, V_{CMPIN} = 0.6V (Note 9)	●	86	89	92	%
$t_{ON(MIN)}$	TG Minimum Pulse Width	(Notes 7, 10)			50		ns
	BG Minimum Pulse Width	V_{CMPIN} = 0V (Note 9)			400		ns
t_{NOV}	Driver Nonoverlap	No Load		10	30	80	ns
$R_{DS(ON)}$	TG High $R_{DS(ON)}$	I_{OUT} = 100mA (Note 7)			1.6	2.20	Ω
	TG Low $R_{DS(ON)}$				1.3	1.80	Ω
	BG High $R_{DS(ON)}$				1.8	2.50	Ω
	BG Low $R_{DS(ON)}$				0.7	1.00	Ω

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC3802 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: To ensure proper operation, PV_{CC} and BV_{CC} ($V_{BOOST} – V_{SW}$) must be greater than $V_{GS(ON)}$ of the external MOSFETs.

Note 5: Supply current in normal operation is dominated by the current needed to charge and discharge the external MOSFET gates. This current will vary with supply voltage and the external MOSFETs used.

Note 6: Supply current in shutdown is dominated by external MOSFET leakage and may be significantly higher than the quiescent current drawn by the LTC3802, especially at elevated temperature.

Note 7: Guaranteed by design, not subject to test.

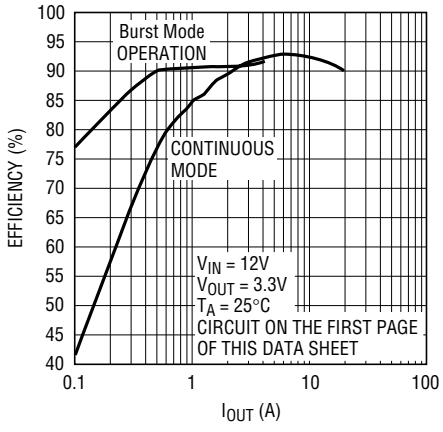
Note 8: Rise and fall times are measured using 10% and 90% levels. Delay and nonoverlap times are measured using 50% levels.

Note 9: If V_{CMPIN} is less than 90% of its nominal value, BG minimum pulse width is limited to 400ns.

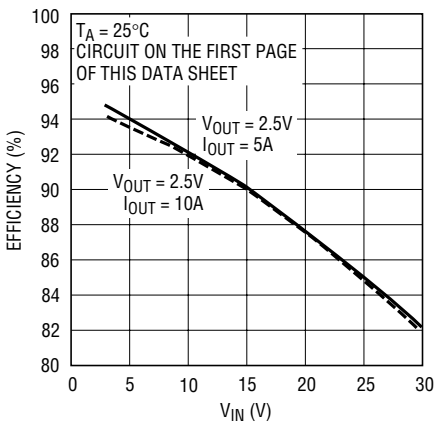
Note 10: The LTC3802 leading edge modulation architecture does not have a minimum TG pulse width requirement. The TG minimum pulse width is limited by the rise and fall times.

TYPICAL PERFORMANCE CHARACTERISTICS

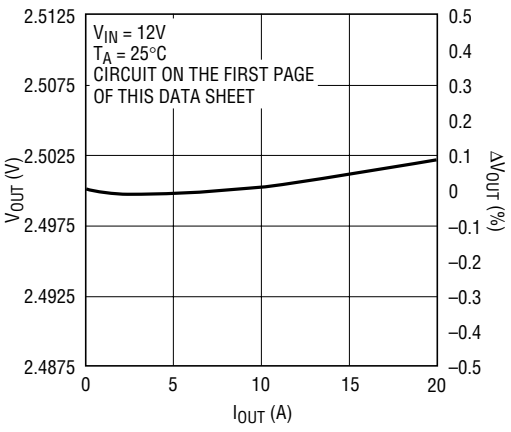
Efficiency vs I_{OUT}



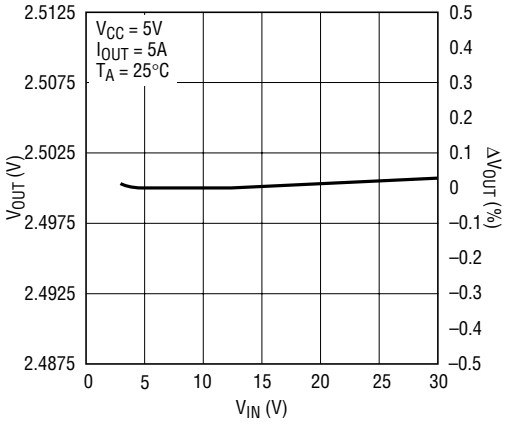
Efficiency vs V_{IN}



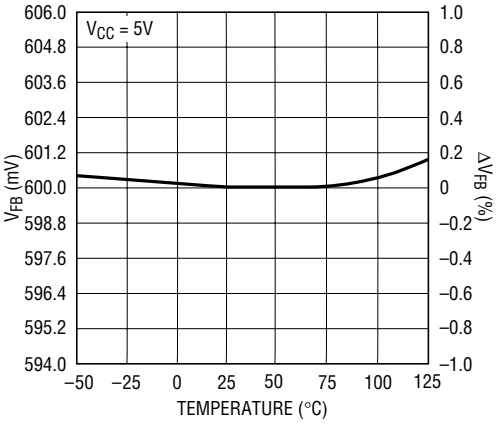
Load Regulation



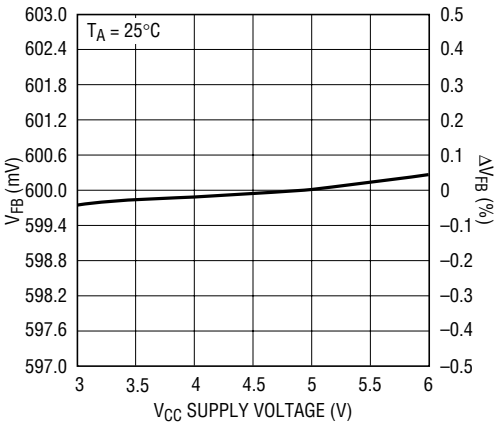
Line Regulation



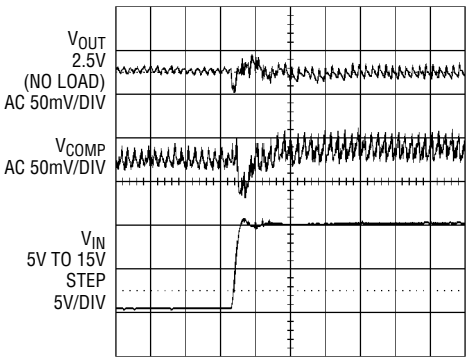
V_{FB} vs Temperature



V_{FB} vs V_{CC} Supply Voltage



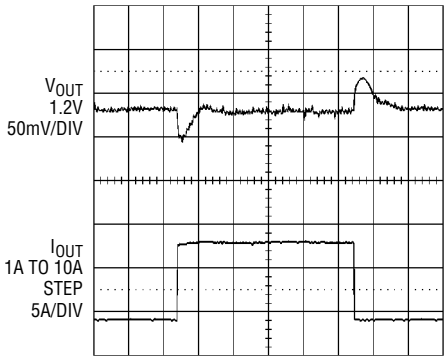
Line Feedforward Transient



CIN: 1µF/50V ×6 10µs/DIV
SANYO 35CV220AX

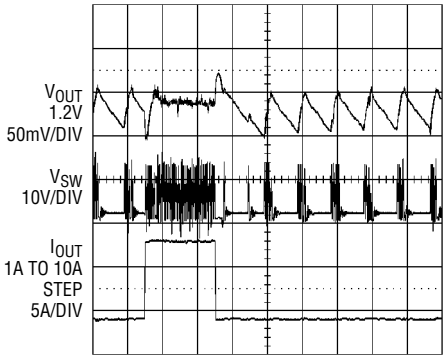
TYPICAL PERFORMANCE CHARACTERISTICS

Load Step in Continuous Mode



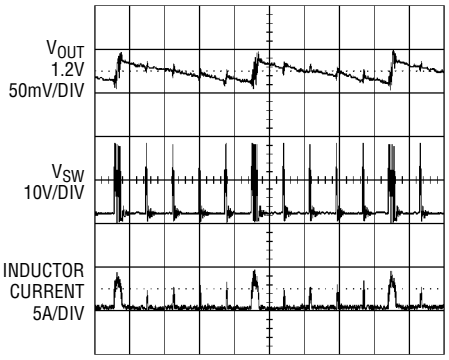
V_{IN} = 12V 20µs/DIV
CIRCUIT ON
FIRST PAGE OF THIS DATA SHEET

Load Step in Burst Mode Operation



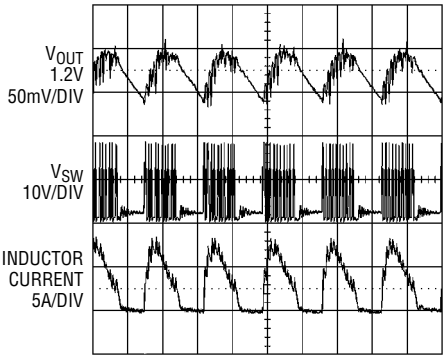
V_{IN} = 12V 50µs/DIV
CIRCUIT ON
FIRST PAGE OF THIS DATA SHEET

Burst Mode Waveform with 0.2A Load



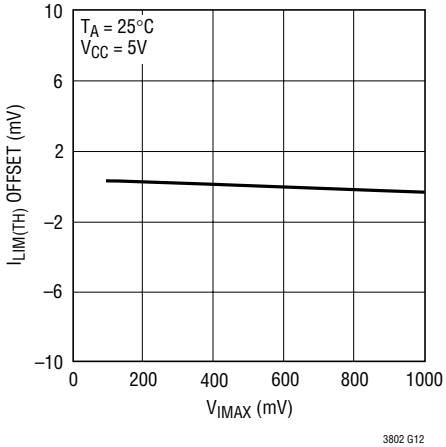
V_{IN} = 12V 50µs/DIV
CIRCUIT ON
FIRST PAGE OF THIS DATA SHEET

Burst Mode Waveform with 3A Load

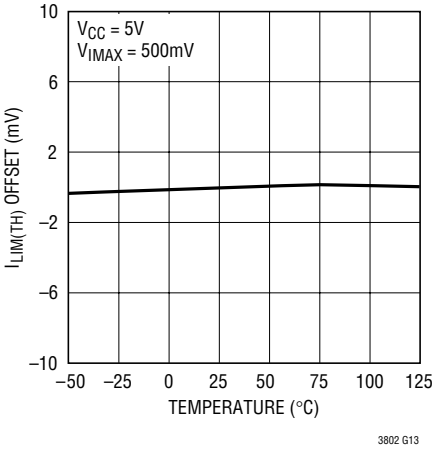


V_{IN} = 12V 20µs/DIV
CIRCUIT ON
FIRST PAGE OF THIS DATA SHEET

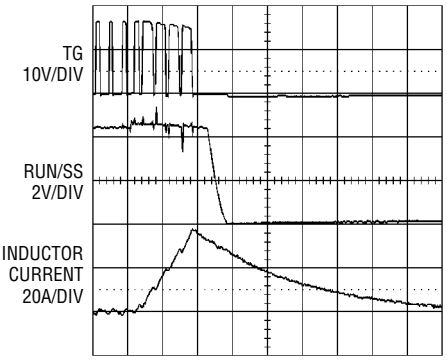
$I_{LIM(TH)}$ Offset vs V_{IMAX}



$I_{LIM(TH)}$ Offset vs Temperature

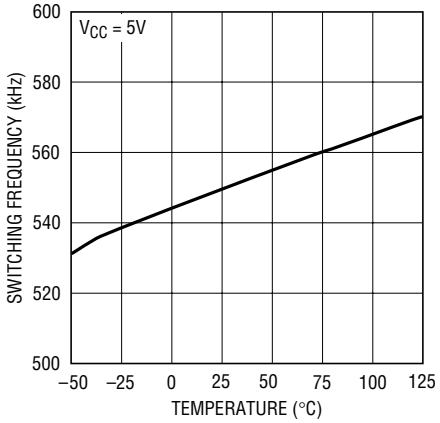


Short-Circuit Test

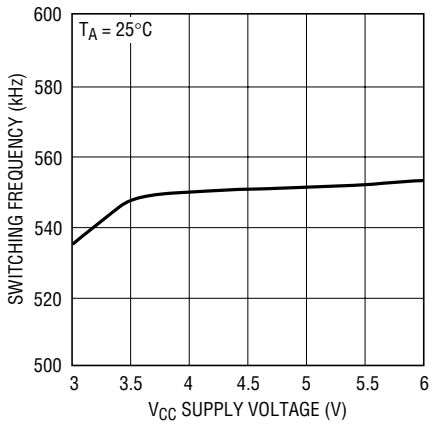


CIRCUIT ON 5µs/DIV
FIRST PAGE OF THIS DATA SHEET
V_{IN} = 12V, V_{OUT} = 3.3V, C_{SS} = 0.01µF,
$R_{I(MAX)}$ = 47k, L = 1µH (TOKO-FDA1254-1ROM)

Switching Frequency vs Temperature

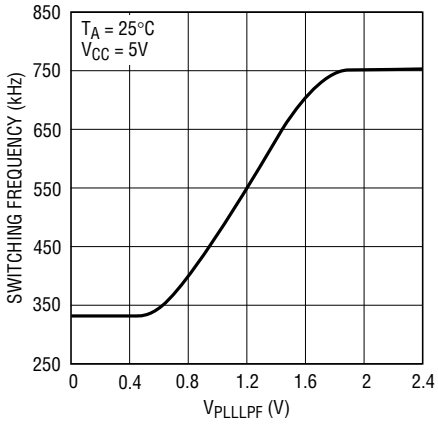


Switching Frequency vs V_{CC} Supply Voltage

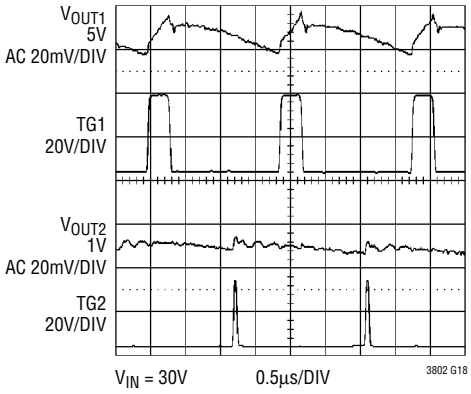


TYPICAL PERFORMANCE CHARACTERISTICS

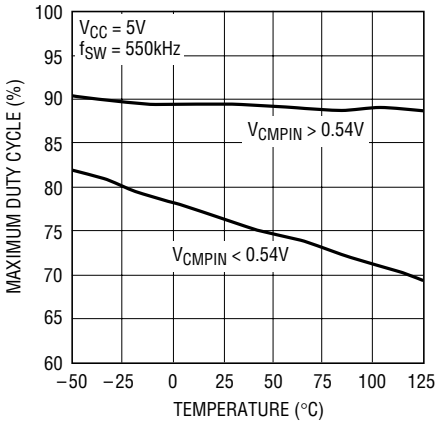
Switching Frequency vs V_{PLLLPF}



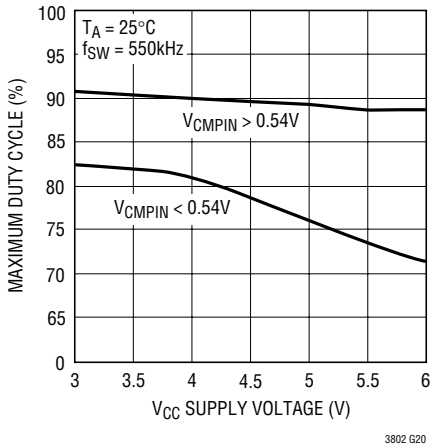
Continuous Mode Operation



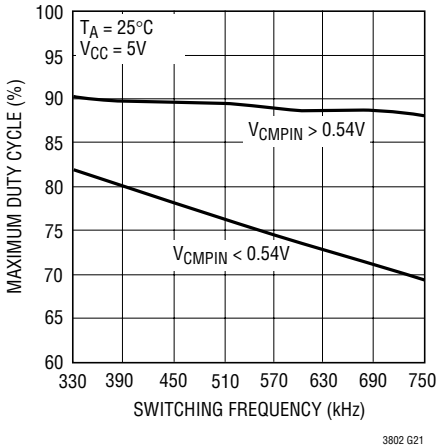
Maximum Duty Cycle vs Temperature



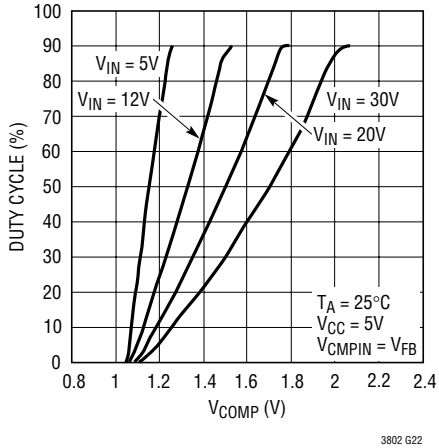
Maximum Duty Cycle vs V_{CC} Supply Voltage



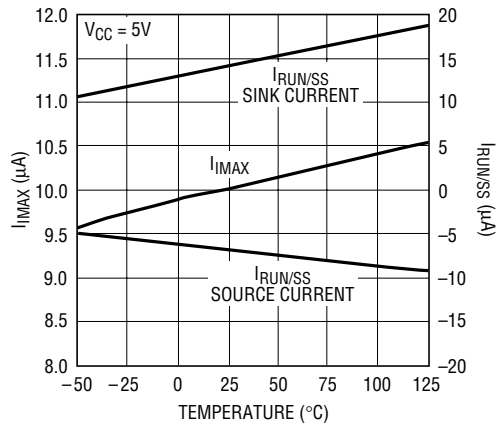
Maximum Duty Cycle vs Switching Frequency



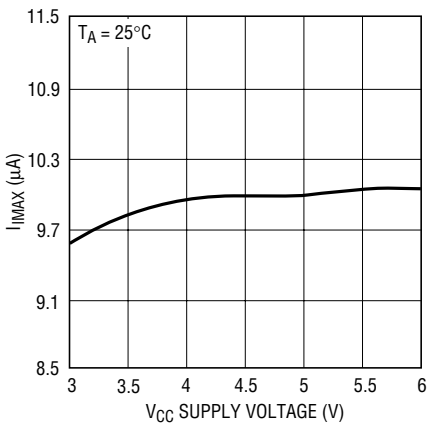
Duty Cycle vs V_{COMP}



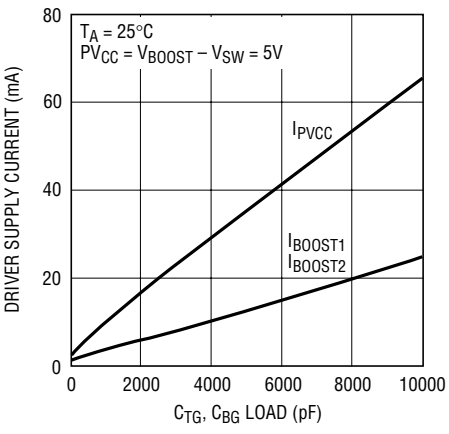
I_{IMAX} and $I_{RUN/SS}$ vs Temperature



I_{IMAX} vs V_{CC} Supply Voltage

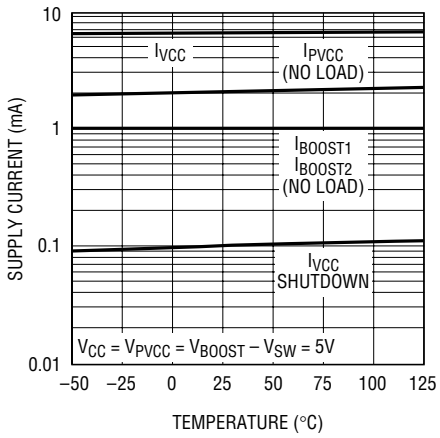


Driver Supply Current vs Load

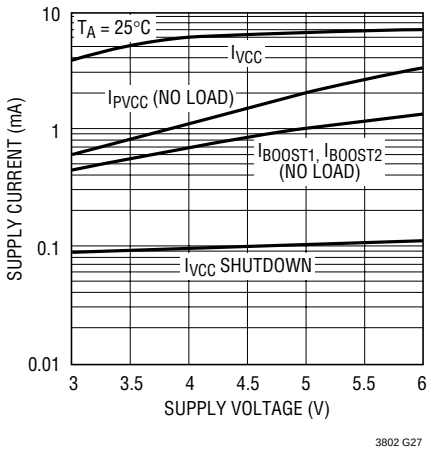


TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Temperature



Supply Current vs Supply Voltage



PIN FUNCTIONS (28-Pin SSOP/32-Pin QFN Package)

PV_{CC} (Pin 1/Pin 29): Driver Power Supply Input. PV_{CC} provides power to the two BG drivers and must be connected to an external voltage high enough to fully turn on the external MOSFETs, QB1 and QB2. PV_{CC} requires at least a 10µF bypass capacitor directly to PGND.

BG1 (Pin 2/Pin 30): Channel 1 Controller Bottom Gate Drive. The BG1 pin drives the gate of the bottom N-channel synchronous switch MOSFET, QB1. BG1 is designed to drive typically up to 10,000pF of gate capacitance.

BOOST1 (Pin 3/Pin 31): Channel 1 Controller Top Gate Driver Supply. BOOST1 should be bootstrapped to SW1 with a 0.1µF capacitor. An external Schottky diode from PV_{CC} to BOOST1 creates a complete floating charge-pumped supply at BOOST1. No other external supplies are required.

TG1 (Pin 4/Pin 32): Channel 1 Controller Top Gate Drive. The TG1 pin drives the top N-channel MOSFET with a voltage swing equal to PV_{CC} superimposed on the switch node voltage SW1. TG1 is designed to drive typically up to 6000pF of gate capacitance.

SW1 (Pin 5/Pin 1): Channel 1 Controller Switching Node. Connect SW1 to the switching node of the channel 1 converter. When the bottom MOSFET QB1 turns on, the current limit comparator and the burst comparator monitor the voltage at SW1. If the voltage drop across MOSFET QB1 is too large, the controller enters current limit; if it is too small, the switcher enters Burst Mode operation. See Current Limit and Burst Mode Applications Information.

PGND (Pin 6/Pins 2, 3, 23, 24): Power Ground. The BG drivers return to this pin. Connect PGND to a high current ground node in close proximity to the sources of external MOSFETs QB1 and QB2 and the V_{IN}, PV_{CC} and V_{OUT} bypass capacitors.

I_{MAX1} (Pin 7/Pin 4): Channel 1 Controller Current Limit Set. The I_{MAX1} pin has an internal 10µA current source pull-up, allowing the current limit and burst comparator threshold to be programmed by a single external resistor to SGND. See Current Limit and Burst Mode Applications Information.

PIN FUNCTIONS (28-Pin SSOP/32-Pin QFN Package)

FBT (Pin 8/Pin 5): Feedback Tracking Input. FBT should be connected through a resistive divider network to V_{OUT1} to set the channel 1 output slew rate. Upon power-up/-down, the LTC3802 servos FBT and CMPIN2 to the same potential to control the output power-up/-down slew rate. To program both outputs to have the same slew rate, duplicate the CMPIN2 resistive divider at FBT. To have a ratiometric slew rate, short FBT to CMPIN1. To disable the tracking function, short FBT to CMPIN2.

CMPIN1 (Pin 9/Pin 6): Channel 1 Controller Comparators Input. CMPIN1 should be connected through a resistive divider network to V_{OUT1} to monitor its real time output voltage. To improve transient response, a feedforward capacitor can be added to the resistive divider. The power good comparators, overvoltage comparator and Burst reset comparators monitor this node directly. CMPIN1 is a sensitive pin, avoid coupling noise into this pin.

COMP1 (Pin 10/Pin 7): Channel 1 Controller Error Amplifier Output. The COMP1 pin is connected directly to the channel 1 error amplifier output and the input of the line feedforward circuit. Use an RC network between the COMP1 pin and the FB1 pin to compensate the feedback loop for optimum transient response. Under start-up conditions, the potential at RUN/SS controls the slew rate at COMP1.

FB1 (Pin 11/Pin 8): Channel 1 Controller Error Amplifier Input. FB1 should be connected through a resistive divider network to V_{OUT1} to set the channel 1 switcher output voltage. Also, connect the channel 1 switcher loop compensation network to FB1.

SGND (Pin 12/Pin 9): Signal Ground. All the internal low power circuitry returns to the SGND pin. Connect to a low impedance ground, separated from the PGND node. All feedback, compensation and soft-start connections should return to SGND. SGND and PGND should be connected only at a single point, near the PGND pin and the negative terminal of the V_{IN} bypass capacitor.

FCB (Pin 13/Pin 10): Force Continuous Bar. Internally pulled high. When FCB is shorted to GND, the controller forces both converters to maintain continuous synchronous operation regardless of load current.

EXTREF (Pin 11, QFN Package Only): External Reference. The EXTREF pin and the internal bandgap voltage are used as the switcher control loop's reference in a diode OR manner. If the potential at the EXTREF pin is less than 0.6V, it overrides the internal reference and lowers the switcher output voltages. If EXTREF potential is more than 1V, the internal bandgap voltage controls both channel output voltages. EXTREF has no effect on the PGOOD threshold. EXTREF is internally connected to the RUN/SS pin in the GN28 package.

RUN/SS (Pin 14/Pin 12): Run Control and Soft-Start Input. An internal 7μA current source pull-up and an external capacitor to ground at this pin sets the start-up delaly (approximately 300ms/μF), the output ramp rate and the time delay for soft current limit. Forcing this pin below 0.8V with an open-drain/collector transistor shuts down the device. Pulling RUN/SS high with a current greater than 10μA can result in malfunctioning of tracking during start-up. Pulling RUN/SS high with currents higher than 50μA can interfere with current limit protection.

PGOOD (Pin 15/Pin 13): Open-Drain Power Good Output. PGOOD is pulled to ground under shutdown condition or when any switcher output voltage is not within ±10% of its set point .

V_{INFF} (Pin 16/Pin 14): Line Feedforward Compensation Input. Connects to the V_{IN} power supply to provide line feedforward compensation. A change in V_{IN} immediately modulates the input to the PWM comparator and changes the pulse width in an inversely proportional manner, thus bypassing the feedback loop and providing excellent transient line regulation. V_{INFF} is a sensitive pin, an external lowpass filter can be added to this pin to prevent noisy signals from affecting the loop gain.

PIN FUNCTIONS (28-Pin SSOP/32-Pin QFN Package)

PHASEMD (Pin 17/Pin 15): Phase Selector Input. This pin determines the phase relationships between controller 1, controller 2 and the PLLIN signal. When PHASEMD is floating, its value is around 2V, and the internal phase-locked loop synchronizes the falling edge of TG1 to the falling edge of the PLLIN signal. When PHASEMD is forced high, PLLIN leads TG1 by 90°. TG1 and TG2 remain at 180° out of phase independent of the PHASEMD input. When PHASEMD is forced low, an internal current source discharges the RUN/SS slowly to provide power down tracking. Avoid coupling noise into this sensitive pin.

FB2 (Pin 18/Pin 16): Channel 2 Controller Error Amplifier Input. See FB1.

COMP2 (Pin 19/Pin 17): Channel 2 Controller Error Amplifier Output. See COMP1.

V_{CC} (Pin 20/Pin 18): Power Supply Input. All the internal circuits except the switcher output drivers are powered from this pin. V_{CC} should be connected to a low noise 5V supply and should be bypassed to SGND with at least a 10µF capacitor in close proximity to the LTC3802.

CMPIN2 (Pin 21/Pin 19): Channel 2 Controller Comparators Input. See CMPIN1.

I_{MAX2} (Pin 22/Pin 20): Channel 2 Controller Current Limit Set. See I_{MAX1}.

PLLLPF (Pin 23/Pin 21): Phase-Locked Loop Lowpass Filter. The phase-locked loop's lowpass filter is tied to this pin. Alternatively, this pin can be driven with an AC or DC voltage source to vary the frequency of the internal oscillator.

PLLIN (Pin 24/Pin 22): Phase-Locked Loop Input/External Synchronization Input to the Phase Detector. The falling edge of this signal is used for frequency synchronization. When PLLIN floats or shorts to ground, the controllers free run at 550kHz.

SW2 (Pin 25/Pin 25): Channel 2 Controller Switching Node. See SW1.

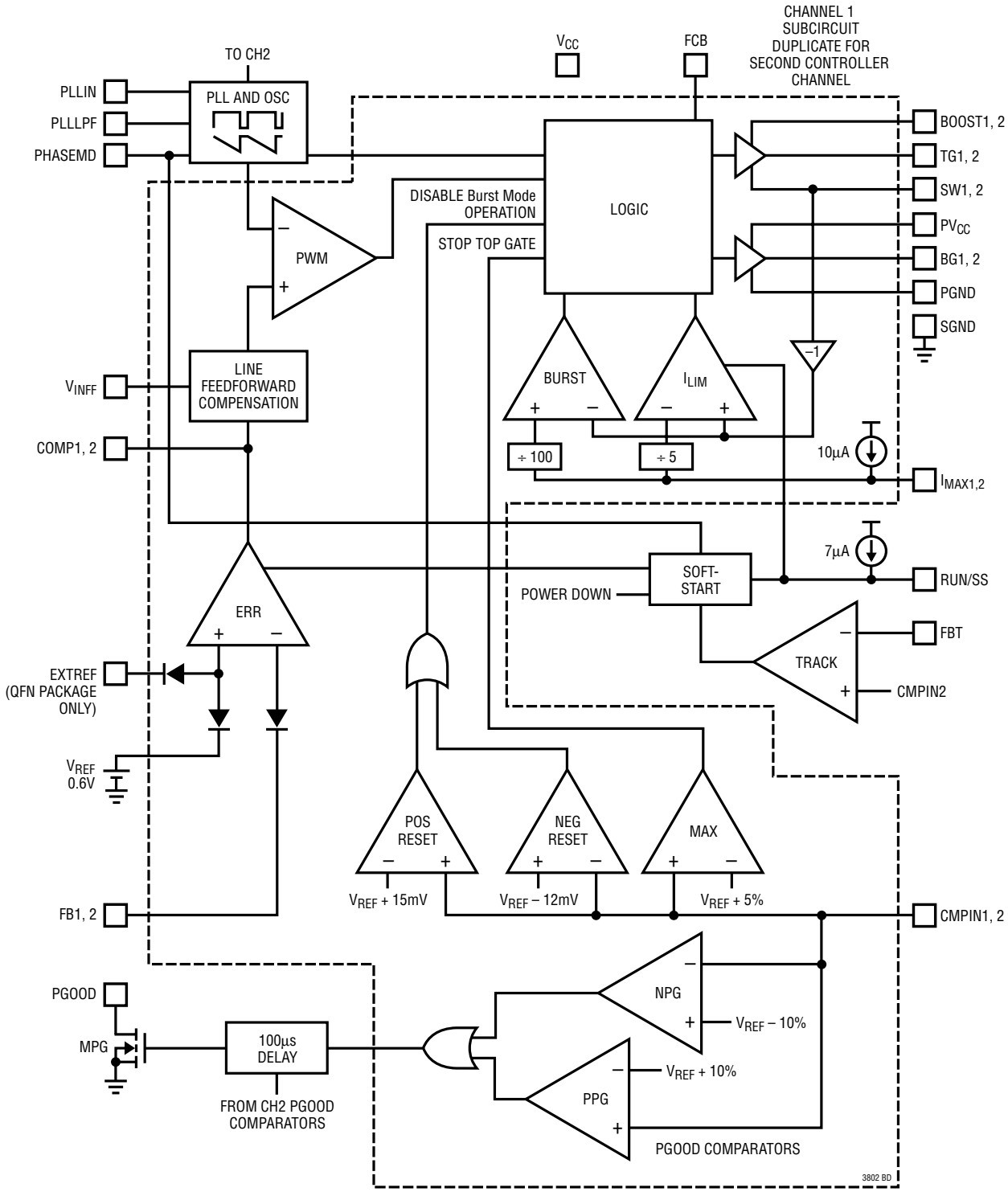
TG2 (Pin 26/Pin 26): Channel 2 Controller Top Gate Drive. See TG1.

BOOST2 (Pin 27/Pin 27): Channel 2 Controller Top Gate Driver Supply. See BOOST1.

BG2 (Pin 28/Pin 28): Channel 2 Controller Bottom Gate Drive. See BG1.

Exposed Pad (Pin 33, QFN Package Only): Exposed Pad is PGND, must be soldered to PCB.

BLOCK DIAGRAM



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Switching Architecture

The LTC3802 includes two step-down (buck) voltage mode feedback switching regulator controllers. These two controllers act independently of each other except at start-up and current limit. For proper power-up sequencing, channel 1 is designated to be the **higher** output voltage channel (see Start-Up Tracking).

Each channel uses two external sychronous N-channel MOSFETs. A floating topside driver and a simple external charge pump provide full gate drive to each upper MOSFET. The controller uses leading edge modulation architecture to allow extremely low duty cycle and fast load recovery operation. In a typical LTC3802 switching cycle, the PWM comparator turns on the top MOSFET and charges up the output capacitor. Some time later, an internal clock resets the top MOSFET, turns on the bottom MOSFET and reduces the output charging current. The top gate duty cycle is controlled by the feedback amplifier, which compares the divided output voltage with an internal reference. This switching cycle repeats itself at a fixed 550kHz frequency or in synchronization with an external oscillator.

The internal master clock runs at 550kHz, turning off the top gate once every 1.8µs. Thus, feedback loop components and output inductors and capacitors can be scaled to a particular operating frequency. Noise generated by the circuit will always be in a known frequency band, with the 550kHz frequency designed to leave the 455kHz IF band free of interference. Subharmonic oscillation and slope compensation, common headaches with constant frequency current mode switchers, are absent in voltage mode designs like the LTC3802. Two LTC3802 channels run from a common clock, with the phasing chosen to be 180° from channel 1 to channel 2. This has the effect of doubling the frequency of the switching pulses seen by the input bypass capacitor, significantly lowering its RMS current and reducing the capacitance required.

Feedback Control

Each LTC3802 channel senses the output voltage at V_{OUT} with an internal feedback op amp (see Block Diagram). This is a real op amp with a low impedance output, 80dB open-loop gain and 10MHz gain-bandwidth product. The positive input is connected to a level-shifted internal 600mV reference, while the negative input is connected to the level-shifted FB pin. The output is connected to COMP, which is in turn connected to the line feedforward circuit and from there to the PWM generator. To speed up the overshoot recovery time, the maximum potential at the COMP pin is internally clamped at a level corresponding to the maximum top gate duty cycle. Under start-up conditions, RUN/SS controls the COMP pin slew rate.

At steady state, as shown in Figure 1, the output of the switching regulator is given the following equation

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R1}{R_B}\right)$$

Unlike many regulators that use a transconductance (g_m) amplifier, the LTC3802 is designed to use an inverting summing amplifier topology with the FB pin configured as a virtual ground. This allows the feedback gain to be tightly controlled by external components, which is not possible with a simple g_m amplifier. In addition, the voltage feedback amplifier allows flexibility in choosing pole and zero locations. In particular, it allows the use of "Type 3" compensation, which provides a phase boost at the LC pole frequency and significantly improves the control loop phase margin.

In a typical LTC3802 circuit, the feedback loop consists of the line feedforward circuit, the modulator, the external inductor, the output capacitor and the feedback amplifier with its compensation network. All these components affect loop behavior and need to be accounted for in the loop compensation. The modulator consists of the PWM generator, the output MOSFET drivers and the external MOSFETs themselves. The modulator gain varies linearily with the input voltage. The line feedforward circuit compensates for this change in gain, and provides a constant gain from the error amplifier output to the inductor input regardless of input voltage. From a feedback loop point of view, the combination of the line feedforward circuit and the modulator looks like a linear voltage transfer function from COMP to the inductor input and has a gain roughly equal to 22V/V. It has fairly benign AC behavior at typical loop compensation frequencies with significant phase shift appearing at half the switching frequency.

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The external inductor/output capacitor combination makes a more significant contribution to loop behavior. These components cause a second order LC roll-off at the output with 180° phase shift. This roll-off is what filters the PWM waveform, resulting in the desired DC output voltage, but this phase shift causes stability issues in the feedback loop and must be frequency compensated. At higher frequencies, the reactance of the output capacitor will approach its ESR, and the roll-off due to the capacitor will stop, leaving –20dB/decade and 90° of phase shift.

Figure 1 shows a Type 3 amplifier. The transfer function of this amplifier is given by the following equation:

$$\frac{V_{COMP}}{V_{OUT}} = \frac{-(1+sC1R2)[1+s(R1+R3)C3]}{sR1(C1+C2)[1+s(C1//C2)R2](1+sC3R3)}$$

The RC network across the error amplifier and the feedforward components R3 and C3 introduce two pole-zero pairs to obtain a phase boost at the system unity gain frequency, f_C. In theory, the zeros and poles are placed symmetrically around f_C, and the spread between the zeros and the poles is adjusted to give the desired phase boost at f_C. However, in practice, if the crossover frequency is much higher than the LC double-pole frequency, this method of frequency compensation normally generates a phase dip within the unity bandwidth and creates some concern regarding conditional stability.

If conditional stability is a concern, move the error amplifier's zero to a lower frequency to avoid excessive phase dip. The following equations can be used to compute the feedback compensation components value:

f_{SW} = Switching frequency

$$f_{LC} = \frac{1}{2\pi\sqrt{LC_{OUT}}}$$

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}}$$

choose:

$$f_C = \text{Crossover frequency} = \frac{f_{SW}}{10}$$

$$f_{Z1(ERR)} = f_{LC} = \frac{1}{2\pi R2C1}$$

$$f_{Z2(RES)} = \frac{f_C}{5} = \frac{1}{2\pi(R1+R3)C3}$$

$$f_{P1(ERR)} = f_{ESR} = \frac{1}{2\pi R2(C1//C2)}$$

$$f_{P2(RES)} = 5f_C = \frac{1}{2\pi R3C3}$$

Required error amplifier gain at frequency f_C:

$$\approx 40\log\sqrt{1+\left(\frac{f_C}{f_{LC}}\right)^2} - 20\log\sqrt{1+\left(\frac{f_C}{f_{ESR}}\right)^2} - 20\log(A_{MOD})$$

$$\approx 20\log\frac{R2}{R1}\bullet\frac{\left(1+\frac{f_{LC}}{f_C}\right)\left(1+\frac{f_{P2(RES)}}{f_C}+\frac{f_{P2(RES)}-f_{Z2(RES)}}{f_{Z2(RES)}}\right)}{\left(1+\frac{f_C}{f_{ESR}}+\frac{f_{LC}}{f_{ESR}-f_{LC}}\right)\left(1+\frac{f_{P2(RES)}}{f_C}\right)}$$

where A_{MOD} is the modulator and line feedforward gain and is equal to:

$$A_{MOD} \approx \frac{V_{IN(MAX)}\bullet DC_{MAX}}{V_{SAW}} = \frac{30\bullet 0.89}{1.2} \approx 22V/V$$

Once the value of resistor R1, poles and zeros location have been decided, the value of R2, C1, C2, R3 and C3 can be obtained from the above equations.

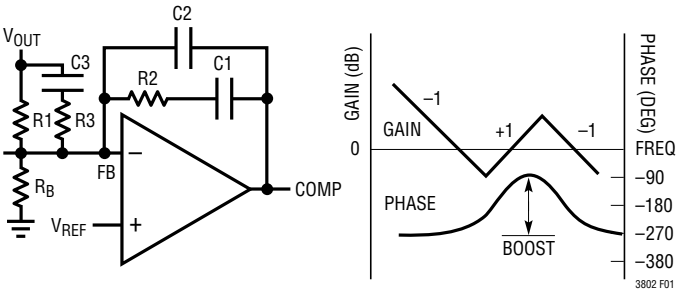

Figure 1. Type 3 Amplifier Compensation

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Compensating a switching power supply feedback loop is a complex task. The applications shown in this data sheet show typical values, optimized for the power components shown. Though similar power components should suffice, substantially changing even one major power component may degrade performance significantly. Stability also may depend on circuit board layout. To verify the calculated component values, all new circuit designs should be prototyped and tested for stability.

Overvoltage Protection and Power Good Flag

Notice that the FB pin is the feedback amplifier's virtual ground node (offset by V_{REF}). Because the typical compensation network does not include local DC feedback around the amplifier, the DC level at FB will be an accurate replica of the output voltage, divided down by the resistive divider. However, the compensation capacitors will tend to attenuate AC signals at FB, especially during quick transients. Because of this delay in the servo loop, the duty cycle is not able to adjust immediately to shifts in the output voltage. This problem is most apparent at high input and low output voltages. Under transient conditions, a slow reaction in the duty cycle could cause a large step in the output voltage. The LTC3802 avoids this voltage instability through the use of an additional comparator input pin, CMPIN, which provides real time measurement of the output voltage. A duplicate FB divider, R1 and R_B should be connected to this pin. A small feedforward capacitor can be added across the top resistor to speed up the comparators.

The MAX comparator monitors the output voltage through the CMPIN pin. If the output moves 5% above its nominal value, the comparator immediately turns the top MOSFET (QT) off and the bottom MOSFET (QB) on and maintains this state until the output falls back within 5% of its nominal value. This pulls the output down as fast as possible, preventing damage to the (often expensive) load. If CMPIN rises because the output is shorted to a higher supply, QB will stay on until the short goes away, the higher supply current limits or QB dies trying to save the load. This behavior provides maximum protection against overvoltage fault at the output, while allowing the circuit to resume normal operation when the fault is removed.

CMPIN is also used as the input for the positive power good comparator PPG and the negative power good comparator NPG. The PPG comparator goes high if the potential at CMPIN is 10% above the nominal value. The NPG comparator fires if CMPIN potential is 10% lower than the nominal value. The output of PPG and NPG is connected to the PGOOD pin through the transistor MPG (see Block Diagram). PGOOD is an open-drain output and requires an external pull-up resistor. If channel 1 and 2 regulator output voltages are within ±10% of their nominal values, the transistor MPG shuts off and PGOOD is pulled high by the external pull-up resistor. If any of the two outputs is outside the 10% window for more than 100μs, PGOOD pulls low indicating that at least one output is out of regulation. For PGOOD to go high, both switcher outputs must be in regulation. PGOOD remains active during soft-start and current limit. Upon power-up, PGOOD is forced low. As soon as the RUN/SS pin rises above the shutdown threshold, the power good comparators take over and control the transistor MPG directly. The 100μs delay ensures that short output transient glitches that are successfully "caught" by the power good comparators don't cause momentary glitches at the PGOOD pin.

Current Limit Protection

The LTC3802 includes an onboard current limit circuit that limits the maximum output current to a user-programmed level. It works by sensing the voltage drop across QB when QB is on and comparing that voltage to a user-programmed voltage at I_{MAX}. The I_{MAX} pin includes a trimmed 10μA pull-up, enabling the user to set the voltage at I_{MAX} with a single resistor, R_{IMAX}, to ground. The current comparator reference input is equal to V_{IMAX} divided by 5 (see Block Diagram).

Any time QB is on and the current flowing to the output is reasonably large, the SW node at the drain of QB will be somewhat negative with respect to PGND. Since QB looks like a low value resistor during its on-time, the voltage drop across it is proportional to the current flowing in it. The LTC3802 senses this voltage, inverts it and compares it to the current comparator reference. The current comparator begins limiting the output current when the magnitude of the negative voltage is larger than its reference.

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The current limit detector is connected to an internal 100μA current source. Once current limit occurs, this current begins to discharge the soft-start capacitor at RUN/SS, reducing the duty cycle and controlling the output voltage until the current drops below the limit. The soft-start capacitor needs to move a fair amount before it has any effect on the duty cycle, adding a delay until the current limit takes effect. This allows the LTC3802 to experience brief overload conditions without affecting the output voltage regulation. The delay also acts as a pole in the current limit loop to enhance loop stability.

Under severe short-circuit conditions, if the load current is 1.5 times larger than the programmed current limit threshold, the LTC3802 shuts off the top MOSFET immediately. This stops the increase in the inductor current. At this moment, if CMPIN is 10% lower than its nominal value, the LTC3802 hard current limit latches and discharges the RUN/SS capacitor with a current source of more than 1mA until RUN/SS hits its shutdown threshold. Once RUN/SS is completely discharged, the LTC3802 cycles its soft-start again.

Programming the current limit on the LTC3802 is straightforward. To set the current limit, calculate the expected voltage drop across QB at the maximum desired current:

$$V_{PROG} = (I_{LIMIT})(R_{DS(ON)})$$

I_{LIMIT} should be set much higher than the expected operating current, to allow for MOSFET $R_{DS(ON)}$ changes with temperature. Power MOSFET $R_{DS(ON)}$ varies from MOSFET to MOSFET, limiting the accuracy obtainable from the LTC3802 current limit loop. Setting I_{LIMIT} to 150% of the maximum normal operating current is usually safe and will adequately protect the power components if they are chosen properly. Note that ringing on the switch node can cause an error for the current limit threshold. This factor will change depending on the layout. The SW node should have minimum routing from the MOSFETs to the LTC3802 to reduce parasitic inductor and hence ringing. V_{PROG} is then programmed at the I_{MAX} pin using the internal 10μA pull-up current and an external resistor:

$$R_{IMAX} = \frac{5 \bullet V_{PROG}}{10\mu A}$$

The resulting value of R_{IMAX} should be checked in an actual circuit to ensure that the current circuit kicks in as expected. Circuits that use very low values for R_{IMAX} (<25k) should be checked carefully, since small changes in R_{IMAX} can cause large I_{LIMIT} changes when the switch node ringing makes up a large percentage of the total V_{PROG} value. If V_{PROG} is set too low, the LTC3802 may fail to start up. The LTC3802 current limit is designed primarily as a disaster preventing, "no blow up" circuit, and is not useful as a precision current regulator.

The LTC3802 bottom MOSFET V_{DS} current sensing architecture not only eliminates the external current sense resistors and the corresponding power losses in the high current paths, it allows a wide range of output voltage setting, including extremely low duty cycle operation. On the other hand, for high input voltage with small output inductance applications, care must be taken to avoid inductor saturation during dead-short conditions. As soon as the output short circuits, the controller instantaneously enters maximum duty cycle operation.

During the top MOSFET on interval, the current comparator is not monitoring the current and there is no current limit action until the bottom MOSFET turns on and the inductor current exceeds its hard current limit threshold. Typically, the top MOSFET and the inductor need to withstand one clock period of transient high current operation until the hard current limit operation engages. Peak currents can exceed 6 times the maximum DC output current during this period. Most MOSFETs allow 10μs of high current and this short duration of current should not damage the MOSFET. Nevertheless, it is a good idea to reduce the peak inductor current. This can be achieved by having a larger inductance to limit the short-circuit current slew rate, or an inductor with a saturation current that is higher than the hard current limit threshold. Alternatively, an inductor core material with a softer saturation characteristic such as iron powder can be used.

Shutdown/Soft-Start

The RUN/SS pin performs two functions: when pulled to ground it shuts down the LTC3802, and it acts as a conventional soft-start pin, enforcing a maximum duty cycle limit proportional to the voltage at RUN/SS. An

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internal 7μA current source pull-up is connected to the RUN/SS pin, allowing a soft-start ramp to be generated with a single external capacitor to ground. The 7μA current source is active even when the LTC3802 is shut down, ensuring the device will start when the external pull-down at RUN/SS is released. Under shutdown conditions, the LTC3802 goes into a micropower sleep mode, and the quiescent current drops to 100μA.

The RUN/SS pin shuts down the LTC3802 when it falls below 0.8V (Figure 2). Between about 0.8V and 2V, the LTC3802 wakes up and the duty cycle is kept to a miminum. As the potential at RUN/SS goes higher, the duty cycle increases linearly between 2V and 3.2V, reaching its final value of 89% when RUN/SS exceeds 3.2V. Prior to this point, the feedback amplifier will assume control of the loop and the output will come into regulation. Note that the RUN/SS linear range varies with the potential at V_{INFF}; for 5V input voltage, the RUN/SS active range reduces to 2V-2.25V.

The value of the soft-start capacitor, C_{SS}, may depend on the input and output voltages, inductor value, output capacitance and load current. The inductor's start-up current (from V_{OUT} = 0V), can be much higher than its steady-state current. The difference depends on the input power supply slew rate, the input and output voltages, the LTC3802 soft-start slew rate, and the inductor and output capacitor values.

For a given application, the known input and output requirements determine the output inductor and capacitor values. These values establish the transient load recovery time. In general, a low value inductor combined with a high value capacitor yields a short transient load recovery time at the expense of higher inductor ripple and start-up current. These components, together with a small soft-start capacitor, can also cause high inrash current. This triggers the LTC3802 current limit comparator and forces the LTC3802 to repeat the soft-start cycle, never allowing the supply to start.

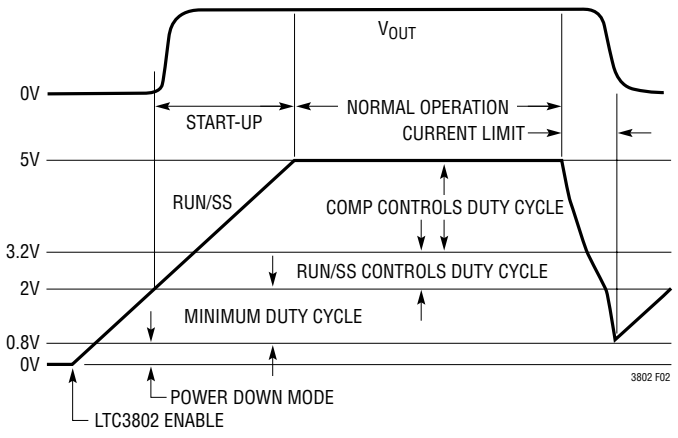

Figure 2. Soft-Start Operation in Start-Up and Current Limit

Start-up problems can also occur when a small soft-start capacitor is used with a small output inductor and capacitor. High input voltages generate high inrash currents, charging the output capacitor quickly and causing the output to overshoot. The LTC3802 OVP comparator turns off the top MOSFET once the output is 5% higher than its nominal value. However, the residual energy in the inductor will continue to charge the output capacitor, forcing the output voltage to increase further until the inductor energy is depleted. This overshoot at the output causes the feedback loop to operate nonlinearly; the output tends to ring for several cycles until the loop mechanism is restored.

Therefore, select C_{SS} with start-up in mind. Choosing C_{SS} to ensure that there is no output overshoot and the inrush current is not able to trigger the current comparator. A minimum recommended soft-start capacitor of C_{SS} = 0.1μF will be sufficient for most applications.

Undervoltage Lockout

The LTC3802 is designed for wide V_{IN} operation. The internal UVLO circuit monitors the V_{CC} and V_{INFF} potential and starts operation as long as they are above their 2.5V UVLO thresholds. For high V_{IN} supply operation, the low UVLO threshold should not cause any problem under typical application conditions. Upon power-up, once the V_{IN} potential is higher than the UVLO threshold, the LTC3802 releases the RUN/SS node and allows the start-up current to charge the soft-start capacitor. The time interval for the RUN/SS potential to ramp from 0.8V to 2V allows the V_{IN} supply to slew to its steady-state potential. A 0.1μF soft-start capacitor creates a 17ms time delay before the driver starts switching. Most power supplies have a start-up time well within this time interval. For some

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special power supplies with a slow start-up slew rate, the LTC3802 drivers might start switching before the input supply reaches its steady-state value. The high inrush current through the input power cable might cause the V_{IN} supply to dip below the UVLO threshold and cause start-up problems. Figure 3 shows a simple circuit to fix this problem. The selection of the zener voltage allows the V_{IN} UVLO trip point to be programmed externally.

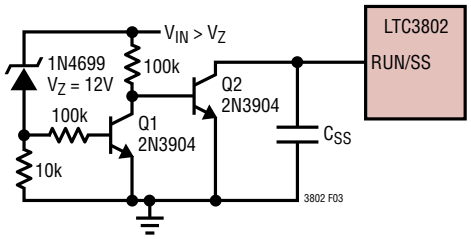

Figure 3. External UVLO Setting

Start-Up Tracking

Many DSP chips, microprocessors, FPGAs and ASICs require multiple power supplies for the core and I/O sections. Internally, the core and I/O blocks are isolated by structures which may become forward biased if the supply voltages are not at specified levels. During power-up and power-down operations, differences in the starting point and ramp rates of the two supplies may cause current to flow between the isolation structures which, when prolonged and excessive, can reduce the useable life of the semiconductor device. These currents can also trigger latch-up in devices, leading to device failure.

Of greater concern than internal isolation of core and I/O structures are system-level concerns, such as bus contention between the I/O pins of the DSP and external peripheral devices. Power supply sequencing between the core and I/O may be required to prevent bidirectional I/O pins of the DSP and a peripheral device from opposing each other. Since the bus control logic originates in the core section, powering the I/O prior to the core may cause the DSP and peripheral pins to be configured simulatneously as outputs. If the data values on each side are opposing, then the output drivers contend for control, causing excessive current flow and eventually device failure.

The LTC3802 can be configured to give two different power-up/power-down slew rates to meet different application requirements: ratiometric and coincident tracking configurations (Figure 4). With a ratiometric configuration, the LTC3802 produces two different output slew rates (with $V_{OUT1} > V_{OUT2}$). Because each channel's slew rate is proportional to its corresponding output voltage, the two output voltages reach their steady-state value at about the same time. The coincident configuration produces the same slew rate at both outputs, so that the lower output voltage channel reaches its steady state first.

Figure 4 shows the simplified schematic to realize this power-up function. During power-up, the tracking amplifier TRACK servos the tracking feedback loop and forces FBT to be at the same potential as CMPIN2.

For ratiometric start-up, set:

$R_{T5} = R51$

or remove resistors R_{T4} and R_{T5} and short FBT to CMPIN1. At power-up, if the channel 2 output voltage slew rate is too fast, or CMPIN2 is higher than FBT, the tracking amplifier will force a smaller channel 2 duty cycle. Channel 1's duty cycle is controlled by the RUN/SS pin and is not affected by the tracking amplifier.

For coincident start-up, set:

$R_{T5} = R52$

During power-up, if the channel 1 output voltage is higher than that of channel 2, or if FBT is higher than CMPIN2, the tracking amplifier TRACK starts to discharge the C_{SS} capacitor and forces both channels to have the same duty cycle and output voltage. The tracking amplifier stops discharging once channel 2 reaches its negative power good threshold.

To have the proper power-down sequence, ground the PHASEMD pin. This turns on an internal current source which slowly discharges the soft-start capacitor. Once the RUN/SS potential is low enough to control the duty cycle, the tracking amplifier takes control and servos the feedback loop to produce the selected output ramp. The LTC3802 tracking function can be easily disabled by disconnecting the FBT resistive divider and shorting FBT to CMPIN2.

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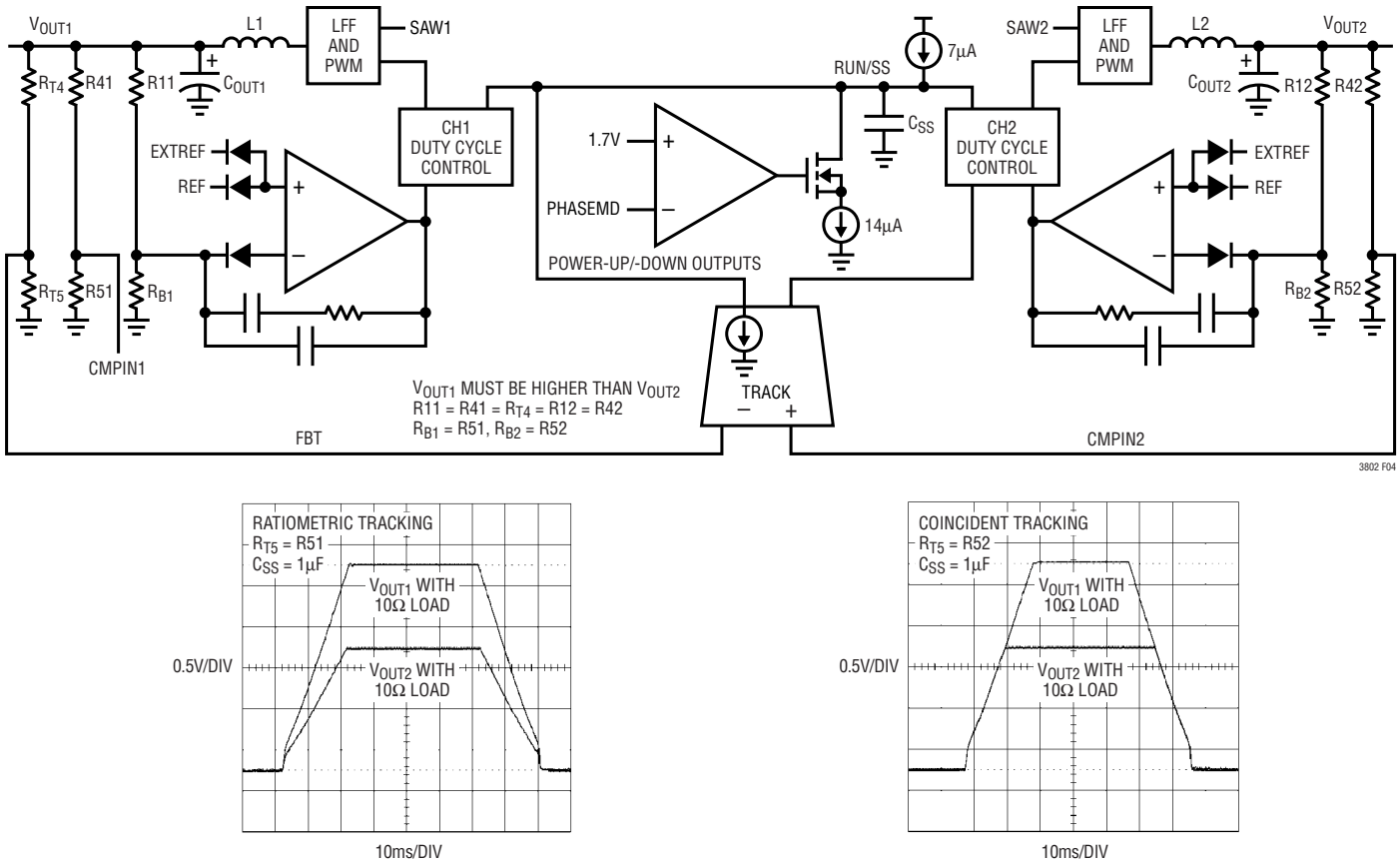

Figure 4. Simplified Power-Up/Power-Down Output Tracking Schematic

The QFN version of the LTC3802 provides an additional reference pin for external ratiometric start-up. If the potential at the EXTREF pin is less than 0.6V, it overrides the internal reference. This pin can be connected to an external ramp to control the output slew rate. If external tracking is not required, connect EXTREF to a potential somewhat larger than 0.6V or short EXTREF to the RUN/SS pin. The EXTREF pin should never be allowed to float. In the GN28 package, EXTREF is internally shorted to the RUN/SS pin.

Burst Mode Operation

The LTC3802 switcher supply has two modes of operation. Under heavy loads, it operates as a fully synchronous, continuous conduction switching regulator. In this mode of operation (continuous mode), the current in the inductor flows in the positive direction (towards the output) during the entire switching cycle, constantly supplying current to the load. In this mode, the synchronous switch (QB) is on whenever QT is off, so the current always flows through a low impedance switch, minimizing voltage drop and power loss. This is the most efficient mode of operation at heavy loads, where the resistive losses in the power devices are the dominant loss term.

Continuous mode works efficiently when the load current is greater than half of the ripple current in the inductor. In a buck converter like the LTC3802, the average current in the inductor (averaged over one switching cycle) is equal to the load current. The ripple current is the difference between the maximum and the minimum current during a switching cycle (see Figure 5a). The ripple current depends on inductor value, clock frequency and output voltage, but is constant regardless of load as long as the LTC3802 remains in continuous mode. See the Inductor Selection section for a detailed description of ripple current.

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As the output load current decreases in continuous mode, the average current in the inductor will reach a point where it drops below half the ripple current. At this point, the current in the inductor will reverse during a portion of the switching cycle, or begin to flow from the output back to the input. This does not adversely affect regulation, but does cause additional losses as a portion of the inductor current flows back and forth through the resistive power switches, giving away a little more power each time and lowering the efficiency. There are some benefits to allowing this reverse current flow: the circuit will maintain regulation even if the load current drops to zero and the output ripple voltage and frequency remain constant at all loads, easing filtering requirements. However, continuous mode at low output current does cause losses in efficiency. A portion of the inductor current flows back and forth through the resistive power switches, causing I^2R losses. The drivers continue to switch QT and QB on and off once a cycle. Each time an external MOSFET is turned on, the internal driver must charge its gate to a potential above the MOSFET's source voltage; when the MOSFET is turned off, that charge is lost to ground or SW. At the high switching frequencies, the lost gate charges can add up to tens of millicoulombs. As the load current continues to drop, these charges quickly become the dominant power loss term, reducing efficiency once again.

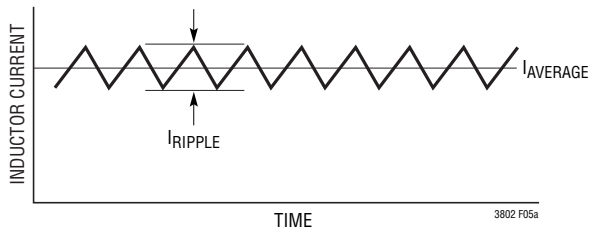

Figure 5a. Continuous Mode

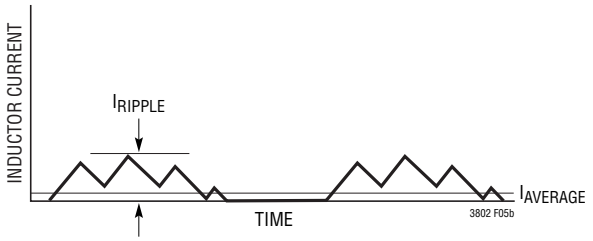

Figure 5b. Burst Mode Operation

To minimize the switching loss and reverse current flow at light loads, the LTC3802 switches to a second mode of operation: Burst Mode operation (Figure 5b). In Burst Mode operation, at the end of the QB cycle, if the inductor current approaches zero or goes negative, the LTC3802 turns off both drivers. The actual cutoff threshold is proportional to the I_{MAX} setting and is equal to:

$$-\frac{V_{IMAX}}{100} - 3mV$$

The –3mV built-in offset overcomes the random mismatch in the burst compararator trip point and allows Burst Mode operation at no load.

Once both MOSFETs shut off, the voltage at the SW pin will float around V_{OUT}, and the inductor current and the voltage across the inductor will be close to zero. This prevents current from flowing backwards in QB, eliminating that power loss term.

The moment the LTC3802 enters Burst Mode operation, both drivers skip a number of switching cycles until the internal 36µs timeout forces the switcher to return to continuous operation. This timeout eliminates the audible noise from certain types of inductors when they are lightly loaded. After the 36µs timeout, the LTC3802 forces one continuous mode cycle and checks the inductor current at the end of the period. If it is still too small, it enters Burst Mode operation again. This pattern repeats until the output is loaded. The LTC3802 returns to continuous mode operation if it detects that CMPIN potential is 12mV below or 15mV above its nominal bandgap voltage. Immediately after returning to continuous mode operation, the regulator output might continue to droop slightly until the feedback loop responds and requests an increase in duty cycle. During sudden transient steps, the regulator output ripple is limited by the feedback loop transient response and is independent of the mode of operation.

The small 15mV and –12mV offset at the POS and NEG RESET comparators ensure that after a transient load step, the LTC3802 returns to continuous mode quickly. This minimizes the output ripple under Burst Mode operation. For proper Burst Mode operation, the LTC3802 requires very precise CMPIN and FB sensing. To realize this, CMPIN and FB must use the same resistive divider values

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and all resistors should have better than 1% tolerance. If this is not possible and Burst Mode operation is required, the potential at CMPIN can be set slightly higher than FB by using a slightly bigger resistor from CMPIN to ground. This removes the requirement of having expensive resistors at the FB and CMPIN pins, at the expense of having a higher Burst Mode ripple and slightly different overvoltage and power good thresholds. To ensure clean Burst Mode operation, the CMPIN and FB resistive divider requires good layout technique. Both resistive dividers must be connected to the same nodes and away from high current paths.

Low load current efficiency depends strongly on proper Burst Mode operation. In an ideal system, the gate drive is the dominant loss term at low load currents. Burst Mode operation turns off all output switching for several clock cycles in a row, significantly cutting gate drive losses. As the load current in Burst Mode operation falls toward zero, the current drawn by the LTC3802 falls to a quiescent level—about 6.5mA. To maximize low load efficiency, make sure the LTC3802 is allowed to enter Burst Mode operation as cleanly as possible.

Operating Frequency/Frequency Synchronization

The LTC3802 controller uses a constant frequency, phase-lockable internal oscillator with its frequency determined by an internal capacitor. This capacitor is charged by a fixed current plus an additional current that is proportional to the voltage applied to the PLLLPF pin. When the PLLIN pin is not used, an internal pull-down current source forces PLLIN to ground and the controller runs at a fixed 550kHz switching frequency.

The phase-locked loop allows the internal oscillator to be synchronized to an external source via the PLLIN pin. The phase-locked loop consists of an internal voltage controlled oscillator, a divide by 12 frequency divider and a phase detector. The voltage controlled oscillator monitors the output of the phase detector at the PLLLPF pin. It provides a linear relationship between the PLLLPF potential and the master oscillator frequency. A DC voltage input from 0.5V to 1.9V corresponds to a 330kHz to 750kHz master switching frequency.

The phase detector used is an edge sensitive digital circuit which provides zero degree phase shift between the external and internal oscillators. This type of phase detector will not lock up on an input frequency close to the harmonics of the VCO center frequency. The output of the phase detector is a complementary pair of current sources charging or discharging the external filter network on the PLLLPF pin. A simplified block diagram is shown in Figure 6.

If the external frequency, f_{PLLIN}, is greater than the oscillator frequency, f_{OSC}, current is sourced continuously, pulling up the PLLLPF pin. When f_{PLLIN} is less than f_{OSC}, current is sunk continuously, pulling down the PLLLPF pin. If f_{PLLIN} and f_{OSC} are the same but exhibit a phase difference, the current sources turn on for a period corresponding to the phase difference. Thus the voltage on the PLLLPF pin is adjusted until the phase and frequency of the external and internal oscillators are identical. At this stable operating point the phase comparator output is open and the filter capacitor, C_{LP}, holds the voltage. When locked, the PLL aligns the turn off of the top MOSFET to the falling edge of the synchronizing signal.

The loop filter components, C_{LP} and R_{LP}, smooth out the current pulses from the phase detector and provide a stable input to the voltage controlled oscillator. The filter components, C_{LP} and R_{LP}, determine how fast the loop acquires lock. Typically R_{LP} = 10k and C_{LP} is between 0.01µF and 0.1µF.

The PHASMD pin determines the relative phases between the TG1, TG2 and the PLLIN signals. When PHASEMD is

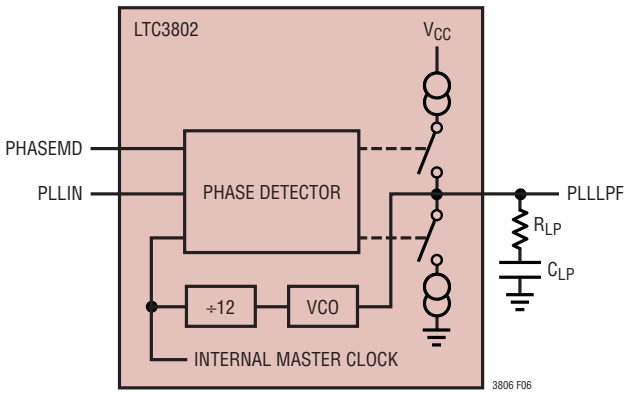

Figure 6. Phase-Locked Loop Block Diagram

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floating, it sits at around 2V and the internal phase-locked loop synchronizes TG1's falling edge to the falling edge of the PLLIN signal. When PHASEMD is high, these two signals are 90° out of phase. TG1 and TG2 remains 180° out of phase independent of PHASEMD input.

The PHASEMD signal together with the PLL circuit can be used to synchronize an additional LTC3802 power supply circuit to provide a 4-phase, 4-output solution. Compared to an in-phase multiple controller solution, the LTC3802's 4-phase design reduces the input capacitor ripple current requirements and efficiency losses because the peak current drawn from the input capacitor is spaced out within the switching cycle.

EXTERNAL COMPONENTS SELECTION

V_{CC} and PV_{CC} Power Supplies

Power for the top and bottom MOSFET drivers is derived from the PV_{CC} pin; the internal controller circuitry is derived from the V_{CC} pin. Under typical operating conditions, the total current consumption at these two pins should be well below 100mA. Hence, PV_{CC} and V_{CC} can be connected to an external auxiliary 5V power supply. If an auxiliary supply is not available, a simple zener diode and a darlington NPN buffer can be used to power up these two pins as shown in Figure 7. To prevent switching noise from coupling to the sensitive analog control circuitry, V_{CC} should

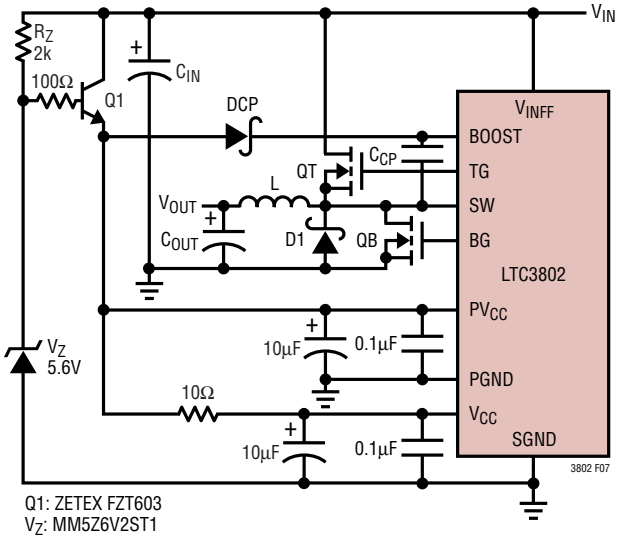

Figure 7. LTC3802 Power Supply Inputs

have a 10µF bypassed capacitor close to the device. The BiCMOS process that allows the LTC3802 to include large on-chip MOSFET drivers also limits the maximum PV_{CC} and V_{CC} voltage to 7V. This limits the practical maximum auxiliary supply to a loosely regulated 7V rail. If V_{CC} drops below 2.5V or PV_{CC} drops below V_{CC} by more than 1V, the LTC3802 goes into undervoltage lockout and prevents the power switches from turning on.

Top MOSFET Driver Supply

An external bootstrap capacitor, C_{CP}, connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. This capacitor is charged through diode DCP from PV_{CC} when the switch node is low. When the top MOSFET turns on, the switch node rises to V_{IN} and the BOOST pin rises to approximately V_{IN} + PV_{CC}. The boost capacitor needs to store about 100 times the gate charge required by the top MOSFET. In most applications a 0.1µF to 1µF, X5R or X7R dielectric capacitor is adequate.

Power MOSFET Selection

The LTC3802 requires two external N-channel power MOSFETs, one for the top (main) switch and one for the bottom (synchronous) switch. Important parameters for the power MOSFETs are the threshold voltage $V_{(GS)TH}$, breakdown voltage $V_{(BR)DSS}$, maximum current $I_{DS(MAX)}$, on-resistance $R_{DS(ON)}$ and input capacitance.

The gate drive voltage is set by the 5V PV_{CC} supply. Consequently, logic-level threshold MOSFETs must be used in LTC3802 applications. If the PV_{CC} voltage is expected to drop below 5V, then sub-logic level threshold MOSFETs should be considered. Pay close attention to the $V_{(BR)DSS}$ specification, because most logic-level MOSFETs are limited to 30V or less. The MOSFETs selected should have a $V_{(BR)DSS}$ rating greater than the maximum input voltage and some margin should be added for transients and spikes. The MOSFETs selected should also have an $I_{DS(MAX)}$ rating of at least two times the maximum power stage output current. Still, this may not be a sufficient margin so it is advisable to calculate the MOSFET's junction temperature to ensure that it is not exceeded.

The LTC3802 uses the bottom MOSFET as the current sense element, particular attention must be paid to its

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on-resistance. MOSFET on-resistance is typically specified with a maximum value $R_{DS(ON)(MAX)}$ at 25°C. In this case, additional margin is required to accommodate the rise in MOSFET on-resistance due to self heating and higher ambient temperature:

$$R_{DS(ON)(MAX)}\,(T) = \rho_T \bullet R_{DS(ON)(MAX)}\,(25°C)$$

The ρ_T term is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically about 0.4%/°C as shown in Figure 8a. For a maximum junction temperature of 100°C, using a value ρ_T = 1.3 is reasonable.

MOSFET input capacitance is a combination of several components but can be taken from the typical "gate charge" curve included on most data sheets (Figure 8b). The curve is generated by forcing a constant input current into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time. The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain drops the voltage across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given V_{DS} drain voltage, but can be adjusted for different V_{DS} voltages by multiplying by the ratio of the application V_{DS} to the curve specified V_{DS} values. A way to estimate the C_{MILLER} term is to take the change in gate charge from points a and b on a manufacturers data sheet and divide by the stated V_{DS} voltage specified. C_{MILLER} is the most important selection criteria for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets. C_{RSS} and C_{OS} are specified sometimes but definitions of these parameters are not included.

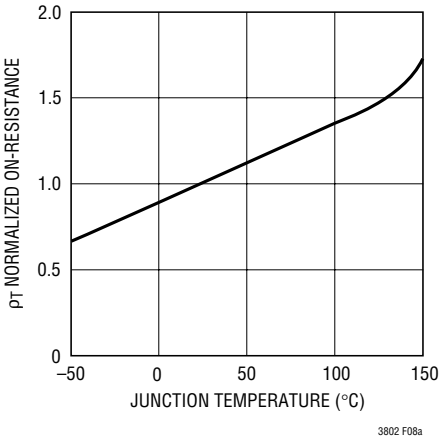

Figure 8a. Typical MOSFET $R_{DS(ON)}$ vs Temperature

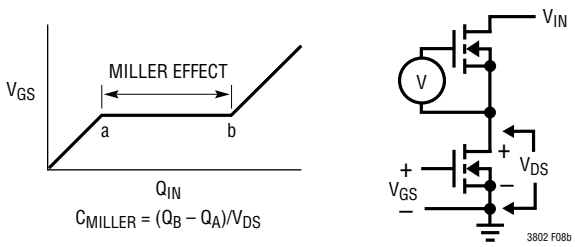

Figure 8b. Gate Charge Characteristics

When the controller is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Top Gate Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Bottom Gate Duty Cycle} = \left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

The power dissipation for the top and bottom MOSFETs at maximum output current are given by:

$$P_{TOP} = \frac{V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}{}^2\right)\left(\rho_{T(TOP)}\right)\left(R_{DS(ON)(MAX)}\right) + V_{IN}{}^2\left(\frac{I_{OUT(MAX)}}{2}\right)\left(R_{DR}\right)\left(C_{MILLER}\right)\bullet \left(\frac{1}{PV_{CC} - V_{TH(IL)}} + \frac{1}{V_{TH(IL)}}\right)\bullet f_{SW}$$

$$P_{BOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}{}^2\right)\left(\rho_{T(TOP)}\right)\left(R_{DS(ON)(MAX)}\right)$$

where:

R_{DR} = Effective top driver resistance

$V_{TH(IL)}$ = MOSFET data sheet specified typical gate threshold voltage at the specified drain current

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C_{MILLER} = Calulated Miller capacitance using the gate charge curve from the MOSFET data sheet

f_{SW} = Switching frequency

Both MOSFETs have conduction losses (I^2R) while the topside N-channel equation includes an additional term for transition losses, which peak at the highest input voltage. For $V_{IN} < 12V$, the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 12V$, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The bottom MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short circuit when the bottom switch is on close to 100% of the period.

Schottky Diode D1/D2 Selection

The Schottky diode D1 shown in Figure 7 conducts during the dead time between the conduction of the power MOSFET switches. It is intended to prevent the body diode of the bottom MOSFET from turning on and storing a charge during the dead time, which can cause a modest (about 1%) efficiency loss. The diode can be rated for about one half to one fifth of the full load current since it is on for only a fraction of the duty cycle. In order for the diode to be effective, the inductance between it and the bottom MOSFET must be as small as possible, mandating that these components be placed adjacently.

C_{IN} Selection

The input bypass capacitor in an LTC3802 circuit is common to both channels. The input bypass capacitor gets exercised in three ways: its ESR must be low enough to keep the supply drop low as the top MOSFETs turn on, its RMS current capability must be adequate to withstand the ripple current at the input, and the capacitance must be large enough to maintain the input voltage until the input supply can make up the difference. Generally, a capacitor (particularly a non-ceramic type) that meets the first two parameters will have far more capacitance than is required to keep capacitance-based droop under control.

The input capacitor's voltage rating should be at least 1.4 times the maximum input voltage. Power loss due to ESR occurs not only as I^2R dissipation in the capacitor itself, but also in overall battery efficiency. For mobile applications, the input capacitors should store adequate charge to keep the peak battery current within the manufacturer's specifications.

The input capacitor RMS current requirement is simplified by the multiphase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used to determine the maximum RMS current requirement. Increasing the output current drawn from the other out-of-phase controller will actually decrease the input RMS ripple current from this maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

In continuous mode, the source current of the top N-channel MOSFET is approximately a square wave of duty cycle V_{OUT}/V_{IN}. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{OUT(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. The total RMS current is lower when both controllers are operating due to the interleaving of current pulses through the input capacitors. This is why the input capacitance requirement calculated above for the worst-case controller is adequate for the dual controller design.

Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

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Medium voltage (20V to 35V) ceramic, tantalum, OS-CON and switcher-rated electrolytic capacitors can be used as input capacitors, but each has drawbacks: ceramics have high voltage coefficients of capacitance and may have audible piezoelectric effects; tantalums need to be surge-rated; OS-CONs suffer from higher inductance, larger case size and limited surface mount applicability; and electrolytics' higher ESR and dryout possibility require several to be used. Sanyo OS-CON SVP, SVPD series; Sanyo POSCAP TQC series or aluminum electrolytic capacitors from Panasonic WA series or Cornel Dublilier SPV series, in parallel with a couple of high performance ceramic capacitors, can be used as an effective means of achieving low ESR and its big bulk capacitance goal for the input bypass.

C_{OUT} Selection

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The output ripple ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8 \bullet f_{SW} \bullet C_{OUT}} \right)$$

where ΔI_L is the inductor ripple current.

ΔI_L may be calculated using the equation:

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Since ΔI_L increases with input voltage, the output ripple voltage is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

Manufacturers such as Sanyo, Panasonic and Cornell Dublilier should be considered for high performance through-hole capacitors. The OS-CON semiconductor electrolyte capacitor available from Sanyo has a good (ESR)(size) product. An additional ceramic capacitor in parallel with OS-CON capacitors is recommended to offset the effect of lead inductance.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or transient current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer surface mount capacitors offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent output capacitor choices are the Sanyo POSCAP TPD, POSCAP TPB, AVX TPS, AVX TPSV, the Kemet T510 series of surface mount tantalums,Kemet AO-CAPs or the Panasonic SP series of surface mount special polymer capacitors available in case heights ranging from 2mm to 4mm. Other capacitor types include Nichicon PL series and Sprague 595D series. Consult the manufacturer for other specific recommendations.

Inductor Selection

The inductor in a typical LTC3802 circuit is chosen primarily for inductance value and saturation current. The inductor should not saturate below the hard current limit threshold.

The inductor value sets the ripple current, which is commonly chosen at around 40% of the anticipated full load current. Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency is obtained at low frequency with small ripple current. However, achieving high efficiency requires a large inductor and generates higher output voltage excursion during load transients. There is a tradeoff between component size, efficiency and operating frequency. Given a specified limit for ripple current, the inductor value can be obtained using the following equation:

$$L = \frac{V_{OUT}}{f_{SW} \bullet \Delta I_{L(MAX)}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right)$$

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy

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or Kool Mμ® cores. A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Panasonic, Coiltronics, Coilcraft and Toko.

PC Board Layout Checklist

When laying out the printed circuit board, start with the power device. Be sure to orient the power circuitry so that a clean power flow path is achieved. Conductor widths should be maximized and lengths minimized. After you are satisfied with the power path, the control circuitry should be laid out. It is much easier to find routes for the relatively small traces in the control circuits than it is to find circuitous routes for high current paths. After the layout, the following checklist should be used to ensure proper operation of the LTC3802.

1. Place the top N-channel MOSFETs QT1 and QT2 within 1cm of each other with a common drain connection at C_{IN}. Do not attempt to split the input decoupling for the two channels because doing so can create a resonant loop.
2. Place C_{IN}, C_{OUT}, the MOSFETs, Schottky diode and the inductor together in one compact area.
3. Split the signal and power grounds. The path formed by the top and bottom N-channel MOSFETs, Schottky diode, and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other. The combined LTC3802 signal ground pin and the ground return of C_{VCC} must return to the combined C_{OUT} (–) terminals. Use a modified "star ground" technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors, with tie-ins for the bottom of the V_{CC} decoupling capacitor, the bottom of the voltage feedback resistive divider and the SGND pin of the IC.
4. Keep the switching nodes (SW1, SW2), top gate nodes (TG1, TG2), and boost nodes (BOOST1, BOOST2) away from sensitive small-signal nodes, especially from the opposite channel's voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the "output side" of the LTC3802 and occupy minimum PC trace area.
5. Reduce the parasitic inductance at the SW and PGND connections to allow proper Burst Mode operation. Use multiple vias if possible.
6. Use the same resistor values for the FB and CMPIN resistive divider. Connect these dividers to the same node: the (+) terminals of C_{OUT} and signal ground. The dividers should be connected to a node away from any high current path.
7. Place the V_{CC} and PV_{CC} decoupling capacitor close to the IC, between the V_{CC} and the signal ground, and between PV_{CC} and PGND. The V_{CC} capacitor provides a quiet supply for the sensitive analog circuits and the PV_{CC} capacitor carries the MOSFET drivers current peaks. An additional 1μF ceramic capacitor placed immediately next to the V_{CC} and SGND pins can substantially improve noise performance.

Checking Transient Response

For all new LTC3802 PCB circuits, transient tests need to be performed to verify the proper feedback loop operation. The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \bullet (ESR)$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for excessive overshoot or ringing which would indicate a stability problem.

Measuring transient response presents a challenge in two respects: obtaining an accurate measurement and generating a suitable transient for testing the circuit. Output measurements should be taken with a scope probe directly across the output capacitor. Proper high frequency probing techniques should be used. Do not use the 6" ground lead that comes with the probe! Use an adapter that fits on the tip of the probe and has a short ground clip

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to ensure that inductance in the ground path doesn't cause a bigger spike than the transient signal being measured. The typical probe tip ground clip is spaced just right to span the leads of a typical output capacitor. In general, it is best to take this measurement with the 20MHz bandwidth limit on the oscilloscope turned on to limit high frequency noise. Note that microprocessor manufacturers typically specify ripple ≤20MHz, as energy above 20MHz is generally radiated and not conducted and will not affect the load even if it appears at the output capacitor.

Now that we know how to measure the signal, we need to have something to measure. The ideal situation is to use the actual load for the test, switching it on and off while watching the output. If this isn't convenient, a current step generator is needed. This generator needs to be able to turn on and off in nanoseconds to simulate a typical switching logic load, so stray inductance and long clip leads between the LTC3802 and the transient generator must be minimized.

Figure 9 shows an example of a simple transient generator. Be sure to use a noninductive resistor as the load element—many power resistors use an inductive spiral pattern and are not suitable for use here. A simple solution is to take ten 1/4W film resistors and wire them in parallel to get the desired value. This gives a noninductive resistive load which can dissipate 2.5W continuously or 250W if pulsed with a 1% duty cycle, enough for most LTC3802 circuits. Solder the MOSFET and the resistor(s) as close to the output of the LTC3802 circuit as possible and set up the signal generator to pulse at a 100Hz rate with a 1% duty cycle. This pulses the LTC3802 with 100µs transients 10ms apart, adequate for viewing the entire transient recovery time for both positive and negative transitions while keeping the load resistor cool.

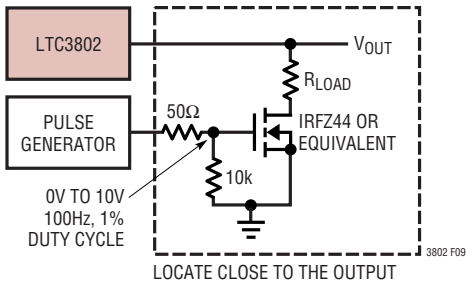
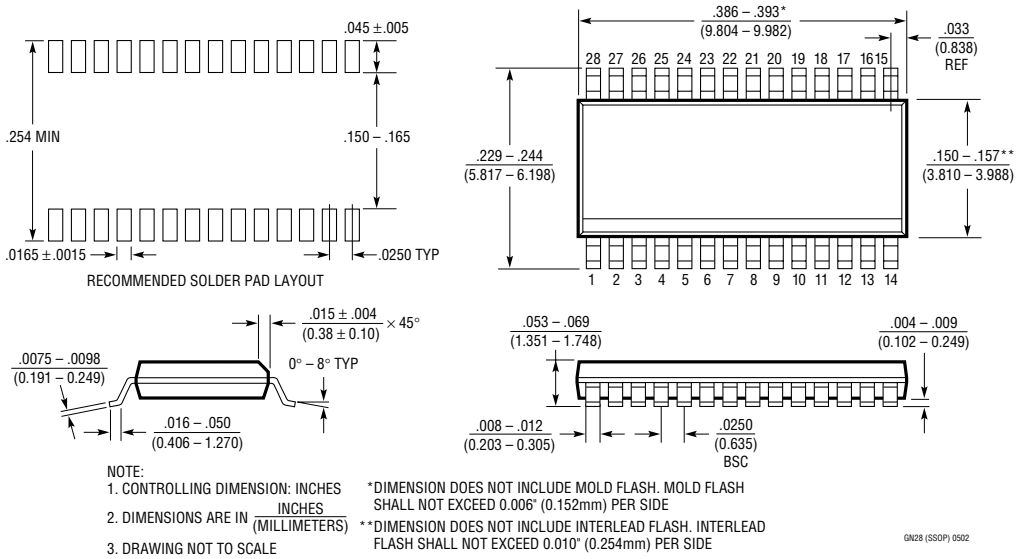


Figure 9. Transient Load Generator

PACKAGE DESCRIPTION

GN Package
28-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)

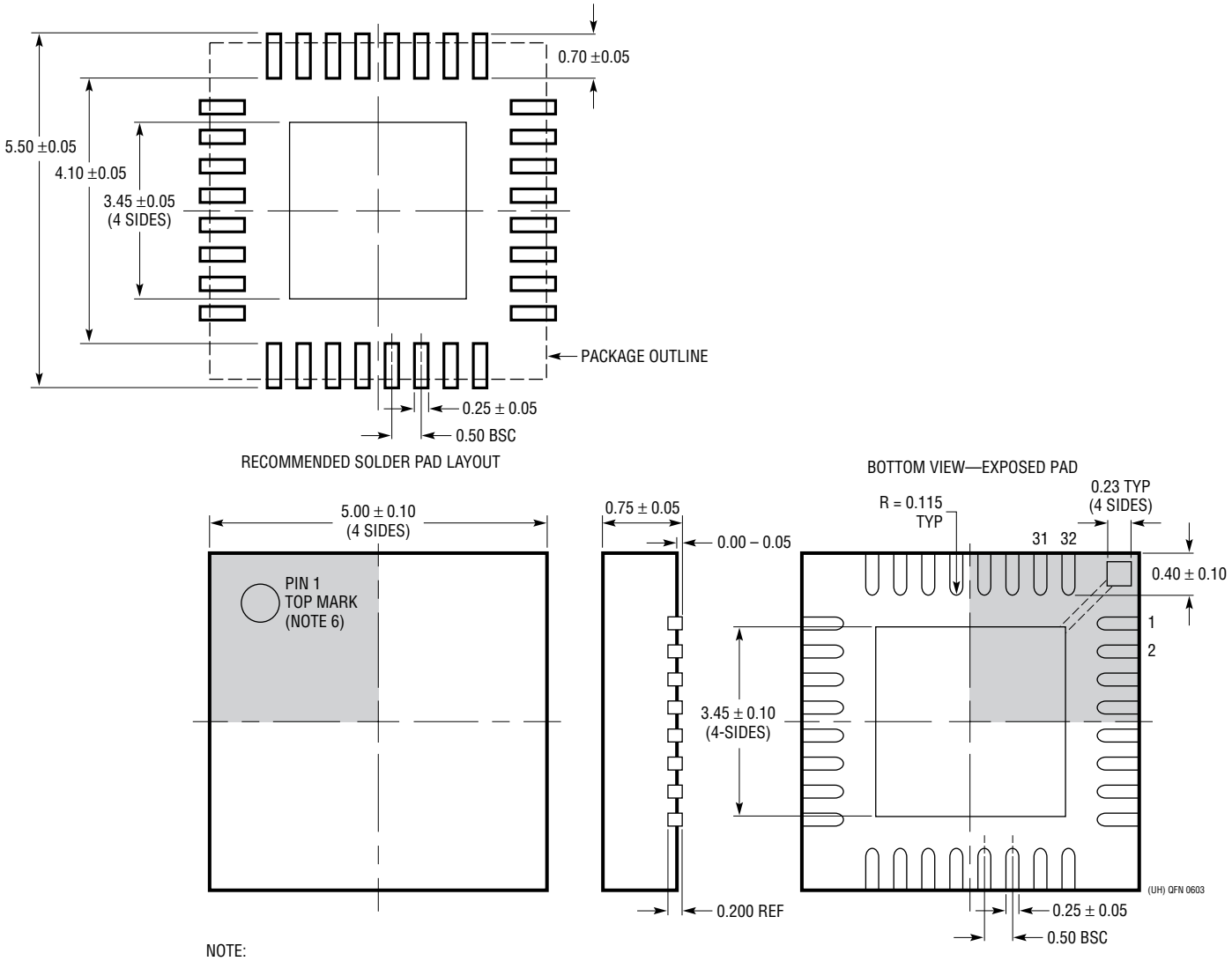


NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN INCHES (MILLIMETERS)
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693)



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE