Synchronous Flyback DC/DC Controller

FEATURES

- **High Efficiency at Full Load**
- **Better Cross Regulation Than Nonsynchronous Converters (Multiple Outputs)**
- **Soft-Start Minimizes Inrush Current**
- Current Mode Control Provides Excellent Transient Response
- High Maximum Duty Cycle: 89% Typical
- ±2% Programmable Undervoltage Lockout Threshold
- ±1% Internal Voltage Reference
- Micropower Start-Up
- Constant Frequency Operation (Never Audible)
- 3mm × 4mm 12-Pin DFN Package

APPLICATIONS

- 48V Telecom Supplies
- 12V/42V Automotive
- 24V Industrial
- VoIP Phone
- Power Over Ethernet

DESCRIPTION

The LTC®3806 is a current mode synchronous flyback controller that drives N-channel power MOSFETs and requires very few external components. It is intended for medium power applications where multiple outputs are required. Synchronous rectification provides higher efficiency and improved output cross regulation than nonsynchronous converters.

The IC contains all the necessary control circuitry including a 250kHz oscillator, precision undervoltage lockout circuit with hysteresis, gate drivers for primary and synchronous switches, current mode control circuitry and soft-start circuitry.

Programmable soft-start reduces inrush currents. This makes it easier to design compliant Power Over Ethernet supplies.

Low start-up current reduces power dissipation in the start-up resistor and reduces the size of the external start-up capacitor.

The LTC3806 is available in a 12-pin, exposed pad DFN package.

TYPICAL APPLICATION

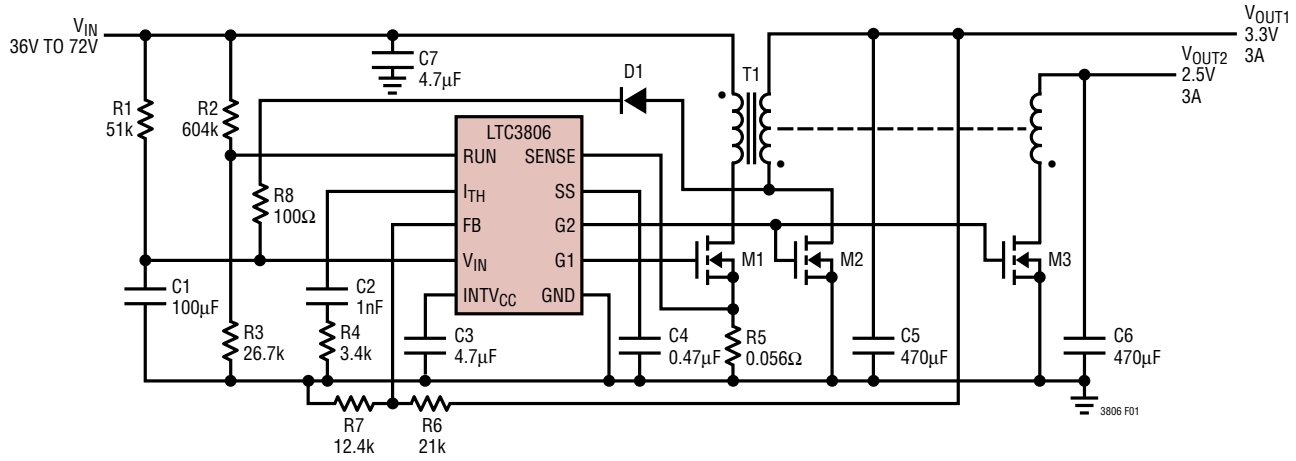


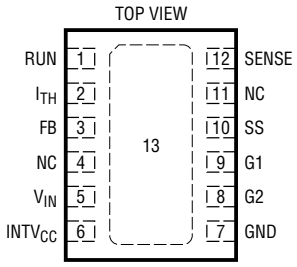
Figure 1. Multiple Output Flyback Converter for Telecom

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage 25V
$INTV_{CC}$ Voltage 8V
$INTV_{CC}$ Output Current 50mA
G1, G2 Voltages ..... –0.3V to V_{INTVCC} + 0.3V
I_{TH}, FB, SS Voltages .....–0.3V to 2.7V
RUN Voltage ..... –0.3V to 7V
SENSE Pin Voltage ..... –0.3V to 8V
Operating Ambient Temperature Range
(Note 2) ..... –40°C to 85°C
Junction Temperature (Note 3)..... 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



DE12 PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 13) IS GND
MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3806EDE#PBF	LTC3806EDE#TRPBF	3806	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 10V, V_{RUN} = 1.5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
$V_{IN(MIN)}$	Minimum Input Voltage	(Note 4)		10			V
I_Q	Input Voltage Supply Current	(Note 5)					
	Quiescent				1000		µA
	Shutdown Mode	V_{RUN} = 0V			50	90	µA
	Start-Up Mode	V_{RUN} > 1.255V, V_{IN} < 7V			80	140	µA
V_{RUN}^+	Rising RUN Input Threshold Voltage	V_{IN} = 20V		1.205	1.230	1.255	V
			●	1.181		1.279	V
V_{RUN}^-	Falling RUN Input Threshold Voltage	V_{IN} = 20V		1.116	1.139	1.162	V
			●	1.093		1.185	V
$V_{RUN(HYST)}$	RUN Pin Input Threshold Hysteresis	V_{IN} = 20V		45	91	137	mV
I_{RUN}	RUN Input Current				1	60	nA
V_{FB}	Feedback Voltage	V_{ITH} = 0.75V (Note 6)		1.218	1.230	1.242	V
			●	1.212		1.248	V
I_{FB}	Feedback Pin Input Current	V_{ITH} = 0.75V (Note 6)			18	100	nA
$\Delta V_{FB}/\Delta V_{IN}$	Line Regulation	10V ≤ V_{IN} ≤ 20V			0.01		%/V
$\Delta V_{FB}/\Delta V_{ITH}$	Load Regulation	V_{TH} = 0.55V to 0.95V (Note 6)	●	–1	–0.1		%
g_m	Error Amplifier Transconductance	I_{TH} Pin Load = ±5µA (Note 6)			650		µMho

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 10V, V_{RUN} = 1.5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{SENSE(MAX)}$	Maximum Current Sense Input Threshold			110	150	190	mV
$I_{SENSE(ON)}$	SENSE Pin Current (G1 High)	V_{SENSE} = 0V			35	50	µA
$I_{SENSE(OFF)}$	SENSE Pin Current (G1 Low)	V_{SENSE} = 1V			0.1	5	µA
I_{SS}	SS Pin Source Current	V_{SS} = 1.5V		3	5	8	µA
Oscillator							
f_{OSC}	Oscillator Frequency			210	250	290	kHz
DC(MAX)	Maximum Duty Cycle			84	89	94	%
Regulator							
V_{INTVCC}	$INTV_{CC}$ Regulator Output Voltage	V_{IN} = 10V		6	6.9	7.8	V
$\frac{\Delta INTV_{CC}}{\Delta V_{IN}}$	$INTV_{CC}$ Regulator Line Regulation	10V ≤ V_{IN} ≤ 20V				100	mV
$V_{LDO(LOAD)}$	$INTV_{CC}$ Load Regulation	0 ≤ I_{INTVCC} ≤ 20mA		–6	–3		%
V_{UVL}^+	Rising V_{IN} Threshold Voltage			14	15	16	V
V_{UVL}^-	Falling V_{IN} Threshold Voltage			7.5	8	8.5	V
Gate Drivers							
t_{r1}	Gate Driver 1 Output Rise Time	C_{L1} = 3300pF			25	100	ns
t_{f1}	Gate Driver 1 Output Fall Time	C_{L1} = 3300pF			18	100	ns
t_{r2}	Gate Driver 2 Output Rise Time	C_{L2} = 4700pF			25	100	ns
t_{f2}	Gate Driver 2 Output Fall Time	C_{L2} = 4700pF			18	100	ns
t_{DEAD}	Gate Driver Dead Time	C_{L1} = 3300pF, C_{L2} = 4700pF			100		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3806E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet 34°C/W)$$

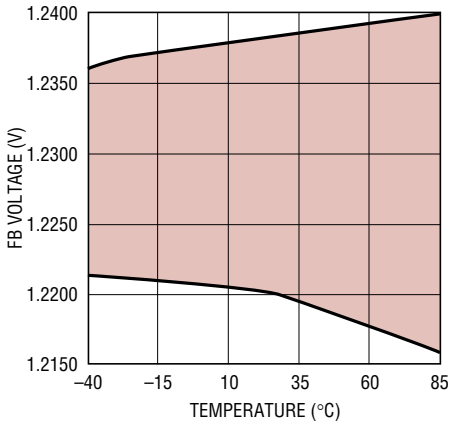
Note 4: The minimum operating voltage is allowed once operation begins. To begin operation, V_{IN} must be above the rising undervoltage lockout threshold with V_{RUN} above the rising RUN input threshold.

Note 5: The dynamic input supply current is higher due to power MOSFET gate charging ($Q_G \bullet f_{OSC}$). See Applications Information.

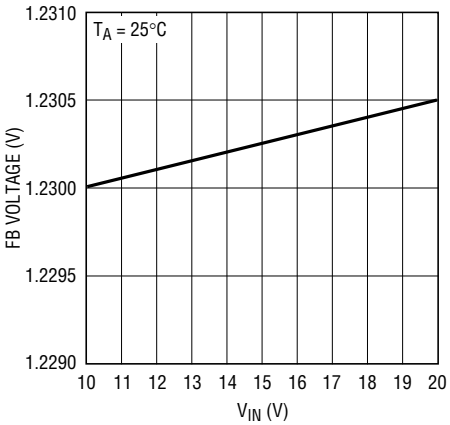
Note 6: The LTC3806 is tested in a feedback loop which servos V_{FB} to the reference voltage with the I_{TH} pin forced to a voltage between 0V and 1.4V (the no load to full load operating voltage range for the I_{TH} pin is 0.3V to 1.23V).

TYPICAL PERFORMANCE CHARACTERISTICS

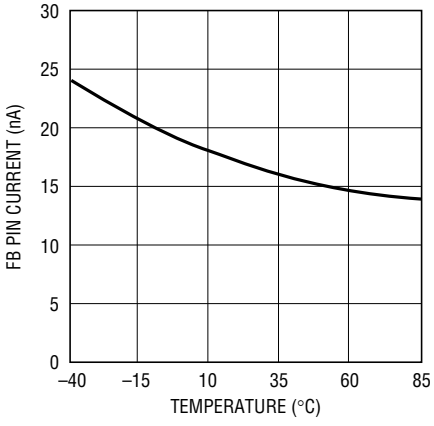
FB Voltage vs Temperature



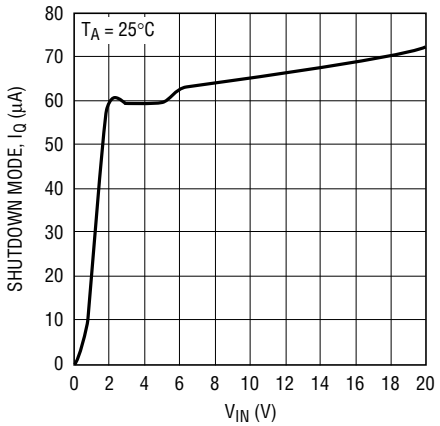
FB Voltage Line Regulation



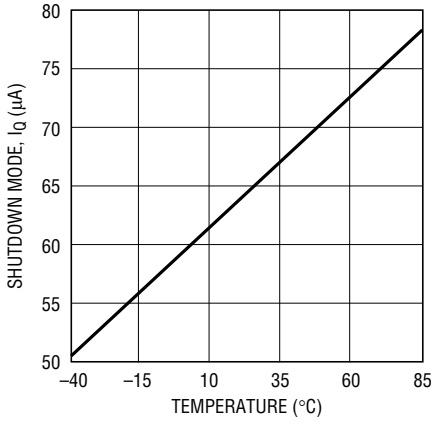
FB Pin Current vs Temperature



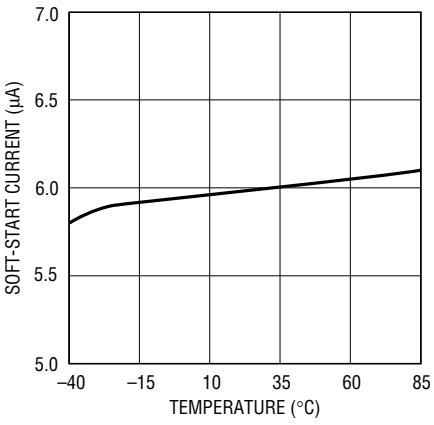
Shutdown Mode I_Q vs V_{IN}



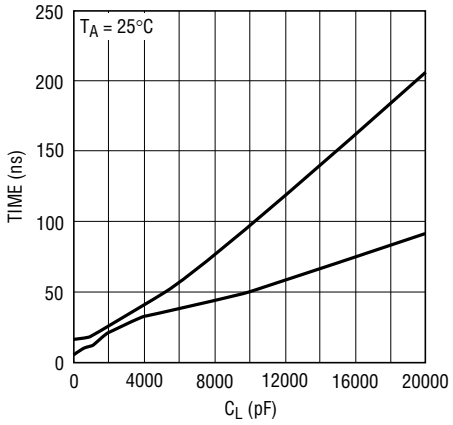
Shutdown Mode I_Q vs Temperature



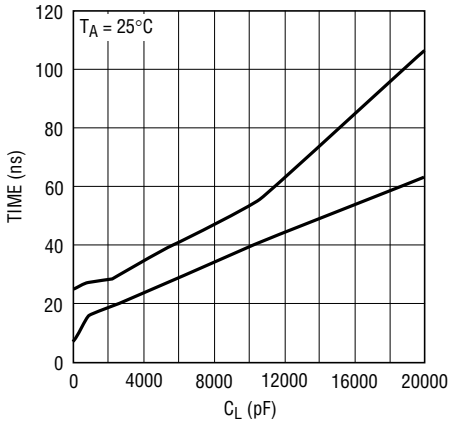
Soft-Start Current vs Temperature



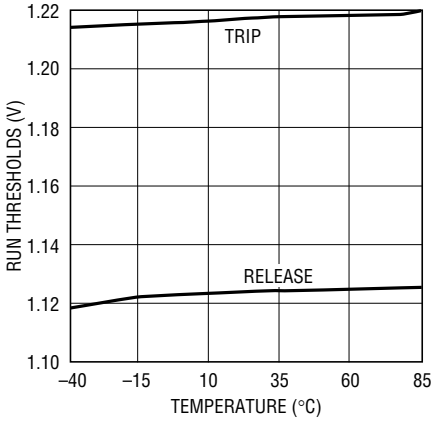
G1 Rise and Fall Time vs C_L



G2 Rise and Fall Time vs C_L

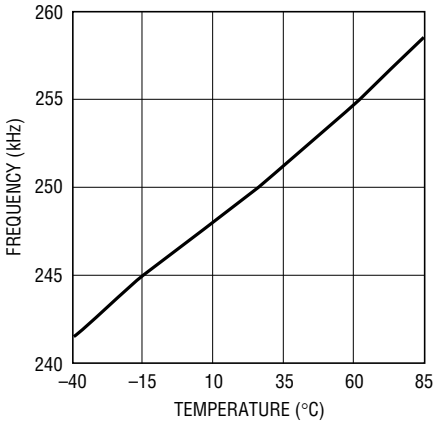


RUN Thresholds vs Temperature

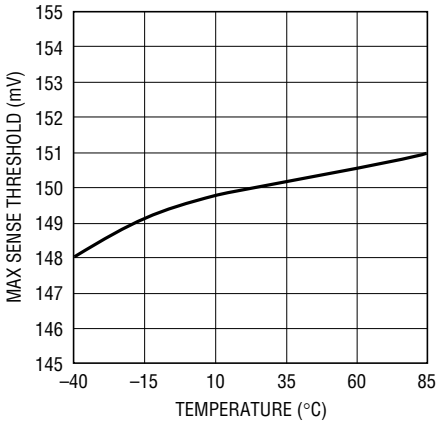


TYPICAL PERFORMANCE CHARACTERISTICS

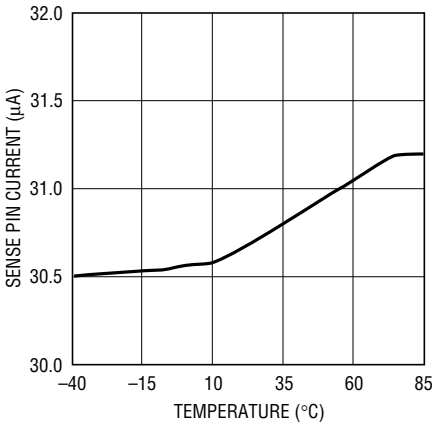
Frequency vs Temperature



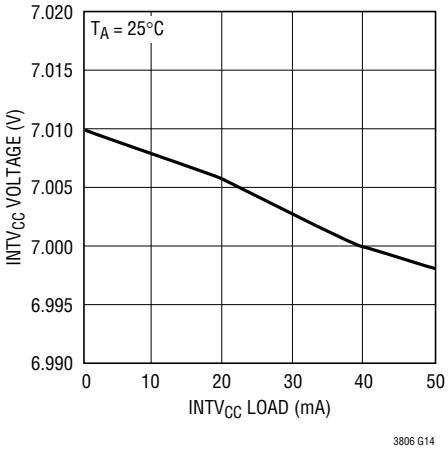
Maximum Sense Threshold vs Temperature



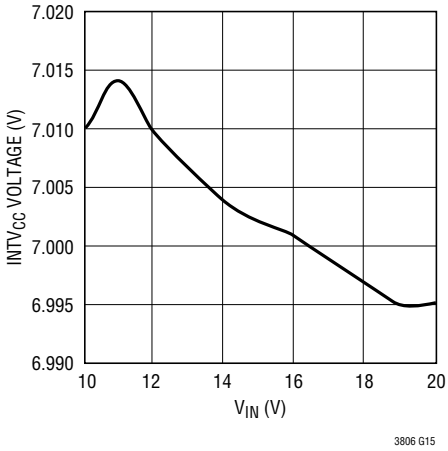
SENSE Pin Current vs Temperature



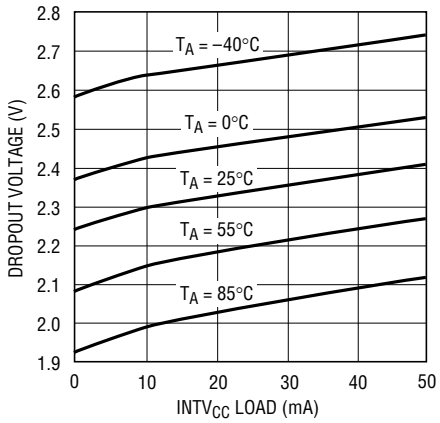
$INTV_{CC}$ Load Regulation



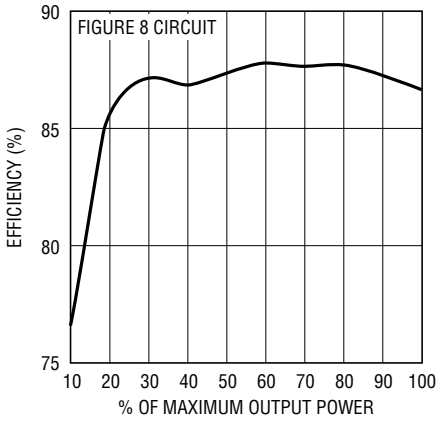
$INTV_{CC}$ Line Regulation



$INTV_{CC}$ Dropout Voltage vs Current, Temperature



Efficiency vs Output Power



PIN FUNCTIONS

RUN (Pin 1): The RUN pin provides the user with an accurate means for sensing the input voltage and programming the start-up threshold for the converter. The falling RUN pin threshold is nominally 1.14V and the comparator has 91mV of hysteresis for noise immunity. When the RUN pin is below this input threshold, the gate drive outputs G1 and G2 are held low. The absolute maximum rating for the voltage on this pin is 7V.

I_{TH} (Pin 2): Error Amplifier Compensation Pin. The current comparator input threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 1.4V.

FB (Pin 3): Receives the feedback voltage from the external resistor divider across the main output. Nominal voltage for this pin in regulation is 1.230V.

NC (Pins 4, 11): Do Not Connect.

V_{IN} (Pin 5): Main Supply Pin. Must be closely decoupled to ground.

$INTV_{CC}$ (Pin 6): The Internal 6.9V Regulator Output. The gate drivers and control circuits are powered from this voltage. Decouple this pin locally to the IC ground with a minimum 4.7μF low ESR ceramic capacitor.

GND (Pins 7, 13): Ground Pins. Exposed pad must be tied to electrical ground.

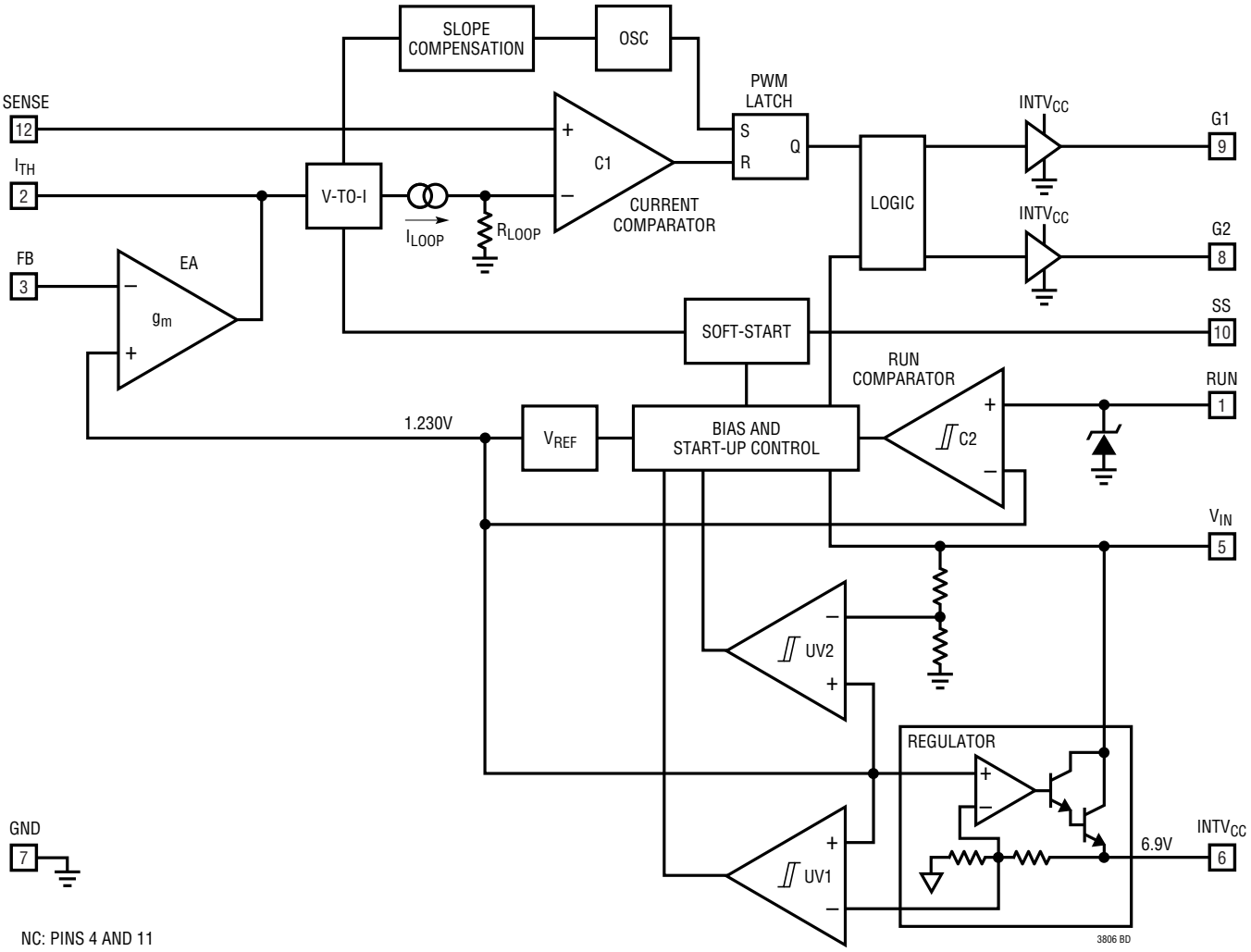
G2 (Pin 8): Secondary-Side Gate Driver Output. This pin drives the gates of all of the synchronous rectifiers.

G1 (Pin 9): Primary-Side Gate Driver Output.

SS (Pin 10): Soft-Start. A capacitor between this pin and ground sets the rate at which the current comparator input threshold may increase when the IC is initially enabled. Increasing the size of the capacitor slows down the ramp rate and reduces the inrush current.

SENSE (Pin 12): Current Sense Input for the Control Loop. Connect this pin to the current sense resistor in the source of the primary side power MOSFET. Internal leading edge blanking is provided.

BLOCK DIAGRAM



OPERATION

Main Control Loop

The LTC3806 is a constant frequency, current mode flyback converter controller. A secondary-side gate driver capable of driving several MOSFET synchronous rectifiers is provided. To insure best cross regulation, DC/DC converters using this controller operate in forced continuous conduction (current is always flowing in either the primary or secondary winding(s) of the transformer.)

For circuit operation, please refer to the Block Diagram of the IC and Figure 1. In normal operation, the primary-side power MOSFET is turned on when the oscillator sets the PWM latch and is turned off when the current comparator C1 resets the latch. V_{OUT1} is divided down and compared to an internal 1.230V reference by error amplifier EA, which outputs an error signal at the I_{TH} pin. The voltage of the I_{TH} pin sets the current comparator C1 input threshold. When the load current on either output increases, a fall in the FB voltage relative to the reference voltage causes the I_{TH} pin to rise increasing the primary-side peak current thereby maintaining regulation. Regulation of V_{OUT2} is indirect, occurring via transformer action.

The RUN pin and undervoltage comparators control whether the IC is enabled or is in a low current state. With the RUN pin below 1.139V, the chip is off and the input supply current is typically only 50μA. If the RUN pin is above 1.230V, most internal circuitry remains off until V_{IN} exceeds the undervoltage comparator UV2 threshold. This reduces start-up current to approximately 80μA allowing smaller values for C1 and larger values for R1 to be used.

The undervoltage comparator UV1 keeps G1 and G2 low until $INTV_{CC}$ voltage is >4.7V to insure that gate drivers will switch the external power MOSFETs properly.

Prior to normal operation, soft-start pin SS is low clamping the output of the V-to-I converter to a low value causing current comparator C1 to trip at a low threshold. Once operation begins, the SS pin ramps up causing the clamp voltage to rise as well. This allows progressively higher trip points on comparator C1 and progressively higher peak currents to be supplied to the primary of the transformer. Soft-start is completed when the voltage on the SS pin exceeds the voltage on the I_{TH} pin.

The nominal operating frequency of the LTC3806 is 250kHz. Since forced continuous operation is used, the noise spectrum over all operating conditions is well controlled with virtually all noise occurring at the operating frequency and its harmonics.

APPLICATIONS INFORMATION

$INTV_{CC}$ Regulator Bypassing and Operation

An internal voltage regulator produces the 6.9V supply that powers the gate drivers and logic circuitry within the LTC3806. The $INTV_{CC}$ regulator can supply up to 50mA and must be bypassed to ground immediately adjacent to the IC pins with a minimum of 4.7µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate drivers.

In an actual application, most of the IC supply current is used to drive the gate capacitances of the power MOSFETs. As a result, high input voltage applications with large power MOSFETs can cause the LTC3806 to exceed its maximum junction temperature rating. The junction temperature can be estimated using the following equations:

$I_{Q(TOT)} = I_Q + f \bullet Q_G$

$P_{IC} = V_{IN} \bullet (I_Q + f \bullet Q_G)$

$T_J = T_A + P_{IC} \bullet R_{TH(JA)}$

where

I_Q is the static supply current

Q_G is the total gate charge of all external power MOSFETs

P_{IC} is the power dissipated in the IC

f is the switching frequency, nominally 250kHz

$R_{TH(JA)}$ is the package thermal resistance, junction to ambient, nominally 34°C/W for the 12-pin DFN package

As an example, consider a 2-output power supply that uses an Si7450DP primary-side power MOSFET, that has a maximum total gate charge of 42nC and two Si4840DY power MOSFETs (one for each output), each of which has 28nC maximum total gate charge.

The total gate charge is:

$Q_G = 42nC + 2 \bullet 28nC = 98nC$

The total supply current is:

$I_{Q(TOT)} = 2000\mu A + 98nC \bullet 250kHz = 27mA$

This demonstrates how significant the gate charge current can be when compared to static quiescent current in the IC.

If V_{IN} is set to 10V, the power dissipation is:

$P_{IC} = 10 \bullet 27mA = 270mW$

and the junction temperature (assuming 70 degree ambient temperature) is:

$T_J = 70°C + 270mW \bullet 120°C/W = 102.4°C$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked when operating at high V_{IN}. If junction temperature is too high, using a separate transformer winding to lower V_{IN} may be tried. Prior to adding an additional transformer winding (which raises transformer cost), be sure to check with power MOSFET manufacturers for their newest low Q_G, low $R_{DS(ON)}$ devices. Power MOSFET manufacturing technologies are continually improving, with newer and better performance devices being introduced almost yearly.

Output Voltage Programming

This IC will generally be used in DC/DC converters with multiple outputs. The output voltage of the master output (V_{OUT1}) is set by a resistor divider according to the following formula:

$$V_{OUT1} = 1.230V \bullet \left(1 + \frac{R6}{R7}\right)$$

The external resistor divider is connected as shown in Figure 1. The resistors R6 and R7 are typically chosen so that the error caused by the current flowing into the FB pin during normal operation is less than 1% (this translates to a maximum value of R7 of about 120k).

The nominal slave output (V_{OUT2}) voltage is set according to the following formula:

$V_{OUT2} = V_{OUT1} \bullet N21$

where N21 is the turns ratio of the transformer windings between V_{OUT2} and V_{OUT1}.

If additional slave outputs are added their voltage is determined by the equation:

$V_{OUTN} = V_{OUT1} \bullet N_{N1}$

where N_{N1} is the turns ratio of the transformer windings between V_{OUTN} and V_{OUT1}.

APPLICATIONS INFORMATION

Cross regulation and tracking between the master and slave outputs are impacted by transformer and secondary-side power MOSFET selection. Select a power MOSFET with low on resistance. In addition, a transformer with low winding resistances and highest coupling coefficient will have better cross regulation and tracking.

Composite Feedback

In applications where accuracy is important on more than one output, composite feedback may be used. This sacrifices some of the accuracy of one output for improved accuracy on the other output(s). Figure 2 shows how composite feedback can be applied to two outputs.

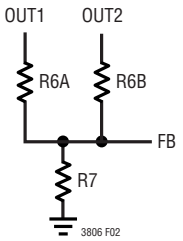


Figure 2. Composite Feedback

Select a value for R7 less than or equal to 120k. Now choose the fraction K of the total feedback taken from V_{OUT1}. The higher the fraction used, the tighter V_{OUT1} is controlled, but the poorer V_{OUT2} is controlled (since it contributes less to the total feedback). The values for R6A and R6B can now be calculated:

$$R6A = \frac{R7}{K}\left(\frac{V_{OUT1}}{V_{REF}} - 1\right)$$

$$R6B = \frac{R7}{1-K}\left(\frac{V_{OUT2}}{V_{REF}} - 1\right)$$

This technique can easily be extended to more outputs if needed.

Programming Turn-On and Turn-Off Thresholds with the RUN Pin

The LTC3806 leaves a comparator detection circuit and the voltage reference active even when the device is shut down (Figure 3). This allows users to accurately program an input voltage at which the converter will turn on and off.

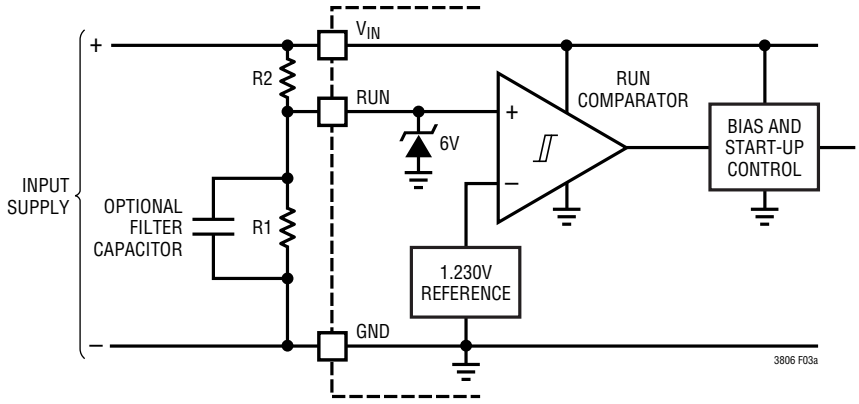


Figure 3a. Programming the Turn-On and Turn-Off Thresholds Using the RUN Pin

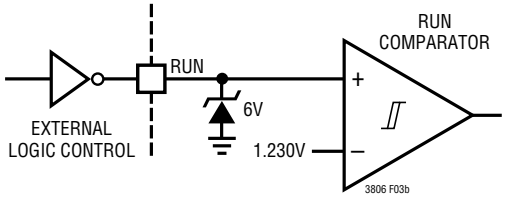


Figure 3b. On/Off Control Using External Logic

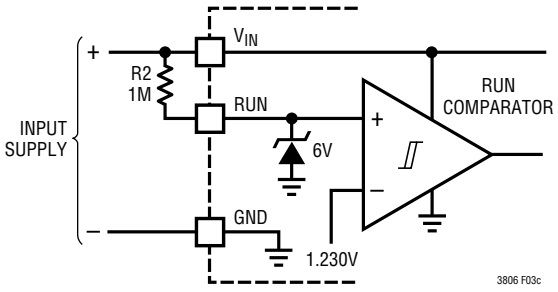


Figure 3c. External Pull-Up Resistor On RUN Pin for "Always On" Operation

APPLICATIONS INFORMATION

The rising threshold voltage on the RUN pin is equal to the internal reference voltage of 1.230V. The comparator has 91mV of hysteresis to increase noise immunity.

The turn-on and turn-off input voltage thresholds are programmed using a resistor divider according to the following formulas:

$$V_{IN(OFF)} = 1.139V \bullet \left(1 + \frac{R2}{R1}\right)$$

$$V_{IN(ON)} = 1.230V \bullet \left(1 + \frac{R2}{R1}\right)$$

The resistor R1 is typically chosen to be less than 1M. **For applications where the RUN pin is only to be used as a logic input, the user should be aware of the 7V Absolute Maximum Rating for this pin!** The RUN pin can be connected to the input voltage through an external 1M resistor, as shown in Figure 3c, for "always on" operation.

Application Circuits

A basic LTC3806 application circuit is shown in Figure 1. External component selection is driven by the characteristics of the load and the input supply.

Duty Cycle Considerations

Current and voltage stress on the power switch and synchronous rectifiers, input and output capacitor RMS currents and transformer utilization (size vs power) are impacted by duty factor. Unfortunately duty factor cannot be adjusted to simultaneously optimize all of these requirements. In general, avoid extreme duty factors since this severely impacts the current stress on most of the components. A reasonable target for duty factor is 50% at nominal input voltage. Using this rule of thumb, calculate the ideal transformer turns ratio:

$$N_{IDEAL} = \frac{V_{OUT1}}{V_{IN}} \bullet \left(\frac{1-D}{D}\right)$$

For a 50% duty factor, this reduces to:

$$N_{IDEAL} = \frac{V_{OUT1}}{V_{IN}}$$

If N_{IDEAL} is integer, use this for your turns ratio. If not, find a ratio of small integers that comes close to N_{IDEAL}. If these conditions are met, bifilar winding techniques can be used that will improve coupling coefficient. Cross regulation will be better and primary-side snubbing may be reduced or eliminated.

The selected turns ratio doesn't have to be perfectly equal to N_{IDEAL} because a flyback converter's output voltage is not set through transformer action. Instead, the transformer stores energy when the primary-side switch turns on and transfers this energy to the output(s) by flyback action when the primary-side switch turns off.

Cross regulation may be improved by using a target duty factor which is less than 50%. This improves cross regulation because the secondary-side MOSFETs (synchronous rectifiers) will be on a larger percentage of the time (thereby increasing the average coupling between the outputs). Duty factor is reduced by proportionately increasing all turns ratios.

Reduced duty factor has the following effect on MOSFET stresses:

LOCATION	MOSFET CURRENT STRESS	MOSFET VOLTAGE STRESS
Primary	Increased	Reduced
Secondary	Reduced	Increased

The duty factor with the selected turns ratio will equal:

$$D = \frac{V_{OUT1}}{V_{OUT1} + (N \bullet V_{IN})}$$

While the output(s)/input turns ratio are not critical, *the turns ratio **between** outputs are critical and affect the accuracy of the slave output voltages.*

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Some common secondary turns ratios:

V_{OUT}	TURNS
2.5 3.3	3 4
3.3 5.0	2 3
1.8 3.3	6 11
1.8 2.5	5 7
2.5 3.3 5.0	3 4 6

For example, assume we need a regulator that operates with a nominal 48V input to produce one 3.3V output and one 5V output. The ideal turns ratio for the 3.3V (master) output is:

$$N_{IDEAL1} = \frac{3.3}{48} = 0.06875$$

We select a turns ratio of 1/15 or N1 = 0.066…

For the 5V output, the ideal turns ratio is:

$$N_{IDEAL2} = N1 \bullet \frac{5}{3.3} = 0.1010...$$

If we choose:

$$N2 = \frac{1}{10}$$

and we assume OUT1 is exact, the voltage on slave output 2 is:

$$V_{OUT2} = 3.3 \bullet \frac{\frac{1}{10}}{\frac{1}{15}} = 3.3 \bullet 1.5 = 4.95V$$

This does not include any other errors, so make sure that the error in V_{OUT2} is only a fraction of what your specification allows. When dealing with large numbers of outputs trial and error is usually required to get reasonable turns ratios on all outputs while keeping the errors (due to imperfect turns ratios) low.

For the selected turns ratios, the duty factor for this design with 48V input would be:

$$D = \frac{V_{OUT1}}{V_{OUT1} + (N \bullet V_{IN})} = \frac{3.3V}{3.3V + \left(\frac{48V}{15}\right)} = 0.508$$

Input Power

The maximum input power is:

$$P_{IN} = \frac{\Sigma_{K=1}^{N} P_{OUTK}}{Eff}$$

where P_{OUTK} is the maximum power supplied by output K and Eff represents the efficiency of the converter.

Continuing the previous example, assume OUT1 delivers 3.3V at 2A and OUT2 delivers 4.95V at 0.5A. For a conversion efficiency at maximum output power of 80%:

$$P_{IN} = \frac{3.3V \bullet 2A + 4.95V \bullet 0.5A}{0.80} = 11.34W$$

Transformer Selection

The transformer primary inductance, L_P, is selected based on the percentage peak-to-peak ripple current (X) in the transformer relative to its maximum value. In general, X should range from 20% to 40% ripple current (i.e., X = 0.2 to 0.4). Higher values of ripple will increase conduction losses, while lower values will require larger cores.

Ripple current and percentage ripple will be largest at minimum duty factor D, in other words at the highest input voltage. L_P can be calculated from:

$$L_P = \frac{V_{IN(MAX)}{}^2 \bullet D_{MIN}{}^2}{f \bullet X_{MAX} \bullet P_{IN}}$$

where f is nominally 250kHz.

Continuing the example, allow 40% maximum ripple at a maximum input voltage of 72V:

$$D_{MIN} = \frac{3.3V}{3.3V + \frac{72V}{15}} = 0.407$$

$$L_P = \frac{72V^2 \bullet 0.407^2}{250000Hz \bullet 0.4 \bullet 11.34W} = 757\mu H$$

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For a minimum input voltage of 36V, the largest duty factor is:

$$D_{MAX} = \frac{3.3V}{3.3V + \frac{36V}{15}} = 0.579$$

and the minimum percentage ripple is:

$$X_{MIN} = \frac{V_{IN}{}^2 \bullet D_{MAX}{}^2}{f \bullet L_P \bullet P_{IN}}$$

$$= \frac{36V^2 \bullet 0.579^2}{250kHz \bullet 757\mu H \bullet 11.34W} = 20.2\%$$

Transformer Core Selection

Once L_P is known, the type of transformer must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite cores. Actual core loss is independent of core size for a fixed inductance, but is very dependent on the inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Generally, there is a tradeoff between core losses and copper losses that needs to be balanced. In addition, increased winding resistance will degrade cross regulation.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper losses and preventing saturation. Ferrite core material saturates "hard," meaning that the inductance collapses rapidly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequently, output voltage ripple. **Do not allow the core to saturate!** The maximum peak primary current occurs at minimum V_{IN}:

$$I_{PK} = \frac{P_{IN}}{V_{IN(MIN)} \bullet D_{MAX}} \bullet \left(1 + \frac{X_{MIN}}{2}\right)$$

Current Sense Resistor Selection

The control circuit limits the maximum voltage drop across the sense resistor to about 110mV (at low duty cycle), and only about 70mV at a duty cycle of 92% due to slope compensation. Use Figure 4 and D_{MAX} to determine the maximum allowable drop in the sense resistor. Using this value calculate:

$$R_{SENSE} \leq \frac{V_{DROP}}{I_{PK}}$$

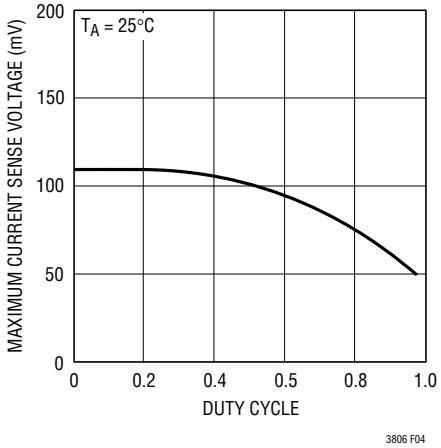

Figure 4. Maximum SENSE Threshold Voltage vs Duty Cycle

Capacitor Selection

In a flyback converter, the input and output current flows in pulses placing severe demands on the input and output filter capacitors. The input and output filter capacitors should be selected based on RMS current ratings and ripple voltage.

Select an input capacitor with a ripple current rating greater than:

$$I_{RMS} = \frac{P_{IN}}{V_{IN(MIN)}} \sqrt{\frac{1 - D_{MAX}}{D_{MAX}}}$$

Continuing the example:

$$I_{RMS} = \frac{11.34W}{36V} \sqrt{\frac{1 - 0.579}{0.579}} = 0.269A_{RMS}$$

Low effective series resistance and inductance is also important in the input capacitor since it affects the electromagnetic interference suppression. In some instances high ESR can also produce stability problems because flyback converters exhibit a negative input resistance

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characteristic. Refer to Application Note 19 for more information.

The output capacitor is sized to handle the ripple current and to insure acceptable output voltage ripple. The output capacitor should have a ripple current rating greater than:

$$I_{RMS} = I_{OUT}\sqrt{\frac{D_{MAX}}{1-D_{MAX}}}$$

This should be calculated for each output. For our example, the OUT1 capacitor needs an RMS current rating greater than:

$$I_{RMS} = 2A\sqrt{\frac{0.579}{1-0.579}} = 2.35A_{RMS}$$

The OUT2 capacitor RMS current rating is calculated in a similar manner. The capacitor rating should be greater than $586mA_{RMS}$. One final note, most capacitor manufacturers base their ripple current ratings on only 2000 hours life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required.

Contributions of ESR (equivalent series resistance), ESL (equivalent series inductance) and the bulk capacitance must be considered when choosing the correct component for a given output ripple voltage. The effects of these three parameters (ESR, ESL and bulk C) on the output voltage ripple waveform are illustrated in Figure 5 for a typical flyback converter.

The capacitance calculation begins with the maximum acceptable ripple voltage (expressed as a percentage of the output voltage), and how this ripple should be divided between the ESR step and the charging/discharging ΔV. For the purpose of simplicity we will choose 2% for the maximum output ripple, to be divided equally between the ESR step and the charging/discharging ΔV. This percentage ripple will change, depending on the requirements of the application, and the equations provided below can easily be modified.

For a 1% contribution to the total ripple voltage, the ESR of the output capacitor can be determined using the following equation:

$$ESR_{COUT} \le \frac{0.01 \bullet V_{OUT} \bullet (1-D_{MAX})}{I_{OUT}}$$

For the bulk C component, which also contributes 1% to the total ripple:

$$C_{OUT} \ge \frac{I_{OUT}}{0.01 \bullet V_{OUT} \bullet F}$$

For many designs it is possible to choose a single capacitor type that satisfies both the ESR and bulk C requirements for the design. In certain demanding applications, however, the ripple voltage can be improved significantly by connecting two or more types of capacitors in parallel. For example, using a low ESR ceramic capacitor can minimize the ESR step, while an electrolytic capacitor can be used to supply the required bulk C.

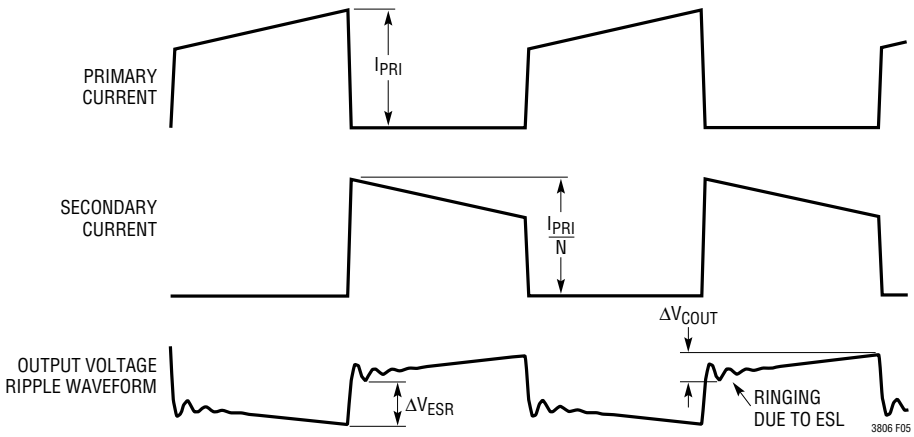

Figure 5. Typical Flyback Converter Waveforms (Single Output)

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Continuing our previous example the filter capacitor for output 1 needs:

$$ESR_{COUT} \le \frac{0.01 \bullet 3.3V \bullet (1-0.579)}{2A} = 7m\Omega$$

$$C_{OUT} \ge \frac{2A}{0.01 \bullet 3.3V \bullet 250kHz} = 242\mu F$$

To get an electrolytic capcitor with an ESR this low would require C_{OUT} much larger than 242µF. Combining a low ESR ceramic capacitor in parallel with an electrolytic capacitor provides better filtering at lower cost.

For output 2, the output capacitor needs an ESR less than 42mΩ and a bulk C greater than 40.4µF. This can be achieved with a single high performance capacitor such as a Sanyo OS-CON or equivalent.

Once the output capacitor ESR and bulk capacitance have been determined, the overall ripple voltage waveform should be verified on a dedicated PC board. Parasitic inductance from poor layout can have a significant impact on ripple. Refer to the layout section for details.

Power MOSFET Selection

Important selection criteria for the power MOSFETs include the "on" resistance $R_{DS(ON)}$, input capacitance, drain-to-source breakdown voltage (BV_{DSS}) and maximum drain current ($I_{D(MAX)}$).

Narrow the choices for power MOSFETs by first looking at the maximum drain currents. For the primary-side power MOSFET:

$$I_{PK} = \frac{P_{IN}}{V_{IN(MIN)} \bullet D_{MAX}} \bullet \left(1 + \frac{X_{MIN}}{2}\right)$$

For each secondary-side power MOSFET:

$$I_{PK} = \frac{I_{OUT}}{1-D_{MAX}} \bullet \left(1 + \frac{X_{MIN}}{2}\right)$$

From the remaining MOSFET choices, narrow the field based on BV_{DSS}. Select a primary-side power MOSFET with a BV_{DSS} greater than:

$$BV_{DSS} \ge I_{PK}\sqrt{\frac{L_{LKG}}{C_P}} + V_{IN(MAX)} + \frac{V_{OUT(MAX)}}{N}$$

where L_{LKG} is the primary-side leakage inductance and C_P is the primary-side capacitance (mostly from the C_{OSS} of the primary-side power MOSFET). A snubber may be added to reduce the leakage inductance related spike. For more information on snubber design, refer to Application Note 19.

For each secondary-side power MOSFET, the BV_{DSS} should be greater than:

$$BV_{DSS} \ge V_{OUT} + V_{IN(MAX)} \bullet N$$

Next, select a logic-level MOSFET with acceptable $R_{DS(ON)}$ at the nominal gate drive voltage (usually 6.9V—set by the $INTV_{CC}$ regulator).

Calculate the required RMS currents next. For the primary-side power MOSFET:

$$I_{RMSPRI} = \frac{P_{IN}}{V_{IN(MIN)} \bullet \sqrt{D_{MAX}}}$$

For each secondary-side power MOSFET:

$$I_{RMSSEC} = \frac{I_{OUT}}{\sqrt{1-D_{MAX}}}$$

Calculate MOSFET power dissipation next. Because the primary-side power MOSFET operates at high V_{DS}, a term for transition power loss must be included in order to get an accurate fix on power dissipation. C_{MILLER} is the most critical parameter in determining the transition loss but is not directly specified on MOSFET data sheets.

C_{MILLER} can be calculated from the gate charge curve included on most data sheets (Figure 6). The curve is generated by forcing a constant input current into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time. The initial slope is the result of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller (gate-to-drain) capacitance as the drain voltage drops. The upper sloping line is due to the gate-to-drain accumulation capacitance and the gate-to-source capacitance. The Miller

APPLICATIONS INFORMATION

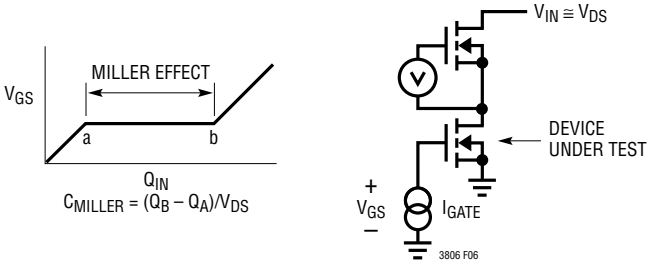

Figure 6. Gate Charge Curve and Test Circuit

charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given V_{DS}, but can be adjusted for different V_{DS} voltages by multiplying by the ratio of the application V_{DS} to the curve specified V_{DS} values. To estimate the C_{MILLER} term, take the change in gate charge from points a and b on the manufacturers data sheet and divide by the specified V_{DS}.

With C_{MILLER} determined, calculate the primary-side power MOSFET power dissipation:

$$P_{DPRI} = I_{RMSPRI}^2 \bullet R_{DS(ON)} (1+\delta) + V_{IN(MAX)} \bullet \frac{P_{IN(MAX)}}{D_{MIN}} \bullet R_{DR} \bullet C_{MILLER} \bullet \left(\frac{1}{V_{INTVCC} - V_{TH}} \right) \bullet f$$

where R_{DR} is the GATE1 driver resistance (maximum is approximately 6Ω), V_{TH} is the typical gate threshold voltage for the specified power MOSFET and f is the operating frequency, typically 250kHz. The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

The secondary-side power MOSFETs typically operate at substantially lower V_{DS}, so transition losses can be neglected. The dissipation may be calculated using:

$$P_{DSEC} = I_{RMSSEC}^2 \bullet R_{DS(ON)} (1 + \delta)$$

For a known power dissipation in the power MOSFETs, the junction temperatures can be obtained from the equation:

$$T_J = T_A + P_D \bullet R_{TH(JA)}$$

where T_A is the ambient temperature and $R_{TH(JA)}$ is the MOSFET thermal resistance from junction to ambient. Compare T_J against your initial estimate for T_J and if necessary, recompute δ, power dissipations and T_J. Iterate as necessary.

Selecting the Compensation Network

Load step testing can be used to empirically determine compensation. Application Note 25 provides information on the technique. When the regulator has multiple outputs, compensation should be optimized for the master output.

PC Board Layout Checklist

1. In order to minimize switching noise and improve output load regulation, the GND pin of the LTC3806 should be connected directly to 1) the negative terminal of the $INTV_{CC}$ decoupling capacitor, 2) the negative terminal of the output decoupling capacitors, 3) the bottom terminal of the current sense resistor, 4) the negative terminal of the input capacitor and 5) at least one via to the ground plane immediately adjacent to Pin 7 (GND).
2. Beware of ground loops in multiple layer PC boards. Try to maintain one central ground node on the board and use the input capacitor to avoid excess input ripple for high output current power supplies. If the ground plane is to be used for high DC currents, choose a path away from the small-signal components.
3. Place the C_{VCC} capacitor immediately adjacent to the $INTV_{CC}$ and GND pins on the IC package. This capacitor carries high di/dt MOSFET gate drive currents. A low ESR X5R 4.7µF ceramic capacitor works well here.
4. The high di/dt loop from the bottom terminal of the input capacitor through the sense resistor, primary-side power MOSFET, transformer primary and back through the input capacitor should be kept as tight as possible in order to reduce EMI. Also keep the loops formed by the *outputs* as tight as possible.
5. Check the switching waveforms of the MOSFETs using the actual PC board layout. Measure directly across the power MOSFET terminals to verify that the BV_{DSS} specification of the MOSFET is not exceeded due to inductive ringing. If this ringing cannot be avoided and

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exceeds the maximum rating of the device, either choose a higher voltage device or specify an avalanche-rated power MOSFET.

6. Place the small-signal components away from high frequency switching nodes. (All of the small-signal components on one side of the IC and all of the power components on the other.) This allows the use of a pseudo-Kelvin connection for the signal ground, where high di/dt gate driver currents flow out of the IC ground pin in one direction (to the bottom plate of the $INTV_{CC}$ decoupling capacitor) and small-signal currents flow in the other direction.

7. Minimize the capacitance between the SENSE pin trace and any high frequency switching nodes. The LTC3806 contains an internal leading edge blanking time of approximately 180ns, which should be adequate for most applications.

8. For optimum load regulation and true remote sensing, the top of the output resistor divider should connect independently to the top of the the output capacitor (Kelvin connection), staying away from any high dV/dt traces. Place the divider resistors near the LTC3806 in order to keep the high impedance FB node short.

9. For applications with multiple switching power converters which connect to the same input supply, make sure that the input filter capacitor for the LTC3806 is not shared with other converters. AC input current from another converter could cause substantial input voltage ripple and this could interfere with the operation of the LTC3806. A few inches of PC trace or wire ($L \cong 100nH$) between the C_{IN} of the LTC3806 and the actual source V_{IN} should be sufficient to prevent current sharing problems.

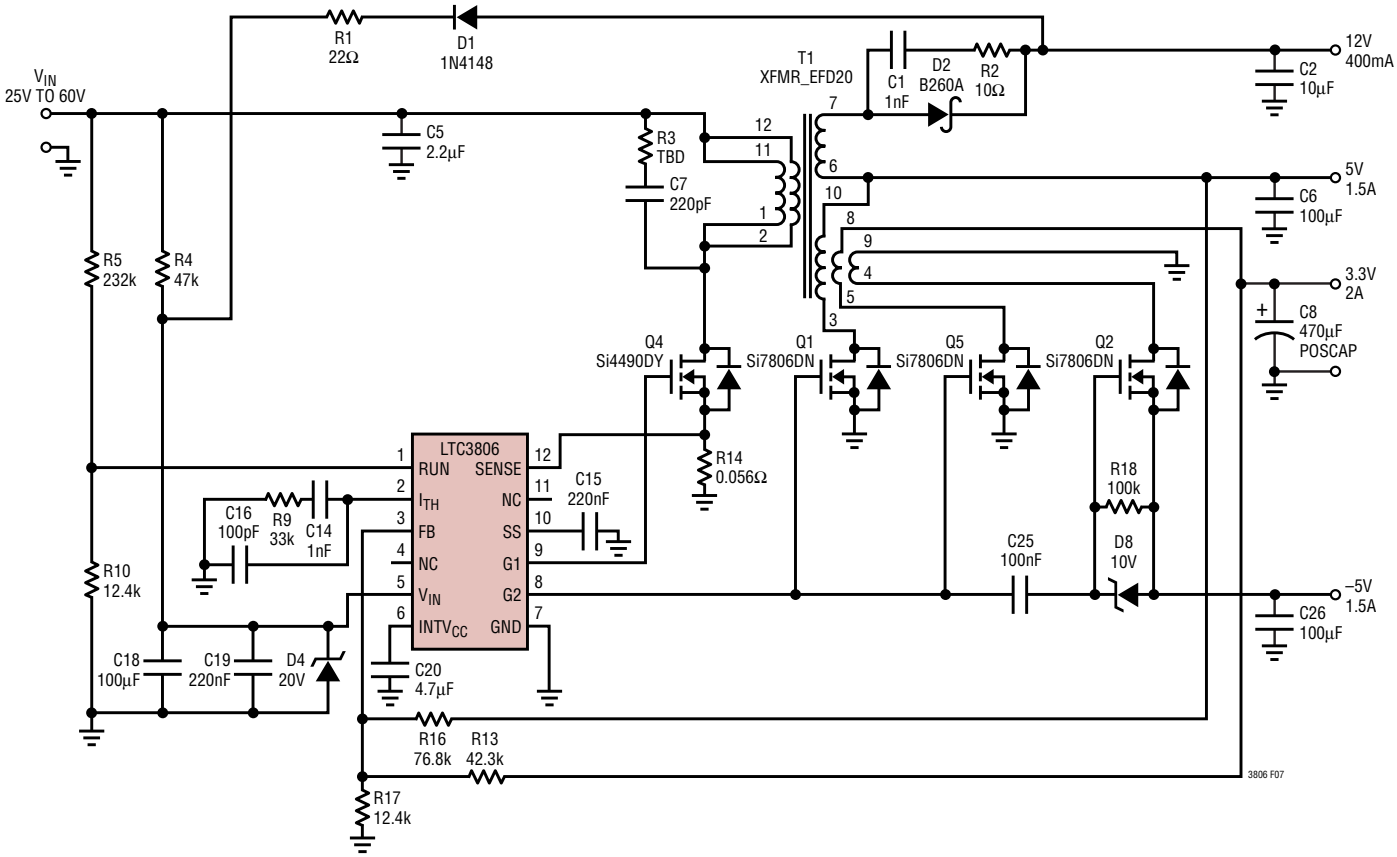

Figure 7. Synchronous Flyback

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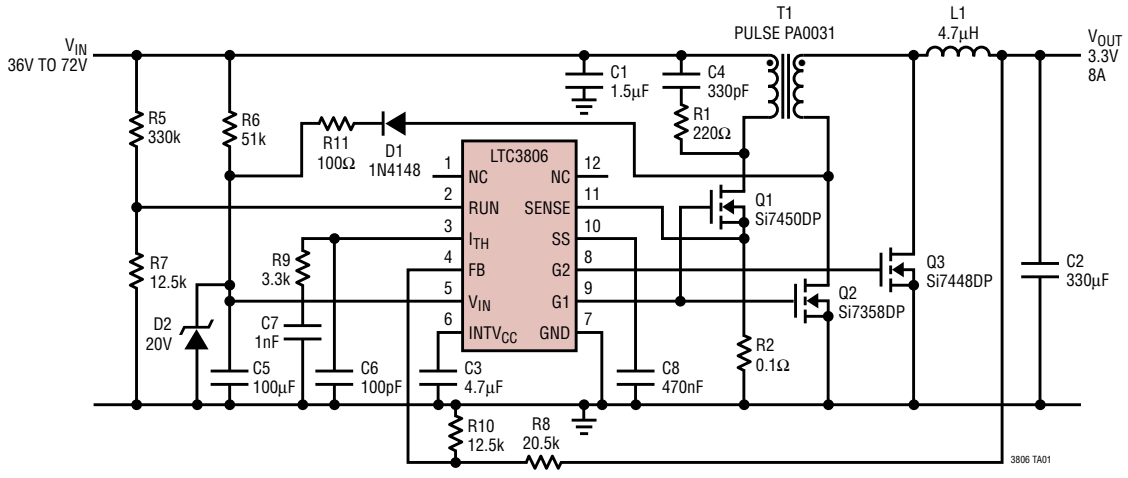
Table 1. Recommended Component Manufacturers

VENDOR	COMPONENTS	TELEPHONE	WEB ADDRESS
AVX	Capacitors	207-282-5111	avxcorp.com
BH Electronics	Transformers	952-894-9590	bhelectronics.com
Coiltronics	Transformers	407-241-7876	coiltronics.com
Diodes, Inc.	Diodes	805-446-4800	diodes.com
Fairchild	MOSFETs	408-822-2126	fairchildsemi.com
General Semiconductor	Diodes	516-847-3000	gerneralsemiconductor.com
International Rectifier	MOSFETs, Diodes	310-322-3331	irf.com
IRC	Sense Resistors	361-992-7900	irctt.com
Kemet	Tantalum Capacitors	408-986-0424	kemet.com
Magnetics Inc.	Toroid Cores	800-245-3984	mag-inc.com
Microsemi	Diodes	617-926-0404	microsemi.com
Murata-Erie	Capacitors	770-436-1300	murata.co.jp
Nichicon	Capacitors	847-843-7500	nichicon.com
On Semiconductor	Diodes	602-244-6600	onsemi.com
Panasonic	Capacitors	714-373-7334	panasonic.com
Sanyo	Capacitors	619-661-6835	sanyo.co.jp
Taiyo Yuden	Capacitors	408-573-4150	t-yuden.com
TDK	Capacitors, Transformers	562-596-1212	component.tdk.com
Thermalloy	Heat Sinks	972-243-4321	aavidthermalloy.com
Tokin	Capacitors	408-432-8020	tokin.com
United Chemicon	Capacitors	847-696-2000	chemi-com.com
Vishay/Dale	Resistors	605-665-9301	vishay.com
Vishay/Siliconix	MOSFETs	800-554-5565	vishay.com
Vishay/Sprague	Capacitors	207-324-4140	vishay.com
Zetex	Small-Signal Discretes	631-543-7100	zetex.com

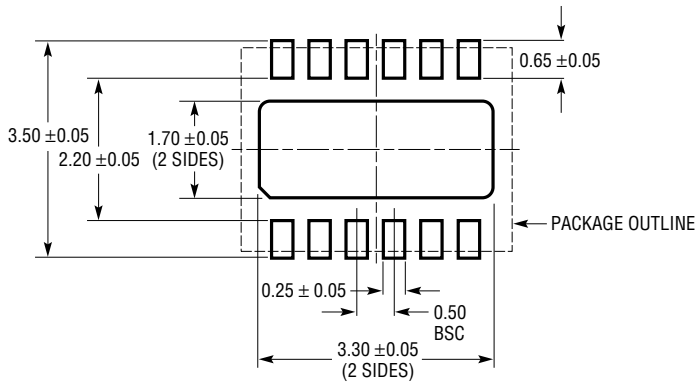
TYPICAL APPLICATION

Synchronous Forward Application

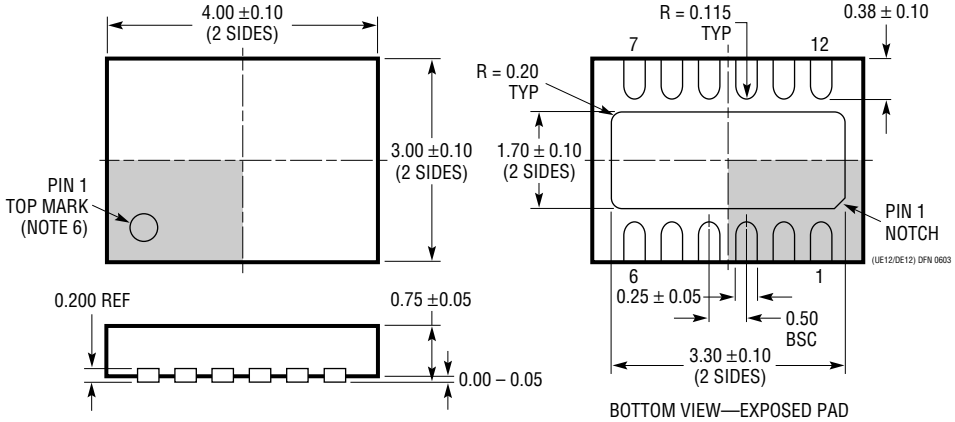


PACKAGE DESCRIPTION

UE/DE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE