# 400MHz to 2.7GHz High Signal Level Downconverting Mixer

## FEATURES

- Internal On-Chip RF Input Transformer
- 50Ω Single-Ended RF and LO Ports
- High Input IP3: +25dBm at 900MHz
  +21.5dBm at 1900MHz
- Low Power Consumption: 280mW Typical
- Integrated LO Buffer: Low LO Drive Level
- High LO-RF and LO-IF Isolation
- Wide RF Frequency Range: 0.4GHz to 2.7GHz*
- Very Few External Components
- Enable Function
- 4.5V to 5.25V Supply Voltage Range
- 16-Lead (4mm × 4mm) QFN Package

## APPLICATIONS

- Cellular, PCS and UMTS Band Infrastructure
- CATV Downlink Infrastructure
- 2.4GHz ISM
- High Linearity Downmixer Applications

## DESCRIPTION

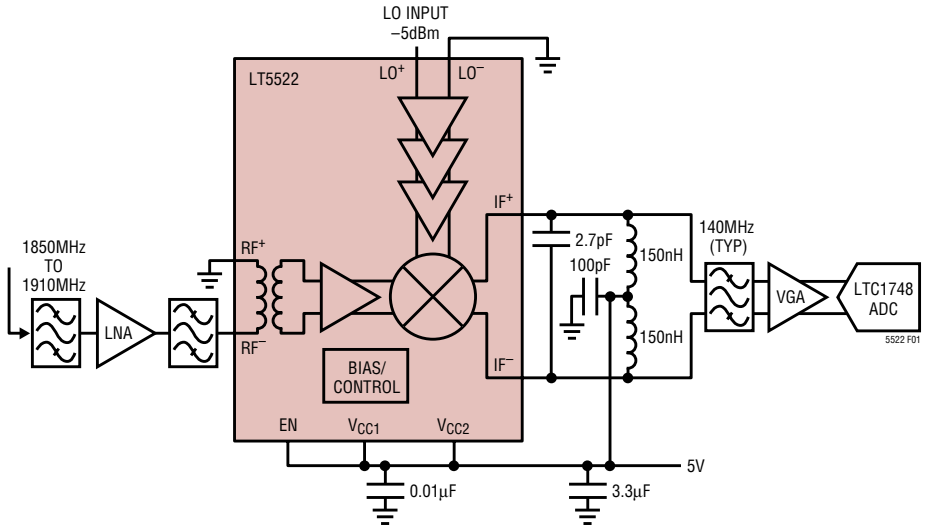
The LT®5522 active downconverting mixer is optimized for high linearity downconverter applications including cable and wireless infrastructure. The IC includes a high speed differential LO buffer amplifier driving a double-balanced mixer. The LO buffer is internally matched for wideband, single-ended operation with no external components.

The RF input port incorporates an integrated RF transformer and is internally matched over the 1.2GHz to 2.3GHz frequency range with no external components. The RF input match can be shifted down to 400MHz, or up to 2.7GHz, with a single shunt capacitor or inductor, respectively. The high level of integration minimizes the total solution cost, board space and system-level variation.

The LT5522 delivers high performance and small size without excessive power consumption.


*Operation over a wider frequency range is possible with reduced performance. Consult factory for information and assistance.

## TYPICAL APPLICATION



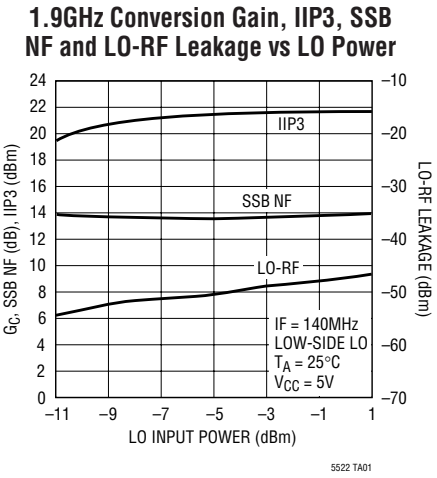



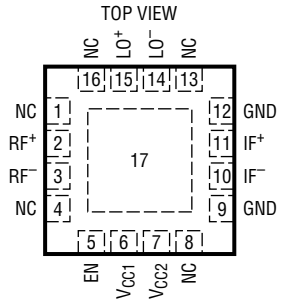

**Figure 1. High Signal Level Downmixer for Wireless Infrastructure**

## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Supply Voltage ..... 5.5V
Enable Voltage ..... –0.3V to $V_{CC}$ + 0.3V
LO Input Power ..... +10dBm
$LO^+$ to $LO^-$ Differential DC Voltage ..... ±1V
LO Input DC Common Mode Voltage ..... ±1V
RF Input Power ..... +10dBm
$RF^+$ to $RF^-$ Differential DC Voltage ..... ±0.2V
RF Input DC Common Mode Voltage ..... ±1V
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C
Junction Temperature ($T_J$) ..... 125°C

## PACKAGE/ORDER INFORMATION




UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 37°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

| ORDER PART NUMBER | UF PART MARKING |
|---|---|
| LT5522EUF | 5522 |

**Order Options** Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## DC ELECTRICAL CHARACTERISTICS

**(Test circuit shown in Figure 2) $V_{CC}$ = 5VDC, EN = high, $T_A$ = 25°C, unless otherwise noted. (Note 3)**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Power Supply Requirements ($V_{CC}$)** | | | | | |
| Supply Voltage | | 4.5 | 5 | 5.25 | VDC |
| Supply Current | $V_{CC}$ = 5V | | 56 | 68 | mA |
| Shutdown Current | EN = Low | | | 100 | µA |
| **Enable (EN) Low = Off, High = On** | | | | | |
| Input High Voltage (On) | | 3 | | | VDC |
| Input Low Voltage (Off) | | | | 0.3 | VDC |
| Enable Pin Input Current | EN = 5VDC | | 55 | 75 | µA |
| Turn On Time | | | 3 | | µs |
| Turn Off Time | | | 5 | | µs |

## AC ELECTRICAL CHARACTERISTICS

**(Notes 2, 3) (Test circuit shown in Figure 2).**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| RF Input Frequency Range | Shunt Capacitor on Pin 3 (Low Band)<br>No External Matching (Mid Band)<br>Shunt Inductor on Pin 3 (High Band) | 400 | 1200 to 2300 | 2700 | MHz<br>MHz<br>MHz |
| LO Input Frequency Range | No External Matching | 400 | | 2700 | MHz |
| IF Output Frequency Range | Requires Appropriate IF Matching | | 0.1 to 1000 | | MHz |
| RF Input Return Loss | $Z_O$ = 50Ω | | 15 | | dB |
| LO Input Return Loss | $Z_O$ = 50Ω | | 13 | | dB |
| IF Output Return Loss | $Z_O$ = 50Ω | | 18 | | dB |
| LO Input Power | | –10 | –5 | 0 | dBm |
| RF to LO Isolation | 50MHz to 2700MHz | | >45 | | dB |

## AC ELECTRICAL CHARACTERISTICS

**Cellular/PCS/UMTS downmixer application: $V_{CC}$ = 5V, EN = high, $T_A$ = 25°C, $P_{RF}$ = –7dBm (–7dBm/tone for 2-tone IIP3 tests, Δf = 1MHz), $f_{LO}$ = $f_{RF}$ – 140MHz, $P_{LO}$ = –5dBm, IF output measured at 140MHz, unless otherwise noted. (Notes 2, 3) (Test circuit shown in Figure 2).**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Conversion Gain | RF = 450MHz, High Side LO | | –2.0 | | dB |
| | RF = 900MHz | | –0.5 | | dB |
| | RF = 1800MHz | –2 | –0.2 | | dB |
| | RF = 1900MHz | | –0.1 | | dB |
| | RF = 2100MHz | | 0.2 | | dB |
| | RF = 2450MHz | | –0.7 | | dB |
| Conversion Gain vs Temperature | $T_A$ = –40°C to 85°C | | –0.02 | | dB/°C |
| Input 3rd Order Intercept | RF = 450MHz, High Side LO | | 22.3 | | dBm |
| | RF = 900MHz | | 25.0 | | dBm |
| | RF = 1800MHz | | 21.8 | | dBm |
| | RF = 1900MHz | | 21.5 | | dBm |
| | RF = 2100MHz | | 20.0 | | dBm |
| | RF = 2450MHz | | 16.8 | | dBm |
| Single Sideband Noise Figure (Note 4) | RF = 900MHz | | 12.5 | | dB |
| | RF = 1800MHz | | 13.9 | | dB |
| | RF = 2100MHz | | 14.3 | | dB |
| | RF = 2450MHz | | 15.6 | | dB |
| LO to RF Leakage | $f_{LO}$ = 400MHz to 2700MHz | | ≤–50 | | dBm |
| LO to IF Leakage | $f_{LO}$ = 400MHz to 2700MHz | | ≤–49 | | dBm |
| 2RF-2LO Output Spurious Product ($f_{RF}$ = $f_{LO}$ + $f_{IF}$/2) | 900MHz: $f_{RF}$ = 830MHz at –12dBm | | –73 | | dBc |
| | 1900MHz: $f_{RF}$ = 1830MHz at –12dBm | | –60 | | dBc |
| 3RF-3LO Output Spurious Product ($f_{RF}$ = $f_{LO}$ + $f_{IF}$/3) | 900MHz: $f_{RF}$ = 806.67MHz at –12dBm | | –72 | | dBc |
| | 1900MHz: $f_{RF}$ = 1806.67MHz at –12dBm | | –65 | | dBc |
| Input 1dB Compression | RF = 450MHz, High Side LO | | 12.0 | | dBm |
| | RF = 900MHz | | 10.8 | | dBm |
| | RF = 1900MHz | | 8.0 | | dBm |

**1150MHz CATV infrastructure application: $V_{CC}$ = 5V, EN = high, $T_A$ = 25°C, RF input = 1150MHz at –12dBm (–12dBm/tone for 2-tone IIP3 tests, Δf = 1MHz), LO input swept from 1200MHz to 2200MHz, $P_{LO}$ = –5dBm, IF output measured from 50MHz to 1050MHz unless otherwise noted. (Note 3) (Test circuit shown in Figure 3).**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Conversion Gain | $f_{LO}$ = 1650MHz, $f_{IF}$ = 500MHz | | –0.6 | | dB |
| Input 3rd Order Intercept | $f_{LO}$ = 1650MHz, $f_{IF}$ = 500MHz | | 23 | | dBm |
| Single Sideband Noise Figure (Note 4) | $f_{LO}$ = 1650MHz, $f_{IF}$ = 500MHz | | 14.3 | | dB |
| LO to RF Leakage | $f_{LO}$ = 1200MHz to 2200MHz | | ≤–51 | | dBm |
| LO to IF Leakage | $f_{LO}$ = 1200MHz to 2200MHz | | ≤–45 | | dBm |
| 2RF – LO Output Spurious Product | $P_{RF}$ = –12dBm (Single Tone), 50MHz ≤ $f_{IF}$ ≤ 900MHz | | ≤–63 | | dBc |
| 2RF1 – LO Output Spurious Product | 2-Tone 2nd Order Spurious Outputs | | –68 | | dBc |
| 2RF2 – LO Output Spurious Product | RF1 = 1147MHz, RF2 = 1153MHz, –15dBm/Tone | | –68 | | dBc |
| (RF1 + RF2) – LO Output Spurious Product | LO = 1650MHz, Spurs at 644MHz, 656MHz and 650MHz | | –63 | | dBc |
| RF Input Return Loss | 950MHz to 1350MHz, $Z_O$ = 50Ω | | >15 | | dB |
| LO Input Return Loss | 1200MHz to 2200MHz, $Z_O$ = 50Ω | | 13 | | dB |
| IF Output Return Loss | 50MHz to 1050MHz, $Z_O$ = 50Ω | | 10 | | dB |

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** 450MHz, 900MHz and 2450MHz performance measured with the following external RF input matching. 450MHz: C5 = 8.2pF, 5mm away from Pin 3 on the 50Ω input line. 900MHz: C5 = 2.2pF at Pin 3. 2450MHz: L3 = 3.9nH at Pin 3. See Figure 2.

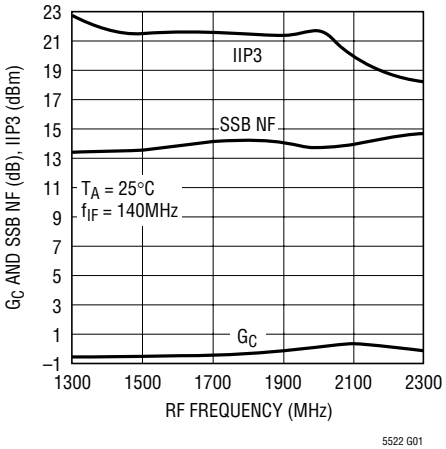
**Note 3:** Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 4:** SSB Noise Figure measurements performed with a small-signal noise source and bandpass filter on RF input, and no other RF signal applied.

## TYPICAL AC PERFORMANCE CHARACTERISTICS

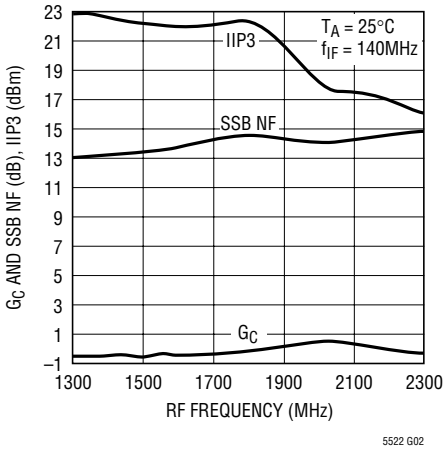
**Mid-band RF (no external RF matching)**
**$V_{CC}$ = 5V, EN = High, $T_A$ = 25°C, $P_{RF}$ = –7dBm (–7dBm/tone for 2-tone IIP3 tests, Δf = 1MHz), $P_{LO}$ = –5dBm, IF output measured at 140MHz, unless otherwise noted. (Test circuit shown in Figure 2).**

### Conv Gain, IIP3 and SSB NF vs RF Frequency (Low Side LO)



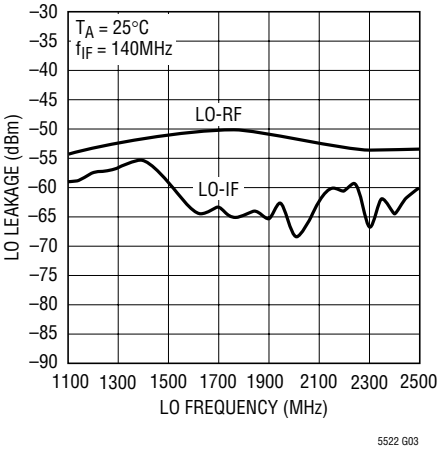

5522 G01

### Conv Gain, IIP3 and SSB NF vs RF Frequency (High Side LO)



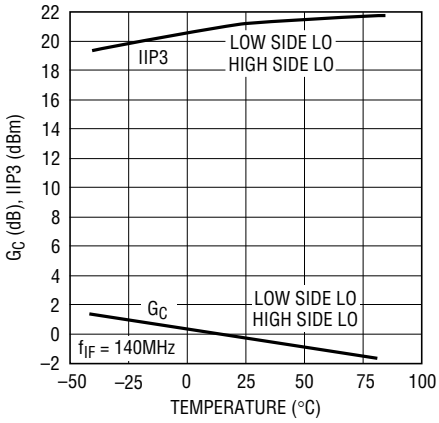

5522 G02

### LO Leakage vs LO Frequency



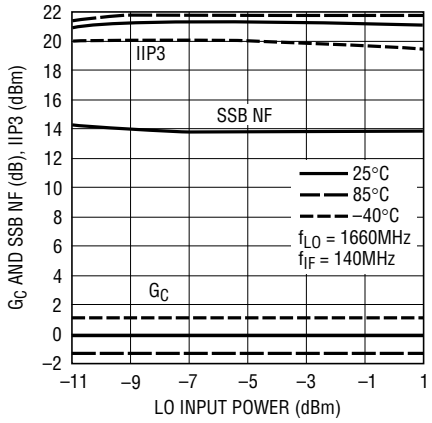

5522 G03

### Conv Gain and IIP3 vs Temperature (RF = 1800MHz)



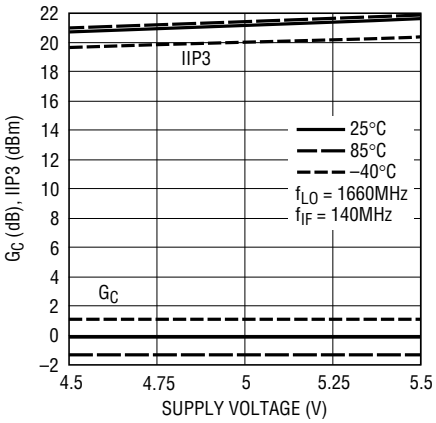

5522 G04

### Conv Gain, IIP3 and SSB NF vs LO Power (RF = 1800MHz)



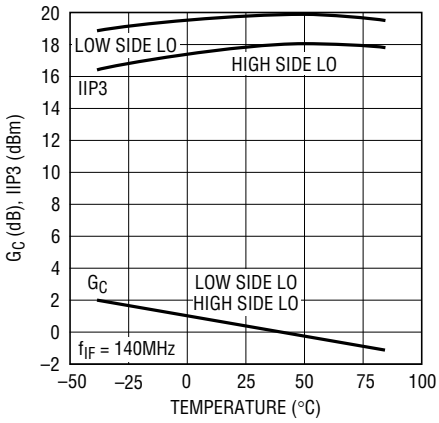

5522 G05

### Conv Gain and IIP3 vs Supply Voltage (RF = 1800MHz)



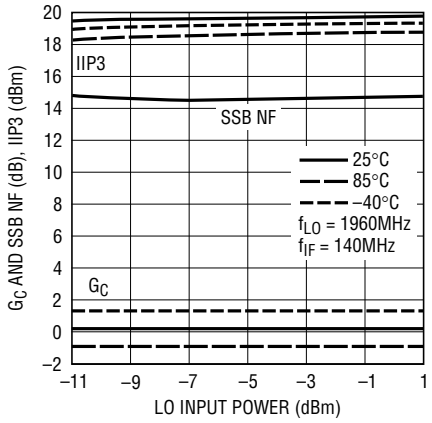

5522 G06

### Conv Gain and IIP3 vs Temperature (RF = 2100MHz)



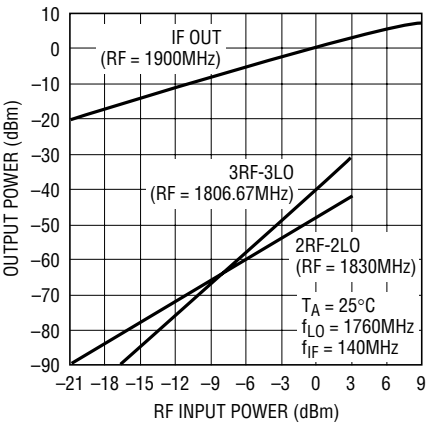

5522 G07

### Conv Gain, IIP3 and SSB NF vs LO Power (RF = 2100MHz)




5522 G08

### IF OUT, 2 × 2 and 3 × 3 Spurs vs RF Input Power (Single Tone)

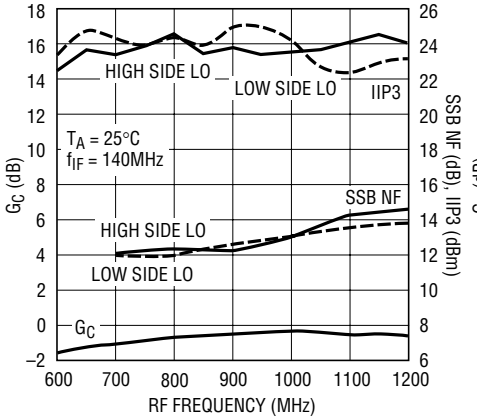



5522 G09

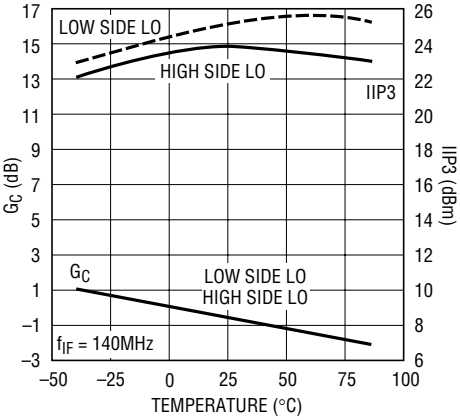
## TYPICAL AC PERFORMANCE CHARACTERISTICS

**Low-band RF (C5 = 2.2pF) and high-band RF (L3 = 3.9nH) $V_{CC}$ = 5V, EN = High, $T_A$ = 25°C, $P_{RF}$ = –7dBm (–7dBm/tone for 2-tone IIP3 tests, Δf = 1MHz), $P_{LO}$ = –5dBm, IF output measured at 140MHz, unless otherwise noted. (Test circuit shown in Figure 2).**

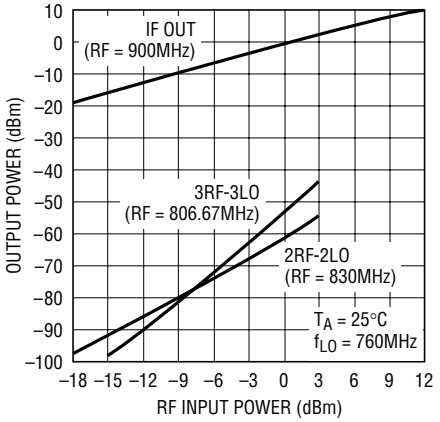
### Low Band Conv Gain, IIP3 and SSB NF vs RF Frequency



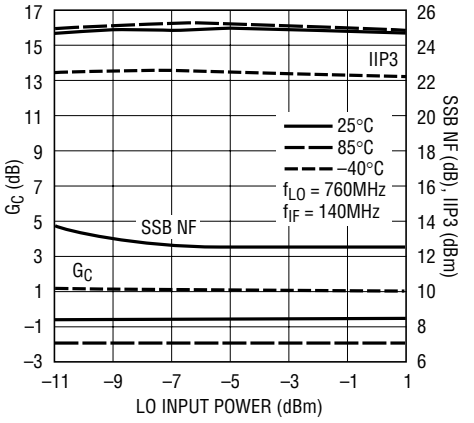

### Low Band Conv Gain and IIP3 vs Temperature (RF = 900MHz)



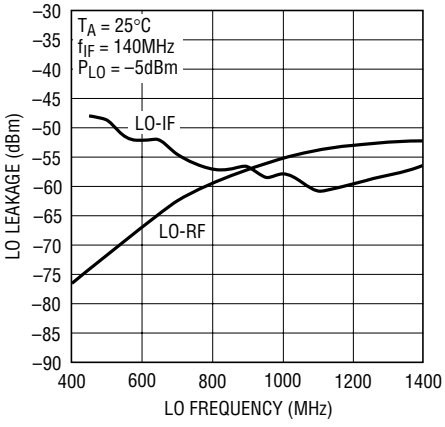

### Low Band IF OUT, 2 × 2 and 3 × 3 Spurs vs RF Input Power (Single Tone)



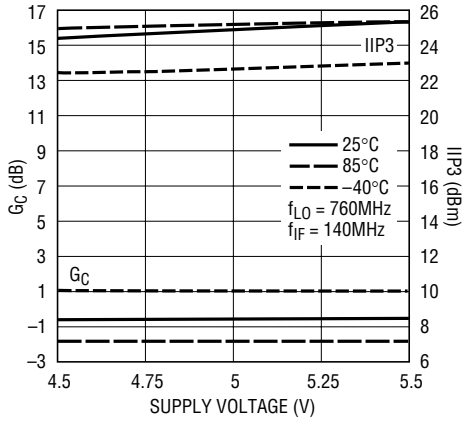

### Low Band Conv Gain, IIP3 and SSB NF vs LO Power (RF = 900MHz)



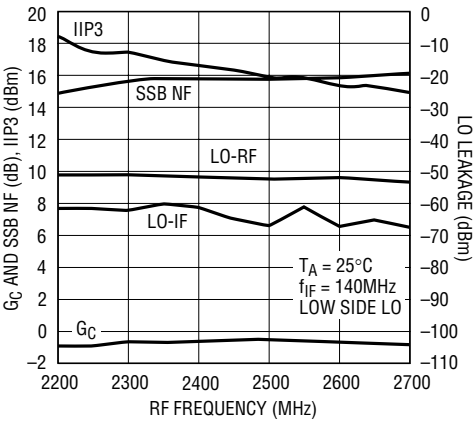

### LO Leakage vs LO Frequency (Low Band RF Match)



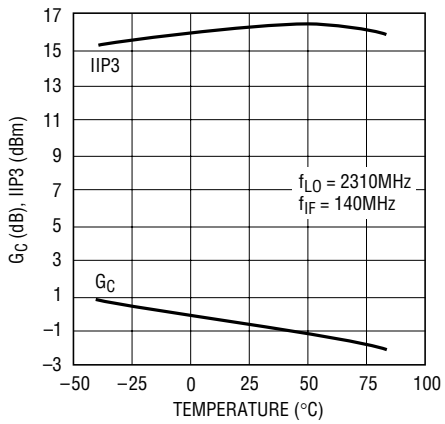

### Low Band Conv Gain and IIP3 vs Supply Voltage (RF = 900MHz)



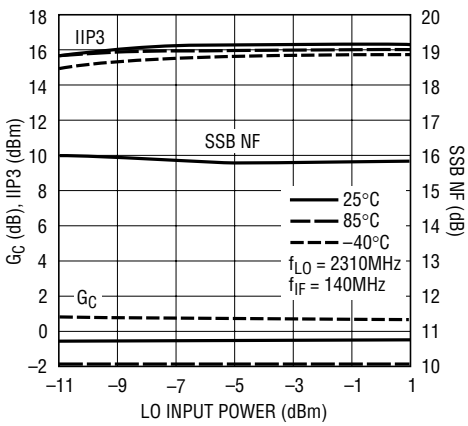

### High Band Conv Gain, IIP3, SSB NF and LO Leakage vs RF Frequency




### High Band Conv Gain and IIP3 vs Temperature (RF = 2450MHz)




### High Band Conv Gain, IIP3 and SSB NF vs LO Power (RF = 2450MHz)

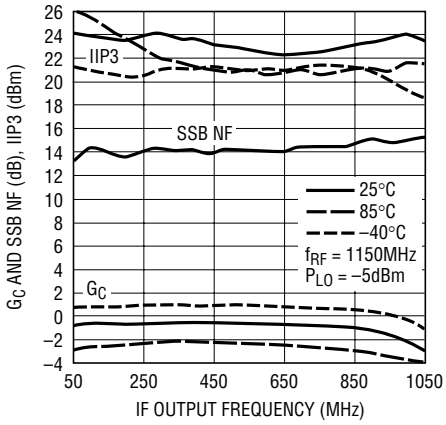


## TYPICAL AC PERFORMANCE CHARACTERISTICS

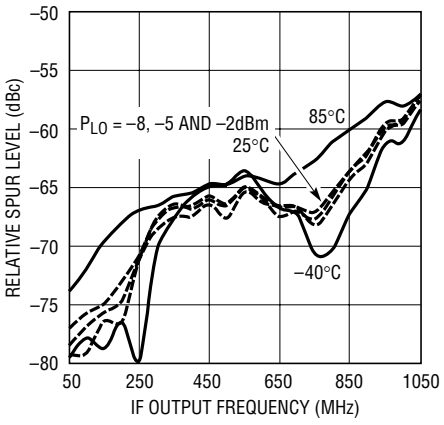
**CATV infrastructure downmixer**

**$V_{CC}$ = 5V, EN = High, $T_A$ = 25°C, $P_{RF}$ = 1150MHz at –12dBm (–12dBm/tone for 2-tone IIP3 tests, Δf = 1MHz), LO swept from 1200MHz to 2200MHz, $P_{LO}$ = –5dBm, IF output measured from 50MHz to 1050MHz, unless otherwise noted. (Test circuit shown in Figure 3)**

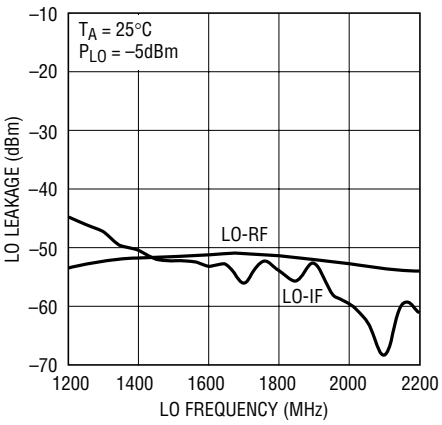
### Conv Gain, IIP3 and SSB NF vs IF Output Frequency



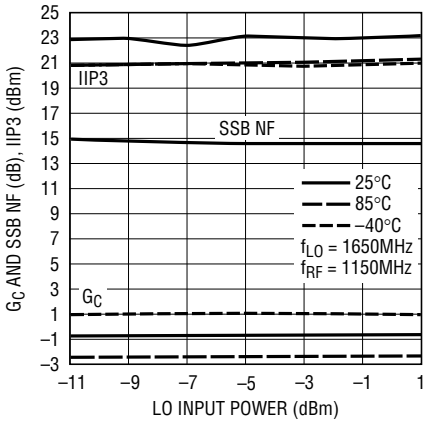

### 2RF-LO Spur vs IF Output Frequency ($P_{RF}$ = –12dBm)



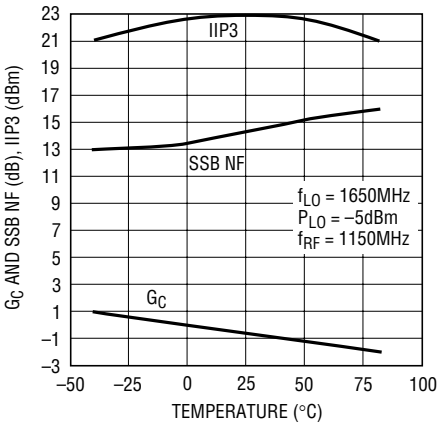

### LO Leakage vs LO Frequency



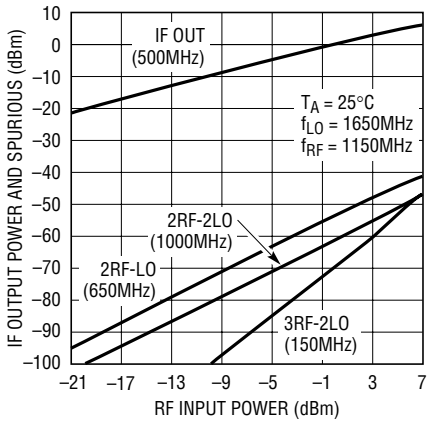

### Conv Gain, IIP3 and SSB NF vs LO Power (IF = 500MHz)



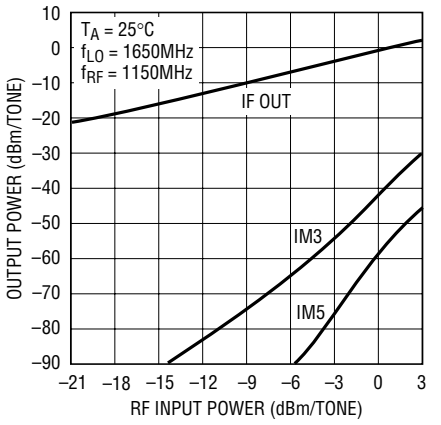

### Conv Gain, IIP3 and SSB NF vs Temperature (IF = 500MHz)




### IF Output Power and Spurious Products vs RF Input Power (Single Tone)



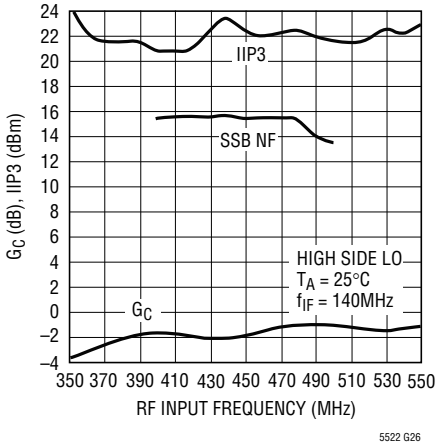

### IF Output Power, IM3 and IM5 vs RF Input Power (Two Input Tones)



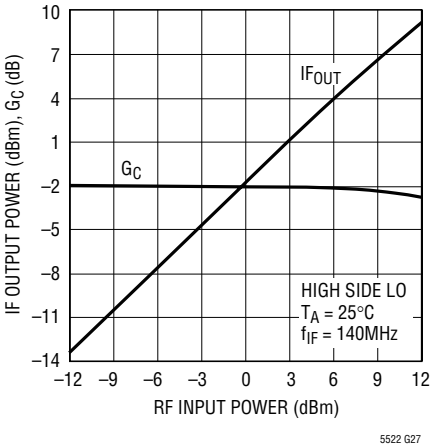
## TYPICAL AC PERFORMANCE CHARACTERISTICS

**450MHz Application (C5 = 8.2pF, 5mm away from Pin 3) $V_{CC}$ = 5V, EN = High, $T_A$ = 25°C, $P_{RF}$ = –7dBm (–7dBm/tone for 2-tone IIP3 tests, Δf = 1MHz), $P_{LO}$ = –5dBm, IF output measured at 140MHz, unless otherwise noted. (Test circuit shown in Figure 2)**

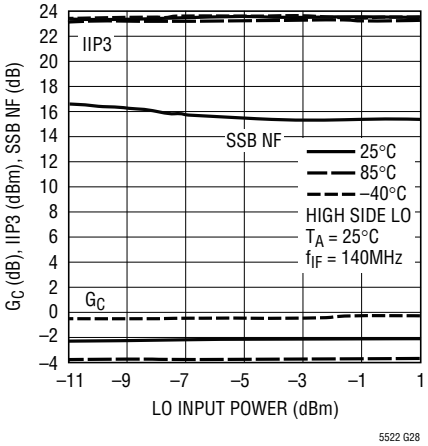
**Conv Gain, IIP3 and SSB NF vs RF Frequency (High Side LO)**




**Single Tone IF Output Power and Conv Gain vs RF Input Power (RF = 450MHz)**



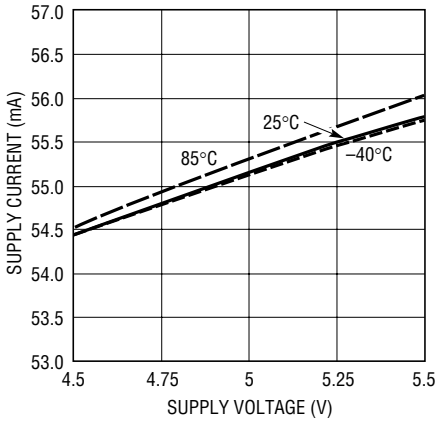

**Conv Gain, IIP3 and SSB NF vs LO Input Power (RF = 450MHz)**



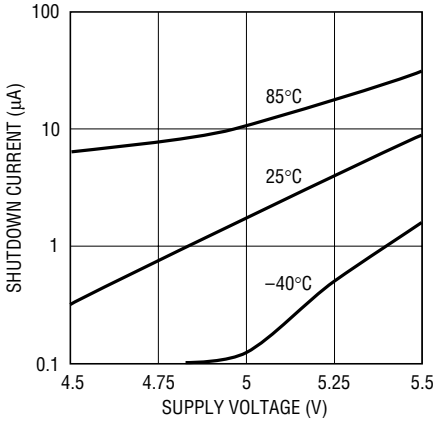

## TYPICAL DC PERFORMANCE CHARACTERISTICS

**(Test circuit shown in Figure 2)**

**Supply Current vs Supply Voltage**




**Shutdown Current vs Supply Voltage**



## PIN FUNCTIONS

**NC (Pins 1, 4, 8, 13, 16):** Not Connected Internally. These pins should be grounded on the circuit board for improved LO to RF and LO to IF isolation.

**$RF^+$, $RF^-$ (Pins 2, 3):** Differential Inputs for the RF Signal. The RF input signal should be applied to the $RF^-$ pin (Pin 3) and the $RF^+$ pin (Pin 2) must be connected to ground. These pins are the primary side of the RF input balun which has low DC resistance. If the RF source is not DC blocked, then a series blocking capacitor must be used.

**EN (Pin 5):** Enable Pin. When the input enable voltage is higher than 3V, the mixer circuits supplied through Pins 6, 7, 10 and 11 are enabled. When the input enable voltage is less than 0.3V, all circuits are disabled. Typical input EN pin current is 55µA for EN = 5V and 0µA when EN = 0V. The EN pin should not be left floating. Under no conditions should the EN pin voltage exceed $V_{CC}$ + 0.3V, even at start-up.

**$V_{CC1}$ (Pin 6):** Power Supply Pin for the LO Buffer Circuits. Typical current consumption is 22mA. This pin should be externally connected to the $V_{CC2}$ pin and decoupled with 0.01µF and 3.3µF capacitors.

**$V_{CC2}$ (Pin 7):** Power Supply Pin for the Bias Circuits. Typical current consumption is 4mA. This pin should be externally connected to the $V_{CC1}$ pin and decoupled with 0.01µF and 3.3µF capacitors.

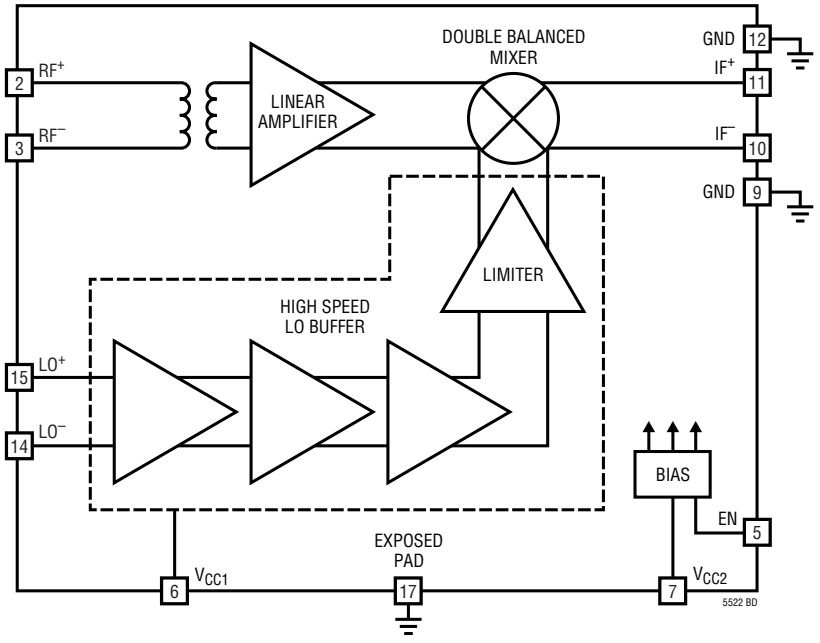
**GND (Pins 9, 12):** Ground. These pins are internally connected to the backside ground for improved isolation. They should be connected to RF ground on the circuit board, although they are not intended to replace the primary grounding through the backside contact of the package.

**$IF^-$, $IF^+$ (Pins 10, 11):** Differential Outputs for the IF Signal. An impedance transformation may be required to match the outputs. These pins must be connected to $V_{CC}$ through impedance matching inductors, RF chokes or a transformer center-tap.

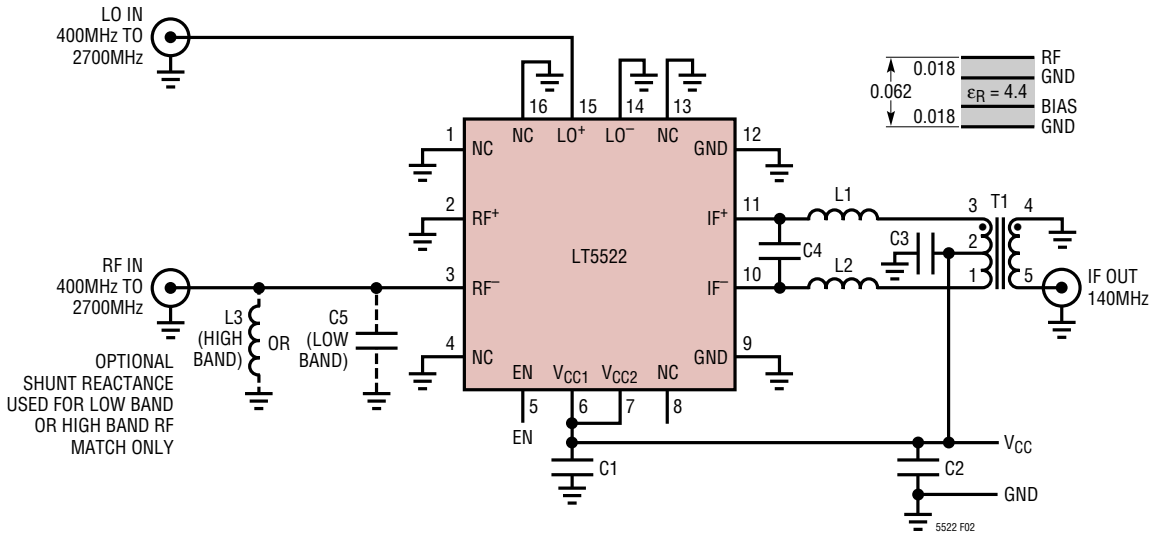
**$LO^-$, $LO^+$ (Pins 14, 15):** Differential Inputs for the Local Oscillator Signal. The LO input can also be driven single ended by connecting one input to ground. These pins are internally matched for 50Ω single-ended operation. If the LO source is not AC-coupled, then a series blocking capacitor must be used.

**Exposed Pad (Pin 17):** Circuit Ground Return for the Entire IC. This must be soldered to the printed circuit board ground plane.

## BLOCK DIAGRAM

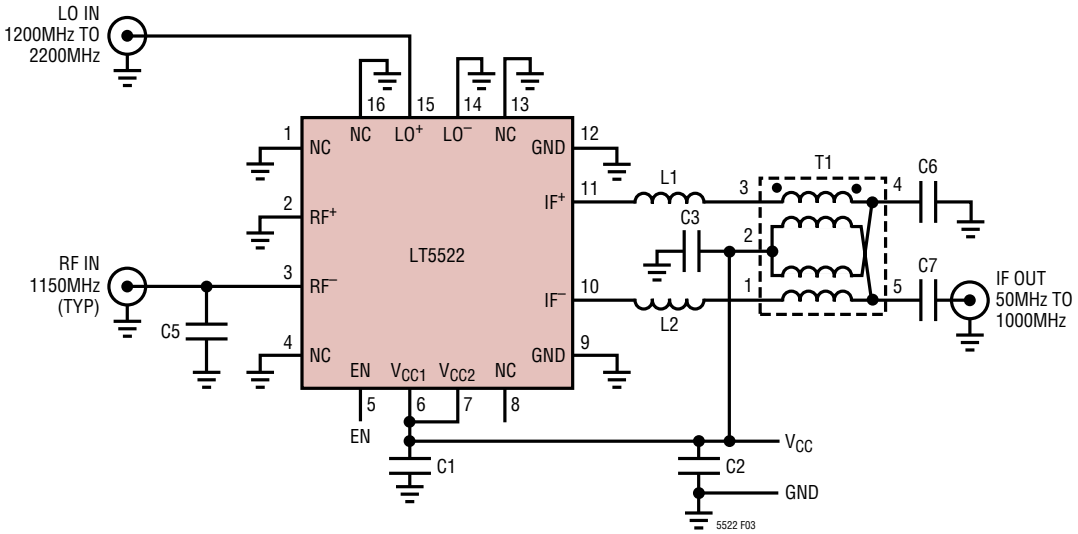


## TEST CIRCUITS




| REF DES | VALUE | SIZE | PART NUMBER | REF DES | VALUE | SIZE | PART NUMBER |
|---|---|---|---|---|---|---|---|
| C1 | 0.01µF | 0402 | Murata GRP155R71C103K | L1, L2 | 82nH | 0603 | Coilcraft 0603CS-82NX |
| C2 | 3.3µF | 1206 | Taiyo Yuden LMK316BJ475ML | T1 | 4:1 | | M/A-Com ETC4-1-2 (2-800MHz) |
| C3 | 100pF | 0402 | Murata GRP1555C1H101J | C5 | 2.2pF | 0402 | Murata GRP1555C1H1R5C (For Low Band Operation Only) |
| C4 | 1.5pF | 0402 | Murata GRP1555C1H1R5C | L3 | 3.9nH | 0402 | Coilcraft 0402CS-3N9X (For High Band Operation Only) |

**Figure 2. Test Schematic for Downmixer Application (140MHz IF) (DC689A)**




| REF DES | VALUE | SIZE | PART NUMBER | REF DES | VALUE | SIZE | PART NUMBER |
|---|---|---|---|---|---|---|---|
| C1 | 0.01µF | 0402 | Murata GRP155R71C103K | C5 | 1.5pF | | Murata GRP1555C1H1R5C |
| C2 | 3.3µF | 1206 | Taiyo Yuden LMK316BJ475ML | L1, L2 | 18nH | 0402 | Toko LL1005-FH18NJ |
| C3, C6, C7 | 330pF | 0402 | Murata GRP155R71H331K | T1 | 4:1 | | M/A-Com MABAES0054 (5-1000MHz) |

**Figure 3. Test Schematic for CATV Infrastructure Downmixer Application (50MHz to 1000MHz IF) (DC651A)**

## APPLICATIONS INFORMATION

### Introduction

The LT5522 consists of a high linearity double-balanced mixer, RF buffer amplifier, high speed limiting LO buffer amplifier and bias/enable circuits. The IC has been optimized for downconverter applications where the RF input signal is in the 400MHz to 2.7GHz range and the LO signal is in the 400MHz to 2.7GHz range. Operation over a wider RF input frequency range is possible with reduced performance.

The IF output can be matched for IF frequencies as low as 100kHz or as high as 1GHz. The RF, LO and IF ports are all differential, although the RF and LO ports are internally matched for single-ended drive as shown in Figure 2. The LT5522 is characterized and production-tested with single-ended RF and LO drive. Low side or high side LO injection can be used.

Two evaluation boards are available. The standard board is intended for most applications, including cellular, PCS, UMTS and 2.4GHz. A schematic is shown in Figure 2 and the board layout is shown in Figure 18. The 140MHz IF output frequency on the standard board is easily changed by modifying the IF matching elements. The second board, intended for CATV applications, incorporates a wideband IF output balun. The CATV evaluation schematic is shown in Figure 3 and the board layout is shown in Figure 19.

### RF Input Port

The mixer's RF input, shown in Figure 4, consists of an integrated balun and a high linearity differential amplifier. The primary terminals of the balun are connected to the $RF^+$ and $RF^-$ pins (Pins 2 and 3, respectively). The secondary side of the balun is internally connected to the amplifier's differential inputs. For single-ended operation, the $RF^+$ pin is grounded and the $RF^-$ pin becomes the RF input. It is also possible to ground the $RF^-$ pin and drive the $RF^+$ pin, although the LO to RF isolation will degrade slightly.

The RF source must be AC-coupled since one terminal of the balun's primary is grounded. If the RF source has DC voltage present, then a coupling capacitor must be used in series with the RF input pin.

As shown in Figure 5, the RF input return loss, with no external matching, is greater than 10dB from 1.2GHz to 2.4GHz. The RF input match can be shifted down in frequency by adding a shunt capacitor at the RF input. Two examples are plotted in Figure 5. A 2.2pF capacitor, located near Pin 3, produces a 900MHz match. An 8.2pF capacitor, located 5mm away from Pin 3 (on the 50Ω line), produces a 450MHz match. The RF input match can also be shifted up in frequency by adding a shunt inductor near Pin 3. One example is plotted in Figure 5, where a 3.9nH inductor produces a 2.3GHz to 2.8GHz match.

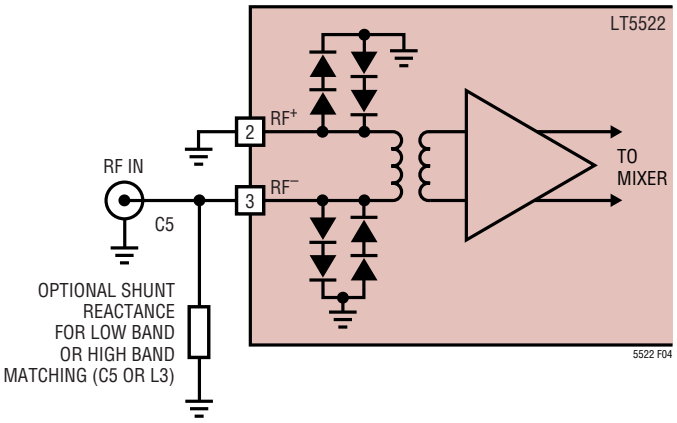



Figure 4. RF Input Schematic

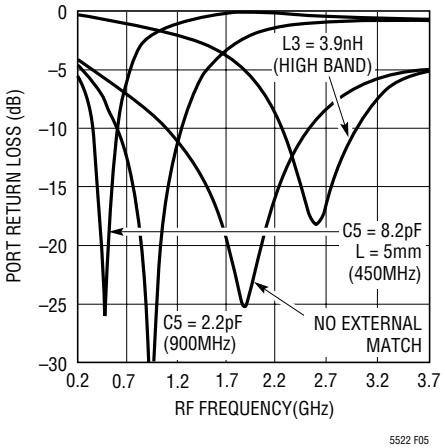



Figure 5. RF Input Return Loss

## APPLICATIONS INFORMATION

RF input impedance and S11 versus frequency are shown in Table 1. The listed data is referenced to the RF⁻ pin with the RF⁺ pin grounded (no external matching). This information can be used to simulate board-level interfacing to an input filter, or to design a broadband input matching network.

A broadband RF input match is easily realized using the shunt inductor/series capacitor network shown in Figure 6. This network provides good return loss at low and high frequencies simultaneously, with reasonable midband return loss. As shown in Figure 7, the RF input return loss is greater than 12dB from 715MHz to 2.3GHz using the element values shown in Figure 6. The input match is optimum at 850MHz and 1900MHz, ideal for triband GSM applications.

**Table 1. RF Port Input Impedance vs Frequency**

| FREQUENCY (MHZ) | INPUT IMPEDANCE | S11 | |
|---|---|---|---|
| | | MAG | ANGLE |
| 50 | 10.4 + j2.6 | 0.660 | 173.5 |
| 500 | 19.5 + j20.6 | 0.507 | 129.5 |
| 700 | 24.1 + j24.2 | 0.454 | 118.7 |
| 900 | 28.6 + j26.1 | 0.407 | 111.1 |
| 1100 | 33.7 + j26.2 | 0.353 | 104.4 |
| 1300 | 39.5 + j24.3 | 0.285 | 98.2 |
| 1500 | 45.6 + j18.9 | 0.199 | 92.0 |
| 1700 | 50.2 + j9.7 | 0.096 | 83.0 |
| 1900 | 50.5 – j2.2 | 0.023 | –76.0 |
| 2100 | 45.6 – j13.2 | 0.143 | –100.7 |
| 2300 | 38.0 – j19.9 | 0.259 | –108.3 |
| 2500 | 30.4 – j22.8 | 0.360 | –114.8 |
| 2700 | 24.5 – j23.0 | 0.440 | –120.7 |
| 3000 | 18.7 – j20.9 | 0.525 | –129.4 |

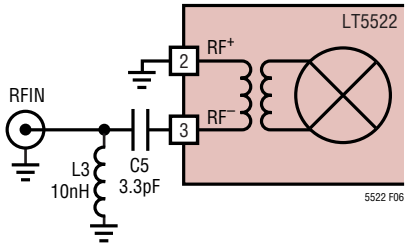



**Figure 6. Wideband RF Input Matching**

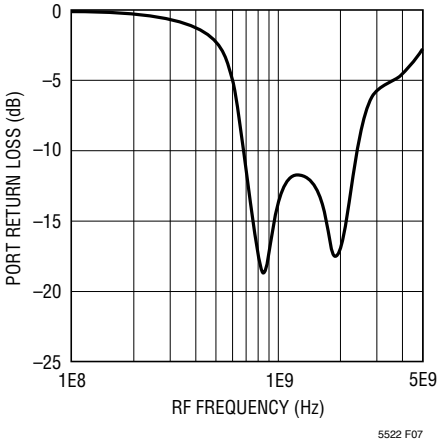



**Figure 7. RF Input Return Loss Using Wideband Matching Network**

### LO Input Port

The LO buffer amplifier consists of high speed limiting differential amplifiers, designed to drive the mixer quad for high linearity. The LO⁺ and LO⁻ pins are designed for single-ended drive, although differential drive can be used if a differential LO source is available. A schematic is shown in Figure 8. Measured return loss is shown in Figure 9.

The LO source must be AC-coupled to avoid forward biasing the ESD diodes. If the LO source has DC voltage present, then a coupling capacitor must be used in series with the LO input pin.

LO input impedance and S11 versus frequency are shown in Table 2. The listed data is referenced to the LO⁺ pin with the LO⁻ pin grounded.

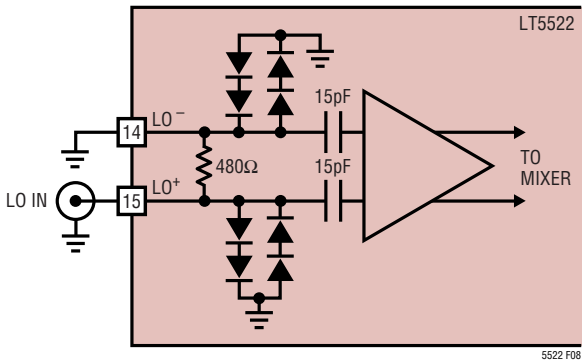



**Figure 8. LO Input Schematic**

## APPLICATIONS INFORMATION

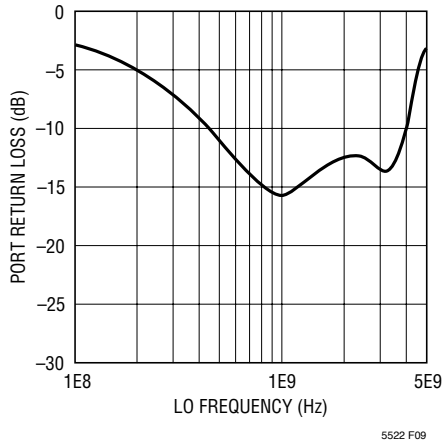



**Figure 9. LO Input Return Loss**

**Table 2. LO Port Input Impedance vs Frequency**

| FREQUENCY (MHZ) | INPUT IMPEDANCE | S11 | |
|---|---|---|---|
| | | MAG | ANGLE |
| 100 | 200.5 – j181.0 | 0.763 | –14.3 |
| 250 | 55.9 – j61.6 | 0.505 | –54.4 |
| 500 | 44.6 – j27.7 | 0.286 | –84.8 |
| 1000 | 37.9 – j7.8 | 0.163 | –142.1 |
| 1500 | 33.6 – j1.8 | 0.197 | –172.3 |
| 2000 | 31.0 – j0.3 | 0.234 | –178.9 |
| 2500 | 30.6 – j0.4 | 0.240 | –178.4 |
| 3000 | 31.8 – j1.0 | 0.223 | –176.0 |

### IF Output Port

The IF outputs, $IF^+$ and $IF^-$, are internally connected to the collectors of the mixer switching transistors (see Figure 10). Both pins must be biased at the supply voltage, which can be applied through the center-tap of a transformer or through matching inductors. Each IF pin draws 15mA of supply current (30mA total). For optimum single-ended performance, these differential outputs should be combined externally through an IF transformer. Both evaluation boards include IF transformers for impedance transformation and differential to single-ended transformation.

The IF output impedance can be modeled as 400Ω in parallel with 1pF. An equivalent small-signal model (including bondwire inductance) is shown in Figure 11. For most applications, the bondwire inductance can be ignored.

For IF frequencies below 140MHz, an 8:1 transformer connected across the IF pins will perform impedance transformation and provide a single-ended 50Ω output. No other matching is required. Measured performance using this technique is shown in Figure 12. Output return loss is shown in Figure 13.

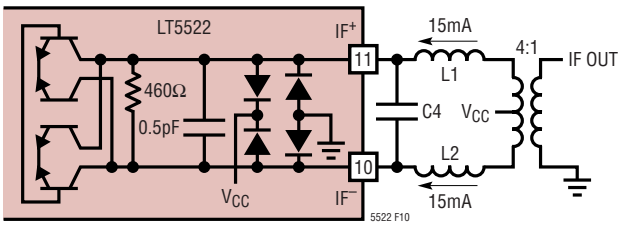



**Figure 10. IF Output with External Matching**

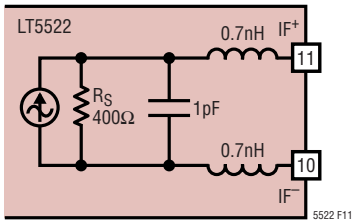



**Figure 11. IF Output Small-Signal Model**

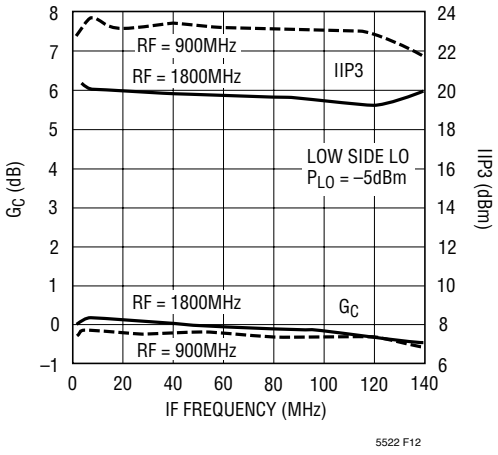



**Figure 12. Typical Conversion Gain and IIP3 Using an 8:1 IF Transformer**

## APPLICATIONS INFORMATION

Higher linearity and lower LO-IF leakage can be realized by using the simple, three element lowpass matching network shown in Figure 10. Matching elements C4, L1 and L2 form a 400Ω to 200Ω lowpass matching network which is tuned to the desired IF frequency. The 4:1 transformer then transforms the 200Ω differential output to 50Ω single-ended. The value of C4 is reduced by 1pF to account for the equivalent internal capacitance.

For optimum linearity, C4 must be located close to the IF pins. Excessive trace length or inductance between the IF pins and C4 will increase the amplitude of the image output and reduce voltage swing headroom for the desired IF frequency. High Q wire-wound chip inductors (L1 and L2) improve the mixer's conversion gain by a few tenths of a dB, but have little effect on linearity.

This matching network is most suitable for IF frequencies of 40MHz or above. Below 40MHz, the value of the series inductors (L1 and L2) is high, and could cause stability problems, depending on the inductor value and parasitics. Therefore, the 8:1 transformer technique is recommended for low IF frequencies.

Suggested matching network values for several IF frequencies are listed in Table 3. Measured output return losses for the 140MHz match and the wideband CATV match are plotted in Figure 13.

**Table 3. IF Matching Element Values (See Figure 10)**

| IF FREQUENCY (MHz) | L1, L2 (nH) | C4 (pF) | IF TRANSFORMER |
|---|---|---|---|
| 2-140 | Short | — | TC8-1 (8:1) |
| 70 | 220 | 4.7 | ETC4-1-2 (4:1) |
| 140 | 82 | 1.5 | |
| 240 | 56 | 0.5 | |
| 380 | 39 | — | |
| 50-1000 (CATV) | 18 | — | MABAES0054 (4:1) |

For fully differential IF architectures, the IF transformer can be eliminated. As shown in Figure 14, supply voltage to the mixer's IF pins is applied through matching inductors in a bandpass IF matching network. The values of L1, L2 and C4 are calculated to resonate at the desired IF frequency with a quality factor that satisfies the required IF bandwidth. The L and C values are then adjusted to

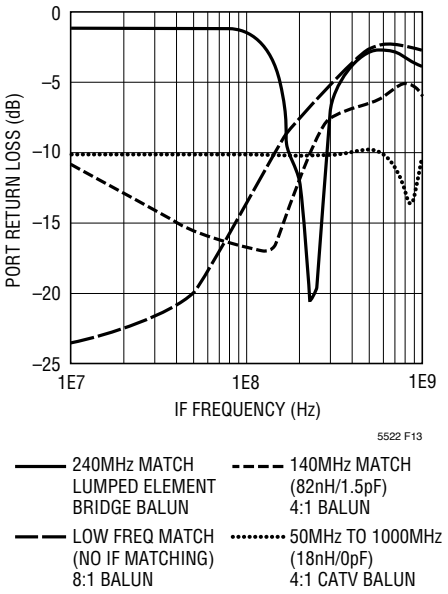



**Figure 13. Typical IF Output Return Losses for Various Matching Techniques**

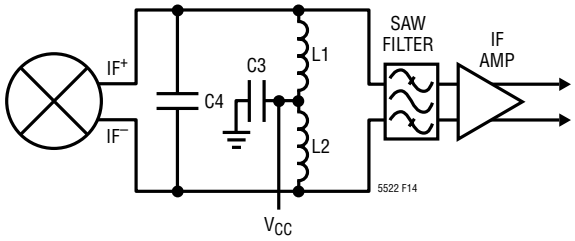



**Figure 14. Bandpass IF Matching for Differential IF Architectures**

account for the mixer's internal 1pF capacitance and the SAW filter's input capacitance. In this case, the differential IF output impedance is 400Ω, since the bandpass network does not transform the impedance.

For low cost applications, it is possible to replace the IF transformer with a lumped-element network which produces a single-ended 50Ω output. One approach is shown in Figure 15, where L1, L2, C4 and C6 form a narrowband bridge balun. The L and C values are calculated to realize a 180 degree phase shift at the desired IF frequency using the equations listed below. Inductor L4 is calculated to cancel the internal 1pF capacitance. L3 also supplies bias voltage to the IF+ pin. Low cost multilayer chip inductors are adequate for L1 and L2. A high Q wire-wound chip

## APPLICATIONS INFORMATION

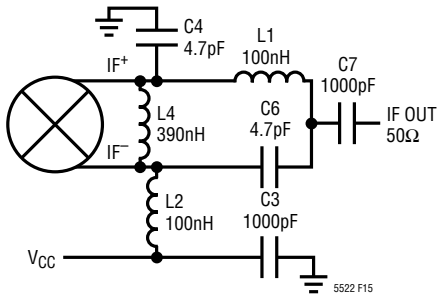



**Figure 15. Narrowband Bridge IF Balun (240MHz Example)**

inductor is recommended for L4 to preserve conversion gain and minimize DC voltage drop to the IF+ pin. C7 is a DC blocking capacitor and C3 is a bypass capacitor.

$$L1, L2 = \frac{\sqrt{Z_{IF} \bullet Z_{OUT}}}{\omega} \qquad (Z_{IF} = 400)$$

$$C4, C6 = \frac{1}{\omega \bullet \sqrt{Z_{IF} \bullet Z_{OUT}}}$$

The narrowband bridge IF balun delivers good conversion gain, linearity and noise figure over a limited IF bandwidth. LO-IF leakage is approximately –32dBm, which is 17dB worse than that obtained with a transformer. Typical IF output return loss is plotted in Figure 13 for comparison with other matching methods. Typical mixer performance versus RF input frequency for 240MHz IF matching is shown in Figure 16. Typical performance versus IF output frequency for the same circuit is shown in Figure 17. The results in Figure 17 show that the usable IF bandwidth is approximately ±25MHz, assuming tight tolerance matching components. Contact the factory for application assistance with this circuit.

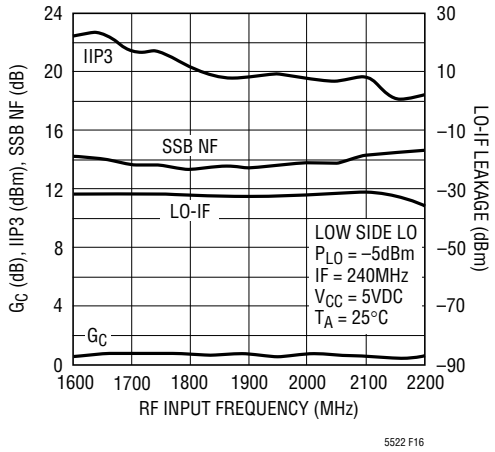



**Figure 16. Typical Performance Using a Narrowband Bridge Balun (Swept RF)**

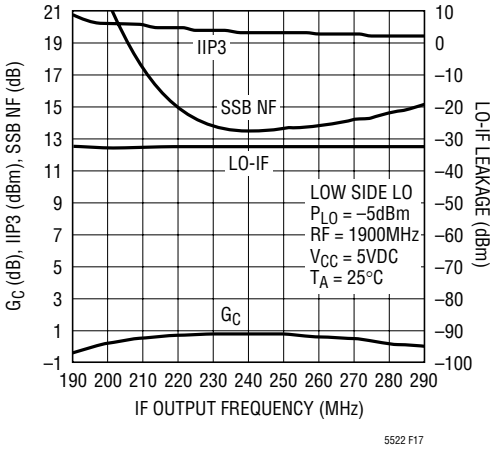
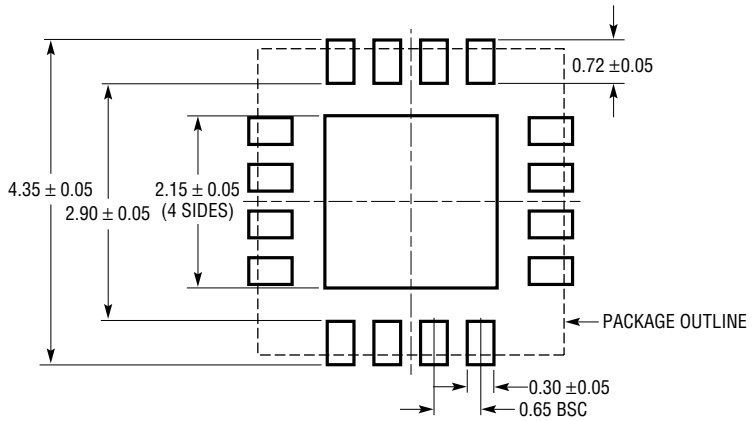


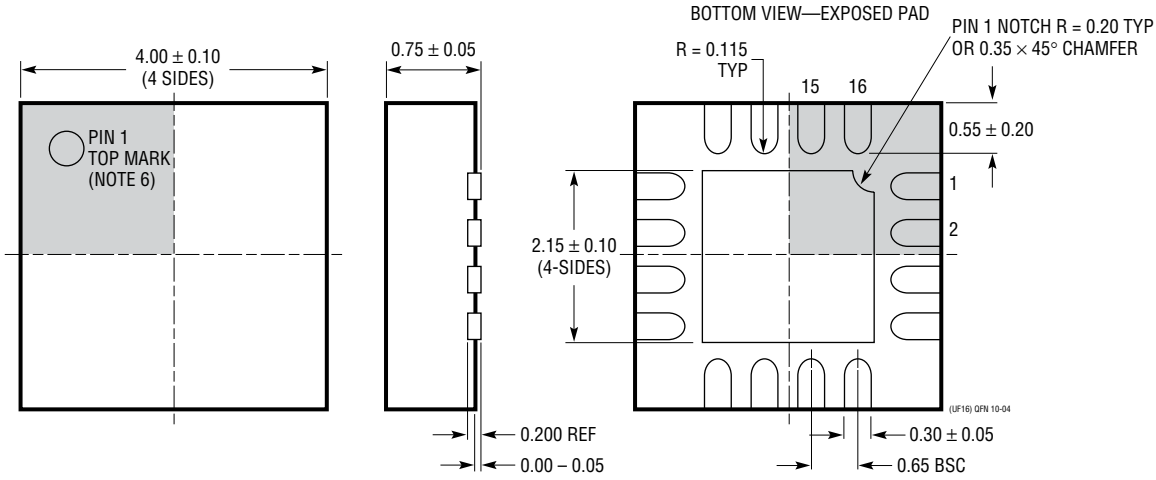

**Figure 17. Typical Performance Using a Narrowband Bridge Balun (Swept IF)**

# PACKAGE DESCRIPTION

**UF Package**
**16-Lead Plastic QFN (4mm × 4mm)**
(Reference LTC DWG # 05-08-1692)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS




NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE