

LTC4063

Standalone Linear Li-Ion Charger with Micropower Low Dropout Linear Regulator

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including 6522118.

The LTC®4063 is a standalone linear charger for single cell lithium-ion batteries with an adjustable low dropout linear regulator (LDO). The adjustable LDO regulates an output voltage between 1.2V to 4.2V at up to 100mA load current. When the input supply (wall adapter or USB supply) is removed, the LDO regulates the output voltage without interruption. The battery charger and LDO regulator can

No external sense resistor or external blocking diode is required for charging due to the internal MOSFET architecture. Internal thermal feedback regulates the charge current to maintain a constant die temperature during high power operation or high ambient temperature conditions. The float voltage is fixed at 4.2V and the charge current is programmed with an external resistor. Charge termination methods include minimum charge current or maximum time. With power applied, the LTC4063 can be put into shutdown mode to reduce the supply current to 35µA and

Features Description

- ⁿ **Charge Current Programmable up to 1A**
- ⁿ **Integrated 100mA Adjustable Low Dropout Linear Regulator**
- ⁿ **Charges Single Cell Li-Ion Batteries Directly from USB Port**
- Preset Charge Voltage with ±0.35% Accuracy
- ⁿ **No External MOSFET, Sense Resistor or Blocking Diode Needed**
- ⁿ **Thermal Regulation Maximizes Charge Rate without Risk of Overheating**
- ⁿ **Adjustable LDO Output Voltage Range: 1.2V to 4.2V**
- **Programmable Charge Termination Timer**
- Programmable Charge Current Detection/Termination
- SmartStart[™] Prolongs Battery Life
- Charge Status Output
- 35µA Charger Quiescent Current in Shutdown
- 15µA LDO Quiescent Current
- Available in a Low Profile (0.75mm) 10-Lead $(3mm \times 3mm)$ DFN Package

Applications

- Handheld Computers
- Portable MP3 Players
- Digital Cameras

Typical Application

Single Cell Li-Ion Battery Charger with Regulated 3V Output (C/10 Termination)

Complete Charge Cycle (900mAh Battery)

Other features include smart recharge, undervoltage lockout, LDO current limiting and a charge status pin to

the battery drain current to less than 2µA.

indicate when the charge cycle has completed. \sqrt{J} , LT, LTC, LTM, Linear Technology and the Linear logo are registered trademarks and SmartStart, ThinSOT and PowerPath are trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners. Protected by U.S. Patents

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Absolute Maximum Ratings Pin Configuration

Order Information

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

Electrical Characteristics **The** l **denotes the specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C. VCC = 5V, unless otherwise noted.**

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temperature range, otherwise specifications are at TA = 25°C. VCC = 5V, unless otherwise noted.

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC4063EDD is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Failure to correctly solder the Exposed Pad of the package to the PC board will result in a thermal resistance much higher than 40°C/W. **Note 4:** Supply current includes PROG pin current and IDET pin current (approximately 100µA each) but does not include any current delivered to the battery through the BAT pin (approximately 100mA).

Note 5: Does not include LDO supply current.

Note 6: The LDO is partially powered from V_{CC}, thus reducing the supply current from the BAT pin.

Note 7: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Overtemperature protection will become active at a junction temperature greater than the maximum operating temperature. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 8: Defined by long term current density limitations.

Typical Performance Characteristics **TA = 25°C, unless otherwise noted.**

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Typical Performance Characteristics **TA = 25°C, unless otherwise noted.**

Recharge Threshold Voltage vs Temperature

Power FET On-Resistance

CHGEN Pin Pull-Down Resistance vs Temperature

vs Temperature Shutdown Current vs Temperature

FB Pin Regulated Voltage

CHGEN Pin Threshold Voltage (On-to-Off) vs Temperature

FB Pin Regulated Voltage vs Temperature

Typical Performance Characteristics **TA = 25°C, unless otherwise noted.**

Pin Functions

BAT (Pin 1): Charger Output and Regulator Input. This pin provides charge current to the battery and regulates the final float voltage to 4.2V. This pin also supplies power to the LDO regulator.

OUT (Pin 2): LDO Regulator Output. This pin should be bypassed with a ≥2µF low ESR capacitor as close to the pin as possible for best performance. The minimum V_{OUT} is 1.2V.

FB (Pin 3): Regulator Feedback Input. The voltage on this pin is compared to the internal reference voltage (800mV) by the error amplifier to keep the output voltage in regulation. An external resistor divider between OUT and FB sets the output voltage.

LDOEN (Pin 4): LDO Enable Input. A logic high on the LDOEN pin shuts down the LDO. In this state, OUT becomes high impedance and the battery drain current drops to less than 5µA. A logic low on the LDOEN pin enables the LDO regulator. A 2M pull-down resistor defaults the LDO to its enabled state.

CHGEN (Pin 5): Charger Enable Input. A logic high on the CHGEN pin places the charger into shutdown mode, where the I_{CC} quiescent current is less than 65 μ A. A logic low on this pin enables battery charging. A 2M pull-down resistor to ground defaults the charger to its enabled state.

CHRG (Pin 6): Open-Drain Charge Status Output. The charge status indicator pin has two states: pull-down and high impedance. This output can be used as a logic interface or an LED driver. In the pull-down state, an NMOS transistor capable of sinking 10mA pulls down on the CHRG pin. The state of this pin is dependent on the value of I_{DETECT} as well as the termination method being used. See Applications Information.

TIMER(Pin7): Timer Program and Termination Select Pin. This pin selects which method is used to terminate the charge cycle. Connecting a capacitor, C_{TIMER} , to ground selects Charge Time termination. The charge time is set by the following formula:

Time (Hours) = 3 Hours
$$
\cdot \frac{C_{TIMER}}{0.1 \mu F}
$$
 or
C_{TIMER} = 0.1 $\mu F \cdot \frac{Time (Hours)}{3 (Hours)}$

Connecting the pin to ground selects Charge Current termination, while connecting the pin to V_{CC} selects User termination. See Applications Information.

IDET (Pin 8): Current Detection Threshold Program Pin. The current detection threshold, I_{DETECT} , is set by connecting a resistor, R_{DFT} , to ground. I_{DFTFCT} is set by the following formula:

$$
I_{\text{DETECT}} = \frac{R_{\text{PROG}}}{10R_{\text{DET}}} \cdot I_{\text{CHG}} = \frac{100V}{R_{\text{DET}}}
$$
 or

$$
R_{\text{DET}} = \frac{100V}{I_{\text{DETECT}}}
$$

The CHRG pin becomes high impedance when the charge current drops below I_{DFTECT} . I_{DFTECT} can be set to 1/10th the programmed charge current by connecting IDET directly to PROG. See Applications Information.

This pin is clamped to approximately 2.4V. Driving this pin to voltages beyond the clamp voltage can draw large currents and should be avoided.

PROG (Pin 9): Charge Current Program and Charge Current Monitor. The charge current is set by connecting a resistor, R_{PROG} , to ground. When charging in constant current mode, this pin servos to 1V. The voltage on this pin can be used to measure the charge current using the following formula:

$$
I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \cdot 1000
$$

V_{CC} (Pin 10): Positive Input Supply Pin. Provides power to the battery charger. This pin should be bypassed with a 1µF capacitor.

GND (Exposed Pad Pin 11): Ground. This pin is the back of the Exposed Pad package and must be soldered to the PCB copper for minimal thermal resistance.

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Block Diagram

OPERATION

The LTC4063 is designed to charge a single cell lithiumion battery and supply a regulated output voltage for battery-powered applications. Using the constant current/ constant voltage algorithm, the charger can deliver up to 1A of charge current with a final float voltage accuracy of ±0.35%. The LTC4063 includes an internal P-channel power MOSFET and thermal regulation circuitry. No blocking diode or external sense resistor is required; thus, the basic charger circuit requires only two external components.

The LDO regulator is powered from the battery terminal and can be programmed for output voltages between 1.2V and 4.2V using external resistors. An output capacitor is required on the OUT pin for stability and improved transient response. A low ESR capacitor of ≥2µF should be used.

Normal Operation

The charge cycle begins when the voltage at the V_{CC} pin rises above the UVLO level and a discharged battery is connected to BAT. If the BAT pin voltage is below 2.9V, the charger enters trickle charge mode. In this mode, the LTC4063 supplies 1/10th of the programmed charge current in order to bring the battery voltage up to a safe level for full current charging.

Once the BAT pin voltage rises above 2.9V, the charger enters constant-current mode where the programmed charge current is supplied to the battery. When the BAT pin approaches the final float voltage (4.2V), the LTC4063 enters constant-voltage mode and the charge current decreases as the battery becomes fully charged.

The LTC4063 offers several methods with which to terminate a charge cycle. Connecting an external capacitor to the TIMER pin activates an internal timer that stops the charge cycle after the programmed time period has elapsed. Grounding the TIMER pin and connecting a resistor to the IDET pin causes the charge cycle to terminate once the charge current falls below a set threshold when the charger is in constant-voltage mode. Connecting the TIMER pin to V_{CC} disables internal termination, allowing external charge termination to be used by the CHGEN input. See Applications Information for more on charge termination methods.

Programming the Charge Current

The charge current is programmed using a single resistor from the PROG pin to ground. The battery charge current is 1000 times the current out of the PROG pin. The program resistor and the charge current are calculated by the following equations:

$$
R_{PROG} = \frac{1000V}{I_{CHG}}, I_{CHG} = \frac{1000V}{R_{PROG}}
$$

The charge current out of the BAT pin can be determined at any time by monitoring the PROG pin voltage and applying the following equation:

$$
I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \cdot 1000
$$

SmartStart

When the LTC4063 is initially powered on or brought out of shutdown mode, the charger checks the voltage on BAT. If the BAT pin is below the recharge threshold of 4.1V (which corresponds to approximately 80% to 90% battery capacity), the LTC4063 enters charge mode and begins a full charge cycle. If the BAT pin is above 4.1V, the LTC4063 enters standby mode and does not begin charging. This feature reduces the number of unnecessary charge cycles, prolonging battery life.

Automatic Recharge

When the charger is in standby mode, the LTC4063 continuously monitors the voltage on the BAT pin. When the BAT pin voltage drops below 4.1V, the charge cycle is automatically restarted and the internal timer is reset to 50% the programmed charge time (if time termination is being used). This feature eliminates the need for periodic charge cycle initiations and ensures that the battery is always fully charged. Automatic recharge is disabled in User Termination mode.

Thermal Regulation

An internal thermal feedback loop reduces the programmed charge current if the die temperature attempts to rise above a preset value of approximately 105°C. This feature

OPERATION

protects the LTC4063 from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the LTC4063. The charge current can be set according to typical (not worst-case) ambient temperatures with the assurance that the charger will automatically reduce the current in worst-case conditions.

Undervoltage Lockout (UVLO)

An internal undervoltage lockout circuit monitors the input voltage and keeps the charger in shutdown mode until V_{CC} rises above the undervoltage lockout threshold (3.8V). The UVLO circuit has a built-in hysteresis of 200mV. Furthermore, to protect against reverse current in the power MOSFET, the UVLO circuit keeps the charger in shutdown mode if V_{CC} falls to less than 45mV above the battery voltage. Hysteresis of 135mV prevents the charger from cycling in and out of shutdown.

Manual Shutdown

At any point in the charge cycle, the charger can be put into shutdown mode by pulling the CHGEN pin high. This reduces the supply current to less than 65µA and the battery drain current of the charger to less than 2µA. A new charge cycle can be initiated by pulling the CHGEN pin low.

Pulling the LDOEN pin high puts the LDO into shutdown mode reducing the battery drain current of the LDO to less than 5µA. When both the CHGEN and LDOEN pins are pulled high, the total battery drain current from the LTC4063 is less than 2µA. If shutdown is not required, leaving these pins disconnected continuously enables the circuit.

Trickle Charge and Defective Battery Detection

When the BAT pin voltage is below the 2.9V trickle charge threshold (V_{TRIKI}), the charger reduces the charge current to 10% of the programmed value. If the battery remains in trickle charge for more than 25% of the total programmed charge time, the charger stops charging and enters a FAULT state, indicating that the battery is defective.¹ The LTC4063 indicates the FAULT state by driving the CHRG open-drain

output with a square wave. The duty cycle of this oscillation is 50% and the frequency is set by C_{TIMFR} :

$$
f_{\overline{CHRG}} = \frac{0.1 \mu F}{C_{\text{TIMER}}} \bullet 3.1 \text{Hz}
$$

An LED driven by the CHRG output exhibits a blinking pattern, indicating to the user that the battery needs replacing. To exit the FAULT state, the charger must be restarted either by toggling the CHGEN input or removing and reapplying power to V_{CC} .

Charge Status Output (CHRG)

The charge status indicator pin has two states: pull-down and high impedance. In the pull-down state, an NMOS transistor pulls down on the CHRG pin and can sink up to 10mA. A pull-down state indicates that the LTC4063 is charging a battery and the charge current is greater than I_{DFTECT} (which is set by the external resistor R_{DFT}). A high impedance state indicates that the charge current has dropped below I_{DETECT} . In the case where the IDET pin is left open ($R_{DFT} = \infty$, $I_{DFTFCT} = 0$), a high impedance state on CHRG indicates that the LTC4063 is not charging.

Low Dropout Linear Regulator (LDO)

The OUT pin provides a stable, regulated output voltage powered from the battery. This output can power devices such as memory or USB controllers from the battery when there is no power applied to V_{CC} .

The LDO can deliver 100mA of current with a nominal dropout voltage of 150mV. It is designed to be stable with a low ESR capacitor greater than 2µF on the OUT pin. Furthermore, the LDO is capable of operating from a Li-Ion battery voltage as low as 2.65V with less than 300mV of dropout over the specified operating conditions. An undervoltage lockout circuit automatically disables the LDO when the battery voltage drops below 2.55V, reducing the battery drain current to less than 5µA. The LDO can be disabled by pulling the LDOEN pin high, reducing the battery quiescent current to less than 5µA.

The defective battery detection feature is only available when time termination is being used.

OPERATION

Figure 1. Adjustable Linear Regulator

Figure 1 shows how an external resistor divider sets the regulator output voltage. The output voltage can be set anywhere between 1.2V and 4.2V, although the upper limit is limited by the battery voltage minus the regulator dropout voltage.

$$
V_{\text{OUT}} = 800 \text{mV} \cdot \left(1 + \frac{\text{R2}}{\text{R1}}\right)
$$

In order to maintain stability under light load conditions, the maximum recommended value of R1 is 160k.

Applications Information

Programming Charge Termination

The LTC4063 terminates a charge cycle using several methods, allowing the designer considerable flexibility in choosing an ideal charge termination algorithm. Table 1 shows a brief description of the different termination methods and their behavior.

Charge Time Termination

Table 1.

Connecting a capacitor (C_{TIMER}) to the TIMER pin enables the timer and selects Charge Time Termination. The total charge time is set by:

Time(Hours) =
$$
\frac{C_{TIMER}}{0.1 \mu F} \cdot 3 \text{ Hours}
$$

When the programmed time has elapsed, the charge cycle terminates and the charger enters standby mode. Subsequent recharge cycles terminate when half the programmed time has elapsed.

The IDET pin determines the behavior of the CHRG output. Connecting a resistor (R_{DET}) from the IDET pin to ground sets the charge current detection threshold, I_{DFTFCT} :

$$
I_{\text{DETECT}} = \frac{R_{\text{PROG}}}{10R_{\text{DET}}} \bullet I_{\text{CHG}} = \frac{100V}{R_{\text{DET}}}
$$

or

$$
R_{\text{DET}} = \frac{100V}{I_{\text{DETECT}}}
$$

When the charge current (I_{BAT}) is greater than I_{DETECT} , the CHRG output is in its pull-down state. When the charger enters constant-voltage mode operation and the charge current falls below I_{DETECT} , the CHRG output becomes high impedance, indicating that the battery is almost

Figure 2. Charge Time Termination. The Charger Automatically Shuts Off After 3 Hours

fully charged. The CHRG output will also become high impedance once the charge time elapses. If the IDET pin is not connected, the CHRG output remains in its pulldown state until the charge time elapses and terminates the charge cycle.

Figure 2 shows a charger circuit using charge time termination that is programmed to charge at 500mA. Once the charge current drops below 100mA in constant-voltage mode (as set by R_{DFT}), the $\overline{\text{CHRG}}$ output turns off the LED. This indicates to the user that the battery is almost fully charged and ready to use. The LTC4063 continues to charge the battery until the internal timer reaches 3 hours (as set by C_{TIMER}). During recharge cycles, the LTC4063 charges the battery until the internal timer reaches 1.5 hours. Figure 3 describes the operation of the LTC4063 charger when Charge Time Termination is used.

Figure 3. State Diagram of a Charge Cycle Using Charge Time Termination

Charge Current Termination

Connecting the TIMER pin to ground selects Charge Current Termination. With this method, the timer is disabled and a resistor (R_{DET}) must be connected from the IDET pin to ground. I_{DETECT} is programmed using the same equation stated in the previous section (repeated here for convenience):

$$
I_{\text{DETECT}} = \frac{R_{\text{PROG}}}{10R_{\text{DET}}} \bullet I_{\text{CHG}} = \frac{100V}{R_{\text{DET}}}
$$

or

$$
R_{\text{DET}} = \frac{100V}{I_{\text{DETECT}}}
$$

The charge cycle terminates when the charge current falls below I_{DFTECT} . This condition is detected using an internal, filtered comparator to monitor the IDET pin. When the IDET pin falls below 100mV for longer than t_{TFRM} (typically 1.5ms), charging is terminated.

When charging, transient loads on the BAT pin can cause the IDET pin to fall below 100mV for short periods of time before the DC current has dropped below the I_{DFTECT} threshold. The 1.5ms filter time (t_{TERM}) on the internal

comparator ensures that transient loads of this nature do not result in premature charge cycle termination. Once the *average* charge current drops below I_{DFTFCT}, the charger terminates the charge cycle.

The CHRG output is in its pull-down state when charging and in its high impedance state once charging has stopped. Figure 4 describes the operation of the LTC4063 charger when charge current termination is used.

User-Selectable Charge Termination

Connecting the TIMER pin to VCC selects User-Selectable Charge Termination, in which all internal termination features are disabled. The charge cycle continues indefinitely until the charger is shut down through the CHGEN pin. The IDET pin programs the behavior of the CHRG output in the same manner as when using Charge Time Termination. Specifically, when the charge current (I_{BAT}) is greater than I_{DFTFCL} the CHRG output is in its pull-down state. When the charger enters constant-voltage mode operation and the charge current falls below I_{DETECT} , the CHRG output becomes high impedance, indicating that the battery is charged. If the IDET pin is not connected, the CHRG output remains in its pull-down state until the charger is shut down.

Figure 4. State Diagram of a Charge Cycle Using Charge Current Termination

Figure 5. State Diagram of a Charger Cycle Using User Termination

With User-Selectable Charge Termination, the SmartStart feature is disabled; when the charger is powered on or enabled, the LTC4063 automatically begins charging, regardless of the battery voltage. Figure 5 describes charger operation when User-Selectable Charge Termination is used.

Programming C/10 Current Detection/Termination

In most cases, an external resistor, R_{DFT} , is needed to set the charge current detection threshold, IDETECT. However, when setting I_{DETECT} to be 1/10th of I_{CHG} , the IDET pin

Figure 6. Two Circuits that Charge at 500mA Full-Scale Current and Terminate at 50mA

can be connected directly to the PROG pin. This reduces the component count, as shown in Figure 6.

When PROG and IDET are connected in this way, the full-scale charge current, I_{CHG} , is programmed using a different equation:

$$
\mathsf{R}_{\mathsf{PROG}} = \frac{500 \text{V}}{\mathsf{I}_{\mathsf{CHG}}}, \mathsf{I}_{\mathsf{CHG}} = \frac{500 \text{V}}{\mathsf{R}_{\mathsf{PROG}}}
$$

Stability Considerations

The battery charger constant voltage mode feedback loop is stable without any compensation provided a battery is connected. However, a 1µF capacitor with a 1 Ω series resistor to GND is recommended at the BAT pin to keep ripple voltage low when the battery is disconnected.

When the charger is in constant current mode, the PROG pin is in the feedback loop, not the battery. The constant current stability is affected by the impedance at the PROG pin. With no additional capacitance on the PROG pin, the charger is stable with program resistor values as high as 10k; however, additional capacitance on this node reduces the maximum allowed program resistor.

For the LDO regulator, a capacitor (C_{OUT}) must be connected from OUT to GND to ensure regulator loop stability. It is recommended that low ESR capacitors be used for C_{OUT} to reduce noise on the output of the linear regulator. C_{OUT} must be ≥2µF for best performance.

Regulator Output Noise

Noise measurements on the output should be made with care to ensure accurate results. Coaxial connections and proper shielding should be used to maintain measurement integrity. Figure 7 shows a test setup for taking the measurement. When the output is set to 3V and a 100mA load is applied, the LTC4063 output noise power in the 10Hz to 100kHz band is typically measured to be $135 \mu V_{RMS}$. For more information on obtaining accurate noise measurements for LDOs, see Application Note 83.

Power Dissipation

When designing the battery charger circuit, it is not necessary to design for worst-case power dissipation scenarios because the LTC4063 automatically reduces the charge current during high power conditions. The conditions that cause the LTC4063 to reduce charge current through thermal feedback can be approximated by considering the power dissipated in the IC. Most of the power dissipation is generated from the internal charger MOSFET (the LDO generates considerably less heat in most applications). Thus, the power dissipation is calculated to be approximately:

$$
P_D = (V_{CC} - V_{BAT}) \cdot I_{BAT}
$$

 P_D is the power dissipated, V_{CC} is the input supply voltage, V_{BAT} is the battery voltage and I_{BAT} is the charge current. The approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$$
T_A = 105^{\circ}C - P_D \cdot \theta_{JA}
$$

\n
$$
T_A = 105^{\circ}C - (V_{CC} - V_{BAT}) \cdot I_{BAT} \cdot \theta_{JA}
$$

\n
$$
T_A = 105^{\circ}C - (V_{CC} - V_{BAT}) \cdot I_{BAT} \cdot \theta_{JA}
$$

\n
$$
T_A = 105^{\circ}C - (V_{CG} - V_{BAT}) \cdot I_{BAT} \cdot \theta_{JA}
$$

Figure 7. Filter Structure for Noise Testing LDOs

Example: An LTC4063 operating from a 5V wall adapter is programmed to supply 800mA full-scale current to a discharged Li-Ion battery with a voltage of 3.3V. Assuming θ_{JA} is 40°C/W (see Thermal Considerations), the ambient temperature at which the LTC4063 will begin to reduce the charge current is approximately:

$$
T_A = 105^{\circ}\text{C} - (5\text{V} - 3.3\text{V}) \cdot (800\text{mA}) \cdot 40^{\circ}\text{C/W}
$$

\n
$$
T_A = 105^{\circ}\text{C} - 1.36\text{W} \cdot 40^{\circ}\text{C/W} = 105^{\circ}\text{C} - 54.4^{\circ}\text{C}
$$

\n
$$
T_A = 50.6^{\circ}\text{C}
$$

The LTC4063 can be used above 50.6°C ambient, but the charge current will be reduced from 800mA. The approximate current at a given ambient temperature can be approximated by:

$$
I_{BAT} = \frac{105\degree C - T_A}{(V_{CC} - V_{BAT}) \bullet \theta_{JA}}
$$

Using the previous example with an ambient temperature of 60°C, the charge current will be reduced to approximately:

$$
I_{BAT} = \frac{105\degree C - 60\degree C}{(5V - 3.3V) \cdot 40\degree C/W} = \frac{45\degree C}{68\degree C/A}
$$

$$
I_{BAT} = 662mA
$$

It is important to remember that LTC4063 applications do not need to be designed for worst-case thermal conditions, since the IC will automatically reduce power iture reaches ap-

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Protection Features

While the thermally regulated charger limits the junction temperature to 105°C during normal operation, current overload at the LDO regulator output may result in excessive power dissipation. Internal circuitry limits the output currents, allowing the battery charger and regulator to be short-circuited to ground indefinitely. Furthermore, if the junction temperature exceeds 150°C, both the battery charger and regulator will shut down. The LTC4063 becomes enabled again once the junction temperature drops below 140°C. If the fault condition remains in place, the part will thermal cycle between the shutdown and enabled states.

The LTC4063 also protects against reverse conduction from the LDO output to the battery input. This provides protection if a discharged (low voltage) battery is powering the LDO, and the output voltage is held above the battery voltage by a backup battery or a second regulator circuit. When the output voltage is higher than the battery voltage, the reverse output current is typically less than 50µA.

Thermal Considerations

In order to deliver maximum charge current under all conditions, it is critical that the exposed metal pad on the backside of the LTC4063 package is properly soldered to the PC board ground. Correctly soldered to a 2500mm² double sided 1oz copper board, the LTC4063 has a thermal resistance of approximately 40°C/W. Failure to make thermal contact between the exposed pad on the backside of the package and the copper board will result in thermal resistances far greater than 40°C/W. As an example, a correctly soldered LTC4063 can deliver over 800mA to a battery from a 5V supply at room temperature. Without a good backside thermal connection this number would drop to much less than 500mA.

V_{CC} Bypass Capacitor

Many types of capacitors can be used for input bypassing, however, caution must be exercised when using multilayer ceramic capacitors. Because of the self-resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions such as connecting the charger input to a live power source. Adding a 1.5Ω resistor in series with an X5R ceramic capacitor will minimize start-up voltage transients. For more information, see Application Note 88.

Charge Current Soft-Start and Soft-Stop

The LTC4063 includes a soft-start circuit to minimize the inrush current at the start of a charge cycle. When a charge cycle is initiated, the charge current ramps from zero to the full-scale current over a period of approximately 100µs. Likewise, internal circuitry slowly ramps the charge current from full-scale to zero when the charger is shut down or self terminates. This has the effect of minimizing the transient current load on the power supply during start-up and charge termination.

Reverse Polarity Input Voltage Protection

In some applications, protection from reverse polarity voltage on V_{CC} is desired. If the supply voltage is high enough, a series blocking diode can be used. In other cases where the voltage drop must be kept low, a P-channel MOSFET can be used (as shown in Figure 8).

Figure 8. Low Loss Input Reverse Polarity Protection

USB and Wall Adapter Power

The LTC4063 allows charging from both a wall adapter and a USB port. Figure 9 shows how to combine wall adapter and USB power inputs. A P-channel MOSFET, MP1, is used to prevent back conducting into the USB port when a wall adapter is present and a Schottky diode, D1, is used to prevent USB power loss through the 1k pull-down resistor.

Most wall adapters can supply more current than the 500mA limited USB port. Therefore, an N-channel MOSFET, MN1, and an extra 3.3k program resistor are used to increase the charge current to 800mA when the wall adapter is present.

Typical Application

Figure 9. Combining Wall Adapter and USB Power

Package Description

DD Package 10-Lead Plastic DFN (3mm × **3mm)**

 MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE 5. EXPOSED PAD SHALL BE SOLDER PLATED 6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE

TOP AND BOTTOM OF PACKAGE

Revision History **(Revision history begins at Rev C)**

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