Fast No R_{SENSE}™ Step-Down Synchronous Controller with Margining, Tracking and PLL

FEATURES

- **Wide V_{IN} Range: 4V to 32V**
- **±0.67% 0.6V Reference Voltage**
- **Output Voltage Tracking Capability**
- **Programmable Margining**
- **Sense Resistor Optional**
- **True Current Mode Control**
- **2% to 90% Duty Cycle at 200kHz**
- **$t_{ON(MIN)}$ ≤ 100ns**
- **Phase-Locked Loop Frequency Synchronization**
- Powerful Dual N-Channel MOSFET Driver
- Adjustable Cycle-by-Cycle Current Limit
- Adjustable Switching Frequency
- Programmable Soft-Start
- Current Foldback Protection (Disabled at Start-Up)
- Output Overvoltage Protection
- Micropower Shutdown: I_Q < 30µA
- Power Good Output Voltage Monitor Tracks the Reference Input Pin
- Available in (5mm × 5mm) QFN and 28-Lead SSOP Packages

APPLICATIONS

- Distributed Power Systems
- Server Power Supply

DESCRIPTION

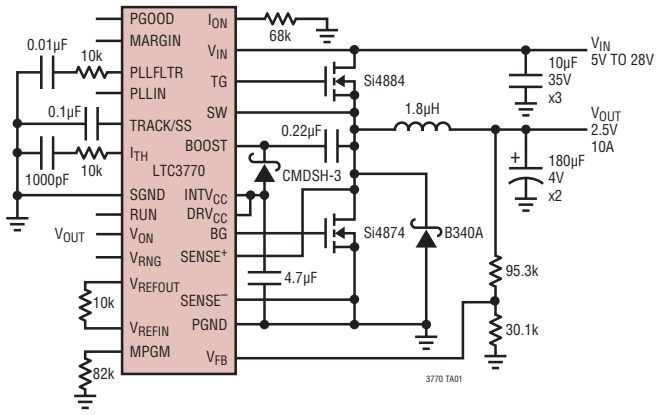
The LTC®3770 is a synchronous step-down switching regulator controller with output voltage up/down tracking capability and voltage margining. Its advanced functions and high accuracy reference are ideal for powering high performance server, ASIC and computer memory systems.

The LTC3770 uses a constant on-time, valley current mode control architecture to deliver very low duty factors without requiring a sense resistor. The operating frequency is selected by an external resistor and is compensated for variations in input supply voltage. An internal phase-locked loop allows the IC to be synchronized to an external clock.

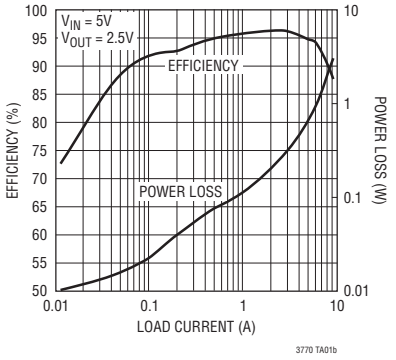
Fault protection is provided by an overvoltage comparator and input undervoltage lockout. The regulator current limit is user programmable. A wide supply range allows voltages as high as 32V to be stepped down to as low as a 0.6V output. Power supply sequencing is accomplished using an external soft-start timing capacitor.

TYPICAL APPLICATION

High Efficiency Step-Down Converter



Efficiency and Power Loss vs Load Current

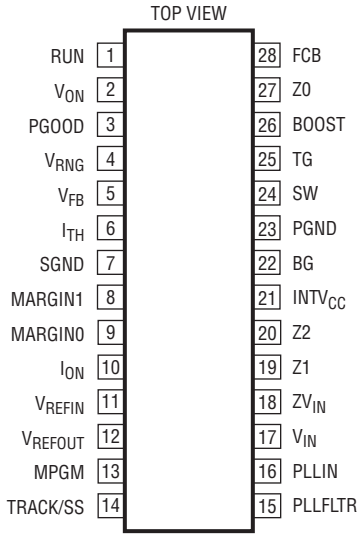


ABSOLUTE MAXIMUM RATINGS

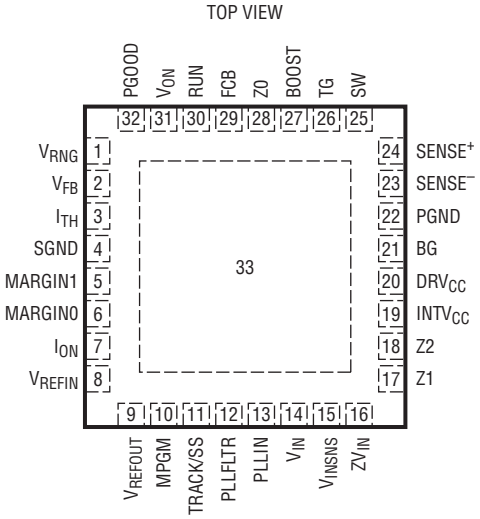
(Note 1)

Input Supply Voltage (V_{IN}, V_{INSNS}) ..... 32V to –0.3V
Boosted Topside Driver Supply Voltage
BOOST ..... 38V to –0.3V
SENSE+, SW Voltage ..... 32V to –5V
DRV_{CC}, (BOOST – SW) Voltages ..... 7V to –0.3V
V_{ON}, V_{RNG}, PGOOD Voltages ..... $INTV_{CC}$ + 0.3V to –0.3V
PLLFLTR, I_{TH}, V_{FB}, V_{REFIN} Voltages ..... 2.7V to –0.3V
TRACK/SS, FCB, Z0, Z1, Z2, RUN, PLLIN, MARGIN0, MARGIN1 Voltages ..... $INTV_{CC}$ + 0.3V to –0.3V
$INTV_{CC}$, ZV_{IN} Voltages ..... 7V to –0.3V
TG, BG, $INTV_{CC}$ Peak Currents 4A
TG, BG, $INTV_{CC}$ RMS Currents 50mA
Operating Ambient Temperature Range (Note 4) ..... –40°C to 85°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range ..... –65°C to 125°C
QFN Reflow Peak Body Temperature ..... 245°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



G PACKAGE
28-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 130°C/W



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD IS SGND (PIN 33)
MUST BE SOLDERED TO THE PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3770EG#PBF	LTC3770EG#TRPBF	LTC3770EG	28-Lead Plastic SSOP	–40°C to 85°C
LTC3770EUH#PBF	LTC3770EUH#TRPBF	3770	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 15V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
I_Q	Input DC Supply Current Normal Operation Shutdown Supply Current				 1300 30	 2200 50	 µA µA
V_{FB}	Feedback Voltage Accuracy (Note 3)	$V_{REFIN} = V_{REFOUT}$; I_{TH} = 1.2V (0°C to 85°C) $V_{REFIN} = V_{REFOUT}$; I_{TH} = 1.2V	 ●	0.596 0.594	0.6 0.6	0.604 0.606	V V
$V_{FB(LINEREG)}$	Feedback Voltage Line Regulation	V_{IN} = 4V to 30V, I_{TH} = 1.2V (Note 3)			0.002		%/V
$V_{FB(LOADREG)}$	Feedback Voltage Load Regulation	I_{TH} = 0.5V to 1.9V (Note 3)			–0.05	–0.3	%
V_{RUN}	Run Pin On Threshold	V_{RUN} Rising		1	1.5	1.9	V
$I_{SS/TRACK}$	Soft-Start Charging Current	$V_{SS/TRACK}$ = 0V		–1.1	–1.4	–1.7	µA
I_{FB}	Feedback Pin Input Current			–100	–20	100	nA
$g_{m(EA)}$	Error Amplifier Transconductance	I_{TH} = 1.2V (Note 3)	●	1	1.3	1.6	mS
V_{FCB}	Forced Continuous Threshold		●	0.57	0.6	0.63	V
I_{FCB}	Forced Continuous Pin Current	V_{FCB} = 0V			–1	–2	µA
t_{ON}	On-Time	I_{ON} = –60µA, V_{ON} = 1.5V I_{ON} = –60µA, V_{ON} = 0V		210 90	250 115	290 150	ns ns
$t_{ON(MIN)}$	Minimum On-Time	I_{ON} = –180µA, V_{ON} = 0V			50	100	ns
$t_{OFF(MIN)}$	Minimum Off-Time	Tested with a Square Wave (Note 5)			250	400	ns
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold V_{SENSE}^- – V_{SENSE}^+	V_{RNG} = 1V, $V_{FB} = V_{REFIN}$ – 30mV V_{RNG} = 0V, $V_{FB} = V_{REFIN}$ – 30mV $V_{RNG} = INTV_{CC}$, $V_{FB} = V_{REFIN}$ – 30mV	● ● ●	113 50 228	133 67 268	153 84 308	mV mV mV
$V_{SENSE(MIN)}$	Minimum Current Sense Threshold V_{SENSE}^- – V_{SENSE}^+	V_{RNG} = 1V, $V_{FB} = V_{REFIN}$ + 30mV V_{RNG} = 0V, $V_{FB} = V_{REFIN}$ + 30mV $V_{RNG} = INTV_{CC}$, $V_{FB} = V_{REFIN}$ + 30mV			–60 –30 –120		mV mV mV
$\Delta V_{FB(OV)}$	Output Overvoltage Fault Threshold Offset			7	10	13	%
$V_{IN(UVLO^+)}$	Undervoltage Lockout	V_{IN} Falling	●		3.2	3.9	V
$V_{IN(UVLO^-)}$	Undervoltage Lockout	V_{IN} Rising	●		3.3	4	V
$V_{MGN(TH)}$	MARGIN0, MARGIN1 Input Thresholds				1.4		V
V_{MPGM}	MPGM Pin Voltage				1.18		V
TG R_{UP}	TG Driver Pull-Up On Resistance	TG High			1.9	2.5	Ω
TG R_{DOWN}	TG Driver Pull-Down On Resistance	TG Low			1.2	2.5	Ω
BG R_{UP}	BG Driver Pull-Up On Resistance	BG High			1.9	3	Ω
BG R_{DOWN}	BG Driver Pull-Down On Resistance	BG Low			0.7	1.5	Ω
TG t_r	TG Rise Time	C_{LOAD} = 3300pF			20		ns
TG t_f	TG Fall Time	C_{LOAD} = 3300pF			20		ns
BG t_r	BG Rise Time	C_{LOAD} = 3300pF			20		ns
BG t_f	BG Fall Time	C_{LOAD} = 3300pF			20		ns

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 15V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Internal V_{CC} Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 30V	●	4.7	5	5.3	V
$\Delta V_{LDO(LOADREG)}$	Internal V_{CC} Load Regulation	I_{CC} = 0mA to 20mA			–0.1	±2	%
Phased-Locked Loop							
R_{PLLIN}	PLLIN Input Resistance				50		kΩ
$I_{PLLFLTR}$	Phase Detector Output Current Sink Capability Source Capability	 $f_{PLLIN} < f_0$ $f_{PLLIN} > f_0$			 –15 15		 µA µA
PGOOD Output							
ΔV_{FBH}	PGOOD Upper Threshold	V_{FB} Rising		7	10	13	%
ΔV_{FBL}	PGOOD Lower Threshold	V_{FB} Falling		–7	–10	–13	%
$\Delta V_{FB(HYS)}$	PGOOD Hysteresis	V_{FB} Returning			1.5	3	%
V_{PGL}	PGOOD Low Voltage	I_{PGOOD} = 5mA			0.15	0.4	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D as follows:

LTC3770EG: $T_J = T_A + (P_D \bullet 130°C/W)$

LTC3770EUH: $T_J = T_A + (P_D \bullet 34°C/W)$

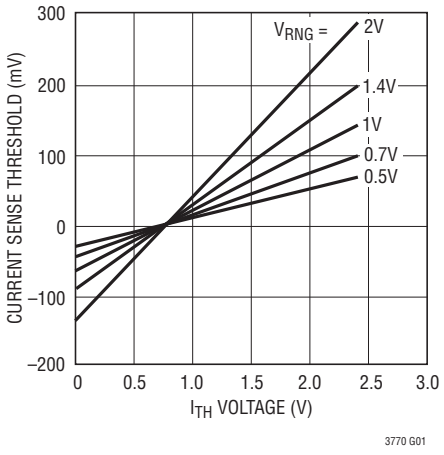
Note 3: The 3770 is tested in a feedback loop that adjusts V_{FB} to achieve a specified error amplifier output voltage (I_{TH}). For these tests, $V_{REFOUT} = V_{REFIN}$.

Note 4: The LTC3770E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

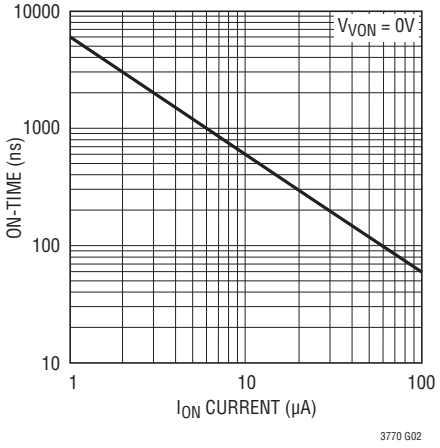
Note 5: The minimum off-time condition is specified for large peak-to-peak inductor ripple current (see Minimum Off-Time Considerations in the Applications Information section).

TYPICAL PERFORMANCE CHARACTERISTICS

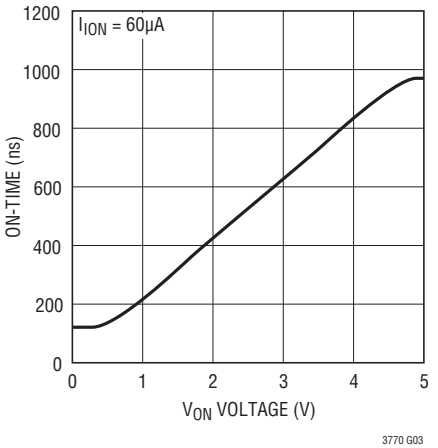
Current Sense Threshold vs I_{TH} Voltage



On-Time vs I_{ON} Current

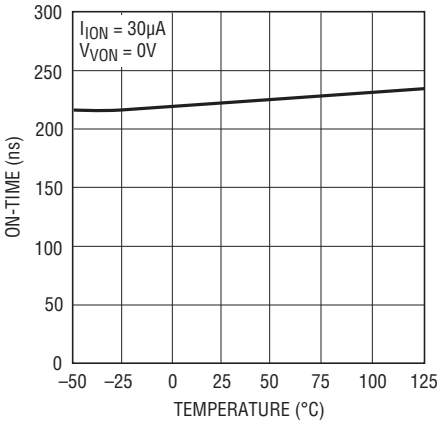


On-Time vs V_{ON} Voltage



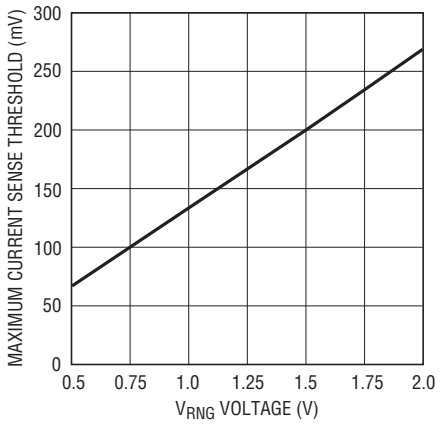
TYPICAL PERFORMANCE CHARACTERISTICS

On-Time vs Temperature



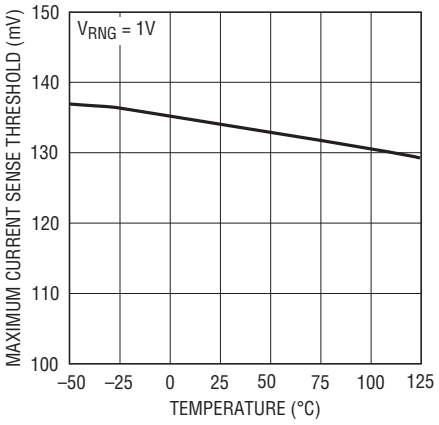
3770 G04

Maximum Current Sense Threshold vs V_{RNG} Voltage



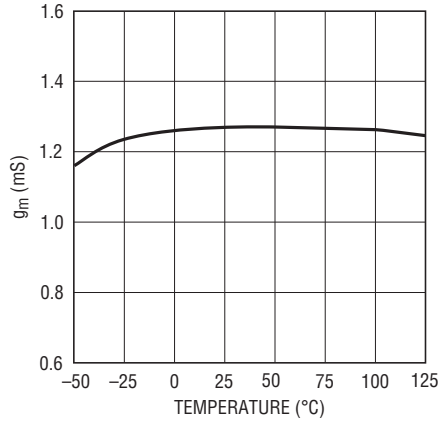
3770 G05

Maximum Current Sense Threshold vs Temperature



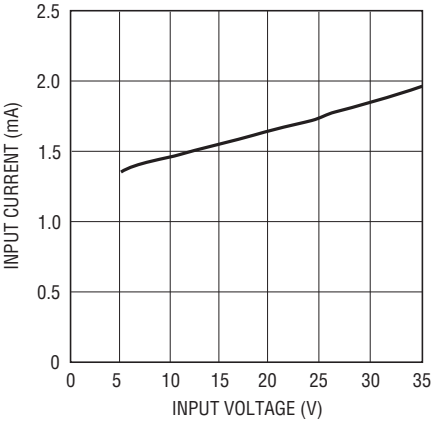
3770 G06

Error Amplifier g_m vs Temperature



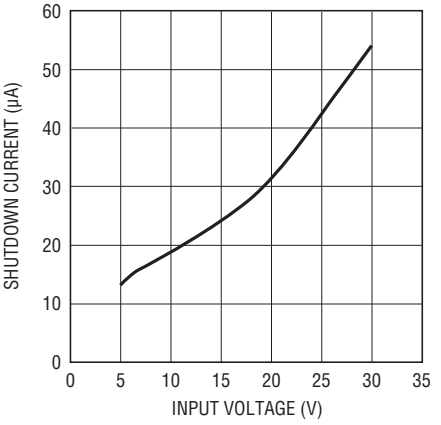
3770 G07

Input Current vs Input Voltage



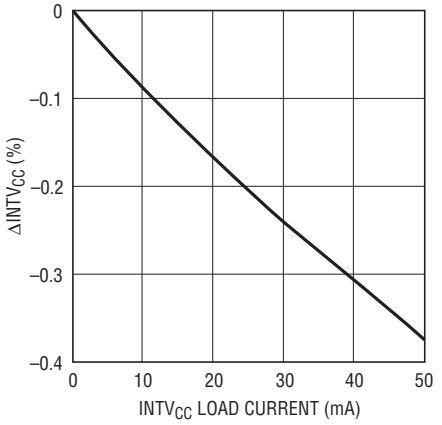
3770 G08

Shutdown Current vs Input Voltage



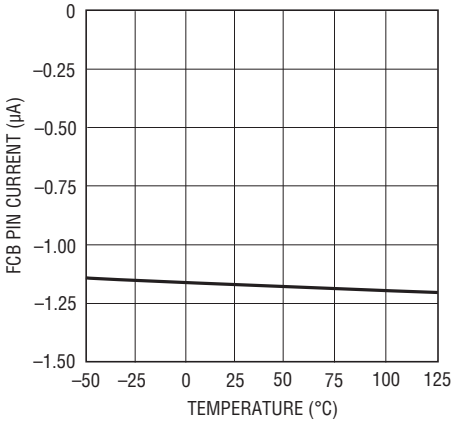
3770 G09

$INTV_{CC}$ Load Regulation



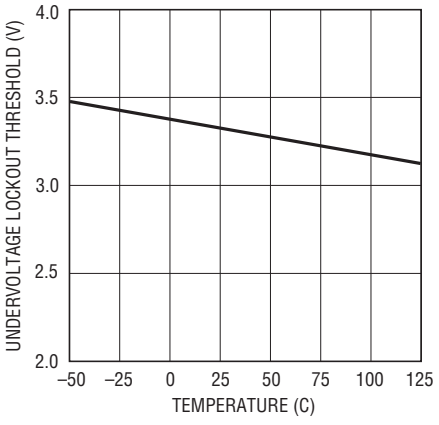
3770 G10

FCB Pin Current vs Temperature



3770 G11

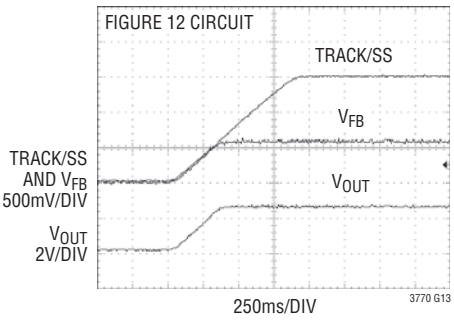
Undervoltage Lockout Threshold vs Temperature



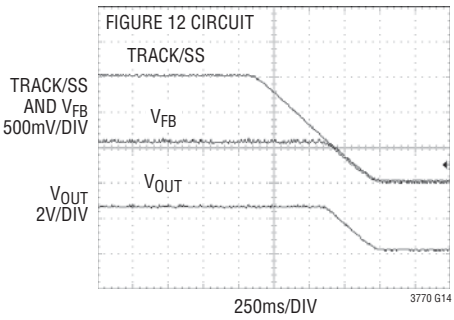
3770 G12

TYPICAL PERFORMANCE CHARACTERISTICS

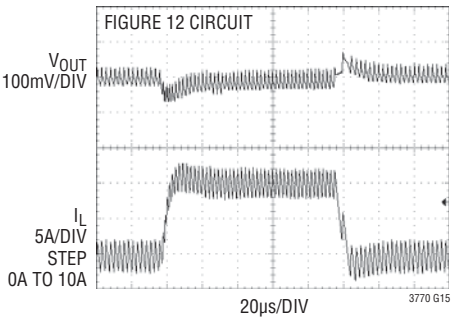
Track Up



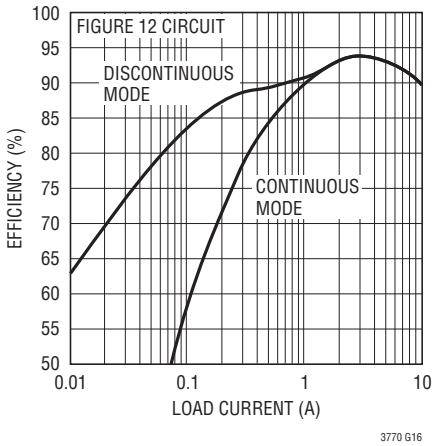
Track Down



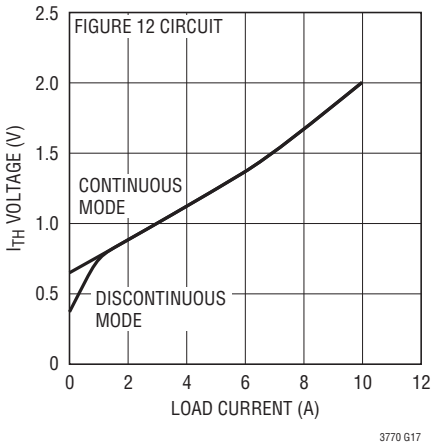
Transient Response



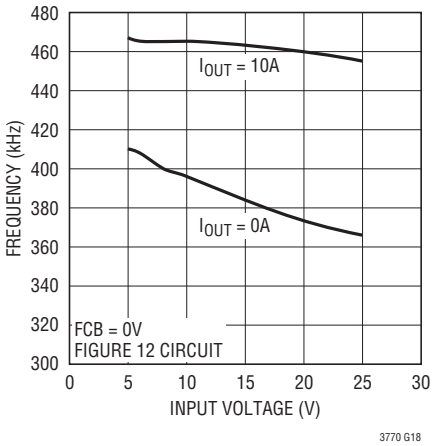
Efficiency vs Load Current



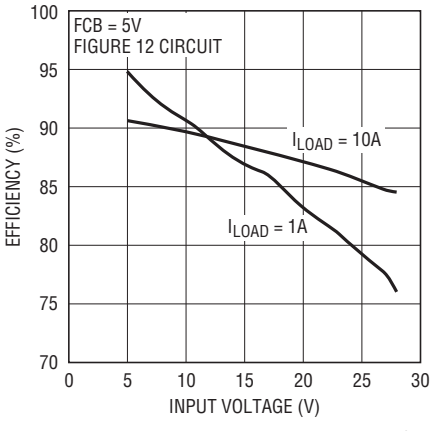
ITH Voltage vs Load Current



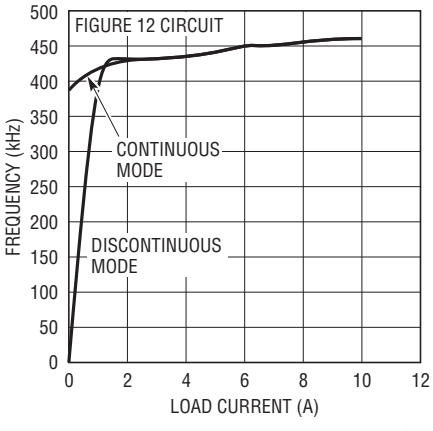
Frequency vs Input Voltage



Efficiency vs Input Voltage

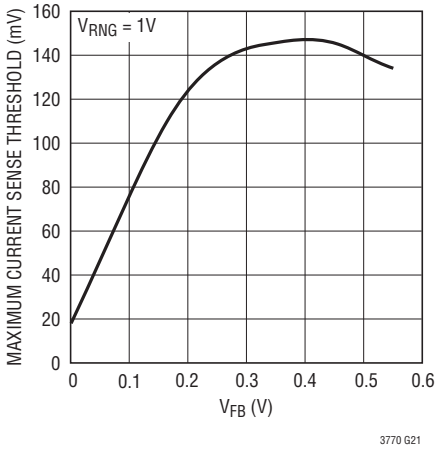


Frequency vs Load Current

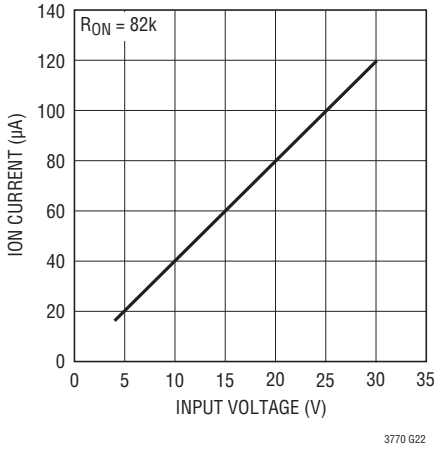


TYPICAL PERFORMANCE CHARACTERISTICS

Current Limit Foldback



Ion Current vs V_{IN}



PIN FUNCTIONS (UH Package/G Package)

V_{RNG} (Pin 1/Pin 4): Sense Voltage Range Input. The voltage at this pin is ten times the nominal sense voltage at maximum output current and can be set from 0.5V to 2V by a resistive divider from $INTV_{CC}$. The nominal sense voltage defaults to 50mV when this pin is tied to ground, 200mV when tied to $INTV_{CC}$. Do not set this voltage between 0.5V to ground or 2V to $INTV_{CC}$.

V_{FB} (Pin 2/Pin 5): Error Amplifier Feedback Input. This pin connects the error amplifier input to an external resistive divider from V_{OUT}.

I_{TH} (Pin 3/Pin 6): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V with 0.75V corresponding to zero sense voltage (zero current).

SGND (Pin 4/Pin 7): Signal Ground. All small-signal components and compensation components should connect to this ground, which in turn connects to PGND at one point.

MARGIN1 (Pin 5/Pin 8): The MSB Logic Input for the Margining Function. Together with the MARGIN0 pin determines whether the IC is in margin high, margin low, or no margin state. This pin has a 50k internal pull-down resistor.

MARGIN0 (Pin 6/Pin 9): The LSB Logic Input for the Margining Function. Together with the MARGIN1 pin determines whether the IC is in margin high, margin low, or no margin state. This pin has a 50k internal pull-down resistor.

I_{ON} (Pin 7/Pin 10): On-Time Current Input. Tie a resistor from this pin to ground to set the one-shot timer current and thereby set the switching frequency.

V_{REFIN} (Pin 8/Pin 11): Error Amplifier Reference Input. The voltage at this pin must be greater than 0.5V and less than 1V.

V_{REFOUT} (Pin 9/Pin 12): Buffered Internal 0.6V Reference Output. The maximum current sinking limit is 50µA at this pin. Do not put a filter capacitor larger than 100pF on this pin.

MPGM (Pin 10/Pin 13): Programmable Margining Input. A resistor from this pin to ground sets the margining current. This current, together with the resistor between the V_{REFOUT} and V_{REFIN} pins, determines the margining voltage offset.

TRACK/SS (Pin 11/Pin 14): Output Voltage Tracking and Soft-Start Input. When the IC is configured to be the master of two outputs, a capacitor to ground at this pin

PIN FUNCTIONS (UH Package/G Package)

sets the ramp rate for the output voltage. When the IC is configured to be the slave of two outputs, the V_{FB} voltage of the master IC is reproduced by a resistor divider and applied to this pin. An internal 1.4µA soft-start current is charging this pin during the soft-start phase.

PLLFLTR (Pin 12/Pin 15): The Phase-Locked Loop's Lowpass Filter is Tied to This Pin. The voltage at this pin defaults to 1.18V when the IC is not synchronized with an external clock at the PLLIN pin.

PLLIN (Pin 13/Pin 16): External Synchronization Input to Phase Detector. This pin is internally terminated to SGND with a 50k resistor.

V_{IN} (Pin 14/Pin 17): Main Input Supply. Decouple this pin to PGND with a capacitor (0.1µF to 1µF).

V_{INSNS} (Pin 15) UH Package: V_{IN} Voltage Sense Input. Normally this pin is tied to V_{IN}. However, in certain applications when the IC is powered from a separate supply, V_{INSNS} is tied to the upper MOSFET supply to sense the V_{IN} voltage. The pin is co-bonded with V_{IN} in the SSOP package.

ZV_{IN} (Pin 16/Pin 18): Post-Package Zener-Trim Voltage Input. Under normal conditions this pin should always be connected to $INTV_{CC}$.

Z1 (Pin 17/Pin 19): Post-Package Zener-Trim Control. This pin is a multifunctional pin used in production for post-package trimming and tracking. Ground this pin under normal soft-start operation. Connecting this pin to $INTV_{CC}$ will turn off the soft-start current during tracking.

Z2 (Pin 18/Pin 20): Post-Package Zener-Trim Control. This pin is used in production for Post-Package trimming. Ground this pin or tie to $INTV_{CC}$ under normal operation.

$INTV_{CC}$ (Pin 19/Pin 21): Internal 5V Regulator Output. The control circuits are powered from this voltage. Decouple this pin to PGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor.

DRV_{CC} (Pin 20) UH Package Gate: Driver Voltage Input. Must be connected to $INTV_{CC}$ externally. Do not exceed 7V at this pin. This pin is co-bonded to $INTV_{CC}$ internally in the SSOP package.

BG (Pin 21/Pin 22): Bottom Gate Driver Output. This pin drives the gate of the bottom N-channel MOSFET between ground and $INTV_{CC}$.

PGND (Pin 22/Pin 23): Power Ground. Connect this pin closely to the source of the bottom N-channel MOSFET, the (–) terminal of CV_{CC} and the (–) terminal of C_{IN}.

$SENSE^-$ (Pin 23) UH Package: Current Sense Comparator Input. The (–) input to the current comparator is used to accurately Kelvin sense the bottom side of the sense resistor or MOSFET. This pin is co-bonded with PGND internally in the SSOP package.

$SENSE^+$ (Pin 24) UH Package: Current Sense Comparator Input. The (+) input to the current comparator is normally connected to the SW node unless using a sense resistor. This pin is co-bonded with SW internally in the SSOP package.

SW (Pin 25/Pin 24): Switch Node. The (–) terminal of the boot-strap capacitor CB connects here. This pin swings from a diode voltage drop below ground up to V_{IN}.

TG (Pin 26/Pin 25): Top Gate Drive Output. This pin drives the top N-channel MOSFET with a voltage swing equal to $INTV_{CC}$, superimposed on the switch node voltage SW.

BOOST (Pin 27/Pin 26): Boosted Floating Driver Supply. The (+) terminal of the boot-strap capacitor CB connects here. This pin swings from a diode voltage drop below $INTV_{CC}$ up to V_{IN} + $INTV_{CC}$.

Z0 (Pin 28/Pin 27): Dead Time Control Input. Applying a DC voltage will vary the dead time between TG-Low and BG-High transition. Do not force a voltage higher than 5V on this pin.

FCB (Pin 29/Pin 28): Forced Continuous Input. Connect this pin to SGND to forced continuous synchronization operation at low load, to $INTV_{CC}$ to enable discontinuous mode operation at low load or to a resistive divider from a secondary output when using a secondary winding.

RUN (Pin 30/Pin 1): Run Control Input. A voltage above 1.5V turns on the IC. Forcing this pin below 1.5V shuts down the device.

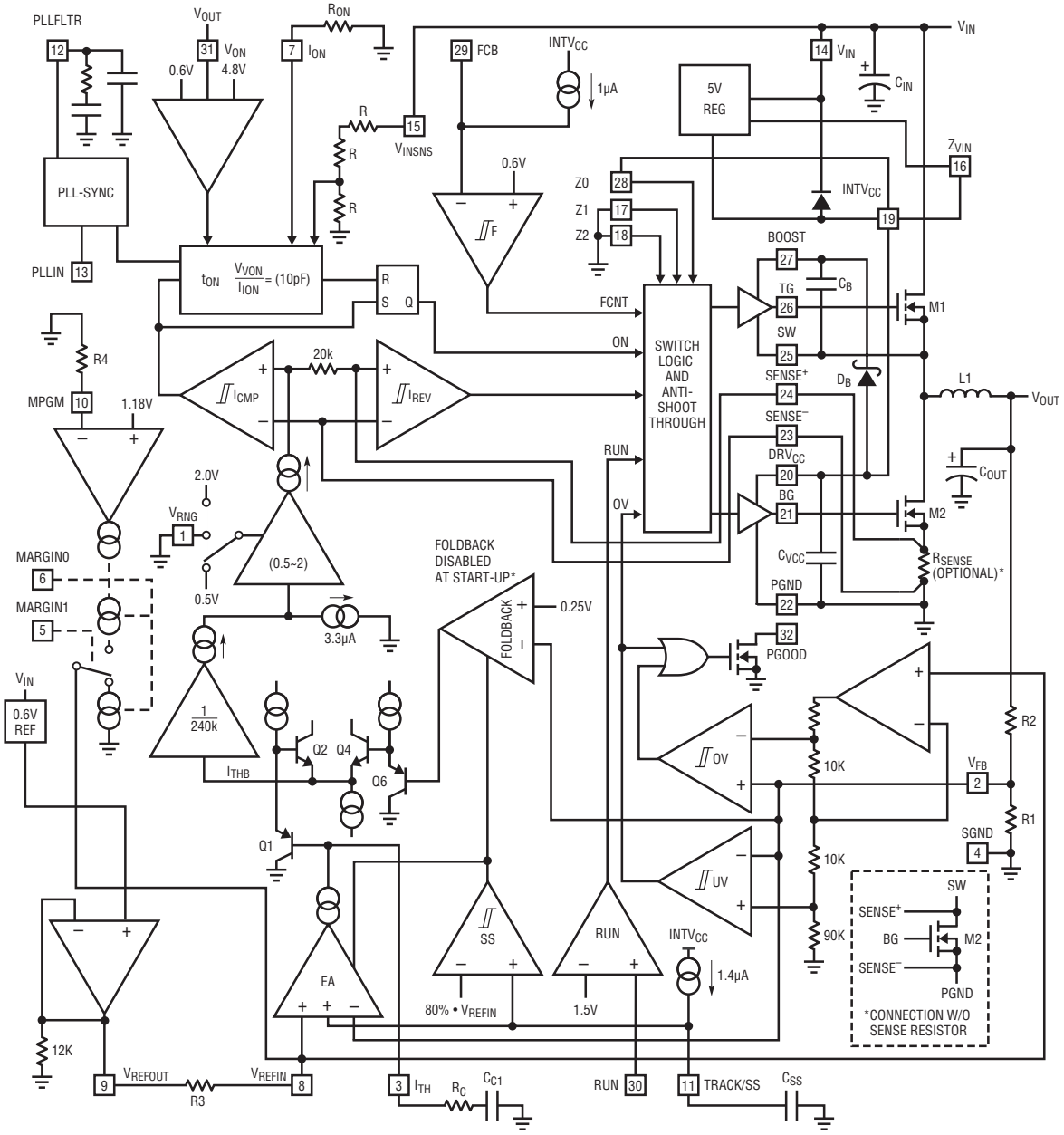
PIN FUNCTIONS (UH Package/G Package)

V_{ON} (Pin 31/Pin 2): On-Time Voltage Input. Connecting this pin to the output voltage makes the on-time proportional to V_{OUT}. The comparator input defaults to 0.6V when the pin is grounded and defaults to 4.8V when the pin is tied to $INTV_{CC}$.

PGOOD (Pin 32/Pin 3): Power Good Output. Open drain logic output that is pulled to ground when the output voltage is not within ±10% of the regulation point, after the internal 25µs power bad mask timer expires.

Exposed Pad (Pin 33) UH Package: Signal Ground. Must be soldered to the PCB ground for electrical contact and optimum thermal performance.

FUNCTIONAL DIAGRAM (UH Package)



OPERATION

Main Control Loop

The LTC3770 is a current mode controller for DC/DC step-down converters. In normal operation, the top MOSFET is turned on for a fixed interval determined by a one-shot timer OST. When the top MOSFET is turned off, the bottom MOSFET is turned on until the current comparator ICMP trips, restarting the one-shot timer and initiating the next cycle. Inductor current is determined by sensing the voltage between the $SENSE^-$ (PGND on G package) and $SENSE^+$ (SW on G package) pins using a sense resistor or the bottom MOSFET on-resistance . The voltage on the I_{TH} pin sets the comparator threshold corresponding to inductor valley current. The error amplifier EA adjusts this voltage by comparing the feedback signal V_{FB} from a reference voltage set by the V_{REFIN} pin. If the load current increases, it causes a drop in the feedback voltage relative to the reference. The I_{TH} voltage then rises until the average inductor current again matches the load current.

At low load currents, the inductor current can drop to zero and become negative. This is detected by current reversal comparator I_{REV} which then shuts off M2, resulting in discontinuous operation. Both switches will remain off with the output capacitor supplying the load current until the I_{TH} voltage rises above the zero current level (0.75V) to initiate another cycle. Discontinuous mode operation is disabled by comparator F when the FCB pin is brought below 0.6V, forcing continuous synchronous operation.

The operating frequency is determined implicitly by the top MOSFET on-time and the duty cycle required to maintain regulation. The one-shot timer generates an on-time that is proportional to the ideal duty cycle, thus holding frequency approximately constant with changes in V_{IN}. The nominal frequency can be adjusted with an external resistor R_{ON}.

For applications with stringent constant frequency requirements, the LTC3770 can be synchronized with an external clock. By programming the nominal frequency of the LTC3770 the same as the external clock frequency, the LTC3770 behaves as a constant frequency part against the load and supply variations.

Overvoltage and undervoltage comparators OV and UV pull the PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point after the internal 25µs power bad mask timer expires. Furthermore, in an overvoltage condition, M1 is turned off and M2 is turned on immediately and held on until the overvoltage condition clears.

Foldback current limiting is provided if the output is shorted to ground. As V_{FB} drops, the buffered current threshold voltage I_{THB} is pulled down and clamped to 0.9V. This reduces the inductor valley current level to one tenth of its maximum value as V_{FB} approaches 0V. Foldback current limiting is disabled at start-up.

Pulling the RUN pin low forces the controller into its shutdown state, turning off both M1 and M2. Forcing a voltage above 1.5V will turn on the device.

$INTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most of the internal controller circuitry is derived from the $INTV_{CC}$ pin. The top MOSFET driver is powered from a floating bootstrap capacitor, C_B. This capacitor is recharged from $INTV_{CC}$ through an external Schottky diode DB when the top MOSFET is turned off. If the input voltage is low and $INTV_{CC}$ drops below 3.2V, undervoltage lockout circuitry prevents the power switches from turning on.

APPLICATIONS INFORMATION

The basic LTC3770 application circuit is shown in Figure 12. External component selection is primarily determined by the maximum load current and begins with the selection of the sense resistance and power MOSFET switches. The LTC3770 uses either a sense resistor or the on-resistance of the synchronous power MOSFET for determining the inductor current. The desired amount of ripple current and operating frequency largely determines the inductor value. Finally, C_{IN} is selected for its ability to handle the large RMS current into the converter and C_{OUT} is chosen with low enough ESR to meet the output voltage ripple and transient specification.

Maximum Sense Voltage and V_{RNG} Pin

Inductor current is determined by measuring the voltage across a sense resistance that appears between the SENSE$^-$ (PGND on G package) and SENSE$^+$ (SW on G package) pins. The maximum sense voltage is set by the voltage applied to the V_{RNG} pin and is equal to approximately $(0.133)V_{RNG}$. The current mode control loop will not allow the inductor current valleys to exceed $(0.133)V_{RNG}/R_{SENSE}$. In practice, one should allow some margin for variations in the LTC3770 and external component values and a good guide for selecting the sense resistance is:

$$R_{SENSE} = \frac{V_{RNG}}{10 \bullet I_{OUT(MAX)}}$$

An external resistive divider from $INTV_{CC}$ can be used to set the voltage of the V_{RNG} pin between 0.5V and 2V resulting in nominal sense voltages of 50mV to 200mV. Additionally, the V_{RNG} pin can be tied to SGND or $INTV_{CC}$ in which case the nominal sense voltage defaults to 50mV or 200mV, respectively. The maximum allowed sense voltage is about 1.33 times this nominal value. However tying the V_{RNG} pin to ground is not recommended because the current comparator offset is now a bigger proportion of the total sense voltage.

Connecting the SENSE$^+$ and SENSE$^-$ Pins

The LTC3770 comes in UH and G packages. The UH package IC can be used with or without a sense resistor. When using a sense resistor, place it between the source of the bottom MOSFET, M2, and PGND. Connect the SENSE$^+$ and SENSE$^-$ pins to the top and bottom of the sense resistor. Using a sense resistor provides a well defined current limit, but adds cost and reduces efficiency. Alternatively, one can eliminate the sense resistor and use the bottom MOSFET as the current sense element by simply connecting the SENSE$^+$ pin to the SW pin and SENSE$^-$ pin to PGND. This improves efficiency, but one must carefully choose the MOSFET on-resistance as discussed below.

Power MOSFET Selection

The LTC3770 requires two external N-channel power MOSFETs, one for the top (main) switch and one for the bottom (synchronous) switch. Important parameters for the power MOSFETs are the breakdown voltage $V_{(BR)DSS}$, threshold voltage $V_{(GS)TH}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and maximum current $I_{DS(MAX)}$.

The gate drive voltage is set by the 5V $INTV_{CC}$ supply. Consequently, logic-level threshold MOSFETs must be used in LTC3770 applications. If the input voltage is expected to drop below 5V, then sub-logic level threshold MOSFETs should be considered.

When the bottom MOSFET is used as the current sense element, particular attention must be paid to its on-resistance. MOSFET on-resistance is typically specified with a maximum value $R_{DS(ON)(MAX)}$ at 25°C. In this case, additional margin is required to accommodate the rise in MOSFET on-resistance with temperature:

$$R_{DS(ON)(MAX)} = \frac{R_{SENSE}}{\rho T}$$

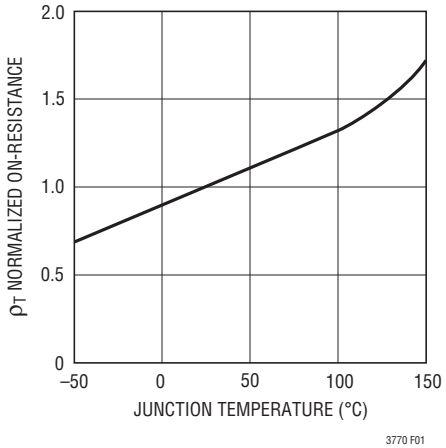


Figure 1. $R_{DS(ON)}$ vs Temperature

APPLICATIONS INFORMATION

The ρ_T term is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically about 0.4%/°C as shown in Figure 1. For a maximum junction temperature of 100°C, using a value ρ_T = 1.3 is reasonable.

The power dissipated by the top and bottom MOSFETs strongly depends upon their respective duty cycles and the load current. When the LTC3770 is operating in continuous mode, the duty cycles for the MOSFETs are:

$$D_{TOP} = \frac{V_{OUT}}{V_{IN}}$$

$$D_{BOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The resulting power dissipation in the MOSFETs at maximum output current are:

$$P_{TOP} = D_{TOP}\, I_{OUT(MAX)}^2\, \rho_{T(TOP)}\, R_{DS(ON)(MAX)} + k\, V_{IN}^2\, I_{OUT(MAX)}\, C_{RSS}\, f$$

$$P_{BOT} = D_{BOT}\, I_{OUT(MAX)}^2\, \rho_{T(BOT)}\, R_{DS(ON)(MAX)}$$

Both MOSFETs have I^2R losses and the top MOSFET includes an additional term for transition losses, which are largest at high input voltages. The constant $k = 1.7A^{-1}$ can be used to estimate the amount of transition loss. The bottom MOSFET losses are greatest when the bottom duty cycle is near 100%, during a short-circuit or at high input voltage.

Operating Frequency

The choice of operating frequency is a tradeoff between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses but requires larger inductance and/or capacitance in order to maintain low output ripple voltage.

The operating frequency of LTC3770 applications is determined implicitly by the one-shot timer that controls the on-time t_{ON} of the top MOSFET switch. The on-time is set by the current out of the I_{ON} pin and the voltage at the V_{ON} pin according to:

$$t_{ON} = \frac{V_{VON}}{I_{ION}}(10pF)$$

Tying a resistor R_{ON} to SGND from the I_{ON} pin yields an on-time inversely proportional to 1/3 V_{IN}. The current out of the I_{ON} pin is:

$$I_{ION} = \frac{V_{IN}}{3\,R_{ON}}$$

For a step-down converter, this results in approximately constant frequency operation as the input supply varies:

$$f = \frac{V_{OUT}}{V_{VON} \bullet 3\,R_{ON}(10pF)}\,[H_Z]$$

To hold frequency constant during output voltage changes, tie the V_{ON} pin to V_{OUT}. The V_{ON} pin has internal clamps that limit its input to the one-shot timer. If the pin is tied below 0.6V, the input to the one-shot is clamped at 0.6V. Similarly, if the pin is tied above 4.8V, the input is clamped at 4.8V. In high V_{OUT} applications, tie V_{ON} to $INTV_{CC}$. Figures 2a and 2b show how R_{ON} relates to switching frequency for several common output voltages.

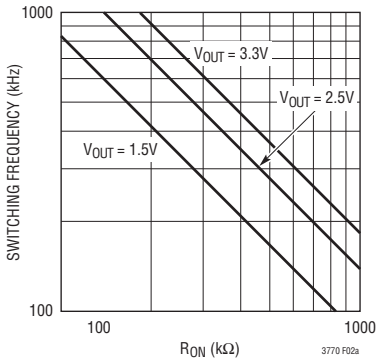


Figure 2a. Switching Frequency vs R_{ON} (V_{ON} = 0V)

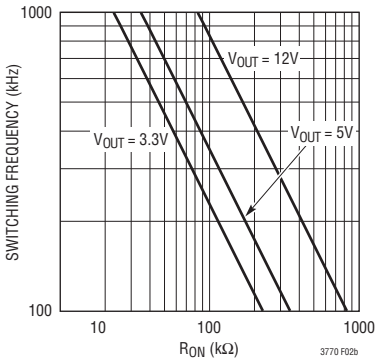


Figure 2b. Switching Frequency vs R_{ON} (V_{ON} = $INTV_{CC}$)

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When there is no R_{ON} resistor connected to the I_{ON} pin, the on-time t_{ON} is theoretically infinite, which in turn could damage the converter. To prevent this, the LTC3770 will detect this fault condition and provide a minimum I_{ON} current of 5µA to 10µA.

Changes in the load current magnitude will cause frequency shift. Parasitic resistance in the MOSFET switches and inductor reduce the effective voltage across the inductance, resulting in increased duty cycle as the load current increases. By lengthening the on-time slightly as current increases, constant frequency operation can be maintained. This is accomplished with a resistive divider from the I_{TH} pin to the V_{ON} pin and V_{OUT}. The values required will depend on the parasitic resistances in the specific application. A good starting point is to feed about 25% of the voltage change at the I_{TH} pin to the V_{ON} pin as shown in Figure 3a. Place capacitance on the V_{ON} pin to filter out the I_{TH} variations at the switching frequency. The resistor load on I_{TH} reduces the DC gain of the error amp and degrades load regulation, which can be avoided by using the PNP emitter follower of Figure 3b.

Minimum Off-Time and Dropout Operation

The minimum off-time $t_{OFF(MIN)}$ is the smallest amount of time that the LTC3770 is capable of turning on the bottom MOSFET, tripping the current comparator and turning the MOSFET back off. This time is generally about 250ns for large peak-to-peak inductor ripple current. In applications where the peak-to-peak inductor ripple current is small, the minimum off-time can approach 400ns. The minimum off-time limit imposes a maximum duty cycle of $t_{ON}/(t_{ON} + t_{OFF(MIN)})$. If the maximum duty cycle is reached, due to a dropping input voltage for example, then the output will drop out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = V_{OUT} \frac{t_{ON} + t_{OFF(MIN)}}{t_{ON}}$$

A plot of Maximum Duty Cycle vs Frequency is shown in Figure 4.

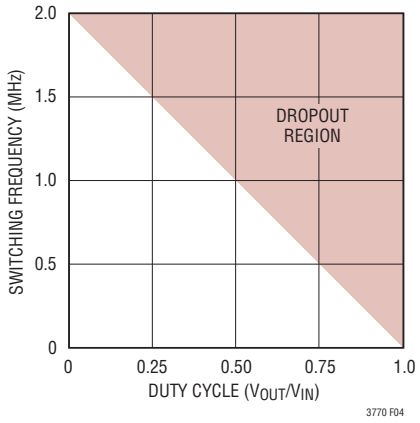

Figure 4. Maximum Switching Frequency vs Duty Cycle

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \left(\frac{V_{OUT}}{f\ L}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a tradeoff between component size, efficiency and operating frequency.

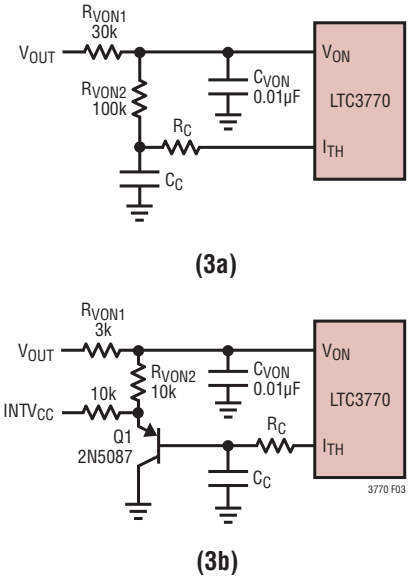

Figure 3. Correcting Frequency Shift with Load Current Changes

APPLICATIONS INFORMATION

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. The largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f\,\Delta I_{L(MAX)}}\right)\left(1-\frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Panasonic, Coiltronics, Coilcraft and Toko.

Schottky Diode D1 Selection

The Schottky diode D1 shown in Figure 12 conducts during the dead time between the conduction of the power MOSFET switches. It is intended to prevent the body diode of the bottom MOSFET from turning on and storing charge during the dead time, which can cause a modest (about 1%) efficiency loss. The diode can be rated for about one half to one fifth of the full load current since it is on for only a fraction of the duty cycle. In order for the diode to be effective, the inductance between it and the bottom MOSFET must be as small as possible, mandating that these components be placed adjacently. The diode can be omitted if the efficiency loss is tolerable.

C_{IN} and C_{OUT} Selection

The input capacitance C_{IN} is required to filter the square wave current at the drain of the top MOSFET. Use a low ESR capacitor sized to handle the maximum RMS current.

$$I_{RMS} \cong I_{OUT(MAX)}\frac{V_{OUT}}{V_{IN}}\sqrt{\frac{V_{IN}}{V_{OUT}}-1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to derate the capacitor.

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The output ripple ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} \le \Delta I_L\left(ESR+\frac{1}{8fC_{OUT}}\right)$$

Since ΔI_L increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications providing that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. When used as input capacitors, care must be taken to ensure that ringing from inrush currents and switching does not pose an overvoltage hazard to the power switches and controller. To dampen input voltage transients, add a small 5μF to 50μF aluminum electrolytic capacitor with an ESR in the range of 0.5Ω to 2Ω. High performance through-hole capacitors may also be used, but an additional ceramic capacitor in parallel is recommended to reduce the effect of their lead inductance.

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Top MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor C_B connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. This capacitor is charged through diode D_B from $INTV_{CC}$ when the switch node is low. When the top MOSFET turns on, the switch node rises to V_{IN} and the BOOST pin rises to approximately $V_{IN} + INTV_{CC}$. The boost capacitor needs to store about 100 times the gate charge required by the top MOSFET. In most applications 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate.

Discontinuous Mode Operation and FCB Pin

The FCB pin determines whether the bottom MOSFET remains on when current reverses in the inductor. Tying this pin above its 0.6V threshold enables discontinuous operation where the bottom MOSFET turns off when inductor current reverses. The load current at which current reverses and discontinuous operation begins depends on the amplitude of the inductor ripple current and will vary with changes in V_{IN}. Tying the FCB pin below the 0.6V threshold forces continuous synchronous operation, allowing current to reverse at light loads and maintaining high frequency operation. To prevent forcing current back into the main power supply, potentially boosting the input supply to a dangerous voltage level, forced continuous mode of operation is disabled when the TRACK/SS voltage is 20% below the reference voltage during soft-start or tracking up. Forced continuous mode of operation is also disabled when the TRACK/SS voltage is below 0.1V during tracking down operation. During these two periods, the PGOOD signal is forced low.

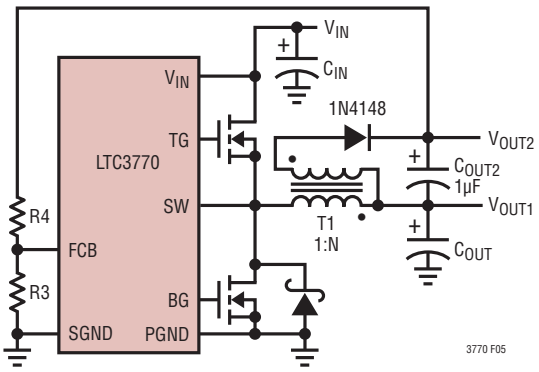

Figure 5. Secondary Output Loop

In addition to providing a logic input to forced continuous operation, the FCB pin provides a mean to maintain a flyback winding output when the primary is operating in discontinuous mode. The secondary output V_{OUT2} is normally set as shown in Figure 5 by the turns ratio N of the transformer. However, if the controller goes into discontinuous mode and halts switching due to a light primary load current, then V_{OUT2} will droop. An external resistor divider from V_{OUT2} to the FCB pin sets a minimum voltage $V_{OUT2(MIN)}$ below which continuous operation is forced until V_{OUT2} has risen above its minimum.

$$V_{OUT2(MIN)} = 0.6V\left(1+\frac{R4}{R3}\right)$$

Fault Conditions: Current Limit and Foldback

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the LTC3770, the maximum sense voltage is controlled by the voltage on the V_{RNG} pin. With valley current control, the maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current. The corresponding output current limit is:

$$I_{LIMIT} = \frac{V_{SNS(MAX)}}{R_{DS(ON)}\ \rho_T} + \frac{1}{2}\Delta I_L$$

The current limit value should be checked to ensure that $I_{LIMIT(MIN)} > I_{OUT(MAX)}$. The minimum value of current limit generally occurs with the largest V_{IN} at the highest ambient temperature, conditions that cause the largest power loss in the converter. Note that it is important to check for self-consistency between the assumed MOSFET junction temperature and the resulting value of I_{LIMIT} which heats the MOSFET switches.

Caution should be used when setting the current limit based upon the $R_{DS(ON)}$ of the MOSFETs. The maximum current limit is determined by the minimum MOSFET on-resistance. Data sheets typically specify nominal and maximum values for $R_{DS(ON)}$, but not a minimum. A reasonable assumption is that the minimum $R_{DS(ON)}$ lies the same percentage below the typical value as the maximum lies above it. Consult the MOSFET manufacturer for further guidelines.

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To further limit current in the event of a short circuit to ground, the LTC3770 includes foldback current limiting. If the output falls by more than 60%, then the maximum sense voltage is progressively lowered to about one tenth of its full value.

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces the 5V supply that powers the drivers and internal circuitry within the LTC3770. The $INTV_{CC}$ pin can supply up to 50mA RMS and must be bypassed to ground with a minimum of 4.7µF low ESR tantalum capacitor or other low ESR capacitor. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate drivers. Applications using large MOSFETs with a high input voltage and high frequency of operation may cause the LTC3770 to exceed its maximum junction temperature rating or RMS current rating. Most of the supply current drives the MOSFET gates. In continuous mode operation, this current is $I_{GATECHG} = f(Q_{g(TOP)} + Q_{g(BOT)})$. The junction temperature can be estimated from the equations given in Note 2 of the Electrical Characteristics. For example, the LTC3770EG is limited to less than 14mA from a 30V supply:

$$T_J = 70°C + (14mA)(30V)(130°C/W) = 125°C$$

External Gate Drive Buffers

The LTC3770 drivers are adequate for driving up to about 50nC into MOSFET switches with RMS currents of 50mA. Applications with larger MOSFET switches or operating at frequencies requiring greater RMS currents will benefit from using external gate drive buffers such as the LTC1693. Alternately, the external buffer circuit shown in Figure 6 can be used.

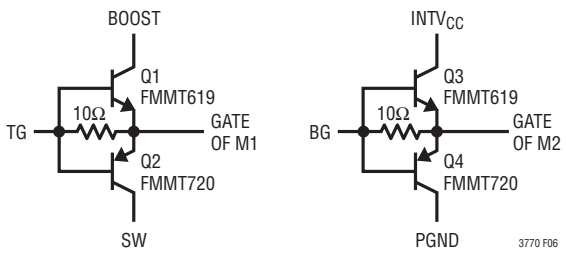


Figure 6. Optional External Gate Driver

Soft-Start and Tracking

The LTC3770 has the ability to either soft-start by itself with a capacitor or track the output of another supply. When the device is configured to soft-start by itself, a capacitor should be connected to the TRACK/SS pin. The LTC3770 is put in a low quiescent current shutdown state ($I_Q < 30µA$) if the RUN pin voltage is below 1.5V. The TRACK/SS pin is actively pulled to ground in this shutdown state. Once the RUN pin voltage is above 1.5V, the LTC3770 is powered up. A soft-start current of 1.4µA then starts to charge the soft-start capacitor C_{SS}. Pin Z1 must be grounded for soft-start operation. Note that soft-start is achieved not by limiting the maximum output current of the controller but by controlling the ramp rate of the output voltage. Current foldback is disabled during this soft-start phase. During the soft-start phase, the LTC3770 is ramping the reference voltage until it is 20% below the voltage set by the V_{REFIN} pin. The forced continuous mode is also disabled and PGOOD signal is forced low during this phase. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = 0.8 \bullet V_{REFIN} \bullet C_{SS}/1.4µA$$

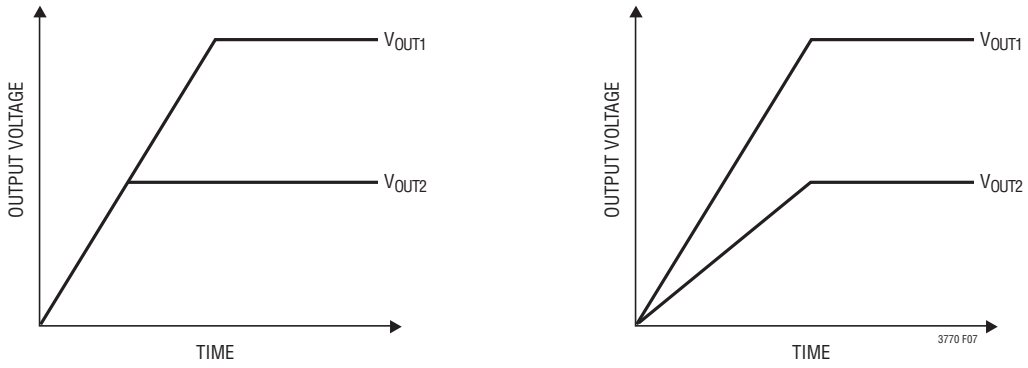
When the device is configured to track another supply, the feedback voltage of the other supply is duplicated by a resistor divider and applied to the TRACK/SS pin. Pin Z1 should be tied to $INTV_{CC}$ to turn off the soft-start current in this mode. Therefore, the voltage ramp rate on this pin is determined by the ramp rate of the other supply output voltage.

Output Voltage Tracking

The LTC3770 allows the user to program how its output ramps up and down by means of the TRACK/SS pin. Through this pin, the output can be set up to either coincidentally or ratiometrically track with another supply's output, as shown in Figure 7. In the following discussions, V_{OUT1} refers to the master LTC3770's output and V_{OUT2} refers to the slave LTC3770's output.

To implement the coincident tracking in Figure 7a, connect an additional resistive divider to V_{OUT1} and connect its midpoint to the TRACK/SS pin of the slave IC. The ratio of this divider should be selected the same as that of the slave IC's feedback divider shown in Figure 8. In this

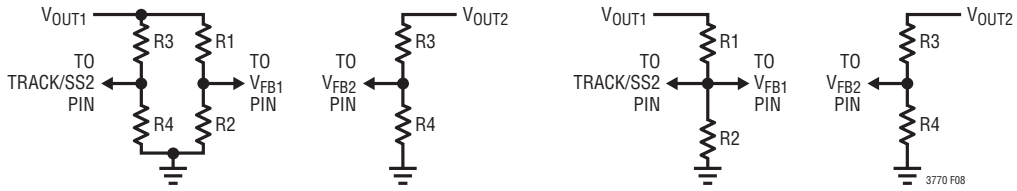
APPLICATIONS INFORMATION



(7a) Coincident Tracking

(7b) Ratiometric Tracking

Figure 7. Two Different Modes of Output Voltage Tracking



(8a) Coincident Tracking Setup

(8b) Ratiometric Tracking Setup

Figure 8. Setup for Coincident and Ratiometric Tracking

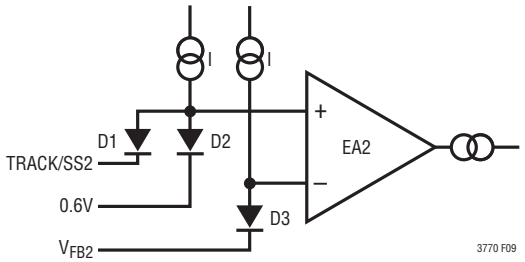


Figure 9. Equivalent Input Circuit of Error Amplifier

tracking mode, V_{OUT1} must be set higher than V_{OUT2}. To implement the ratiometric tracking, the ratio of the divider should be exactly the same as the master IC's feedback divider. Note that the pin Z1 of the slave IC should be tied to $INTV_{CC}$ so that the internal soft-start current is disabled in both tracking modes or it will introduce a small error on the tracking voltage depending on the absolute values of the tracking resistive divider.

By selecting different resistors, the LTC3770 can achieve different modes of tracking including the two in Figure 7. So which mode should be programmed? While either mode in Figure 7 satisfies most practical applications, there do exist some tradeoffs. The ratiometric mode saves a pair of resistors, but the coincident mode offers better output regulation. This can be better understood with the help of Figure 9. At the input stage of the slave IC's error amplifier, two common anode diodes are used to clamp the equivalent reference voltage and an additional diode is used to match the shifted common mode voltage. The top two current sources are of the same amplitude. In the coincident mode, the TRACK/SS voltage is substantially higher than 0.6V at steady state and effectively turns off D1. D2 and D3 will therefore conduct the same current and offer tight matching between V_{FB2} and the internal precision 0.6V reference. In the ratiometric mode, however, TRACK/SS equals 0.6V at steady state. D1 will divert part of the bias current to make V_{FB2} slightly lower than 0.6V. Although this error is minimized by the exponential I-V characteristic of the diode, it does impose a finite amount of output voltage deviation. Furthermore, when the master IC's output experiences dynamic excursion (under load transient, for example), the slave IC output will be affected as well. *For better output regulation, use the coincident tracking mode instead of ratiometric.*

APPLICATIONS INFORMATION

Margining

Margining is a way to program the reference voltage to the error amplifier to a voltage different from the default 0.6V. Margining is useful for customers who want to stress their systems by varying supply voltages during testing. The reference voltage to the error amplifier is set according to the following equation when the margining function is enabled:

$$V_{REFIN} = 0.6V \pm(1.18V/R4) \bullet R3$$

Referring to the functional diagram, 0.6V is the buffered system reference at the V_{REFOUT} pin. R3 and R4 are resistors used for programming the amount of margining. V_{REFIN} should be a voltage between 0.5V and 1V.

There are two logic control pins, MARGIN1 and MARGIN0, to determine whether the margining function is enabled, Margin up(+) or Margin down(–). Table 1 summarizes the configurations:

Table 1. Margining Function

MARGIN1	MARGIN0	MODE
LOW	LOW	No Margining
LOW	HIGH	Margin Up
HIGH	LOW	Margin Down
HIGH	HIGH	No Margining

The buffered reference at V_{REFOUT} has the ability to source a large amount of current. However, it can only sink a maximum of 50µA of current. To increase the sinking capability of this reference, connect a resistor to ground at this pin. One may also be tempted to connect a large capacitor to this pin to filter out the noise. **However, it is recommended that no larger than 100pF of capacitance should be connected to this pin.**

Phase-Locked Loop and Frequency Synchronization

The LTC3770 has a phase-locked loop comprised of an internal voltage controlled oscillator and phase detector. This allows the top MOSFET turn-on to be locked to the rising edge of an external source. The frequency range of the voltage controlled oscillator is ±30% around the center frequency f_O. The center frequency is the operating frequency discussed in the previous section. The LTC3770 incorporates a pulse detection circuit that will detect a clock on the PLLIN pin. In turn, it will turn on the phase-locked loop function. The pulse width of the clock has to be greater than 400ns and the amplitude of the clock should be greater than 2V.

During the start-up phase, phase-locked loop function is disabled. When LTC3770 is not in synchronization mode, PLLFLTR pin voltage is set to around 1.18V. Frequency synchronization is accomplished by changing the internal on-time current according to the voltage on the PLLFLTR pin.

The phase detector used is an edge sensitive digital type which provides zero degrees phase shift between the external and internal pulses. This type of phase detector will not lock up on input frequencies close to the harmonics of the VCO center frequency. The PLL hold-in range, Δf_H, is equal to the capture range, Δf_C:

$$\Delta f_H = \Delta f_C = \pm 0.3\ f_O$$

The output of the phase detector is a complementary pair of current sources charging or discharging the external filter network on the PLLFLTR pin. A simplified block diagram is shown in Figure 10.

If the external frequency (f_{PLLIN}) is greater than the oscillator frequency f_O, current is sourced continuously, pulling up the PLLFLTR pin. When the external frequency is less than f_O, current is sunk continuously, pulling down the PLLFLTR pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. Thus the voltage on the PLLFLTR pin is adjusted until the phase and frequency of the external and internal

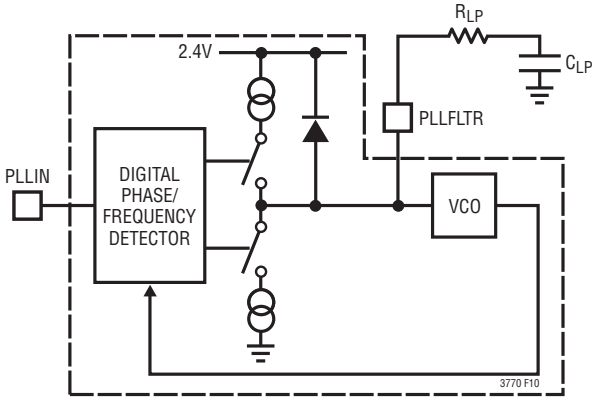


Figure 10. Phase-Locked Loop Block Diagram

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oscillators are identical. At this stable operating point the phase comparator output is open and the filter capacitor C_{LP} holds the voltage. The LTC3770 PLLIN pin must be driven from a low impedance source such as a logic gate located close to the pin.

The loop filter components (C_{LP}, R_{LP}) smooth out the current pulses from the phase detector and provide a stable input to the voltage controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} =10kΩ and C_{LP} is 0.01µF to 0.1µF.

Dead Time Control

To further optimize the efficiency, the LTC3770 gives users some control over the dead time of the Top gate low and Bottom gate high transition. By applying a DC voltage on the Z0 pin, the TG low BG high dead time can be programmed. Because the dead time is a strong function of the load current and the type of MOSFET used, users need to be careful to optimize the dead time for their particular applications. Figure 11 shows the relation between the TG Low BG High Dead time by varying the Z0 voltages. For an application using LTC3770 with load current of 5A and IR7811W MOSFETs, the dead time could be optimized. To make sure that there is no shoot-through under all conditions, a dead time of 70ns is selected. This corresponds to a DC voltage about 2.6V on Z0 pin. This voltage can easily be generated with a resistor divider off $INTV_{CC}$.

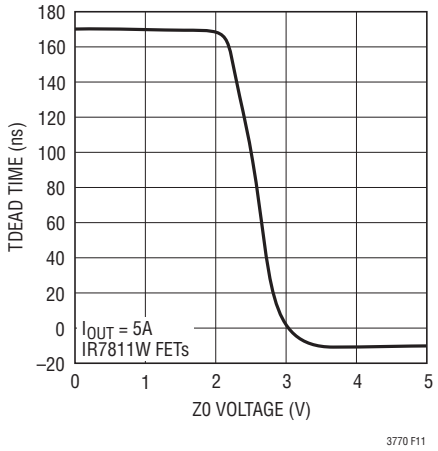

Figure 11. TG Low BG High Dead Time vs Z0 Voltage

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LTC3770 circuits:

1. DC I^2R losses. These arise from the resistances of the MOSFETs, inductor and PC board traces and cause the efficiency to drop at high output currents. In continuous mode the average output current flows through L, but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and the board traces to obtain the DC I^2R loss. For example, if $R_{DS(ON)}$ = 0.01Ω and R_L = 0.005Ω, the loss will range from 15mW to 1.5W as the output current varies from 1A to 10A.

2. Transition loss. This loss arises from the brief amount of time the top MOSFET spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. The loss is significant at input voltages above 20V and can be estimated from:

$$\text{Transition Loss} \cong (1.7A^{-1})\ V_{IN}^2\ I_{OUT}\ C_{RSS}\ f$$

3. $INTV_{CC}$ current. This is the sum of the MOSFET driver and control currents.

4. C_{IN} loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator. It must have a very low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

Other losses, including C_{OUT} ESR loss, Schottky diode D1 conduction loss during dead time and inductor core loss generally account for less than 2% additional loss.

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency.

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If you make a change and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. The I_{TH} pin external components shown in Figure 12 will provide adequate compensation for most applications. For a detailed explanation of switching control loop theory see Application Note 76.

Design Example

As a design example, take a supply with the following specifications: V_{IN} = 5V to 28V (15V nominal), V_{OUT} = 2.5V ±5%, $I_{OUT(MAX)}$ = 10A, f = 450kHz. First, calculate the timing resistor with $V_{ON} = V_{OUT}$:

$$R_{ON} = \frac{2.5V}{3(2.5V)(450kHz)(10pF)} = 74k\Omega$$

and choose the inductor for about 40% ripple current at the maximum V_{IN}:

$$L = \frac{2.5V}{(450kHz)(0.4)(10A)}\left(1-\frac{2.5V}{28V}\right) = 1.3\mu H$$

Selecting a standard value of 1.8µH results in a maximum ripple current of:

$$\Delta I_L = \frac{2.5V}{(450kHz)(1.8\mu H)}\left(1-\frac{2.5V}{28V}\right) = 2.8A$$

Next, choose the synchronous MOSFET switch. Choosing a Si4874 ($R_{DS(ON)}$ = 0.0083Ω (NOM) 0.010Ω (MAX), θ_{JA} = 40°C/W) yields a nominal sense voltage of:

$V_{SNS(NOM)}$ = (10A)(1.3)(0.0083Ω) = 108mV

Tying V_{RNG} to 1.1V will set the current sense voltage range for a nominal value of 110mV with current limit occurring at 146mV. To check if the current limit is acceptable, assume a junction temperature of about 80°C above a 70°C ambient with $\rho_{150°C}$ = 1.5:

$$I_{LIMIT} \geq \frac{146mV}{(1.5)(0.010\Omega)} + \frac{1}{2}(2.8A) = 11A$$

and double check the assumed T_J in the MOSFET:

$$P_{BOT} = \frac{28V - 2.5V}{28V}(11A)^2(1.5)(0.010\Omega) = 1.65W$$

T_J = 70°C + (1.65W)(40°C/W) = 136°C

Because the top MOSFET is on for such a short time, an Si4884 $R_{DS(ON)(MAX)}$ = 0.0165Ω, C_{RSS} = 100pF, θ_{JA} = 40°C/W will be sufficient. Checking its power dissipation at current limit with $\rho_{100°C}$ = 1.4:

$$P_{TOP} = \frac{2.5V}{28V}(11A)^2(1.4)(0.0165\Omega) + (1.7)(28V)^2(11A)(100pF)(250kHz) = 0.25W + 0.37W = 0.62W$$

T_J = 70°C + (0.62W)(40°C/W) = 95°C

The junction temperature will be significantly less at nominal current, but this analysis shows that careful attention to heat sinking on the board will be necessary in this circuit.

C_{IN} is chosen for an RMS current rating of about 3A at 85°C. The output capacitors are chosen for a low ESR of 0.013Ω to minimize output voltage changes due to inductor ripple current and load steps. The ripple voltage will be only:

$\Delta V_{OUT(RIPPLE)} = \Delta I_{L(MAX)}$ (ESR)

= (2.8A) (0.013Ω) = 36mV

However, a 0A to 10A load step will cause an output change of up to:

$\Delta V_{OUT(STEP)} = \Delta I_{LOAD}$ (ESR) = (10A) (0.013Ω) = 130mV

An optional 22µF ceramic output capacitor is included to minimize the effect of ESL in the output ripple. The complete circuit is shown in Figure 12.

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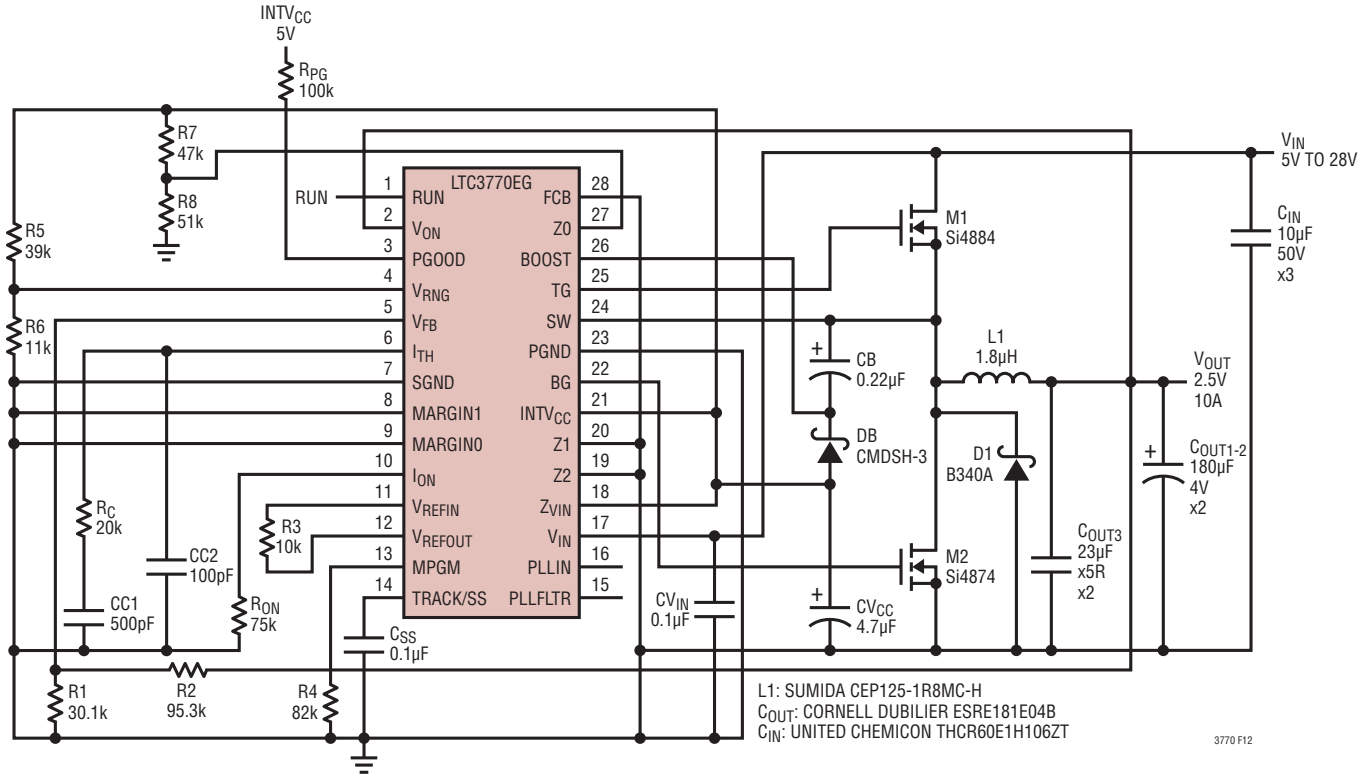


Figure 12. Design Example: 2.5V/10A at 450kHz

To set a ±25% margining, select the resistors R3, R4 such that:

$$V_{REFIN} = 0.6 \pm 25\% \bullet 0.6$$

or

$$\frac{1.18 \bullet R3}{R4} = 25\% \bullet 0.6$$

$$R4 \approx 8R3$$

Choose R3 to be 10k, R4 to be 82k for this application.

PC Board Layout Checklist

When laying out a PC board follow one of two suggested approaches. The simple PC board layout requires a dedicated ground plane layer. Also, for higher currents, it is recommended to use a multilayer board to help with heat sinking power components.

- The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.
- Place C_{IN}, C_{OUT}, MOSFETs, D1 and inductor all in one compact area. It may help to have some components on the bottom side of the board.
- Use an immediate via to connect the components to ground plane including SGND and PGND of LTC3770. Use several bigger vias for power components.
- Use compact plane for switch node (SW) to improve cooling of the MOSFETs and to keep EMI down.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power component. You can connect the copper areas to any DC net (V_{IN}, V_{OUT}, GND or to any other DC rail in your system).

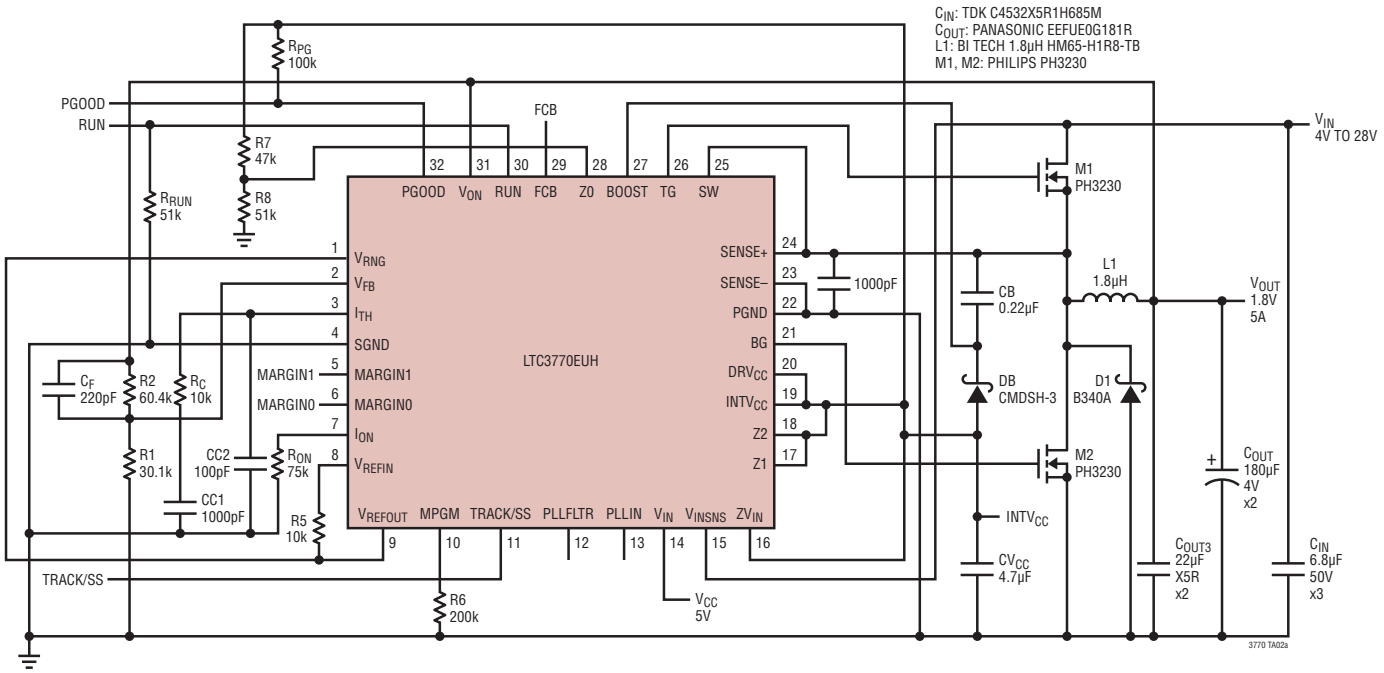
APPLICATIONS INFORMATION

When laying out a printed circuit board, without a ground plane, use the following checklist to ensure proper operation of the controller.

- Segregate the signal and power grounds. All small signal components should return to the SGND pin at one point which is then tied to the PGND pin close to the source of M2.
- Place M2 as close to the controller as possible, keeping the PGND, BG and SW traces short.
- Connect the input capacitor(s) C_{IN} close to the power MOSFETs. This capacitor carries the MOSFET AC current.
- Keep the high dV/dt SW, BOOST and TG nodes away from sensitive small-signal nodes.
- Connect the $INTV_{CC}$ decoupling capacitor CV_{CC} closely to the $INTV_{CC}$ and PGND pins.
- Connect the top driver boost capacitor CB closely to the BOOST and SW pins.
- Connect the V_{IN} pin decoupling capacitor C_{IN} closely to the V_{IN} and PGND pins.

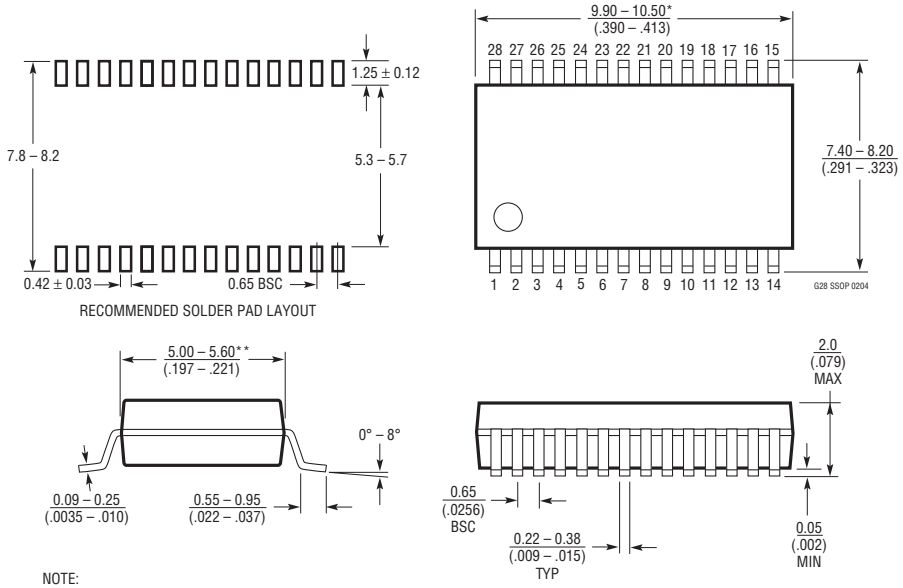
TYPICAL APPLICATIONS

1.8V/5A at 450kHz with Tracking



PACKAGE DESCRIPTION

G Package
28-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)

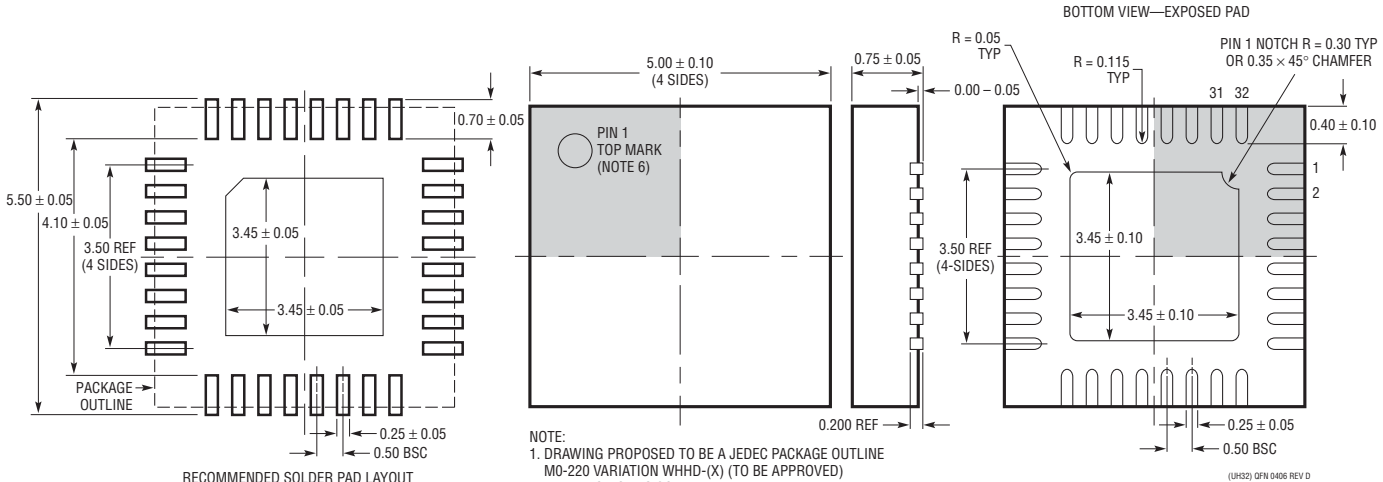


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE