Dual Synchronous, 400mA/800mA, 2.25MHz Step-Down DC/DC Regulator

FEATURES

- **High Efficiency: Up to 95%**
- **Very Low Quiescent Current: Only 40µA**
- **Low Output Ripple Burst Mode® Operation**
- **2.25MHz Constant-Frequency Operation**
- **High Switch Current: 0.7A and 1.2A**
- **No Schottky Diodes Required**
- **Low $R_{DS(ON)}$ Internal Switches: 0.35Ω**
- Current Mode Operation for Excellent Line and Load Transient Response
- Short-Circuit Protected
- Low Dropout Operation: 100% Duty Cycle
- Ultralow Shutdown Current: I_Q < 1µA
- Output Voltages from 5V down to 0.6V
- Power-On Reset Output
- Externally Synchronizable Oscillator
- Small Thermally Enhanced MSOP and 3mm × 3mm DFN Packages

APPLICATIONS

- PDAs/Palmtop PCs
- Digital Cameras
- Cellular Phones
- Portable Media Players
- PC Cards
- Wireless and DSL Modems

DESCRIPTION

The LTC®3548 is a dual, constant-frequency, synchronous step down DC/DC converter. Intended for low power applications, it operates from 2.5V to 5.5V input voltage range and has a constant 2.25MHz switching frequency, allowing the use of tiny, low cost capacitors and inductors with a profile ≤1mm. Each output voltage is adjustable from 0.6V to 5V. Internal synchronous 0.35Ω, 0.7A/1.2A power switches provide high efficiency without the need for external Schottky diodes.

A user selectable mode input is provided to allow the user to trade-off noise ripple for low power efficiency. Burst Mode operation provides high efficiency at light loads, while pulse-skipping mode provides low noise ripple at light loads.

To further maximize battery runtime, the P-channel MOSFETs are turned on continuously in dropout (100% duty cycle), and both channels draw a total quiescent current of only 40µA. In shutdown, the device draws <1µA.

TYPICAL APPLICATION

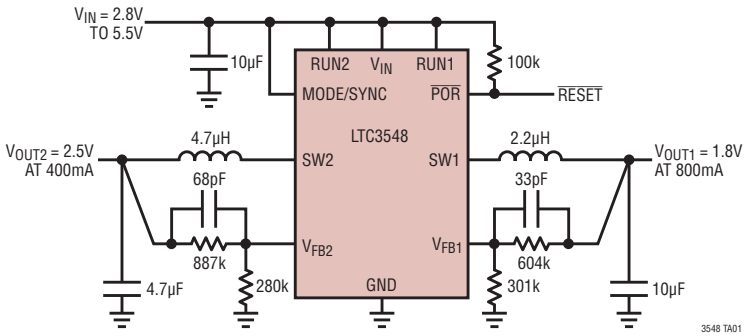
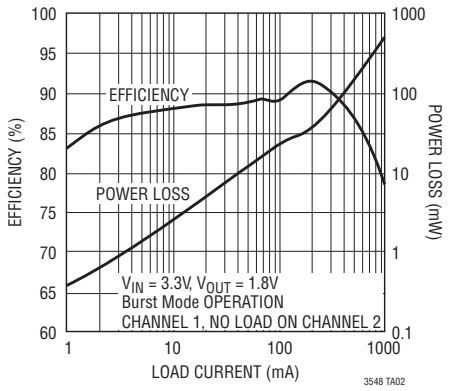


Figure 1. 2.5V/1.8V at 400mA/800mA Step-Down Regulators

LTC3548 Efficiency Curve



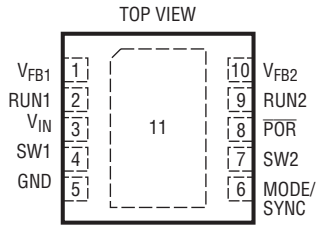
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltages ..... –0.3V to 6V
V_{FB1}, V_{FB2} Voltages ..... –0.3V to V_{IN} +0.3V
RUN1, RUN2 Voltages ..... –0.3V to V_{IN}
MODE/SYNC Voltage ..... –0.3V to V_{IN} + 0.3V
SW1, SW2 Voltage ..... –0.3V to V_{IN} + 0.3V
$\overline{POR}$ Voltage ..... –0.3V to 6V

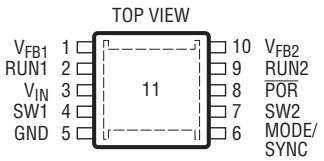
Operating Temperature Range (Note 2) .... –40°C to 85°C
Junction Temperature (Note 5) ..... 125°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
MSE Only ..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 45°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 11) IS PGND, MUST BE CONNECTED TO GND
(SOLDERED TO A 4-LAYER BOARD)



MSE PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 45°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 11) IS PGND, MUST BE CONNECTED TO GND
(SOLDERED TO A 4-LAYER BOARD)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3548EDD#PBF	LTC3548EDD#TRPBF	LBNJ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3548IDD#PBF	LTC3548IDD#TRPBF	LBNJ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3548EMSE#PBF	LTC3548EMSE#TRPBF	LTBNH	10-Lead Plastic MSOP	–40°C to 85°C
LTC3548IMSE#PBF	LTC3548IMSE#TRPBF	LTBNH	10-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, unless otherwise specified. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage Range		●	2.5		5.5	V
I_{FB}	Feedback Pin Input Current		●			30	nA
V_{FB}	Feedback Voltage (Note 3)	0°C ≤ T_A ≤ 85°C –40°C ≤ T_A ≤ 85°C	 ●	0.588 0.585	0.6 0.6	0.612 0.612	V V
$\Delta V_{LINEREG}$	Reference Voltage Line Regulation	V_{IN} = 2.5V to 5.5V (Note 3)			0.3	0.5	%V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, unless otherwise specified. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\Delta V_{LOADREG}$	Output Voltage Load Regulation	(Note 3)			0.5		%
I_S	Input DC Supply Current Active Mode Sleep Mode Shutdown	(Note 4) $V_{FB1} = V_{FB2} = 0.5V$ $V_{FB1} = V_{FB2} = 0.63V$, MODE/SYNC = 3.6V RUN = 0V, V_{IN} = 5.5V, MODE/SYNC = 0V			 700 40 0.1	 950 60 1	 µA µA µA
f_{OSC}	Oscillator Frequency	V_{FB} = 0.6V	●	1.8	2.25	2.7	MHz
f_{SYNC}	Synchronization Frequency				2.25		MHz
I_{LIM}	Peak Switch Current Limit Channel 1 Peak Switch Current Limit Channel 2	V_{IN} = 3V, V_{FB} = 0.5V, Duty Cycle <35% V_{IN} = 3V, V_{FB} = 0.5V, Duty Cycle <35%		0.95 0.6	1.2 0.7	1.6 0.9	A A
$R_{DS(ON)}$	Top Switch On-Resistance Bottom Switch On-Resistance	(Note 6) (Note 6)			0.35 0.30	0.45 0.45	Ω Ω
$I_{SW(LKG)}$	Switch Leakage Current	V_{IN} = 5V, V_{RUN} = 0V, V_{FB} = 0V			0.01	1	µA
POR	Power-On Reset Threshold	V_{FB} Ramping Down, MODE/SYNC = 0V			–8.5		%
	Power-On Reset On-Resistance				100	200	Ω
	Power-On Reset Delay				262,144		Cycles
V_{RUN}	RUN Threshold		●	0.3	1	1.5	V
I_{RUN}	RUN Leakage Current		●		0.01	1	µA
MODE	Mode Threshold Low Mode Threshold High			0 V_{IN} – 0.5		0.5 V_{IN}	V V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3548 is guaranteed to meet specified performance from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3548I is guaranteed to meet specified performance over the full –40°C to 85°C temperature range.

Note 3: The LTC3548 is tested in a proprietary test mode that connects V_{FB} to the output of the error amplifier.

Note 4: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

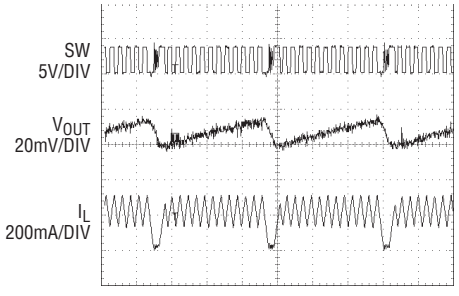
Note 5: T_J is calculated from the ambient T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D \bullet \theta_{JA})$.

Note 6: The DFN switch on-resistance is guaranteed by correlation to wafer level measurements.

TYPICAL PERFORMANCE CHARACTERISTICS

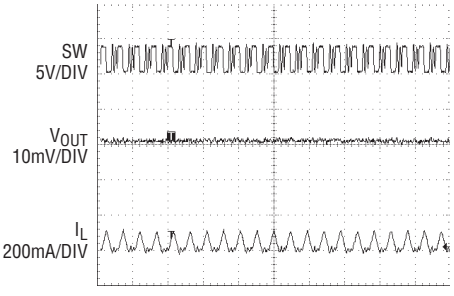
T_A = 25°C unless otherwise specified.

Burst Mode Operation



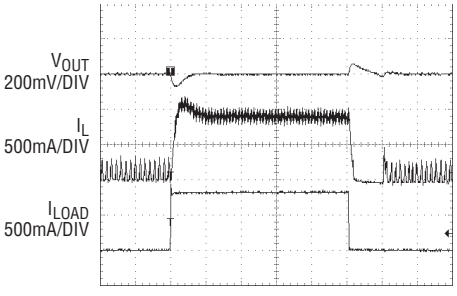
V_{IN} = 3.6V 2µs/DIV
V_{OUT} = 1.8V
I_{LOAD} = 180mA
CHANNEL 1; CIRCUIT OF FIGURE 3

Pulse-Skipping Mode



V_{IN} = 3.6V 1µs/DIV
V_{OUT} = 1.8V
I_{LOAD} = 30mA
CHANNEL 1; CIRCUIT OF FIGURE 3

Load Step

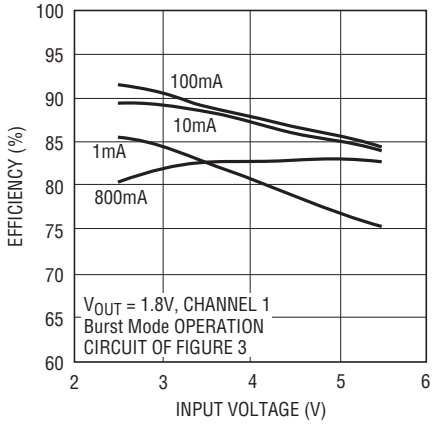


V_{IN} = 3.6V 20µs/DIV
V_{OUT} = 1.8V
I_{LOAD} = 80mA TO 800mA
CHANNEL 1; CIRCUIT OF FIGURE 3

TYPICAL PERFORMANCE CHARACTERISTICS

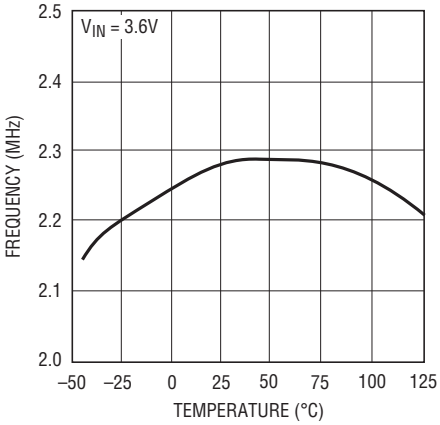
T_A = 25°C unless otherwise specified.

Efficiency vs Input Voltage



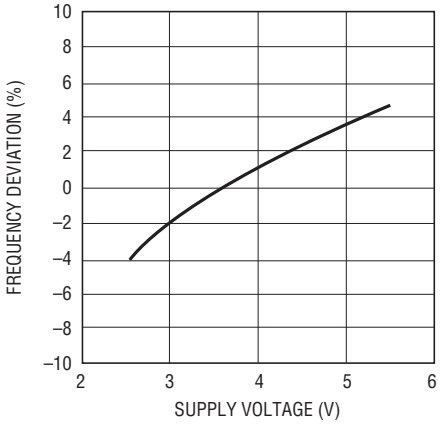
3548 G04

Oscillator Frequency vs Temperature



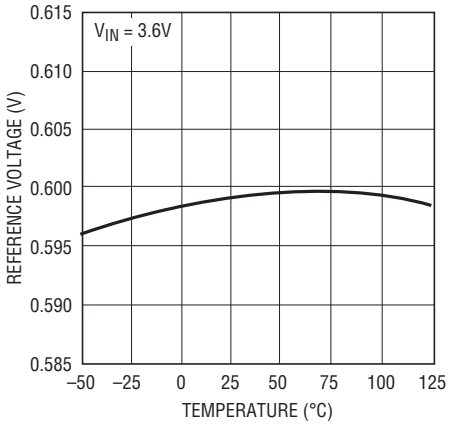
3548 G05

Oscillator Frequency vs Supply Voltage



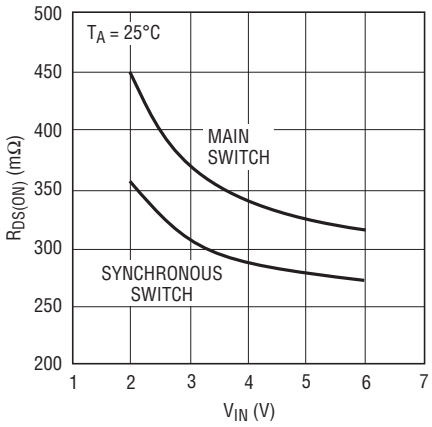
3548 G06

Reference Voltage vs Temperature



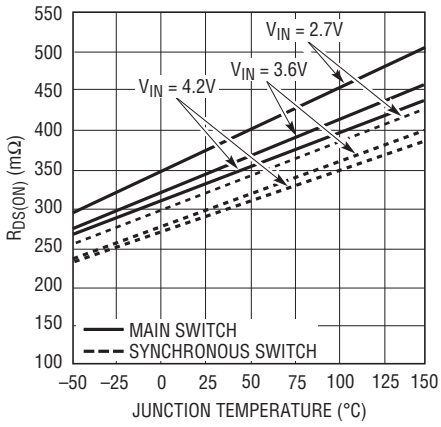
3548 G07

$R_{DS(ON)}$ vs Input Voltage



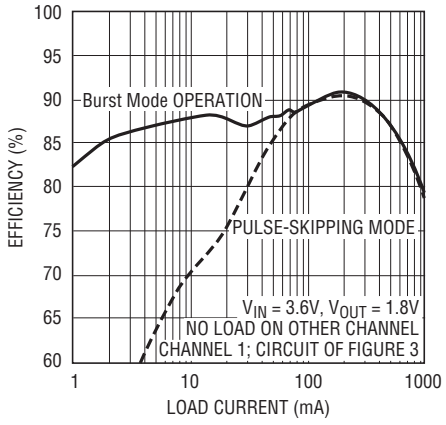
3548 G08

$R_{DS(ON)}$ vs Junction Temperature



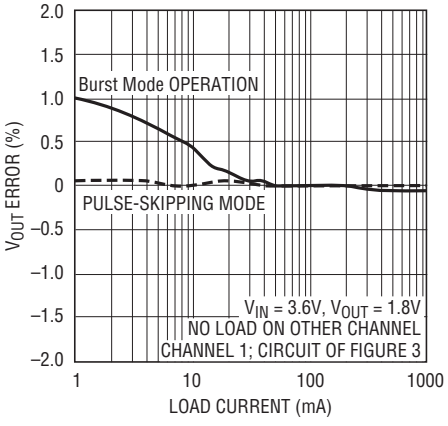
3548 G09

Efficiency vs Load Current



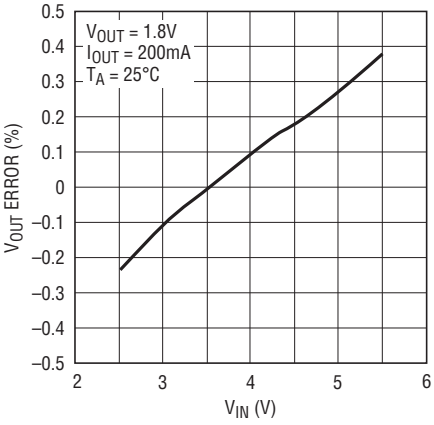
3548 G11

Load Regulation



3548 G12

Line Regulation

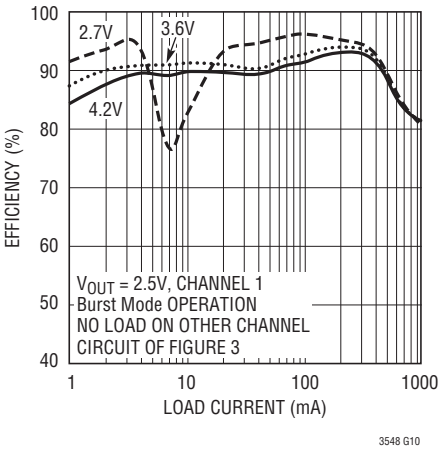


3548 G15

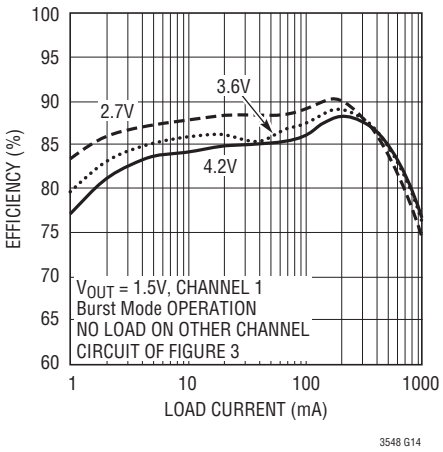
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C unless otherwise specified.

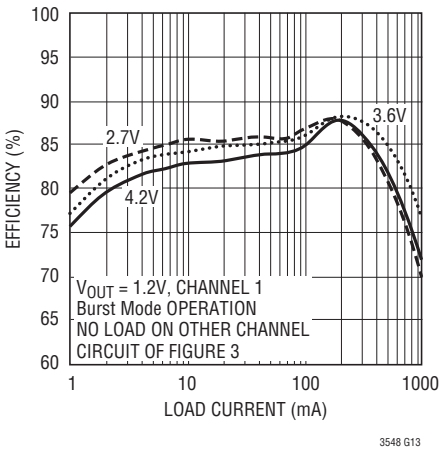
Efficiency vs Load Current



Efficiency vs Load Current



Efficiency vs Load Current



PIN FUNCTIONS

V_{FB1} (Pin 1): Output Feedback. Receives the feedback voltage from the external resistive divider across the output. Nominal voltage for this pin is 0.6V.

RUN1 (Pin 2): Regulator 1 Enable. Forcing this pin to V_{IN} enables regulator 1, while forcing it to GND causes regulator 1 to shut down. This pin must be driven; do not float.

V_{IN} (Pin 3): Main Power Supply. Must be closely decoupled to GND.

SW1 (Pin 4): Regulator 1 Switch Node Connection to the Inductor. This pin swings from V_{IN} to GND.

GND (Pin 5): Ground. This pin is not connected internally. Connect to PCB ground for optimum shielding.

MODE/SYNC (Pin 6): Combination Mode Selection and Oscillator Synchronization. This pin controls the operation of the device. When tied to V_{IN} or GND, Burst Mode operation or pulse-skipping mode is selected, respectively. Do not float this pin. The oscillation frequency can be synchronized to an external oscillator applied to this pin and pulse-skipping mode is automatically selected.

SW2 (Pin 7): Regulator 2 Switch Node Connection to the Inductor. This pin swings from V_{IN} to GND.

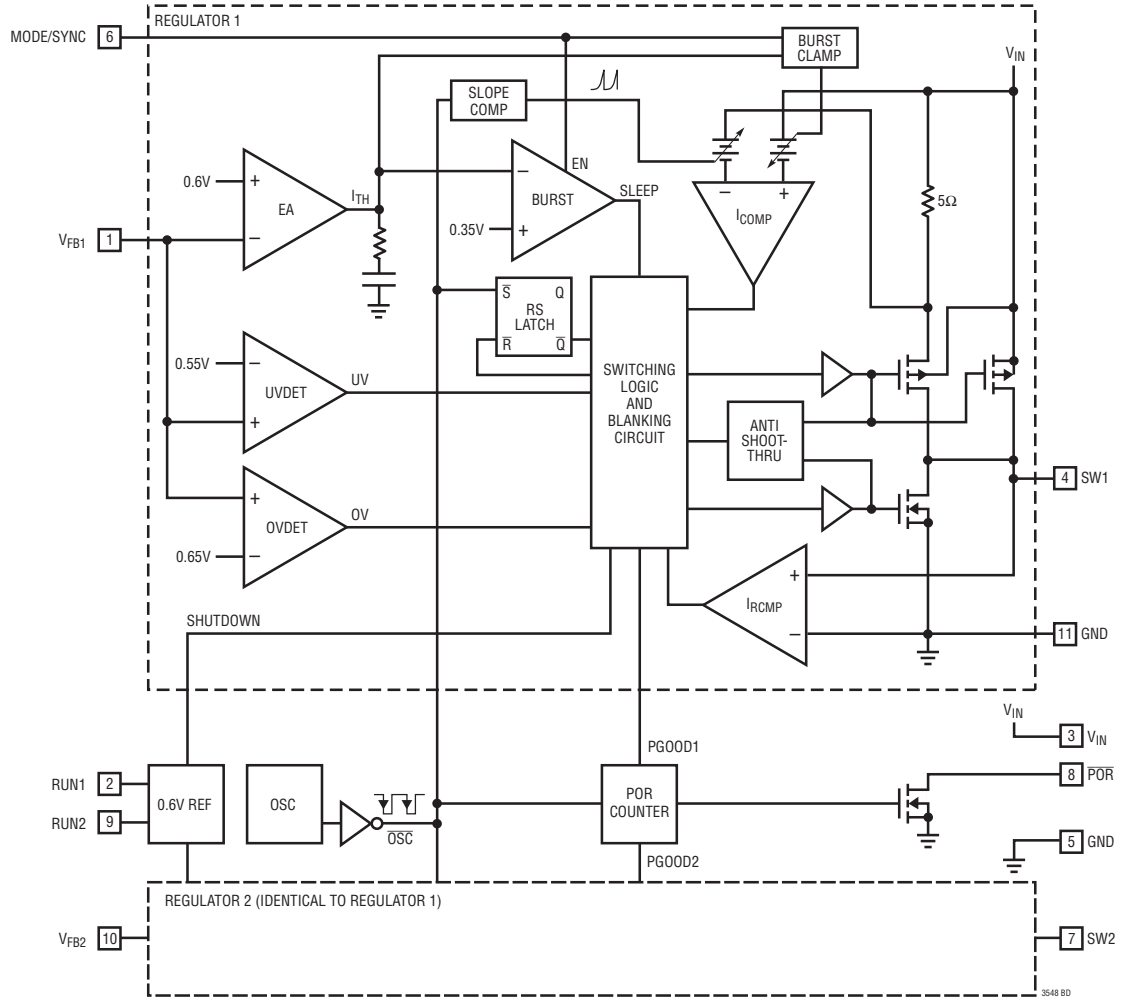
$\overline{POR}$ (Pin 8): Power-On Reset . This common-drain logic output is pulled to GND when the output voltage falls below –8.5% of regulation and goes high after 117ms when both channels are within regulation.

RUN2 (Pin 9): Regulator 2 Enable. Forcing this pin to V_{IN} enables regulator 2, while forcing it to GND causes regulator 2 to shut down. This pin must be driven; do not float.

V_{FB2} (Pin 10): Output Feedback. Receives the feedback voltage from the external resistive divider across the output. Nominal voltage for this pin is 0.6V.

Exposed Pad (GND) (Pin 11): Power Ground. Connect to the (–) terminal of C_{OUT}, and (–) terminal of C_{IN}. Must be connected to electrical ground on PCB.

BLOCK DIAGRAM



OPERATION

The LTC3548 uses a constant-frequency, current mode architecture. The operating frequency is set at 2.25MHz and can be synchronized to an external oscillator. Both channels share the same clock and run in-phase. To suit a variety of applications, the selectable Mode pin allows the user to choose between low noise and high efficiency.

The output voltage is set by an external divider returned to the V_{FB} pins. An error amplifier compares the divided output voltage with a reference voltage of 0.6V and adjusts the peak inductor current accordingly. An undervoltage comparator will pull the $\overline{POR}$ output low if the output voltage is not above –8.5% of the reference voltage. The $\overline{POR}$ output will go high after 262,144 clock cycles (about 117ms) of achieving regulation.

Main Control Loop

During normal operation, the top power switch (P-channel MOSFET) is turned on at the beginning of a clock cycle when the V_{FB} voltage is below the the reference voltage. The current into the inductor and the load increases until the current limit is reached. The switch turns off and energy stored in the inductor flows through the bottom switch (N-channel MOSFET) into the load until the next clock cycle.

The peak inductor current is controlled by the internally compensated I_{TH} voltage, which is the output of the error amplifier.This amplifier compares the V_{FB} pin to the 0.6V reference. When the load current increases, the V_{FB} voltage decreases slightly below the reference.

OPERATION

This decrease causes the error amplifier to increase the I_{TH} voltage until the average inductor current matches the new load current.

The main control loop is shut down by pulling the RUN pin to ground.

Low Current Operation

By selecting MODE/SYNC (Pin 6), two modes are available to control the operation of the LTC3548 at low currents. Both modes automatically switch from continuous operation to the selected mode when the load current is low.

To optimize efficiency, the Burst Mode operation can be selected. When the load is relatively light, the LTC3548 automatically switches into Burst Mode operation, in which the PMOS switch operates intermittently based on load demand with a fixed peak inductor current. By running cycles periodically, the switching losses which are dominated by the gate charge losses of the power MOSFETs are minimized. The main control loop is interrupted when the output voltage reaches the desired regulated value. A voltage comparator trips when I_{TH} is below 0.35V, shutting off the switch and reducing the power. The output capacitor and the inductor supply the power to the load until I_{TH} exceeds 0.65V, turning on the switch and the main control loop which starts another cycle.

For lower ripple noise at low currents, the pulse-skipping mode can be used. In this mode, the LTC3548 continues to switch at a constant frequency down to very low currents, where it will begin skipping pulses. The efficiency in pulse-skipping mode can be improved slightly by connecting the SW node to the MODE/SYNC input which reduces the clock frequency by approximately 30%.

Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases to 100% which is the dropout condition. In dropout, the PMOS switch is turned on continuously with the output voltage being equal to the input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor.

An important design consideration is that the $R_{DS(ON)}$ of the P-channel switch increases with decreasing input supply voltage (see Typical Performance Characteristics). Therefore, the user should calculate the power dissipation when the LTC3548 is used at 100% duty cycle with low input voltage (see Thermal Considerations in the Applications Information section).

Low Supply Operation

To prevent unstable operation, the LTC3548 incorporates an undervoltage lockout circuit which shuts down the part when the input voltage drops below about 1.65V.

APPLICATIONS INFORMATION

A general LTC3548 application circuit is shown in Figure 2. External component selection is driven by the load requirement, and begins with the selection of the inductor L. Once the inductor is chosen, C_{IN} and C_{OUT} can be selected.

Inductor Selection

Although the inductor does not influence the operating frequency, the inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance and increases with higher V_{IN} or V_{OUT}:

$$\Delta I_L = \frac{V_{OUT}}{f_0 \bullet L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple, greater core losses, and lower output current capability. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3 \bullet I_{OUT(MAX)}$, where $I_{OUT(MAX)}$ is 800mA for channel 1 and 400mA for channel 2. The largest ripple current ΔI_L occurs at the maximum input voltage. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L \geq \frac{V_{OUT}}{f_0 \bullet \Delta I_L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

APPLICATIONS INFORMATION

The inductor value will also have an effect on Burst Mode operation. The transition from low current operation begins when the peak inductor current falls below a level set by the burst clamp. Lower inductor values result in higher ripple current which causes this to occur at lower load currents. This causes a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirements and any radiated field/EMI requirements than on what the LTC3548 requires to operate. Table 1 shows some typical surface mount inductors that work well in LTC3548 applications.

Input Capacitor (C_{IN}) Selection

In continuous mode, the input current of the converter is a square wave with a duty cycle of approximately V_{OUT}/V_{IN}. To prevent large voltage transients, a low equivalent series resistance (ESR) input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{MAX} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

where the maximum average output current I_{MAX} equals the peak current minus half the peak-to-peak ripple current, $I_{MAX} = I_{LIM} - \Delta I_L/2$.

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case is commonly used to design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours lifetime. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. An additional 0.1µF to 1µF ceramic capacitor is also recommended on V_{IN} for high frequency decoupling, when not using an all ceramic capacitor solution.

Table 1. Representation Surface Mount Inductors

PART NUMBER	VALUE (µH)	DCR (Ω MAX)	MAX DC CURRENT (A)	SIZE W × L × H (mm^3)
Sumida CDRH3D16	2.2 3.3 4.7	0.075 0.110 0.162	1.20 1.10 0.90	3.8 × 3.8 × 1.8
Sumida CDRH2D11	1.5 2.2	0.068 0.170	0.900 0.780	3.2 × 3.2 × 1.2
Sumida CMD4D11	2.2 3.3	0.116 0.174	0.950 0.770	4.4 × 5.8 × 1.2
Murata LQH32CN	1.0 2.2	0.060 0.097	1.00 0.079	2.5 × 3.2 × 2.0
Toko D312F	2.2 3.3	0.060 0.260	1.08 0.92	2.5 × 3.2 × 2.0
Panasonic ELT5KT	3.3 4.7	0.17 0.20	1.00 0.95	4.5 × 5.4 × 1.2

Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is driven by the required ESR to minimize voltage ripple and load step transients. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8 f_0 C_{OUT}} \right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. With $\Delta I_L = 0.3 \bullet I_{OUT(MAX)}$ the output ripple will be less than 100mV at maximum V_{IN} and $f_O = 2.25MHz$ with:

$$ESR_{COUT} < 150m\Omega$$

Once the ESR requirements for C_{OUT} have been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement, except for an all ceramic solution.

In surface mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirement of the application. Aluminum electrolytic, special polymer, ceramic and dry

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tantalum capacitors are all available in surface mount packages. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR (size) product of any aluminum electrolytic at a somewhat higher price. Special polymer capacitors, such as Sanyo POSCAP, Panasonic Special Polymer (SP), and Kemet A700, offer very low ESR, but have a lower capacitance density than other types. Tantalum capacitors have the highest capacitance density, but they have a larger ESR and it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Aluminum electrolytic capacitors have a significantly larger ESR, and are often used in extremely cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have the lowest ESR and cost, but also have the lowest capacitance density, a high voltage and temperature coefficient, and exhibit audible piezoelectric effects. In addition, the high Q of ceramic capacitors along with trace inductance can lead to significant ringing.

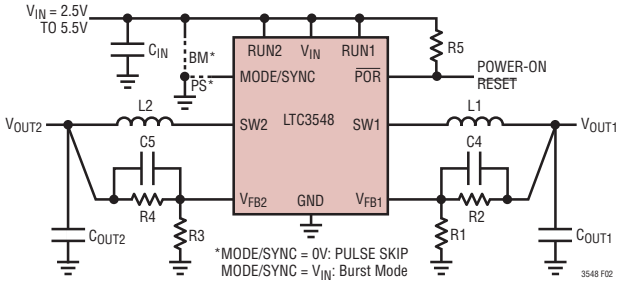

Figure 2. LTC3548 General Schematic

In most cases, 0.1µF to 1µF of ceramic capacitors should also be placed close to the LTC3548 in parallel with the main capacitors for high frequency decoupling.

Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. These are tempting for switching regulator use because of their very low ESR. Unfortunately, the ESR is so low that it can cause loop stability problems. Solid tantalum capacitor ESR generates a loop "zero" at 5kHz to 50kHz that is instrumental in giving acceptable loop phase margin. Ceramic capacitors remain capacitive to beyond 300kHz and usually resonate with their ESL before ESR becomes effective. Also, ceramic caps are prone to temperature effects which requires the designer to check loop stability over the operating temperature range. To minimize their large temperature and voltage coefficients, only X5R or X7R ceramic capacitors should be used. A good selection of ceramic capacitors is available from Taiyo Yuden, AVX, Kemet, TDK and Murata.

Great care must be taken when using only ceramic input and output capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the V_{IN} pin. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, the ringing at the input can be large enough to damage the part.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP} is usually about 2 to 3 times the linear drop of the first cycle. Thus, a good place to start is with the output capacitor size of approximately: More capacitance may be required depending on the duty cycle and load step requirements.

In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 10µF ceramic capacitor is usually enough for these conditions.

Setting the Output Voltage

The LTC3548 develops a 0.6V reference voltage between the feedback pin, V_{FB}, and the ground as shown in Figure 2. The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.6V\left(1+\frac{R2}{R1}\right)$$

Keeping the current small (<5µA) in these resistors maximizes efficiency, but making them too small may allow

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stray capacitance to cause noise problems and reduce the phase margin of the error amp loop.

To improve the frequency response, a feed-forward capacitor C_F may also be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

Power-On Reset

The $\overline{POR}$ pin is an open-drain output which pulls low when either regulator is out of regulation. When both output voltages are above –8.5% of regulation, a timer is started which releases $\overline{POR}$ after 2^{18} clock cycles (about 117ms). This delay can be significantly longer in Burst Mode operation with low load currents, since the clock cycles only occur during a burst and there could be milliseconds of time between bursts. This can be bypassed by tying the $\overline{POR}$ output to the MODE/SYNC input, to force pulse-skipping mode during a reset. In addition, if the output voltage faults during Burst Mode sleep, $\overline{POR}$ could have a slight delay for an undervoltage output condition. This can be avoided by using pulse-skipping mode instead. When either channel is shut down, the $\overline{POR}$ output is pulled low, since one or both of the channels are not in regulation.

Mode Selection and Frequency Synchronization

The MODE/SYNC pin is a multipurpose pin which provides mode selection and frequency synchronization. Connecting this pin to V_{IN} enables Burst Mode operation, which provides the best low current efficiency at the cost of a higher output voltage ripple. Connecting this pin to ground selects pulse-skipping mode, which provides the lowest output ripple, at the cost of low current efficiency.

The LTC3548 can also be synchronized to another LTC3548 by the MODE/SYNC pin. During synchronization, the mode is set to pulse-skipping and the top switch turn-on is synchronized to the rising edge of the external clock.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second-order overshoot/DC ratio cannot be used to determine phase margin. In addition, a feed-forward capacitor, C_F, can be added to improve the high frequency response, as shown in Figure 2. Capacitor C_F provides phase lead by creating a high frequency zero with R2, which improves the phase margin.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

In some applications, a more severe transient can be caused by switching loads with large (>1µF) load input capacitors. The discharged load input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft-starting.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of

Hot Swap is a trademark of Linear Technology Corporation.

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the losses in LTC3548 circuits: 1) V_{IN} quiescent current, 2) switching losses, 3) I^2R losses, 4) other losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics which excludes MOSFET driver and control currents. V_{IN} current results in a small (<0.1%) loss that increases with V_{IN}, even at no load.

2. The switching current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} that is typically much larger than the DC bias current. In continuous mode, $I_{GATECHG} = f_O(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom MOSFET switches. The gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

3. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L, but is "chopped" between the internal top and bottom switches. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (D) as follows:

   $$R_{SW} = (R_{DS(ON)TOP})(D) + (R_{DS(ON)BOT})(1 - D)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses:

   $$I^2R \text{ losses} = (I_{OUT})^2(R_{SW} + R_L)$$

4. Other hidden losses such as copper trace and internal battery resistances can account for additional efficiency degradations in portable systems. It is very important to include these system level losses in the design of a system. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. Other losses including diode conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Thermal Considerations

In a majority of applications, the LTC3548 does not dissipate much heat due to its high efficiency. However, in applications where the LTC3548 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will turn off and the SW node will become high impedance.

To prevent the LTC3548 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$T_J = T_{RISE} + T_{AMBIENT}$$

As an example, consider the case when the LTC3548 is in dropout on both channels at an input voltage of 2.7V with a load current of 400mA and 800mA and an ambient temperature of 70°C. From the Typical Performance Characteristics graph of Switch Resistance, the $R_{DS(ON)}$ resistance of the main switch is 0.425Ω. Therefore, power dissipated by each channel is:

$$P_D = (I_{OUT})^2 \bullet R_{DS(ON)} = 272\text{mW and } 68\text{mW}$$

The MS package junction-to-ambient thermal resistance, θ_{JA}, is 45°C/W. Therefore, the junction temperature of the regulator operating in a 70°C ambient temperature is approximately:

$$T_J = (0.272 + 0.068) \bullet 45 + 70 = 85.3°C$$

which is below the absolute maximum junction temperature of 125°C.

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Design Example

As a design example, consider using the LTC3548 in an portable application with a Li-Ion battery. The battery provides a V_{IN} = 2.8V to 4.2V. The load requires a maximum of 800mA in active mode and 2mA in standby mode. The output voltage is V_{OUT} = 2.5V. Since the load still needs power in standby, Burst Mode operation is selected for good low load efficiency.

First, calculate the inductor value for about 30% ripple current at maximum V_{IN}:

$$L \geq \frac{2.5V}{2.25MHz \bullet 240mA} \bullet \left(1 - \frac{2.5V}{4.2V}\right) = 1.9\mu H$$

Choosing a vendor's closest inductor value of 2.2µH, results in a maximum ripple current of:

$$\Delta I_L = \frac{2.5V}{2.25MHz \bullet 2.2\mu H} \bullet \left(1 - \frac{2.5V}{4.2V}\right) = 204mA$$

For cost reasons, a ceramic capacitor will be used. C_{OUT} selection is then based on load step droop instead of ESR requirements. For a 5% output droop:

$$C_{OUT} \approx 2.5 \frac{800mA}{2.25MHz \bullet (5\% \bullet 2.5V)} = 7.1\mu F$$

A good standard value is 10µF. Since the output impedance of a Li-Ion battery is very low, C_{IN} is typically 10µF.

The output voltage can now be programmed by choosing the values of R1 and R2. To maintain high efficiency, the current in these resistors should be kept small. Choosing 2µA with the 0.6V feedback voltage makes R1~300k. A close standard 1% resistor is 280k, and R2 is then 887k.

The $\overline{POR}$ pin is a common drain output and requires a pull-up resistor. A 100k resistor is used for adequate speed.

Figure 3 shows the complete schematic for this design example.

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3548. These items are also illustrated graphically in the layout diagram of Figure 4. Check the following in your layout:

1. Does the capacitor C_{IN} connect to the power V_{IN} (Pin 3) and GND (exposed pad) as close as possible? This capacitor provides the AC current to the internal power MOSFETs and their drivers.
2. Are the C_{OUT} and L1 closely connected? The (–) plate of C_{OUT} returns current to GND and the (–) plate of C_{IN}.
3. The resistor divider, R1 and R2, must be connected between the (+) plate of C_{OUT} and a ground sense line terminated near GND (exposed pad). The feedback signals V_{FB} should be routed away from noisy components and traces, such as the SW line (Pins 4 and 7), and its trace should be minimized.
4. Keep sensitive components away from the SW pins. The input capacitor C_{IN} and the resistors R1 to R4 should be routed away from the SW traces and the inductors.
5. A ground plane is preferred, but if not available, keep the signal and power grounds segregated with small signal components returning to the GND pin at one point and should not share the high current path of C_{IN} or C_{OUT}.
6. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to V_{IN} or GND.

APPLICATIONS INFORMATION

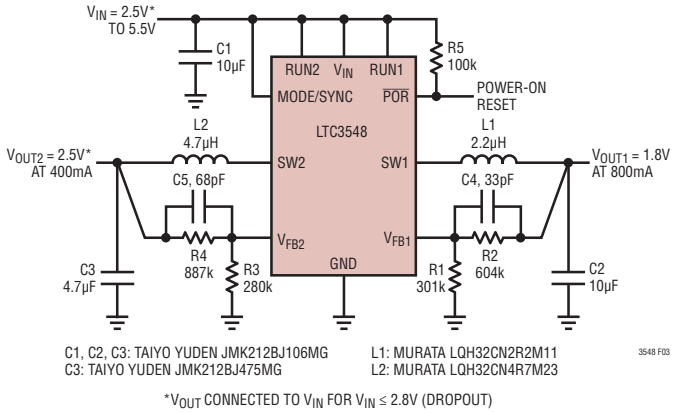


Figure 3. LTC3548 Typical Application

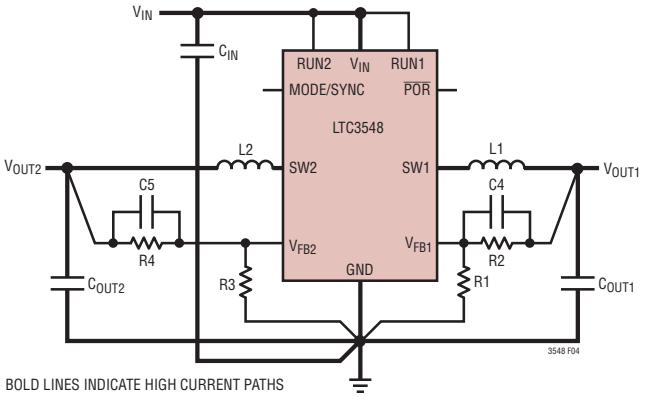
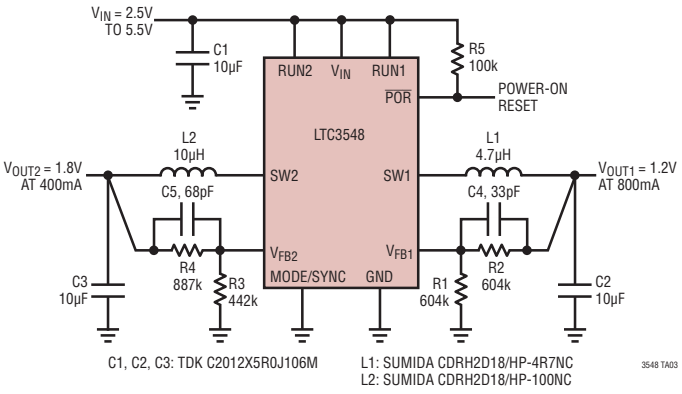


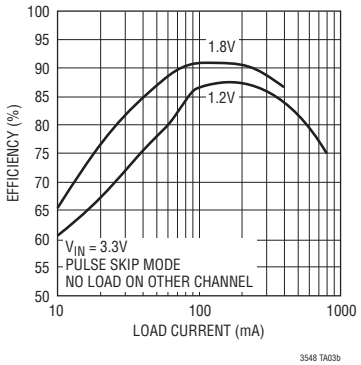
Figure 4. LTC3548 Layout Diagram (See Board Layout Checklist)

TYPICAL APPLICATIONS

Low Ripple Buck Regulators Using Ceramic Capacitors

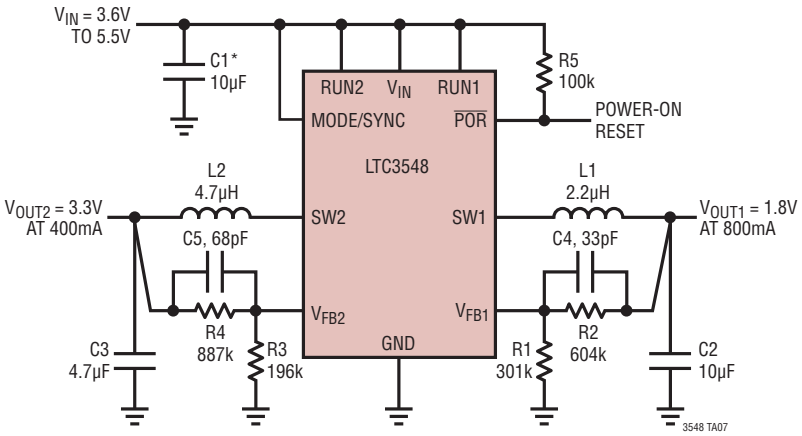


Efficiency vs Load Current



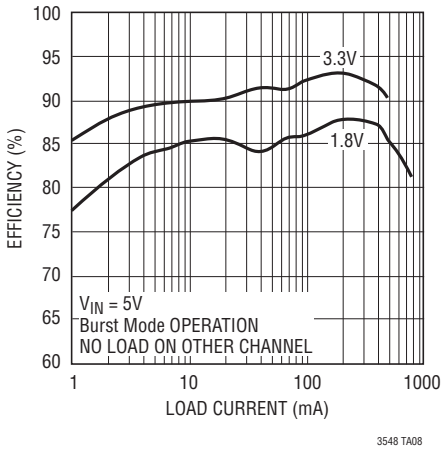
TYPICAL APPLICATIONS

1mm Profile Core and I/O Supplies



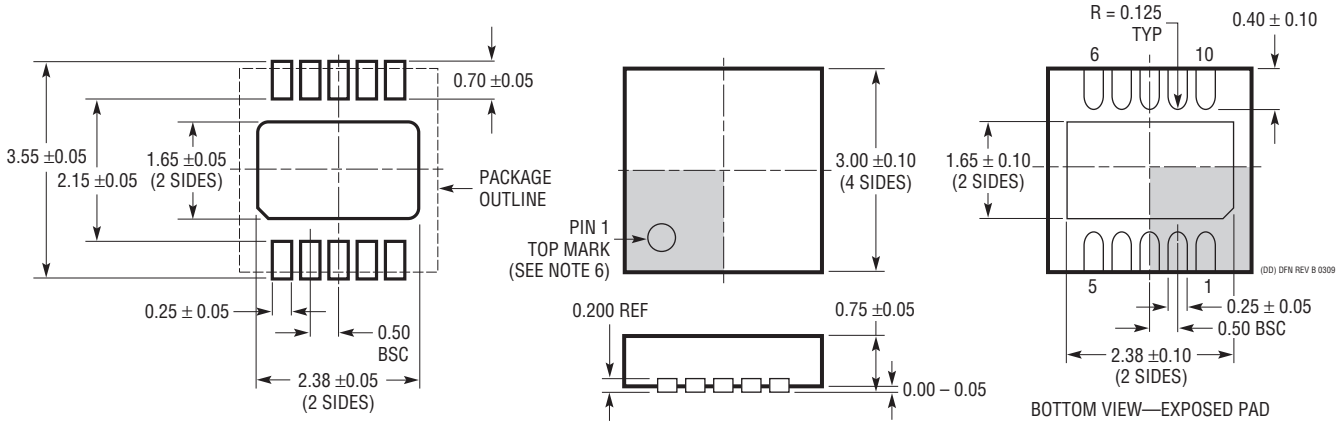
C1, C2: MURATA GRM219R60J106KE19
C3: MURATA GRM219R60J475KE19
L1: COILTRONICS LPO3310-222MX
L2: COILTRONICS LPO3310-472MX
*IF C1 IS GREATER THAN 3" FROM POWER SOURCE, ADDITIONAL CAPACITANCE MAY BE REQUIRED.

Efficiency vs Load Current



PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev B)

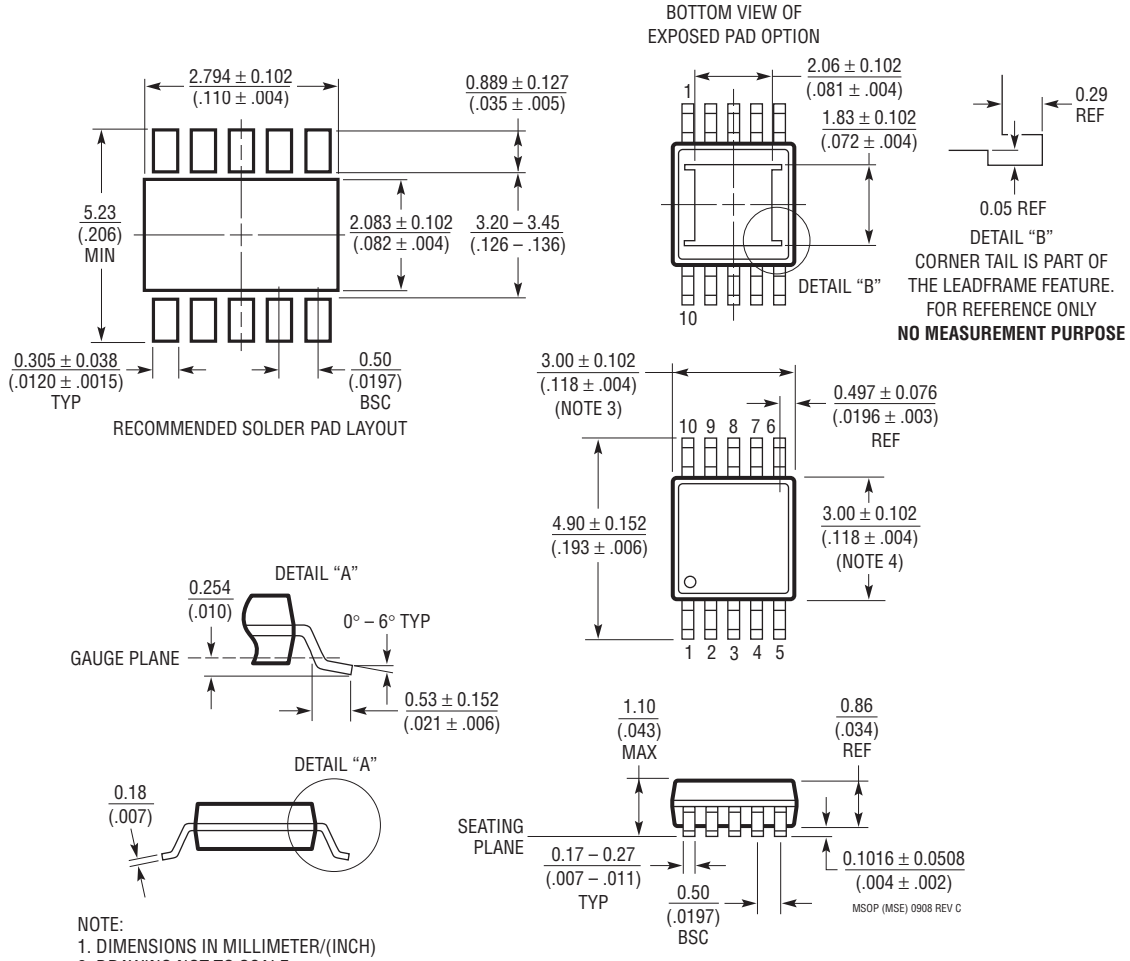


RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev C)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX