750MHz Gain of 1 Triple 2:1Video Multiplexer

FEATURES

- **750MHz –3dB Small Signal Bandwidth**
- **450MHz –3dB $2V_{P-P}$ Large-Signal Bandwidth**
- **120MHz ±0.1dB Bandwidth**
- **High Slew Rate: 2100V/µs**
- **Fixed Gain of 1; No External Resistors Required**
- 72dB Channel Separation at 10MHz
- 52dB Channel Separation at 100MHz
- –84dBc 2nd Harmonic Distortion at 10MHz, $2V_{P-P}$
- –87dBc 3rd Harmonic Distortion at 10MHz, $2V_{P-P}$
- Low Supply Current: 9.5mA per Amplifier
- 6.5ns 0.1% Settling Time for 2V Step
- $I_{SS} \leq 330\mu A$ per Amplifier When Disabled
- Differential Gain of 0.033%, Differential Phase of 0.022°
- Wide Supply Range: ±2.25V (4.5V) to ±6V (12V)
- Available in 24-Lead SSOP and 24-Lead QFN Packages

APPLICATIONS

- RGB Buffers
- UXGA Video Multiplexing
- LCD Projectors

DESCRIPTION

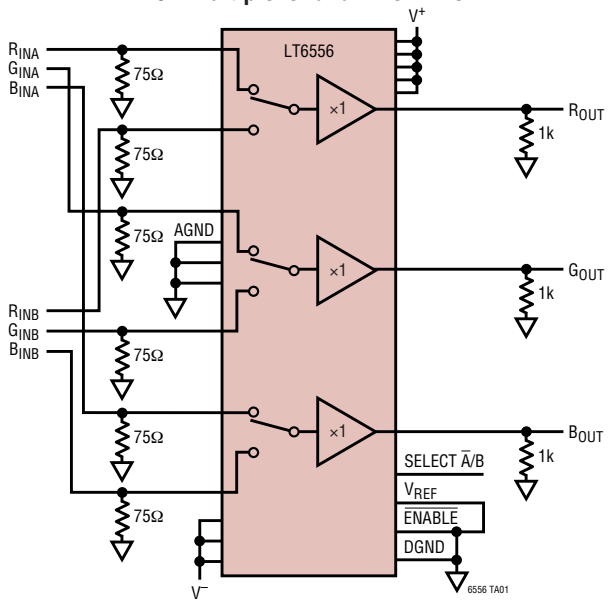
The LT®6556 is a high speed triple 2:1 video multiplexer with an internally fixed gain of 1. The individual buffers are optimized for performance with a 1k load and feature a $2V_{P-P}$ –3dB bandwidth of 450MHz, making them ideal for driving very high resolution video signals. Separate power supply pins for each amplifier boost channel separation to 72dB, allowing the LT6556 to excel in many high speed applications.

While the performance of the LT6556 is optimized for dual supply operation, it can also be operated with a single supply as low as 4.5V. Using dual 5V supplies, each amplifier draws only 9.5mA. When disabled, the amplifiers draw less than 330µA and the outputs become high impedance. For applications requiring a fixed gain of 2, refer to the LT6555 datasheet.

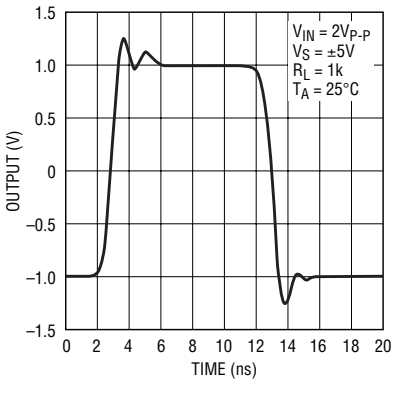
The LT6556 is available in 24-lead SSOP and ultra-compact 24-lead QFN packages.

TYPICAL APPLICATION

RGB Multiplexer and Line Driver



Large-Signal Transient Response

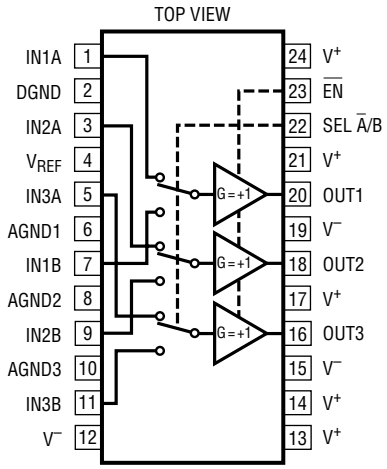


ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 12.6V
Input Current (Note 2) .....±10mA
Output Current (Continuous) .....±70mA
$\overline{EN}$ to DGND Voltage (Note 2) 5.5V
SEL to DGND Voltage (Note 2).....8V
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4) ... –40°C to 85°C
Specified Temperature Range (Note 5) .... –40°C to 85°C

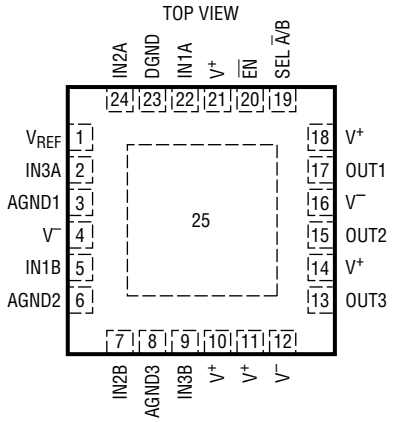
Junction Temperature
SSOP ..... 150°C
QFN..... 125°C
Storage Temperature Range
SSOP ..... –65°C to 150°C
QFN..... –65°C to 125°C
Soldering Temperature (10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
24-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 90°C/W



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 37°C/W, θ_{JC} = 2.6°C/W

EXPOSED PAD (PIN 25) IS V^-
MUST BE SOLDERED TO PCB

ORDER PART NUMBER	GN PART MARKING	ORDER PART NUMBER	UF PART MARKING*
LT6556CGN LT6556IGN	LT6556CGN LT6556IGN	LT6556CUF LT6556IUF	6556

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, R_L = 1k, C_L = 1.5pF, $V_{\overline{EN}}$ = 0.4V, V_{AGND}, V_{DGND}, V_{VREF} = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Offset Voltage	V_{IN} = 0V, V_{OS} = V_{OUT}	● ●		18	±67 ±75	mV mV
I_{IN}	Input Current		●		–12	±45	µA
R_{IN}	Input Resistance	V_{IN} = ±1V	●	100	500		kΩ
C_{IN}	Input Capacitance	f = 100kHz	●		1		pF
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±6V (Note 6)	●	51	62		dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, R_L = 1k, C_L = 1.5pF, V_{EN} = 0.4V, V_{AGND}, V_{DGND}, V_{VREF} = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{PSRR}	Input Current Power Supply Rejection	V_S = ±2.25V to ±6V (Note 6)	●		1	±3	µA/V
A_V ERR	Gain Error	V_{OUT} = V_{REF} = ±2V, Nominal Gain 1V/V	●	–2.8	–1.15	0	%
A_V MATCH	Gain Matching	Any One Channel to Another			±0.05		%
V_{OUT}	Output Voltage Swing	(Note 7)	●	±3.65	±3.85		V
I_S	Supply Current, Per Amplifier	R_L = ∞	 ●		9.5	13 14.5	mA mA
	Supply Current, Disabled, Per Amplifier	$V_{\overline{EN}}$ = 4V, R_L = ∞ $V_{\overline{EN}}$ = Open, R_L = ∞	● ●		47 42	330 330	µA µA
$I_{\overline{EN}}$	Enable Pin Current	$V_{\overline{EN}}$ = 0.4V $V_{\overline{EN}}$ = 4V	● ●	–200 –75	–95 –21		µA µA
I_{SEL}	Select Pin Current	V_{SEL} = 0.4V V_{SEL} = 4V	● ●	–50 –50	–5 –1		µA µA
I_{SC}	Output Short-Circuit Current	R_L = 0Ω, V_{IN} = ±2V, V_{REF} = ±1V	●	±50	±105		mA
SR	Slew Rate	±1V on ±2.2V Output Step (Note 8)		1200	2100		V/µs
–3dB BW	Small-Signal –3dB Bandwidth	V_{OUT} = 200mV_{P-P}			750		MHz
0.1dB BW	Gain Flatness ±0.1dB Bandwidth	V_{OUT} = 200mV_{P-P}			120		MHz
FPBW	Full Power Bandwidth 2V	V_{OUT} = 2V_{P-P} (Note 9)		190	335		MHz
	Full Power Bandwidth 4V	V_{OUT} = 4V_{P-P} (Note 9)			175		MHz
	All-Hostile Crosstalk	f = 10MHz, V_{IN} = 2V_{P-P} f = 100MHz, V_{IN} = 2V_{P-P}			–72 –52		dB dB
	Selected Channel to Unselected Channel Crosstalk	f = 10MHz, V_{IN} = 2V_{P-P} f = 100MHz, V_{IN} = 2V_{P-P}			–85 –64		dB dB
	Channel Select Output Transient	INA = INB = 0V			200		mV_{P-P}
	Channel-to-Channel Select Time	INA = –1V, INB = 1V from 50% SEL to V_{OUT} = 0V			8		ns
t_S	Settling Time	0.1% of V_{FINAL}, V_{STEP} = 2V			6.5		ns
t_R, t_F	Small-Signal Rise and Fall Time	10% to 90%, V_{OUT} = 200mV_{P-P}			500		ps
dG	Differential Gain	(Note 10)			0.056		%
dP	Differential Phase	(Note 10)			0.028		Deg
HD2	2nd Harmonic Distortion	f = 10MHz, V_{OUT} = 2V_{P-P}			–84		dBc
HD3	3rd Harmonic Distortion	f = 10MHz, V_{OUT} = 2V_{P-P}			–87		dBc

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: This parameter is guaranteed to meet specified performance through design and characterization. It is not production tested.

Note 3: As long as output current and junction temperature are kept below the Absolute Maximum Ratings, no damage to the part will occur. Depending on the supply voltage, a heat sink may be required.

Note 4: The LT6556C is guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 5: The LT6556C is guaranteed to meet specified performance from 0°C to 70°C. The LT6556C is designed, characterized and expected to meet specified performance from –40°C and 85°C but is not tested or QA sampled at these temperatures. The LT6556I is guaranteed to meet specified performance from –40°C to 85°C.

Note 6: In order to follow the constraints for 4.5V operation for PSRR and I_{PSRR} testing at ±2.25V, the DGND pin is set to V^-, the $\overline{EN}$ pin is set to V^- + 0.4V, and the SEL pin is set to either V^- + 0.4V or V^- + 4V. At ±6V and all other cases, DGND is set to ground and the $\overline{EN}$ and SEL pins are referenced from it.

Note 7: The V_{REF} pin is set to 3V when testing positive swing and –3V when testing negative swing to ensure that the internal input clamps do not limit the output swing.

Note 8: Slew rate is 100% production tested using both inputs of channel 2. Slew rates of channels 1 and 3 are guaranteed through design and characterization.

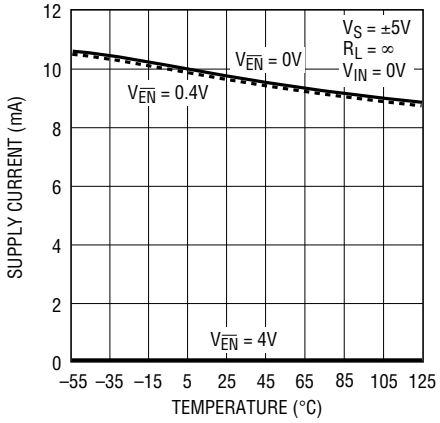
Note 9: Full power bandwidth is calculated from the slew rate:

$FPBW = SR/(\pi \bullet V_{P-P})$

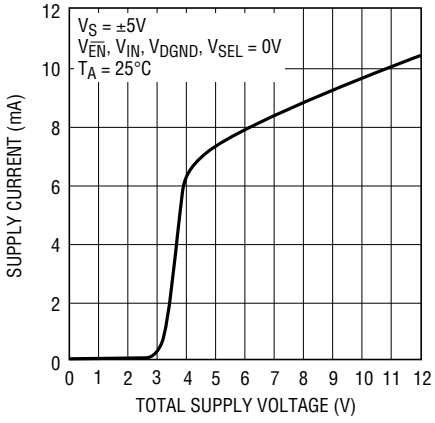
Note 10: Differential gain and phase are measured using a Tektronix TSG120YC/NTSC signal generator and a Tektronix 1780R video measurement set. The resolution of this equipment is better than 0.05% and 0.05°. Nine identical amplifier stages were cascaded giving an effective resolution of better than 0.0056% and 0.0056°.

TYPICAL PERFORMANCE CHARACTERISTICS

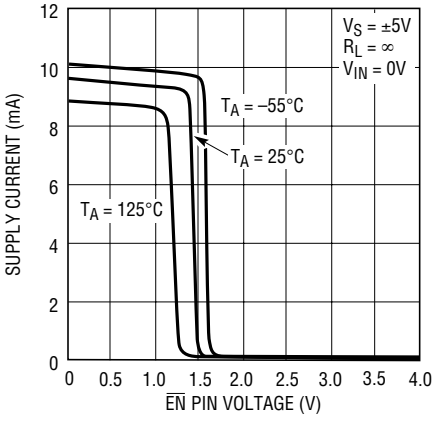
Supply Current per Amplifier vs Temperature



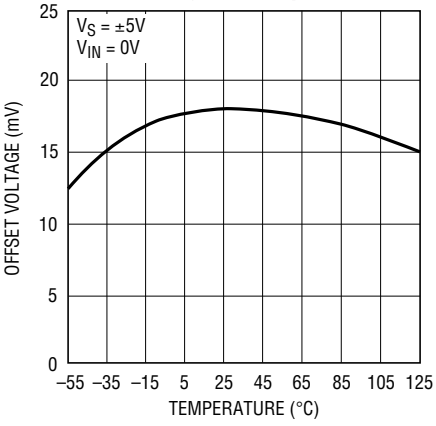
Supply Current per Amplifier vs Supply Voltage



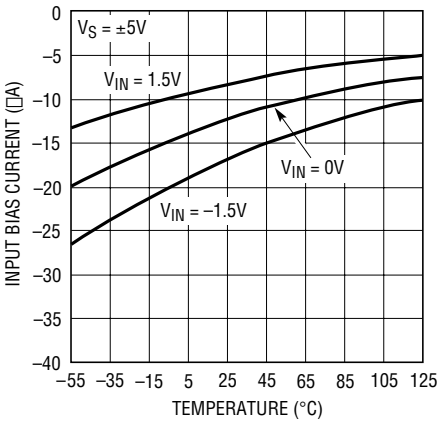
Supply Current per Amplifier vs EN Pin Voltage



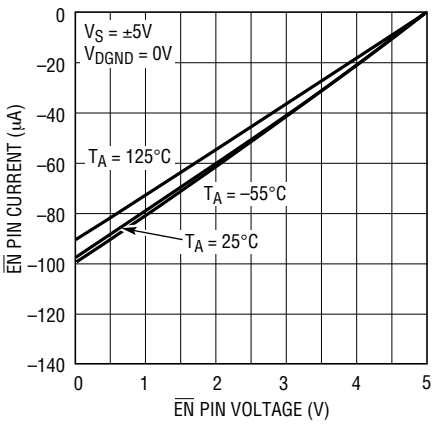
Offset Voltage vs Temperature



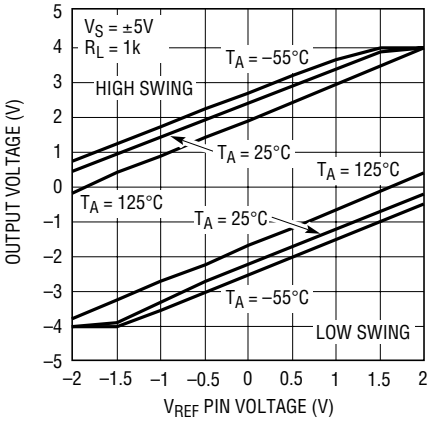
Input Bias Current vs Temperature



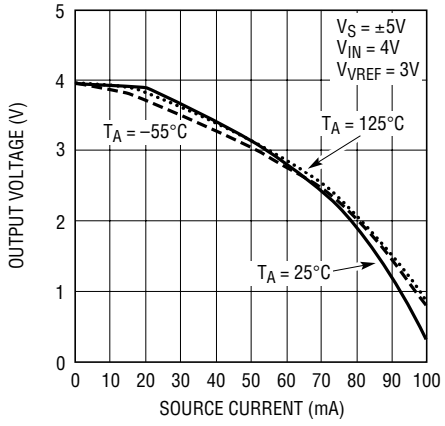
EN Pin Current vs EN Pin Voltage



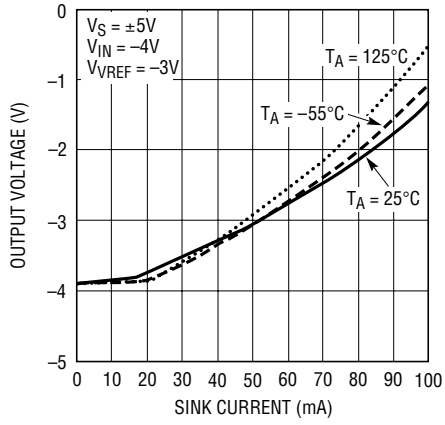
Maximum Output Voltage Swing vs V_{REF} Pin Voltage



Output Voltage Swing vs I_{LOAD} (Output High)

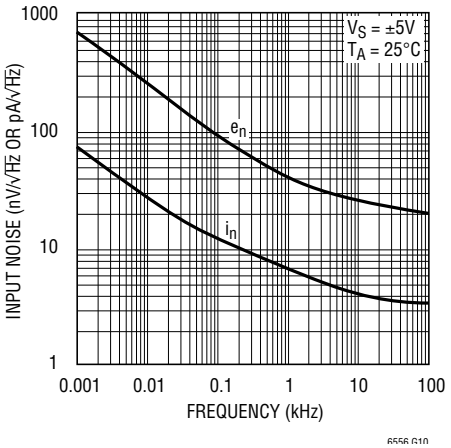


Output Voltage Swing vs I_{LOAD} (Output Low)

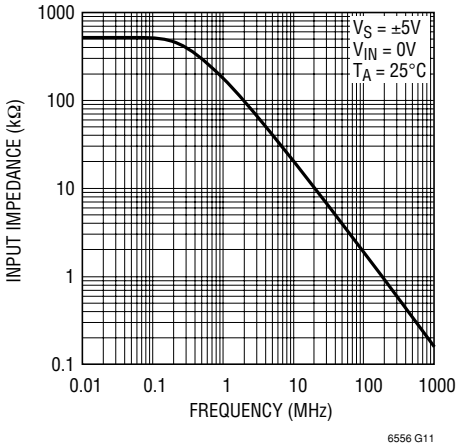


TYPICAL PERFORMANCE CHARACTERISTICS

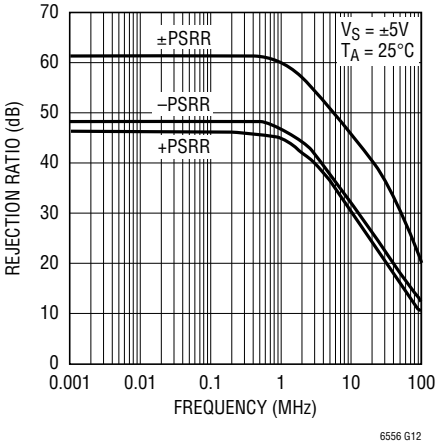
Input Noise Spectral Density



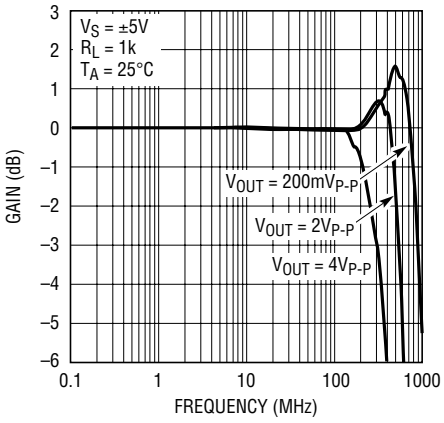
Input Impedance vs Frequency



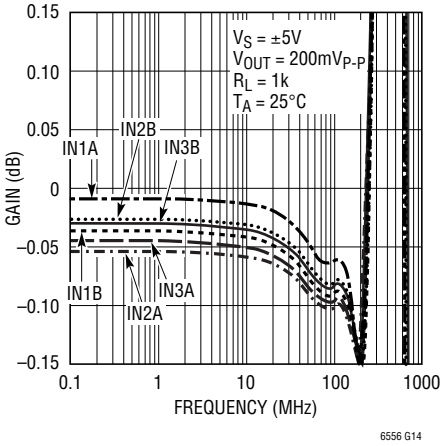
PSRR vs Frequency



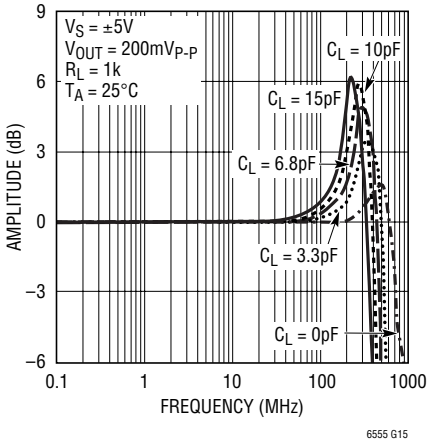
Frequency Response vs Output Amplitude



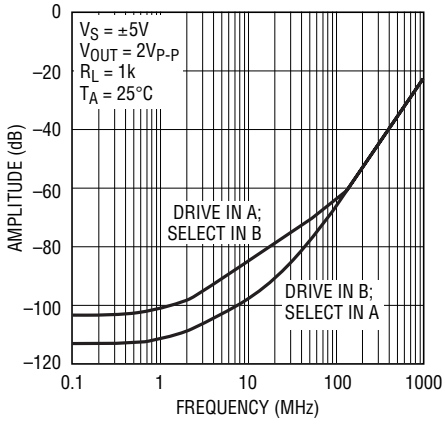
Gain Flatness vs Frequency



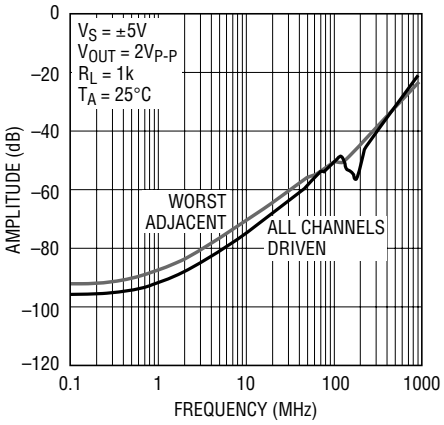
Frequency Response with Capacitive Loads



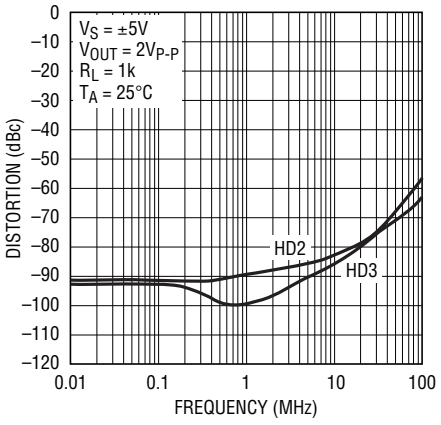
Crosstalk vs Frequency



Crosstalk vs Frequency

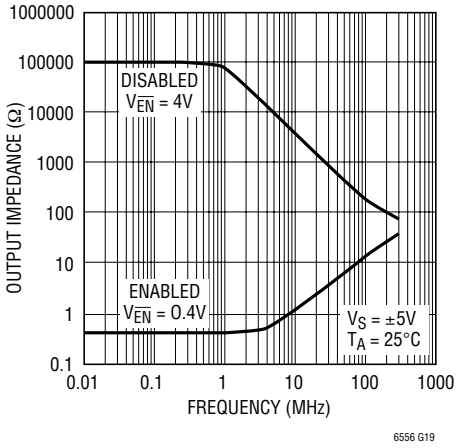


Harmonic Distortion vs Frequency

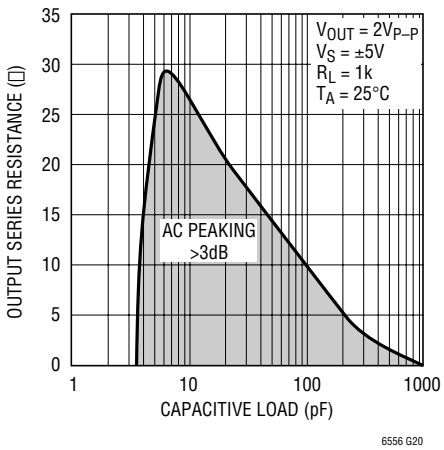


TYPICAL PERFORMANCE CHARACTERISTICS

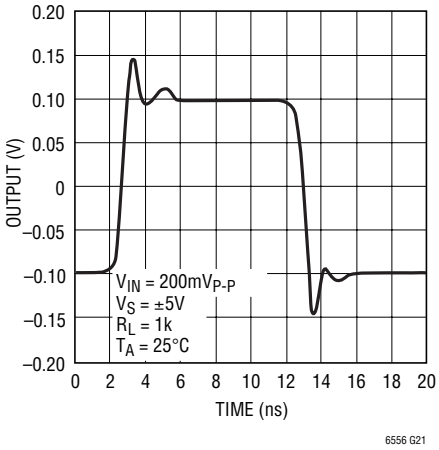
Output Impedance vs Frequency



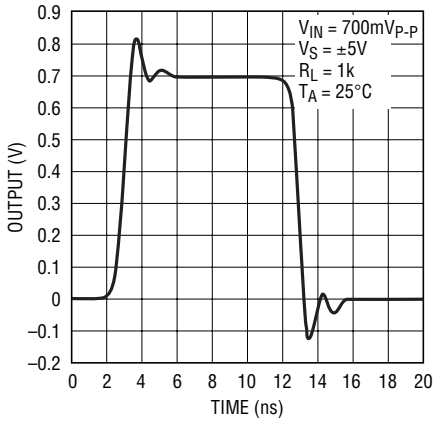
Maximum Capacitive Load vs Output Series Resistor



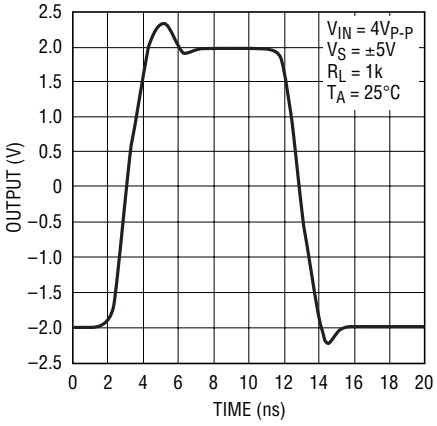
Small-Signal Transient Response



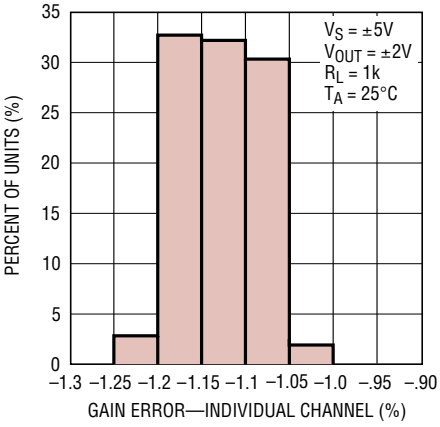
Video Amplitude Transient Response



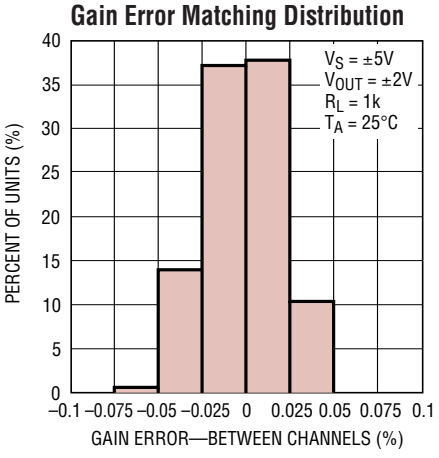
Large-Signal Transient Response



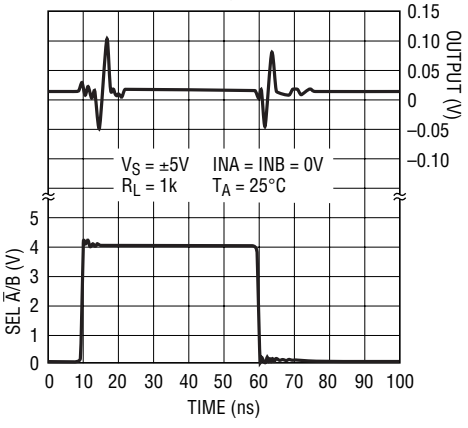
Gain Error Distribution



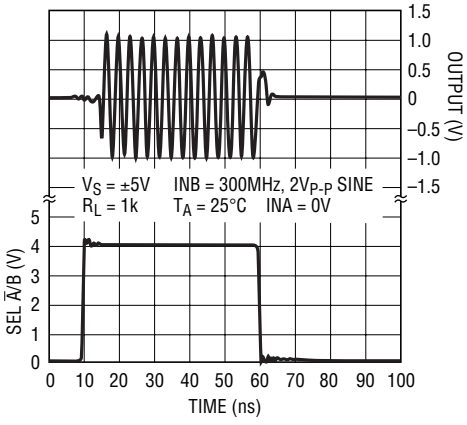
Gain Error Matching Distribution



Channel Switching Transient



Channel Switching Transient



PIN FUNCTIONS (GN24 Package)

IN1A (Pin 1): Channel 1 Input A. This pin has a nominal impedance of 500kΩ and does not have any internal termination resistor.

DGND (Pin 2): Digital Ground Reference for Enable Pin. This pin is normally connected to ground.

IN2A (Pin 3): Channel 2 Input A. This pin has a nominal impedance of 500kΩ and does not have any internal termination resistor.

VREF (Pin 4): Voltage Reference for Input Clamping. This is the tap to an internal voltage divider that defines mid-supply. It is normally connected to ground in dual supply, DC coupled applications.

IN3A (Pin 5): Channel 3 Input A. This pin has a nominal impedance of 500kΩ and does not have any internal termination resistor.

AGND (Pin 6): Analog Ground for Isolation between IN3A and IN1B. AGND pins have ESD protection and should not be connected to potentials outside the power supply range.

IN1B (Pin 7): Channel 1 Input B. This pin has a nominal impedance of 500kΩ and does not have any internal termination resistor.

AGND (Pin 8): Analog Ground for Isolation between IN1B and IN2B. AGND pins have ESD protection and should not be connected to potentials outside the power supply range.

IN2B (Pin 9): Channel 2 Input B. This pin has a nominal impedance of 500kΩ and does not have any internal termination resistor.

AGND (Pin 10): Analog Ground for Isolation between IN2B and IN3B. AGND pins have ESD protection and should not be connected to potentials outside the power supply range.

IN3B (Pin 11): Channel 3 Input B. This pin has a nominal impedance of 500kΩ and does not have any internal termination resistor.

V– (Pin 12): Negative Supply Voltage. V^- pins are not internally connected to each other and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

V+ (Pins 13, 14, 24): Positive Supply Voltage. V^+ pins are not internally connected to each other and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

V– (Pin 15): Negative Supply Voltage for Channel 3 Output Stage. V^- pins are not internally connected to each other and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

OUT3 (Pin 16): Channel 3 Output. It is the buffered output of the selected Channel 3 input.

V+ (Pin 17): Positive Supply Voltage for Channels 2 and 3 Output Stages. V^+ pins are not internally connected to each other and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

OUT2 (Pin 18): Channel 2 Output. It is the buffered output of the selected Channel 2 input.

V– (Pin 19): Negative Supply Voltage for Channels 1 and 2 Output Stages. V^- pins are not internally connected to each other and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

OUT1 (Pin 20): Channel 1 Output. It is the buffered output of the selected Channel 1 input.

V+ (Pin 21): Positive Supply Voltage for Channel 1 Output Stage. V^+ pins are not internally connected to each other and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

SEL $\overline{A}$/B (Pin 22): Select Pin. This high impedance pin selects which set of inputs are sent to the output pins. When the pin is pulled low, the A inputs are selected. When the pin is pulled high, the B inputs are selected.

$\overline{EN}$ (Pin 23): Enable Control Pin. An internal pull-up resistor of 46k defines the pin's impedance and will turn the part off if the pin is unconnected. When the pin is pulled low, the amplifiers are enabled.

Exposed Pad (Pin 25, QFN Only): The Exposed Pad is V^- and must be soldered to the PCB. It is internally connected to the QFN Pin 4, V^-.

APPLICATIONS INFORMATION

Power Supplies

The LT6556 is optimized for ±5V supplies but can be operated on as little as ±2.25V or a single 4.5V supply and as much as ±6V or a single 12V supply. Internally, each supply is independent to improve channel isolation. **Do not leave any supply pins disconnected or the part may not function correctly!**

Enable/Shutdown

The LT6556 has a shutdown mode controlled by the $\overline{EN}$ pin and referenced to the DGND pin. If the amplifier will be enabled at all times, the $\overline{EN}$ pin can be connected directly to DGND. If the enable function is desired, either driving the pin above 2V or allowing the internal 46k pull-up resistor to pull the $\overline{EN}$ pin to the top rail will disable the amplifier. When disabled, the output will become very high impedance. Supply current into the amplifier in the disabled state will be:

$$I_S = \frac{V^+ - V_{\overline{EN}}}{46k} + \frac{V^+ - V^-}{80k}$$

It is important that the following constraints on the DGND, $\overline{EN}$ and SEL pins are always followed:

$$V^+ - V_{DGND} \geq 4.5V$$
$$-0.5V \leq V_{\overline{EN}} - V_{DGND} \leq 5.5V$$
$$V_{SEL} - V_{DGND} \leq 8V$$

In dual supply cases where V^+ is less than 4.5V, DGND should be connected to a potential below ground, such as V^-. Since the $\overline{EN}$ and SEL pins are referenced to DGND, they may need to be pulled below ground in those cases. However, in order to protect the internal enable circuitry, the $\overline{EN}$ pin should not be forced more than 0.5V below DGND.

In single supply applications above 5.5V, an additional resistor may be needed from the $\overline{EN}$ pin to DGND if the pin is ever allowed to float. For example, on a 12V single supply, a 33k resistor would protect the pin from floating too high while still allowing the internal pull-up resistor to disable the part.

On dual ±2.25V supplies, connecting the DGND pin to V^- is the only way of ensuring that $V^+ - V_{DGND} \geq 4.5V$.

The enable/disable times of the LT6556 are fast when driven with a logic input. Turn on (from 50% $\overline{EN}$ input to 50% output) typically occurs in less than 50ns. Turn off is slower, but is typically below 500ns.

Channel Select

The SEL pin uses the same internal threshold as the $\overline{EN}$ pin and is also referenced to DGND. When the pin is logic low, the channel A inputs are passed to the output. When the pin is logic high, the channel B inputs are passed to the output. The pin should not be floated but can be tied to DGND to force the outputs to always be channel A or to V^+ (when less than 8V) to force the outputs to always be channel B.

Truth Table

SEL $\overline{A}$/B	$\overline{EN}$	OUT
0	0	IN A
1	0	IN B
X	1	OFF

Input Considerations

The LT6556 uses input clamps referenced to the V_{REF} pin to prevent damage to the input stage on the unselected channel. Three transistors in series limit the input voltage to within three diode drops (±) from V_{REF}. V_{REF} is nominally set to half of the sum of the supplies by the 40k resistors. A simplified schematic is shown in Figure 1.

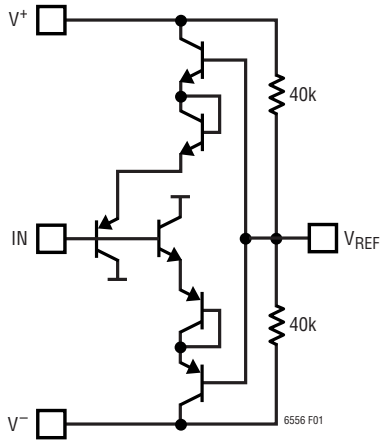


Figure 1. Simplified Schematic of V_{REF} Pin and Input Clamping

APPLICATIONS INFORMATION

To improve clamping, the pin's DC impedance should be minimized by connecting the V_{REF} pin directly to ground in the symmetric dual supply case with a common mode voltage of 0V. If the common mode voltage is not centered at ground or the input voltage exceeds plus or minus three diodes from ground, an external resistor to either supply can be added to shift the V_{REF} voltage to the desired level. The only way to cover the full input voltage range of V^- + 1V to V^+ – 1V is to shift V_{REF} up or down.

The V_{REF} pin can also be directly driven with a DC source. Figure 2 shows the effect of the clamp on input current when sweeping input voltage with various V_{REF} pin voltages. Bypassing the V_{REF} pin is not necessary.

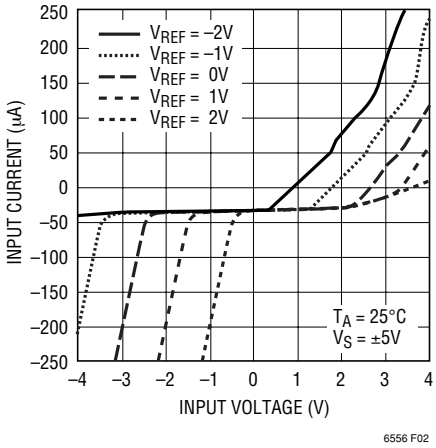


Figure 2. Input Current vs Input Voltage at Different V_{REF} Voltages

The inputs can be driven beyond the point at which the output clips so long as input currents are limited to less than ±10mA. Continuing to drive the input beyond the output limit can result in increased current drive and slightly increased swing, but will also increase supply current and may result in delays in transient response at larger levels of overdrive.

Layout and Grounding

It is imperative that care is taken in PCB layout in order to benefit from the very high speed and very low crosstalk of the LT6556. Separate power and ground planes are highly recommended and trace lengths should be kept as short as possible. If input traces must be run over a distance of several centimeters, they should use a controlled impedance with either series or shunt terminations (nominally 50Ω or 75Ω) to maintain signal fidelity.

Care should be taken to minimize capacitance on the LT6556's output traces by increasing spacing between traces and adjacent metal and by eliminating metal planes in underlying layers. To drive cable or traces longer than several centimeters, using the LT6555 with its fixed gain of+2 in conjunction with series and load termination resistors may provide better results.

A plot of AC performance driving a 1k load with various trace lengths is shown in Figure 3. All data is from a 4-layer board with 2oz copper, 18mil of board layer thickness to the ground plane, a trace width of 12mils and spacing to adjacent metal of 18mils. The 0.2cm output trace places the 1k resistor as close to the part as possible, while the other curves show the load resistor consecutively further away. The worst case, 4cm, trace has almost 10pF of parasitic capacitance.

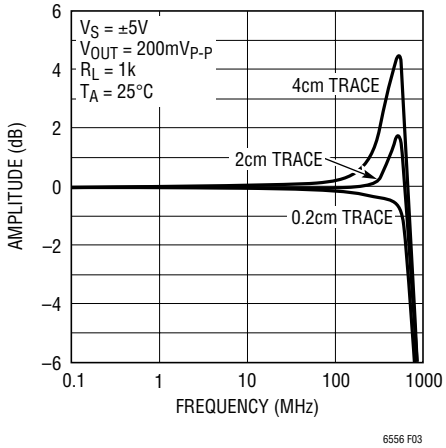


Figure 3. Response vs Output Trace Length

APPLICATIONS INFORMATION

In order to counteract any peaking in the frequency response from driving a capacitive load, a series resistance can be inserted in the line at the output of the part to flatten the response. Figure 4 shows the frequency response with the same 4cm trace from Figure 3, now with a 10Ω series resistor inserted near the output pin of the amplifier. Note that using a 10Ω series resistor with a 1k load only decreases the output amplitude by 0.1dB or 1% and has a minimal effect on the bandwidth of the system. See the graph labeled "Maximum Capacitive Load vs Output Series Resistor" in the Typical Performance Characteristics section for more information.

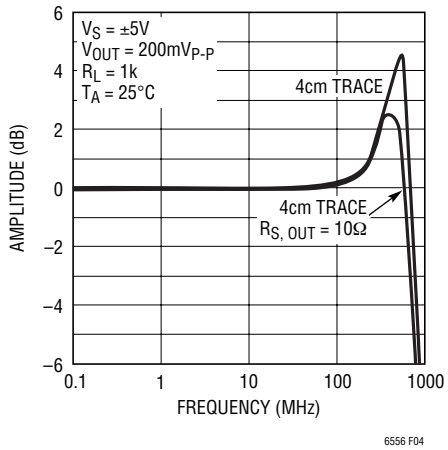


Figure 4. Response vs Series Output Resistance

While the AGND pins on the LT6556 are not connected to the amplifier circuitry, tying them to ground or another "quiet" node significantly increases channel isolation and is always recommended. The AGND pins do have ESD protection and therefore should not be connected to potentials outside the power supply range.

Low ESL/ESR bypass capacitors should be placed as close to the positive and negative supply pins as possible. One 4700pF ceramic capacitor is recommended for both V^+ and V^- supply busses. Additional 470pF ceramic capacitors with minimal trace length on each supply pin will further improve AC and transient response as well as channel isolation. For high current drive and large-signal transient applications, additional 1µF to 10µF tantalums should be added on each supply. The smallest value capacitors should be placed closest to the package.

To maintain the LT6556's channel isolation, it is beneficial to shield parallel input and parallel output traces using a ground plane or power supply traces. Vias between topside and backside metal may be required to maintain a low inductance ground near the part where numerous traces converge. See Figures 7 and 8 for photos of an optimized layout.

Single Supply Operation

Figure 5 illustrates how to use the LT6556 with a single supply ranging from 4.5V to 12V. Since the output range is comparable to the input range, the DC bias point at the input can be set anywhere between the supplies that will prevent the AC-coupled signal from running into the output range limits. As shown, the DC input level is mid-supply.

The only additional power dissipation in the single supply configuration is through the resistor bias string at the input and through any load resistance at the output. In many cases, the output can be used to directly drive other single supply devices without additional coupling and without any resistive load.

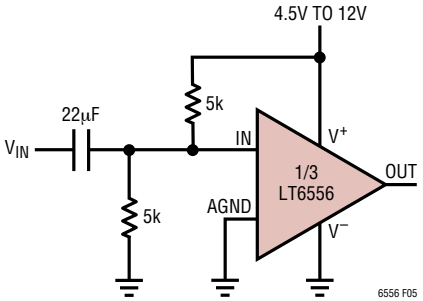


Figure 5. Single Supply Configuration, One Channel Shown

Input Expansion

In applications with more than two inputs per channel, multiple LT6556s can be connected directly together at the outputs. Logic circuitry can be used to drive the $\overline{EN}$ pins of each LT6556 to ensure that only one set of channels is buffered at a time. See Figure 9 for a schematic.

Since the output impedance of a disabled LT6556 is high, adding additional channels will not resistively load an

APPLICATIONS INFORMATION

enabled output. However, since the disabled LT6556 and its traces have around 6pF of capacitance, it may be desirable to resistively isolate the outputs of each channel to maintain flat frequency response as shown in the graph labeled "Maximum Capacitive Load vs Output Series Resistor" in the Typical Performance Characteristics section.

ESD Protection

The LT6556 has reverse-biased ESD protection diodes on all pins. If any pins are forced a diode drop above the positive supply or a diode drop below the negative supply, large currents may flow through these diodes. If the current is kept below 10mA, no damage to the devices will occur.

TYPICAL APPLICATION

RGB Multiplexer Demo Board

The DC892A Demo Board illustrates optimal routing, bypassing and termination using the LT6556 as an RGB video multiplexer. The schematic is shown in Figure 6. All inputs and outputs are routed to have a characteristic impedance of 75Ω and 75Ω input shunt and output series terminations are connected as close to the part as possible. The board is fabricated with four layers with internal ground and power planes.

While the 75Ω back termination resistors at the outputs of the LT6556 minimize signal reflections in the output traces and isolate the part from any capacitive loading in those traces, they also contribute to gain error if the output is not terminated with high impedance. For example, if the output is terminated with a 1k load, the 75Ω back termination will cause a 7% gain error. Decreasing the value of the back termination resistors will decrease the signal attenuation but may compromise the AC response. However, connecting the LT6556 output pins to the output traces on the DC892A board without some series resistance is not recommended; 10Ω to 20Ω is generally sufficient. Figures 7 and 8 show the top and bottom side board layout and placement.

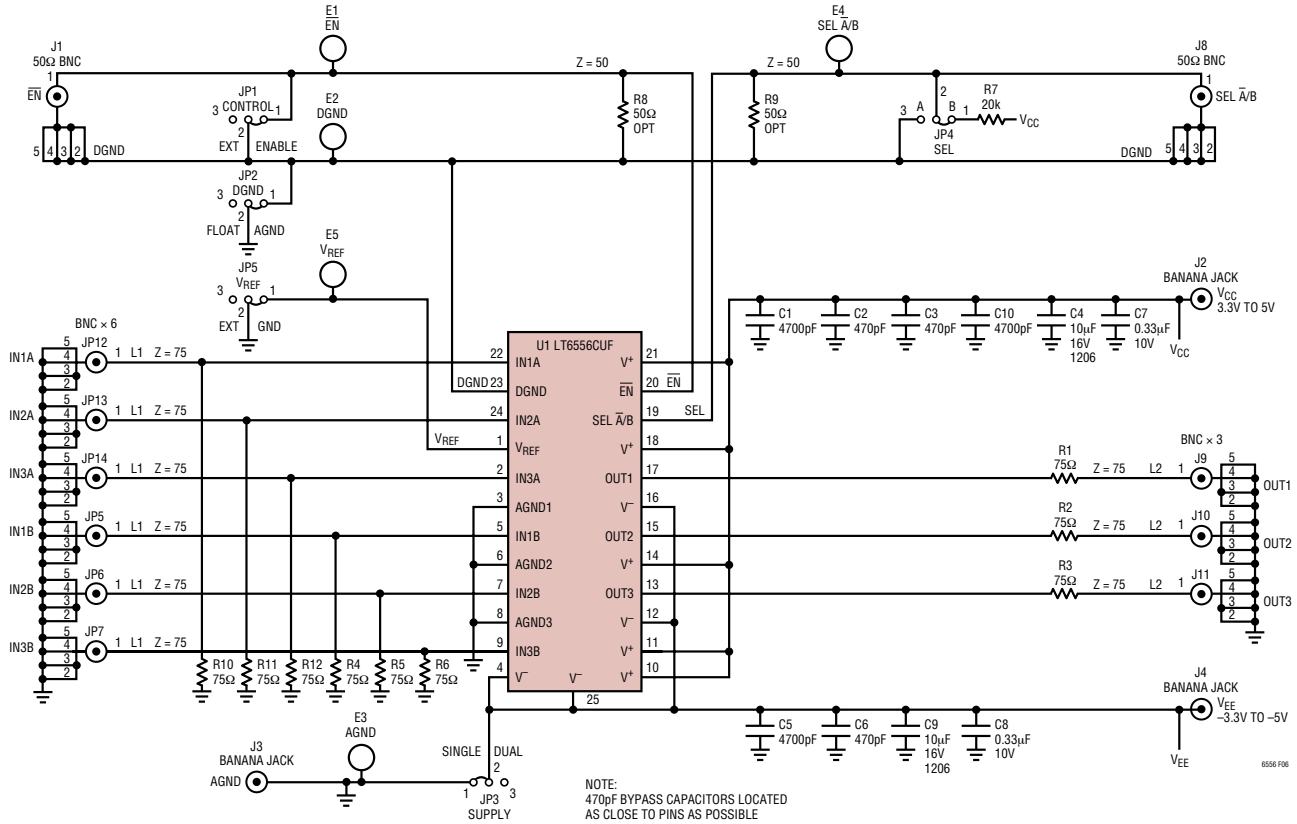


Figure 6. Demo Board Schematic

TYPICAL APPLICATION

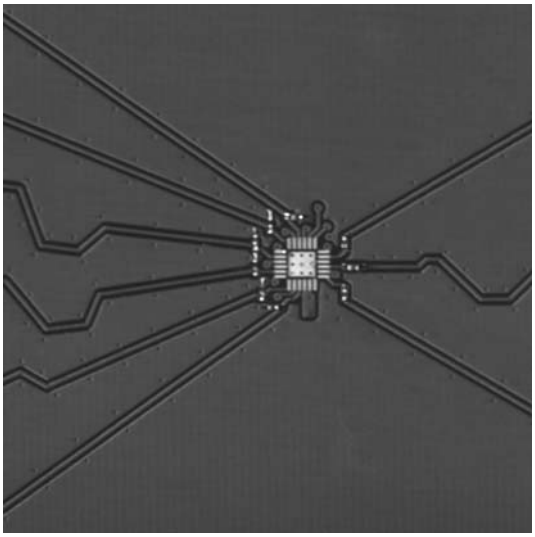


Figure 7. Demo Board Topside
(IC Removed for Clarity)

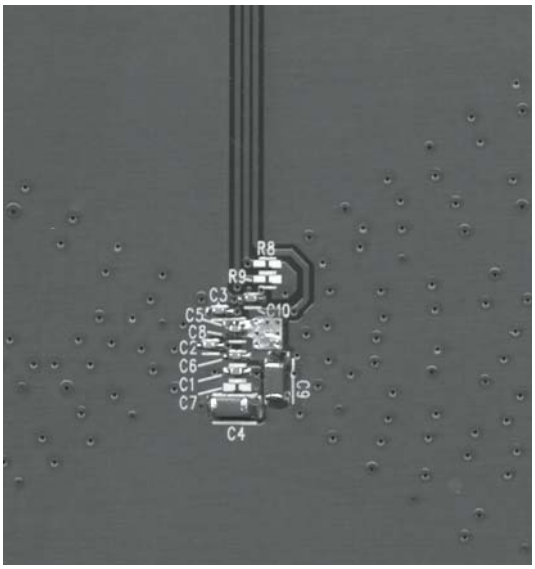
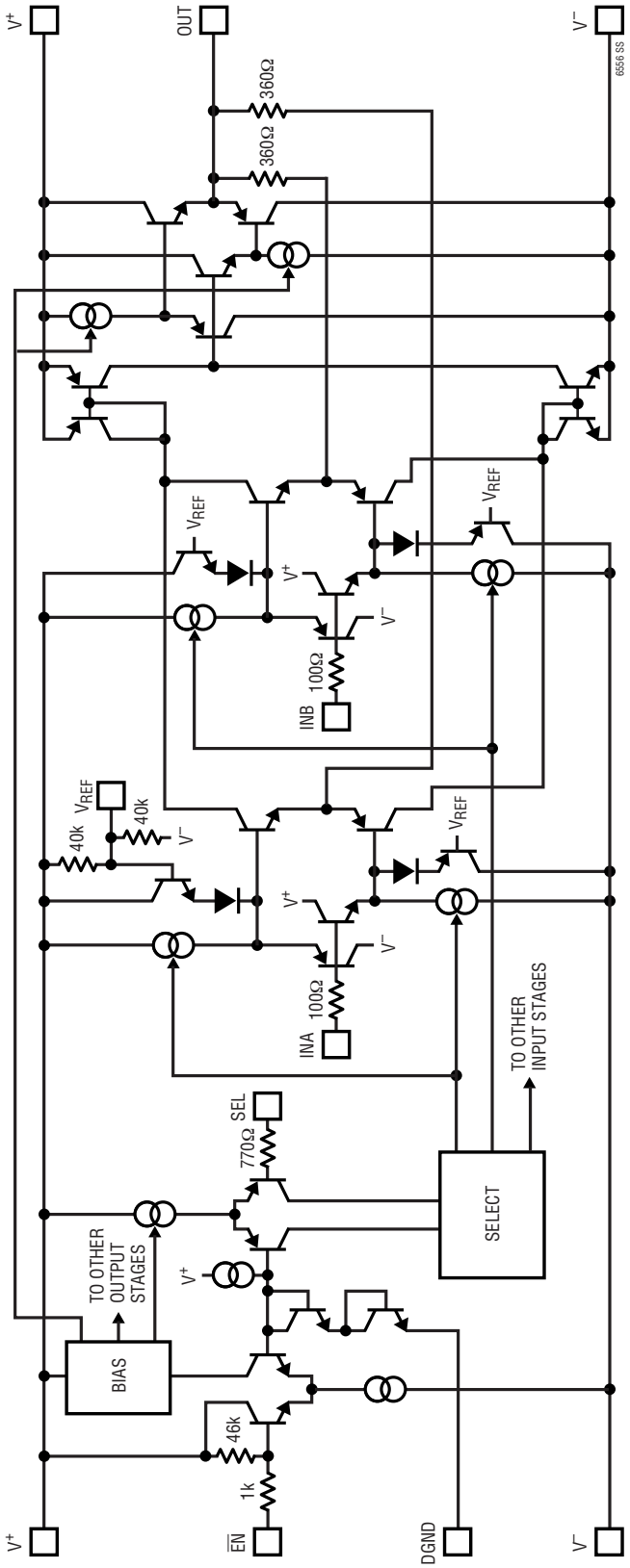


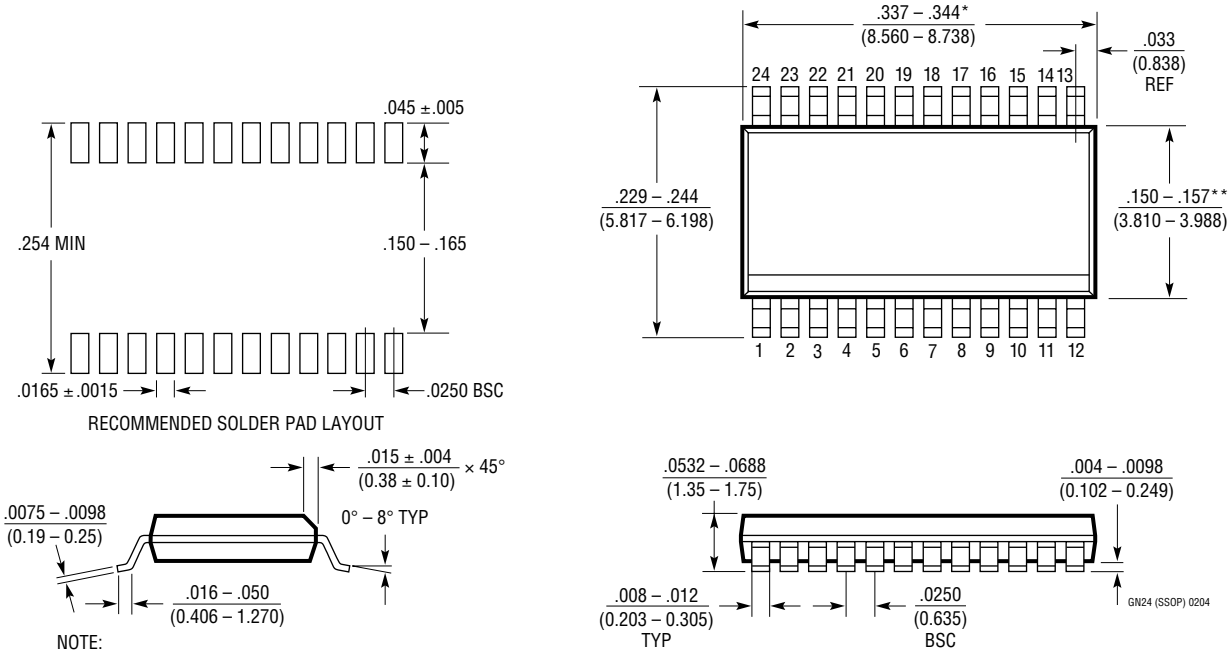
Figure 8. Demo Board Bottom Side

SIMPLIFIED SCHEMATIC (One channel shown)



PACKAGE DESCRIPTION

GN Package
24-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



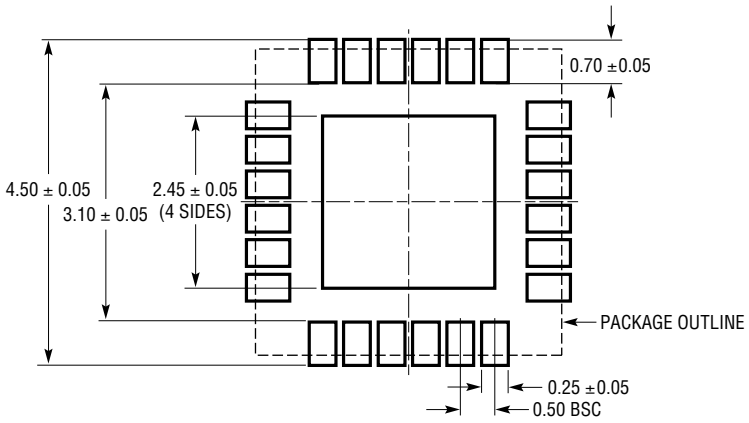
NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

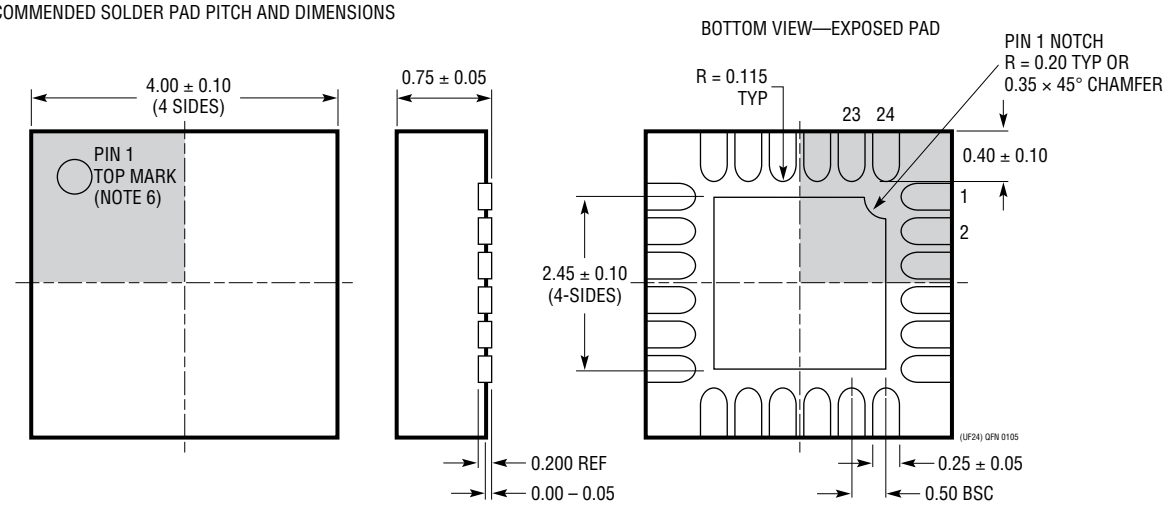
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE